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Analysis of TID Process, Geometry, and Bias Condition Dependence of 14-nm FinFETs and Implications for RF and SRAM Performance

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ABSTRACT:

TID results of 14-nm FinFETs is presented. High-V_{th} FinFETs show the best post-irradiation characteristics. The SRAM on-state is the worst-case irradiation bias condition. nMOSFET pull-down and pass-gate devices show less TID degradation than low-V_{th} devices.

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***Abstract*— Total ionizing dose results are provided, showing the effects of the process considerations, geometry, and irradiation bias condition of 14-nm FinFETs. Minimal threshold voltage shift across a variety of transistor types is observed. Off-state leakage current of nMOSFET transistors (I_{ds} at V_{gs} = 0 V) exhibits a strong gate dependence, indicating electrostatic gate control of the sub-Fin region and the corresponding parasitic conduction path are the largest concern for radiation hardness in FinFET technology. The high-V_{th} transistors exhibit the best post-irradiation performance across all bias conditions, showing a reasonably small change of $I_{ds,off}$ and V_{th}, while the low-V_{th} transistors exhibit a larger response in $\Delta I_{ds,off}$. The "worst-case" bias condition during irradiation for both pull-down and pass-gate nMOSFETs in static random access memory is determined to be the on-state ($V_{gs} = V_{dd}$). We find the nMOSFET pull-down and pass-gate transistors of the SRAM bit-cell show less TID degradation due to transistor geometry and channel doping than the low-V_{th} transistor. The implications of near-threshold operation are presented as a methodology for reducing TID-induced increases in off-state device leakage.**

***Index Terms*— FinFET, Total Ionizing Dose, threshold voltage shift, leakage current**

I. Introduction

Migration of commercial complementary metal-oxide-semiconductor (CMOS) technology to FinFETs has allowed continued scaling below 20-nm gate length feature sizes. In addition to scaling advantages that FinFETs have over traditional planar CMOS devices, they also exhibit reduced short-channel effects, improved electrostatic control over the channel, better subthreshold slope, higher mobility, and reduction in bias-temperature instability and hot-carrier effects [1]. Naturally, the availability of advanced CMOS has resulted in a desire to use the technology in a variety of applications, including terrestrial, aerospace, and military. A key concern for space-based applications is the impact of total ionizing dose (TID) on device performance, which may degrade critical device operating characteristics such as *off*-state leakage (I_{leak}), threshold voltage (V_{th}), subthreshold slope, mobility (μ_n), and transconductance (g_m).

Several groups have previously evaluated development level bulk and silicon-on-insulator (SOI) FinFET technologies with regards to TID effects [2], [3]; however, to date there has been little work done on devices with gate length feature sizes below 20-nm. An initial comparison of the TID response of a representative 14-nm FinFET technology based on bulk and SOI was recently presented [2]. From that limited data, FinFETs showed promise as a viable solution for a radiation-hard leading-edge technology.

In this work we improve on previous reports [2] with a new focus on an in-depth evaluation of the device-level response of a 14-nm bulk FinFET process to TID. In doing so, we investigate the impact of device integration (i.e. spacing and design rules), device threshold voltage, transistor geometry, and irradiation bias configuration on the TID response of a set of discrete transistors in a commercial 14-nm process. In doing so, we consider the influence of all of these parameters on the operation of nMOSFET devices in the configuration of a functional ring oscillator and SRAM bit-cell. We will follow up the experimental results reported here with simulation based efforts to be presented at the conference and discussed in the full paper. The implications of near-threshold operation are presented as a methodology for reducing TID-induced increases in *off*-state device leakage.

II. Device Details and Experimental Methods

The discrete nMOSFET devices evaluated in this work are from a commercial CMOS 14-nm bulk FinFET process. We include a schematic image of a typical FinFET device in cross-section and 3-D in Fig. 1 [4] for illustrative purposes. The FinFET devices are made using a metal gate process with high-κ dielectric. Isolation of the Fin is achieved by use of channel stop doping (CSD) in the sub-Fin region and shallow trench isolation (STI). Three main types of discrete nMOSFET transistors used in the layout of logic circuitry in the technology were evaluated. These transistors were fabricated to have a low, medium, or high threshold voltage. Each of the discrete logic transistors tested are implemented as 2-fin transistors with a constant effective W/L ratio and 14-nm minimum gate length features. Additionally, high threshold voltage discrete pull-down (PD) and pass-gate (PG) transistors that are representative of those used in nominal SRAM bit-cells for the 14-nm FinFET technology (i.e., have the same design rules, spacing, and materials) were also evaluated in this work. These discrete SRAM transistors are externally accessible for

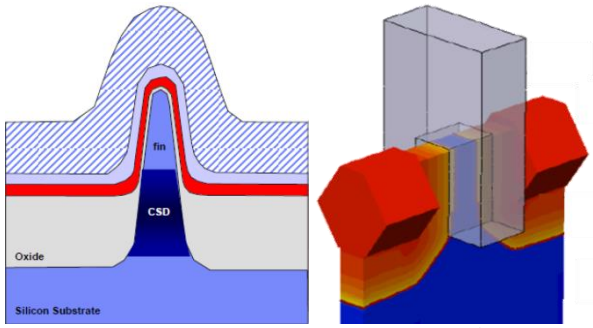

Fig. 1. Schematic cross-section and 3-D representation of bulk FinFET devices representative of devices evaluated in this work. After [4].

electrical characterization. These five types of discrete transistors are representative of basic components found in any CMOS process and account for design considerations of each specific test structure, making them highly-relevant, ideal test vehicles for radiation studies.

Initial characterization was performed through I_{ds}-V_{gs} measurements with low applied drain voltage (V_{ds} = 50 mV), allowing extraction of device operating characteristics such as V_{th}, $I_{ds,off}$, $I_{ds,on}$, and $g_{m,max}$. Here, we define V_{th} using the linear region approximation, $I_{ds,off}$ as the drain current measured at V_{gs} = 0 V, $I_{ds,on}$ as the drain current at V_{gs} = 900 mV, and $g_{m,max}$ as max(dI_{ds}/dV_{gs}). Devices were irradiated with a 10 keV x-ray source (ARACOR 4100) at a dose rate of 525 rad(SiO_2)/s. During irradiation, devices under test (DUT) were placed into a static operating condition representative of nMOSFET drain high (V_{ds} = 1.0 V, V_g = V_b = V_s= 0 V; *off*-state), gate high (V_{gs} = 1.0 V, V_d = V_b = V_s = 0 V; *on*-state), and a near-threshold operating condition (V_{gs} = 0.5 V, V_d = V_b = V_s= 0 V; *half-on*-state). The device response in the so-called "half-on"-state is of interest for the benefits associated with reduced power consumption or quiescent device operation. Following irradiation, final I_{ds}-V_{gs} characterization is performed and all device parameters are again extracted for comparison with pre-irradiation data.

III. Experimental Results

A. Irradiation Bias Condition Dependence

Fig. 2 shows I_{ds}-V_{gs} characteristics representative of the low-V_{th} device for devices irradiated in the *off*- (2 (a)), *on*- (2 (b), and *half-on*-state (2 (c)). Several features present in the *I-V* curves warrant discussion. The radiation-induced shift in $I_{ds,off}$ and V_{th} for all three irradiation bias conditions is shown in Fig. 3.

First, the most dramatic impact of TID on device performance is clearly the modulation of *off*-state leakage current, $I_{ds,off}$ with increasing dose. The change in *off*-state leakage is not simply a static increase in drain current but has a strong dependence on the applied gate voltage. This is consistent with previous reports [2], [3] that attribute TID-induced leakage currents to charge accumulation in the STI near the sub-Fin region of the device that contains the CSD or super-steep retrograde well (SSRW) [5]. Second, the change in V_{th} is observed to be minimal with a corresponding trend in the $I_{ds,on}$ parameter (not shown). The typical change in threshold voltage seems to be on the order of 30-50 mV at a total dose of 1 Mrad(SiO_2) with a corresponding 3-5 % change in total drive

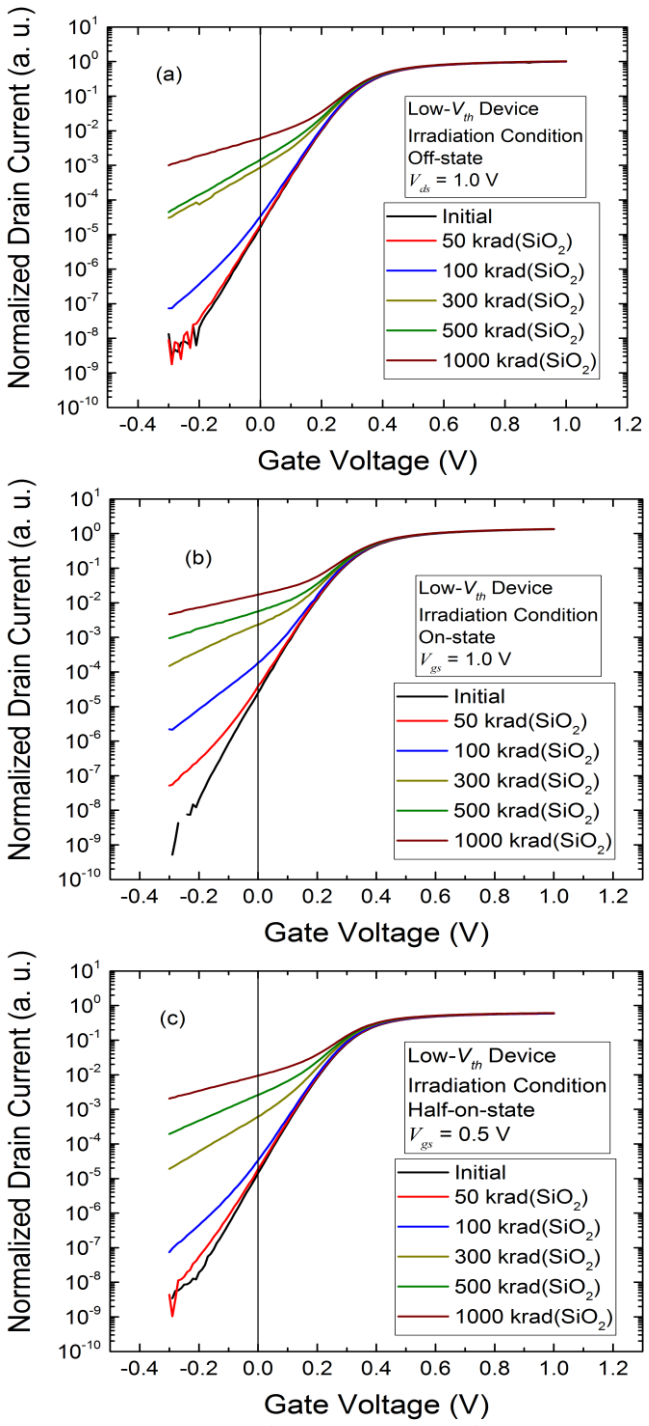

Fig. 2. I_{ds}-V_{gs} characterization for varying total dose of the low-V_{th} device for devices irradiated in the *off*- (a), *on*- (b), and *half-on*-state (c).

current in the *on*-state with a low drain bias (V_{ds} = 50 mV). Lastly, the collapse of the $I_{ds,on}/I_{ds,off}$ current ratio following irradiation from ~10^7 pre-irradiation to closer to 10^2-10^3 at 1 Mrad(SiO_2), depending on the irradiation bias condition. The change in $I_{ds,on}/I_{ds,off}$ ratio preferentially impacts *n*MOSFET devices, with implications for timing of digital circuits due to the resulting drain current drive mismatch between *n*- and *p*-channel devices. Additionally, overall static and dynamic current dissipation of the device will increase significantly, impacting logic states in digital and memory applications.

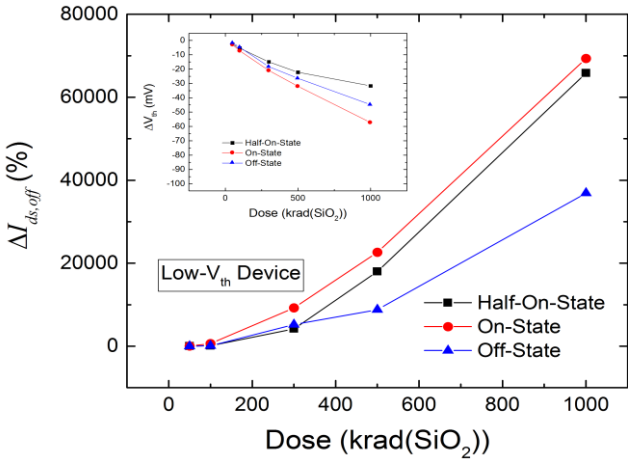

Fig. 3. Percent change in $I_{ds,off}$ as a function of dose for the low-V_{th} device indicates the worst-case bias condition for FinFET logic transistors is the *on*-state condition. The inset shows the ΔV_{th} vs dose exhibits a moderate negative shift.

Clearly, the magnitude of change in *off*-state leakage current is dependent on the bias condition during irradiation with the most dramatic shift occurring for the nMOSFET in the *on*-state with the gate high. For the low-V_{th} device, this can be slightly mitigated in part by employing a reduced supply voltage condition, as seen in Fig. 2 (c). Intuitively, a lower operating voltage should result in lower electric fields that will reduce charge yield in the STI and impact charge trapping in the STI dielectric material. A reduction in operating voltage has the obvious advantage of reducing power dissipation and enabling more energy efficient applications for near-threshold computing [6] or dynamic voltage and frequency scaling [7], of particular use when power and not speed is a primary design consideration.

B. TID Response of Low-V_{th} vs High-V_{th} Devices

In Fig. 4 we show the radiation-induced change in *off*-state leakage for low-V_{th} as compared to high-V_{th} devices irradiated in the *on*- (4 (a)), *off*- (4 (b)) and *half-on* (4 (c)) bias conditions. The high-V_{th} device shows a significantly smaller response in $\Delta I_{ds,off}$ post-irradiation than the low-V_{th} device for all bias conditions evaluated in this work. This is presumably due to higher Fin doping and threshold adjust implant of the high-V_{th} device and differences in the CSD and SSRW device isolation required to achieve a higher V_{th} device as compared to the low-V_{th} device. Conceptually, higher body doping would require more charge trapping in the STI dielectric than what is required for a lower body doping to deplete and invert the STI side-wall transistor. Consistent with the results observed in the previous section, we see the *on*-state irradiation condition induces the worst case parasitic leakage current response for both the low-V_{th} and high-V_{th} device. We note that the half-on state does represent a marginal improvement in the post-irradiation TID response of these devices for both the high and low-V_{th} devices. Intuitively, a lower operating voltage should result in smaller electric fields and impact the charge yield and trapping behavior for the gate and STI dielectrics. The reduction in trapped charge, in turn, has a less of an impact on devices with higher threshold voltage adjust implant, requiring a higher total dose to deplete and eventually invert the sidewall region.

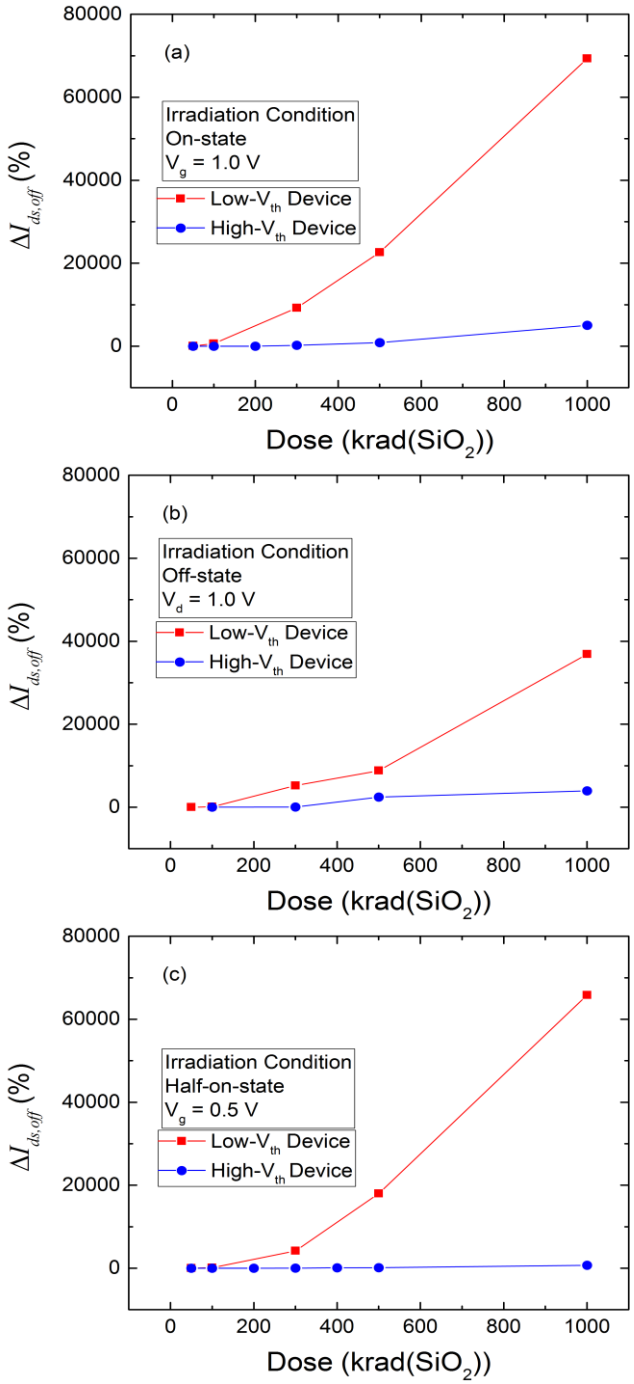

Fig. 4. Percent change in $I_{ds,off}$ as a function of dose for the low-V_{th} and high-V_{th} 14-nm FinFET devices in the *off*- (a), *on*- (b), and *half-on*-state (c) during irradiation shows the worst-case bias condition for leakage current response is the *on*-state condition. The higher threshold voltage device shows a less severe response for all bias conditions.

The threshold voltage of high-V_{th} transistors as a function of dose (not shown) is observed to shift negative roughly 30-50 mV at 1 Mrad(SiO$_2$). We do not observe a significant change in $g_{m,max}$ of any of the devices evaluated and presented in this work, suggesting that the electrostatics and carrier transport processes responsible for conduction in the channel itself are largely unperturbed following accumulation of TID, other than some small change in threshold voltage. $\Delta I_{ds,on}$ shifts are consistent with small changes in the threshold voltage and are on the order of a few percent at 1 Mrad(SiO$_2$).

C. Results for SRAM Pull-down and Pass-gate Transistors

The SRAM PD and PG transistors were evaluated in the same fashion as the low-V_{th} and high-V_{th} logic devices discussed previously. In this case we focus on the results for the *on*-state irradiation bias condition since this has consistently provided a worst-case irradiation response in terms of $I_{ds,off}$. The results of those studies can be seen in Fig. 5 for the on-state (5 (a)) and *half-on*-state (5 (b)), with a summary of ΔV_{th} and $\Delta I_{ds,off}$ shown in Fig. 5 (c). The device irradiated in the half-on-state again shows a smaller relative ΔV_{th} and a significantly reduced $\Delta I_{ds,off}$ as compared to the on-state irradiated device. These results are quantitatively and qualitatively similar to the results on standard logic transistors presented in the previous two sections. We note the devices exhibit less change in the $I_{ds,off}$ than the low-V_{th} device and exhibits leakage more comparable to that of the superior radiation tolerance of the high-V_{th} device. The geometry of the discrete nMOSFET SRAM transistors varies slightly from that of the logic transistors discussed above, and is evident in the $\Delta I_{ds,off}$ vs Dose response of the device. The PD and PG transistors also exhibit a higher initial V_{th} suggesting the body doping of the channel would require higher amounts of trapped charge in the STI to invert the side-wall transistor. In the full paper we will present TCAD analysis to confirm these results and additionally demonstrate the reduction in static noise margin of the SRAM cell that arises from mismatched *p*MOSFET and *n*MOSFET device drive current. An evaluation of the timing will also be presented for a simple RO circuit.

IV. Conclusions

An initial evaluation of the device-level response of a 14-nm bulk FinFET process to TID was reviewed. Device threshold voltage is shown to shift in a manner consistent with charge trapping in the oxide and buildup of interface states and is minimal. Drain leakage current is shown to have a gate voltage dependence, indicating electrostatic control from the gate electrode in the sub-Fin region. Radiation-induced leakage is the largest concern for radiation hardness in advanced FinFET CMOS technology. The high-V_{th} transistors exhibit the best post-irradiation performance across all bias conditions, showing a reasonably small change of $I_{ds,off}$ and V_{th}, while the low-V_{th} transistors exhibit a larger response in $\Delta I_{ds,off}$.. The "worst-case" bias condition during irradiation for pull-down and pass-gate nMOSFETs in static random access memory (SRAM) is the *on*-state $V_{gs} = V_{dd}$ condition resulting from the establishment of electric fields in the shallow trench isolation (STI) near the sub-Fin region during irradiation. The nMOSFET pull-down and pass-gate transistors of the SRAM bit-cell show less TID degradation due to transistor geometry and channel doping than the low-V_{th} transistor. Significant reduction in leakage current is observed in SRAM transistors when operating under reduced supply voltage conditions, suggesting advantages for devices implemented in low-power and sub-threshold operation regimes.

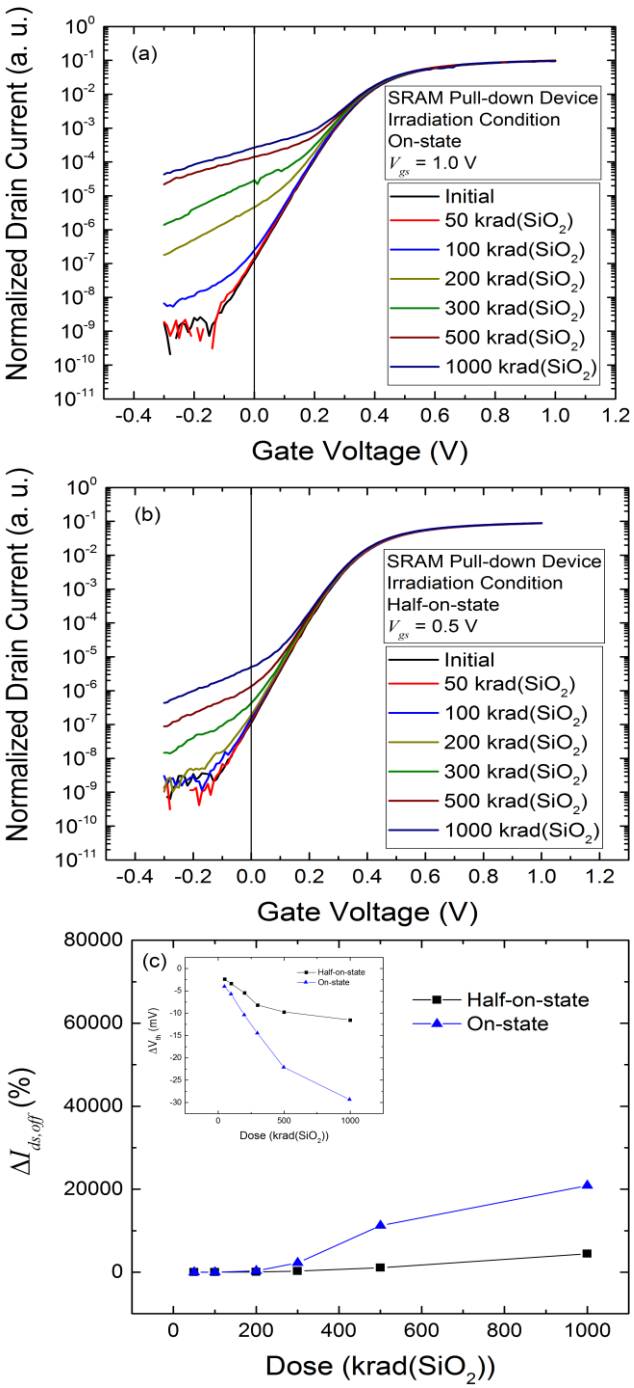

Fig. 5. Percent change in $I_{ds,off}$ as a function of dose for the low-V_{th} and high-V_{th} 14-nm FinFET devices in the *off*- (a), *on*- (b), and *half-on*-state (c) during irradiation shows the worst-case bias condition for leakage current response is the *on*-state condition. The higher threshold voltage device shows a less severe response for all bias conditions.

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