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THE MPI/AIT X - RAY IMAGER (MAXI) - HIGH SPEED PN-CCD's FOR X - RAY DETECTION

L. Strüder, H. Bräuninger, M. Meier, P. Predehl, C. Reppin, M. Sterzik, J. Trümper
Max-Planck-Institute for Physics and Astrophysics
Institute for Extraterrestrial Physics, Garching

P. Cattaneo, D. Hauff, G. Lutz, K. F. Schuster, A. Schwarz
Max-Planck-Institut for Physics and Astrophysics
Werner-Heisenberg-Institut for Physics, Munich

E. Kenziorra, A. Staubert
Astronomical Institute of the University of Tübingen

E. Gatti, A. Longoni, M. Sampietro
Politecnico di Milano

V. Radeka, P. Rehak, S. Rescia
Brookhaven National Laboratory, New York

P. F. Manfredi
University di Pavia

W. Buttler
Fraunhofer Institute for Microelectronics, Duisburg

P. Holl, J. Kemmer, U. Prechtel, T. Ziemann
Messerschmitt-Bölkow-Blohm GmbH, Ottobrunn

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1. ABSTRACT

MAXI (MPI/AIT X-ray Imager) is part of a proposal submitted to the European Space Agency (ESA) as focal plane instrumentation of the X-ray Multi Mirror Mission (XMM). Within a collaboration of 13 european institutes we have proposed a fully depleted (sensitive) pn CCD of 280 μm thickness with a homogeneous sensitive area of 36 cm^2 and a pixel size of 150 $\times$ 150 μm^2 which is well matched with the telescope's angular resolution of 30 arcsec, translating to a position resolution of approximately 1 mm in the focal plane.

The X-ray sensitivity is higher than 90% from 250 eV up to 10 keV, the readout time in the full frame mode of the complete focal plane will be 2 ms with a readout noise of better than 5 e$^-$ (rms). Prototypes of all individual components of the camera system have been fabricated and tested. The camera concept will be presented. The measured transfer properties of the CCD and the on-chip electronics will be treated. Taking into account the coupling of the on-chip amplifier to the following front-end electronics the expected performance will be derived.

2. INTRODUCTION

The X-ray Multi Mirror Mission (XMM) of the European Space Agency (ESA) is one of four cornerstone projects in the long term programme for space science. XMM is due to be launched in 1998 as an astronomical facility with X-ray focussing optics of unprecedented

throughput in the energy domain of 0.1 to 10 keV. The three telescopes are supposed to be operated with three different CCD cameras in the focal plane of the Wolter-type telescope, two with conventional MOS type devices (GEC, THOMSON) and one fully depleted pn type CCD. We are going to describe the pn-CCD, its on-chip electronics and their coupling to a 64 channel multiplexing CMOS amplifier array (CAMEX64). This chip was originally developed for the readout of the mini-vertex detector with 56.000 individual signal channels for the ALEPH experiment at CERN. All components have already been tested individually: the CCD, the JFET electronics on high resistivity n-type silicon and the CAMEX64 VLSI chip. Based on these measured performances the system parameters and possible operating modes will be calculated.

3. FULLY DEPLETED PN CCD'S

In 1983 Gatti and Rehak [1] proposed a new detector scheme based on the idea that a large semiconductor wafer of e.g. high resistivity n - type silicon can be depleted from a small n^+ ohmic contact positively biased with respect to the planar p^+ contacts covering both surfaces of the wafer. The depletion zone will expand from both rectifying junctions simultaneously as long as the ohmic access from the n^+ anode to the entire bulk is not interrupted. At a given voltage the depleted regions touch each other. Under this condition the former conductive electron channel symmetrically located in the middle of the substrate between the large p^+ implants will abruptly disappear. At this moment the depletion is completed at a voltage which is four times lower than the voltage needed to deplete a simple diode of the same thickness. The above described removal of mobile charge carriers is called sideward depletion. In this case the electron potential energy in a cut perpendicular to the wafer surface has a parabolic shape, with an electron potential minimum in the middle of the wafer. The electron potential minimum can be moved out of the center towards either surface by applying non equal voltages to the two p^+ contacts.

The advantages of the technique are obvious: Independently of the size of the depletion region the capacitance of the n^+ anode can be kept extremely small – necessary condition for good noise performance – and the position of the potential minimum can be controlled by external means. This scheme is adapted for the operation of fully depleted pn CCD's. The basic topology is shown in Fig. 1. The p^+ back contact is negatively biased with respect to the shift electrodes on the top side thereby shifting the electron potential minimum close to the top surface. By an appropriate choice of the voltages at the p^+ tranfer registers φ_1, φ_2, and φ_3 it is possible to create local potential minima for electrons and an adequate change with time in these voltages allows a discrete shift of the signal charges towards the readout anode.

The more complex three dimensional arrangement of a linear CCD structure including the readout region with the p^+ guard ring is shown in Fig. 2. A deep n - implantation below the p^+ transfer registers and below the SiO_2 is introduced a) to prevent large thermally injected currents (reach through currents) between p^+ junctions at different potentials and b) to form a guiding channel for signal charges. The lateral spread of the charges is prevented by the gap of the deep n - implant between neighboring guiding channels. The absence of the positive space charge in the vicinity of a channel guide creates a negative potential for electrons with respect to the depleted deep n - doped region, thus acting as a potential barrier for the signal charges, confining them to the channel guide area [2, 3]. The entire

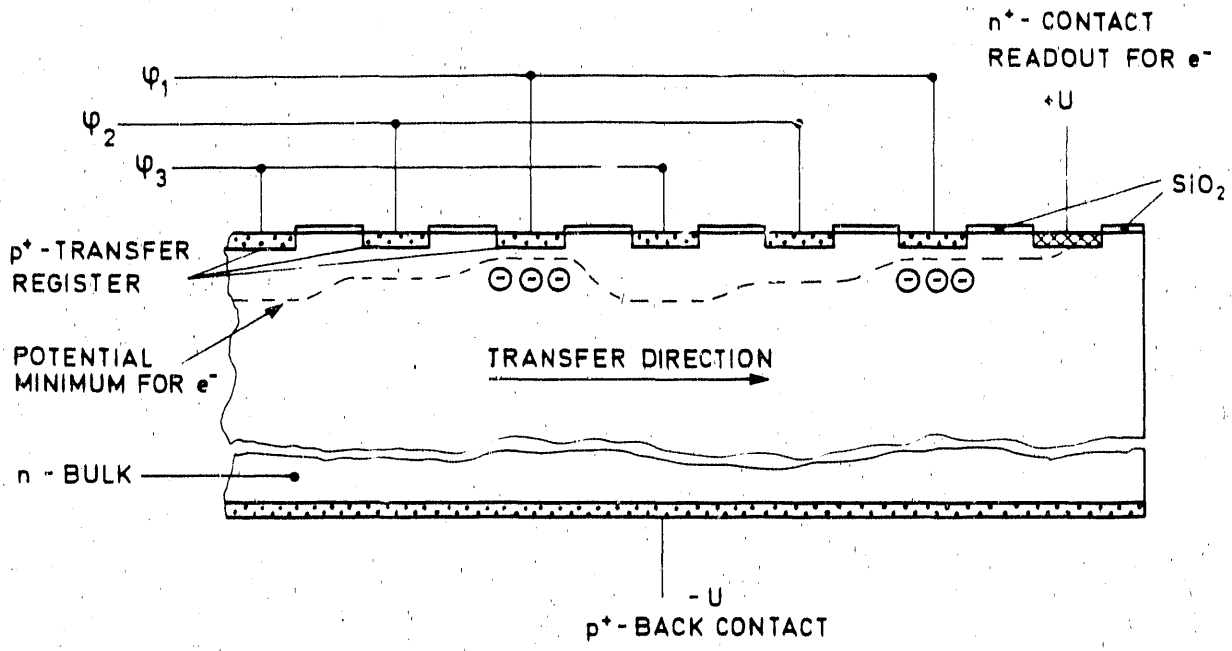


Fig. 1: Basic configuration of a fully depleted pn CCD topology derived from the silicon drift chamber principle.

CCD structure is surrounded by a reverse biased p^+ guard ring preventing charges from the undepleted regions o the chip to flow in the sensitive area. The schematic layout of the XMM CCD is depic ed in Fig. 3.

We have fabric ted devices of this type with pixel sizes varying from $50 \times 50\,\mu m^2$ up to $150 \times 170\,\mu m^2$. In a first attempt a charge transfer inefficiency per pixel of 1×10^{-3} was achieved for shift frequencies starting from 500 kHz up to 8 MHz.

We have understood in detail the charge losses resulting in a modified design being actually processed. This should lead to the same or a better charge transfer as compared to standard buried channel MOS CCD's. Two-dimensional multilinear arrays with channel stops between the individual linear CCD's are under test. An interference between adjacent pixels was not observed. The measured position dependent CCD output signal is shown in Fig. 4. Concerning the transfer properties and the realization of an arbitrary two dimensional pixel pattern the pn CCD will be competitive with the best existing MOS devices.

The new concept however leads to some additional significant improvements for X - ray spectroscopy:

1. As the entire thickness of the wafer is completely sensitive to radiation the device can be backside illuminated. The radiation penetrates through an ultra thin completely homogeneously doped reverse biased p^+ back contact where the strong electric field separates the electron-hole pairs instantaneously and drifts the electrons within less than 10 ns to the wafer surface having the pixel structure.
2. The detection efficiency of soft X - rays will be higher than 90% for photon energies above 250 eV because the backside entrance window is thinner than 200 Å defining the lower cut-off of the energy response. The limitation of the soft X – rays is in practical applications dictated by the light- and UV-filter. At 10 keV the detection efficiency is

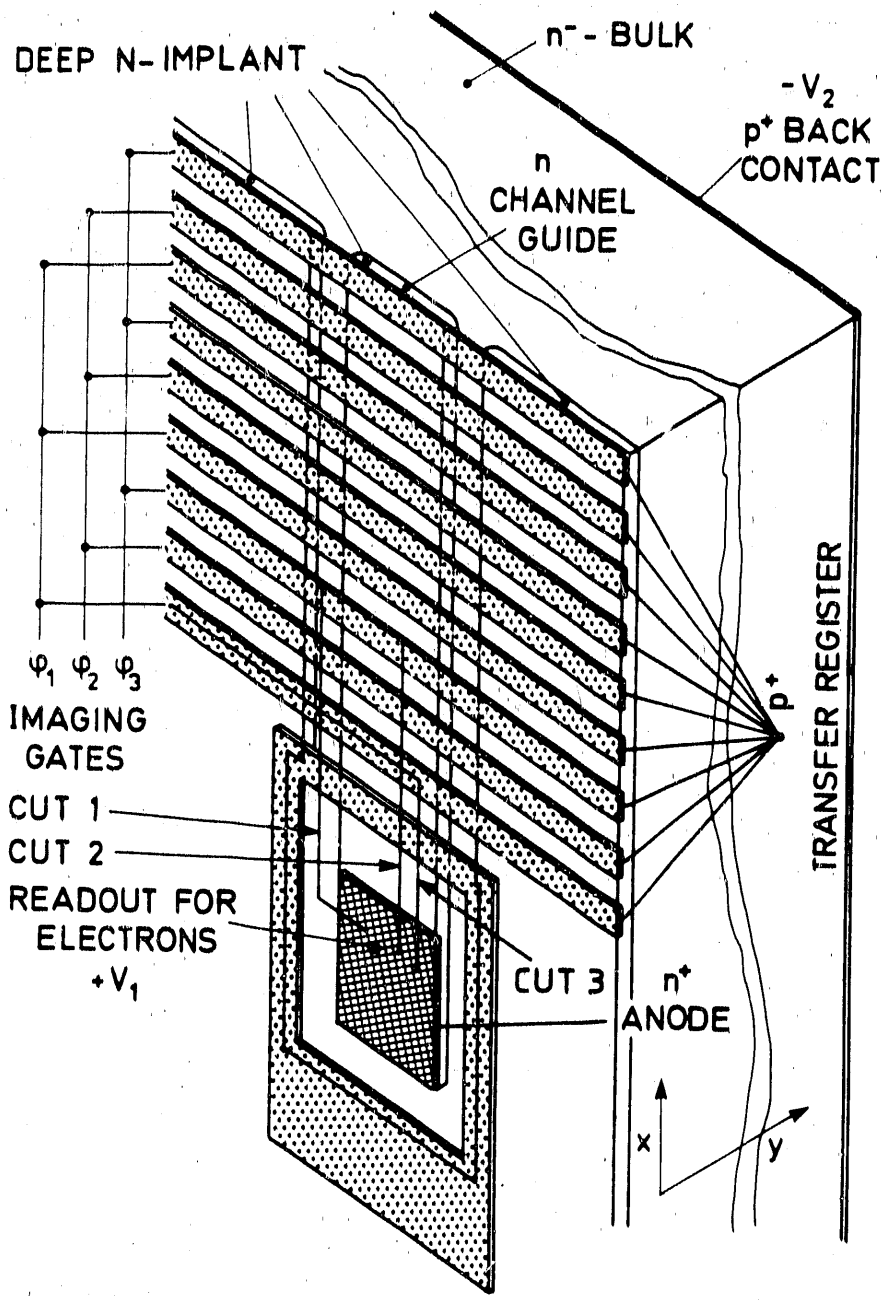


Fig. 2: Schematic view of the linear CCD geometry with implantation topologies including the channel stop mechanism. The entire CCD area is surrounded by p^+ guard ring separating the sensitive area from the undepleted rest of the chip.

still higher than 90% because of the 280 μm sensitive thickness of the detector. Between 250 eV and 10 keV the efficiency for X-rays varies between 90% and 100% according to the functional dependence of the silicon absorption coefficient from the incident photon energy.

3. The fact that the charge can be efficiently transferred up to a depth of approximately 40 μm in the bulk of the device pixel sizes from $20\times20\,\mu m^2$ up to $200\times200\,\mu m^2$ can be implemented. For the XMM mission a pixel geometry of $150\times150\mu m^2$ seems to be adequate. An ideal matching with the resolution of the X-ray telescope becomes

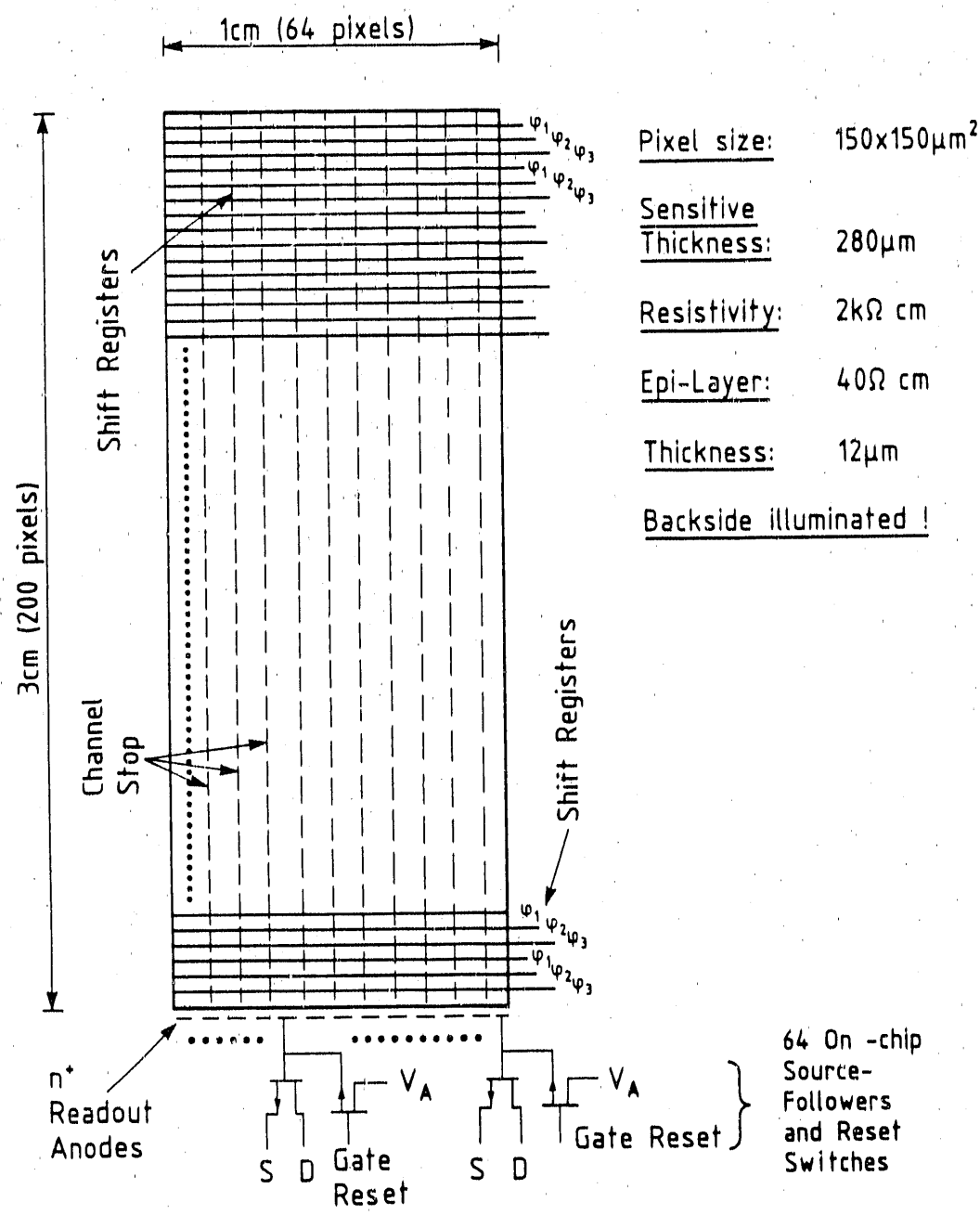


Fig. 3: Schematic view of the pn-CCD geometry with multianode readout structure, on-chip source followers and reset switches for each individual CCD line.

possible.

This reduces the readout time compared to standard MOS devices by a factor of 56 due to the reduced number of pixels without any loss of physical information.

Furthermore the charge splitting in more than one pixel is reduced.

4. In a 280 μm thick completely sensitive detector a minimum ionizing particle (mip) deposits an energy of 80 keV. This type of background can be directly rejected from the comparison of the signal amplitudes with a 10 keV photon signal. Without any further signal analysis the background rejection is 100% in practical applications.
5. The exclusive use of pn structures instead of MOS structures makes this CCD intrinsi-

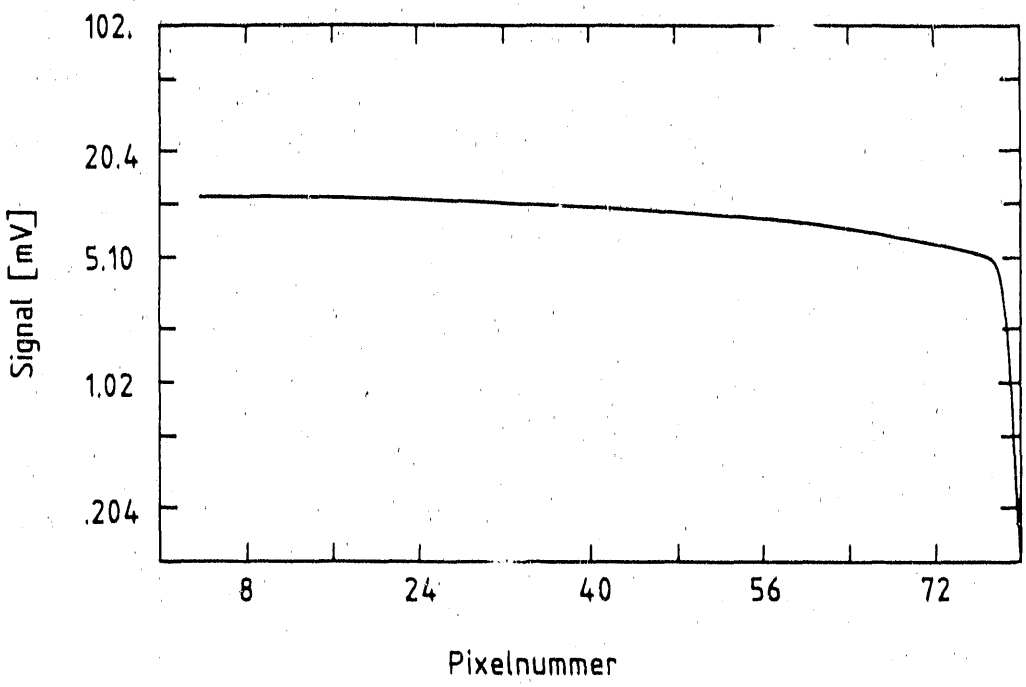


Fig. 4: Position dependence of the output signal. The pn-CCD was operated with off-chip electronics with a noise level of 300 e^-. Up to pixel no. 50 the transfer efficiency per pixel was 0.999. The efficiency drop from pixel no. 50 to 80 may be due to resistivity fluctuations in the bulk of the silicon. The shift frequency was 1 MHz, the signal charges have been generated by a pulsed infrared laser. All measurements were performed at room temperature.

cally radiation hard. Up to 1 Mrad no significant degradation should occur. Experiences from high energy physics experiments show that devices based on the same technology are radiation hard up to 5 Mrad [9]).

These conceptual advantages are in c properties of all fully depleted pn CCD's. The specific system performance of the XM vice is described in section 5.

4. FRONT END ELECTRONICS ON HIGH RESISTIVITY SILICON

In order to use the low detector capacitance for fast and low noise applications new types of transistors have been developed: single sided gate n-channel JFET's. Basing on the same fabrication technology as the detector itself the new components will be monolithically integrated close to the detectors readout nodes. The design and first results of the new JFET's are documented in [6, 7, 8] and [10]. With the current technology and a suitable geometry the gate capacitance can be made as small as 100 fF. The gatelength of the transistors is 6 μm while the gatewidth is 90 μm (see Fig.5).

An output resistance of 50 kΩ was m red. The transconductance g_m was 0.35 mS at a source drain current of 250 μA. The pin voltage has been ermined to 1.5 V. A recent detailed review of the JFET' performa given in [10]. Ins ing those measured values into a noise analysis of the first amplify ge a lower limit for the noise of 2 electrons (rms) was calculated for the CCD specificat r XMM at a readout frequency of 100 kHz and an operating temperature of 180 K assuming that the shot noise contribution of the leakage

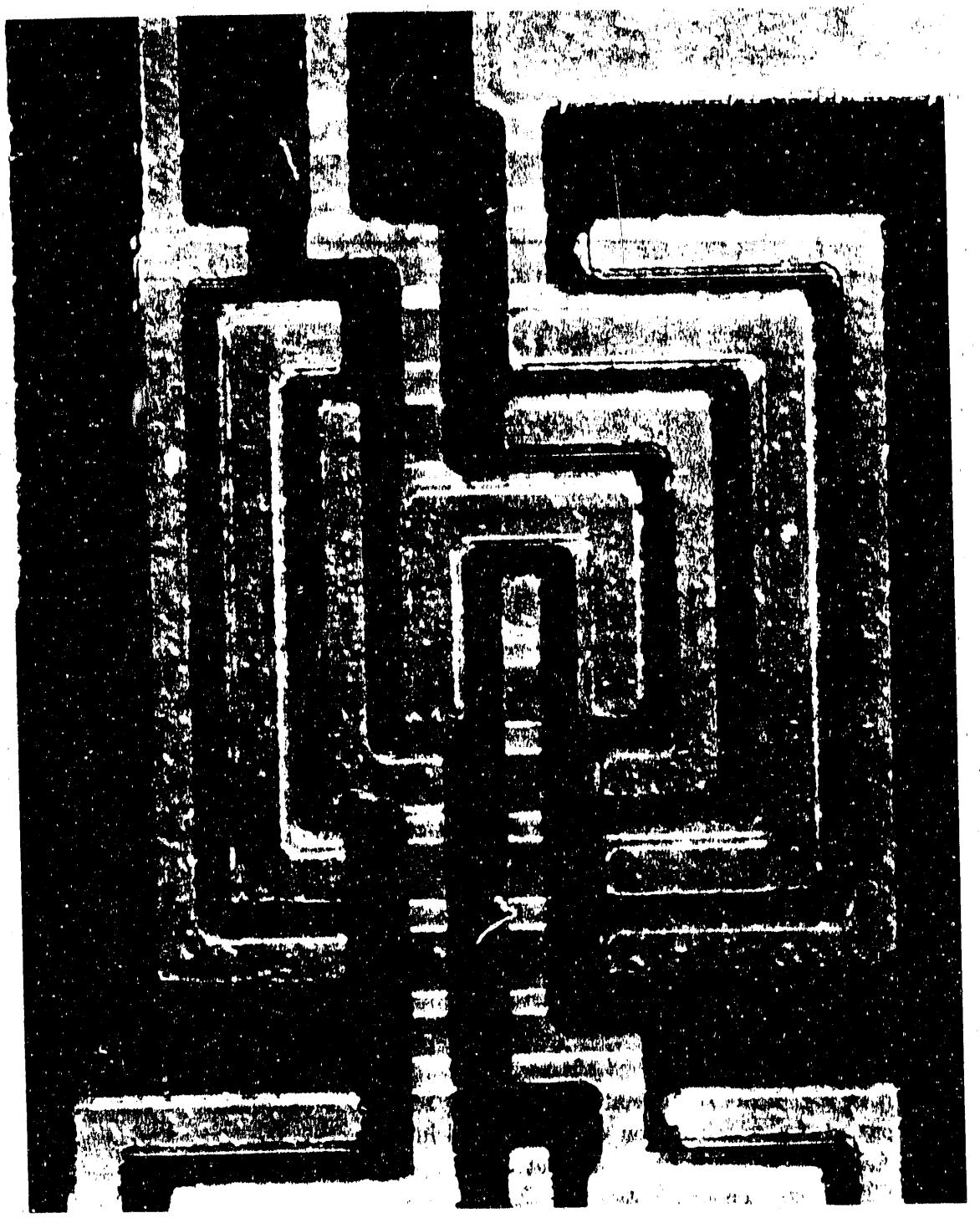


Fig. 5: Photomicrograph of two single sided gate n - channel JFET's. They are part of a cascode input stage of a charge sensitive preamplifier. (Photo: B. Marin, BNL)

current is negligible at that temperature. The 1/f corner frequency was determined to be lower than 10 kHz for our configuration. Under these considerations all other additional noise contributions from further signal processing should be made small compared to the ENC of 2 e^-. This will be achieved with a slightly modified version of the VLSI CAMEX64 chip as described in the next section.

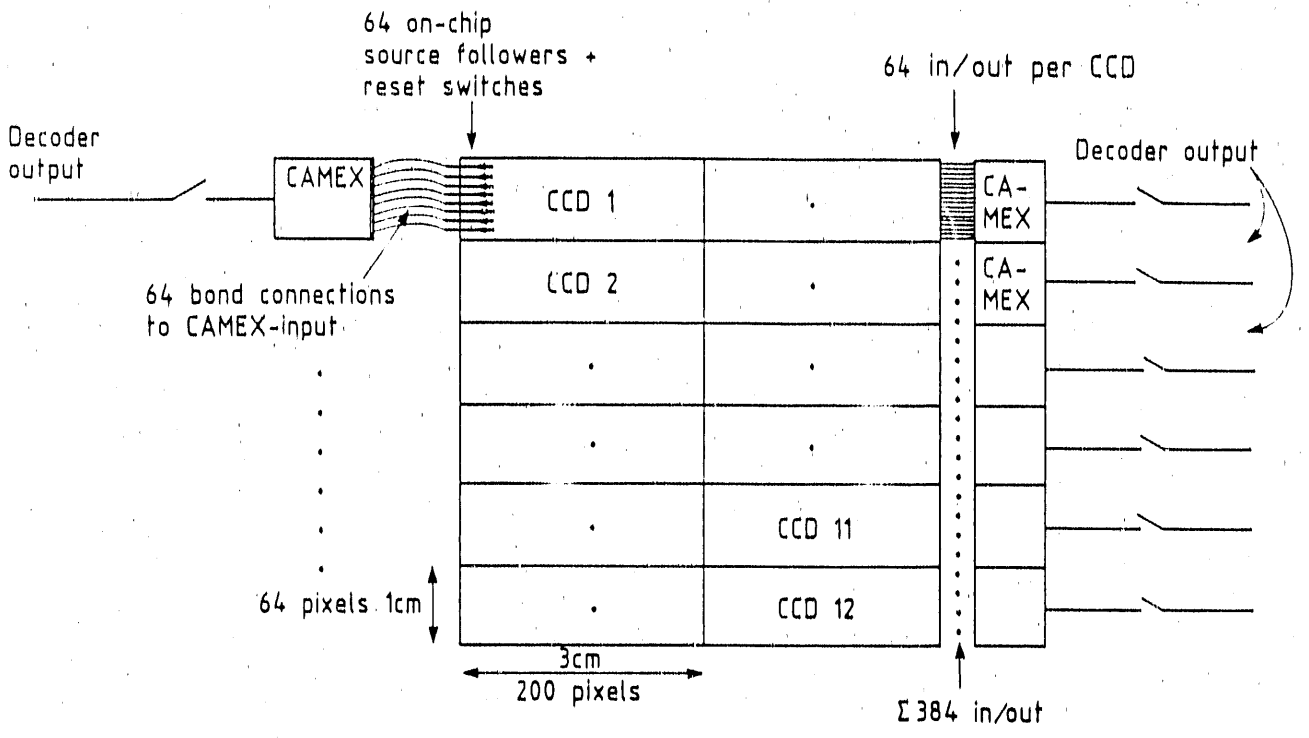


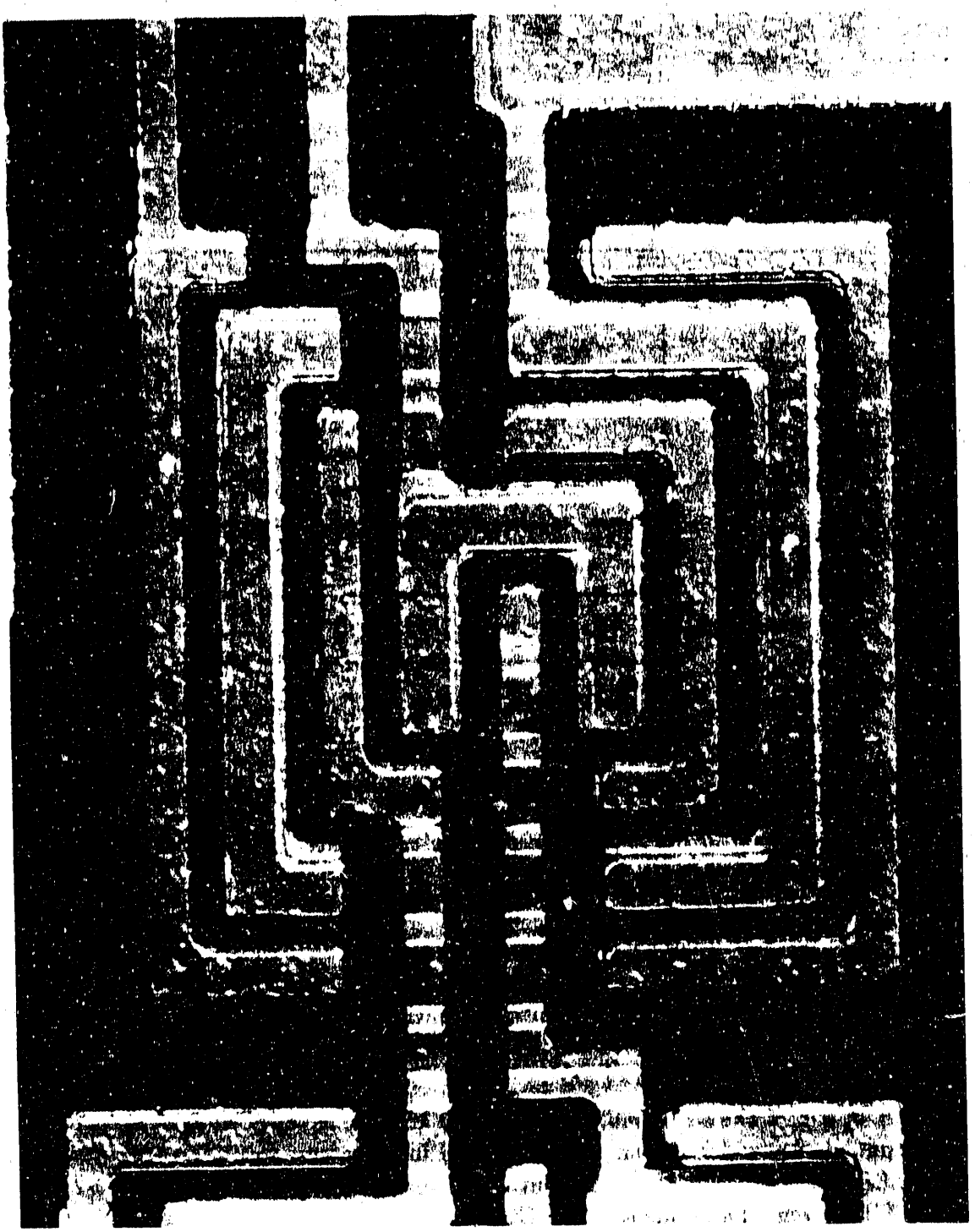
Fig. 6: General layout of the focal plane detector consisting of 2×6 *pn-CCDs each with a sensitive area of* 3×1 cm^2.

5. THE ADOPTED CONCEPT AND CHIP DIMENSIONS

The entire focal plane will be made out of 12 identical pn CCD's as shown in Fig. 6. A single chip will have 200 pixels in the transfer direction and 64 pixels in the vertical direction resulting in chip dimensions of 3×1 cm^2. The pixel size is $150 \times 150 \mu$m^2. The entire sensitive area of the focal plane will be 6×6 cm^2.

As shown in Fig. 7 the serial multiplexing CCD register is replaced by a total of 64 parallel output anodes which are on chip connected in the actual fabrication with 64 on chip preamplifiers each consisting of one input JFET operated in a source follower mode and a reset JFET switch. Those identical 64 CCD output channels are bonded after the source follower to a 64 channel CMOS amplifier chip (CAMEX64). The custom designed VLSI chip (CAMEX64) has been developed in CMOS technology by the Max-Planck-Institut, Munich and the Fraunhofer Institute, Duisburg. The chip provides signal amplification, noise filtering, parallel storage and serial readout of the analog signals and contains in addition a digital control for power switching [11]. Fig. 8 shows a schematic of one channel of the amplifier chip. Switched capacitor filters are used in order to reduce the noise by multicorrelated double sampling.

This concept takes advantage of the fact that the slow time consuming amplifying and noise filtering procedure is effectuated in parallel with approximately 100 kHz while the



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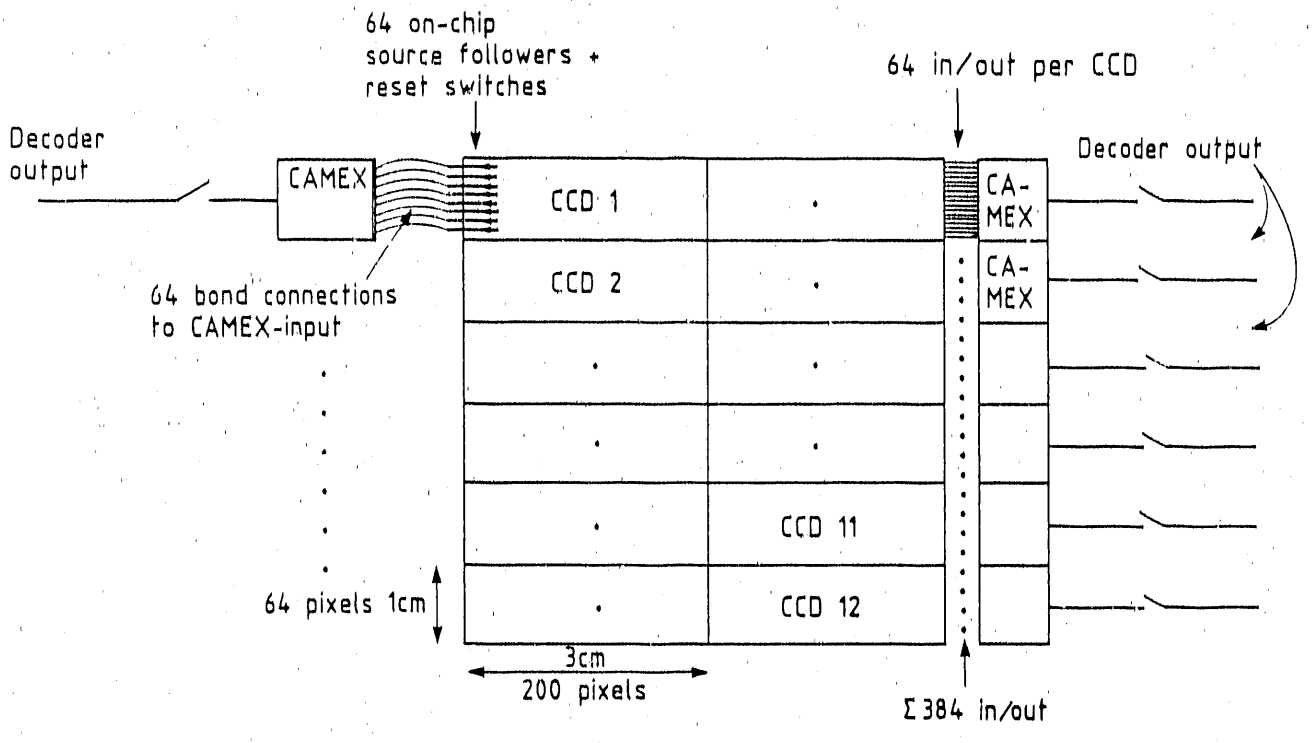
current is negligible at that temperature. The 1/f corner frequency was determined to be lower than 10 kHz for our configuration. Under these considerations all other additional noise contributions from further signal processing should be made small compared to the ENC of 2 e^-. This will be achieved with a slightly modified version of the VLSI CAMEX61 chip as described in the next section.



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The entire focal plane will be made cut of 12 identical pn CCD's as shown in Fig. 6. A single chip will have 200 pixels in the transfer direction and 64 pixels in the vertical direction resulting in chip dimensions of 3×1 cm^2. The pixel size is $150 \times 150 \mu m^2$. The entire sensitive area of the focal plane will be 6×6 cm^2.

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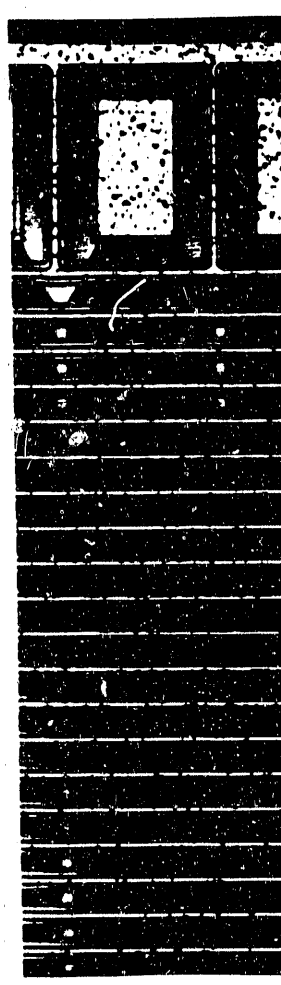

Fig. 7: Phot

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the event 20 pixels (3.0mm) within 2 μs towards the anode before integrating the next 22 μs and so on. In this **timing mode** we would registrate the point like image every 3 mm on the 3 cm long chip. Within the resolution of the X-ray telescope of about 1 mm in the focal plane ($\sigma \approx 30$ arcsec, the focal length is ≈ 7.5 m) there should be no significant spatial ambiguity for the single event recognition. This procedure can be repeated 10 times before the signal charges of the entire chip is consecutively detected at the readout node with the signal detection frequency of 40 kHz then leading to a dead time of the detector of 2 ms for the slow readout of the complete CCD chip. This **timing mode** allows a low noise timing bandwidth in the order of 40 kHz: 10 samples with a time resolution of 24 μs can be recorded in one readout sequence.

All procedures decribed so far still yield the high energy resolution of 5 e^- as in the full frame mode. If we would tolerate a higher noise level the speed could be further improved.

This seems to us to be fast enough to penetrate into a wide field of unknown transient astrophysical phenomena so that more sophisticated techniques to reduce the readout and integration time are not needed.

One complete readout channel including the on chip electronics and the slight modifications in the input of the CAMEX64 are depicted in Fig. 8. On the left side of the diagram the CCD anode, source follower and reset switch of one of the 64 identical on chip circuits can be seen. The resistor of the source follower will be realized as a current source on the CAMEX64 chip.In addition a 10 pF input capacitor will be added to the charge sensitive preamplifier.

Fig. 9 shows the system noise at the output of the CAMEX64 chip translated into electron fluctuations at the CCD's readout anode. The electrical parameters needed for the calculation are measured values from prototype devices. They are inserted in Fig. 9. If the bandwidth of the amplifier is 500 kHz an equivalent noise charge of about 4 e^- is expected if a fourfold correlated sampling is applied.

The power consumption is controlled by an external reference voltage allowing thus a large flexibility in the variation of speed, noise performance and power consumption. The actual overall size of the 64 channel chip is 6.35×4.95 mm^2 (see Fig. 10).

Fig. 10 shows a photograph of the aluminium layer of the CAMEX64 chip. On the upper side of the chip are the signal input pads and on the opposite side are the pads for the control bus and the multiplexed output.

In order to reduce the number of input lines and to minimize the amount of cable connections to the cryogenic part of the detector a digital steering chip (TIMEX64) has been designed in CMOS technology. Upon receipt of two input lines (an initialize pulse and a pulse train) it provides all 18 switching pulses that are needed for the amplifier chip.

Power consumption and heat dissipation are below the values required by the passive cooling system. The entire focal plane detector will be built up with 12×64 i.e. 768 identical readout channels. During the readout the CCD detector's power consumption is in the order of .5 mW per channel. The overall dissipation of one CAMEX64 channel is also .5 mW during the operation leading to .8 W for the entire electronics of the camera. All amplifying devices can be switched off during the x-ray integration time resulting in a power consumption of less than .1 W for the electronics in the cryogenic part of the camera head. The TIMEX64 chip will not be located in that region. As the externally steered pulse train of the TIMEX64 determines the timing sequences of the CAMEX64 a large readout variety can be realized.

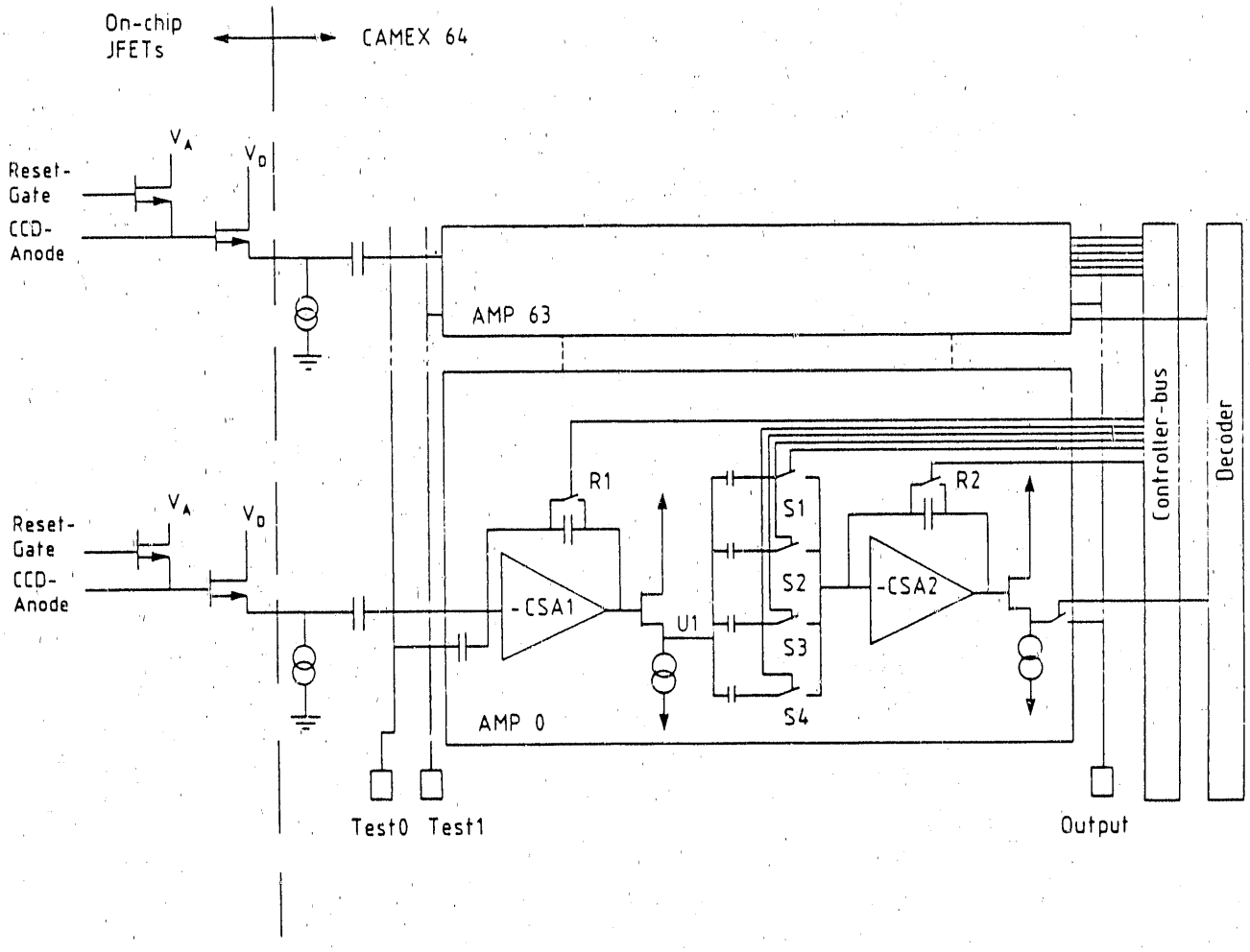

Fig. 8: One of 64 identical readout channels including the on chip JFET electronics of the CCD.

Intensive studies are going on to replace the front end CMOS circuits of the CAMEX64 chip by JFET's (e.g. [14]). This will reduce once more the noise contribution of this second amplifying stage and increase the radiation hardness and the reliability of the device [15]

6. SUMMARY

The described high speed pn CCD X - ray camera will have the following properties:

- The overall sensitive area of the focal plane will be $6\times6\text{cm}^2$, consisting of 12 independent $3\times1\text{cm}^2$ pn CCD's each with 64 individual readout channels and a pitch of 150 μm .
- The detection efficiency between 250 eV and 10 keV is higher than 90% . For most of the physically interesting energies the effieciency is closer to 100% than to 90% . Because of the highly reduced charge splitting due to the large pixel sizes averaging and summing over more than one pixel is not needed. This guarantees the high detection efficiency

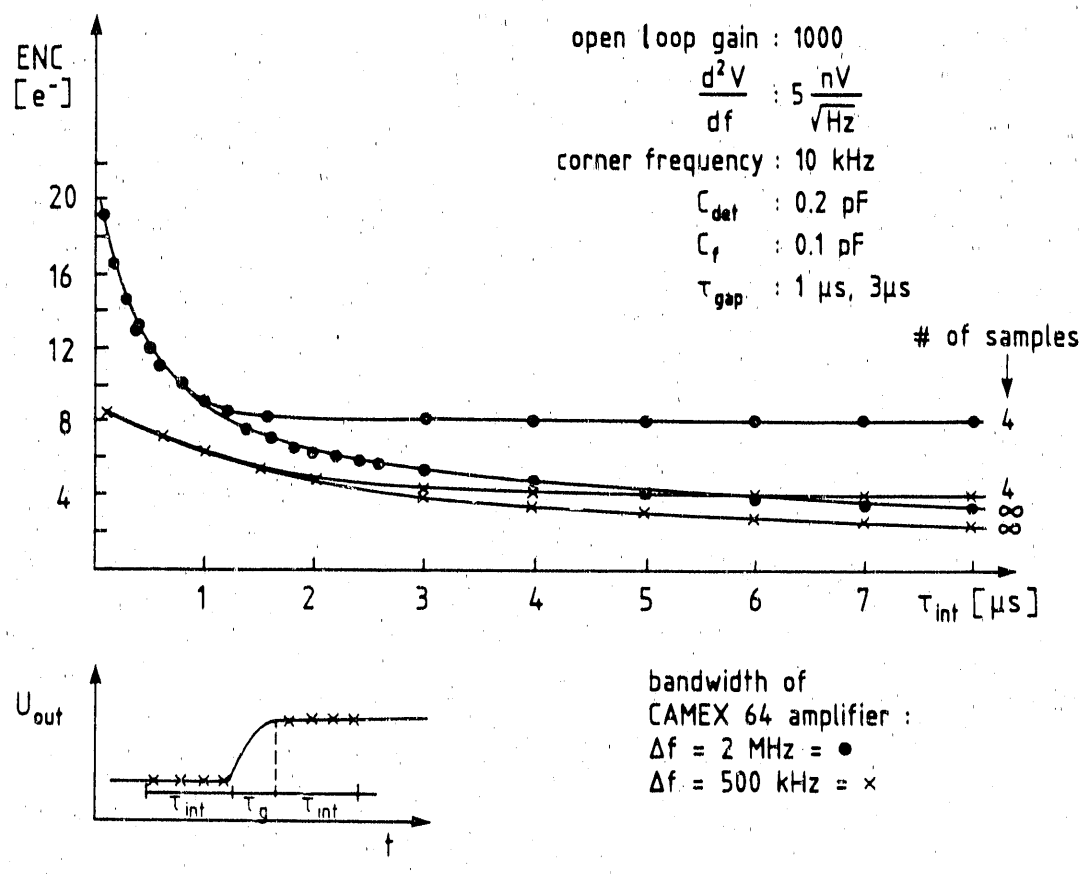

Fig. 9: Effect of the multicorrelated sampling on the amplifier filter time dependent electronic noise. The electrical parameters are inserted in the figure.

for practically all events with the noise level of one single pixel.

- The system noise will be below 5 e^- corresponding to an energy resolution of better than 45 eV.
- By including an eleven times higher integration time of the image than the effective readout time one achieves the following time resolution:

  the readout time of 24 ms in the **full frame mode** still allows the detection of e.g. the pulsar inside the crab nebula.

  In the **windowing mode** the time resolution is 2 ms.

  In the **timing mode** the time resolution becomes 24 μs (with a dead time of 2 ms after approximately 10 event integration times).
- The spatial resolution is defined by the pixel size of $150 \times 150\,\mu m^2$. That is approximately 7 times smaller than the resolution of the XMM X – ray mirror system.
- The suppression of background events originating from minimum ionizing particles can be made immeasurably small.
- The 768 individual electronic channels make the CCD system redundant to a very high degree.
- For a ten year mission the CCD's are sufficiently radiation hard.

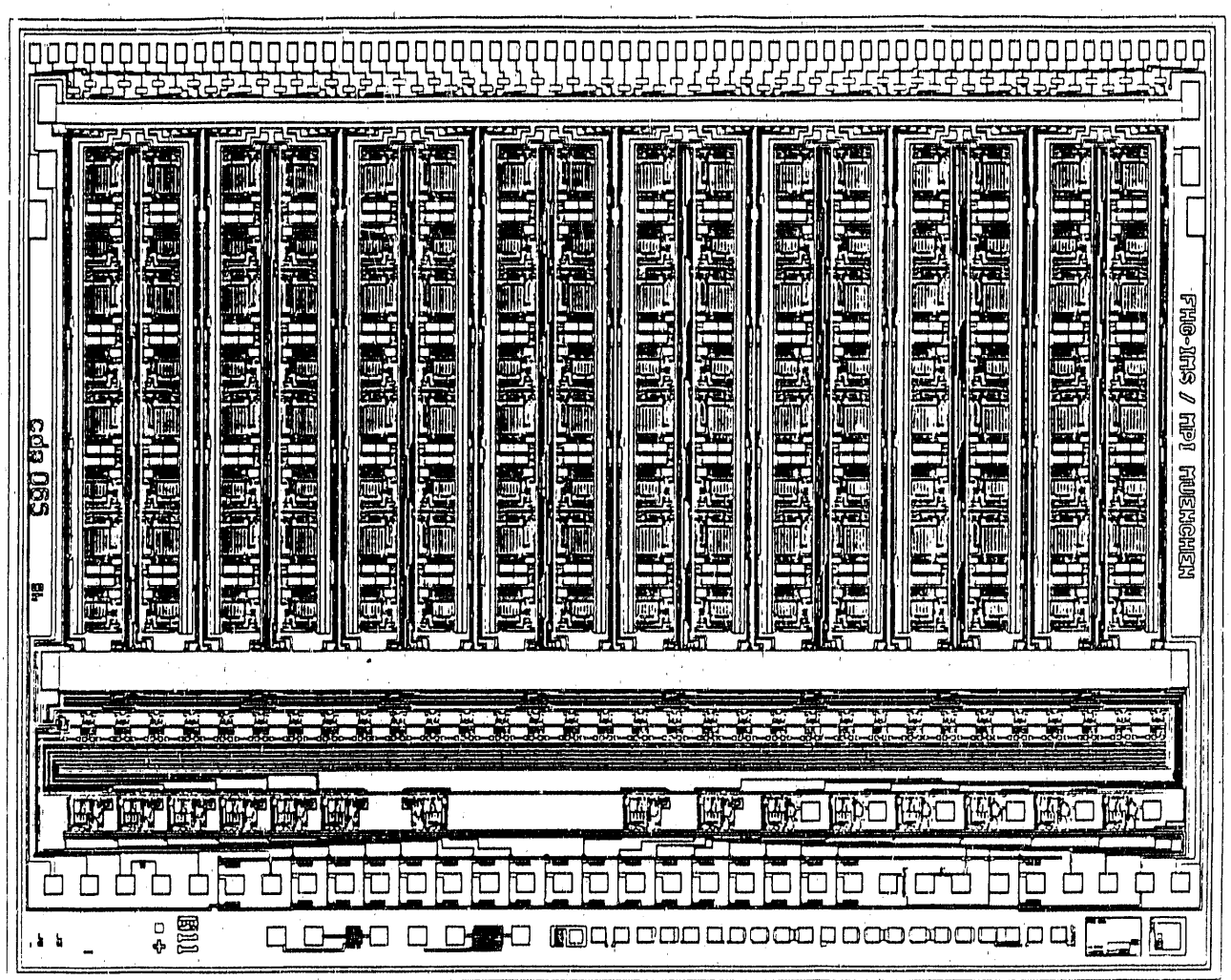

Fig. 10: Photograph of the CAMEX64 chip.

REFERENCES

1. E. Gatti, P. Rehak: Semiconductor Drift Chamber - an Application of a Novel Charge Transport Scheme, in Proc. 2nd Pisa Meeting on Advanced Detectors, Grosetto, Italy (1983) NIM A, Vol. 225 (1984) pp.608-614.

2. L. Strüder et al., Device Modeling of Fully Depletable CCD's, NIM A, Vol. 253 (1987) pp. 386 -393.

3. L. Strüder et al, Development of Fully Depletable CCD's for High Energy Physics Applications, NIM A, Vol. 257 (1987), pp. 594-602.

4. L.Strüder et al., Development and Test of Fully Depleted pn CCD's for X-Ray Detection, Proceedings of the 32^{nd} SPIE Meeting, San Diego 1988.

5. L.Strüder et al., First Tests with Fully Depleted CCD's, IEEE Transactions on Nuclear Science, Vol. 35, No. 1, Feb. 1988, pp 372 - 376.

6. V.Radeka et al., Design of a Charge Sensitive Preamplifier on High Resistivity Silicon, IEEE 1987 Nuclear Science Symposium, NS Vol. 35, No. 1 (1988), pp. 155 - 159.

7. V. Radeka et al., JFET for Completely Depleted High Resistivity Silicon, contributed paper for the ESSDERC conference, 1988.

8. V. Radeka et al., Implanted Silicon JFET on Completely Depleted High Resistivity Devices, submitted to IEEE Electron Devices 1988.

9. H. Dietl, G. Lutz et al., Radiation Damage in Silicon Strip Detectors NIM A253 (1987) pp. 460-466.

10. E. Gatti et al. Front End Electronics Integrated on the Detector Wafer – State of the Art and Research, to be submitted to NIM A, 1989

11. W. Buttler et al., Low Noise - Low Power Monolithic Multiplexing Readout Electronics for Silicon Strip Detectors, NIM A, in print (1988).

12. CAMEX64 Data Sheet, Available at Max-Planck-Institut für Physik, Werner-Heisenberg-Institut für Physik Föhringer Ring 6, 8000 München 40, West Germany.

13. G.Lutz et al., Low Noise Monolithic CMOS Front End Electronics, NIM A263 (1988) pp. 163 - 173.

14. G.Lutz et al., On the Design of a JFET - CMOS Front-End For Low Noise Data Aquisition From Microstrip Detectors, NIM A264 (1988) pp. 391 -398.

15. W. Buttler et al., Noise Performance And Radiation Hardness of the CAMEX64 Analog Multiplexing Chip, Contribution to the XXIV International Conference on High Energy Physics, August 4 – 10, 1988, Munich.

FIGURE CAPTIONS

1. Basic configuration of a fully depleted pn CCD topology derived from the silicon drift
chamber principle.

2. Schematic view of the linear CCD geometry with implantation topologies including the channel stop mechanism. The entire CCD area is surrounded by p^+ guard ring separating the sensitive area from the undepleted rest of the chip.

3. Schematic view of the pn-CCD geometry with multianode readout structure, on-chip source followers and reset switches for each individual CCD line.

4. Position dependence of the output signal. The pn-CCD was operated with off-chip electronics with a noise level of 300 e^-. Up to pixel no. 50 the transfer efficiency per pixel was 0.999. The efficiency drop from pixel no. 50 to 80 may be due to resistivity fluctuations in the bulk of the silicon. The shift frequency was 1 MHz, the signal charges have been generated by a pulsed infrared laser. All measurements were performed at room temperature.

5. Photomicrograph of two single sided gate n - channel JFET's. They are part of a cascode input stage of a charge sensitive preamplifier. (Photo: B. Marin, BNL)

6. General layout of the focal plane detector consisting of 2×6 pn-CCDs each with a sensitive area of 3×1 cm^2.

7. Photomicrograph of the multianode region of the pn CCD. (Photo: B. Marin, BNL)

8. One of 64 identical readout channels including the on chip JFET electronics of the CCD.

9. Effect of the multicorrelated sampling on the amplifier filter time dependent electronic noise. The electrical parameters are inserted in the figure.

10. Photograph of the CAMEX64 chip.

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