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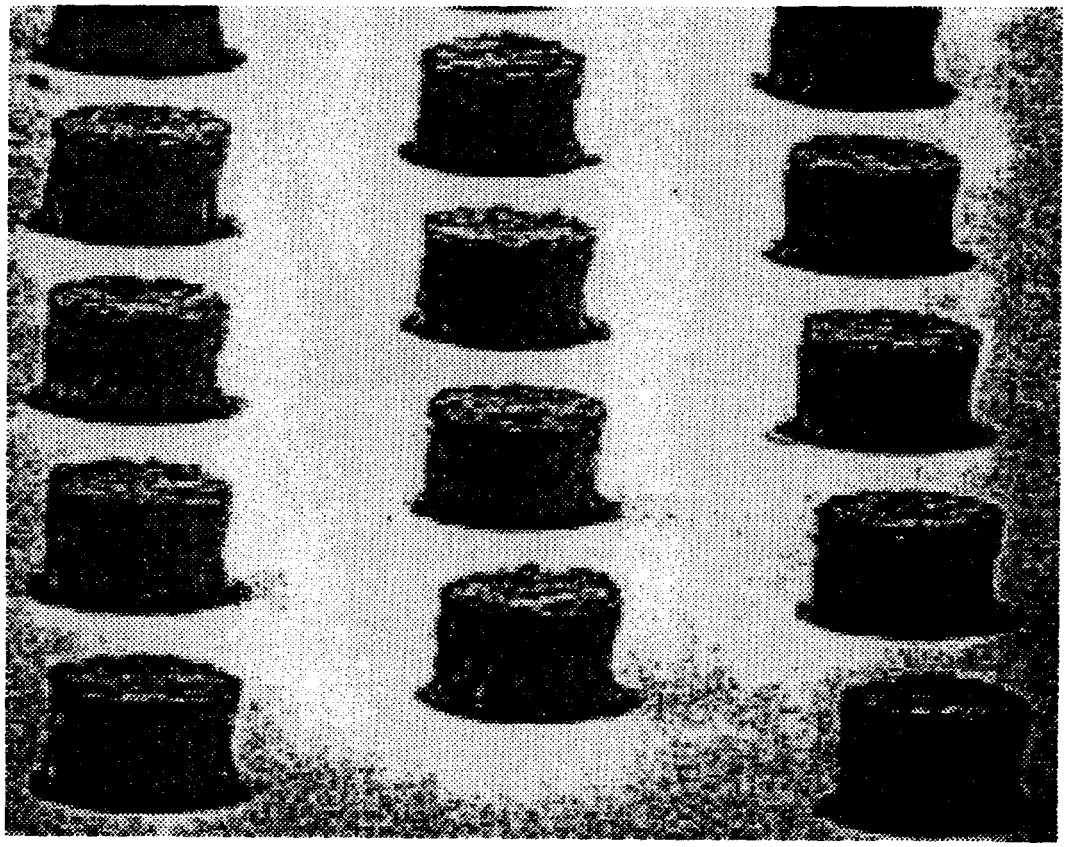
HIGH PERFORMANCE LOW COST INTERCONNECTIONS FOR FLIP CHIP ATTACHMENT WITH ELECTRICALLY CONDUCTIVE ADHESIVE

DARPA TRP No. DE-FC-04094AL98817



DISCLAIMER

FORWARD

This final report is a compilation of final reports from each of the groups participating in the program entitled "High Performance Low Cost Interconnections for Flip Chip Attachment with Electrically Conductive Adhesive", project number DE-FC-04094AL98817, sponsored by DARPA TRP. The main three groups involved in this effort are the Thomas J. Watson Research Center of IBM Corporation in Yorktown Heights, New York, Assembly Process Design of IBM Corporation in Endicott, New York, and SMT Laboratory of Universal Instruments Corporation in Binghamton, New York. The group at the research center focussed on the conductive adhesive materials development and characterization. The group in process development focussed on processing of the Polymer-Metal-Solvent Paste (PMSP) to form conductive adhesive bumps, formation of the Polymer-Metal Composite (PMC) on semiconductor devices and study of the bonding process to circuitized organic carriers, and the long term durabililty and reliability of joints formed using the process. The group at Universal Instruments focussed on development of an equipment set and bonding parameters for the equipment to produce bond assembly tooling. Reports of each of these individual groups are presented here reviewing their technical efforts and achievements. An executive summary has been put together to present in abbreviated form the results of this work. An outline has been compiled as a guide and overview for the contents to each individual report.

EXECUTIVE SUMMARY

This project has developed an isotropic, electrically conductive adhesive, dispense and bond processes and bonding equipment to form a reliable interconnection for Flip Chip Attach (FCA) at a cost competitive with solder assembly. Two groups within the IBM Corporation, at Thomas J. Watson Research Center and at the Assembly Process Design Laboratory in Endicott, NY, collaborated with Universal Instruments Corporation to complete this research effort.

The efforts at the IBM Research Center focus on the development of the Polymer-Metal-Solvent Paste (PMSP) materials systems which is a composite of thermoplastic polymer binder, conductive silver particles, and a solvent. The Research team focused on key materials properties of not only the PMSP but also the resulting Polymer-Metal Composite (PMC) formed once the solvent is driven off. The PMSP is required to be manufacturable and have the appropriate rheological behavior to achieve fine feature dispensability. Once the PMC is formed it requires good adhesion to form mechanically and electrically stable bonds and high electrical conductivity to yield low contact resistance at PMC contact interfaces. The formulations and evaluations have demonstrated several features. Good mechanical compliance enables reliable bond attainment under large thermal mismatch between the semiconductor and the organic chip carrier. The material is dispensable at the wafer level for bumping semiconductor devices. The PMC interconnect can withstand industry standard environmental stresses. The PMSP has a long shelf life at room temperature. The electrical conductivity can achieve 25 micro ohm cm and provide stable joint resistance's of less than 10 milli ohms. Low alpha particle emissions were demonstrated which can minimize occurrence of radiation-induced soft error rates in electronic devices.

The efforts at the IBM Assembly Process Design Laboratory in Endicott, NY focused on process development for paste deposition, chip bonding, encapsulation material selection and processing, and PMC reliability testing in industry standard tests. The paste deposition process involved the development of a photo bumping process to deposit PMSP onto chip pads of a wafer. Flat surface bumps nearly 0.004" high, 0.008" diameter on 0.020" pitch were achieved with a high yield per chip. The chip bonding process effort was focused on process optimization for high speed assembly under controlled time temperature and pressure conditions to 135psi pressure, 235C temperature, and 30 seconds time at temperature. This set of parameters resulted in acceptable bond strengths with acceptable mechanical and electrical integrity. Several underfill encapsulant materials were investigated which resulted in selection of Matsushita CV5183S as the best candidate. Chip and card test vehicles were assembled using these process conditions and materials and subjected to stress tests including accelerated thermal cycling, thermal aging and temperature and humidity testing. Ten sets of stress trials were completed for test chips with PMC bumps bonded to laminate test cards. Results demonstrated the feasibility of reliable and stable PMC interconnection between chips and laminates with gold pads.

The efforts at Universal Instruments focused on placement and bonding equipment experimentation to determine the equipment related process parameters needed for a successful process. The work included construction of a variety of manual and fully automated test beds used to support the experimentation. A Computer Aided Cost Estimation (CACE) software tool

was developed to help understand the tradeoff issues when comparing the PMC process to those using conventional solder based Flip Chip Attachment. The set of optimal time, temperature, and pressure bonding parameters were found for the attachment of IBM supplied PMC bumped flip chips to laminate Printed Wiring Board (PWB) material using the Prototype bonder. With total bond cycle times of approximately one minute competitive assembly processing compared with solder based processes were achieved.

Key features of the resulting process include elimination of fluxing for metal oxide removal, elimination of lead, reworkability of the conductive bumps due to the thermoplastic nature of the PMC, and elimination of the necessity for solder mask pad isolation in the chip site on the organic chip carrier. Any new studies will focus on progression to finer pitch bumping feasibility for dual use application development for microelectronic products.

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Conclusions
Future Work

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Polymer/Metal Composite for Flip Chip Attach Interconnect: Material Development

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Polymer/Metal Composite for Flip Chip Attach Interconnect: Material Development

Motivation:

Spurred by increasing miniaturization that requires higher functionality in smaller spaces, flip chip attach (FCA) is becoming more attractive than the conventional wire bonding and tape automated bonding methods currently used in chip level interconnection. The average annual growth rate for FCA interconnects for the next five years is expected to be about 38% compared to less than 15% for wire bonding.

The largest growth rate is expected to be in low end applications where the chip is bonded directly to a relatively inexpensive organic board rather than an expensive ceramic substrate. It is difficult to make a stress-free structure using conventional FCA technology using solder material interconnects because of the large differences in the thermal expansivity between the organic board and also due to the chip and the rigidity of the solder interconnect. Furthermore, the critical material dispensing methodology, to ensure the shape and composition of the interconnect is uniform, makes conventional FCA difficult to perform requiring significant skills that are not readily available. To practice FCA, a typical assembly manufacturer would most likely be forced to have the FCA solder interconnect out-sourced to an expert house such as IBM, Delco, etc. As a result, the cost of manufacturing to the assembler increases.

In this project, we have tried to develop a material and technology that addresses the salient challenges of the conventional FCA technology posed by low-end assembly applications; such as stress due to thermal mismatch, rework, and soft-error due to α-particle emission from solder interconnect. Furthermore, the assembly process, that primarily requires a dispensing and bonding step, is fairly simple so that it can be practiced by any assembly house.

It should also be pointed out that the technology developed and reported here is not a replacement to conventional FCA technology but complimentary to it. The present process is more suitable to lower end products where the interconnect diameter is not too small and the pin count is not very high. For the present study, we have been able to achieve reliable chip to organic board structures with diameters of the interconnects ranging from 250-165 μm and their pin count less than 300. (The reliability study in the smaller diameter range is limited). In contrast, conventional FCA on ceramic board is well proven for 100 μm interconnect size with pin count over 1000. Low end products, such as memory or ASIC chip on laminate board, would be ideal applications for this FCA technology.

Property Requirements: The FCA Structure

Fig. 1 shows a typical structure where a silicon chip is attached to a circuit board or a substrate using interconnects. The area surrounding the bonded regions is subsequently encapsulated using a filled thermoset material. In the case studied, we replaced the solder interconnect with a polymer/metal composite (PMC) material where the polymer binder is a thermoplastic material. The substrate is an organic board typically made of glass particles embedded in an epoxy matrix. The encapsulant is either silica or alumina particle filled epoxy. The terminal metallurgy on the interconnect pads on the chip and the board is an oxide free metal, such as Au, Pd, or Au/Sn alloy.

To achieve this structure, the PMC material has to have basic properties: (i) Appropriate rheological behavior to achieve fine feature dispensability. (ii) Good adhesion to make a mechanically and electrically stable bond that can withstand the environmental stresses and processing operations, such as, encapsulation. (iii) High electrical conductivity to give low bond resistance with (more importantly) small variations in resistance among the PMC interconnections in the chip.

To make the PMC based FCA (PMC/FCA) manufacturable, the material must have these additional characteristics: (a) Good mechanical compliance to attain reliable bond under large strain caused by thermal mismatch. (b) Material should be dispensable at wafer level. (c) The PMC interconnected structure should withstand environmental stresses as per industry standards. (d) The material should have a long shelf life, preferably at room temperature. (e) The process steps should have appropriate logistics, i.e., compatible with other assembly processes. (f) The required equipment set for assembly should be available. (g) The assembly process cost should be lower or comparable to conventional flip chip process, i.e., C4 technology.

Concept of PMC/FCA Technology

Fig. 2 shows the basic scheme to bond two surfaces using the PMC material designed at IBM. We start with a paste composed of a thermoplastic polymer, silver particles, and solvent. This will be subsequently referred to as Ykt-paste or Yorktown-paste, and abbreviated as PMSP. The paste, with appropriate rheological properties, is placed on the I/O pad of the chip or substrate by either screening, stenciling or nozzle-dispensing. Since the conductivity of the interconnect is due to silver particles that form an electrical connection by contact, the terminal metallurgy of the I/O pads on both the chip and substrate need to be oxide free. The appropriate metallurgy discussed later in the report are Au, Pd, or Au/Sn alloy.

The dispensed PMSP is then dried at around 70 °C to drive off (most of) the solvent to form a dried bump. The dried bump is then bonded to the other pad by heating the surfaces to temperature T_B for bond time t_B and at pressure p_B. During the bonding process, the residual solvent is liberated and the material densifies to form a PMC bond. The optimum bonding parameters and their interplay are discussed later. To note also is that if the PMSP is dispensed on the chip surface, the chip may be stored indefinitely in a dried bump state before bonding, making the PMC/FCA technology similar to a C4 method. In contrast, epoxy-based materials

would have to be bonded within a short time span after the paste is dispensed as they can not be stored except at frigid temperatures.

Dispensability and Paste Rheology

The rheology of the paste, (PMSP), is key in defining the following structural features of the FCA interconnection:

- Feature size of the interconnect
- Pitch of the interconnect
- Planarity of the PMC bumps
- Height of the interconnect

The first three properties above will determine the limits of the dimensions and density of I/O's the package can have. The fourth property is crucial in determining the reliability of the package, i.e., integrity on thermal shock, encapsulant underfill and life-time of the interconnection. Furthermore, the rheological behavior may also play an important role in determining the dispensing method, i.e., simple screening, extrusion screening, syringe dispensing, etc.

In a typical dispensing operation, the shear rate of the squeegee is well over 100/s. Thus, the rheological evaluation scheme should measure the dynamic response of the material in this range. The dynamical feature of the process corresponds to a Reynolds's number significantly less than unity, i.e., creeping flow regime. This signifies that the viscous terms are more important than the inertial effects during the dispensing operation. Owing to these kinametic and dynamic features of the flow, we have designed experiments using a cone-and-plate viscometer where the material response under a constant shear rate is measured.

Fig. 3 shows a typical cone-and-plate geometry used in our studies. The sample is placed in the gap between the cone and plate. The angle of the cone with respect to the horizontal is, θ_0=0.02 radians and the diameter, D of the plate (and the cone) is 25 mm. At a 10^3/s shear rate, the typical viscosity is about 10^2 P. The characteristic distance scale, L is about 5×10^{-4} m (largest gap), the maximum velocity, V is about 12.5 m/s (corresponding to maximum angular velocity of 10^3/s), and density, ρ of the paste is about 2.5×10^3 kg/m^3. This corresponds to Reynolds number of,

$$Re = VL\rho/\eta \sim 0.16 \qquad (1)$$

Thus, consistent with the dispensing process, the flow is in the creeping flow regime.

Compatible with dispensing operation, the shear rate range for measurement is up to 10^3/s. The coriolis force to expel the fluid as the cone rotates is ~30 MPa and the restoring force is at least, $\tau_{\theta\theta} \sim 800$ MPa. Therefore, the paste sample will remain trapped in the gap during the experiment. This is expected because we are in the creeping flow regime.

The rotating shaft is spring loaded to measure the normal force due to the elastic component of the paste. The total shear force is measured by determining the torque on the plate. The shear rate, γ, the non-Newtonian viscosity, η, are calculated from the angular velocity and the torque, T as:

$$\gamma = \omega/\theta_0 \quad (2)$$

and,

$$\eta = 12T/\pi\gamma R^3 \quad (3)$$

Finally from the normal force, F, the first normal stress difference, $\tau_{11} - \tau_{22}$ can be calculated as,

$$\tau_{11} - \tau_{22} = 8F/\pi D^2 \quad (4)$$

Since the shear rate, γ is constant in the fluid at a given ω, by measuring the torque, T and normal force, F as a function of ω the shear thinning behavior and the viscoelastic nature of the material can be quantitatively measured. Fig. 4 shows a typical curve for one of the Yorktown paste systems.

The following parameters in Fig. 4 are of interest:

- Zero shear rate viscosity, η_0
- On-set of shear thinning behavior, γ_τ
- Shear thinning exponent, n (defined in eq. 5)
- Normal force, F

The zero shear viscosity is an important parameter to determine the stability of the paste. A high η_0 is desirable for longer shelf-life. The on-set of shear thinning, γ_τ is important in determining the process conditions. A low γ_τ implies that a high-shear screening process may not be needed. It should be noted that γ_τ is also nominally the onset of elastic response, and is desired to be regulated at lowest possible values. A simple Ostwald-de Waale model (5) simulates the generalized Newtonian behavior in the shear thinning regime. The viscosity is given by,

$$\eta = m\,|\gamma|^{n-1} \quad (5)$$

where, m is the Newtonian viscosity, η_0 and exponent, n determines the shear rate response of the fluid. For $n > 1$ the material is shear thickening or a dilatant fluid, for $n < 1$ the fluid is shear thinning or pseudoplastic, and n=1 corresponds to a Newtonian fluid. As will be discussed later in Table 1, Ag-filled pastes have $n < 1$. The last parameter is the normal force, F. The normal force causes the paste to recoil out of the screening aperture. If we assume a simple power law with a negligible small second normal stress difference compared to the first normal stress, the recoil normal force, N can be calculated as,

$$N \sim n(\tau_{11} - \tau_{22})/3 \quad (6)$$

The assumption of lower second normal stress difference compared with first normal stress difference is generally valid for all polymeric fluids and their mixtures with the exception of

fluids that are self-organizing. We note that in our systems, $(\tau_{11} - \tau_{22})$ is at most $5x10^5$ dynes/cm^2 corresponding to a normal force N ~ $8x10^4$ MPa only! Thus, in this study we can neglect the elastic recoil property.

Another important criteria for careful analysis of the paste system is the particle rearrangement during screening. Fig. 5 shows the shear rate response of the paste after consecutive runs. The zero shear viscosity, η_0 drops from ~ $20x10^3$ P to $8x10^3$ P after the first scan. This implies that the particles rearrange significantly during the first scan causing higher internal friction that leads to a larger viscosity. The drop in η_0 suggests that the silver flakes tend to align with their surfaces parallel to the shear plane. Differences between subsequent scans is not significant, indicating that the morphology is stable.

Fig. 6 shows the shear rate response of three of our "optimized" pastes labeled Paste A, C, and D with two commercially available pastes labeled CM1 and CM2. CM1 is Ablestik one of the best Ag-epoxies on the market today with respect to electrical properties and screenability. CM2 is Staystik one of the best thermoplastic-based materials on the market. To note is that commercially available thermoplastic-based materials, including CM2, tend to exhibit very low η_0 and as a result have a short shelf life and dissatisfactory screenability (as will be seen in Fig. 8). The Ag-epoxies have longer shelf life but require storage at -40 °C. Yorktown-pastes have a shelf life well over 6 months at room temperature.

Table 1 shows the various parameters for five pastes, two commercial and three typical Yorktown pastes. We expect a larger n for epoxy-based materials (CM1) compared to thermoplastic materials because the epoxy is not polymeric in the paste and as a result should not exhibit significant pseudoplastic responses. However, the CM2 (a thermoplastic) is expected to exhibit a small n. The reason for this discrepancy may be due to inadequate wetting of the polymer on the Ag and agglomeration of Ag particles.

Table 1 shows that the n in the range 10-10^3/s for both CM1 and CM2 is significantly larger than typical Yorktown pastes labeled Ykt.1 Ykt.2, and Ykt.3. This gives our material two distinct advantages:

1. Even though the η_0 for Ykt.1 to 3 is large, the η in the shear rate range corresponding to screening operations is small. In some cases, it is lower than CM1 and CM2.
2. A low n also further diminishes the normal recoil force, N. For example, CM2 has the lowest F among the select list of competitive polymer based materials. Although the N at 10^3/s for CM2 is 5 folds lower than Ykt.2 (highest among all the five pastes reported), the n of Ykt.2 is 3 fold lower than CM2 (see Table 1), as a result the recoil force, N of Ykt.2 is only 30% higher than that of CM2.

Fig. 7 shows the viscous response as a function of Ag loading. The loadings are all in weight percentages. For the same polymer solution concentration, the effective viscosity at low γ, i.e., η_0 decreases as the Ag loading increases showing that the viscosity is essentially due to the polymer flow. The contribution from the drag due to Ag particle does not change

significantly at loadings of 75% and 88%. However, the onset of shear thinning shifts from $\gamma <$ 10/s for the paste compared to $\gamma >$ 100/s for the pure polymer. Importantly, in all cases, the η_0 is larger than that of the pure polymer indicating good dispersion of the particles. Furthermore, F is higher than the pure polymer also indicating good dispersion. Thus, the behavior illustrates the wetting nature of the polymer; an important criteria for ensuring the stability and shelf life of the paste.

Based on our experiments discussed above, the Yorktown paste has a larger η_0, smaller n, reasonable F corresponding to a low N, and low γ compared to the best commercial materials, leading to better screenability. Fig. 8 compares two feature sizes screened through a Molybdenum stencil for the five pastes reported. The features are circular with the following dimensions:

1. 100 μm diameter at 225 μm pitch
2. 170 μm diameter at 225 μm pitch

Visual comparison points out that Ykt.1 and Ykt.2 are superior compared to the other pastes discussed in this report. Subsequently in the report Ykt1 is labeled paste A, the first optimum paste that was tested in some detail by the Endicott team.

The parameters described above are not independent of each other. Therefore, defining an operating window is quite complex and depends on the interplay and synergy of all the above criteria. Nevertheless, the trends numerated above should serve as a guide to optimize the paste rheology for fine-feature-screening. Some broad criteria to select a paste for fine pitch screening may be concluded:

1. High η_0, preferably in the range $5x10^3$ to $2x10^4$ P
2. High shear thinning index, n in the range of 0.2-0.05
3. Viscosity at 10^3/s in the range of 20-200 P
4. Low normal force, F below $5x10^5$ dynes/cm^2

Electrical Properties

It is well known that electrical conductivity in metal/dielectric mixtures is achieved when the volume fraction of the electrically conductive component (usually conductive metal particles) is over a certain fraction defined as the percolation threshold, ϕ_c. Theoretical calculations indicate that if there is no specific correlation between the conducting particles, i.e., the mixture is random, the threshold ϕ_c for a three dimensional structure is ~0.16. However, in conventional metal particle/polymer mixtures, $\phi_c < 0.2$. due to the clustering of the particles.

Fig. 9 shows an experimental percolation curve for our PMC where the Ag particles are ~5 μm and the ϕ_c~0.36. More interestingly, the conductivity of the composite for Ag particle volume fraction, $\phi < 0.4$ is better than eutectic Sn/Pb solder. In this study, we have optimized the

properties for Ag loading, ϕ in the range of 0.42 to 0.47 and the resistivity is ~20 $\mu\Omega$-cm compared to 30 $\mu\Omega$-cm for eutectic Sn/Pb solder. The 'optimum paste I' is Paste A. The second generation 'optimum paste II' is labeled as Paste D in this report.

The resistivities are measured using a 4-point probe method shown in Fig. 10. A 4.75 mm wide strip of the paste is deposited by screening through a 100 μm thick Molybdenum stencil between the two Au electrodes. After drying and heating to 220 °C, a constant DC current is passed through the Au electrodes and the potential drop between P1 and P2 is measured using Au coated probe pins. The P1 and P2 test points are reasonably far from the electrodes to avoid any current non-uniformities due to edge effects. The contact force at P1 and P2 is <0.007 Pa to avoid any sample deformation. Fig. 11 shows two I/V curves of Ag loadings corresponding to the plateau region in ϕ=0.42-0.47 range (i.e., 24.4 $\mu\Omega$-cm) and in the region close to ϕ_c (i.e., 711 $\mu\Omega$-cm). We note that in highly conductive samples, Ohm's law holds for current densities up to 10^4 A/cm^2.

To further confirm the resistive behavior of the PMC, we measured the I/V curves as a function of temperature. Fig. 12 shows an increase in resistivity with temperature for PMC at ϕ=0.39. The resistive behavior is confirmed in Fig. 13 where a linear decrease in resistivity is observed as the sample is cooled from 300 to 4 K. If the electron hopping between the Ag particles was thermal, analogous to metal/insulator/metal structures, the resistivity would increase as the temperature decreases. The above behavior suggests electron tunneling between the Ag particles. Although the tunneling is temperature independent, the decrease in resistance is caused by decrease in phonon scattering of electrons in the Ag particles. Thus, from the thermal mechanism we conclude that the conduction mechanism involves electron tunneling between the particles and resistive conduction in Ag. The over-all conductivity is determined by the number of percolation path explained above with reference to Fig 9.

Next, we measure the contact resistance. We designed a method to measure both the contact resistance, R_C, and adhesion simultaneously, as shown in Fig. 14. A 4 mm diameter paste feature is screened through a 100 μm thick Molybdenum stencil on one surface of two copper 'L' shaped pieces electroplated with Pd/Ni. The paste is dried at 70 °C and subsequently bonded at 220 °C under a load, F, to form a structure as shown in Fig. 14. The magnitude of F is less than 1 MPa. A 4-point probe method is used to measure the resistance by passing constant DC current through A and D and measuring the potential drop between B and C. The width of the 'L' is 6.2 mm which is significantly larger than the bond size to ensure uniform current distribution. The thickness of the bond is ~40 μm. Table 2 shows R_C as a function of ϕ. The measured contact resistance is well below 1 $\mu\Omega$-cm^2.

After the R_C measurements, the sample is subjected to a tensile strain at 0.025 cm/min. Fig. 15 shows a typical stress-strain curve for bonding at 220 °C and applied load, F. The measured adhesion strength as a function of Ag loading is shown in Table 2. To note is that the paste formulation in this example is a typical example, it is not the optimum composition. The behavior of the optimum formulation is discussed in the next section.

Fig. 15 denotes that the maximum strain at the breaking point is over 100%. The latter indicates that the bond is compliant enough to endure significantly larger thermal mismatches than conventional solder bonds (C4 or eutectic Sn/Pb interconnects) and Ag-epoxy bonds. This large compliance further suggests that the interconnect height requirement may not be as stringent (i.e., large) as that in C4 technology, provided the electrical response does not change during strain. The mechanical properties and bond compliance are discussed in the next section.

Time domain reflectometry (TDR) studies on the Yorktown paste were performed in Dr. Len Schaper's group at the University of Arkansas. Coplanar transmission lines, 5 cm. long, were tested in the TDR studies. The Yorktown paste was compared to aluminum. The aluminum lines were 2 μm thick and 160 μm wide. The paste lines were 150 μm thick. The thickness of the paste was such so that the impedance of the Al and paste lines were comparable, viz., 7.4 Ω. and 8 Ω, respectively. The DC resistance measurements were two-point probed, thus include the contact pad resistance. The coplanar ground conductors were 290 μm from the center line.

The TDR measurements gave excellent results. The target impedance of the transmission line was 50 Ω, and the paste line measured 42 Ω. Both the paste and Al lines had ~ 460 ps delay between the input and output, i.e., 92 ps/cm delay. The output pulse rise time for paste and Al was 190 ps and 213 ps respectively. The pulse measurements attest that the high frequency response of the conductive adhesive is metallic. Thus, the conductive adhesive may be used as an interconnect material at frequencies in the GHz range.

Adhesion and Mechanical Properties of the Bond:

The last salient property of PMC pertains to the mechanical stability of the FCA structure. The adhesion is measured by subjecting the bonded surface under a tensile load. The stress at break (of the bond) is reported as the adhesion strength. Two types of sample geometries were chosen: (i) Two elbows coated with Au or Pd/Ni were bonded by PMC as shown in Fig. 14. (ii) Two blanket Au coated silicon wafer bonded by 226 bumps that are 10 mil in diameter on 20 mil pitch.

The first method (i) was mainly designed for contact resistance measurements and has been described before. The stress-strain curve for the optimum paste D is similar to Fig. 15 with a breakpoint occurring over 100% strain. However, the bond strength is about 18 MPa which is significantly larger than prior formulations. Furthermore, the contact resistance is also significantly better than the formulations listed in Table 2.

In method (ii), the array screened on a blanket Au coated 1 x 1 cm silicon chip is shown in Fig. 16. The bumps are screened through a 4 mil thick Molybdenum stencil. The bumps are dried at 70 °C for 60 sec. The dry bumped chip is then bonded to a 1" silicon wafer substrate also coated with Au. The bonding is performed in special chip bonder designed by Research Devices. The chip is placed on the substrate at 30 °C, then a pressure of 200 psi is applied and the assembly is heated upto 240 °C. The sample is maintained at 240 °C for 60 sec.

Subsequently, the load is removed and the sample is air cooled to room temperature. A stainless steel peg is attach to the chip and the substrate is glued to a 2" Pyrex disk. The stress-strain curve is obtained by holding the lower Pyrex disk in a special jig and pulling the stainless steel peg in an extensometer. Fig. 17 shows a typical stress-strain curve for Paste D. Fig. 18 shows a typical SEM micrograph of the sample after the failure. To note is that some portion of the material is present on both the chip and the substrate side indicating that the mode of failure is cohesive.

One of the most important reliability concerns is the mechanical and electrical integrity of the PMC bond under thermal cycling. The origin of the stress on the bond is due to the thermal mismatch of the structure parts that induces a shear stress, ε given by,

$$\varepsilon \sim \Delta\alpha\Delta T/h \quad (7)$$

Where, $\Delta\alpha$ is the difference between the in-plane, linear thermal expansion coefficient of the chip and the substrate, ΔT is the temperature difference, and h is the height of the interconnect. We assume the chip is 1x1 cm. It is important to note that ε will increase if the substrate is organic instead of ceramic. Furthermore, to lower the ε, the bond height should be increased to the largest possible value. The h is fixed by the size, shape, and pitch of the features to be screened, the method for dispensing, and the bonding process. For a typical FCA geometry (1x1 cm chip, 75 μm bump height), ε ranges from <2% for typical glass ceramic substrate to as high as 18% for an organic carrier, such as FR4. The temperature difference is assumed to be 100 °C. Thus, the question is whether the PMC can withstand 20% strain. From the stress-strain curve shown, for example, in Fig. 17, the PMC is compliant to withstand the 20% thermal strain. However, to prove the reliability of the bond under strain, a direct measurement is important. This is considered next in Figs. 19-21.

Before we discuss the compliance behavior of PMC, we consider the effects of temperature. Fig. 19 indicates that on the first heating the PMC behaves in a nonlinear manner. However, on subsequent cooling and heating cycles the resistivity follows a linear behavior typical of an ohmic material. Therefore, electrically PMC is ohmic under thermal cycling. This is consistent with observation noted in Figs. 12 and 13.

PMC is a composite material of silver particles dispersed in polymer matrix. It is reasonable to expect that under tensile load the particles will tend to move farther apart increasing the particle-to-particle and particle-contact pad contact resistance. To measure this behavior, we devised a special measurement to probe (the true four-point probe) contact resistance during tensile deformation. Fig. 20 shows a typical contact resistance versus strain behavior. Up to 50% strain, well above the required strain limit of 20%, the contact resistance is nominally constant (as seen from the % contact resistance change axis on the right hand side y-axis).

In most applications, the structure is usually subjected to a thermal cycle: (a) during the bonding process, (b) as the appliance is turned on and off. Thus, the hysteresis behavior is also important. Fig. 21 shows the contact resistance characteristics as the PMC is subjected to a loading-unloading cycle. We note that in a cycle up to 60% strain, the contact resistance change

is insignificant. This indicates that the interconnect is resilient both electrically and mechanically under large strains. Furthermore, the reversibility for strains <40% suggests that FCA to organic substrates should be feasible.

Miscellaneous Properties

Apart from the three salient properties described above, for the material to be attractive for FCA it must also have several other properties. Most of the material related issues with respect to assembly will be discussed in a later section. Some of the aspects not touched in these later sections are described here. The properties we discuss are:

- Shelf-life
- α-particle emission
- Bump height variability
- Reworkability

Shelf Life:

One of the major advantages of a thermoplastic based paste is that low temperature storage is not required. However, owing to ~10 fold higher density of the Ag-filler particles relative to the polymer binder, there is some sedimentation in a quiescent mixture. We have significantly reduced this sedimentation rate by improving the particle/polymer interaction thru optimization of Ag particle characteristics, proper choice of the polymer binder, and compounding process. Nonetheless, the paste needs to be mixed manually for 30-60 seconds to homogenize the particles before dispensing operation. It is suspected that such a low-shear mixing process will tend to entrap air that may lead to a porous bond. A porous interconnect can affect the properties of a structure in two distinct ways:

- It can reduce the ultimate bond strength of the PMC by acting as a nucleation site for cracks.
- During the under-filling process, the encapsulant can be incorporated into the PMC bond producing detrimental effects, such as swelling.

We studied the effect of low-shear stirring on the behavior of the bond strength. A quantity batch of freshly compounded paste was partitioned into three batches. The paste used was Paste A in this example. All bonds were made on an as received Pd/Ni coated 'L' described elsewhere. The first batch was not stirred and was the control sample. The second batch was stirred for less than 10 mins. The third batch was stirred for 40 mins. while 25% by volume of air was slowly injected into the material. Similar 'L' bonds were made from this batch immediately after the mixing operation. Fig. 22 compares the typical stress-strain curves for PMC bonds made from the three batches.

The bond strength, as defined by the stress at the breakpoint of the bond, for the control and the '10 min. stirred' pastes are similar. The strain at the breakpoint is large (well above 5% in comparison to solder bonds). However, a significant degradation of the bond strength is observed for the third batch. This degradation of batch #3 proves that entrapped air will reduce

the bond strength significantly and is therefore a concern for reliability. Nevertheless, a stirring process up to 10 mins. does not affect the paste's bonding characteristics significantly. Since the stirring time required for a paste stored for a year is less than 5 mins., we can safely conclude that the paste has a shelf-life of at least 6 months at room temperature.

α-Particle Emission

The advent of CMOS technology to design low power, high functionality chips has posed a difficult problem of soft error generation. The random generation of α-particles from the Pb-containing interconnects produces an electrical noise comparable to the (low power) signal in the chips. As a result, the interconnect has a significant soft error rate (SER). Pb-containing solder material with acceptably low α-particle emission is more expensive and limited by the world supply. The present C4 technology is a Pb-rich Pb/Sn alloy used to interconnect chips directly to a circuit board. C4 is pervasive in the industry. In this study, we present a novel interconnect material and a bonding scheme to achieve flip chip attach of a chip to a substrate with acceptably low levels of α-particle generation. Alpha-Induced SER is driven by the presence of radioactive impurities in C4 lead. In contrast to cosmic SER, alpha SER is highly sensitive to Qcrit. (Qcrit is the amount of charge injection into a node that will modify the state of a circuit). In the next generation CMOS chips, chip designers will have to consider SER along with the density/performance/power/reliability tradeoffs.

Efforts to minimize SER are at two levels: (a) Design circuits to lower the sensitivity to charge injection from α-particle impact; and (b) Develop Pb-free interconnect materials and technologies (replacing current C4) to reduce α-particle emission/generation.

The filler for the present PMC is Ag, a low alpha particle emission is expected. The total generation for a PMC sample over a two week period was 0 ± 5 counts/cm^2.

With low alpha emission and excellent interconnect properties, PMC may prove to be a solution for low SER.

Bump Height Variability

In conventional C4 technology for FCA the height of the interconnect bumps is required to be very uniform (within a couple of microns). By contrast, screened PMC interconnect bumps have larger variation in heights. Fig. 23 shows 6.5 mil diameter bumps that are deposited through a 2.5 mil thick Molybdenum stencil. The deposited bumps are dried at 30 °C for 30 sec. Fig. 23(a) and (b) show the bumps after the drying process. The bumps are subsequently pressed against a glass substrate at a pressure of 100 psi. Fig. 23(c) and (d) show the bumps through the glass substrate. A low pressure was used to ensure a small deformation of the bumps. Since the contact area varies, not all of the bumps had the same original height. Nevertheless, all the bumps deformed significantly under this small load to make 100% contact with the glass.

A complete deformation resulting in uniform contact is achieved by pressing the dried bumps at a pressure of 100 psi at 220 °C for 60 sec. Fig. 24 shows the resultant bumps. In Fig.

24, the bumps are 10 mils in diameter and are screened through a 3 mil thick Molybdenum stencil.

Reworkability

Since the polymer binder is thermoplastic, interconnects made before encapsulation can be removed by applying a combination of local heat and solvent. Solvents that swell the PMC are NMP, xylene, and iso-propyl alcohol. Local heat, although not essential, tends to facilitate the bond softening process. The preferred temperature range is 80-150 °C, depending on the solvent employed. After debonding, the pads sites can be cleaned using any of the above solvents.

Table 1: Viscous Behavior of Silver Paste

Paste	Zero shear viscosity (Poise)	n
CM1 (Ablestik)	2510	0.40
CM2 (Staystik)	450	0.21
Ykt.1 (Paste A)	14960	0.05
Ykt.2	13340	0.07
Ykt.3	7270	0.13

Table 2: Adhesion Strength and Contact Resistance for PMC

Ag Loading (by volume)	Avg. R_C ($\mu\Omega$-cm^2)	Stress at Break (MPa)
75	0.729	6.5
78	0.617	6.0
80	0.610	6.9
85	0.657	5.2

Figure Captions

Fig. 1: Chip attached to a substrate by flip chip attach using conductive adhesive. The major material and process challenges are indicated.

Fig. 2: The bond between a chip-pad and substrate-pad can be accomplished with or without a drying step. The former method is more suitable for FCA. The paste may be deposited on either or both the pads. The (typical) terminal metallurgy of Al pads on the chip and Cu on the substrate is modified to Ni/Au, Ni/Pd, or any other oxide-free, conductive surface.

Fig. 3: Schematic of Cone-and-Plate viscometer.

Fig. 4: Typical shear rate versus viscosity and normal force for a Yorktown Paste. The zero shear viscosity and n the shear thinning exponent are properties of interest.

Fig. 5: Effect of consecutive runs on the same paste. To note is that the hysteresis effect is insignificant after the first run.

Fig. 6:(a) Shear thinning and (b) viscoelastic behavior of three Yorktown formulations, A, C, and D, and two commercial pastes, Ablestik (CM1) and Staystik (CM2).

Fig. 7: Effect of Ag loading on the rheological behavior of a typical Yorktown formulation.

Fig. 8: Two screened array of 10 x 10 for the five pastes shown in Fig. 6. The feature diameter and pitch are 100 μm on 225 μm and 170 μm on 225 μm.

Fig. 9: Percolation curve for PMC composite.

Fig. 10: Four-point probe method used to measure the bulk conductivity of PMC reported in Figs. 11 and 12. The length of Au electrodes, A = 1 cm and the gap between the electrodes is 4.8 cm. A 4.75 mm (= B) thick strip of paste is screened between the electrodes that is subsequently baked to 220 °C. A constant DC current is passed between the electrodes and the voltage drop at P1 and P2 that are 3 cm apart is measured.

Fig. 11: I-V curves for Ag volume fractions of 0.35 and 0.46 indicate bulk resistivity of 711 and 24.4 μΩ-cm respectively.

Fig. 12: I-V curves as a function of temperature for Ag volume fraction of 0.39. PMC demonstrates an increase in resistivity as temperature increases.

Fig. 13: Resistivity versus temperature of 25% Ag loaded PMC as it is cooled to liquid He temperature. The linear decrease in resistance with temperature indicates metallic behavior.

Fig. 14: A 4-point test probe to measure the contact resistance and bond strength of PMC.

Fig. 15: Stress-strain curve for Yorktown-PMC (paste A) bonded at 0.62 MPa using the design shown in Fig. 14.

Fig. 16: The 10 mil pads on 20 mil pitch used for chip on board testing.

Fig. 17: The stress-strain behavior for paste D.

Fig. 18: The chip and wafer side after the stress-strain test shown in Fig. 17.

Fig. 19: The resistivity as a function of temperature for a typical Yorktown formulation. The formulation is similar to Paste D, except with lower silver content to enhance the thermal effect.

Fig. 20: Using a structure shown in Fig. 14, concomitant measurement of contact resistance as a function of strain is measured for paste D. To note is that the bond can withstand over 100% tensile strain and the contact resistance is reasonably constant up to 60% strain.

Fig. 21: Similar measurement as Fig. 20, except the bonds is strained up to 60% then reversed to 0% strain.

Fig. 22: The adhesive nature of PMC (Paste A) is not significantly altered after stirring the paste for 10 mins. under ambient condition. However, the properties degrade significantly when stirring is continued for 40 mins. and 25% (by volume) of air is syringed into the paste during mixing.

Fig. 23: 6.5 mil diameter bumps deposited through 2.5 mil thick Mo stencil. The 110 bumps deposited are dried at 30 °C for 30 sec. (a) and (b) are bumps after the drying process. The bumps are subsequently pressed against a glass substrate at a pressure of 100 psi. (c) and (d) show the bumps through the glass substrate after pressure.

Fig. 24: 10 mil diameter bumps screened through 3 mil thick Mo stencil pressed at 220 °C and 100 psi load. The bumps are dried prior to squeezing at 100 psi. A complete deformation of the bumps is achieved resulting in uniform contact.

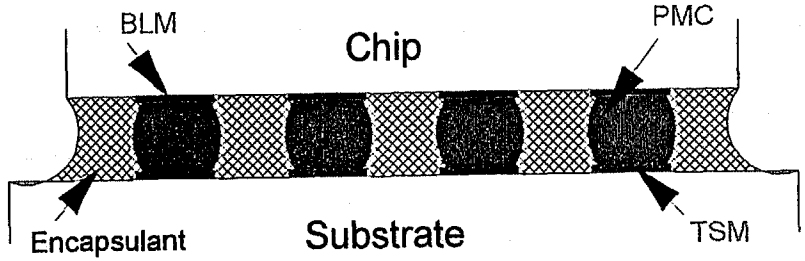
Flip-Chip Attach Technology Challenge

Screenability

Fine pitch
Planarity

Encapsulation

Underfill
Inert to PMC



Adhesion

BLM and TSM
Bonding process

Contact resistance

BLM and TSM
Bulk conductivity

Reliability

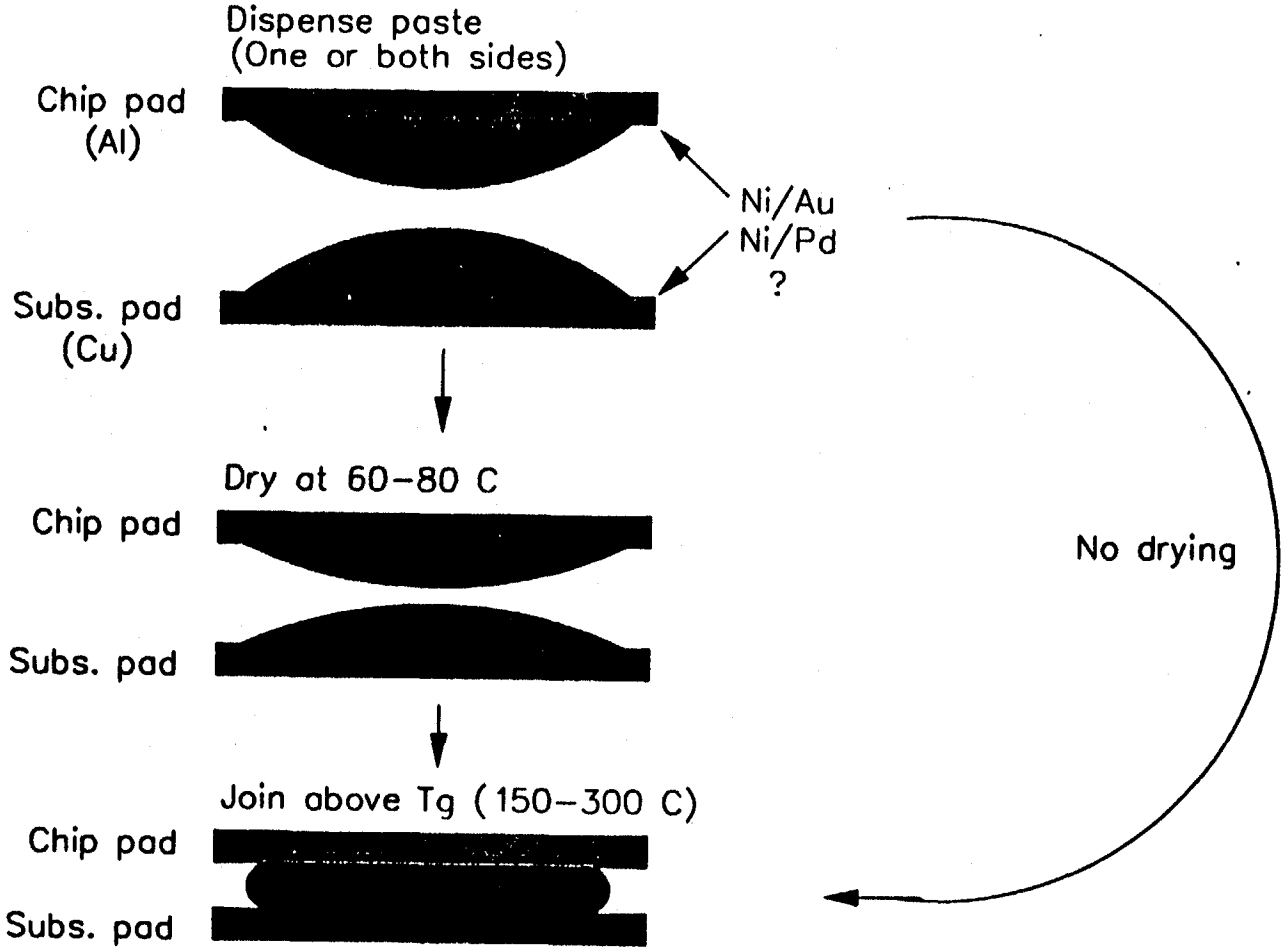
T&H, T-cycle
Thermal shock
Ag migration
Paste Shelf-life

Manufacterability

Paste scale-up
Low cost process
Wafer level screening
Equipment set

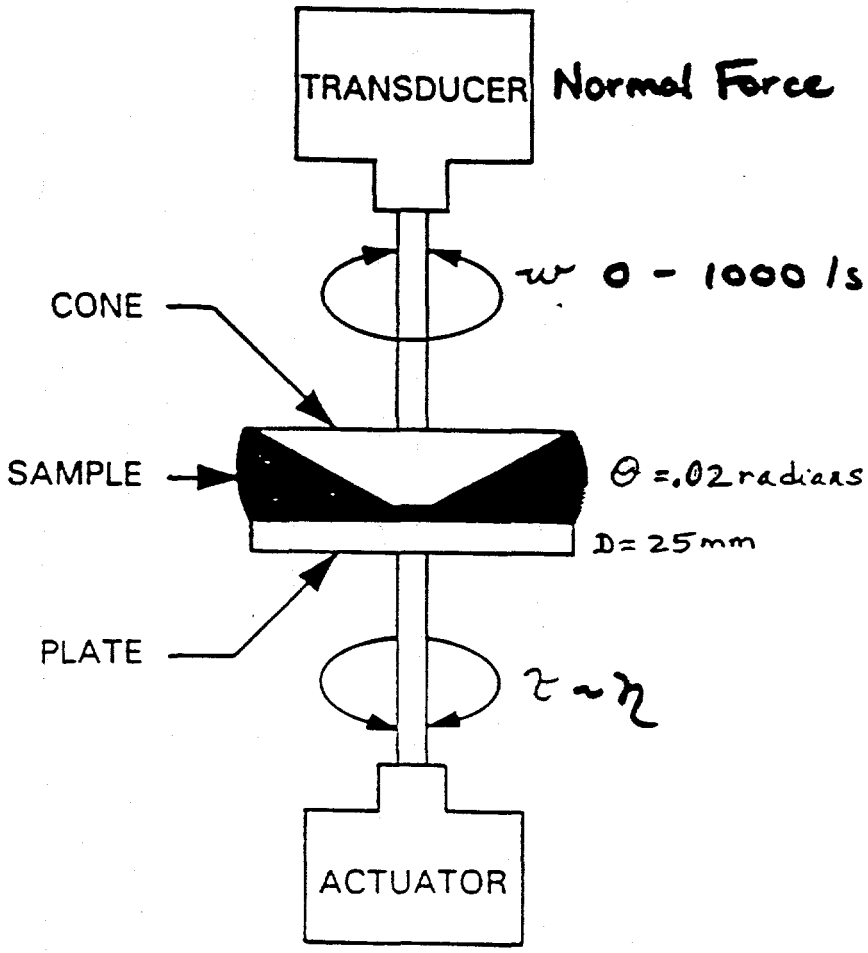
Ravi Saraf
IBM, Yorktown

Polymer/Metal Composite Interconnect Scheme



Ravi Saraf
IBM, Yorktown

Fig 2



$$\eta = \frac{\tau}{\dot{\gamma}}$$

FIG. 3

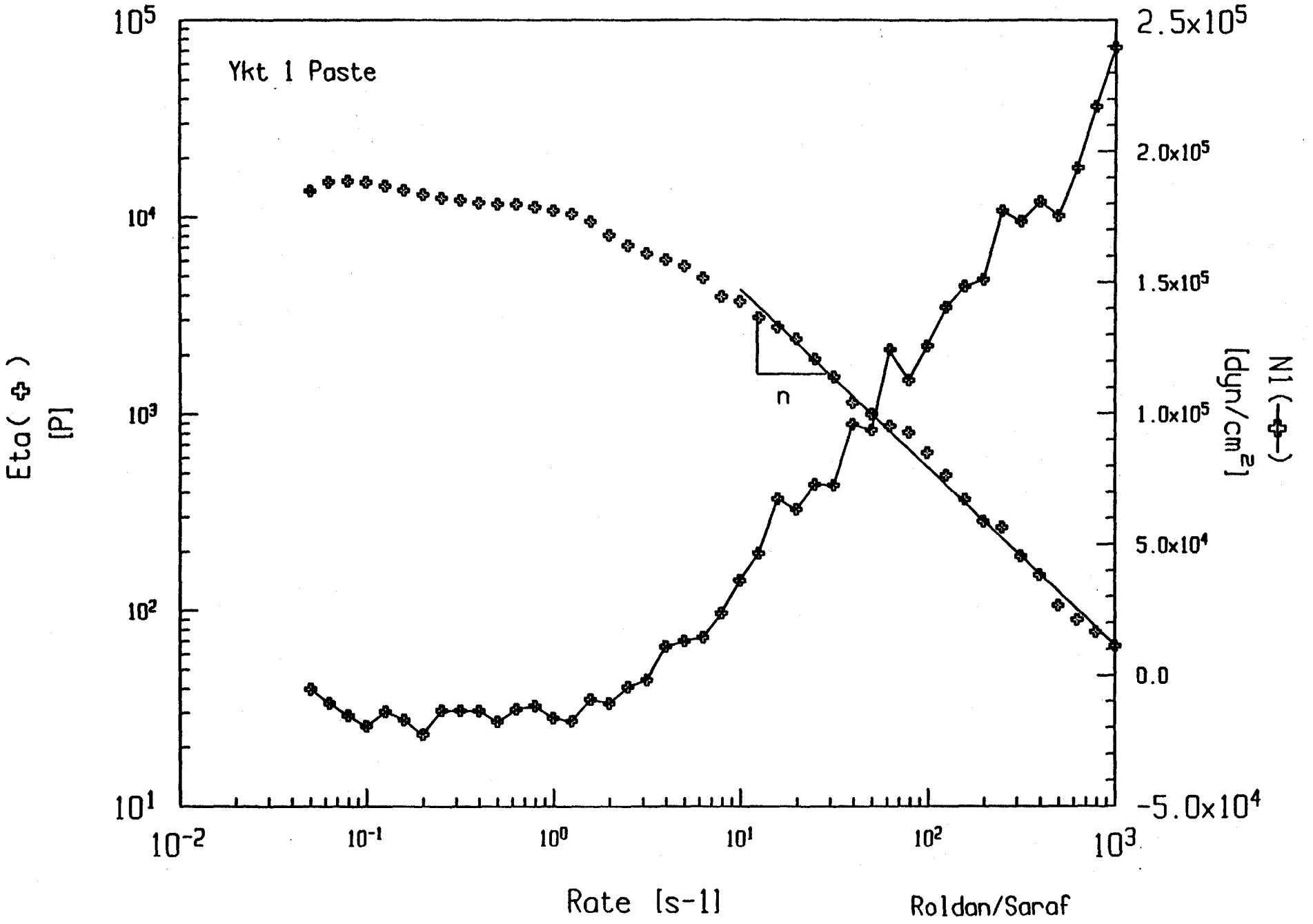

Ykt 1 Paste
Eta(+) [P]
N1(—+—) [dyn/cm²]
Rate [s-1]
Roldan/Saraf
n
10⁵
10⁴
10³
10²
10¹
10⁻²
10⁻¹
10⁰
10¹
10²
10³
2.5x10⁵
2.0x10⁵
1.5x10⁵
1.0x10⁵
5.0x10⁴
0.0
-5.0x10⁴

FIG 4

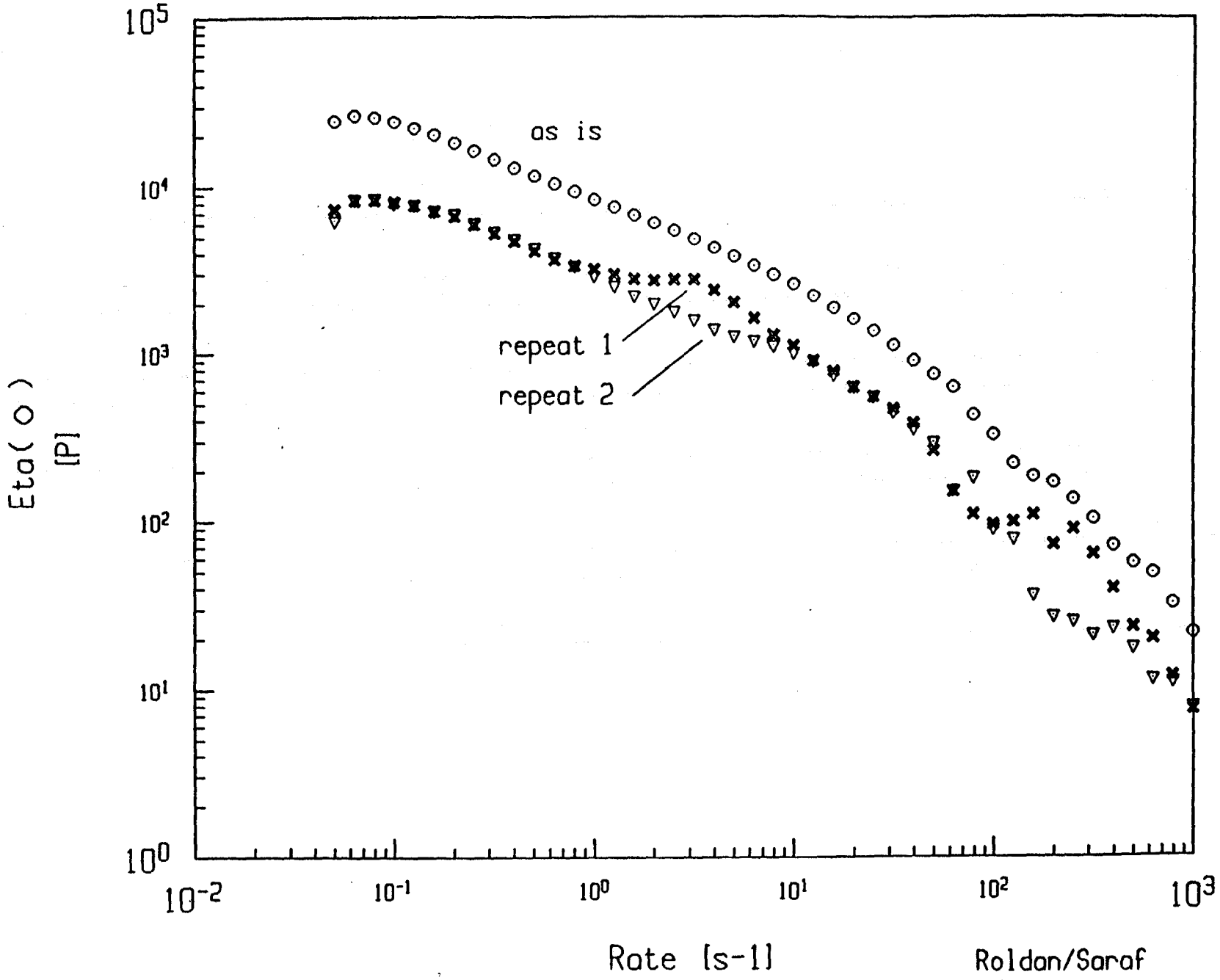

10^5
10^4
10^3
10^2
10^1
10^0
Eta(O)
[P]
as is
repeat 1
repeat 2
10^{-2}
10^{-1}
10^0
10^1
10^2
10^3
Rate [s-1]
Roldan/Saraf

Fig 5

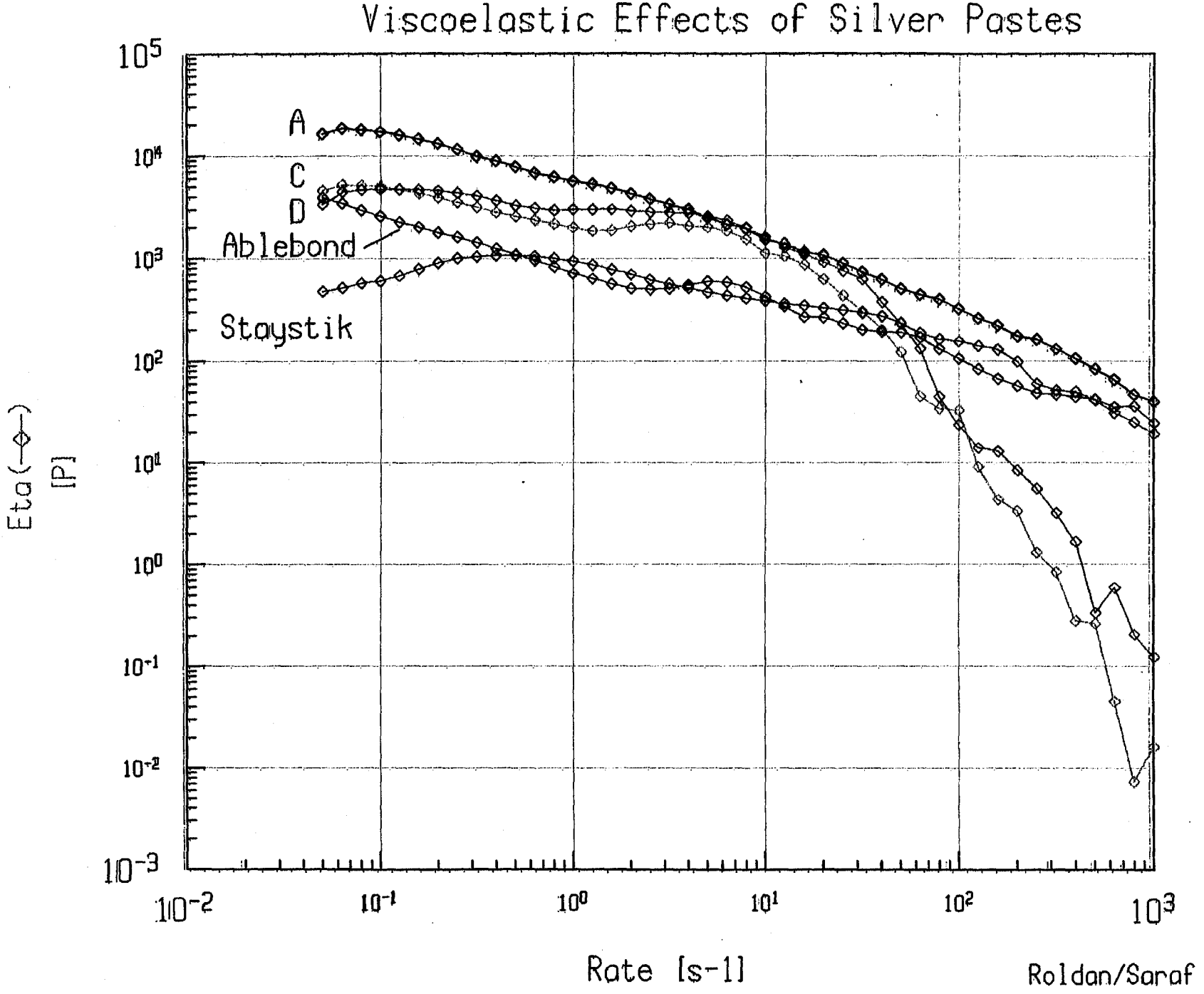
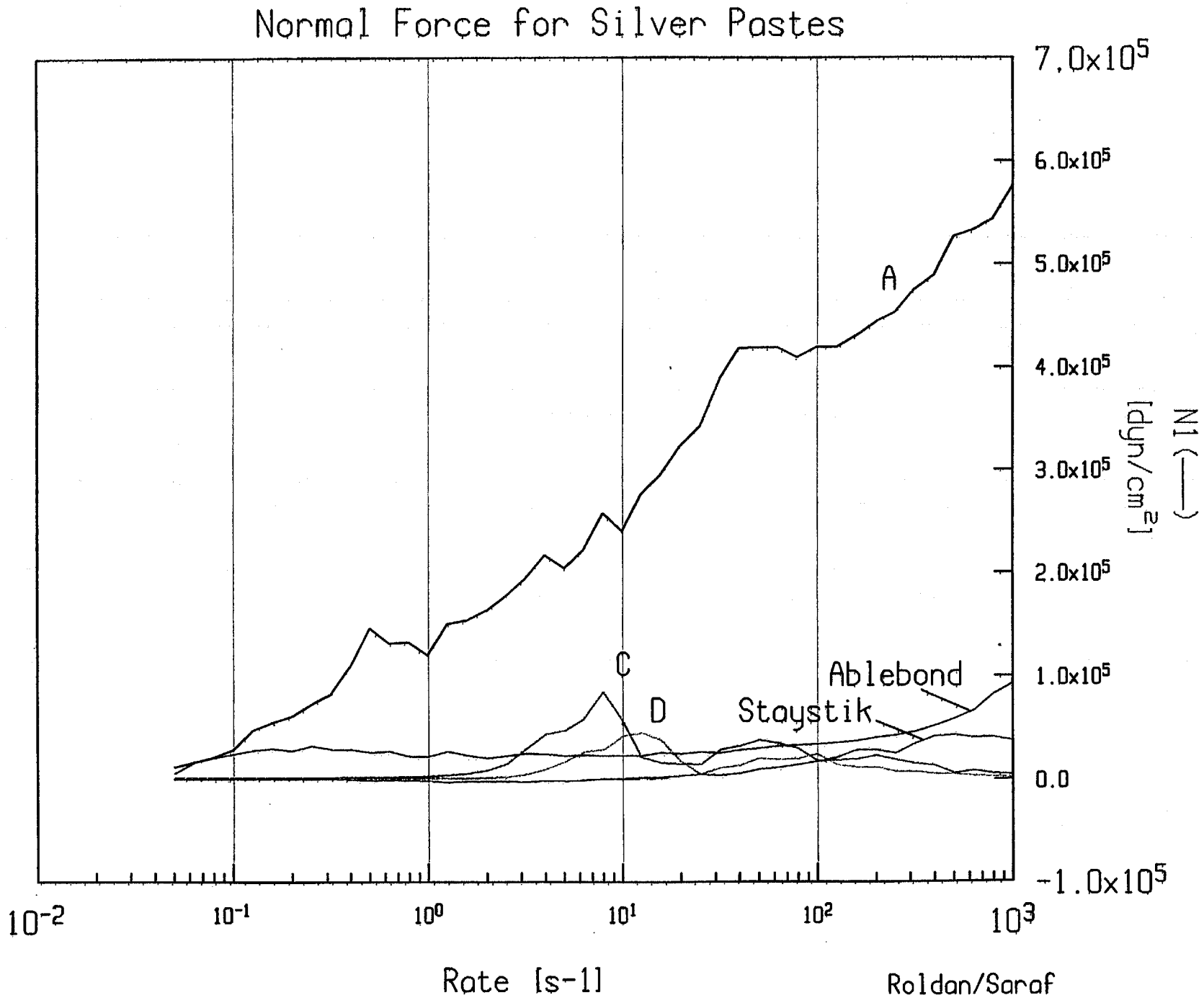

Viscoelastic Effects of Silver Pastes
A
C
D
Ablebond
Staystik
Eta(—◇—)
[P]
Rate [s-1]
Roldan/Saraf

FIG 6(a)


Normal Force for Silver Pastes
7.0x10^5
6.0x10^5
5.0x10^5
4.0x10^5
3.0x10^5
2.0x10^5
1.0x10^5
0.0
-1.0x10^5
N1 (——) [dyn/cm^2]
A
C
D
Ablebond
Staystik
10^-2
10^-1
10^0
10^1
10^2
10^3
Rate [s-1]
Roldan/Saraf

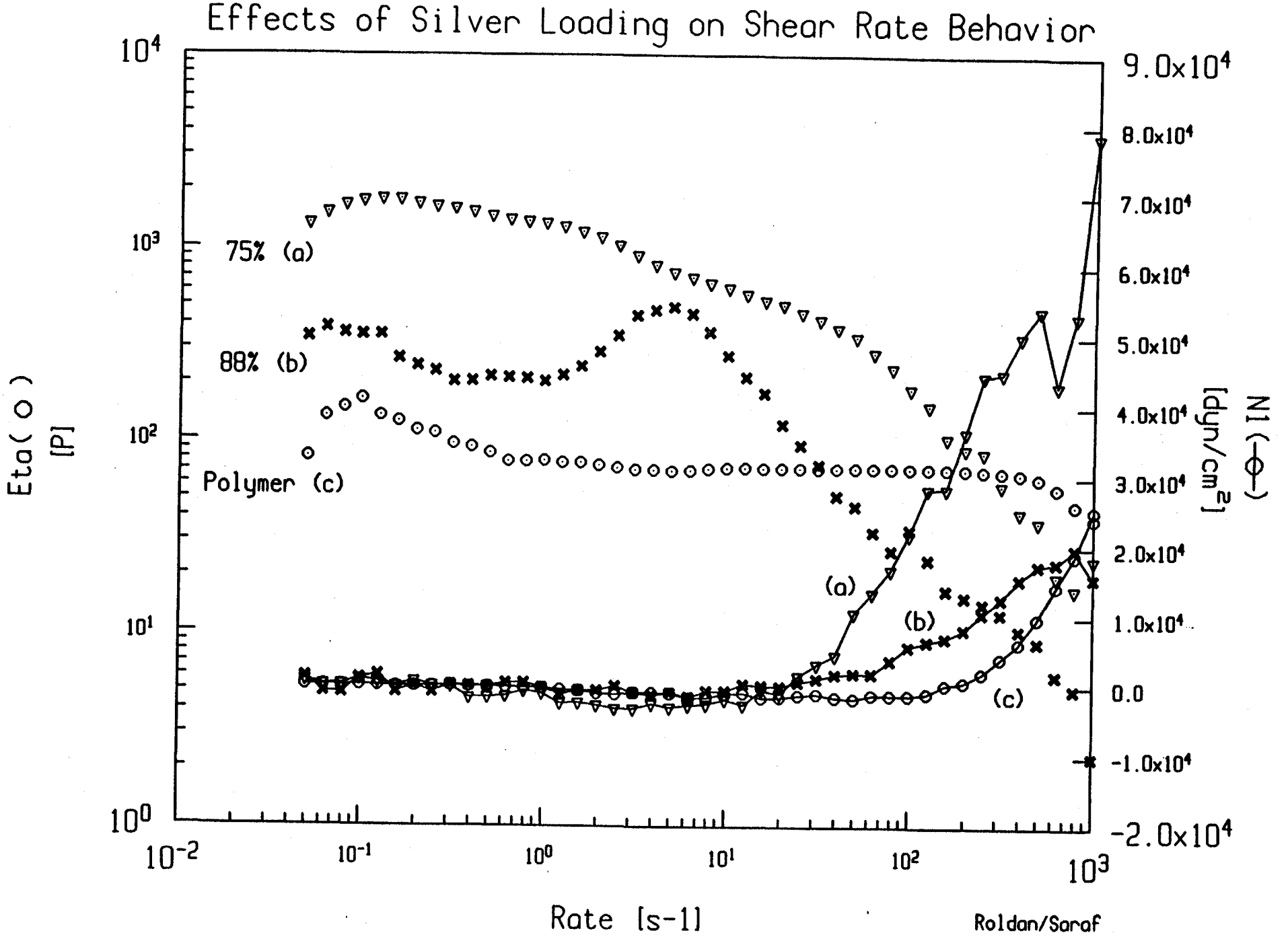
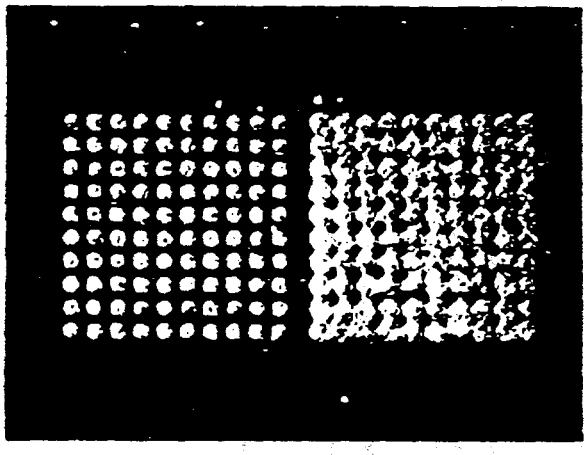
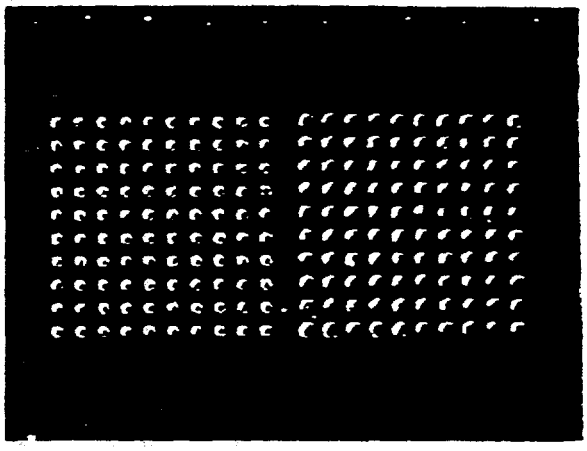

Effects of Silver Loading on Shear Rate Behavior
Eta(O) [P]
N1 (-O-) [dyn/cm2]
Rate [s-1]
75% (a)
88% (b)
Polymer (c)
(a)
(b)
(c)
Roldan/Saraf

FIG 7

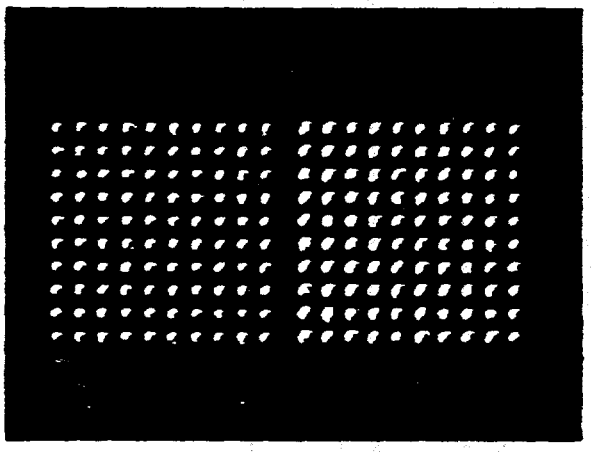
cm2

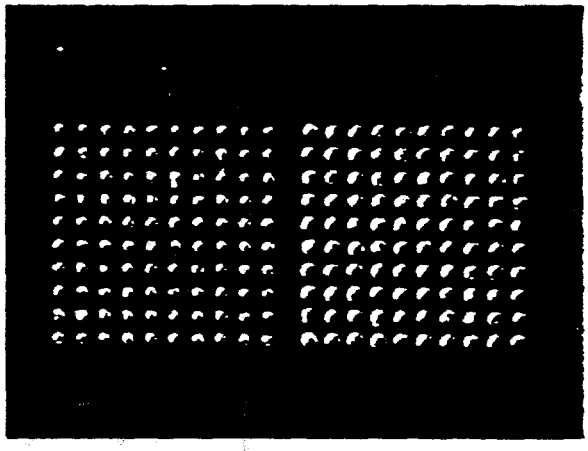




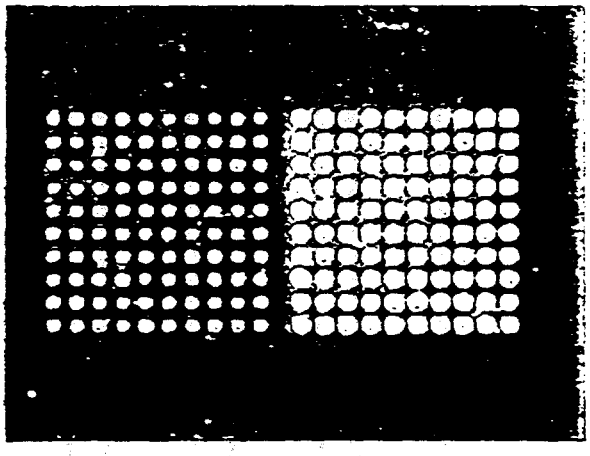
Ykt. 1

Ykt. 2





Ykt. 3



cm1

FIG. -8

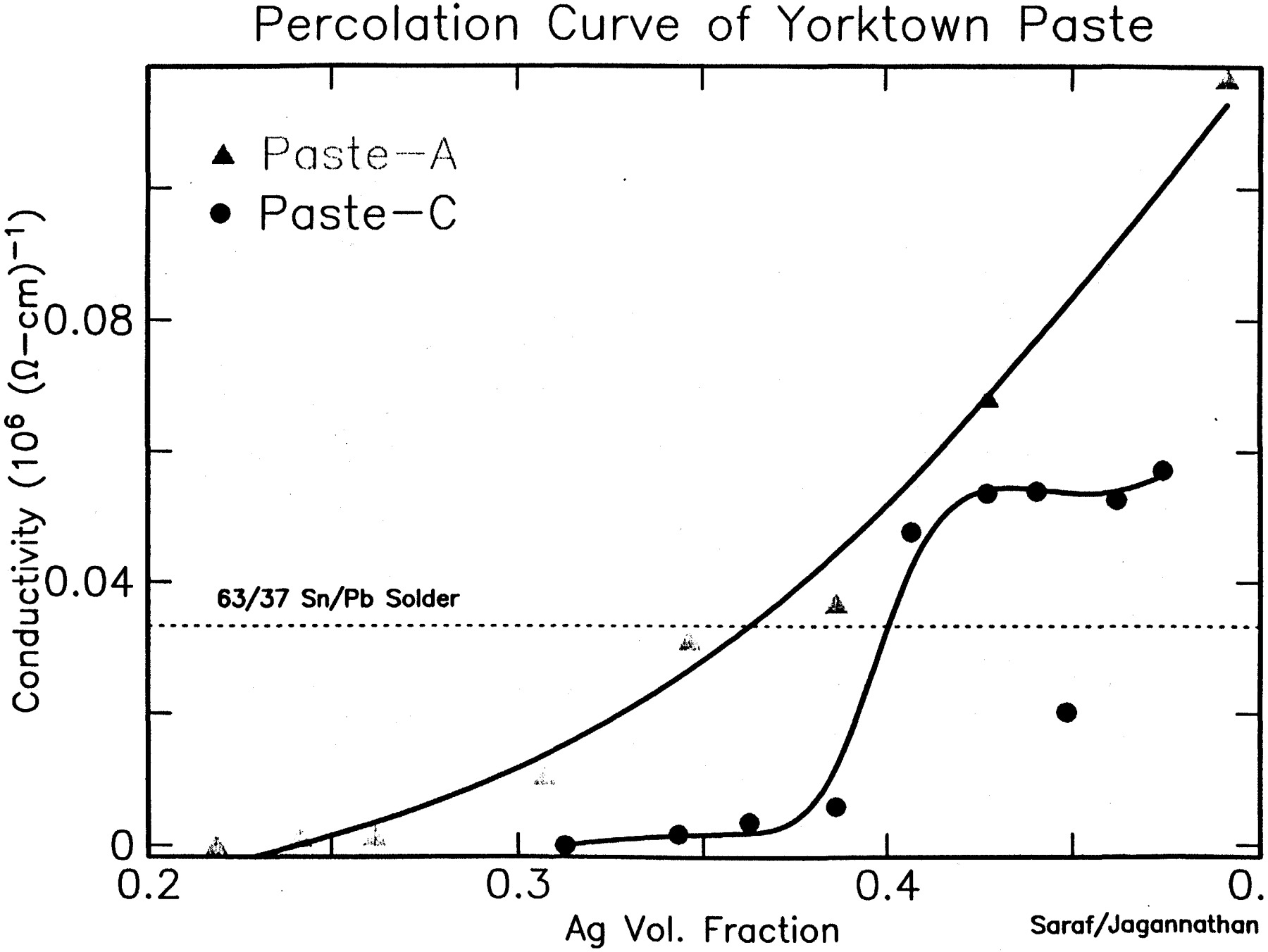


FIG 9

Four-Point Probe Measurement

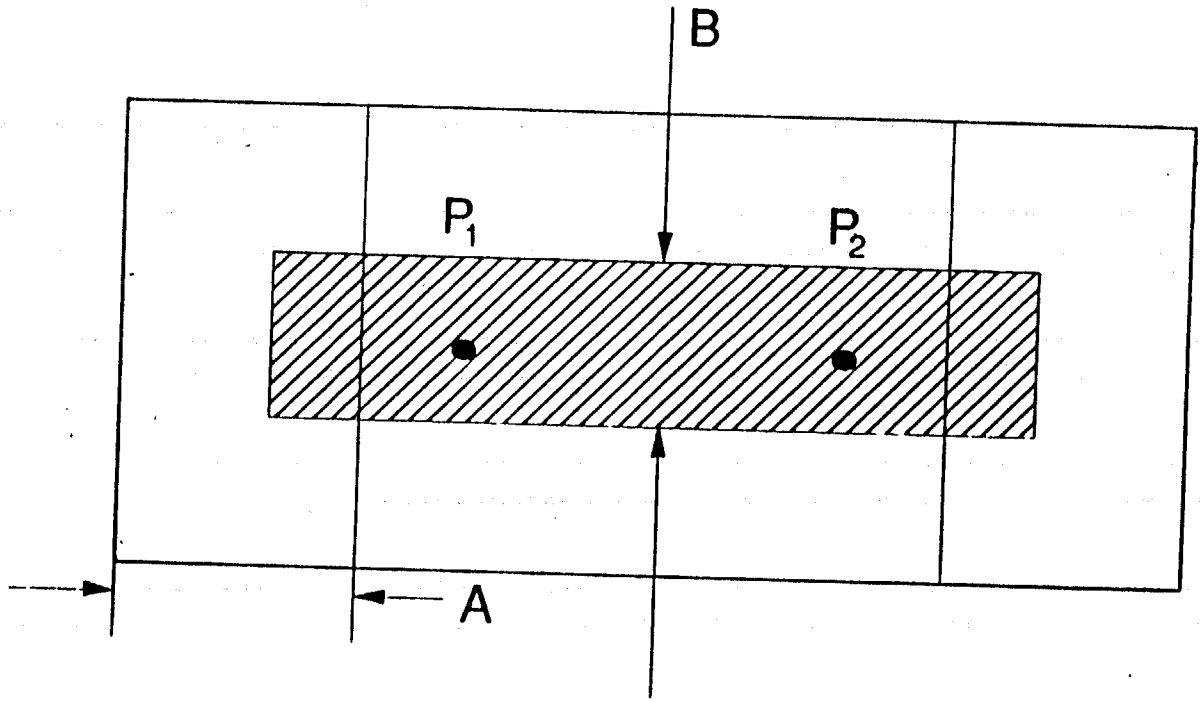


Fig. 10

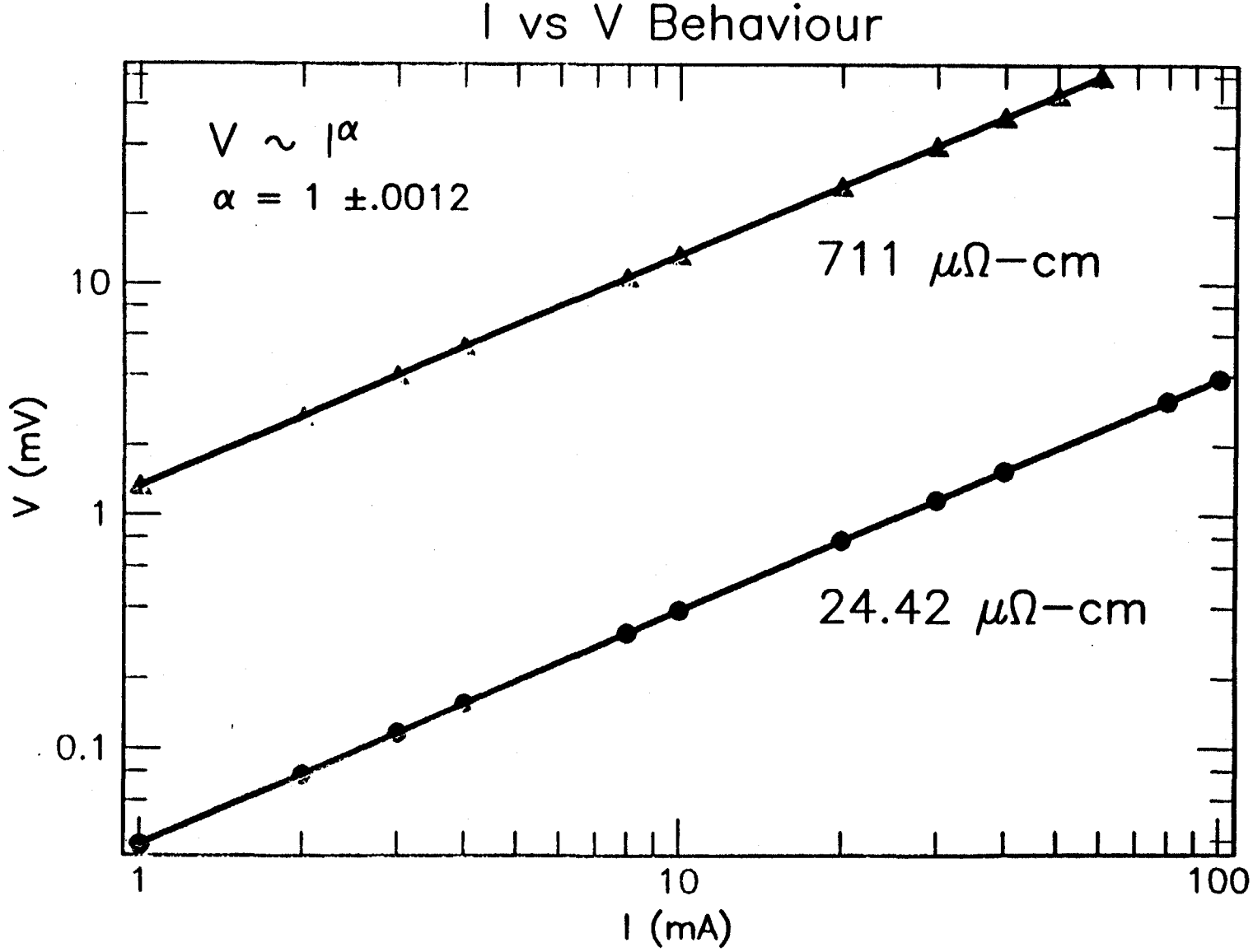


Fig. 11

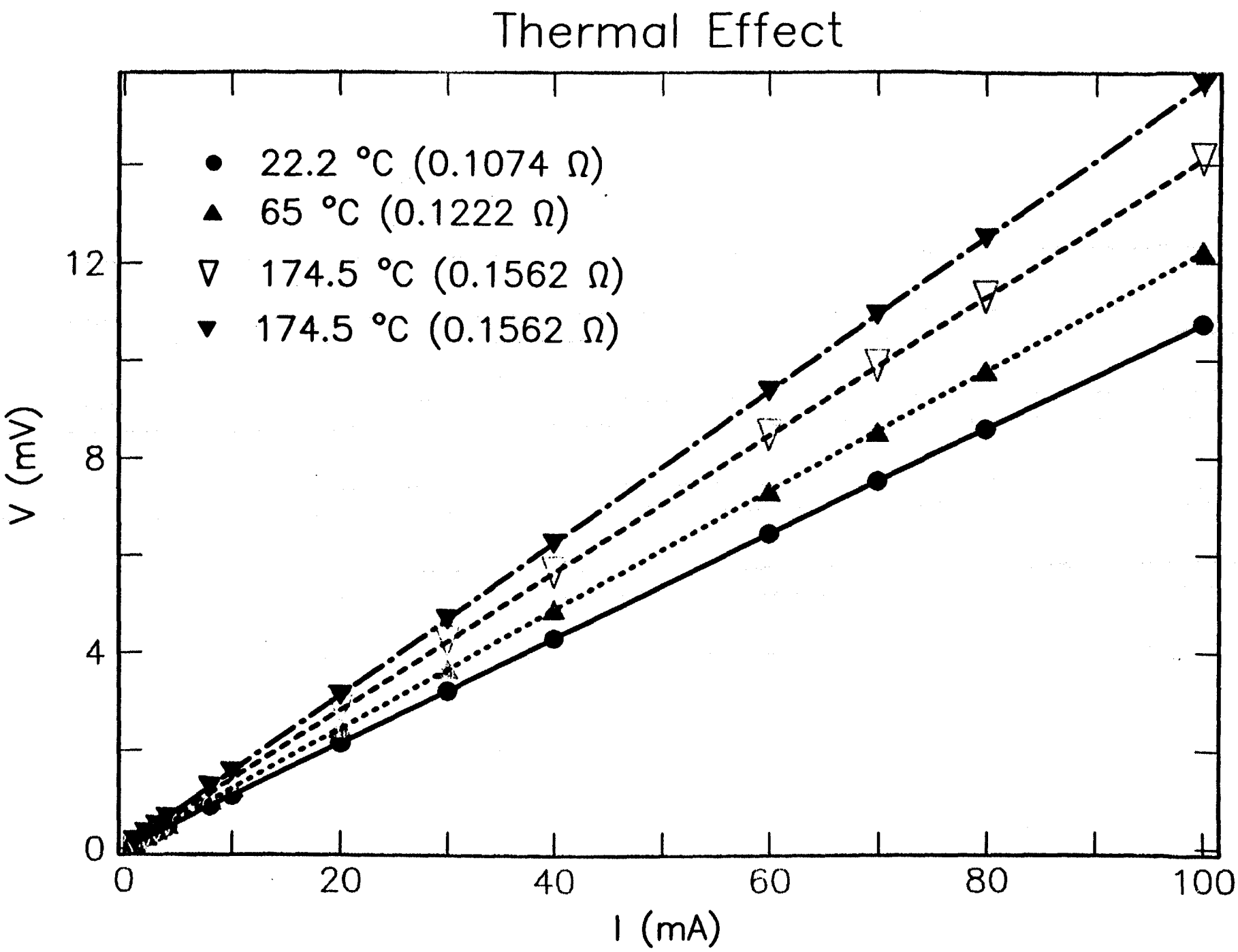


FIG. 12

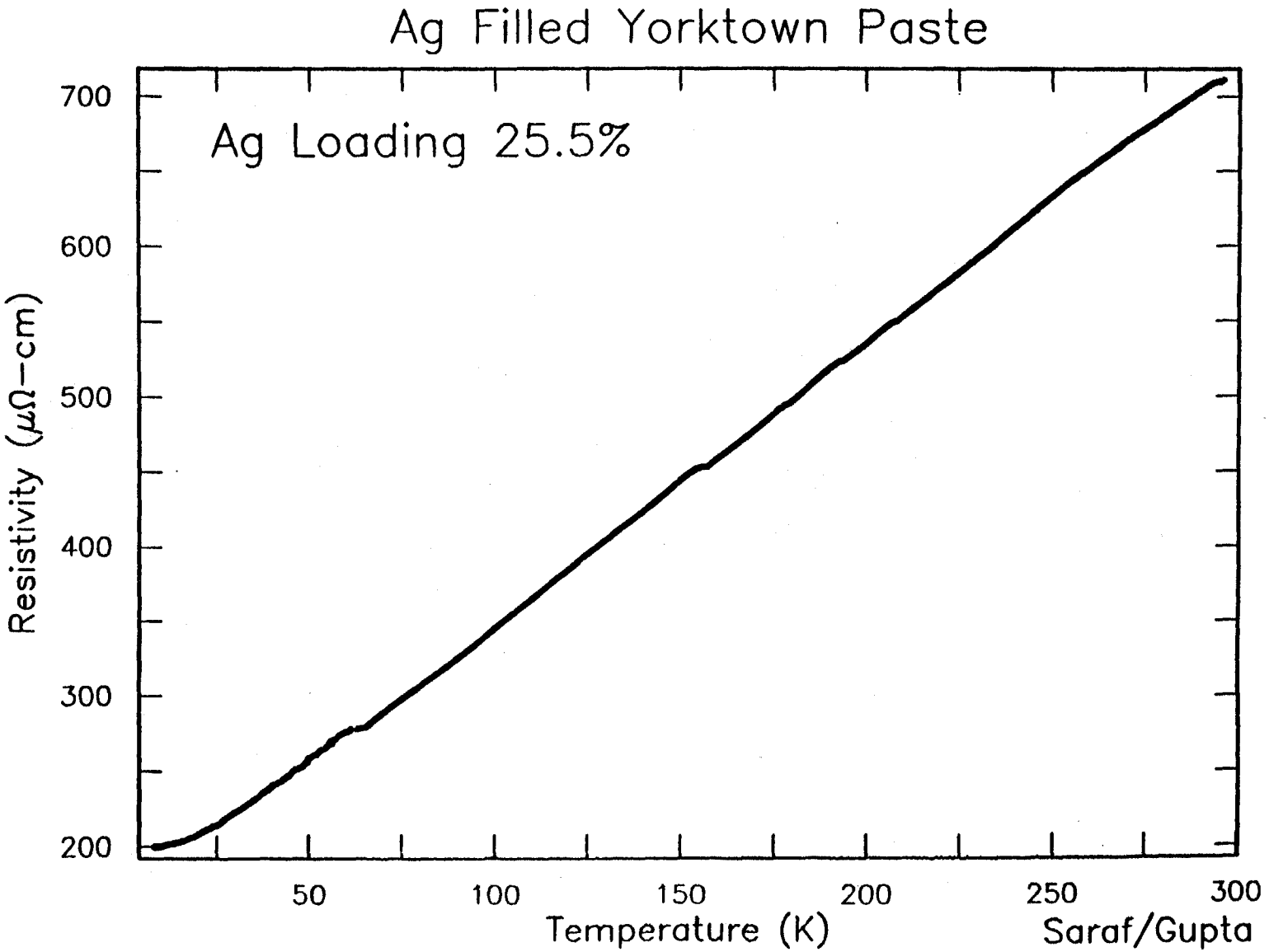


FIG. 13

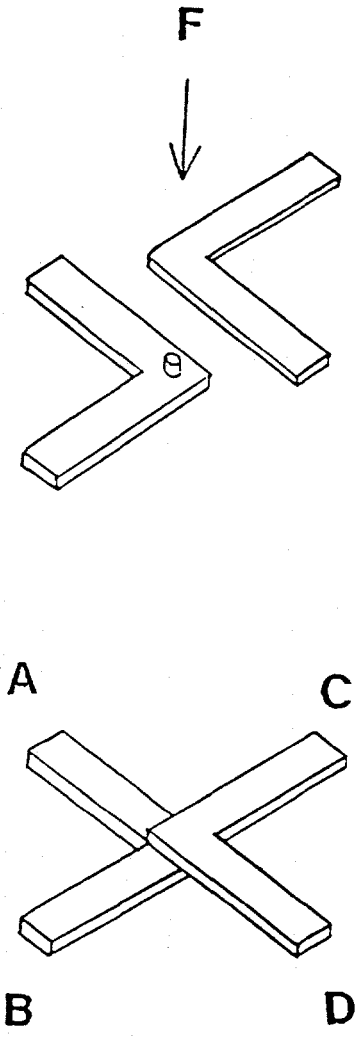


Fig. 14

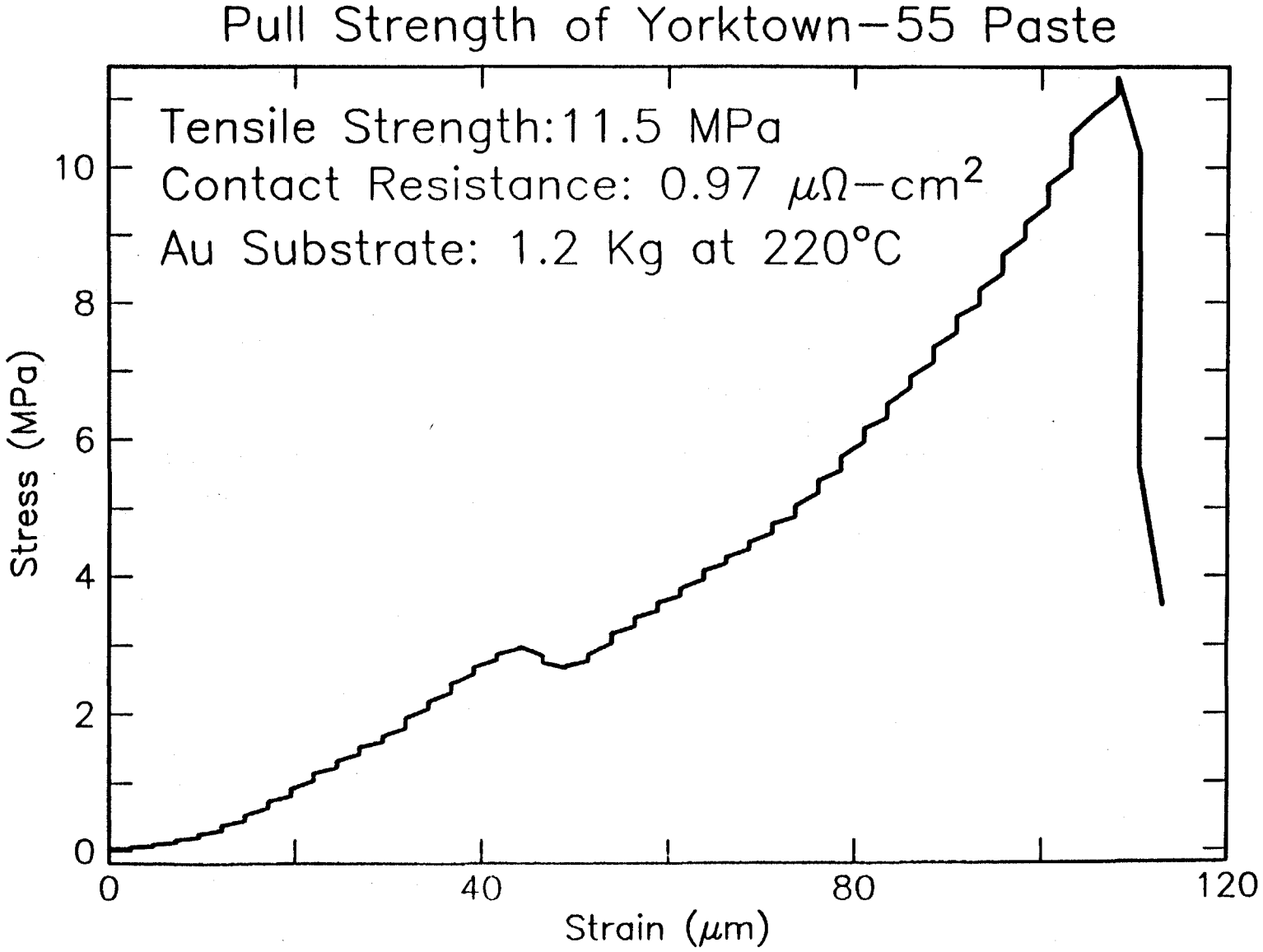
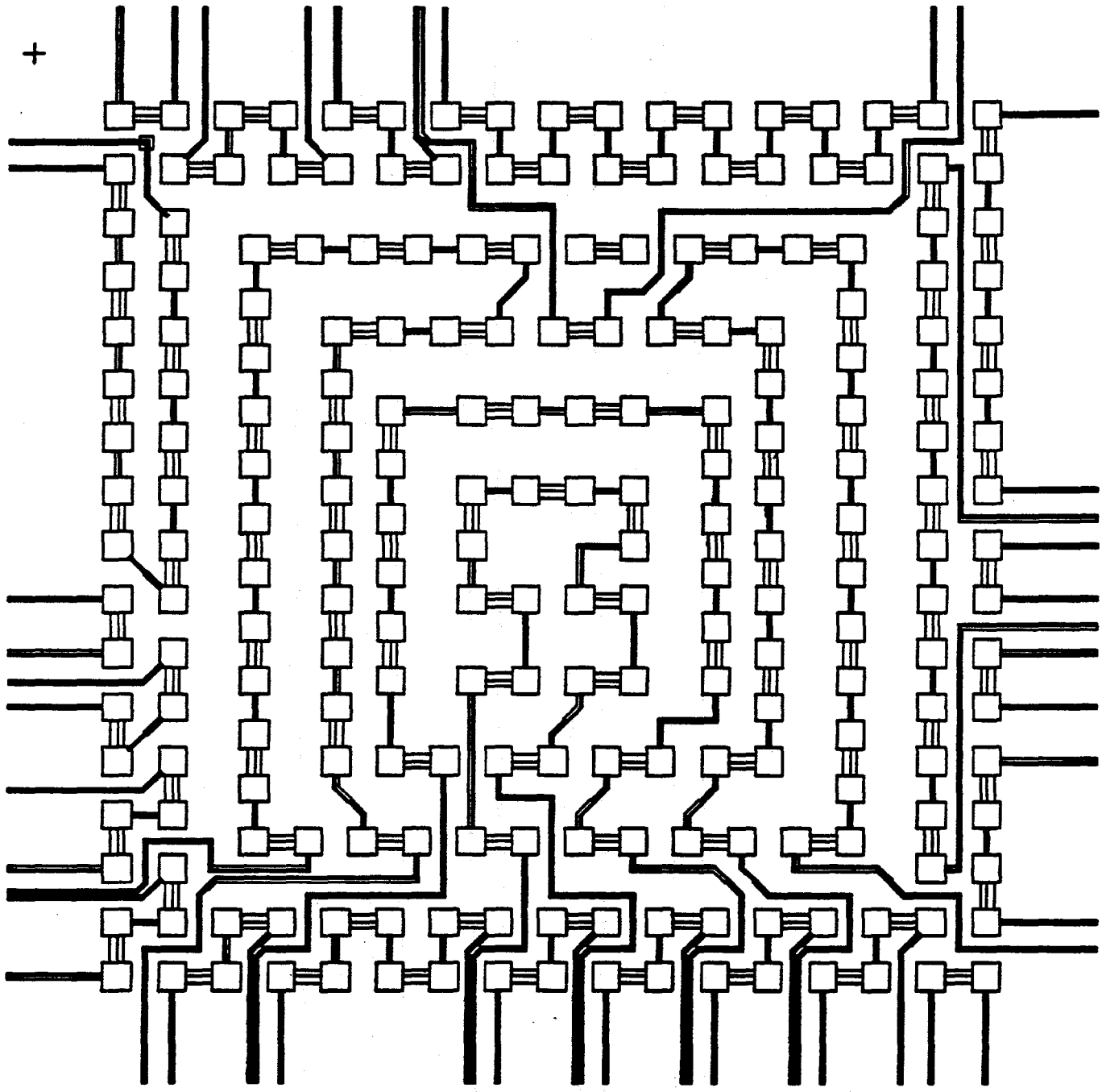


FIG. 15



FIG

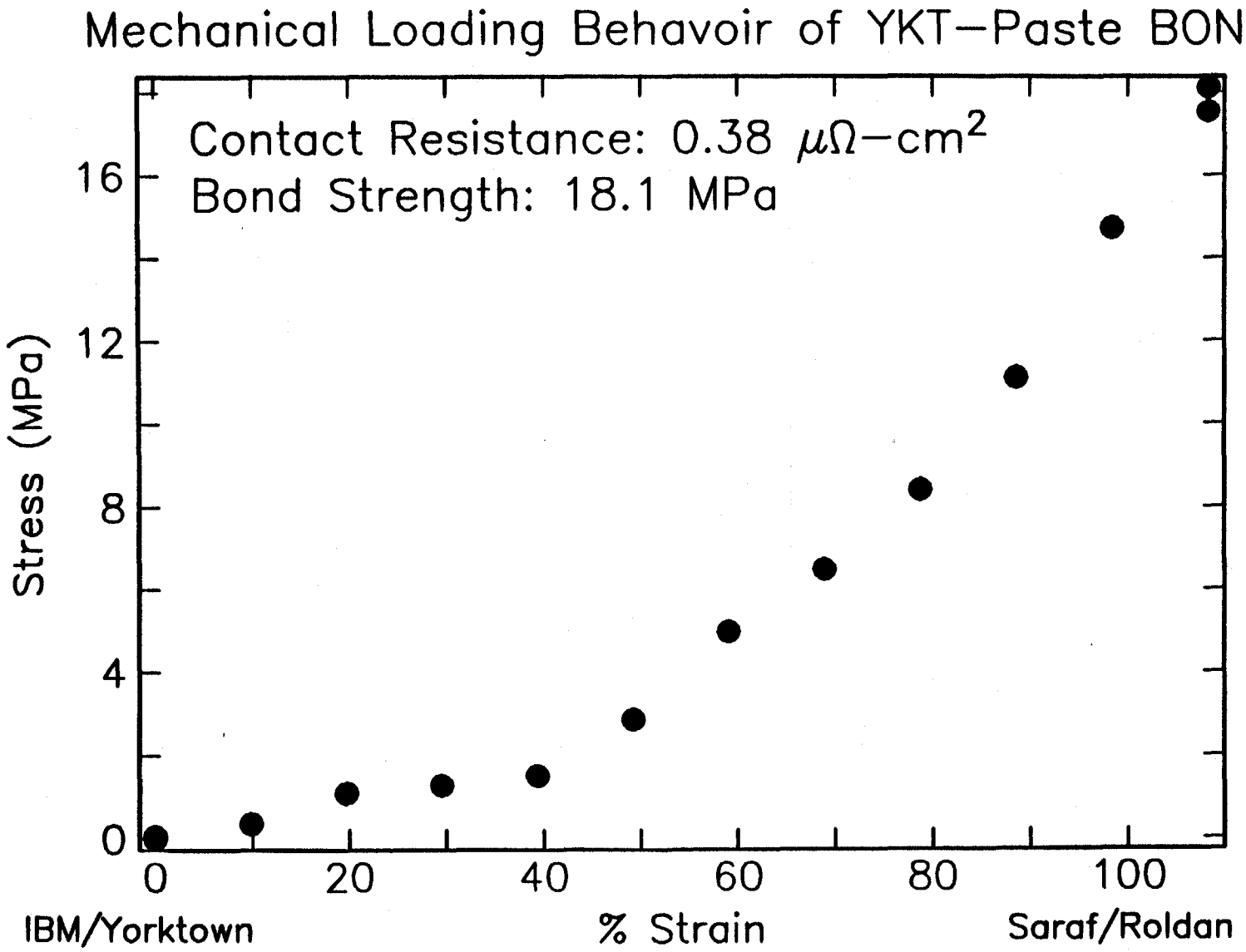
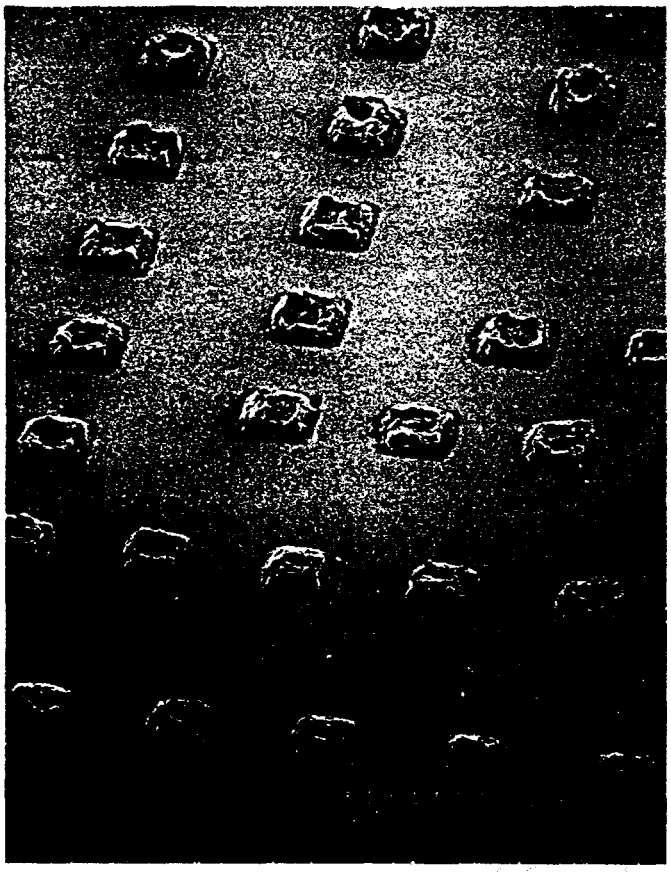
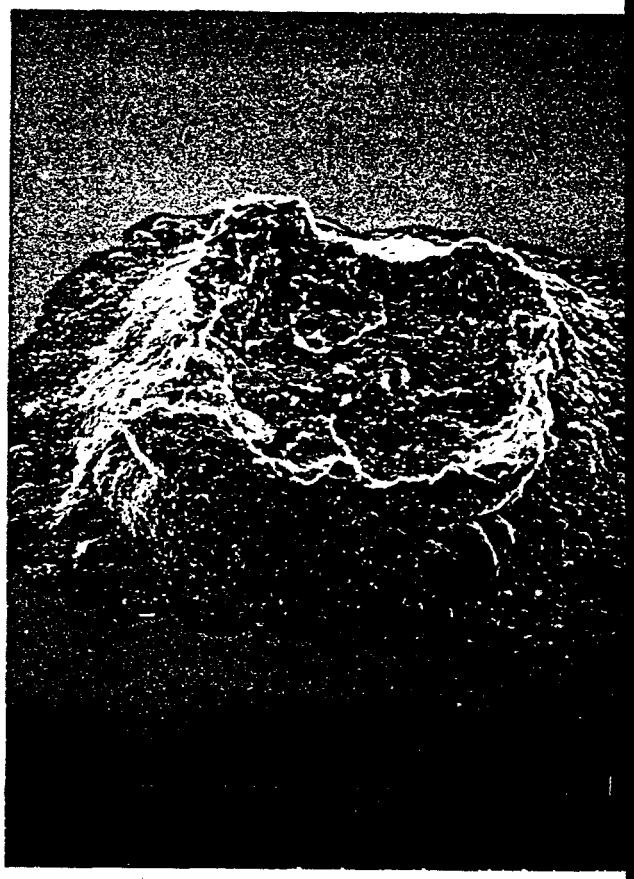


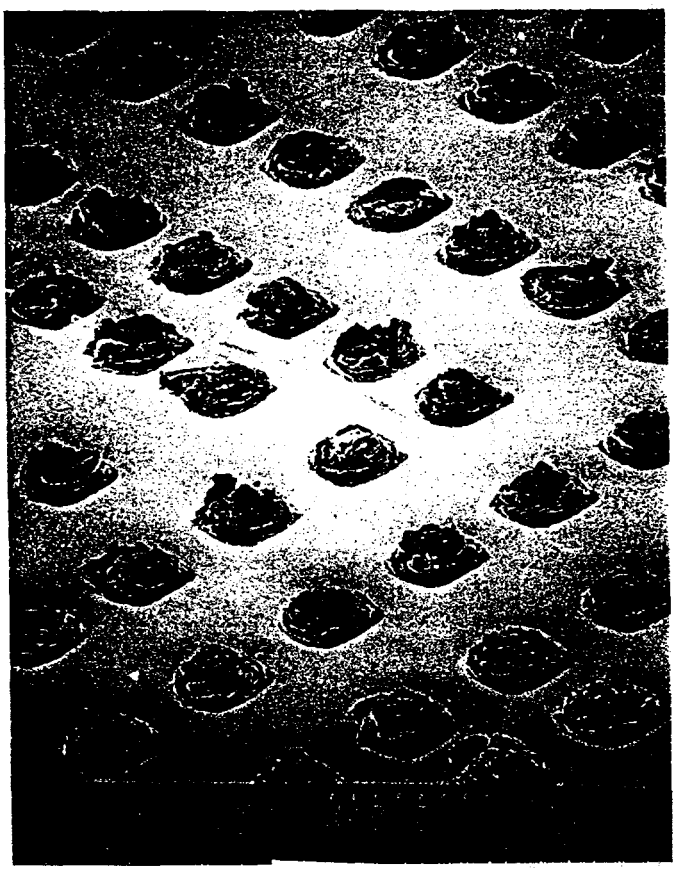
FIG 17



Chip side



Chip side



wafer side

wafer side

FIG 1

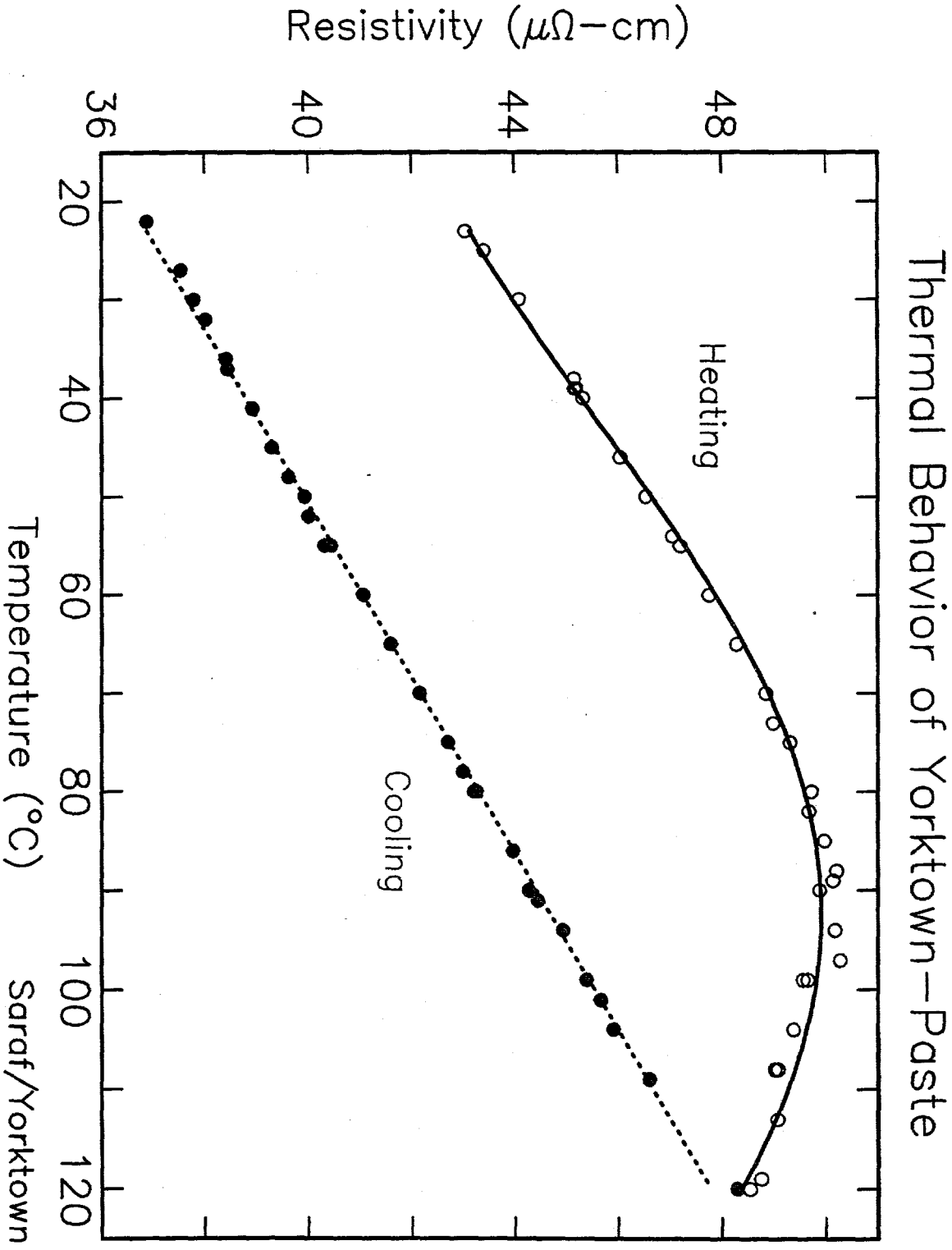
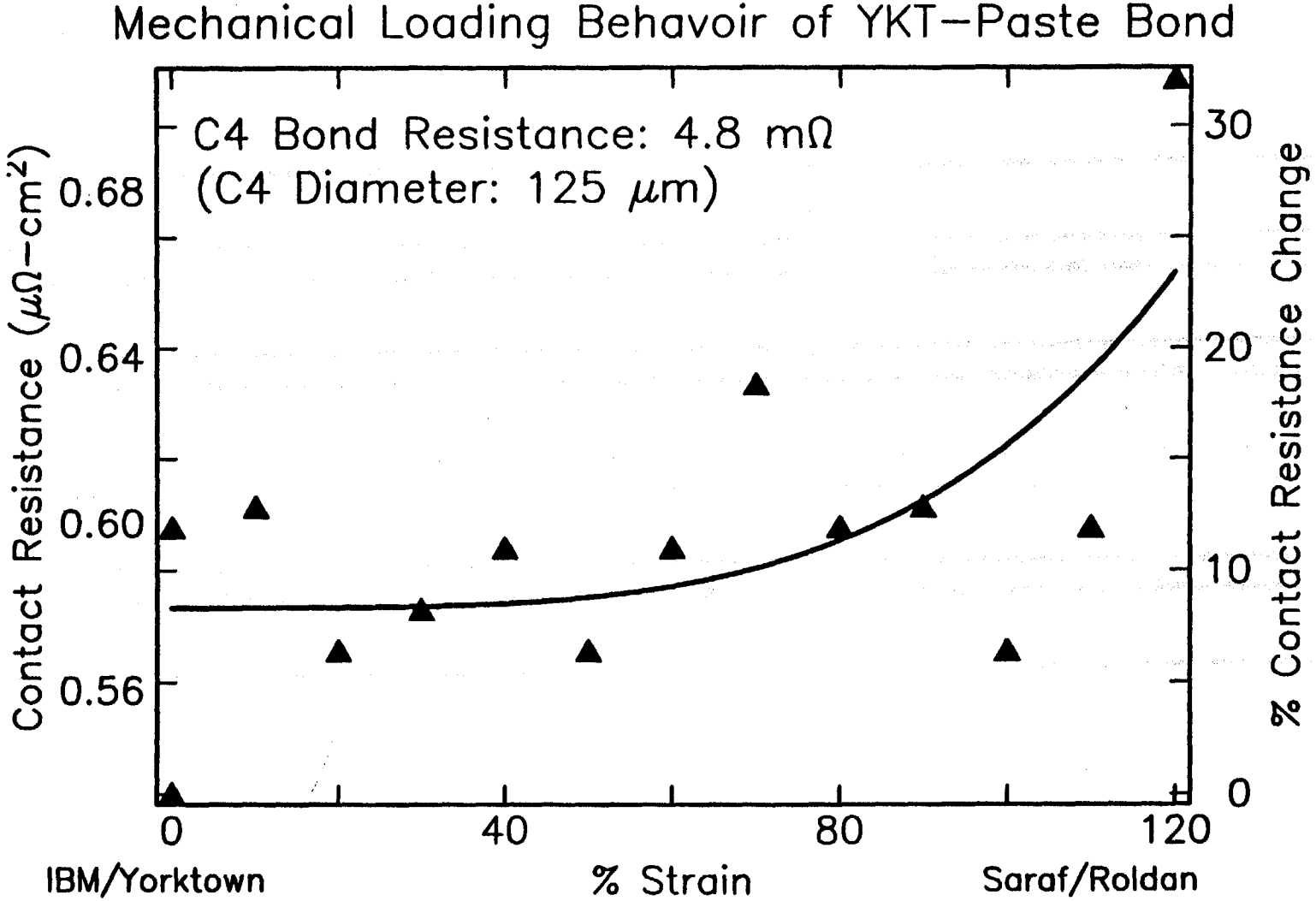


FIG 19

-ps HC55A (GSIZE 6.0 8.0 ROTATE 90 FILL COLOR REPLACE BOTOPTION



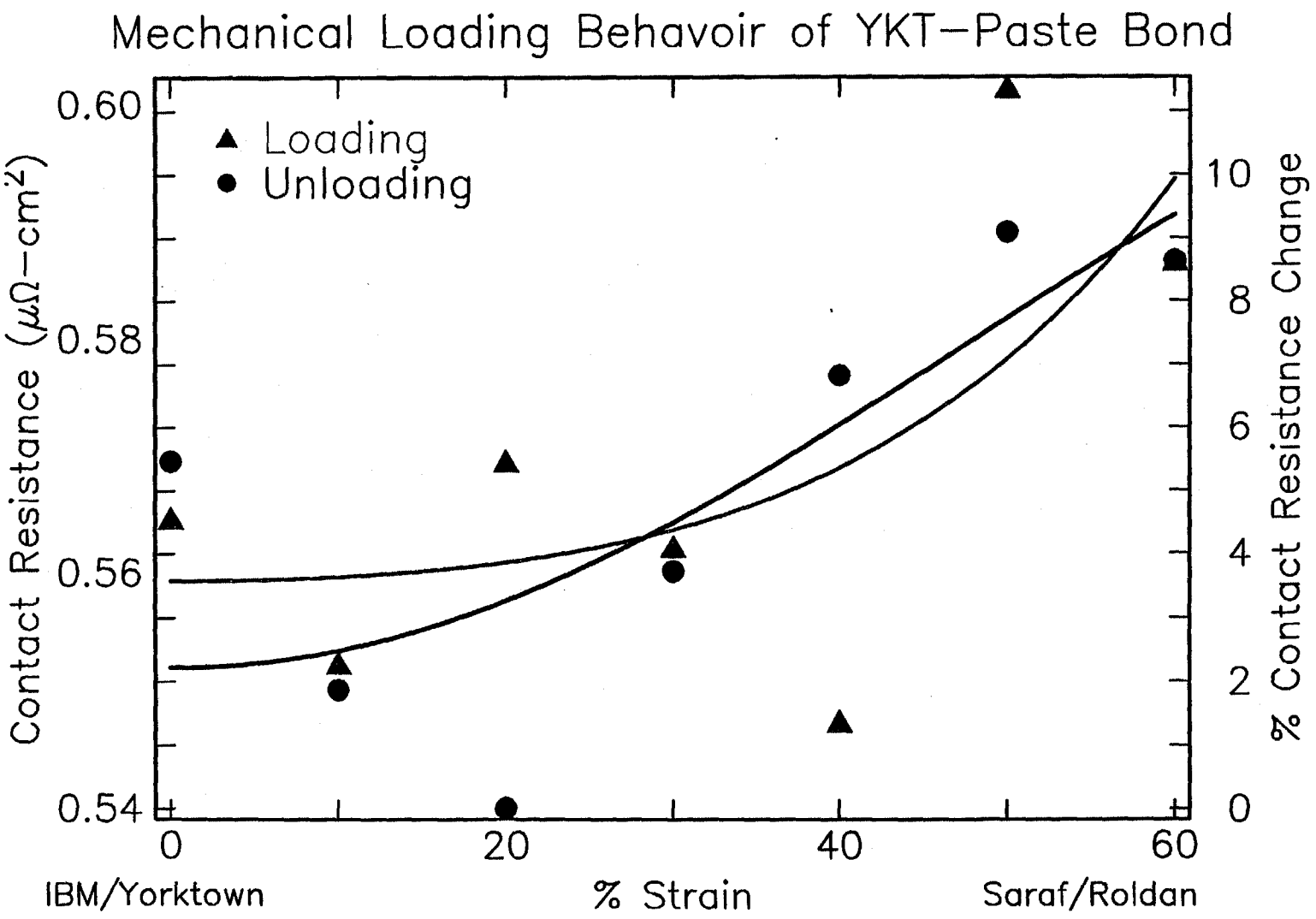


FIG 21

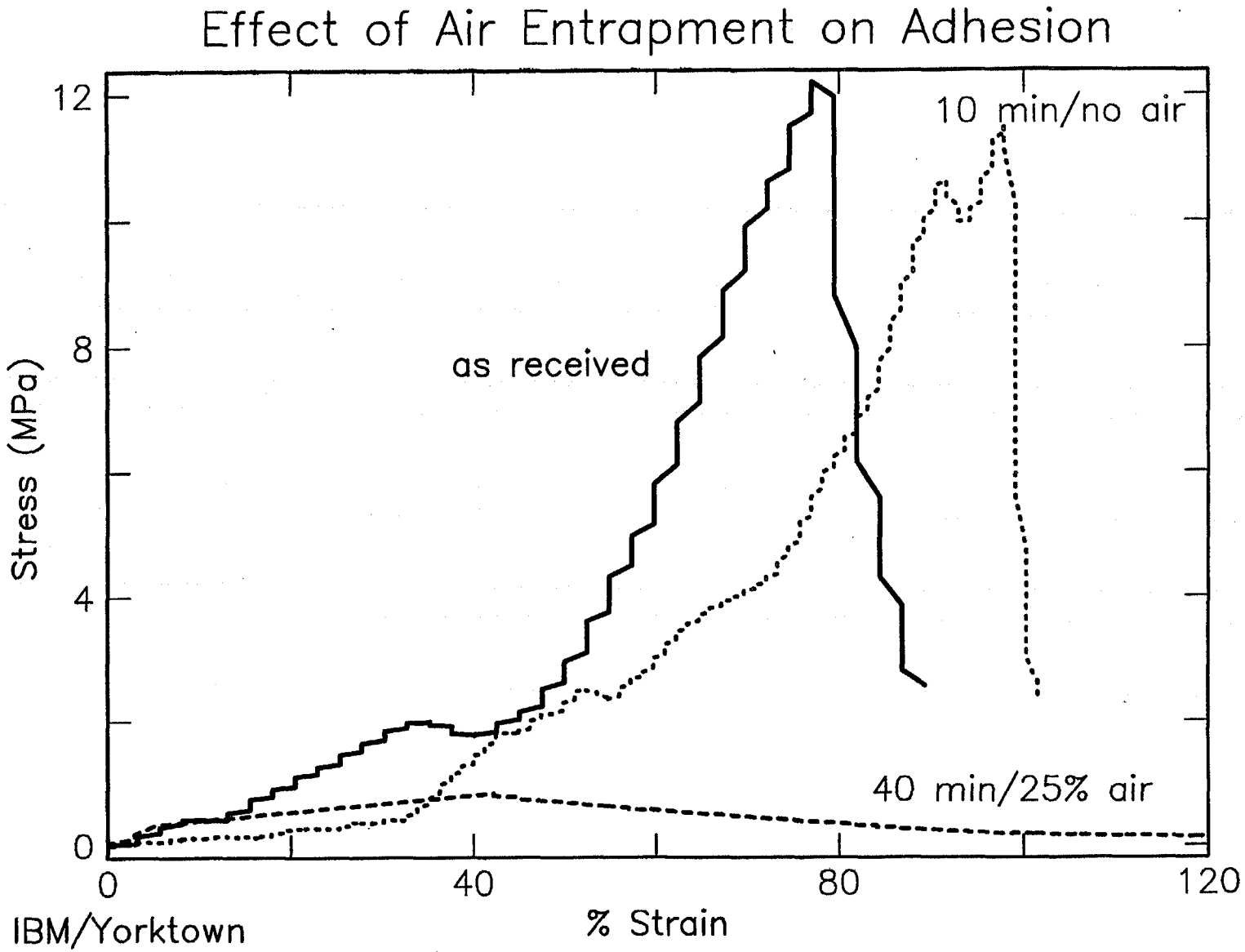
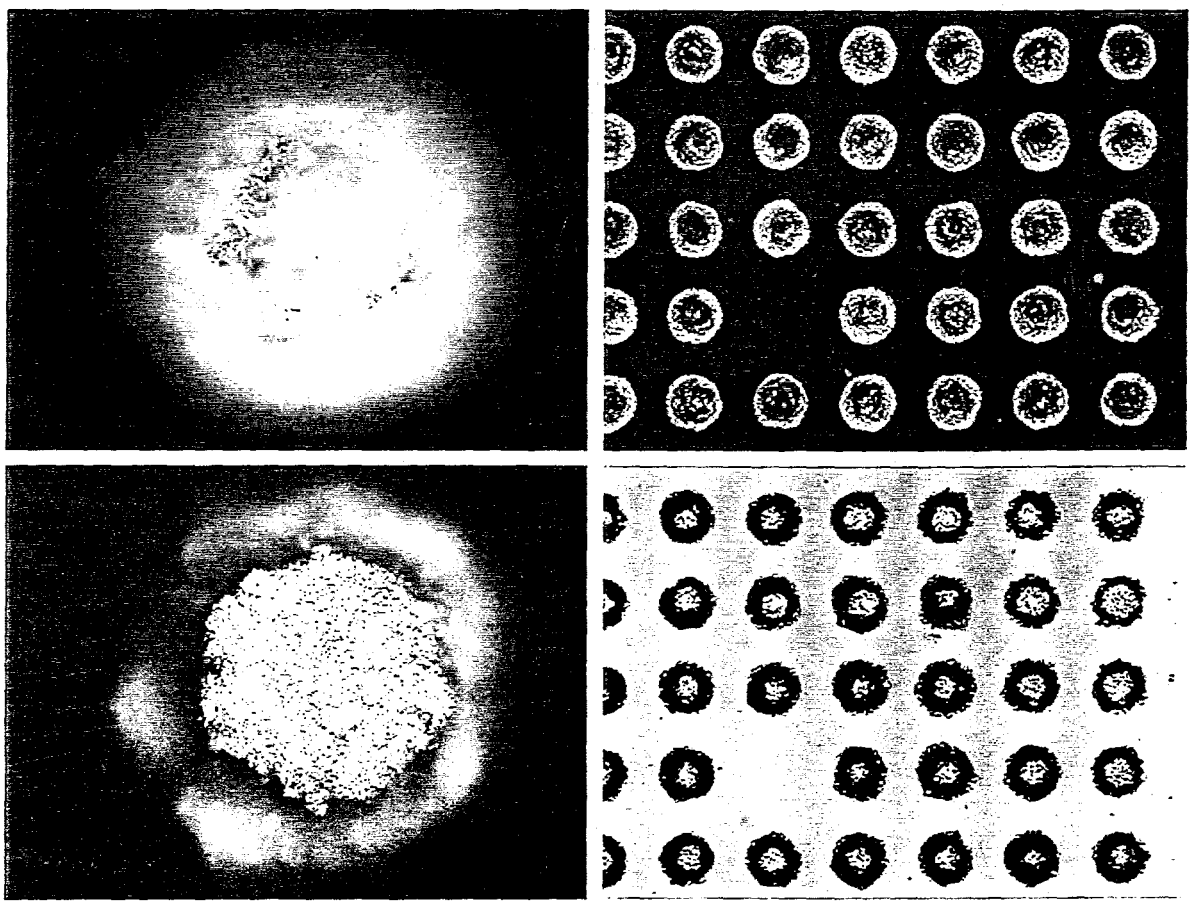


FIG 22



(b) (a) (d) (c)

FIG 23

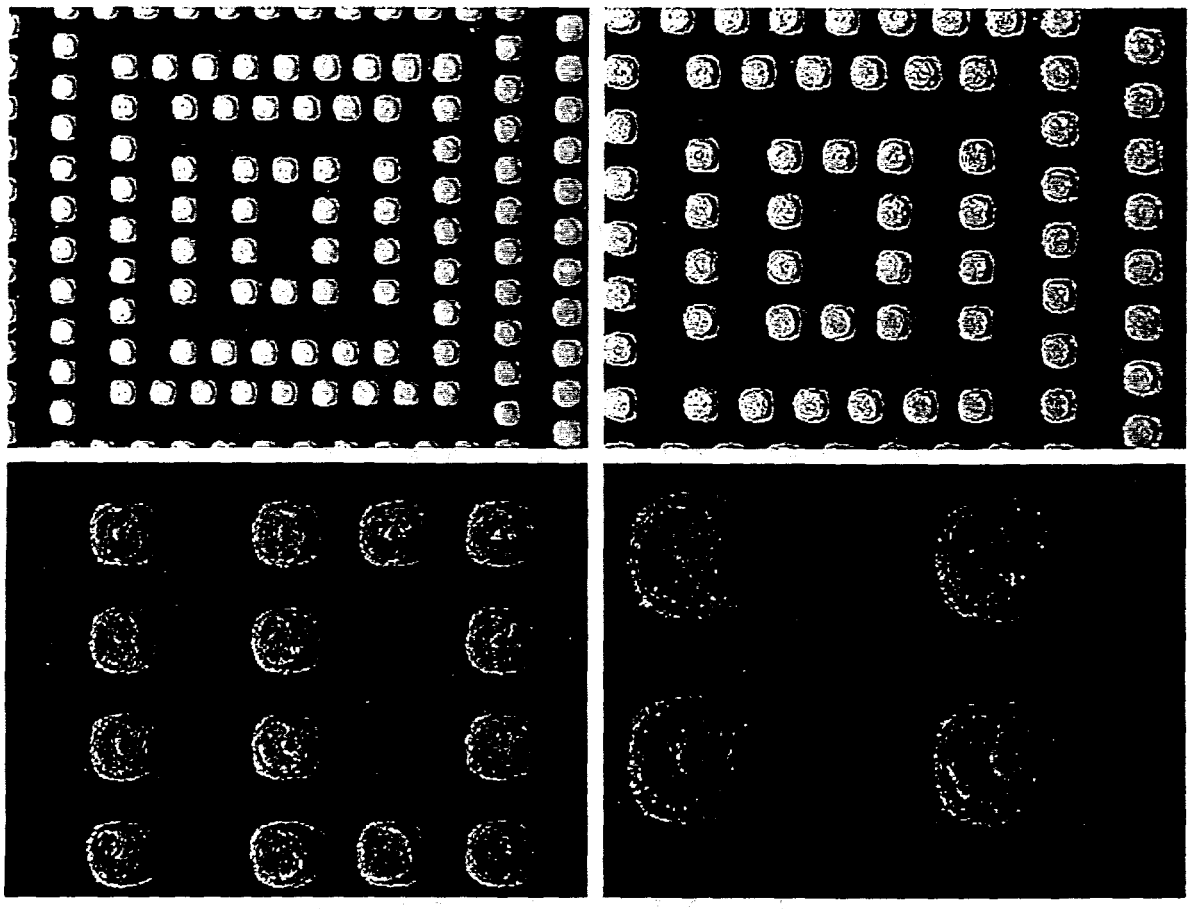


FIG 2

Executive Summary

IBM ENDICOTT, FINAL ANNUAL REPORT

IBM Endicott, Assembly Process Design has completed the development activity on **DARPA TRP No. DE-FC-04094AL98817 for High Performance, Low Cost Interconnections for Flip Chip Attach.** The scope of Endicott activity for this three year project includes

Paste Deposition Process Development
Chip Bonding Process Development
Encapsulation Material Recommendation
PMC Interconnection Stability in Stress Testing

Paste Deposition Process Development

Objective: PMSP (Polymer Metal Solvent Paste) material must be deposited on a five inch wafer with a goal of 100% bump survival at a chip level. The target geometry is 0.010" diameter, and 0.004" high with a flat surface.

Accomplishments:
A process called "photobumping" has been invented and developed to deposit PMSP onto the chip pads of a wafer. This process uses a special dispense head that was invented and designed for PMSP. The head contains the PMSP and prevents it from drying out. Through a thin slit, defined by flexible parallel blades, a piston extrudes PMSP. The wafer is prepared with photoresist by laminating successive layers of 0.003" and 0.001" thickness. The 0.004" thick photoresist is imaged to create apertures, exposing bond pads on the wafer. Next, the dispense head is traversed over the wafer and the apertures are filled with PMSP in two passes with a solvent drying process that occurs between the first and the second pass. A semiaqueous photoresist is used because it is more solvent resistant than aqueous photoresists. Flat surface bumps, nearly 0.004" high bumps, 0.008" diameter on 0.020" pitch can be defined with a 90% yield on five inch wafers. Photobumping process windows have been defined and include high feed pressure and slow screening speed. A screen head modification that used metal stiffeners to support the compliant metal blades through which paste is extruded allowed higher feed pressure. Small void formation at the base of the deposits was reduced. An additional modification was made to the head that allowed a vacuum draw in the aperture just prior to paste injection. A small reduction in void size resulted. No failure is attributed to these voids during stress testing.

Chip Bonding Process Development

Objective : The objective of the bonding process development effort was to identify the significant process variables that influence bond strength and fracture. Stress test were used to verify electrical and mechanical integrity. Design-of-Experiment process optimization was used to identify the fastest bond cycle that can be used to produce reliable joints.

Accomplishments: Chip bonding process development has focused on defining a process window and identifying an optimal process point. Repeatable tensile bond strengths between 1400 to 2000 psi can be achieved. Fracture mode typically occurs near an interface. Bonding temperature, pressure, and pressure on cool-down (to 120°C) were identified as key process variables. The optimum bonding process point is applying 135 psi to the chip, while heating to 235 C. Pressure is maintained for 30 seconds at temperature and until cooled to 70 C. These optimum bond parameters resulted in PMC bondlines of 0.0025"±0.0002" . Encapsulation processing was comparable to soldered flip chips. Stable contact resistances have been measured in stress testing of encapsulated PMC joints. Shelf life in excess of 6 months was identified for photobumped chips. Preliminary rework process and feasibility has been established. Reworked chips (2) exhibited stable and a reliable electrical performance through stress test (-55 to 125°C).

Encapsulation Material Recommendation

Objective: The objective of the flip chip encapsulation activity was to evaluate and recommend a material that is commercially available that would be compatible with PMC flip chip interconnection to organic carriers.

Accomplishments: Strong adhesion of PMC bumps to pads on the card is required to prevent encapsulant wicking and damage to the PMC interconnects. PMSP C provides the most robust interconnect during the underfill process because of its superior adhesion. However, underfilling has been found to increase the joint resistance during the initial stage of cure two to five milliohms for blanket wafers and 12-30 milliohms for stitched wafers. Stable contact resistance has been observed throughout the subsequent stress tests. Experiments conducted to study the correlation between viscosity and contact resistance show that the contact resistance increase is minimized for the higher viscosity underfills both at ambient temperature and during cure. Matsushita CV5183S (MAT) and Dexter 4511 (4511) encapsulants are used to achieve good reliability performance of PMC joints, with MAT being more effective. Encapsulation flow times less than two minutes, with no voids were achieved at bondline of 0.0025"±0.0002". Rapid cure at 150°C, higher viscosity, and shorter gel time (4 minutes) of encapsulant resulted in the minimum increase in contact resistance of assembled chips. Dispense at 80°C and 1 hour cure at 150°C are identified as optimum process conditions for PMC encapsulation (with MAT and 4511)

PMC Interconnection Stability in Stress Testing

Objective: The first objective in achieving PMC interconnection stability was to select a terminal metallization to be used at both the chip and card level. The approach was to evaluate the initial contact resistance distribution independent of electronic packaging variables such as coefficient of thermal expansion differences or warpage. Contact resistance stability was studied as a function of environmental aging. The second objective was to demonstrate that the PMC joints between a chip and card laminate can maintain stable contact resistance as a function of exposure to environmental stress. These stresses include accelerated thermal cycle (ATC), thermal age and temperature and humidity (T/H)

Accomplishments: Four metal finishes were evaluated for initial contact resistance and contact resistance stability and found to be all acceptable: soft gold, hard gold, palladium nickel alloy and palladium. After stress for 1000 hours at 125 C and 85 C/80% RH, contact resistance changes were less than one milliohm. Soft gold was selected as the preferred surface finish because of its general availability in industry. Palladium and palladium nickel as evaporated, were highly stressed and thus prone to delamination from the chip surface.

A total of 10 separate stress tests were completed on chips with PMC bumps that were bonded to a laminate test card. Four types of PMSP (A, B, C and D) were used. PMSP C was selected as the preferred paste because of its higher bond strength and predominantly cohesive fracture mode. The results of the stress tests demonstrate the feasibility of PMC interconnection between chips and laminates. Chips with blanket gold had PMC joints that performed similar to solder interconnects during stress. Chips with stitch patterns showed a general increase in contact resistance in the range of 20 to 40 milliohms. It is hypothesized that this resistance increase is caused by an incompatibility between the photobumping stripper solution and polyimide passivation. Artifacts of the interaction are deposited on the PMC bumps and compromise the interface between PMC and card bond pads. Quartz passivation may be a way to eliminate the contact resistance drift for the stitched chips.

PMSP DEPOSITION DEVELOPMENT FINAL REPORT

OBJECTIVE:

The objective of paste deposition was to repeatedly create a multiplicity of miniature features of PMSP (Polymer Metal Solvent Paste) material on a chip to replace solder. The final features are 0.004" high, 0.008" diameter on 0.020" centers.

HISTORY

The deposition process created several severe physical challenges that had to be understood to move the process forward. A special dispense head was developed. The stencil material had to be compatible with the PMSP material. An invention was needed to create a nonphysical removal of the stencil to protect the PMSP bumps from damage or removal after deposition. The dispense process must be robust enough to form thousands of miniature features consistently and repeatedly .

THE DISPENSE HEAD was designed and developed especially for this PMSP material and process. It was determined that the PMSP material dried quickly and any unnecessary exposure to air would change the viscosity of the material. It would then change the yield of void less bumps as a function of time exposed to air. Since the PMSP material is high in viscosity, it was felt that the PMSP material needed to be pressurized to force it into the tiny cavities. The blades that held the material needed to be stiff enough to contain the pressure being applied to the material, compliant to adjust slightly to the topography of the surface of the stencil, and stiff enough to create a seal on the surface of the stencil where the material is pressurized.

To prove or disprove an idea, several changes were made to the head. **Figure 1** shows an end section view of the head. The pressurized PMSP is forced out between (2) the inner blades (3). The extra outer blades (5) that were added to keep the blades from flexing as the dispense pressure was increased. The end slider bars (6) were modified from spring retention to a solid retainer with air bearings for reduced friction. This modification was also necessary to deal with the higher pressure. The final modification was to add another pair of blades (4) to pull vacuum (1) outside of the original PMSP dispense blades.

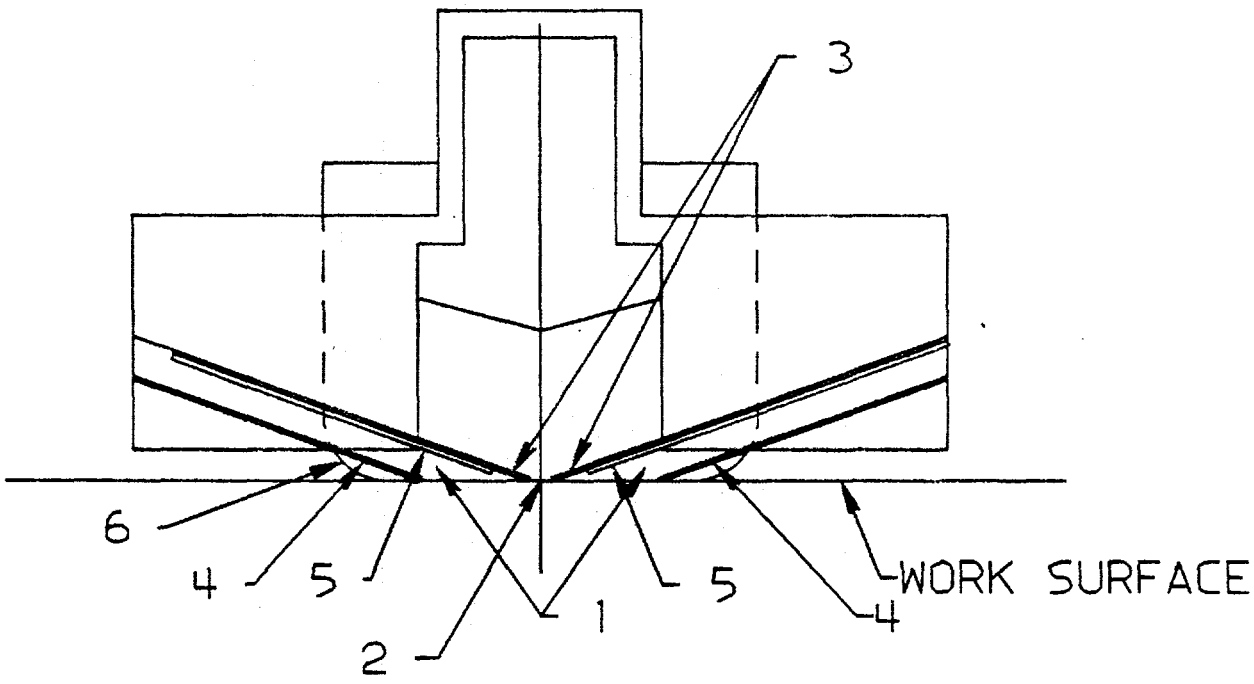
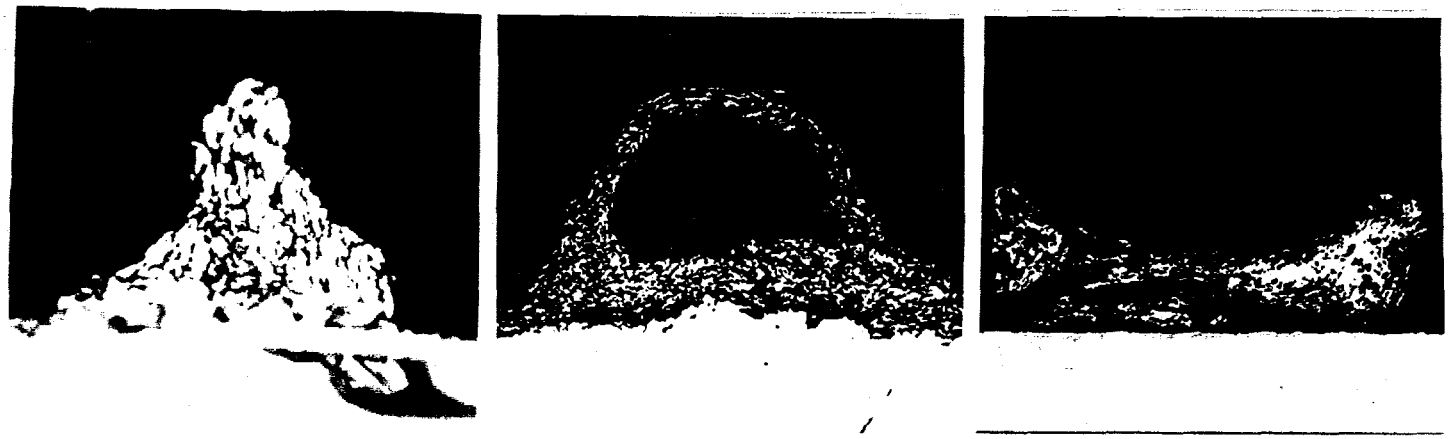


Figure 1 **is an end section view of the special PMSP dispensing head.**

THE PHOTOBUMP PROCESS was the second innovation that was a nesessitity for both bump survival and a cylindrical bump formation.

At the beginning of this project, stainless steel metal stencils were used with 0.010" diameter features on a 0.020 grid. Some were coated with titanium nitride, some were not coated. Figure 2 shows the results of the final bump form. Because of the retraction movement of the stencil from the wafer surface, the wet PMSP stuck to the stencil and formed either a solid volcano form (4) or a hollow volcano form (5). The other formation was screened, dried and then the stencil was removed. The crossection (6) looked good, but the bump survival was less than 50 % because some PMC (Polymer Metal Composite) adhered to the inside diameter of the stencil more than the wafer surface, even with a titanium nitride surface.



Solid Volcano form (4) **Hollow Volcano form (5)** **Dried PMC form with stencil attached (6)**

Figure 2 **Various crosssections of PMC with a metallic stencil shows bump formation variability.**

After the above observations were collected, it was obvious that a major deposition process change was needed.

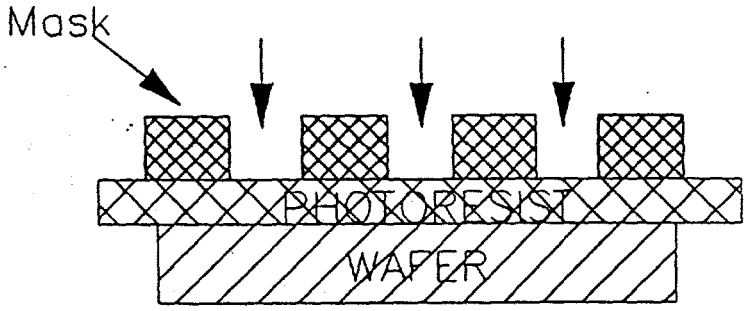
A good way to keep the bump yield high was to come up with a tough, dissolvable stencil. Conceptually, if it completely dissolved, each and every bump would survive. No shear or tension forces would be transmitted to the delicate PMC bump. The dissolvable stencil had to be resilient, to take the scraping motion of the dispense head blades, yet be of a material that could dissolve with non corrosive, light activity chemistry. The forming and stripping chemistry must also be totally compatible with the PMSP material. The process that was invented is called the Photobumping process showed on Figure 3.

The process flow is as follows: Photoresist is laminated to a wafer, using a fixture to keep it flat and protect the backside of the wafer. A glass mask, with precise metallized features, is carefully aligned to the wafer features. The photoresist is exposed with ultraviolet light. The photoresist is developed to remove the areas just above the wafer pads. The dispense head makes four strokes to fill the cylindrical forms in the photoresist with fresh PMSP. The PMSP material is dried at 70 degrees C for ½ hour. The top of each bump is concave, due to the volume reduction of solvents being driven off in the baking operation. A second pass dispense operation again fills the hole. It is baked again. Now the PMSP has a firm shape. The photo resist is then carefully stripped off to totally expose the PMC bumps. The wafer is then diced into individual chips and placed in chip trays.

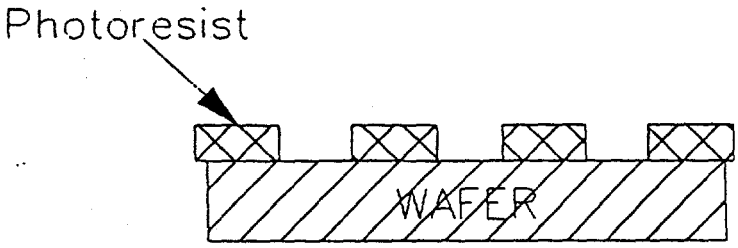
After the above processes were optimized, the results are shown on Figure 4.

1. Add Photoresist to Wafer

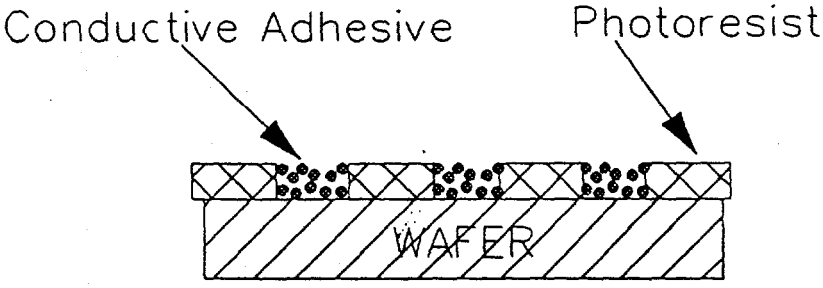
2. Place Photo Mask on Photo Resist & Align to Features on Wafer & Expose



3. Develop Photoresist



4. Screen on Conductive Adhesive & Dry Solvent



5. Strip off Photoresist (Clean Surfaces)

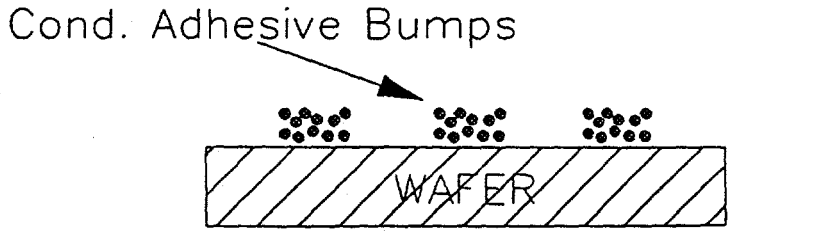


Figure 3 is the photobumping process

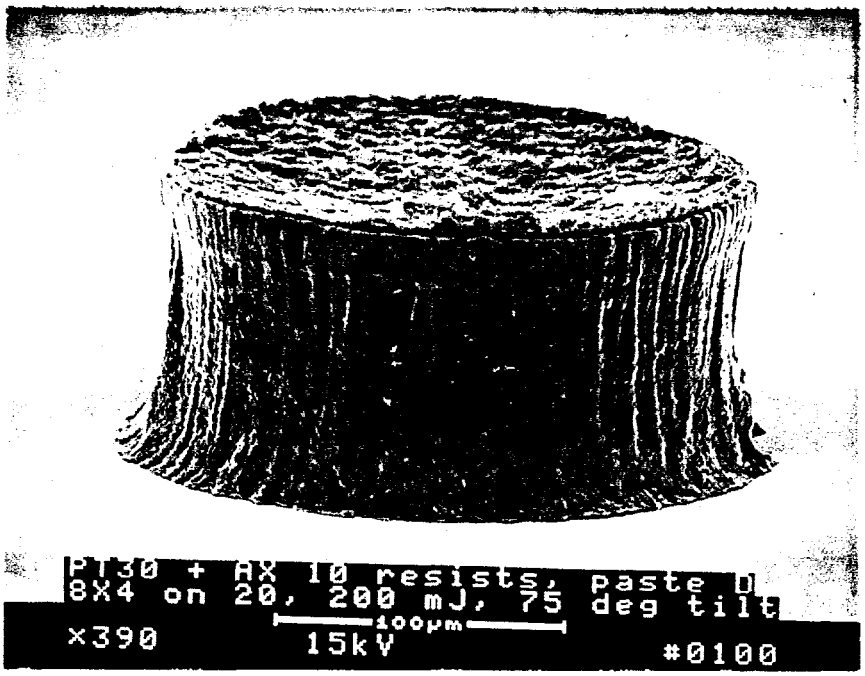


Figure 4 **a typical PMC photobump**

THE PHOTO BUMP RESIST had many physical challenges that eventually led to much higher bump survival yields.

At the beginning of the photo bumping process, Dupont aqueous Riston was used as the resist of choice. The yields were about 40%, however the bumps were very nicely formed. Unfortunately, the yields did not improve with continued development. Everything looked good until the resist was stripped off. The action of the aqueous resist, when observed under a microscope, showed that the stripping fluid went down the side walls of the bumps, then to the wafer surface. The photoresist started pulling away from the wafer and swelled, as shown in Figure 5. Under those circumstances, it was then understood that the swelling distortion played a major role in shearing the bumps from the wafer. In random areas, the resist had not lifted, so it was secured at that spot. However, a small distance away from the secured spot was resist that *had* pulled away from the bump and was distorting to the point that it was shearing bumps off.

A second problem with the aqueous resist, also shown in Figure 5 was the distortion of the holes in the photoresist caused by chemical incompatibility with the PMSP. In photobumping, 0.004" thick photoresist is imaged to create holes. These holes are filled with PMSP in two passes with a solvent drying process that occurs between the first and second pass. After the first pass filling, solvent from the PMSP interacted with the photoresist and caused the top surface, at the

circumference of the hole, to shrink. On the second pass filling, this slightly depressed surface fills up with PMSP. We call this blooming because the diameter of the bump is extended at the surface. When the photoresist is stripped, the thin surface extension of the bump diameter is folded over on the top of the bump. This fold created a ridge at the circumference of the bump that would make initial contact with the card surface during bonding. The result was a high probability of air entrapment at the joint interface. The blooming problem was corrected by changing from aqueous to a semi aqueous photoresist that was more solvent resistant. Flat surface bumps are made with 90% yield on five inch wafers.

At this stage several other types of photo resist material were processed. It was found that the solvent based resists worked but the stripping agents were too severe for the PMSP material. The best resist for this PMSP is semi aqueous. It is stronger than the aqueous resist and was more chemically inert to the PMSP material than the solvent based resist. The semi aqueous resist cured the blooming and the yields went above 90% immediately. Observation of the stripping action showed that the resist was completely dissolved in place. It did not detach or distort. That is why the semi aqueous works so well for this particular application.

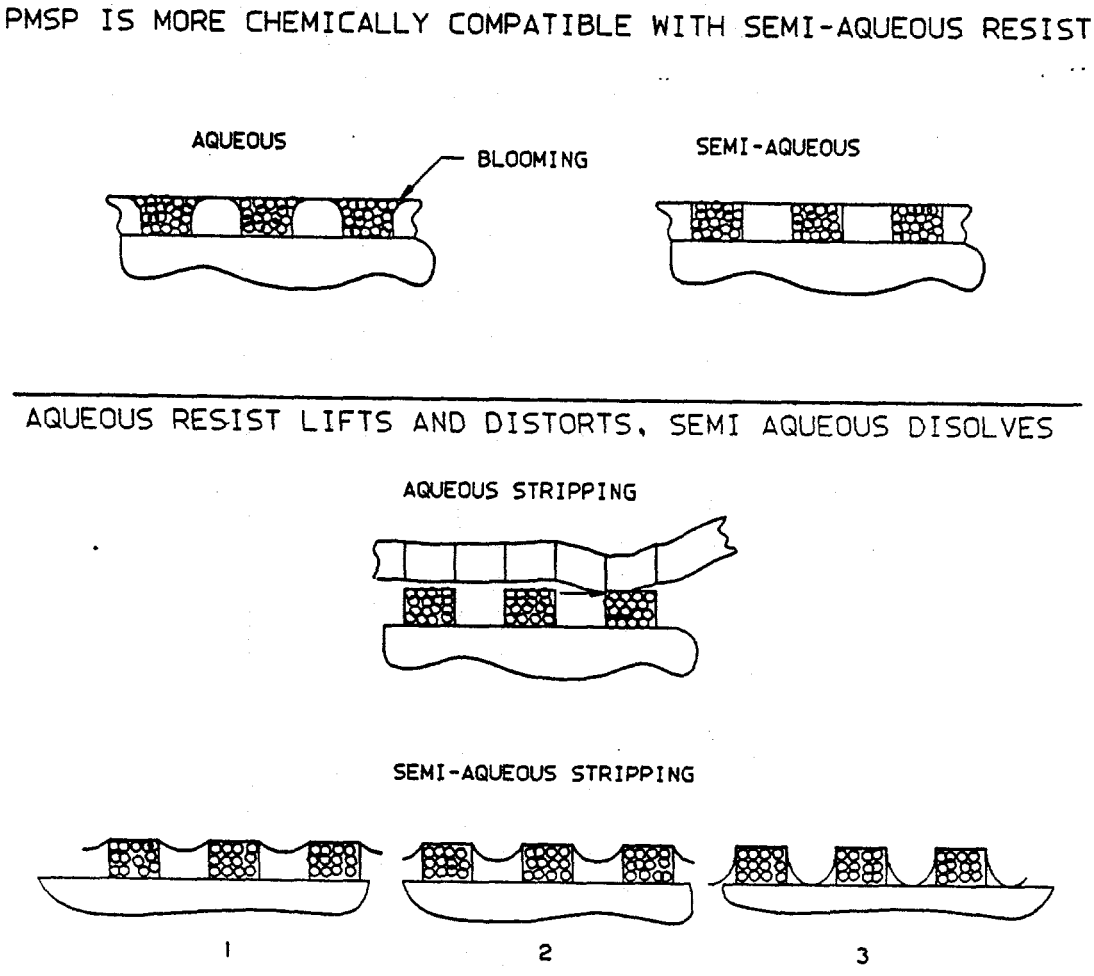


Figure 5 **several cross section views that show the physical differences between Aqueous and semi-aquous resists**

Void formation within the bump or on the outside of the bump was another technical challenge.

Void formation was to be the last technical challenge that needed to be addressed because it is the least obvious of all yield detractors. First, there was bump survival, then "Kings Crown" elimination, finally, inspection was focused on the sides of the bumps, and how they looked. If the wafer was tipped at a 45 degree angle or more, it was easy to see the absence of PMC material after the resist is removed.

There are three types of voids shown on Figure 5: internal (10), tunnel (11) and the mouse bite (12). The internal void can not be seen without cross sectioning, which makes it more difficult to detect. The tunnel void is an air pocket that goes completely under the bump without severing it into two separate pieces. Luckily, both the internal and tunnel voids can be prevented by slowing the velocity of the dispense head. The mouse bite void is an air pocket at the lower edge of the bump. It can be on the middle, but it is usually on the bottom corner of the bump. It is caused by the interaction of the PMSP material viscosity and the aspect ratio of the diameter to resist thickness.

Most of the latest experiments were to eliminate the mouse bite voids. Altering the pressure of the PMSP from 12 to 40 psi reduced the size of the voids. Slowing the speed of the dispense head moved the voids from tunnel to internal to mouse bite, in that order.

Internal void (10) **Tunnel void (11)** **Mouse bite void (12)**

Figure 6 **different types of voids**

Several different experiments were pursued to eliminate the mouse bite void:

1. Head vibration in the direction of travel. Did not have any major impact on void elimination.
2. Higher PMSP pressure. Had a slight impact on void size.
3. Vacuum at the resist surface. Had a very slight impact on void size.
4. A slight volume of ethyl benzoate solvent on the resist surface lowered the viscosity. It had a great impact on void elimination but the high solvent concentration in the PMC bump made it too weak. The bump fell apart during the dicing operation cleaning process...which is a very mild spray pressure.
5. Pre-heat photoresist.
6. The filled dispense head was degassed in a vacuum chamber.

PRESENT

At this time we have the capability to make 90% yield wafers with 0.004" high x 0.008" diameter bumps on 0.020" centers using PMC with 10% voids that are under 0.003" diameter in size.

To make high yields, our photobumping process is as follows:

PROCESS	PROCESS PARAMETERS
RESIST LAMINATION	0.003" and 0.001" thickness semi aqueous resist at 115C to 130C. at 0.3 "/minute speed.
EXPOSE	1000 watts ultraviolet light @ 150mj/(cm)(cm)
DEVELOP	Developer @ 30 psi and @ 30C with belt speed at 5"/min
PMSP APPLY # 1	Head force: 30#; Velocity: 0.1"/sec; PMSP pressure: 30 psi four strokes
BAKE	70C for 30 minutes
PMSP APPLY # 2	Head force: 30#; Velocity: 0.1"/sec; PMSP pressure: 30psi 2 strokes
BAKE	70C for 30 minutes
STRIP RESIST	Dupont S1100X at 50C for 30 minute soak
WASH	DI water at 23C

PROCESS	PROCESS PARAMETERS
DRY	Nitrogen at 23C
DICE WAFER	

FUTURE WORK

Several projects will and are being pursued to continue the PMC work so it can eventually be implemented by IBM.

The memory business is a long term, high value project that will likely be a major effort in the future. However, the feature sizes are more demanding than the current work. The memory bumps will be 0.004" high x 0.005" diameter on 0.010 centers.

Known good die testing is another good application for PMC material. The flexibility and high conductivity and disolvability make it ideal for a temporary contact. Since it can be completely washed away, it is also transparent to the rest of the solder bumping processes, including contamination.

Complete void elimination will be pursued aggressively. The pursuit of more aggressive aspect ratios between the bump diameter and resist thickness will need more experimentation and invention. Since most of the memory product mix has finer bump features, void elimination is a requirement.

Bonding Process Development

Objective

The objective of the bonding process development effort is to identify the significant process variables that influence the bond strength and fracture mode. Reliability tests are used to verify electrical and mechanical integrity. Process optimization will use the Design of Experiments (DOEs) to identify the fastest bond cycle that can be used to produce reliable joints.

Terminal Metal Finishes

In early work, four metal finishes -- soft gold, hard gold, palladium, and palladium nickel alloy -- were evaluated for initial contact resistance and contact resistance stability and were all found to be acceptable. These metal finishes were used in test vehicles and samples used for bonding process development.

Early DOEs

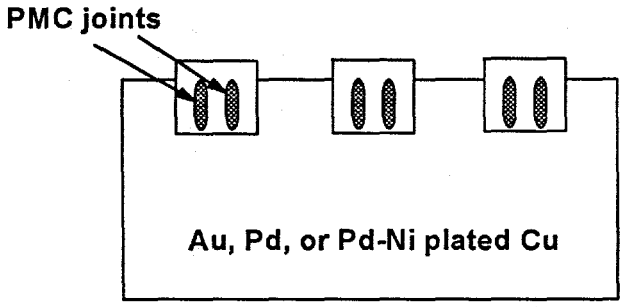
For initial bonding experiments with PMC, eight bonding variables were tested for significance in several DOEs, and six responses were recorded. The test variables and the responses used in these DOEs are as follows.

Test Variables	Response
1. Bond Temperature (≥ 180°C)	1. Bond Area
2. Bond Pressure	2. Shear Strength
3. Dwell Time at Bond Temp.	3. Polymer Bleed
4. Preheat Temperature	4. Internal Fissures
5. Temperature when Pressure is Applied	5. Perimeter Cracking
6. Surface Dispensed	6. Fracture Mode
7. Solvent Dry after Dispensing	
8. Cool Down under Pressure	

Simulated chips (5mm square, and 0.5mm thick Cu samples plated with Au, Pd, or Pd-Ni alloy) were bonded to plated Cu substrates (25mm x 50mm x 3.2mm, plating finish matched to that of the simulated chips), by dispensing 2 parallel polymer metal solvent paste (PMSP) lines on the chip, aligning the chip to substrate, and bonding under temperature and pressure. A schematic of the test sample is shown. The chips were sheared on an Instron and the above responses were monitored.

These DOEs identified bond pressure, temperature and dwell time to be the most significant variables. Higher bond pressures resulted in increased bond area, polymer bleed, internal fissures, perimeter cracks and adhesive failure of the joints. Higher bond temperatures and longer dwell times resulted in higher shear strengths. The predominant fracture mode was adhesive failure of

PMC joints in shear. The detailed discussion of these results is provided in the first (1995) annual report.



Peg Bonding with PMC (Paste A)

In addition to the above test samples, 0.125" diameter, and 0.25" long Au-plated Cu pegs were bonded together with PMC, to establish the bulk material properties of the PMC. The testing of pegs also helped verify the significant bonding variables. PMC paste was screened on one peg, dried (at 70°C for 30 minutes), and then this screened peg was bonded to another peg (w/o PMC) in a Universal test bonder (Figure 1). The bonded pegs were fractured in tension, and the fracture strength and mode were monitored as a function of PMC processing and bond parameters. Average failure stress of 1100 psi with a large standard deviation was measured. The joints failed adhesively. The high standard deviations negated the possibility of using the data to statistically differentiate the effect of various bonding parameters. The failures revealed a "starter crack" between the PMC material and the unscreened peg around the outside of the bond due to a slightly convex shape of the PMC as deposited on the screened peg. The presence of the starter crack in addition to the weak interfacial (adhesive) strength of the PMC resulted in the high standard deviation. Figure 2 illustrates the adhesive fracture observed in the pegs. Increasing the adhesive strength of the PMC to promote a cohesive or bulk failure in the PMC was desired.

Chip Bonding with PMC (Paste A)

During the second year of the research program, photobumped PMC chips were also available for chip bonding and process development. These chips had 0.008" or 0.010" features on a 0.020" pitch in an area array pattern. Detailed description of the screening and photobumping of chips is provided in the deposition section. The screening and the subsequent drying of the PMC joints resulted in craters on the top surface of the PMC deposits (Figure 3). These craters could potentially trap air in PMC joints, with a resulting high contact resistance (CR) of the joint. To eliminate the effect of these craters, the photobumps were either flattened (at 80 - 100 psi) or the craters were filled with supplemental deposits of the PMSP. These chips (Figure 4) were bonded using a commercial chip bonder from Research Devices (RDI, Model M8 Flip Chip Aligner Bonder) to the test boards (Figure 5). The photobumps on the chip were aligned to the chip site foot print on the board using the split optics on RDI bonder. To establish thermode temperatures for PMC bonding, the chip site on the board was thermocoupled and thermode temperatures were varied until a 210-220°C reflow temperature was obtained at the PMC joints. The bond temperature in the range of 210-220°C had resulted in high shear strength and stable CR of PMC joints in the comb experiments, described in Reliability section. The lower thermode temperature was limited to 120°C so as not to exceed the T_g of the BT board, and to prevent the resulting warpage of the board.

Thermal Modelling for Process Development

A transient thermal model was also developed which verified the chip and the card heating during the bonding cycle. A very small volume of the card, under the chip, heats up to the PMC bond temperature 225°C, while the rest of the card sets at 120°C. The heated volume is the size of the chip in area and about half the card thickness for the test board. The ability to heat this minimal volume to accomplish the bonding supports the concept of rapid heating through the chip. Based on this localized heating predicted by the thermal model, and the rapid heating capability of the Universal chip bonder, we were be able to accomplish short bond cycles (< 1 minute). The detailed discussion of the thermal modelling was presented at the 47th Electronic and Components Technology Conference in May '97 (copy of the paper is attached).

Contact Resistance (CR) of PMC Joints

After chip bonding the contact resistance of the PMC joints was measured. Two types of test chips were used - blanket test chips and stitched chips. The blanket chips had a 5000 Å evaporated Au layer with a 200 Å Cr adhesion layer. There was no test pattern on these chips. The stitched chips on the other hand had a stitch test pattern that complemented the pattern on the boards. The pads on these chips were stitched to one another with Al. Polyimide passivation defined pad openings were 0.2mm in diameter, and were plated up with electroless Ni (2000-3000Å) and immersion Au (2000Å) metallurgy.

The bonded chips were monitored for contact resistance, and fracture strength in a chip-pull test. These chips were also encapsulated for subsequent reliability testing. The contact resistance values measured for the blanket chips were in the range of 50 to 90 mΩ, and for stitched chips in the range of 600 to 900 mΩ. A large fraction of the PMC joints electrically opened when the chip was encapsulated. These fails were caused by the wicking of the encapsulant between the PMC bump and the pad, compounded mostly by the weak interfacial strength of the PMC adhesive. Further description of these fails and some pictures are included in the following section. The low adhesive strength of the PMC was also observed in the chip pull tests. In the chip pull tests a Cu slug 6mm in diameter was glued to the chip (w/ Loctite 415 adhesive) and pulled on an Instron. The fracture strengths of 300 psi or less were measured for the PMC joints, with adhesive failure of the joints from the card surface. Thus, improving the adhesion of the PMC was identified to be a critical goal in further development of reliable PMC interconnects.

Modified PMC - Paste C

Subsequently, a modified version of the PMC, Paste C, was formulated by IBM Yorktown in order to increase the interfacial strength. This modified version performed much better than the earlier material. When tested on the pegs described above, the new PMC demonstrated failure stress in tension of well over 4000 psi, and a tight (10%) standard deviation. In addition, the failure was driven in the bulk of the PMC (Figure 6). This high failure stress is comparable to the 5000 psi failure stress of the solder. These peg samples were used to characterize the failure envelope of the PMC at various loading conditions (different combinations of tensile and shear stresses) that the joint may see. The results and detailed discussion on these tests was presented at the ISHM/IMAPS Conference in March, 97. A copy of the paper is attached.

Process Development and Optimization for Chip Bonding

Blanket chips bumped with the new PMC (Paste C) formulation were bonded to test cards, and

when encapsulated the PMC joints did not electrically open. The chip pull on the new material was also significantly increased to 1400-2000 psi, with the joint failures occurring predominantly in bulk of the PMC joint. The new formulation of the PMC was now used for process development and optimization for chip bonding. Through numerous DOEs, the following bonding parameter windows have been found to give the strongest, most reliable interconnects:

	Process Window	Optimal Point Process
Upper Temp. Setting (chip):	285°C to 315°C	315°C
Lower Temp. Setting (board):	120°C	120°C
Bonding Force:	120 psi to 170 psi	135 psi
Bonding Dwell Time:	30 to 60 seconds	30 or 60 sec
Cooling (Lift-off) Temp.:	120°C and Cooler	70°C

Figure 7 shows the results of one particular experiment which helped to define these values. In this experiment several test chips were bonded with the Universal bonder, and fractured (chip-pulled) on an Instron. Bonding temperature and force were varied, while holding a 60 sec. dwell and cooling the assembly to 70°C after bonding. On a side, this exact same curve (Figure 8), showing an optimum process region to achieve high bond strength, was obtained 2 months earlier with a different set of chips and the Research Devices M8 Flip Chip Bonder. These results substantiate the repeatability and reproducibility of PMC bonding and performance. Main observations of these experiments are as follows.

In general terms, hotter temperatures give higher bond strength. The lowest temperatures seen by the adhesive in this window is 215°C, well above the melting temperature (180°C) of the PMC. Experiments with no bottom side heating have shown no significant difference in the thermal profile of the PMC joints. No degradation in bond strength occurs when bottom side heat is removed. This situation may be unique to our test vehicle and its thermal mass.

The data identifies an optimal pressure at 135 psi, that results in high bond strength (1400-2000 psi), and PMC bondline of 0.0025"±0.0002". These bondlines, although smaller than our target 0.003" bondline, resulted in representative encapsulation flow times (< 2 minutes), and typically no encapsulation voids. Bonding pressure below 120 psi gives very low tensile fracture strengths and encapsulated poorly. Forces over 170 psi produced high fracture strengths, but cracking of the adhesive occurred at these high pressures, and bondline thickness became too small (0.0013"±0.0003") for rapid encapsulation. The small bondlines also result in voids in encapsulation and a significant reduction in fatigue life of encapsulated (solder) joints.

Dwell times below 30 seconds showed a drastic reduction in bond strength. Times in the 30 to 60 second range gave the best bonds, with little difference observed for dwell times in this range.

Immediate liftoff of the upper thermode had some destructive effect on the joint. Allowing the adhesive to cool and solidify before lift-off gave excellent results. Cooling the bond assembly to 120°C or below, before removing the bond pressure resulted in high fracture strengths and stable contact resistance of the joints.

The standard deviations of fracture strengths measured for PMC joints were 10% - 20% of the mean. All attempts to reduce the variability of this adhesive fracture strength did not result in improvement. We attributed this variability to the lot-to-lot variability in screened ECA bumps, to sample preparation variability, and to sample loading and stresses during fracture testing on the Instron. The observed variability is quite typical of adhesive joint test methods. Furthermore, it seems that higher bonding pressure and temperature gave a tighter spread than lower parameter values.

Tensile fracture strengths of chips bonded within these parameter windows typically varied from 1400 psi to 2000 psi. (The highest strength achieved to date is 2354 psi.) Fracture mode varies from chip to chip, but fracture always occurs within a boundary layer near one of the interfaces. Blanket chips tend to fracture at the card side 50 % of the time, and at the chip side the other 50 %. Chemical analysis has shown adhesive left on the pads where it seems the fracture has occurred, and in assemblies which demonstrate high fracture strength, adhesive can be visibly seen remaining on the pads. These visual observations and chemical analyses indicate that the failure is primarily cohesive.

Ten sets of chips bonded to boards were evaluated in environmental tests. Three PMSPs were used - pastes A, C, and D. The bonding results and reliability performance of PMSP D were encouraging. But, PMSP C appeared to have more robust fracture strength and stress test performance and was thus selected as the preferred paste. The results and detailed discussion of the environmental test performance of the three pastes is provided in the Reliability section.

PMC Shelf Life

To establish the PMC shelf life (of screened photobumps) several chips screened in Feb. '97 were bonded in Aug. '97. After bonding, the chips were either fractured, encapsulated, or exposed to reliability testing (deep thermal cycle of -55 to 125°C). High fracture strength (1400 psi to 2000 psi), cohesive fracture, and 1000+ ATC cycles without a failure were observed for these stored chips. The results indicate a shelf life in excess of 6 months for the PMC photobumps. We anticipate a much longer shelf life for the PMC bumps, since the thermoplastic resin in the PMC is not likely to degrade. Nonetheless, actual shelf life, if any, for the PMC should be established with further experimentation.

PMC Rework

A rework process has been established for the PMC. Non encapsulated chips were mechanically pulled from the chip site (on Instron), and new chips were re-bonded to achieve good bonds. The card side was wiped clean with IPA before the re-bonding. The small adhesive residue left behind on the cards side did not interfere with the re-bond process. The new chips bonded at the reworked sites exhibited average contact resistances for all 16 nets per chip. One reworked card (two chips), was also exposed to deep thermal cycle (-55 to 125°C) and exhibited solder equivalent performance. No fails occured in 700 thermal cycles, and a couple of joints on one chip failed (CR increase >100 mΩ) at 1000 cycles. This preliminary result is very encouraging and needs to be reproduced and repeated to develop a statistical data set.

Stitch Chip Anomaly

All above results are encouraging and reproducible, and were obtained with blanket Au chips. The test results using chips with a stitch pattern have been consistently disappointing, despite identical photobumping and bonding processes for stitch and blanket chips. To explain this anomaly, we hypothesize that the polyimide passivation on the stitch wafers gets etched during the photoresist strip with Ethanol Amine (DuPont S1100), generating polyamic acid which adsorbs on the PMC bumps, and results in a weak interface between the bump and the Au pad (on card) during bonding. Chemical analysis of the PMC bumps on blanket and stitch chips should be done to verify the hypothesis. If acid adsorption is evidenced on the PMC bumps, inorganic passivation can be used for the stitched wafers in the future.

Summary of Bonding Process Development

- A repeatable and reproducible bonding process has been established and optimised for Paste C.
- Bulk fracture strength of 4000 psi (in tension), and a cohesive fracture was obtained for PMC joints.
- Bonding temperature, pressure, and pressure on cool-down (to 120°C) were identified as key process variables.
- Photobumped chips bonded to BT boards, when pulled, fractured cohesively at 1400-2000 psi fracture strength.
- Optimum bond parameters resulted in PMC bondlines of 0.0025"±0.0002" and encapsulation results comparable to soldered flip chips.
- Stable contact resistances have been measured in reliability testing of encapsulated PMC joints.
- Shelf life in excess of 6 months was identified for the PMC.
- Preliminary rework process and feasibility is established. Reworked chips (2) exhibited stable and a reliable electrical performance through stress test (-55 to 125°C).

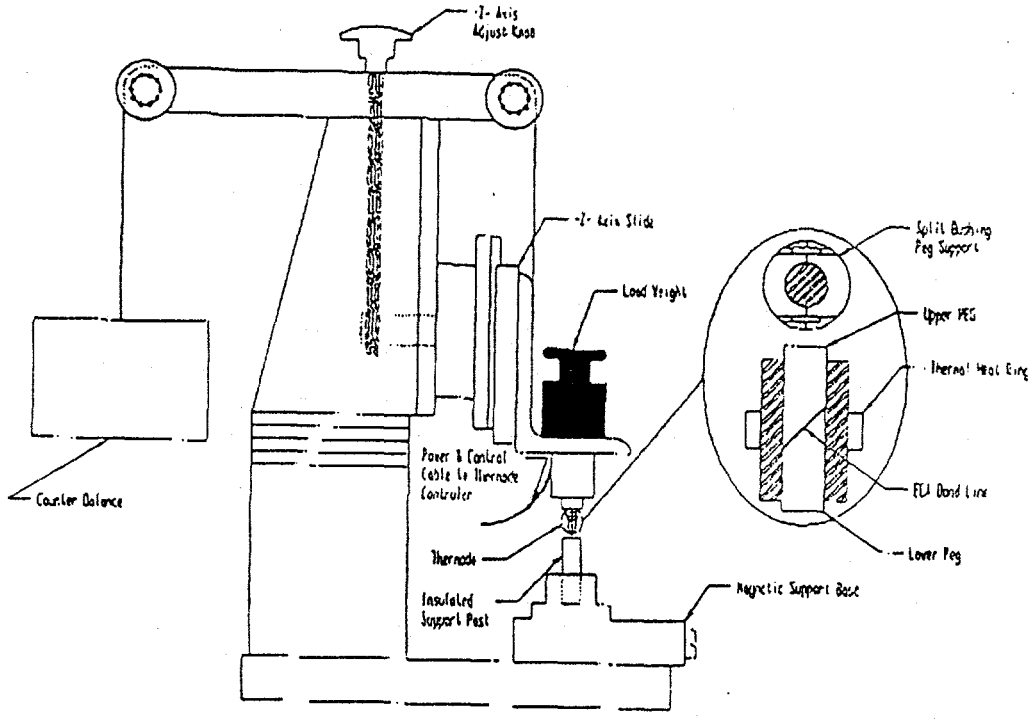


Figure 1: Peg bonding system designed and built by Universal for characterization of PMC bulk material properties.

PASTE "A"

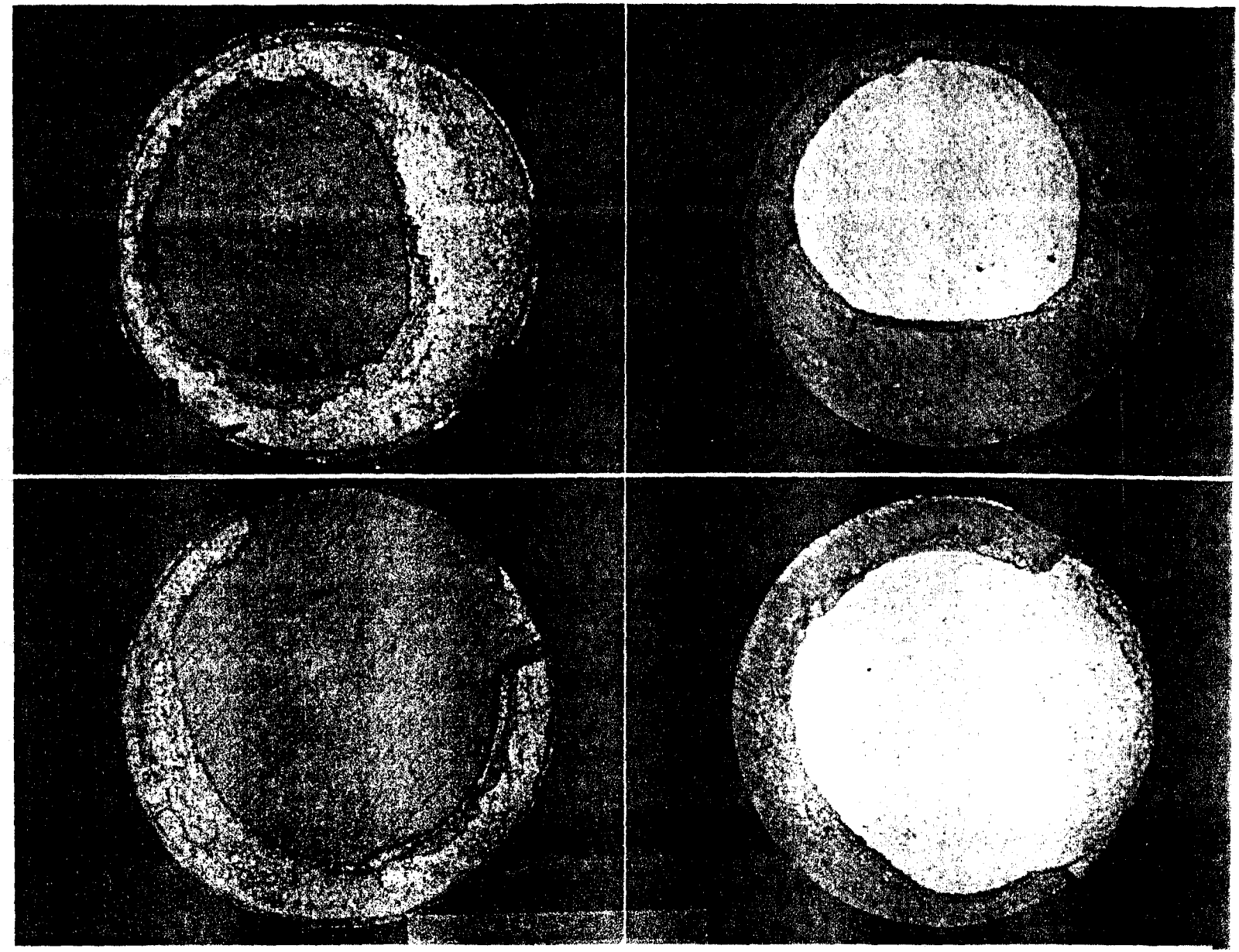


Figure 2: Adhesive fracture of PMC joints (paste A) between Au-plated Cu pegs. The presence of a "starter crack" alongwith the weak adhesive strength of the PMC resulted in low fracture strength (1100 psi), and high variability.

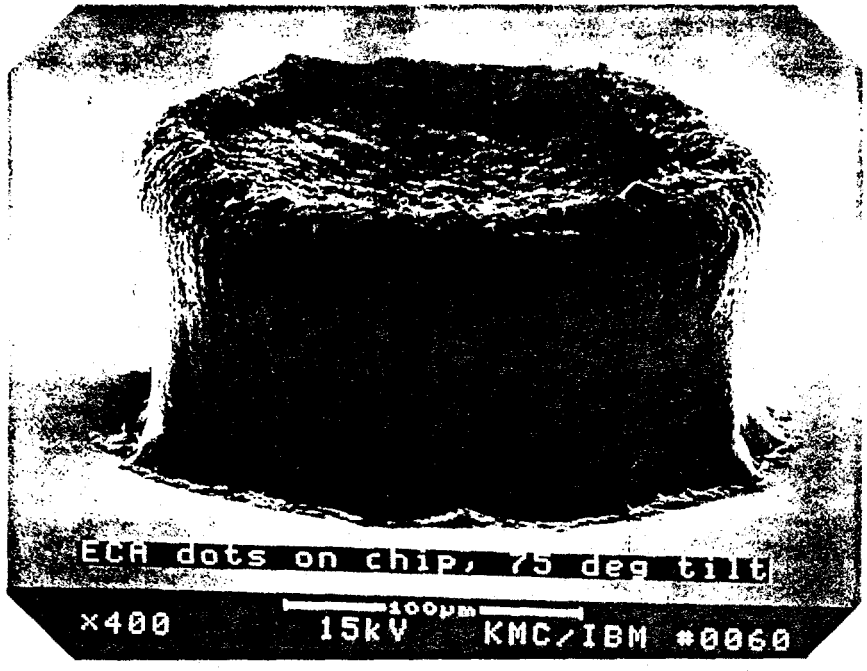


Figure 3: Crater formed in the top surface of the PMC joints screened on blanket wafers. These craters resulted in low bonding areas, and high contact resistance of the joints.

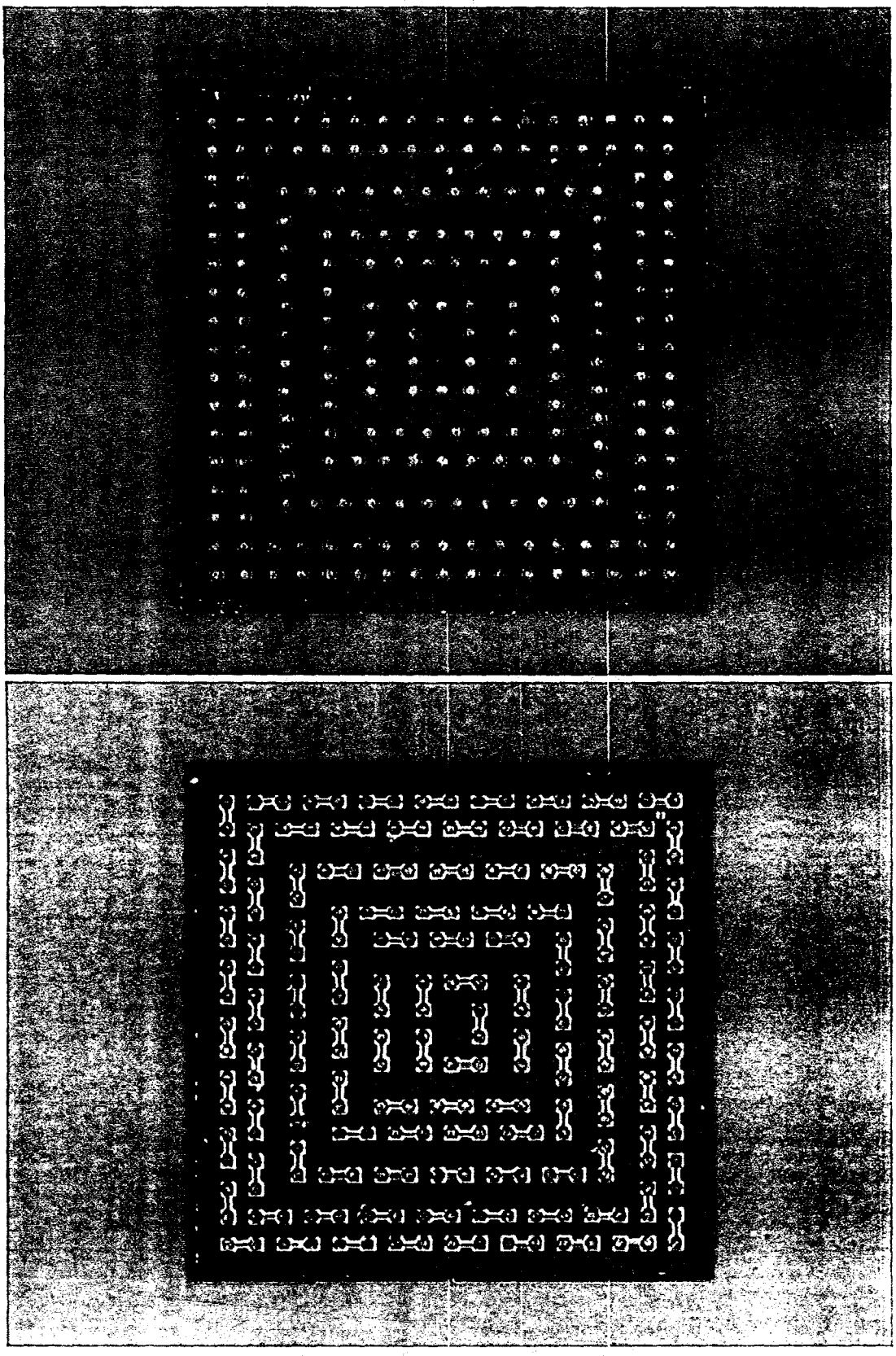


Figure 4: Photobumped blanket and stitch chips with 0.010" deposits on a 0.020" pitch.

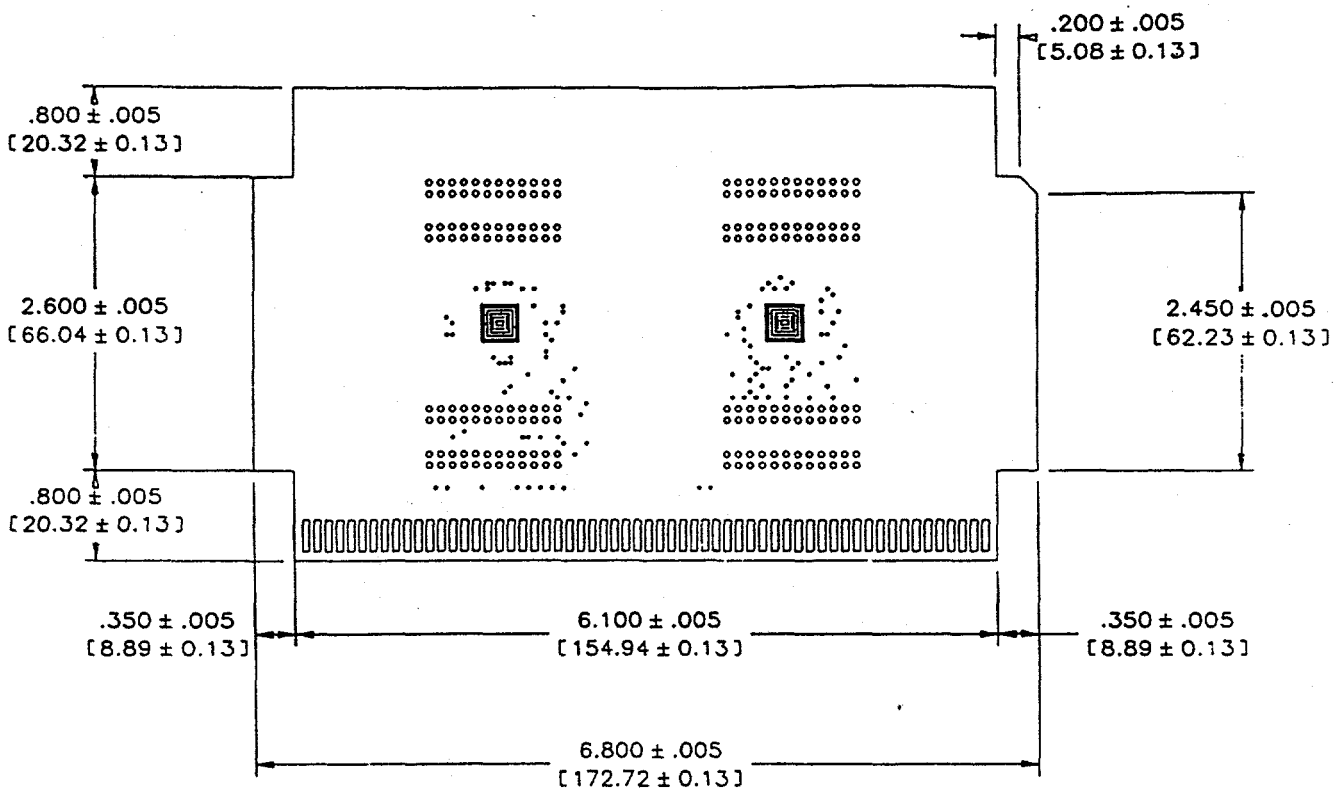


Figure 5: 10 on 20 card (0.010" pads at 0.020" pitch) of 2S0P construction (2 signal and 0 power planes).

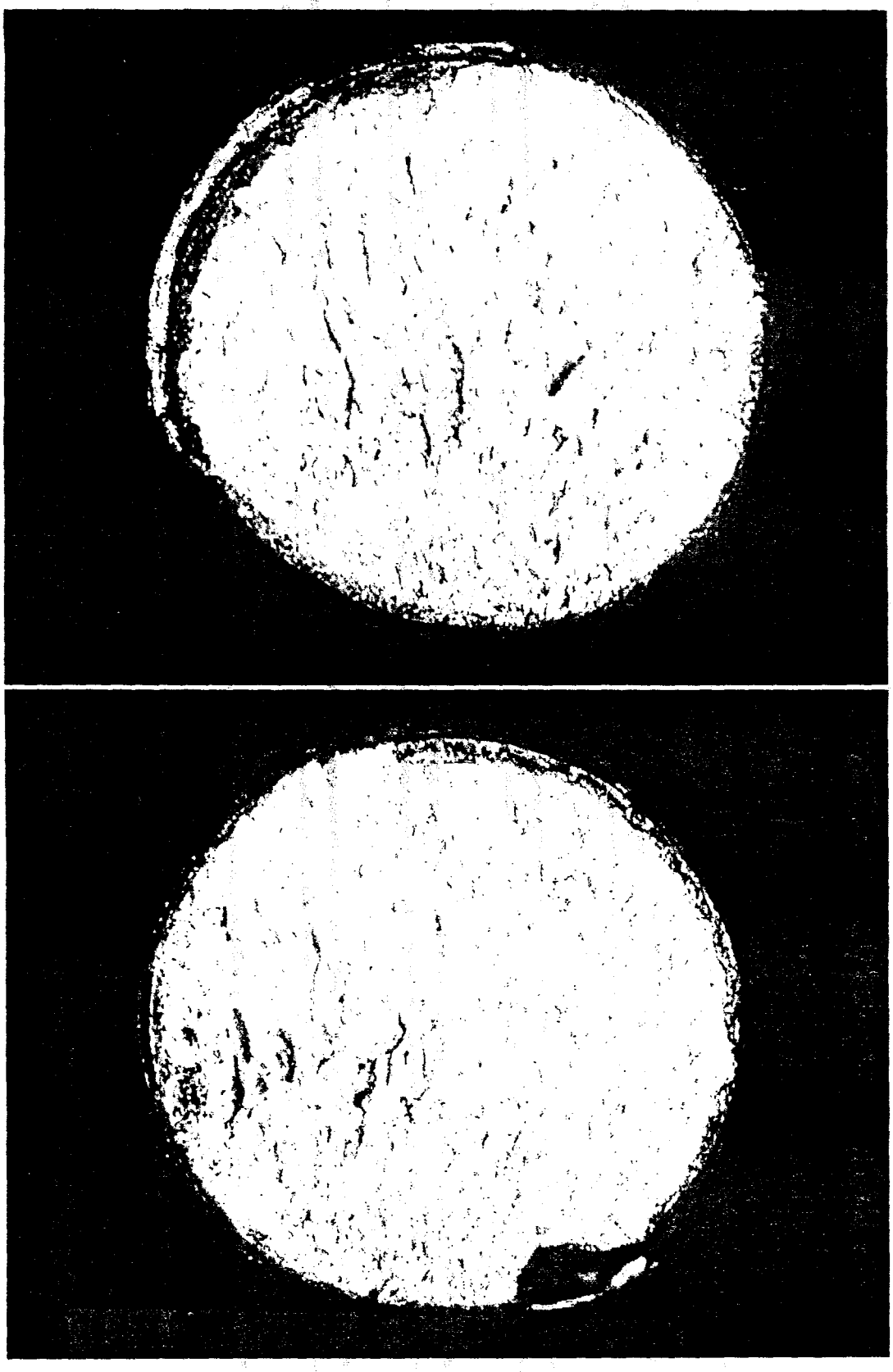


Figure 6: Cohesive fracture of PMC joints (paste C) between Au-plated Cu pegs. Fracture strengths in excess of 4000 psi were achieved.

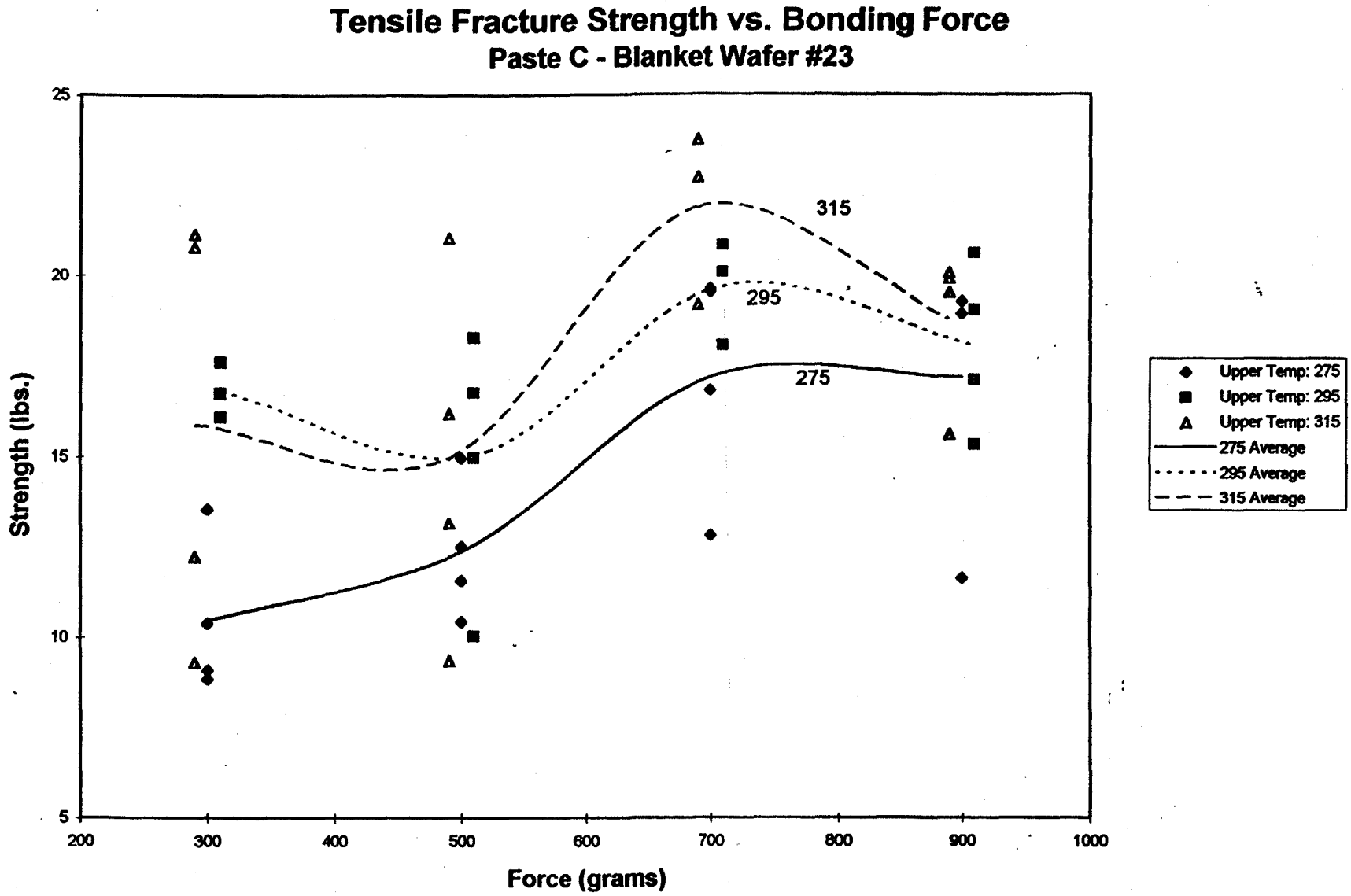


Figure 7: Tensile fracture strength of PMC joints (chip-pull on an Instron), as a function of bonding load at different bond temperatures (chip side). Optimum bond parameters are established based on these DOEs.

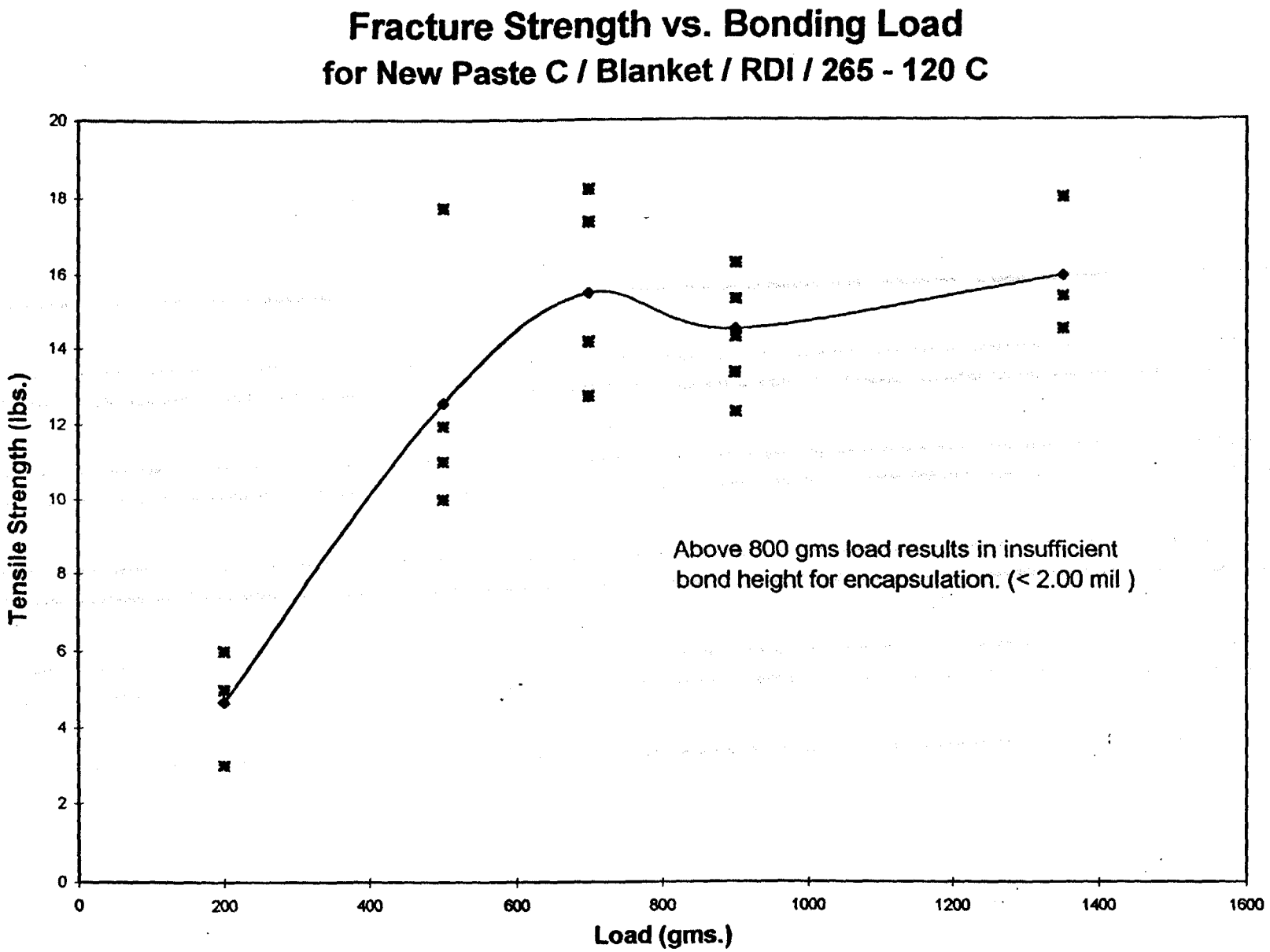


Figure 8: Tensile fracture strength of PMC joints (chip-pull on an Instron), as a function of bonding load on the Research Devices bonder. This data was reproduced on the Universal bonder (Figure 7).

Characterizing The Failure Envelope of a Conductive Adhesive

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Abstract- The importance of flip chip technology is beginning to grow as the use of such technology is seen to be more and more advantageous. The search for alternatives to lead-based solder has also led to the study of conductive adhesives as a possible replacement for solder interconnect technology. Under a grant from DARPA, the IBM and Universal Instruments Corporations have sought to create a flip chip package using conductive adhesive interconnects. This paper presents the preliminary results of mechanical testing designed to determine the static failure envelope of the adhesive. A difference in fracture mode was observed between the tensile and compressive samples indicating that a change in failure mechanism occurred. Further work is being conducted in order to isolate the specific failure mechanisms involved.

INTRODUCTION

While flip chip attach (FCA) does not constitute a large portion of the microchip market today, this technology is expected to grow at an accelerated rate in the near future and it is likely that FCA will be an important consideration in the microelectronics industry as the next century opens [1]. Multi-chip module (MCM) technology, as well, is becoming more attractive to microelectronics customers [2]. Indeed, FCA appears to be an appealing way to implement MCM technology [3]. Concomitant with these trends is the ever present drive for lower cost assembly methods. In addition, environmental concerns and legal uncertainties with respect to the use of lead-based solder has helped to motivate the search for lead-free alternatives to solder interconnection [4].

A project was undertaken whose goal is the development of an alternative to solder interconnect technology in flip chip devices. The project is a joint effort between the IBM Corporation (Endicott, NY. and Yorktown, NY.) and the Universal Instruments Corporation and partially funded by DARPA (Defense Advanced Research Projects Agency). Central to the project is the creation of an isotropically and electrically conductive adhesive as well as the process needed to assemble flip chip packages with such an adhesive. Reworkability was also a stated goal in light of MCM technology considerations.

This report focuses on work completed after a conductive adhesive had been formulated and determined to be the "official" adhesive for the project. After an overview of the adhesive, the static failure properties of the material will be reviewed. Specifically, the static failure strength of the material as a function of loading condition will be examined along with the testing method used to generate the data. The results will be useful in several ways. First, the information obtained for this report will be used in conjunction with finite element analyses of the chip package to assess the performance of the adhesive. In addition, the work required for this report produced a testing procedure that can be used to assess the potential of other materials. Comparison to the "official" conductive adhesive will thus be helpful for possible future use either connected with the project or independent of it. In fact, this type of comparison has already begun with an alternative formulation considered to be independent of the project.

OVERVIEW OF MATERIAL

In light of several advantages related to thermoplastics, it was decided that a polymer or copolymer from this group would be chosen. For example, since a paste was desired that could be used for MCM applications, the paste needed to be reworkable. This would allow one bad chip to be replaced without having to start with a new module, thus losing all of the good chips already on the module.

A thermoplastic polymer is well suited for such a requirement. In addition, thermoplastics do not require a B-staging process in order to partially crosslink the material for handling considerations. Neither do they require storage at low temperature in order to retard further crosslinking. Thus, a thermoplastic was chosen to take advantage of these qualities.

With the above considerations in mind, a polyimidesiloxane was developed by researchers at IBM, Yorktown in order to meet the needs of the project [5]. This material has several advantages other than the ones already mentioned including good thermal stability and good solubility [6]. A long shelf life is also an advantage of this formulation. The polyimidesiloxane is dissolved in a solvent and can remain at room temperature for many months in this "paste" form. The rheological properties of this paste were also important in light of the need for dispensing the material. Here again, the IBM formulation was tailored to meet the specific dispensing requirements.

A possible disadvantage of this material is poor interfacial strength, especially at higher temperatures. Indeed, the formulation under consideration in this report is not the original formulation developed by the researchers. After static as well as reliability testing, however, it was clearly evident that the original formulation suffered from a level of interfacial strength that was unacceptably low. Thus, a second version was developed and it is this second polyimidesiloxane formulation which is under review in this report.

Electrical conductivity was accomplished by loading the polymer with silver flakes. Several factors motivated the choice of silver including the conductivity of silver which is among the highest of the metals that were under consideration. In addition, silver flakes are relatively inexpensive compared to many of the other choices.

Several assumptions were made concerning the behavior of the conductive adhesive. First, it was assumed that the adhesive joint behaved in a linear-elastic manner. This assumption was clearly shown to be valid as testing progressed. In addition, it was assumed that the material was strain rate independent. As with the last assumption, this one was made at room temperature where the testing would take place. Before test data was taken, several different strain rates were tested in an informal manner and variations in joint strength were not detected. Finally, it was assumed that the residual stresses due to processing would not be a factor.

SPECIMEN PREPARATION

It was decided that a sample design should be chosen such that various stress states (both tension and compression) could be achieved with the same basic design. It was also necessary that the specimens be tested using relatively simple equipment such as an Instron uniaxial tester. A custom designed, six-axis, micromechanical tester was available but it was recognized early on that the loadcell's (the only loadcell available for this apparatus) capacity of eight pounds would not be adequate.

The testing sample consisted of two copper pegs (d=0.125 in.) with a circular cross section that were bonded together using the adhesive. The pegs were cut at a number of angles including zero (butt sample), fifteen, thirty, and forty-five degrees. This would allow the collection of data at a number of different loading conditions using a single Instron tester with tensile and compression loadcells.

Preparatory work was required before the conductive paste could be tested. The pegs were first inspected and unsatisfactory pegs were discarded. The peg faces were then electroplated with gold in order to mimic the gold-plated copper pads on the card. Following this, the conductive adhesive was screened onto the pegs. To begin this process, the pegs were cleaned using dilute hydrochloric acid in order to remove the various organic compounds that can accrue. A peg was then placed in a fixture which corresponded to the respective angle of the peg. A stencil with the appropriate opening was then placed on top of the fixture and the adhesive was screened onto the peg face. The peg was then removed from the fixture and placed on a hot plate. This process was repeated for each peg. After sufficient time on the hot plate, the solvent had completely evaporated off such that the deposits on the pegs were solid.

The bonding process was implemented using a prototype machine constructed by the Universal Instruments Corporation for this specific purpose. The bonding machine consists of a resistive heating element controlled by an open-loop computer program and situated between two platforms. A two piece aluminum collar with an inside diameter equal to the outside diameter of the pegs was also used for the bonding process. The two pegs from a single pair were placed, face to face, on one side of the collar and the two halves of the collar were brought together, enclosing the pegs. The collar was then placed inside the resistive heating element which is itself a collar whose inside diameter is approximately equal to the outside diameter of the peg collar. The necessary weight was then placed on top of the upper platform which was then lowered into place. The computer program was

then used to set the bonding parameters based on the desired bonding temperature and time. Following this, the bonding process was carried out. This was repeated for each peg set.

RESULTS

Table 1: Raw Data

Peg Angle	Loading	# of samples	F_y (lbs.)	Std. Dev. (lbs.)
0	Tensile	29	51.0	6.1
15	Tensile	28	49.5	3.5
30	Tensile	28	51.8	4.6
45	Tensile	30	63.0	4.8
30	Comp.	31	-123.3	9.4
45	Comp.	25	-103.8	12.2

The raw data for each test can bee see in Table 1. These numbers represent a large improvement over the performance of the first conductive adhesive formulation that was tested. For this first formulation, the average value of F_y (failure load) for the zero degree peg samples was about 20 lbs. Moreover, the samples failed at the polymer-peg interface (adhesive) indicating weak interfacial strength. The failure was thus not representative of the actual material strength. With the second formulation however, failure of the zero degree peg samples occurred through the bulk of the conductive adhesive (cohesive) thus giving a more accurate picture of the bulk material strength. A standard stress transformation was performed to find the normal and shear stress components for each loading condition. Since F_y is the only non-zero load component, the relevant equations become

$$\sigma_{nn} = \frac{F_y}{A}\cos^2\alpha$$

$$\sigma_{ns} = \frac{F_y}{2A}\sin 2\alpha$$

where A is the peg cross section area, F_y is the failure load, and α is the angle between the loading direction (y) and the normal to the failure surface (n). Figure 1 shows the failure envelope based on the equations and the test data.

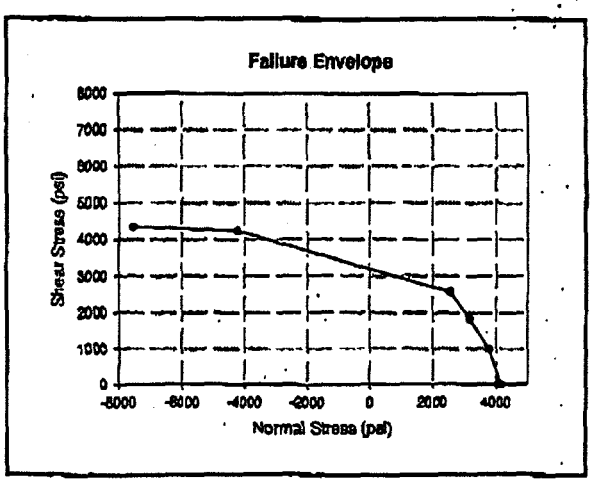

Figure 1: Failure Envelope of an Electrically Conductive Adhesive

Two different failure modes occurred during testing. Aside from some relatively minor edge effects, failure in the four tensile loading conditions was cohesive. This was not the case, however, for the two compression loading conditions. For the compression samples, failure consistently occurred along the interface between the adhesive and the peg. In addition, the left side of the failure envelope was expected to be linear and inclined. Instead, the shear stress values for the two compression conditions were nearly the same. Thus, while the tensile information should be fairly representative of the actual material strength, the compression data appears to be artificially low due to a change in failure mode. Further work is being conducted to investigate the interfacial failure mode and to modify the testing procedures in order to drive the failure through the bulk of the adhesive for each loading condition. It should be mentioned that the compression loading conditions are rarely seen in packaging applications so clarification of the failure mechanisms associated with those conditions is more of a theoretical interest than a practical one.

ACKNOWLEDGMENTS

The authors would like to thank T. M. Niu for his help during testing.

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A STUDY OF THE THERMAL CHARACTERISTICS OF A CONDUCTIVE ADHESIVE CHIP ATTACH PROCESS

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ABSTRACT

Electrically conductive adhesives (ECAs) have been proposed as an alternative to solder in the surface mount (SMT) and flip chip attach (FCA) applications. This paper describes the development of a transient heat transfer model of a chip bonding process using the ECA bumps. The chip is heated using a top thermode directly contacting the chip and the card is heated from the back side (z=0) using a heater. A detailed three-dimensional heat transfer model to account for the conduction, heat storage and convection and radiation from the card is developed using the finite volume technique. The spatial and temporal temperature distributions are studied through initial ramp-up, dwell and cool-down processes. It is seen that the bump temperatures are dominated and controlled by the heating process near the chip as opposed to heating the back side of the card. The numerical model is verified via actual measurements and the agreement is within 15 percent.

NOMENCLATURE

c_p	specific heat capacity (J/kg-K)
F	radiation shape factor
h	heat transfer coefficient (W/m^2K)
J	radiosity (W/m^2)
k	thermal conductivity (W/mK)
k_{eff}	effective thermal conductivity of the bump layer (W/mK)
L	characteristic length (m)
q	heat flux (W/m^2)
R	thermal resistance (K/W)
Ra	Rayleigh number, eq [6,7]
S	radiation source term in energy equation (W/m^3)
t_{eff}	effective thickness of the bump layer (m)
T	temperature (K)
V	volume (m^3)
w	interconnect layer width (m)
x,y,z	coordinates (m)

subscripts

s	surface
∞	ambient
⊥	perpendicular
//	parallel

superscripts

r	radiation

greek letters

α	thermal diffusivity (m^2/s)
ϵ	total hemispherical emissivity
ρ	density (kg/m^3)
σ	Stefan-Boltzmann constant (W/m^2K^4)

INTRODUCTION

Isotropically electrically conductive adhesives (ECAs) are used in the electronic packaging industry, primarily as die attach materials, [1,2]. A more recent application for ECAs is solder replacement in electrical interconnection. Advantages for this new interconnect technology include lower processing temperatures, reduced environmental impact and improved mechanical fatigue performance, [3-9]. Disadvantages include limited electrical contact resistance experience, the requirement for noble metal conductor surface finishes, weaker bond strength and concern for silver migration, [1,4,6,7,10,11].

A thermoplastic ECA filled with silver has been developed that has electrical contact resistance comparable to eutectic solder [12]. Additionally, this material offers fine feature definition. Concerns with bond strength less than solder and silver migration are overcome in flip chip attach (FCA) applications that inherently require underfilling. The underfill provides robust mechanical integrity and seals the silver from the environment. Chips attached with these thermoplastic interconnects can be reworked prior to underfilling.

A brief description of the overall ECA/FCA process is provided

as background. The main focus of this paper is to present the methodology and results of a transient thermal model that was developed to understand the flip chip bonding process. The mathematics upon which the model is based are presented. Next, the boundary conditions are described for both convection and the thermode that provides heat input during the bond cycle. Finally, results of the model are compared to experimentally measured data.

ECA/FCA PROCESS BACKGROUND

An FCA process has been developed that uses a silver filled thermoplastic ECA. ECA bumps are defined at a wafer level as shown in Figure 1. These bumps are the dried thermoplastic adhesive and measure 0.2 mm in diameter and 0.1 mm high. Next, the wafers are diced. Chips can be stored at room temperature prior to the bonding process. In this study, the chips measured 9.4 mm square with 256 pads, 0.25 mm in diameter. Polyimide passivation was used. During bonding, a chip is picked and aligned to the chip footprint on a laminate carrier. The chip can be placed with a load between 50 to 300 grams. With the load applied, the heat cycle begins and establishes a bond. Since this bond process does not have the advantage of gang reflow attach, characteristic of solder, the cycle must be very rapid to be competitive. Preliminary estimates indicate that a pick, align, place, bond, cool cycle of less than 30 seconds can be competitive with solder attach processes. The chips are underfilled after bonding to provide mechanical integrity, fatigue life and protection from silver migration. The chip bond process is important in that the resulting assembly must have reliable interconnects and be cost competitive.

It was determined that a transient thermal model of the bonding process would provide valuable insight and guidance in developing an optimized process and chip bonder design. The ideal process was thought to be one that allowed very rapid heating to as small an area as possible, without generating thermal gradients in the laminate that would cause dynamic warpage.

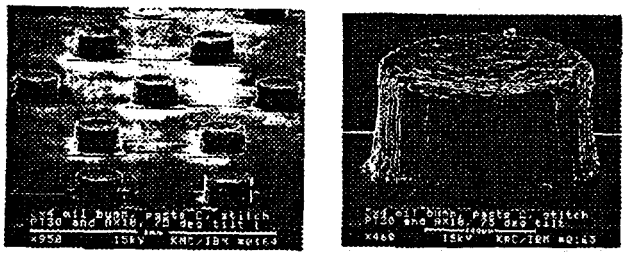

Photo 1 Photo 2

Fig. 1 ECA bumps on the chip (photo 1) and magnified view of the bump (photo 2).

A schematic of the laminate carrier with the chips and heater (back side, z = 0) is shown in Figure 2. The location and size of the chip bonder heating thermodes for both chip and laminate are shown by the dotted outline in Figure 2. The card was prepared with five K-type, chromel-alumel thermocouples (40 gage wire) at locations marked in Figure 2. One thermocouple was placed in the center of the chip site while the other four were placed at varying distances away from the chip site. These thermocouples were embedded in the card so that the tip was flush with the card surface and were fixed in place using a thermally conductive epoxy (k=1W/mK). This card was used to experimentally record temperatures during an ECA/FCA bonding cycle. The input ramp rates of the top and bottom heating thermodes were noted. The resulting thermal profiles of these five locations were modeled based on the thermode ramp rates, material properties, and heat losses. Detailed development of the thermal model, comparison of measured and predicted temperatures, and spatial and temporal characteristics of the process are now discussed.

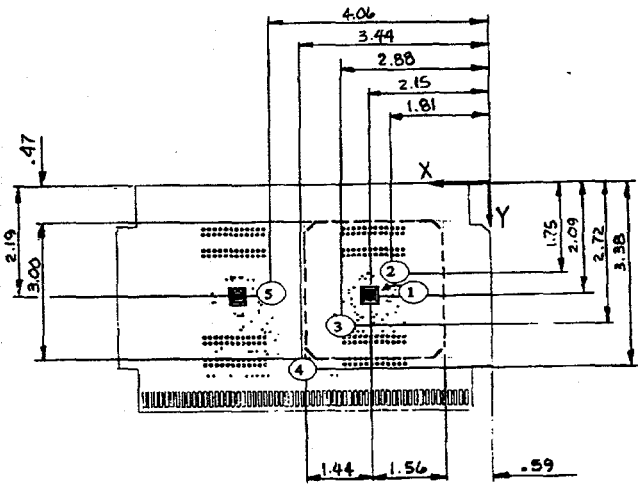

Fig. 2 Thermocouple locations 1 - 5 and bottom thermode (heater) outline on the card used for experimental validation. The top thermode covers the chip site. Point 1 is below the chip. The card is 1.6 mm thick with two copper planes 0.03 mm thick placed 0.35 mm from the card surfaces. All dimensions above are in inches.

MATHEMATICAL FORMULATION

The card with its power planes, the chip and the interconnect material were modelled using the finite volume method. The geometric computer model with the different blocks corresponding to the different materials in the package is shown in Fig. 3, which shows the isometric view. Material properties and thicknesses of the different blocks are shown in Table 1. The details of the governing equations, surface radiation, convection at the surface,

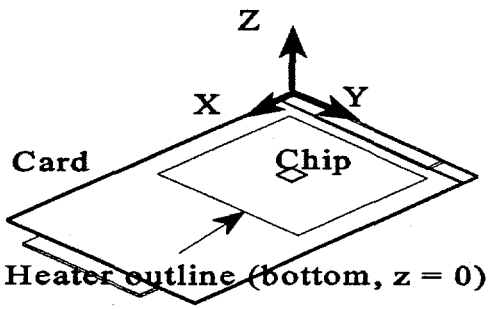

Fig. 3 Isometric view of the geometric computer model showing the different blocks.

Table 1. Material Properties [14] and Dimensions

Item	CARD	Copper+	Silicon Chip
Thickness $x10^3$ (m)	1.6	0.03	0.75
α (m^2/s)	*$1.6x10^{-7}$	$1.1x10^{-4}$	$8.7x10^{-5}$
k (W/mK)	**0.34	381	145

* Estimated from an average of four board materials [13] over a temperature range of 300 K to 433 K.
**k = 0.34 W/mK estimated from the thermal diffusivity.
+The copper planes are placed 0.35 mm from the top and bottom surfaces of the card.

thermode boundary conditions and modeling of the arrays of the bumps follow.

Governing Equation

The transient heat conduction in the chip, interconnect and the card is governed by:

$$\partial T/\partial t = \alpha(\nabla^2 T) + S^r \qquad [1]$$

The density, specific heat and the thermal conductivity are assigned to the separate blocks in the model. The different properties are listed in Table 1. Individual density and specific heat should be inputted so that the product of these gives the correct thermal diffusivity along with the correct conductivity.

Surface Radiation Modelling

The air is assumed to be non-participating in radiation, and both the surfaces of the card as well as the cover plate are assumed to be gray and diffuse. The card surfaces not in contact with the top or bottom thermode are allowed to have radiation exchange with the casing of the bonder, environment and the thermode vertical surfaces. This forms a 4-surface gray-body exchange problem with radiation loss from the card given by [14, 15]:

$$q^r = \sum F_{s-i}(J_s - J_i) \text{ summed over i} \qquad [2]$$

where i denotes the surfaces other than the card and s refers to the card surface. The shape factors F were determined by double integration on the subsurfaces using a FORTRAN program. The description of this program is beyond the scope of this paper. Each surface of the card was subdivided into four parts and equation (2) was applied to each part separately.

The source term in equation (1) is then $S^r = q^r/s$ where s is the thickness of the control volume perpendicular to the radiating surface. The radiation source term is applied only to the cells adjacent to the solid surface. The value of T_i is assumed to be 298 K for the casing and environment and the thermode temperature for the thermode surfaces.

Since the heater surfaces and the casing have a relatively high emissivity (> 0.7) and the shape factor for card surface to thermode is very small, equation (2) reduces to the following as a first order approximation:

$$q^r = \sigma\epsilon(T_s^4 - T_i^4) \qquad [3]$$

In trial runs it was found that the application of equation (3) instead of equation (2) changed the temperature predictions by less than 5 percent, however it was computationally more efficient (about 25 percent faster) to use equation (3).

Modelling of the bumps

The different materials are modeled as solid blocks. However, there are too many bumps to model each one separately and yet be computationally efficient. To simplify the situation, the connections are handled by using blocks with the effective thermal property and thickness such that both the perpendicular and parallel resistances of the interconnect layer are accounted for. This allows modeling of anisotropic properties in the interconnect layers using isotropic property blocks. The details are found in [16].

The properties and thickness of the block to be used in the model is computed as:

$$k_{eff} = 1/[(R_\perp R_\parallel)^{1/2} w] \qquad [4]$$
$$t_{eff} = w(R_\perp/R_\parallel)^{1/2} \qquad [5]$$

Using this technique, it is not necessary to model individual balls but an effective layer can be used which accurately describes the transport in all three dimensions, without using a prohibitively large grid size. The density of this block layer is adjusted to keep the same thermal mass (ρVC_p) as all the bumps and the

encapsulant. In trial runs it was found that property changes in the bump layer by an order of magnitude had a negligible effect on the overall temperature predictions, indicating the small bump layer thermal resistance and thermal mass compared to other components of the system modelled. To speed convergence in subsequent runs, the bump layer was ignored completely.

Thermal Radiation Measurements

The total hemispherical emissivity of the card surface was measured by comparing radiation from these surfaces with that from a gray, diffuse surface of known temperature and emissivity using a radiometer (model 600) by Inframetrics Inc. with an imaging system by Thermoteknix Ltd. The card emissivities were measured and found to be in the range of 0.8 to 0.9 and an average value of 0.85 was used. Changing the card emissivities in the model from 0.8 to 0.9 changed the junction temperature rise above ambient no more than 2 percent in the worst case.

CONVECTIVE BOUNDARY CONDITIONS

The convective coefficients for the card top and bottom surfaces were initially estimated from the following correlations:

$h = 0.54(k/L)(Ra)^{0.25}$ Upper heated surface [6]
$h = 0.27(k/L)(Ra)^{0.25}$ Lower heated surface [7]

Strictly speaking, the above correlations are for steady state conditions with Ra as a function of the surface temperature. The Rayleigh number was estimated based on an average card temperature. The above were iteratively used at each time step by applying the boundary conditions in a pseudo-steady fashion. The computations were performed using the finite-difference control volume method in the package FLOTHERM (trademark of FLOMERICS Inc.) and hence the coefficients had to be input manually at the end of each time step. To reduce computational time, sensitivity runs were later performed by using constant convection coefficients at all time steps in a range bounded by surface temperature between 250 C and 25 C. The solution changed by less than 3 percent in the two extremes. This indicates the dominant heat loss mechanism to be radiation heat transfer. A constant h was thus used for all subsequent runs to significantly reduce the computational time for the "what if" parametric runs. Exponentially spaced grids were used to ensure adequate grid density inside and near the chip and the monitor points 1 to 5. The spatial and temporal grids were doubled and the results were compared for the different grids. Finally a grid of 50x25x10 with a time step of 5 s was used as a compromise between accuracy and speed, and this grid size is estimated to be less than 2 percent off from the finest grid tested on doubling.

THERMODE BOUNDARY CONDITIONS

The actual thermode temperatures were fitted within an accuracy of 5 percent with the following fit for modeling purposes:

$T(\text{thermode}) = a + bt$, t = time in seconds [8]

Table 2. Coefficients in equation [8]

	Top		Bottom	
t (s)	a(K)	b (K/s)	a(K)	b(K/s)
0-50	35	2.32	35	1.7
50-90	35	2.32	122	0
90-170	245	0	122	0
170-250	497	-1.50	162	-0.23
250-350	240	-0.45	162	-0.23

The top thermode conditions were applied on the chip and the bottom conditions were applied on the heater surface outlined in Fig. 2.

MODEL VERIFICATION

The comparison of the experimentally measured temperatures and the numerically predicted ones are shown in Fig. 4 for the card with two power planes.

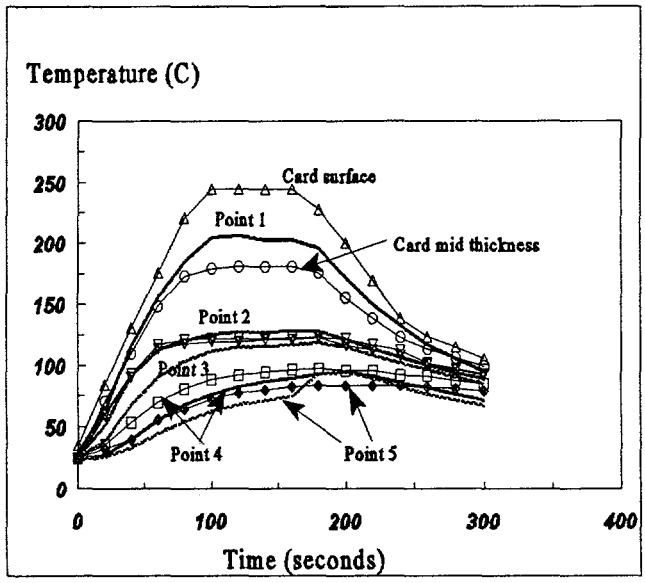

Fig. 4 Comparison of the experimental and predicted temperatures during the bond cycle. The locations of the points are shown in Fig. 2.

The solid lines denote the measurements and the symbols denote computations. Note that the measurements points 2, 3, 4 and 5 are on the top sub-surface (flush) of the card away from the chip, while point 1 is under the chip. Point 1 measurement lies between the prediction at the card surface and that at the midpoint of the card thickness. Due to the very sharp gradient in the z direction

in this region, it was difficult to monitor the point in the model that corresponded exactly to the thermocouple bead embedded below the chip. The sharp gradient (240 C to 180 C in a distance of 0.5 mm) indicates that the top thermode primarily affects the bump temperatures and the bottom heater has a minimal effect. This information was key in developing a successful bond process where the heat is delivered through the chip by controlling the top temperatures. Hence, one process control variable, namely the bottom heater temperature was eliminated. Points 2, 3 on the card surface agree very well (within a 7 percent) for t > 100s. The maximum discrepancy is for point 3 at around 50 s of the order of 12 percent. Point 4 and 5 agree very well (within a 15 percent) over the whole time range studied. It is estimated that the sudden change in slope for point 5 at around 160 s could be a combination of hot spots caused in the actual set-up due to strong convective cells [17] arising from a horizontal heated surface. These convective cells and the resulting hot spots were not accounted for in the conduction model. A conjugate heat transfer/fluid dynamics model is required to solve for the convective flow.

The results indicate that the model accurately predicts the temperatures in the chip and bump vicinity, thereby enabling the use of modeling to study different bonding parameters such as ramp rates, dwell time, card thicknesses, heater sizes etc. to optimize the bonding process. Some of the parameters are explored in another study to understand the bonding process in more detail.

TEMPERATURE PROFILES

Figs. 5 (a) and (b) show the temperature contours on the surface of the card (z = 1.6 mm, see Table 1 for thicknesses) at t = 50 s and t = 90 s, respectively. The contours are not symmetric because the chip and the heater are not symmetric with respect to the card centerlines. There is a relatively sharp gradient around the periphery of the chip, while the chip is isothermal. This shows the dominance of the chip heating on the bump temperatures, a key to achieving successful bonding. The remaining of the heater area is again relatively isothermal, with steeper gradients outside the back-side heater area. The figure shows the heat wave propagation away form the heater from 50 to 90s.

Shown in Fig. 6 are the temperature profiles across the card under the chip. Z =0 corresponds to the back-side of the card in contact with the heater. The top surface corresponds to z = 1.6 mm and the top of the chip is at z = 2.35 mm. It is clear that at the end of the ramp up and dwell, the major gradient is between z = 1.2 mm to z = 1.6 mm, showing clearly again that the bump temperatures are best controlled by heating the chip from the top and not by the heater at the bottom. During initial rampup and the coolodown process, the card shows minimal gradient across the thickness, with temperatures decreasing only slightly (by 20 percent) over 100 seconds.

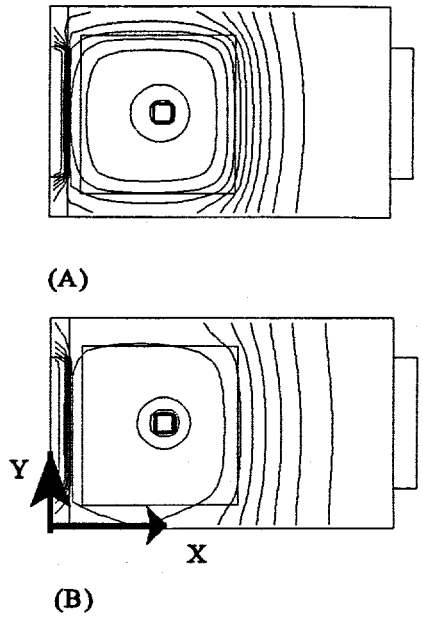

Fig. 5 Temperatures contours on the card top surface (z = 1.6 mm); (a) t = 50 s, 15 equispaced contour lines from 25 C to 143 C; (b) t = 90 s, 15 equispaced contour lines from 25 C to 222 C.

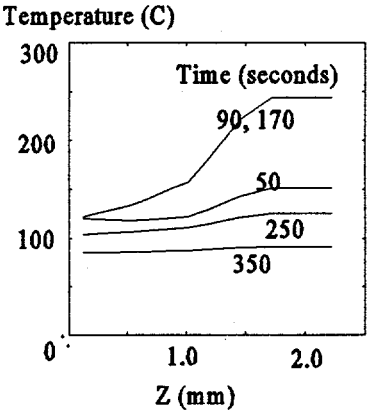

Fig. 6 Temperature profiles at different times across the card and chip at the geometric center of the chip.

CONCLUSIONS

A detailed, three-dimensional transient thermal model has been developed for an ECA/FCA bond process. The model is developed using a finite volume technique solving for the conduction field in the chip, adhesive and the card. Radiation effects are accounted for assuming gray body exchange.

Convection coefficients for the card surfaces were estimated from known correlations eq (6,7). The thermode thermal boundary conditions were determined experimentally for both the heating as well as the cooling phases of the transient.

Agreement between the model predictions and measured temperatures at five distinct locations in the assembly is found to be within 15 percent. The model successfully predicts all relevent temperatures and trends during the entire bonding process. It shows that radiation heat transfer dominates over convective loss. The model also reveals that the heat that is required to bond the thermoplastic bumps of a chip to a laminate carrier can be delivered primarily by the top thermode that places the chip. The heated area of the laminate is confined to the chip site and the depth to about half the card thickness. This very small, local heating supports the idea of a very rapid bond cycle of less than 30 seconds. Also, this controlled local heating avoids in-plane thermal gradients on the card, preventing laminate warpage of the card in the bump vicinity. This model can be used to design a chip bonder for rapid and optimized bonding.

ACKNOWLEDGEMENTS

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Encapsulation Process

Objective

Select a commercially available flip chip encapsulant (a.k.a. underfill), and establish encapsulation process that provides acceptable interconnect reliability to be used with polymer metal composite (PMC) joints.

Background

Silica filled epoxy encapsulants are used extensively in solder flip chip devices to improve the fatigue life of the solder interconnects. The high modulus (> 9 GPA) and low CTE (< 40 ppm/°C) of the encapsulant relieves the stresses on the solder interconnects, and all thermal stresses arising from CTE mismatch between the chip and the laminate are carried by the encapsulant. A similar fatigue life enhancement is anticipated for PMC joints with the use of commercial encapsulants.

In the selection of encapsulation material and process, several commercial materials were benchmarked for flow characteristics, flow time, fillet formation, voiding, and reliability performance. Most of the early work was done using 9.4mm soldered chips (PMC chips were not available until 1996) on test boards (described in Test Vehicle Design and Fabrication report of 10/95). Dexter 4511 (4511) and Matsushita CV5183S (MAT) were identified as two leading candidates. Detailed results of these early tests are included in the 1995 annual report.

Encapsulation of PMC bumped chips (Paste A)

PMC chips were available and assembled in early 1996. Electrically good joints were obtained with PMC (paste A) bumped chips, assembled to cards. When these chips were encapsulated with 4511, the PMC joints were electrically opened. The cross section of the failed joints revealed separation between the PMC joint and the pads on the card, and occasionally PMC joints separated from the chip surface. Figure 1 and Figure 2 show the cross sections of failed PMC joints after encapsulation.

It was thought that the low CTE of 4511 relative to the PMC material created z-axis tensile stresses upon cool down, resulting in the PMC joint separation and electrical opens. Subsequent work did not support this theory. A simple analytical model was constructed which showed that even with a CTE difference of 75 ppm between the PMC and the encapsulant, the normal stress applied to the bumps would not be large enough (less than 50 psi) to cause the fails. An experiment was also run whereby chips were bonded to glass slides and encapsulated with five different encapsulants covering a wide CTE range. Each encapsulant regardless of the CTE, wicked into the interface between the bumps and the glass slide producing damage. Figure 3 shows representative encapsulant (4511) wicking under the bump. The damage, of course, occurred while the encapsulant was still in the liquid stage -- long before the CTE differences could be meaningful. It was then believed that fissures and cracks formed during PMC bonding along with the weak interfacial strength of the PMC gives rise to encapsulant wicking and makes it very difficult to achieve consistently good joints. The weak interfacial strength even if it doesn't lead to encapsulant wicking, gives rise to an adhesive failure mode which opens the door to a defect-driven catastrophic failure of the PMC joints. Increasing the adhesion strength of the material in order to promote a more robust cohesive failure mode was therefore desired.

Encapsulation of PMC bumped chips (Paste C)

The need for improved (high) adhesive strength was addressed by the modified version of the PMC, Paste C, developed by IBM Yorktown. This new PMC formulation resulted in higher failure stresses and a highly desired "cohesive" failure mode discussed in the Bonding section. When the chips photobumped with Paste C were bonded to glass and encapsulated with various encapsulants, no wicking of the encapsulants was observed (Figure 4). A group of cards was then assembled with Paste C bumped chips, encapsulated, and put on the reliability stress tests. No electrical failures occurred in 1200 thermal cycles (-55 to 125°C), 1200+ hours of 85°C/85% RH, and thermal age at 125°C. Thus, the modified PMC formulation marked a significant advancement in forming reliable PMC interconnects.

Encapsulation Effect on Contact Resistance of PMC Joints

A detailed analysis of the contact resistance (CR) data of PMC joints revealed a 5-20% increase in CR after encapsulation (50-100 mΩ increase over a 600 to 800 mΩ reading of a stitched net). Once increased, the CR values remained constant through reliability stress tests. Such a CR increase is not observed for solder joints after encapsulation. Actually, a 5-10 mΩ increase in CR for a solder joint occurs after a complete fracture crack has formed.

Regardless of initial joint quality, time-zero contact resistance, or encapsulant, the contact resistance of almost every circuit increased during the encapsulation process. Hysol 4511 and Hysol 4526 gave increases averaging 100 mΩ or more. Matsushita and a proprietary encapsulant formulation (RECAP) performed better, but still produced increases up to 50 mΩ. Figure 5 shows a comparison among the four encapsulants. The percent change in contact resistance after encapsulation is based on a typical time-zero (pre-encapsulation) resistance of stitched chips.

An experiment was performed which monitored the contact resistance at regular intervals during the entire encapsulation process. A previously encapsulated reference card was run along side the test card so that the thermal coefficient of resistance for each net could be determined. Once these were found, the resistance increases due to temperature effects were normalized out, and increases due only to encapsulation problems were found. 85% to 100% of the resistance increase occurred within the first 5 to 10 minutes of encapsulant cure. Minimal increases occurred during encapsulant flow under the chip, but the greatest increase within each net occurred almost immediately after the card was placed in the oven to cure. Figures 6, 7, and 8 show changes in normalized resistance which occurred from one reading to the next for encapsulants 4511, 4526 and MAT. As labelled, the peaks occur between the 5 and 10 minute mark. Since 1°C temperature change produces a 5 to 10 mΩ change, experimental error accounts for the noise in the rest of the chart. Each point on these charts is an average of all 32 readings taken on the card.

It was now hypothesized that these CR increases are still caused by the encapsulant wicking under the PMC joint at the perimeter during the encapsulant flow and cure. Although the PMC adhesion to the Au pads was significantly improved in the new paste C formulation, some cracks and fissures formed during bonding act as weak spots for encapsulant wicking. Also, the extent of encapsulant wicking and damage depends on the encapsulant viscosity during cure and the gel time for the material. Higher viscosity of the encapsulant, and shorter gel time, resulted in less wicking and damage by the encapsulant. This hypothesis was validated by the following experiment and optimum encapsulant process parameters were established.

Encapsulant Viscosity and Contact Resistance Increase

Dynamic viscosity of 4511, 4526, MAT, and RECAP were measured through encapsulation flow and cure process, in a Bohlin Rheometer. The encapsulants were heated to the dispense temperature (80°C), and then ramped (at 17 or 25°C/minute) to cure temperature (130 or 150°C). The viscosity of the encapsulants with time is plotted in Figures 9 and 10. At the dispense temperature of 80°C, the encapsulant viscosity is low, and this facilitates rapid flow and complete coverage under the flip chip device. As the encapsulant advances to the cure process at 130 to 150°C, the material viscosity takes a further dip before the gelation of the material. It is during this time when the encapsulant viscosity is at its minimum (before gelation), that the encapsulant wicks in and causes the CR increase. The following table compares the dispense viscosity, the minimum viscosity and the gel time and temperature for the four encapsulants.

Encapsulant	Dispense/Cure Process	Dispense viscosity cps	Min. Viscosity cps	Gelation Time/Temp
Mat. CV5183S	Disp.@80°C; Cure @130°C	8.5	6.8	5 min (90-100°C)
Mat. CV5183S	Disp.@80°C; Cure @150°C	7.9	6.4	4 min (90-100°C)
Dexter FP4511	Disp.@80°C; Cure @130°C	3.3	1.5	5 min (100-110°C)
Dexter FP4511	Disp.@80°C; Cure @150°C	3.5	1.0	4 min (120°C)
Dexter FP4526	Disp.@80°C; Cure @130°C	1.5	0.5	6 min (100-110°C)
Dexter FP4526	Disp.@80°C; Cure @150°C	1.7	0.5	4 min (120°C)

The encapsulant wicking and the CR increase are inversely related to the viscosity and gel time of the material. Hysol 4526 which dips the most in viscosity and has the longest time to gel (6 minutes), causes the most increase in the CR of PMC joints. Matsushita encapsulant with higher dispense viscosity (at 80°C) over most encapsulants resulted in a void free encapsulation in 2 minutes or less for the 9.4 mm test chips. A rapid cure at 150°C, higher viscosity, and shorter gel time (4 minutes) for this material resulted in a <5% increase in contact resistance of assembled chips. Dispense at 80°C and 1 hour cure at 150°C are the optimum process conditions identified for PMC encapsulation.

Summary of Encapsulation Process Development

- Encapsulation is identified as the most critical process for electrical stability and reliability stress performance of PMC joints.
- Strong adhesion of PMC to pads on the board is required to prevent encapsulant wicking and damage to the PMC interconnects. This is achieved by PMSP, paste C formulation, and bonding process optimization.
- Matsushita CV5183S (MAT) and Dexter 4511 (4511) encapsulants are used to achieve good reliability performance of PMC joints, with MAT being more effective.
- Encapsulation flow times of <2 minutes, with no voids are achieved at bondline of 0.0025"±0.0002".
- Rapid cure at 150°C, higher viscosity, and shorter gel time (4 minutes) of encapsulant resulted in a <5% increase in contact resistance of assembled chips.
- Dispense at 80°C and 1 hour cure at 150°C are identified as optimum process conditions for PMC encapsulation (with MAT and 4511).

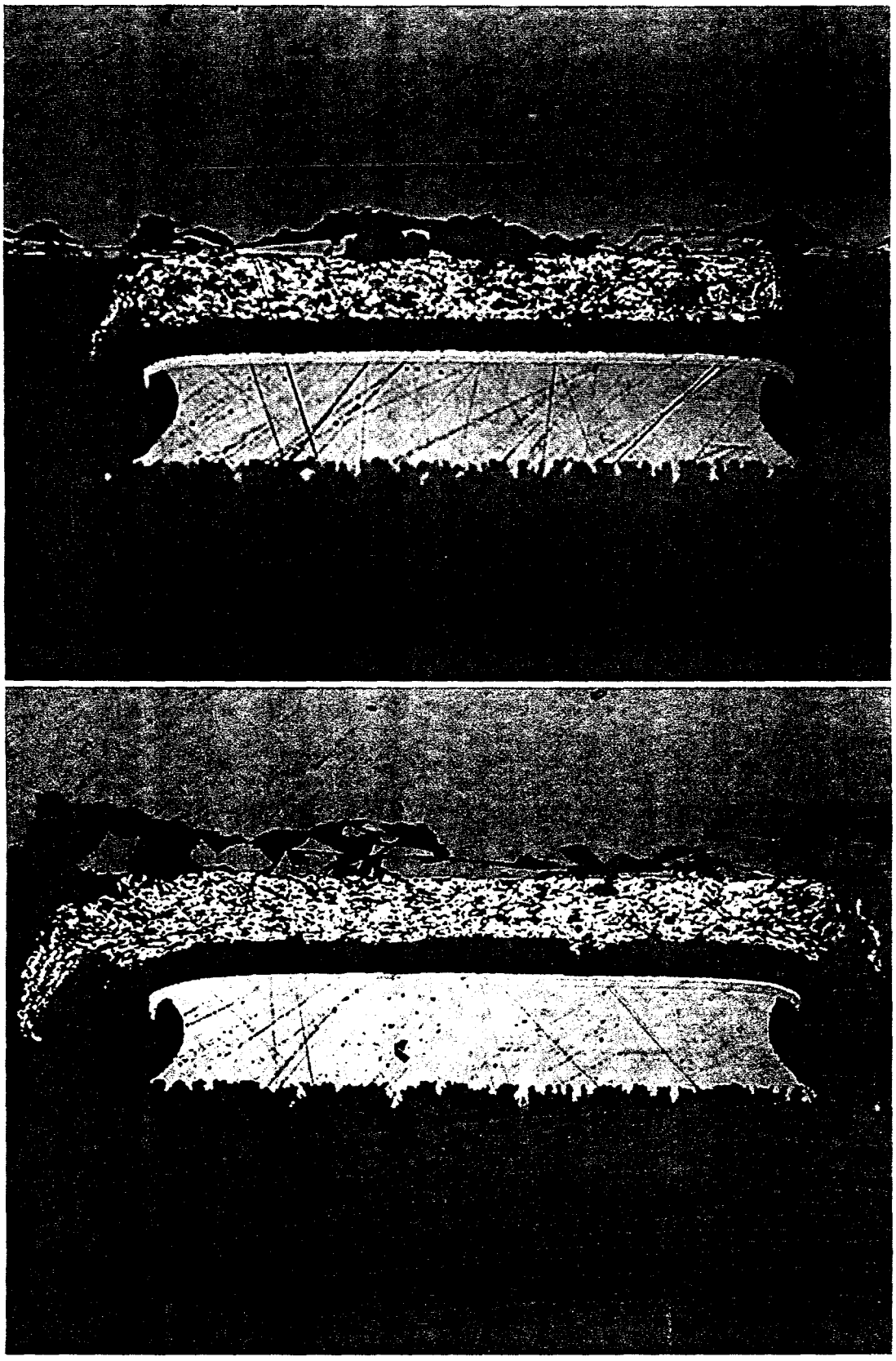

Figure 1: Cross section of PMC joints (hand-dispensed, paste A) after encapsulation. The PMC joints between the chip and the pad on the card failed adhesively after encapsulation.

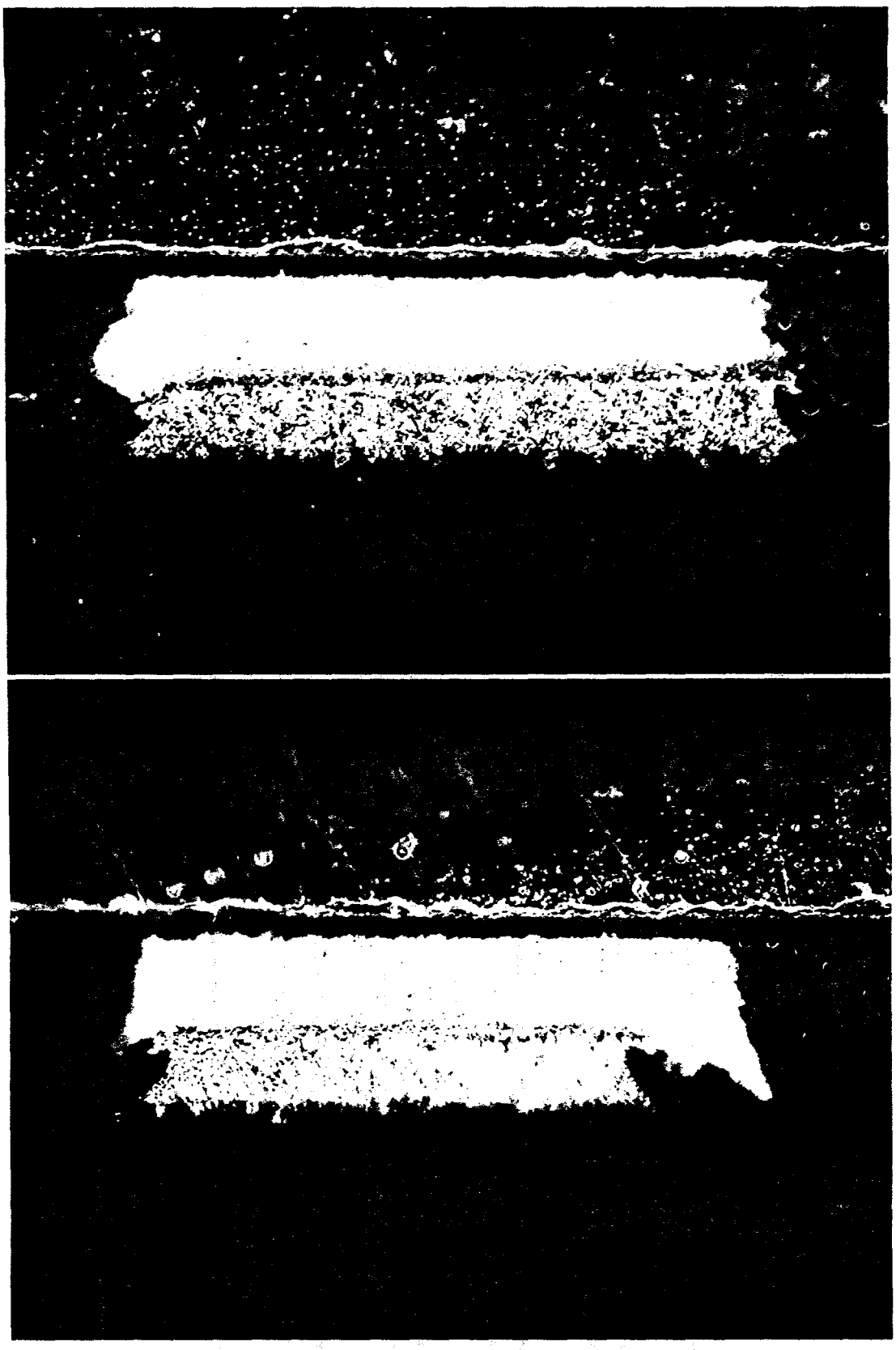

Figure 2: Cross section of photobumped PMC joints (paste A) after encapsulation. The PMC joints between the chip and the pad on the card failed adhesively after encapsulation.

PASTE "A"

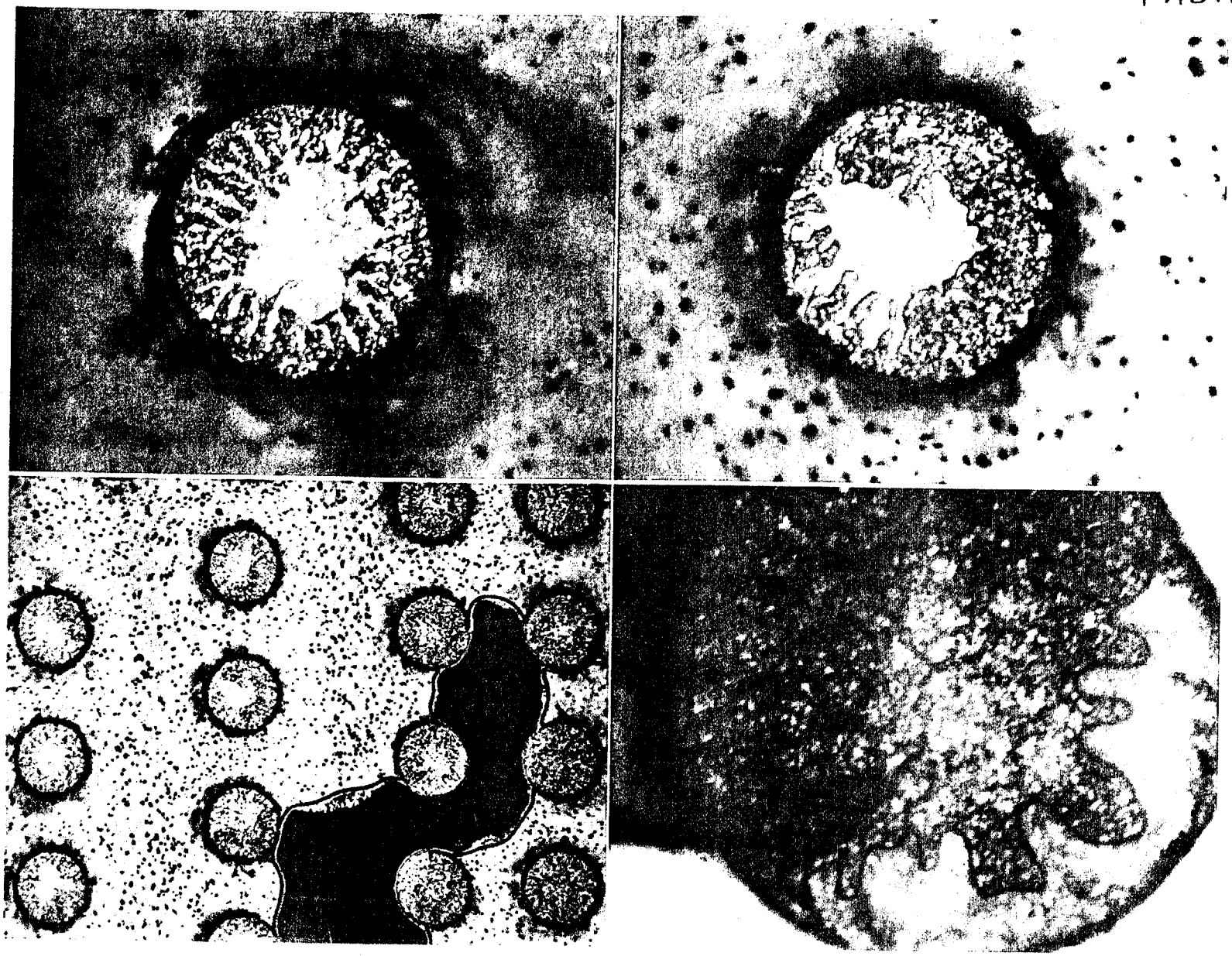

Figure 3: Extensive encapsulant wicking under the PMC joints (paste A). Photobumped chip bonded to glass substrate, and encapsulated with 4511. Fissures and cracks in the bonded joints alongwith the weak interfacial adhesion of the PMC resulted in encapsulant wicking.

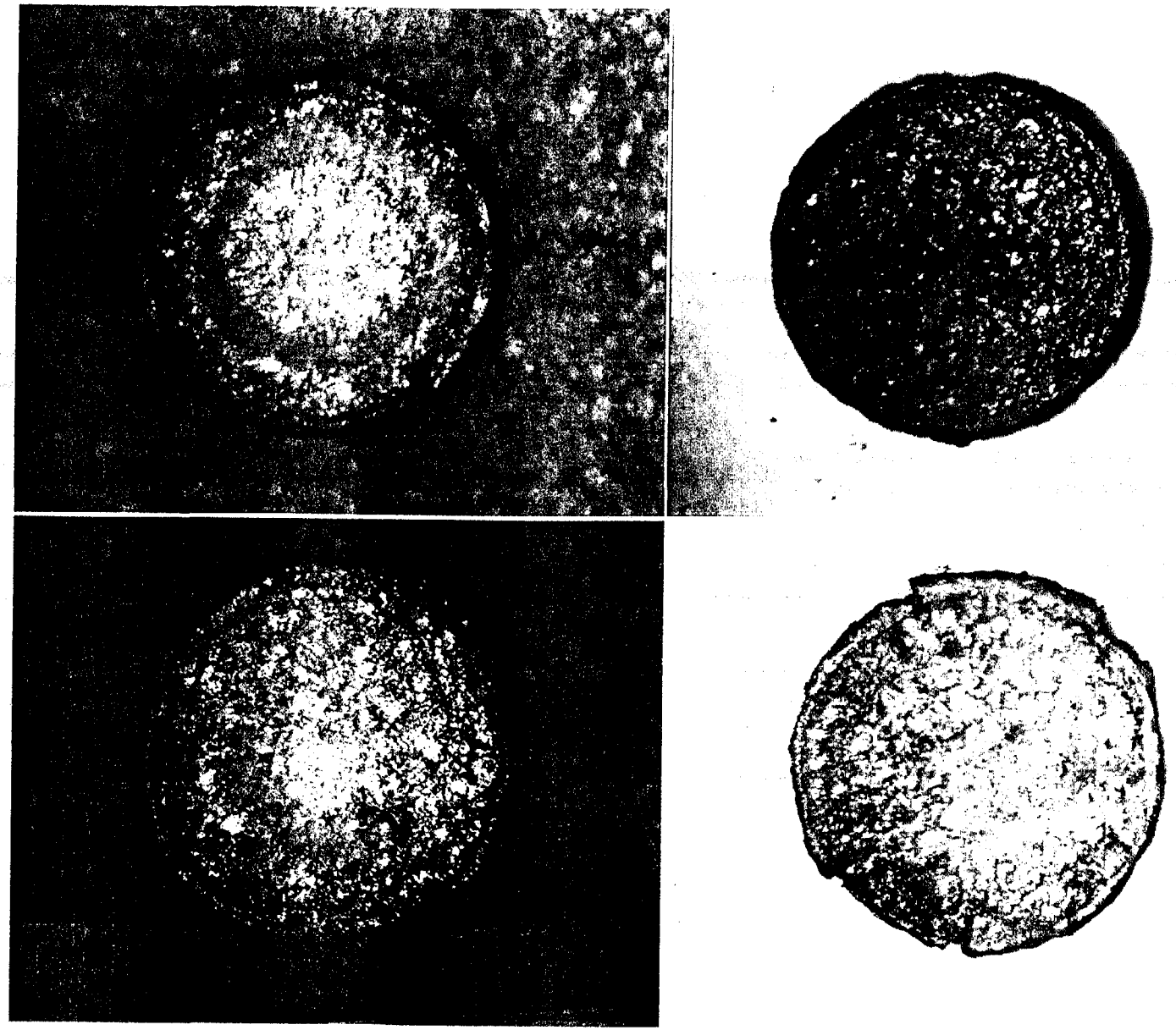

Figure 4: Low to no encapsulant wicking under PMC joints (paste C). Improved PMC adhesion of the new PMSP formulation, prevented encapsulant wicking. Images on the right are PMC joints before encapsulation and the ones on left are joints after encapsulation with 4511 and 4526.

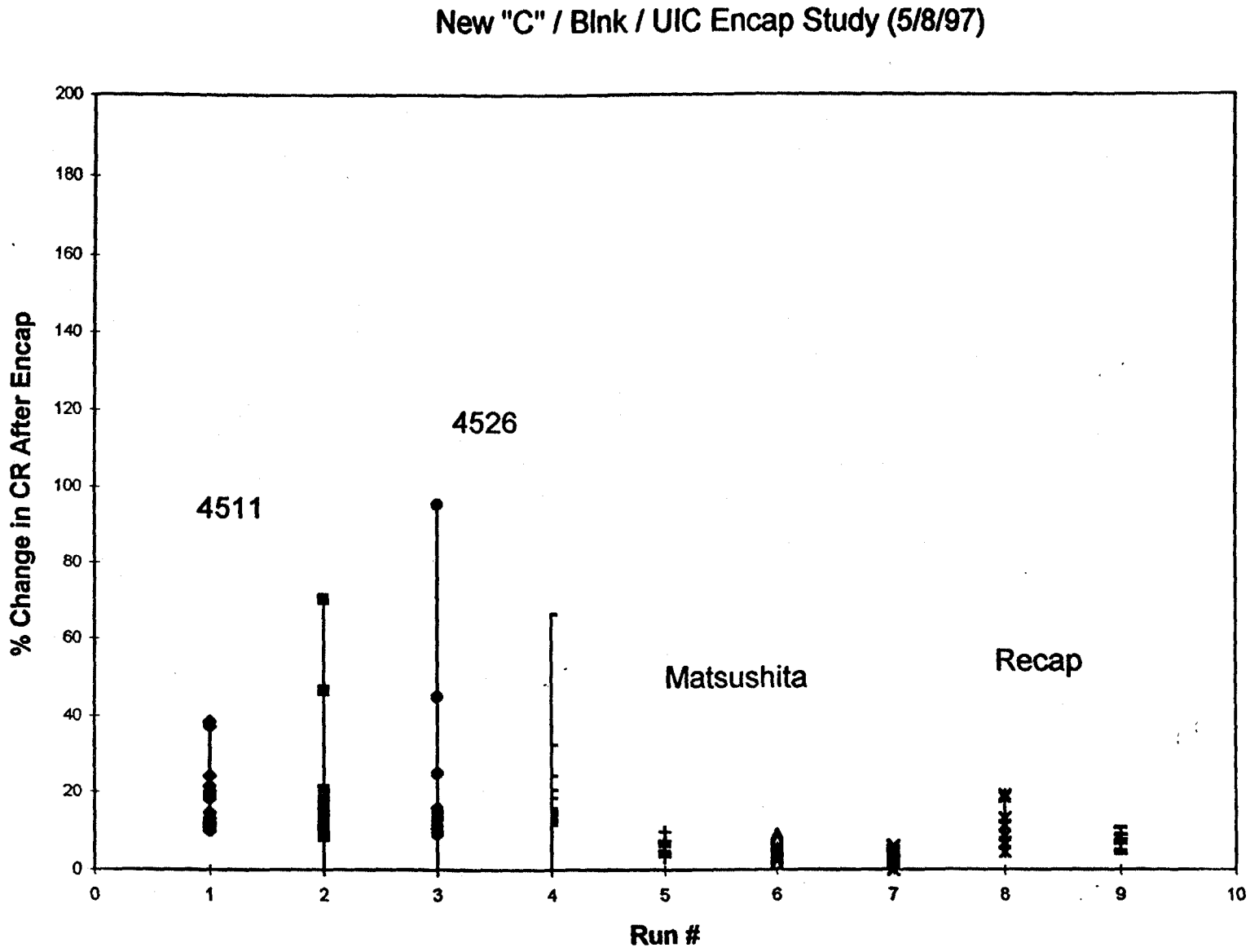

Figure 5: Increase (% change) in contact resistance of PMC joints (paste C) after encapsulation with four representative encapsulants. 4526 and 4511 resulted in a significant change in PMC contact resistance.

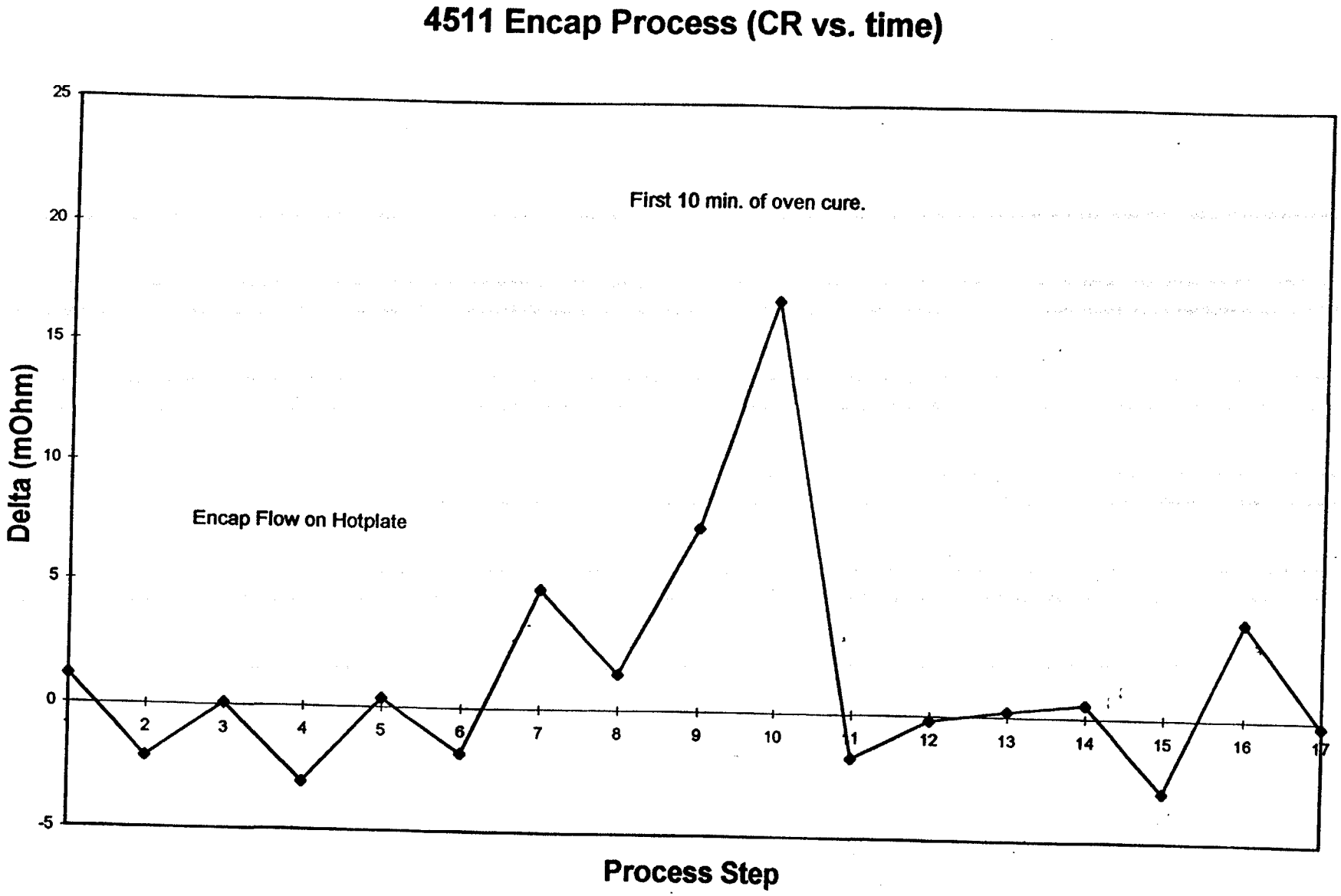

Figure 6: Change in contact resistance of PMC joints through encapsulation (4511) flow and cure. Data is normalized for thermal effects on CR changes during encapsulation. Largest increase in CR occurs during the first 10 minutes of encapsulant cure.

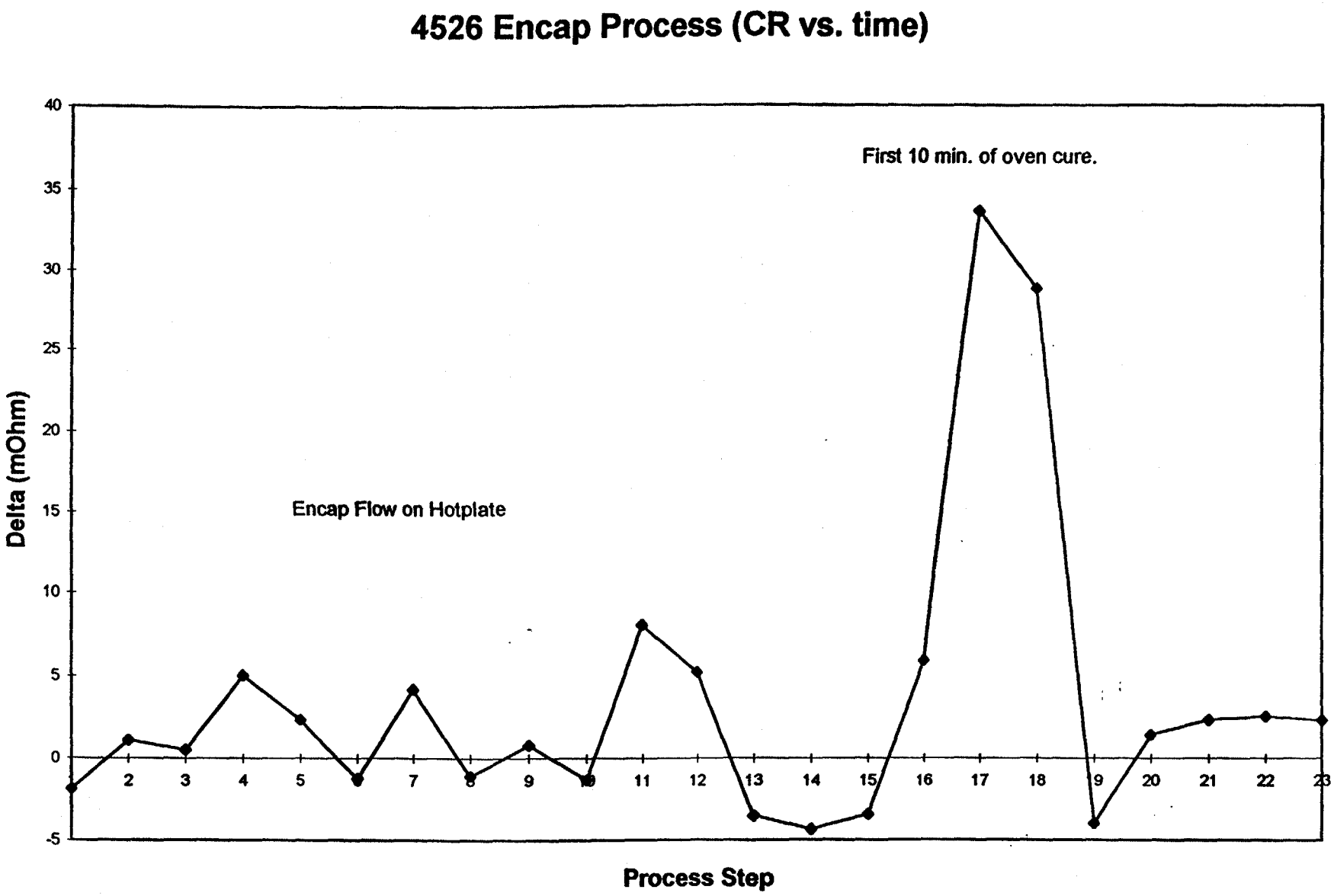

Figure 7: Change in contact resistance of PMC joints through encapsulation (4526) flow and cure. Data is normalized for thermal effects on CR changes during encapsulation. Largest increase in CR occurs during the first 10 minutes of encapsulant cure.

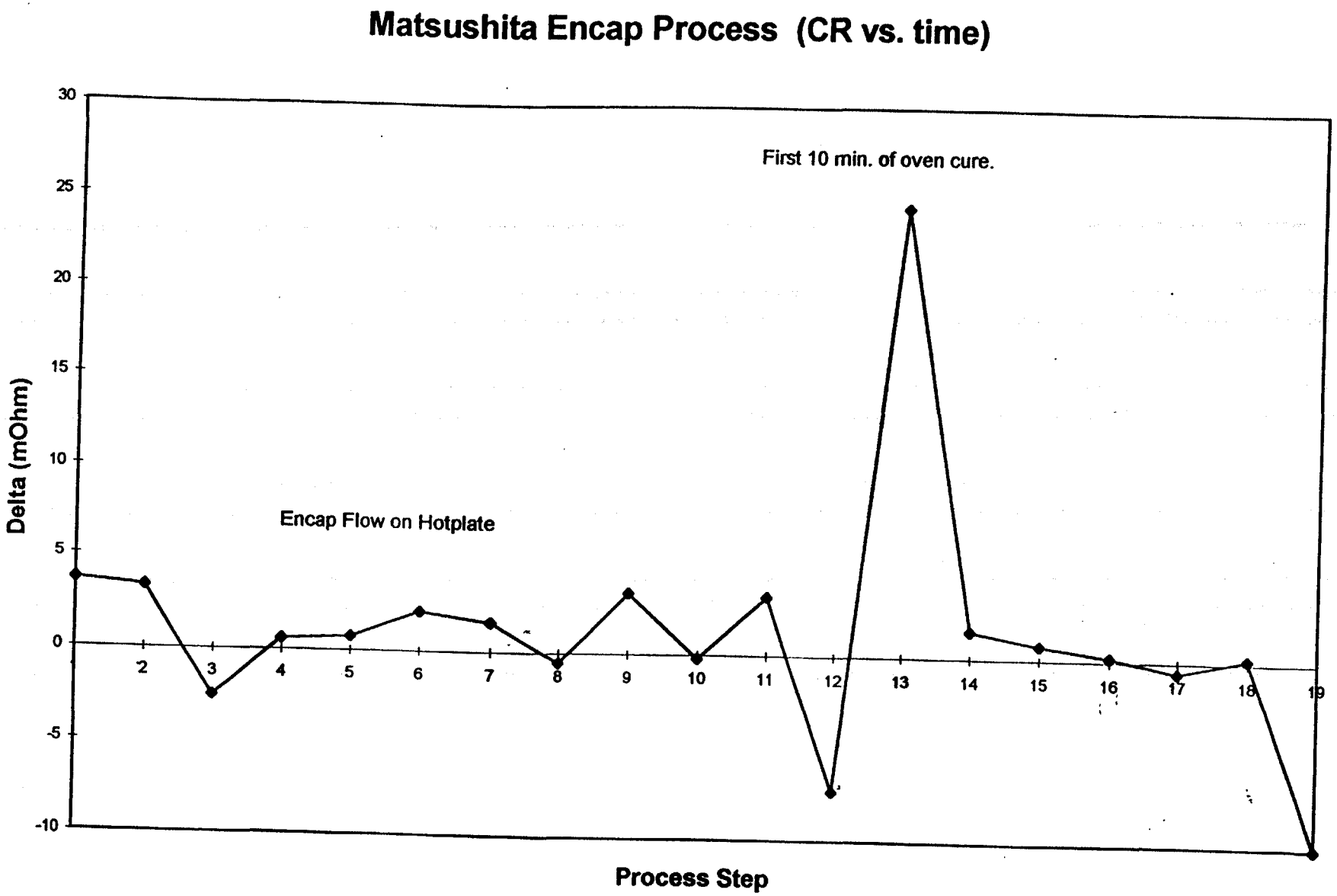

Figure 8: Change in contact resistance of PMC joints through encapsulation (MAT) flow and cure. Data is normalized for thermal effects on CR changes during encapsulation. Largest increase in CR occurs during the first 10 minutes of encapsulant cure.

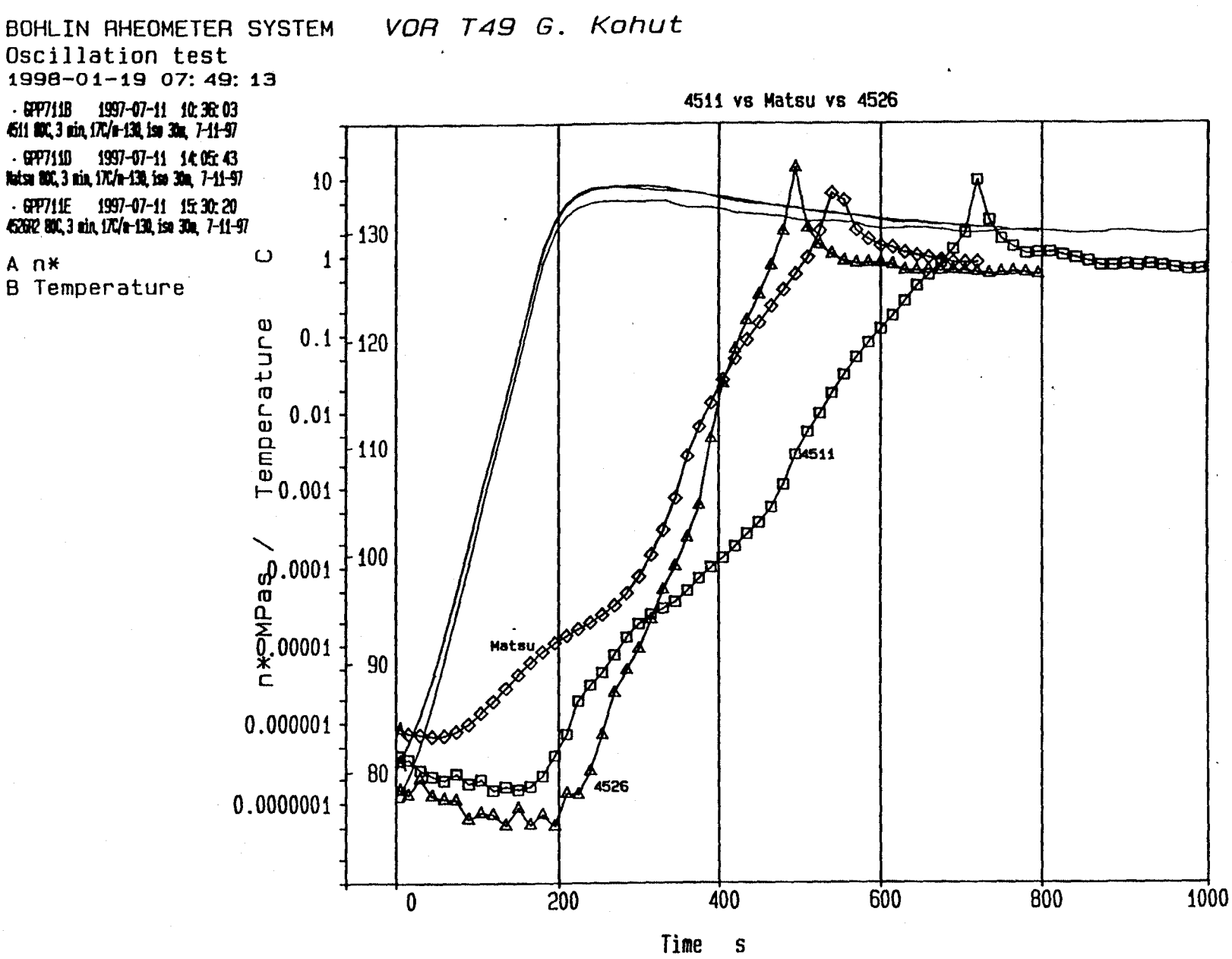

Figure 9: Encapsulant viscosity during cure for MAT, 4511, 4526 and RECAP. Encapsulant at dispense temperature (80°C) is ramped at 17°C to final cure temperature, 130°C. MAT encapsulant with a 5X to 10X larger viscosity than 4511 and 4526, results in the smallest increase in CR.

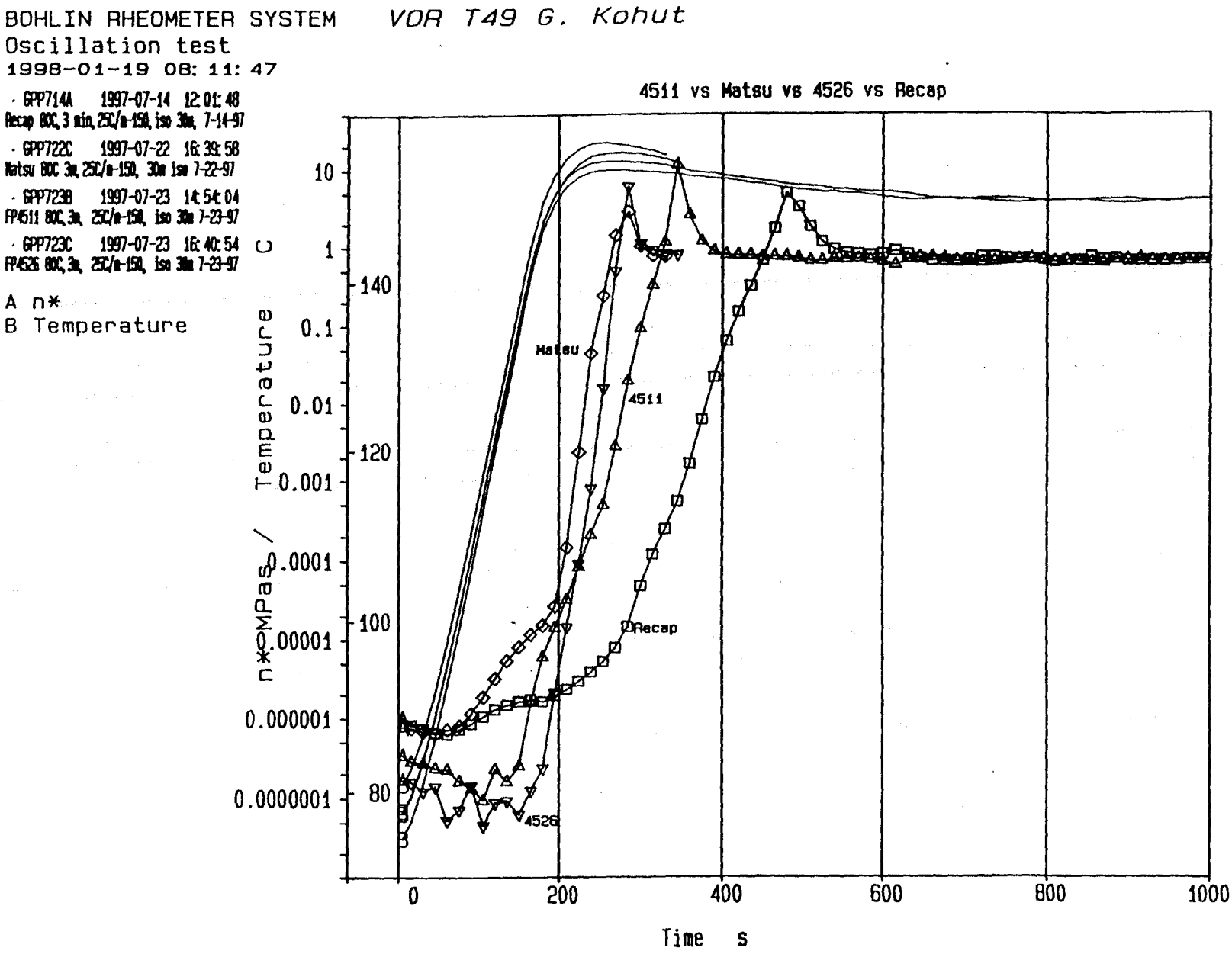

Figure 10: Encapsulant viscosity at improved cure conditions for MAT, 4511, 4526 and RECAP. Encapsulant is dispensed at 80°C, and ramped at 25°C to final cure temperature of 150°C. MAT encapsulant with a 5X to 10X larger viscosity than 4511 and 4526, results in the smallest increase in CR.

PMC Interconnection Stability in Stress Testing

Objective: The first objective in achieving PMC interconnection stability was to select a terminal metallization to be used at both the chip and card level. The approach was to evaluate the initial contact resistance distribution independent of electronic packaging variables such as coefficient of thermal expansion differences or warpage. Contact resistance stability was studied as a function of environmental aging. The second objective of was to demonstrate that the PMC joints between a chip and card laminate can maintain stable contact resistance as a function of exposure to environmental stress. These stresses include accelerated thermal cycle (ATC), thermal age and temperature and humidity (T/H)

Four metal finishes were evaluated for initial contact resistance and contact resistance stability and found to all be acceptable. These are soft gold, hard gold, palladium nickel alloy and palladium. After stress for 1000 hours at 125 C and 85 C/80% RH, contact resistance changes were less than one milliohm. Soft gold was selected as the preferred surface finish because of its general availability in industry. Palladium and palladium nickel as evaporated, were highly stressed and thus prone to delamination from the chip surface.

A total of 10 separate stress tests were completed on chips with PMC bumps that were bonded to a laminate test card. Three types of PMSP were used. PMSP C was selected as the preferred paste because of its higher bond strength and predominantly cohesive fracture mode. The results of the stress tests demonstrate the feasibility of PMC interconnection between chips and laminates. Chips with blanket gold had PMC joints that performed similar to solder interconnects during stress. Chips with stitch patterns showed a general increase in contact resistance in the range of 20 to 40 milliohms. It is hypothesized that this resistance increase is caused by an incompatibility between the photobumping stripper solution and polyimide passivation. Artifacts of the interaction are deposited on the PMC bumps and compromise the interface between PMC and card bond pads. Quartz passivation may be a way to eliminate the contact resistance drift for the stitched chips. Detailed discussion of the test vehicles and stress testing follows.

Copper Comb Pattern Test Vehicle

Effects and variables due to circuit packaging, processing, and materials compatibility were intentionally avoided in the first phase as the main focus was to understand joint resistance behavior as a function of adhesive and substrate finish. After these insights were gained regarding the best adhesive-substrate combination, the next step was to add the effects of circuit packaging. The test conditions, therefore, are not intended to drive failure mechanisms associated with circuit packaging such as residual stresses or coefficient of thermal expansion mismatches. These are intended as environmental stresses that may shed some insights regarding bulk conductivity stability of the adhesives or chemical changes occurring at interfaces. A 0.25 mm thick copper lead frame material was the substrate. Through a photolithographic process, fingers 0.25 mm wide and 9.5 mm long on a pitch of 0.64 mm were defined. Both surfaces of the substrate were etched simultaneously to define the fingers. Eight comb patterns comprised one lead frame strip and were electroplated with the following plating combinations.

1. 1.5 microns of nickel underplate followed by 1.1 microns soft Au
2. 1.5 microns of nickel underplate followed by 1.1 microns hard Au

3. 1.5 microns of nickel underplate followed by 1.5 microns PdNi alloy
4. 1.5 microns of nickel underplate followed by 1.5 microns Pd

In preparation for bonding, comb patterns were ultrasonically cleaned for five minutes in a solution of 70% isopropyl alcohol, 30 % deionized (DI) water that was heated to 40 C. The samples were rinsed with fresh DI water and blown dried with nitrogen. Next adhesive was dispensed on the tips of the fingers by hand with a syringe dispenser, using needles with a 0.25 mm diameter orifice. A second comb pattern with matching metallurgy was aligned to the first on the Research Device's M8, chip bonder and the two were bonded in a stack fashion. Bonding conditions were 230 C, 300 psi for 30 seconds. The top common bar was laser cut without damage to the comb pattern below. Hand probing was used on individual joints to reduce handling damage that was experienced on the first round of tests by using an alignment fixture and a test head that probed all samples simultaneously. Bond thickness were between 0.05 and 0.08 mm. The bond area was typically 0.13 mm^2. Three coupons with forty joints each were made for all four surface finishes with PMC (12 coupons total). The yield after bonding was significantly greater than the first test because the Bonding DOE #1 was used to define the bonding parameters (detailed discussion in the 1995 Annual report). Also, the Research Devices bonder allowed precise control of bond pressure. Notwithstanding these improvements, there were several joints that did not bond well. These were caused by low bond area that resulted from the height variation of hand deposition. Every set of three coupons was subjected to the following three test conditions:

1. 120 C thermal storage for 1000 hours
2. 0 to 100 C thermal cycle (ATC) for 2000 cycles
3. 85 C 80% RH temperature and humidity (T/H) for 1000 hours

Contact resistance results showed very tight initial distribution with standard deviations of between 0.2 and 0.4 milliohms. Figures 1-8 summarize the contact resistance (CR) stability as a function of stress. Figures 1-4 show the mid-test change in contact resistance. Typically the change in CR is less than +/- 0.5 milliohms and in no case does the change exceed one milliohm. Figures 5-8 show the end-of-test change in CR with the same results as mid test. These positive results indicate that any of the four plating finishes tested could be used at the chip or card level. Test chips were built with soft gold, palladium and palladium nickel alloy. Soft gold was selected as the preferred surface finish because it is readily available at a card level in industry. Since it is an electroless plating process, electrical commoning, as required in electroplating is not necessary. Evaporated palladium and palladium-nickel were highly stressed on a wafer and become prone to delamination. After selecting soft gold as the surface finish for both the chip pad and card pad, test wafers and cards were designed and fabricated.

Chip Design

Two, 221 IO (Input/Output) area array chip designs were used: blanket and stitch. Both chips were 9.4mm square in size. The chip design and fabrication was completed at IBM Yorktown's Central Scientific Services Materials Laboratory. These two test chips, when bonded to the card carrier, allowed contact resistance measurements. Chips were fabricated on five inch wafers. Figure 9 depicts the chip footprint which was 0.010 inches in diameter on a 0.020 inch pitch. The

blanket wafers had 200 Angstroms of chromium evaporated as an adhesion layer for the subsequent gold layer that was 2000 to 5000 Angstroms thick. The stitched wafer fabrication process used a single aluminum-copper (AlCu) metallurgy layer to stitch the pads to one another. The AlCu alloy composition was 99.5 wt% Al, the balance Cu. The AlCu pad thickness was two microns. A polyimide passivation layer was then deposited on the wafer, vias were exposed and developed prior to depositing the final pad metallurgy. The polyimide via diameter was 0.007 to 0.008 inches compared to the 0.010 inch terminal pad diameter.

Card Design

The card test vehicle contains two chip sites with a card thickness of 0.062 inches. The card is 4.2 inches X 6.8 inches and contains a gold edge connector for contact resistance measurement. Both chip sites are wired independently and designed so the card can be cut in half and individual chips can be tested and analyzed. The chips and card were designed such that through the stitch pattern there is complete readout of every I/O. Consequently, the I/O in the center of the devices are on a less aggressive pitch than the outer rows of the device. The 10 on 20 test vehicle design gives a total of 16 contact resistance nets per chip site or 32 per card. Figures 10 and 11 illustrate the 10 on 20 card test vehicle. The copper lines and pads in the chip site were required to have a NiAu final metallurgy typical for wirebond chips:100 microinches of Ni and 40 microinches of gold. A high Tg laminate, BT resin, was used for fabricating the test vehicles. The card test vehicle is unique from other flip chip array test vehicles in that the solder mask is removed from the chip sites. Removing the solder mask provided more than 0.001" more gap between the chip bottom side and card surface for underfilling. The function of the solder mask was not needed because the PMC does not wick down the circuit lines as eutectic Sn/Pb does. A total of ten sets of stress tests were completed during the last two years of this three year project. These are summarized in Tables I and II.

Set	Paste	Card	Pitch	Chip	Comments
1	A	2S0P	10/20	blanket	Photobumped, hand dispense
2	A	2S0P	10/20	blanket	Photobumped, supplemental dispense
3	C	2S0P	10/20	blanket	Hand dispense
4	C	2S0P	10/20	blanket	No underfill
5	C	2S0P	10/20	blanket	Photobumped
6	C	2S0P	10/20	blanket	Photobumped, with and without underfill
7	D	2S0P	10/20	blanket	Photobumped
8	D	2S0P	8/20	stitched	Photobumped
9	C	2S0P	8/20	blanket	Photobumped
10	C	2S0P	8/20	blanket, stitched	Photobumped

Table I: Summary of Stress Tests

Set	Paste	Chip SS	fails/nets tested 0 to 100 C	fails/nets tested -55 to 125 C	fails/nets tested 85C/85% RH	fails/nets tested 125 C
1	A	5	7/48, 1000 cycles		15/32, 1000 hours	
2	A	7	14/48, 2000 cycles		3/32, 1220 hours	7/32, 1220 hours
3	C	4	0/32, 4000 cycles		0/16, 2070 hours	0/16, 2000 hours
4	C	1	16/16, 200 cycles			
5	C	12	0/48, 4000 cycles	5/48, 2260 cycles	0/48, 2000 hours	0/48, 2000 hours
6	C	5	30/32, 130 cycles	0/48, 1771 cycles		
7	D	6		0/32, 1000 cycles	0/32, 1000 hours	0/32, 1000 hours
8	D	6	2/32, 5260 cycles	3/32, 2730 cycles	10/32, 1976 hours	0/32, 2175 hours
9	C	35	0/112, 7760 cycles	6/145, 1000 cycles	0/124, 1000 hours	0/159, 1100 hours
10	C	10 26	 4/96, 5000 cycles	6/160, 1000 cycles 22/160, 1000 cycles	 2/75, 2200 hours	

Table II: Summary of Stress Results

Sets 1 and 2

PMSP A was used to bond one chip per card. Cards were cut in half in order to facilitate bonding on the Research Devices chip bonder which could not accommodate the full size card. Set one included four cards that were made with photobumped chips (concave surface or King's crown), and one card that was made by hand dispensing deposits (convex surface) on the card. Three cards, including the card with hand dispensed deposits, were placed on thermal cycle testing between 0 and 100 C. Two cards were placed on temperature and humidity test, 85 C/80% RH. Set two had photobumped chips bonded to cards that had hand deposits. These card deposits were intended to fill the concave surface of the chip photobumps. Seven cards were placed on test: three in thermal cycle, two in temperature/humidity and two in temperature age, 125 C. Sixteen nets of two joints per net were electrically measured for every chip. Some prior experiments had resulted in defining an expected contact resistance CR (exp) value for good joints. It was known that several joints had resistances higher than CR (exp) by 2x or more. The joints that showed high resistance increases, typically showed initial contact resistance > CR (exp), suggesting an initial defect or low bond area. Joints near CR (exp) were stable with stress. These data demonstrated that a stable PMC interconnection between a chip and laminate can be achieved. Several opportunities to further improve the contact resistance performance were identified. The gap for underfilling between the chip and laminate carrier was measured to be less

than 0.002". Experience with solder flip chip attach to organic carriers supports a preferred gap between 0.0025" and 0.003". Thinner gaps result in higher stress and even underfilling does not adequately extend fatigue life. By making 0.003" or 0.004" high bumps with 0.003" or 0.004" photoresist and controlling bond pressure, PMC bond heights equivalent to solder would be achievable. A second improvement could be realized by eliminating the concave surface of the photobump. (discussed in detail in paste deposition section, Reference 2nd and 3rd quarterly reports of second year). Finally, a third improvement that was pursued was modifying the PMSP to provide better adhesion: higher fracture strength and more importantly, a cohesive fracture mode.

Set 3

An experimental paste, PMSP B was used for Set 3 and was hand dispensed. Efforts to dispense this material in the photobumping process were unsuccessful because of the solvent interaction with the photoresist. There were four chips in Set 3. No significant contact resistance increases were observed on any interconnections after 4000 cycles of 0 to 100 C on two chips; 2000 hours of 85C/85%RH on one chip and 2000 hours of 125 C thermal age on one chip.

Sets 4, 5, and 6

PMSP C was used to bond blanket chips to the printed circuit cards that were cut in half, as before. The intent of PMSP C was to improve the fracture strength and move the fracture mode from adhesive to cohesive. Both goals were achieved. (see discussion in Bonding Section). Set 4 was one chip only that was not underfilled. As expected, 100% failure occurred within 200 thermal cycles of 0 to 100 C.

Set 5 included 12 chips that were tested and had encouraging results. All resistance measurements were stable at less than five milliohms after 4000 cycles of 0 to 100 C, thermal cycle; 2000 hours of 85C/85% RH and 2000 hours of 125 C thermal age. Five joints on one card increased more than 10 milliohms, however, this chip site was purposely underfilled so that a large void area was created. This result demonstrated that underfilling was required in the central area for PMC interconnects, just as for solder joints. Two chips that had been underfilled correctly, survived 2260 thermal cycles without any contact resistance failures.

Set 6 was comprised of five chips. Two chips were not underfilled and had 94% of interconnects failing after 131 cycles of 0 to 100 C. Three chips were properly underfilled and had all resistance increases less than 10 milliohms except two which were 12 and 23 milliohms after 1800 cycles of -55 to 125 C. Experience with soldered FCA on laminate has shown that interconnects will begin failing as early as 700 cycles of -55 to 125 C. One explanation for the apparent robustness of PMC interconnects versus solder in the -55 to 125 C thermal cycle test is that any tensile strain that the solder joint experiences, accumulates as plastic strain damage and eventually will result in failure. Tensile strain develops in underfilled solder joints as a result of underfill wear out that is manifested by cracks in the fillet. In contrast, PMC joints can withstand very large strains with plastic damage. Elongation to break has been measured at least 50% and greater than 100%.

Sets 7 and 8

A third PMSP formulation, D, was used in Sets 7 and 8. It was expected that PMSP D would have equivalent electrical performance to PMSP C, but better rheology. Set 7 was made with blanket chips and Set 8 was made with stitched chips. Contact resistance results were less robust with PMSP D. Five of 32 interconnections increased more than 10 milliohms after 1000 cycles of -55 to 125 C in Set 7. Contact resistance was stable at less than 10 milliohms after 1000 hours of 85C/85% RH. One joint increased more than 10 milliohms after 1000 hours of 125 C thermal age. Set 8 consisted of eight stitched chips with two each in 0 to 100 C, -55 to 125 C thermal cycle, 85C/85% RH and 125 C thermal age. Contact resistance increases greater than 100 milliohms were observed in all tests except the thermal age. Two increases in each of the thermal cycles tests occurred early at less than 500 cycles. Continued cycling out to 5260 and 2731 cycles, respectively for 0 to 100 and -55 to 125, resulted in no failures. The temperature and humidity cell had 30% of the nets increase more than 100 milliohms after 2000 hours. Although PMSP D results were encouraging, PMSP C appeared to have more robust fracture strength and stress test performance and was thus selected as the preferred paste for the remainder of the project.

Set 9

Set 9 consisted of 18 cards with two chips per card and were bonded using the Universal Instrument development bonder. Blanket chips were used because the stitch chips were not yet available. Four cards were tested in 0 to 100 C, thermal cycle. No stress failures were observed after 7760 cycles (112 nets, two joints per net). All nets were stable at much less than 10 milliohm change throughout stress. One hundred and seven nets changed less than two milliohms.

Five cards with 145 nets were tested in -55 to 125 C thermal cycle. Three cards with 96 nets demonstrated very stable contact resistance with less than five milliohm changes. Two cards experienced four and six resistance changes that exceeded 10 milliohms. Six of the 10 nets increased several hundred milliohms while cycling to 1000 cycles. Four of the 10 nets increased more than 10 milliohms before the first readout at 250 cycles. Sonoscan images taken at T0 showed that one of these cards had 20% underfill delamination, explaining the resistance increases noted. The second card showed no underfill delamination at T0, however, after 1000 cycles, approximately 40% of the underfill interface was delaminated. It is concluded that the underfill delamination is related to the observed contact resistance increases in the -55 to 125 C stress.

Four cards with 124 nets were tested in 85C/85% RH for 1000 hours. Three cards with 96 nets total, showed stable contact resistance at less than 10 milliohms change except four nets that had changes of 11, 12 , 24 and 44 milliohms after 1000 hours. The fourth card showed T0 underfill delamination on one chip site which resulted in all 16 nets exceeding a 10 milliohm change by 1000 hours. The second chip on this card, with 16 nets, showed good underfill interfaces and resulted in contact resistance changes of less than three milliohms during the 1000 hours.

Five cards with a total of 159 nets were subjected to 150 C for 1100 hours. One hundred and fifty seven of these nets were stable at less than 10 milliohms change. Two nets increased 11 and 12 milliohms after 1100 hours.

Set 9 was the first set of cards that was bonded on UIC's bonder. For the first time, both chip sites were bonded on the card and the largest sample size yet was tested. Twenty cards were started to yield the 18 cards and 35 chip sites that were tested. The stress test results are quite encouraging, showing very robust performance in 0 to 100 thermal cycling and 150 C thermal age. The -55 to 125 thermal cycle stress showed the most significant contact resistance fluctuation, but this instability occurred on only two cards out of five and is associated with underfill delamination. The temperature and humidity (T/H) cell showed good stability with the exception of four nets out of 112. From a design perspective, the stress test results demonstrate that stable interconnects can be made from the PMC material. The very few nets that showed increases exceeding 10 milliohms are related to underfill voids and delamination.

Set 10

Set 10 consisted of five cards (Cards 14 - 18) that were built with blanket chips and 13 cards (Cards 1 - 13) that were built with stitched chips, two chips per card. The five cards with blanket chips were stressed at -55 to 125 C. Card 14 had one open at 1000 cycles and two nets at 20 milliohm change. Card 15 was very stable at less than three milliohm change for 32 nets. Card 16 had two fails exceeding 100 milliohms and five readings that exceeded 10 milliohms but were less than 50 milliohms. These increases were evident at the 1000 cycle readout. Card 17 had one open at 1000 cycles with the other 31 nets stable at less than two milliohms change. Card 18 had two fails exceeding 100 milliohms and six nets that exceeded 10 milliohms but were less than 70 milliohms. A total of six fails (CR > 100 milliohms) and 13 unstable nets exist in this group of five cards with ten chips. Sonoscan images at T0 show several small voids (0.005" to 0.020" in diameter) in the underfill for all of these cards.

The stitched chips did not show the underfill voiding that was observed on the blanket chips. The major difference between these two chip sets is that the blanket chip did not have a polyimide passivation layer as the stitched chip did. Six cards with stitched chips were tested in -55 to 125 C. Twenty two nets out of 160 showed increases greater than 100 milliohms. Most of the other nets showed significant increases beyond 10 milliohms, typically on the order of 30 milliohms. This result is poorer than the blanket chip performance. One concern about the stitch chip is the compatibility of the photobumping stripper solution with the polyimide passivation. The blanket chips never used a polyimide passivation and never showed the general trend of increasing contact resistance. The increasing contact resistance of the stitch chips requires further study to understand the chemical compatibility concern between the stripper solution and polyimide. The other stress test results for the stitched chip are more encouraging than the deep thermal cycle test. Three cards were tested out to 5000 cycles of 0 to 100 C. Only four nets out of 96 failed. These nets were all on the same card and two occurred at 500 cycles one at 3000 cycles and the fourth at 5000 cycles. The general population trend of increasing contact resistance was not evident until the 5000 cycle readout when many nets showed a typical increase of 20 to 40 milliohms. Typically, this test runs out to 2000 to 3000 cycles. The typical increase at 4000 cycles was less than 10 milliohms. Three cards were tested out to 2200 hours of 85C/85% RH. Out of 75 nets, two nets exceeded 100 milliohms at 2200 hours. Typically, contact resistance changes were less than 10 milliohms (on 68 nets) throughout the 2200 hours. Five nets had increases of 12 milliohms.

Summary
The harshest stress is the deep thermal cycle test for both the blanket and stitched chips. The performance of the interconnects on the blanket chip is comparable to soldered flip chip on laminate. The performance of the interconnects on the stitch chip is less than interconnects for blanket and solder. It is believed that reaction between the photobumping stripper and the polyimide passivation results in a weak interface between the PMC bump and card metallurgy. Future activity includes analysis of the PMC interconnects that showed increasing contact resistance. In addition to analysis, to further understand the polyimide passivation concern, quartz passivation on stitched chips will be pursued. Analysis of yield loss due to underfill delamination at T0 is important. The results of all of the stress testing demonstrate the design feasibility of PMC interconnects for flip chip attach to laminates.

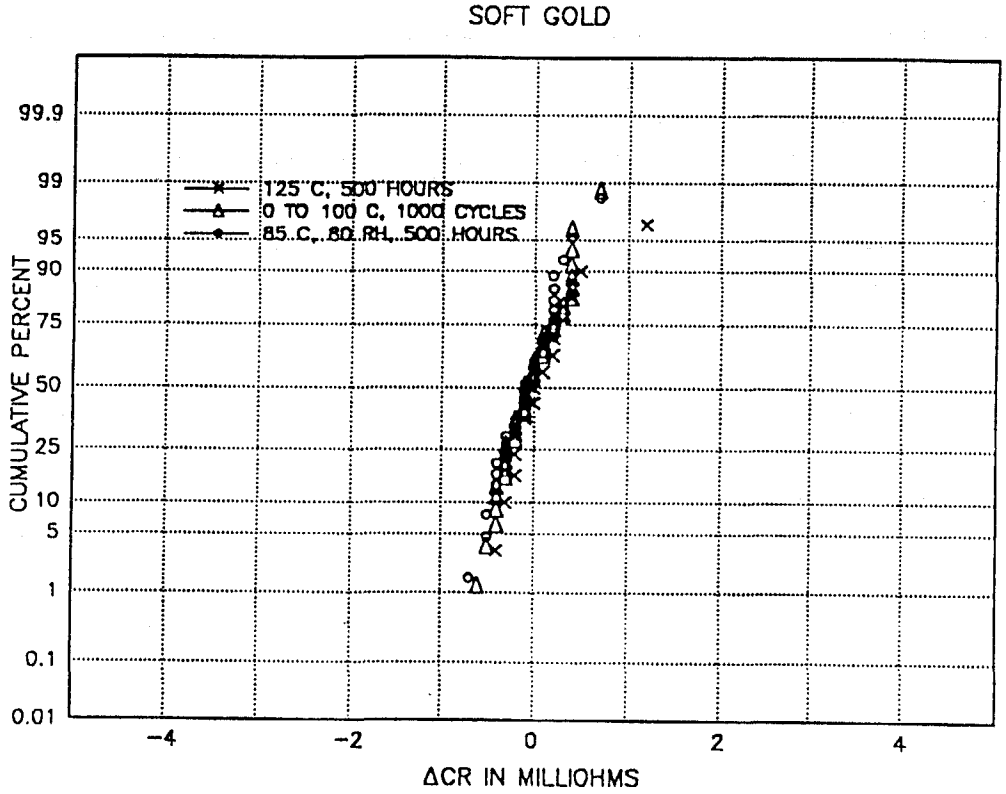

Figure 1. Distribution of changes in contact resistance for soft gold plated copper comb pattern, mid stress readout

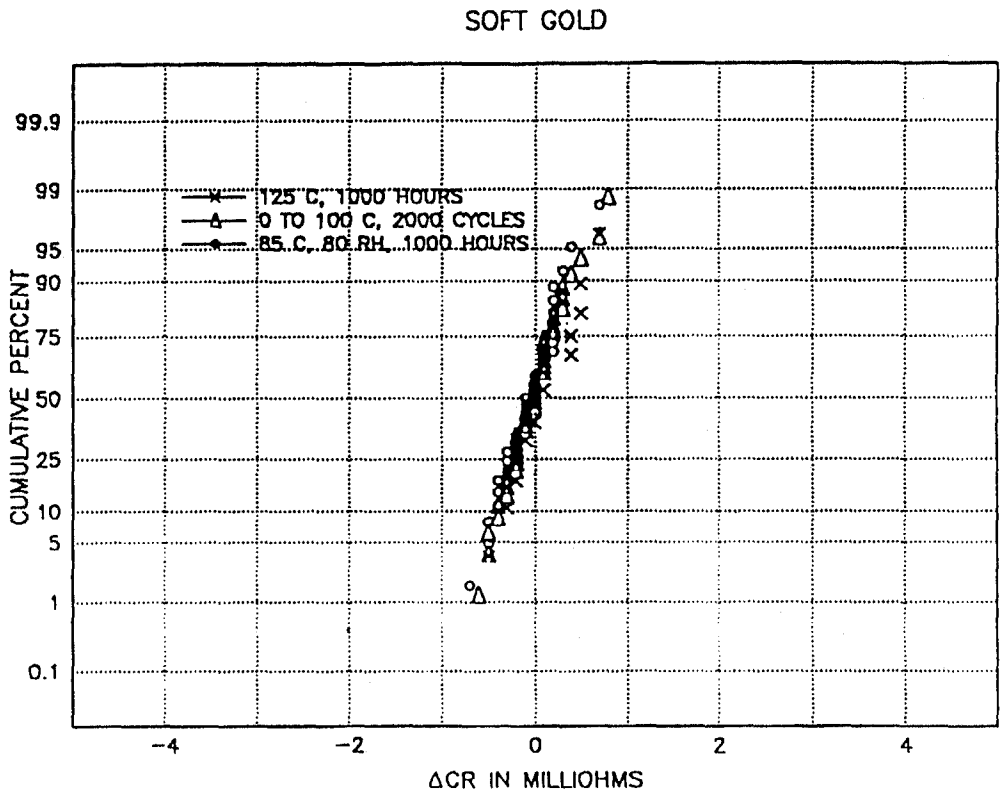

Figure 2. Distribution of changes in contact resistance for soft gold plated copper comb pattern, final stress readout

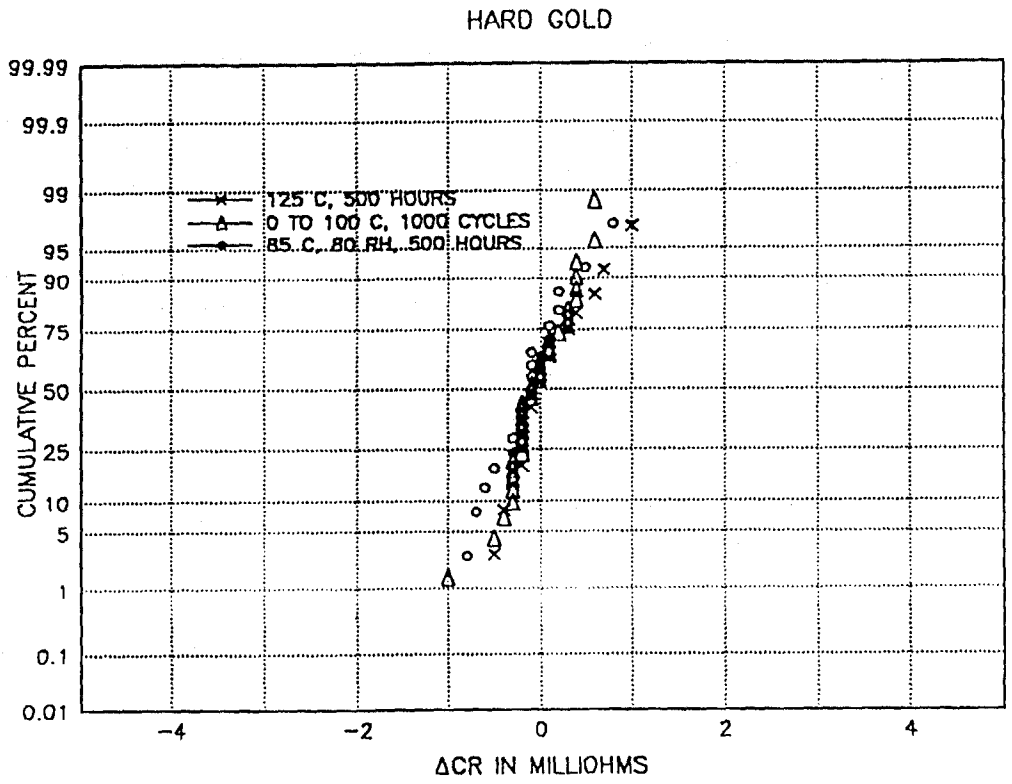

Figure 3. Distribution of changes in contact resistance for hard gold plated copper comb pattern, mid stress readout

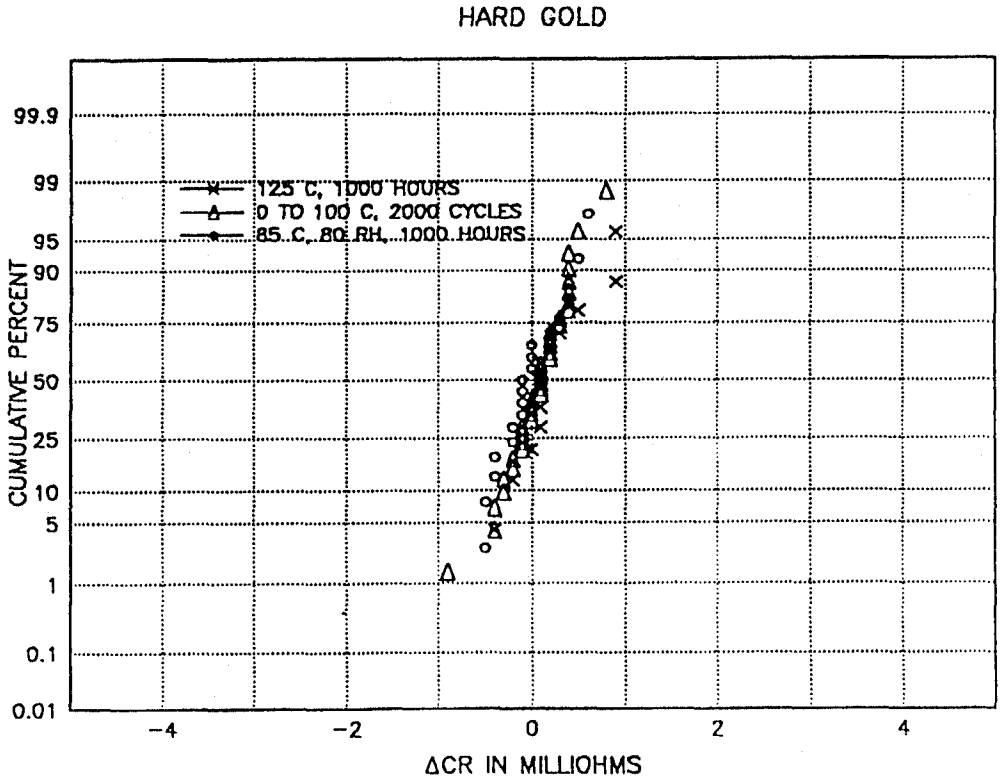

Figure 4. Distribution of changes in contact resistance for hard gold plated copper comb pattern, final stress readout

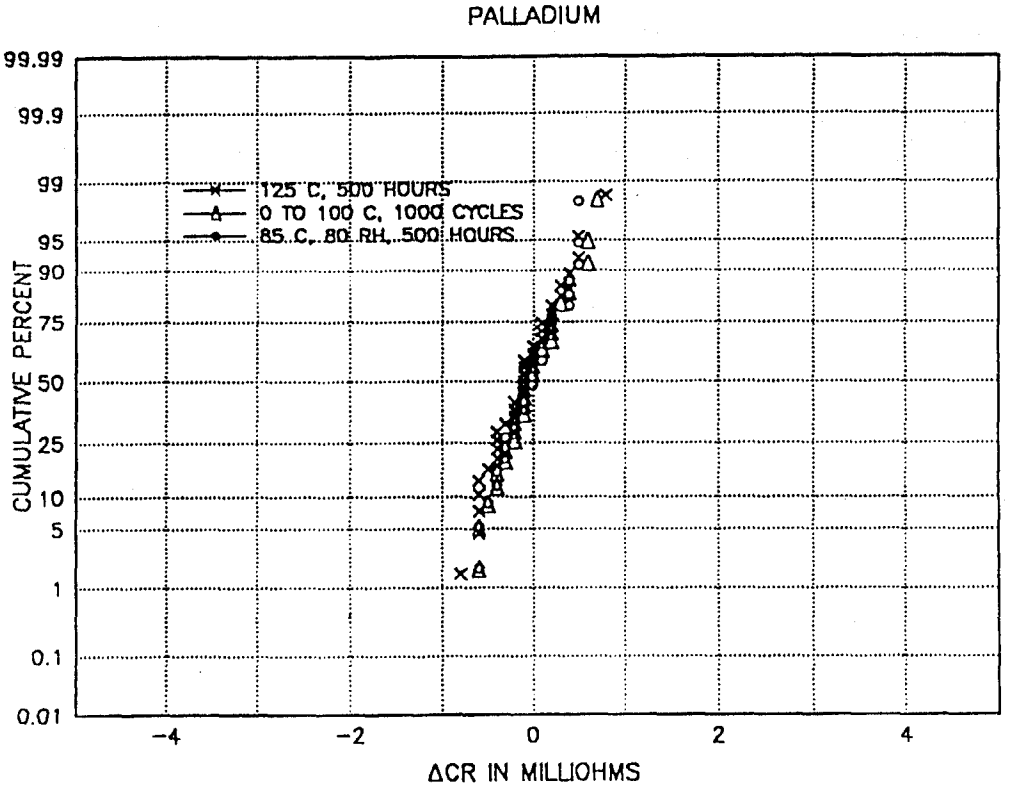

Figure 5. Distribution of changes in contact resistance for palladium plated copper comb pattern, mid stress readout

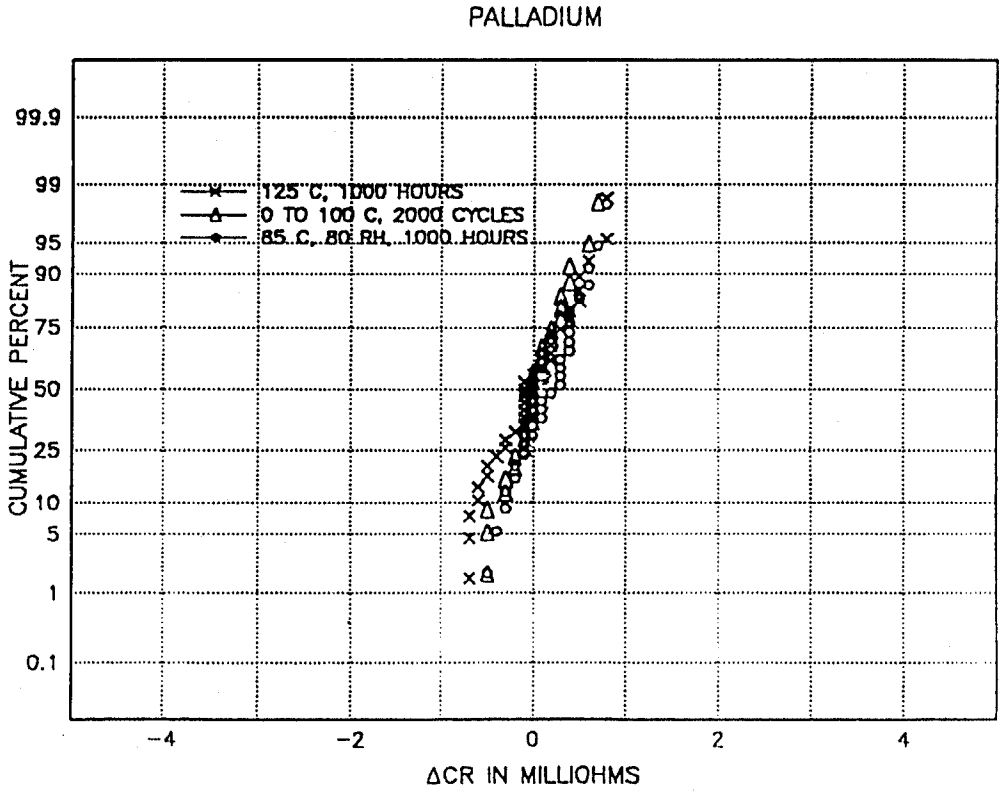

Figure 6. Distribution of changes in contact resistance for palladium plated copper comb pattern, final stress readout

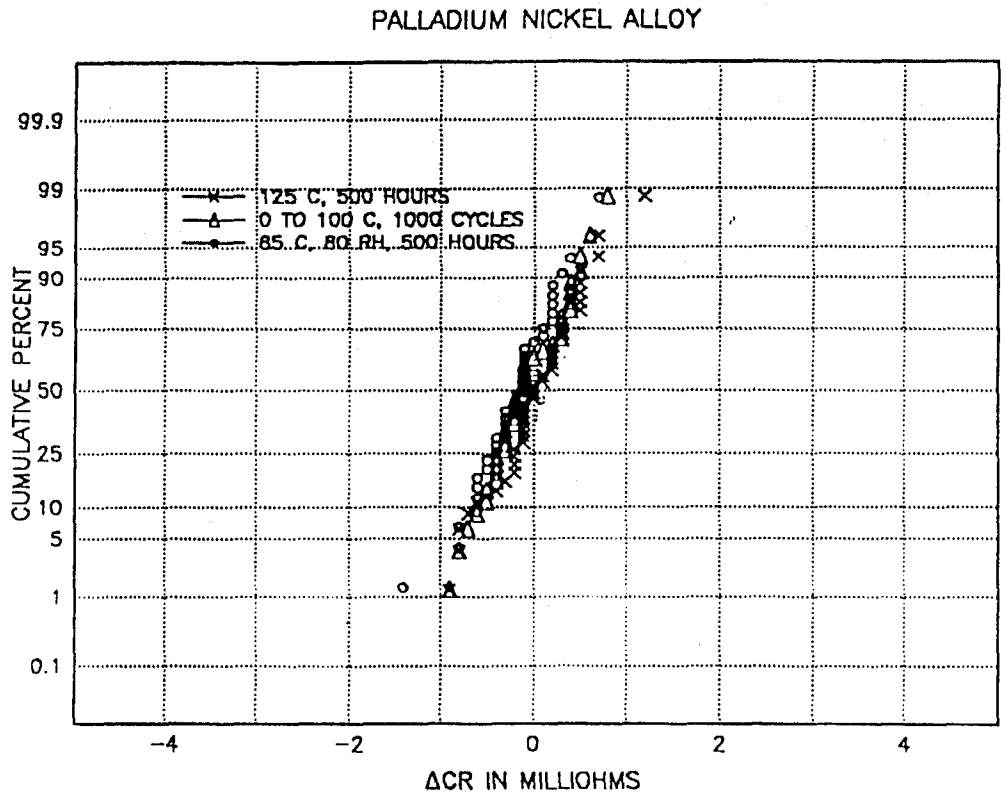

Figure 7. Distribution of changes in contact resistance for palladium-nickel plated copper comb pattern, mid stress readout

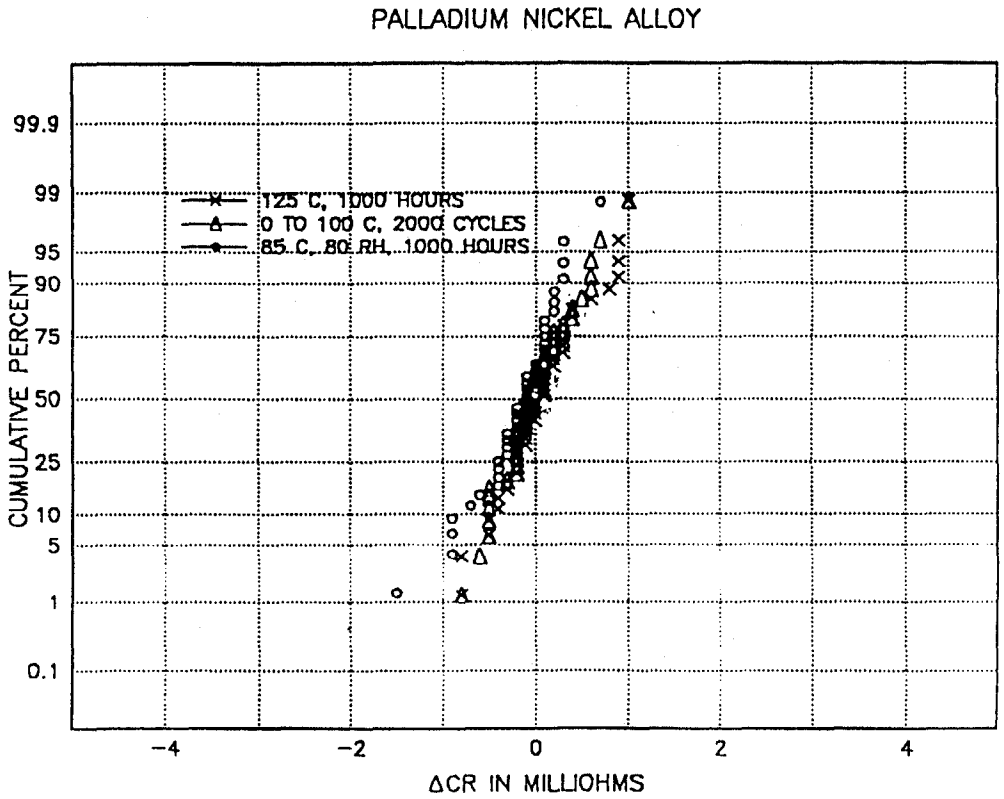

Figure 8. Distribution of changes in contact resistance for palladium-nickel plated copper comb pattern, final stress readout

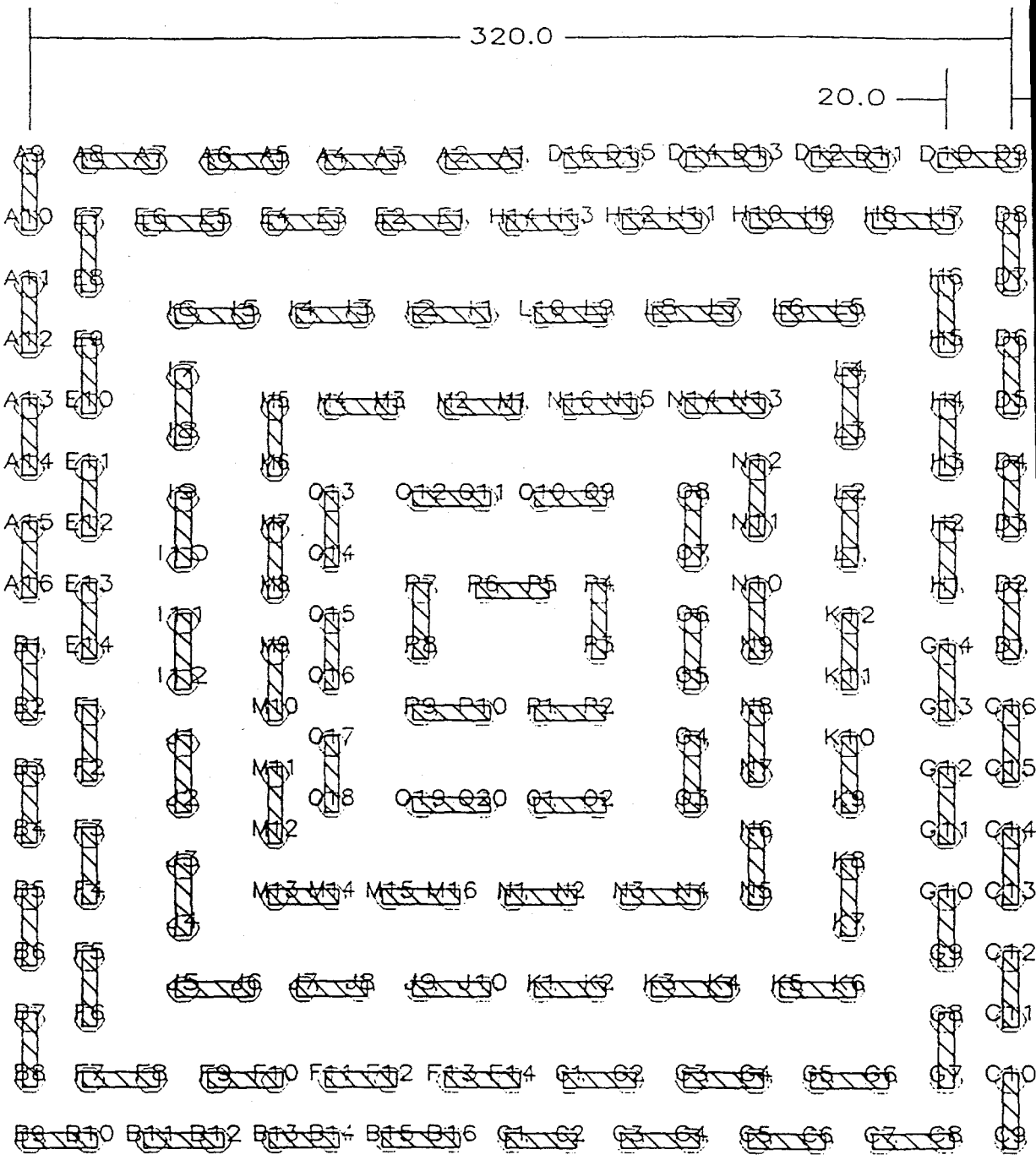

Figure 9. 0.008" feature on 0.020" pitch chip footprint

10 ON 20

UNIVERSAL INSTRUMENTS CORPORATION

ADVANCED ENGINEERING

Work Performed Under DARPA TRP Project #: DE-FC04-94AL98817

Electrically Conductive Adhesive (ECA) Flip Chip Attach

FINAL REPORT

Michael D. Snyder January 23, 1998

Stephen Haruyama January 23, 1998

Abstract

This report describes the work performed by, or under the direction of, Universal Instruments Corporation on a DARPA project investigating the use of Polymer Metal Composite (PMC) material bumped Flip Chip attachment. The work performed by Universal focussed on placement and bonding equipment experimentation to determine the equipment related process paramters needed for a successful production process. The work included construction of a variety of manual and fully automated testbeds used to support the experimentation. Also included was the development of a Computer Aided Cost Estimation (CACE) software tool used to help understand the cost tradeoff issues when comparing the PMC process to those using conventional solder based Flip Chip Attachment. The set of optimal Time-Temperature-Pressure bonding parameters were found for the attachment of IBM supplied PMC bumped Flip Chips to laminate Printed Wiring Board (PWB) material.

SIGNATURE	TITLE	DATE
M. Snyder	Manager, Advanced Engineering	1/23/98

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SECTION I: INTRODUCTION/OVERVIEW OF UIC ACTIVITIES

Introduction

In July of 1993, a TRP Proposal was submitted to the ARPA organization for the development of technology to produce high performance, low cost interconnections for flip chip attachment. Work was proposed to be carried out among IBM, Endicott, IBM, Yorktown, and Universal Instruments Corporation in Binghamton, all within New York State.

Interest in the project sprang from an industry recognized desire to find a lead free alternative to flip chip solder based attachment having lower overall cost, no alpha particle emission, and high electrical conductivity.

The responsibilities of the three parties to the joint effort were allocated such that IBM, Yorktown would develop the material, IBM, Endicott would develop the assembly process, and Universal Instruments would develop the assembly equipment capability.

The project was awarded in October of 1994, and the three parties began work in their respective areas of interest.

This report summarizes the work performed by Universal Instruments Corporation throughout the project and draws conclusions from Universal's perspective. In addition, it describes some of the further work activities on the project anticipated after the conclusion of the Government shared funding portion of the project.

Overview of UIC Activities

Universal's efforts were focused on the assembly equipment set which would ultimately be required to carry out the Polymer Metal Composite (PMC) bumped chip placement and bonding process. Universal's goal was to be able to offer to the assembly industry a set of automated tools for production when the Polymer Metal Solvent Paste (PMSP) and assembly processes were shown to be reliable and with beneficial cost / performance.

In order to achieve this goal, the Universal team carried out a variety of engineering efforts, some of which are delineated below.

- Designed, fabricated and assembled several different "benchtop" test systems to facilitate empirical studies of various aspects and properties of the IBM material under development.
- Wrote software and instrumentation control code to allow automatic data collection from several of the testbeds created.
- Analyzed data collected from the Automated Testbed experimentation.
- Designed, fabricated and assembled an automated testbed to fully carry out the PMC bonding process in conjunction with the placement of IBM supplied PMC bumped test chips.
- Integrated an automatic vision engine and processor into the control architecture of the Automated Testbed to allow automatic and precise location and alignment of the IBM supplied test chips.

- Developed a PMC bonding head with tool suspension, controls and software encompassing electrical, mechanical, pneumatic and computer elements.
- Defined the requirements for a Computer Aided Cost Estimation (CACE) software tool which was subcontracted to Binghamton University personnel for development.
- Supported research by IBM personnel on aspects of the PMSP material and assembly process development by carrying out bonding trials, underfill experiments and Instron® joint strength testing. These tests were carried out at Universal using our Surface Mount Laboratory test equipment. Over 300 such samples were prepared and evaluated.
- Debugged and characterized the various testbed pieces of equipment developed so they could be used as effective evaluation tools.
- Designed, fabricated and assembled unique fixturing to accommodate the IBM supplied substrates and test chips during test and bond exercises.

The majority of the activities described above were performed to help create an understanding of the process and process control attributes required to successfully create reliable PMC joint connections between flip chips and laminate circuit boards.

From the view of an Electronics Assembly machine supplier, Universal Instruments, three major equipment related elements are required for eventual implementation of a PMC flip chip attachment production process into the assembly industry. Those equipment related elements are:

- Attachment machinery capable of carrying out the pick up, alignment, placement and bonding of PMC bumped flip chips.
- Processing capability at rates and reliability's comparable to or better than competitive non-PMC attachment processes.
- Machinery capable of integration with existing SMT assembly process infrastructure.

In broad terms, the equipment development sequence followed the flow below:

- Develop a theoretical understanding of the material properties and identify potential assembly process issues.
- Begin preparation of a "Cost Model" to allow understanding of the business related issues which might impact machine design, cost and performance attributes.
- Develop benchtop test stands to facilitate analysis of bulk material properties.
- Conduct material property tests and assembly process element testing.
- Using the knowledge gained from the above, develop a second generation Automated Testbed to be used for assembly process testing
- Test, analyze and refine processing parametrics, establishing the interrelationships and the allowable process variable tolerances.
- Refine the Cost Model to better reflect attributes of the developing assembly process.
- Verify and optimize the process variables to create the assembly process window giving the highest degree of joint reliability.

The activities listing and the equipment development sequence described above give an overview of the Universal portion of the total work on the project. Following sections of the report will describe in more detail the structure and performance attributes of the testbeds, and discuss some of the characterization results.

SECTION II: MANUAL BONDING SYSTEM

A. Purpose

The purpose of the Manual Bonding System was to investigate the Z axis force versus displacement properties of the PMC bumps under bonding conditions. Specifically, the information was to help understand what force, temperature, and time would be acceptable for bonding so that the proper bond line thickness would be maintained between the chip and substrate. The objective also entailed testing the material characteristic differences between paste C and paste D.

B. Setup/Procedure

The figure below describes schematically the configuration of the system. The heated stage was kept nominally at 225 degrees C, at a position not underneath the spindle. A chip was placed onto the spindle and held by vacuum. The heated stage was then placed directly underneath the spindle/chip while the rod was lifted so that the chip would not contact the heated stage. A varied load was placed onto the top end of the rod. The rod was gently lowered so that the chip contacts the heated stage. The subsequent displacement of the chip under temperature and load was measured using a capacitive sensor control module connected to the Tektronix 2430A scope.

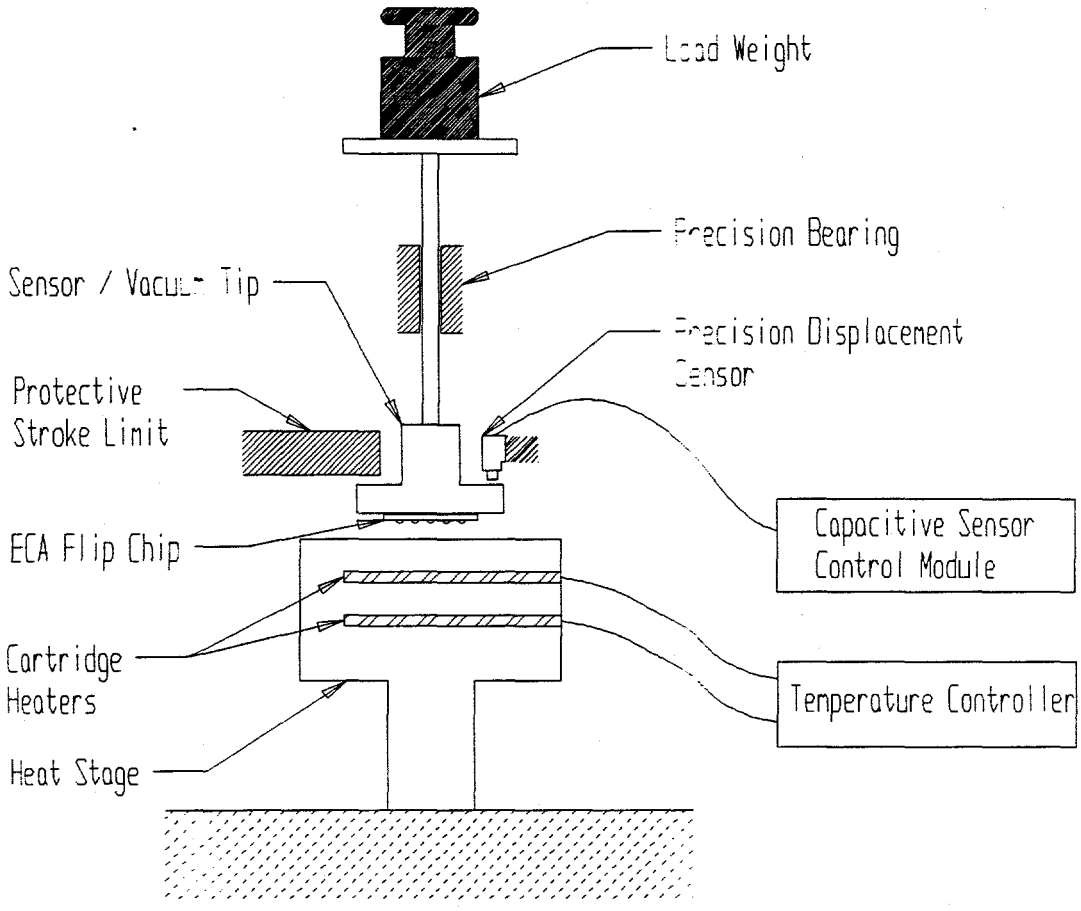


Figure 1: Main Components of the Manual Bench Top Bonding System

C. Setup Test

In order to properly measure the load displacement characteristics of the adhesive paste, precise setup and calibration of the displacement sensor was required. The total displacement of the PMC material was in the range of 25 to 50 μm, while the measurement range of the sensor was only 450 μm. Care had to be taken in the setup to measure the material's compression at the point of contact.

Because of the thermal transfer in the silicon and spindle from the heated stage, some measurement error was expected to be caused by the thermal expansion of the spindle and chip towards the displacement sensor. In order to measure this error a displacement measurement run was made with a blank silicon coupon having no PMC material. The results showed that after 25 seconds the displacement sensor measured a 2.6 μm expansion of the spindle with the heated stage set at 225 degrees C.

Calibration of the displacement sensor was performed by using a micrometer stage to move the spindle up and down by a known amount and measuring the results from the sensor. The calibration measurement results are given in the table below

Table 1: Calibration of the Displacement Sensor

	Trial 1		Trial 2	
Gap, μm	**Voltage, mV**	**Residual, μm**	**Voltage, mV**	**Residual, μm**
130	0	-0.24	0	-0.29
140	478	0.08	482	0.06
150	986	-0.21	986	-0.04
160	1476	-0.14	1496	-0.25

Based on Trial 1, the sensitivity was 20.26 μm/V and the standard deviation of the residual is .14 μm. For Trial 2 the sensitivity was 20.03 μm/V with a standard deviation of the residuals of .17 μm.

D. Results

Two types of PMC material were used for the bump compression test. These were Paste D on blank chips from wafer 7, and paste C on blank chips from wafer 12. For the constant load weight, 500 gm was used and the heated stage was kept to a constant temperature of 225 degrees C representing the expected bonding force and temperature experienced by the PMC material under real bonding conditions.

The results showed high repeatability in both the dynamic and static deflection characteristics of the PMC material. The actual deflection profile can be modeled by a first order, exponentially increasing function, where the time constant is about 0.8 seconds. The Table below shows the various deflection values at 0.5, 2.5, and 4 seconds after contact of the PMC material to the heated stage.

Table 2: PMC Compression After 0.5 seconds, 2.5 seconds, and 4.0 seconds

PMC Material	After .5 sec, μm	After 2.5 sec, μm	After 4 sec, μm
Paste D Wafer 7	11	18	20
Paste D Wafer 7	11	19	no data
Paste D Wafer 7	11	17	19
Paste D Wafer 7	15	27	29
Paste C Wafer 12	11	19	22
Paste D Wafer 7	11	17	19
Paste D Wafer 7	8	15	17
Paste D Wafer 7	4	11	13
Paste D Wafer 7	9	17	18
Paste C Wafer 12	12	17	18
Paste C Wafer 12	10	14	15

Note that the second sample had no data at the 4.0 second mark due to the scope being at the incorrect setting to measure the trace.

More than half of the deflection occurs in the first 0.5 to 1 second of applying the load. Although very repeatable from an equipment standpoint it would be very difficult in production to control the bond line thickness by the time at load. In addition, these results do not specify what time at load is required for the proper adhesion reaction to take place. The bond line thickness repeatability for the 500 gm load conditions was very repeatable from chip to chip which is a good thing from an equipment development perspective.

SECTION III: AUTOMATED TESTBED

A. System Overview

The Automated Testbed was built for the concurrent development and characterization of the PMC bumped chip to board assembly process and equipment. The design goals included the flexibility to adapt the equipment assembly and process monitoring capabilities.

Figure 1 shows the front view of the system. The system is built upon a 4 foot x 5 foot optical breadboard top. Underneath the table are two 19 inch rackmount cabinets. One of the cabinets has a 166 MHz industrial PC as the host controller and an AISI 3500 vision engine. The other cabinet has thermode driver heater cards for the upper and lower bonder heating systems as well as the system power supply. Next to the cabinets is the X-Y table servo amplifier, and various solenoid valves and regulators for the control of the pneumatic system.

Mounted to the top surface of the optical table is a stiff overhead beam to which a downward viewing, substrate location camera and a PMC Bonding Head are separately mounted. The Bonding Head consists of a theta axis for component rotation, a downward Z axis travel/force drive, and the component pick up/heating tool. On the table, directly underneath the bonding head, is a two-position shuttle driven by a pneumatic actuator. The shuttle carries and positions the component viewing illuminator/camera, and the lower board support/ heating tool directly underneath the component pick up tool.

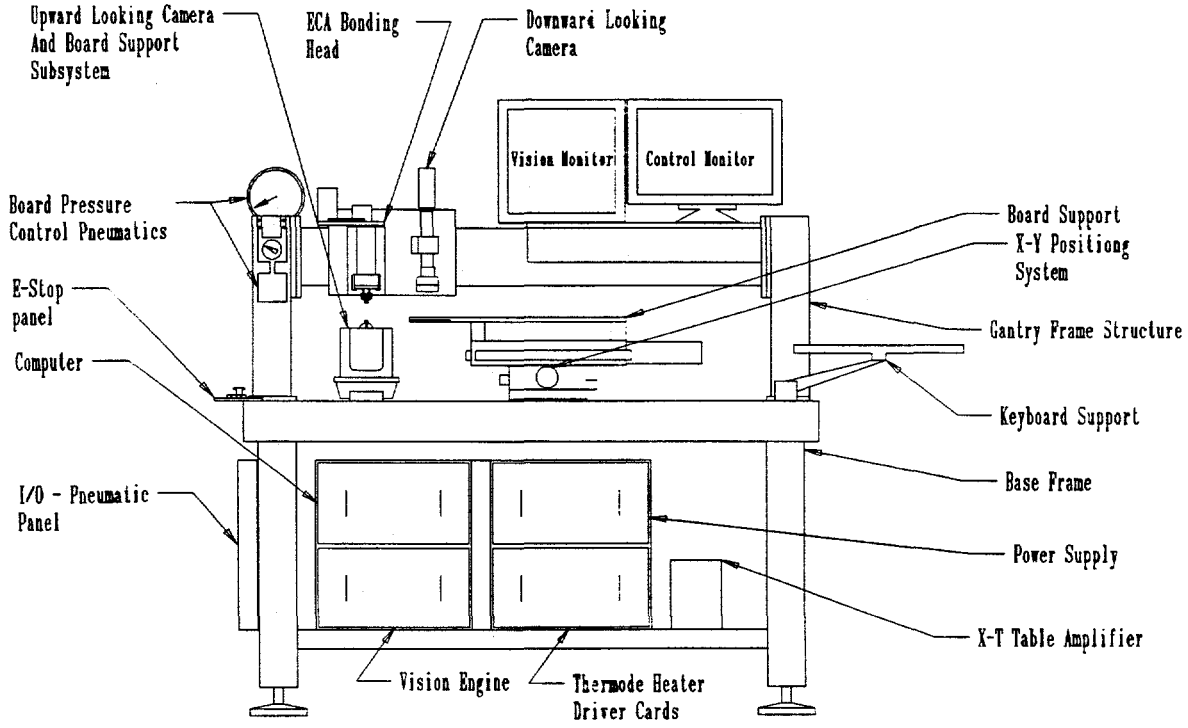


Figure 1 Front View of the Automated PMC Chip Bonding Test System

Mounted to the table directly next to the shuttle is a fully automatic X-Y positioning table. On the X-Y Table is mounted a 1/4" thick pallet which holds both a substrate and a component presentation nest. The pallet is cantilever mounted to the X-Y Table so that both the component nest and substrate bonding locations can be positioned under the component pick up tool. Underneath the substrate bonding sites the pallet material is cut out. This allows the lower heater/ board support tool to be raised into contact with the bottom side of the substrate bonding sites.

B. Key Components

1. Machine Controller

The host machine controller consists of a 166 MHz Pentium computer. The host level control program is written in LabView 4.0 running under the Windows 95 operating system. The following expansion cards are mounted in the host controller's ISA bus slots: Precision MicroControl DCX-AT200 motherboard with two MC200 servo control modules for the X-Y Table control and various digital I/O functions; California Robotics AGL4 Stepper Controller/Driver card with 8 power outputs that control the theta axis and various pneumatic solenoid valves; and a Keithly Metrabyte DDA-06 Analog Output Board with various digital I/O functions which control the upper and lower heating and illumination systems. The host controller communicates to the AISI 3500 Vision System controller through the COM 2, RS232 serial port.

2. X/Y Positioning System

The positioning system consists of a precision 12 inch x 12 inch Daedal Table model 806121 with micron/count resolution linear glass encoders. The actuation is achieved through Balder DC brush motor/Tac, MT-2240-ALYC, with a Baldor TSD series servo drive. The programmable resolution is 1 micron. Since table movement speed and acceleration were not considered critical values, these values were kept low for safety and for facilitating the initial debug activity. The velocity profile is trapezoidal with acceleration/deceleration of 254mm/sec^2, and slew velocity of 20mm/sec.

3. Upper Camera Assembly

The upper camera assembly consists of a 512 X 512 pixel CCD camera, optics, and variable intensity illumination ring. The nominal scale factor of the camera pixel coordinates to global micron coordinates is 6.2 microns/pixel. The upper camera assembly image is sent down to the camera 1 port of the AISI 3500 vision controller.

4. PMC Bonding Head

a. Theta Axis

The theta axis consists of a .9 degrees/step, 118 oz-in holding torque stepper motor rotating the pick up/upper heating tool through a timing belt with a reduction ratio of 7.5:1. Since the motor is operated in quarter steps the programmed step resolution in the theta axis is .03 degrees. The programmed velocity profile is trapezoidal with an acceleration/deceleration of 60 degrees/sec^2, and a slew velocity of 84 degrees/sec.

b. Z Axis

The Z axis subsystem provides the guidance and power required for the controlled vertical motion of the bonding head. The vertical motion is guided by a crossed roller linear bearing set and the power for the motion is provided by two Airpot® pneumatic actuators. These actuators are designed for extremely low internal friction under breakaway or impending motion conditions, and are very suited for precision force and motion control applications.

One of the two actuators controls gross motion of the bonding head along the Z Axis, with its prime function intended to move the head from its full up position to a position approximately 0.1 inches from the surface of the target substrate. The second actuator is used to control Z Axis motion over the last 0.1 inches of travel to the substrate and allows the component to rest upon the substrate target site.

Slightly below the point at which a component would contact the substrate surface is an adjustable "hard stop" which defines the lowest permissible travel of the bonding head. This "hard stop" position is used during the component inspection mode to position the component over the upward viewing camera and illumination system.

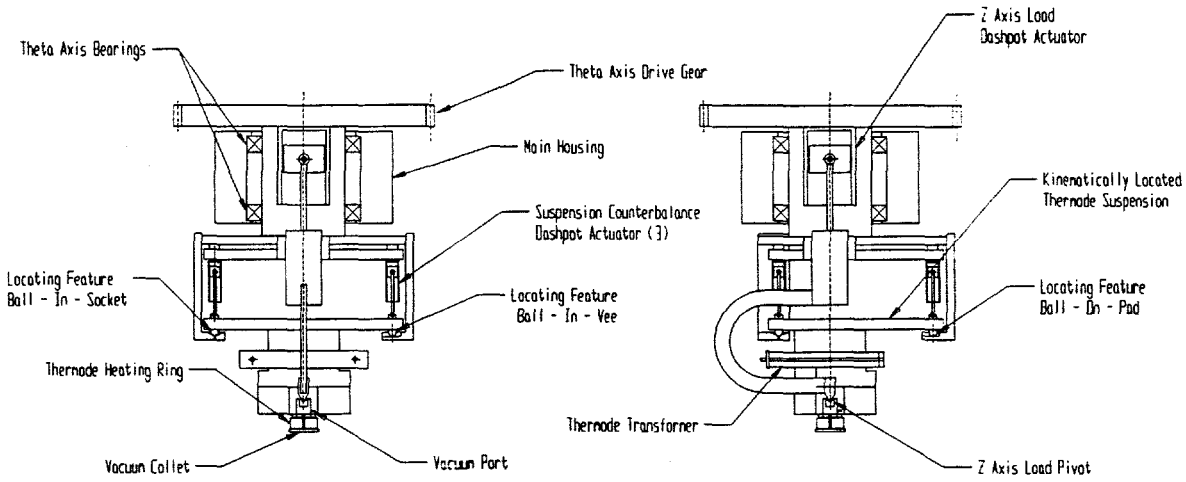
Operation of these two actuators is further detailed under the section dealing with the sequence of operations of the Automated Testbed.

c. Bonding Head Suspension

The suspension mechanism consists of a balanced and virtually free-floating bonding/pick up tool with a downward load applied by an Airpot® actuator. While the bonding head is in the up positions, or while the bonding head is down on the hard stop for component inspection, the bonding/pick up tool is locked into position by a nominally 700 gram load acting on a one degree of freedom kinematic style support. This support consists of three balls on the bonding /pick up tool located by three different mating surfaces on the bonding/pick up tool support bracket mounted from the bonding head. The mating elements consist of a ball to a socket, a ball to a vee groove and a ball to a flat pad. During component pick up and bonding operations the bonding tool is pushed off and unlocked. The bonding/ pickup tool and component is free to comply with the orientation of the pick up or substrate surfaces. A downward load is applied by the airpot to a point very near to, and in the center of the pickup surface in order to assure that only a purely normal load is applied to the component. The pressure to the actuator is programmed through a Proportion-Air BB1ME030-S61 Servo valve, which can deliver a pressure from 0 to 24 PSI. This translates to an output force from the actuator of 0 to 7.36 pounds. The programmable resolution is 0.1 pounds with system error at the actuator of ±.05 pounds.

d. Upper Bonding/Pick Up Tool

The upper bonding /pickup tool is composed of a 40:1 turns ratio transformer with the one turn secondary forming a circular resistance heating element. Inserted into this element is a collet with a vacuum port and component pick up surface. A type K thermocouple supplies the temperature feedback to a current amplifier. The programmable temperature is between room temperature and 500 degrees C. The programmable resolution is 1 degrees C. The steady state temperature error is ± 5 degrees C.



(a) (b)

Figure 2 (a)-(b):Front and Side Views of the Bonding Head

5. Lower Camera and Board Support Subsystem

a. Lower Camera Assembly

The lower camera assembly consists of a 512 X 512 pixel CCD camera, optics and variable intensity illumination ring. The nominal scale factor of the camera pixel coordinates to global micron coordinates is 27.4 microns/pixel. The magnification was designed to allow all the pertinent bumps on the component to be imaged in one field of view.

b. Lower Bonding/Board Support Tool

The lower bonding tool is similar to the upper bonding tool except that the construction is not compliant. Instead the construction has been designed to provide a heated substrate support function.

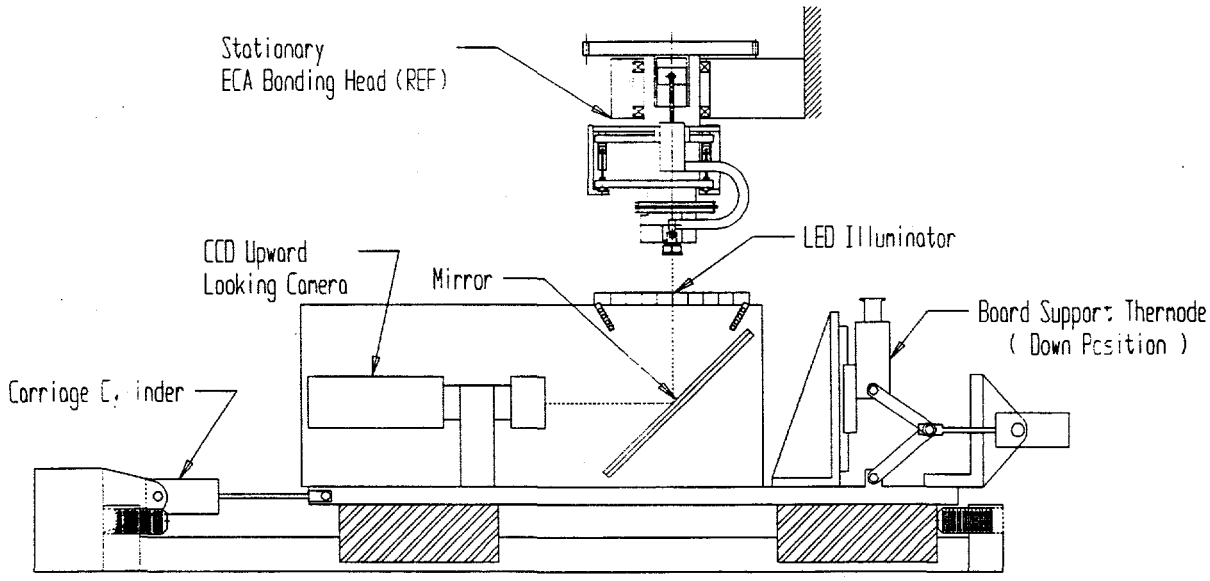


Figure 3 (a): The lower camera and board support subsystem in position to view a chip component on the bond head.

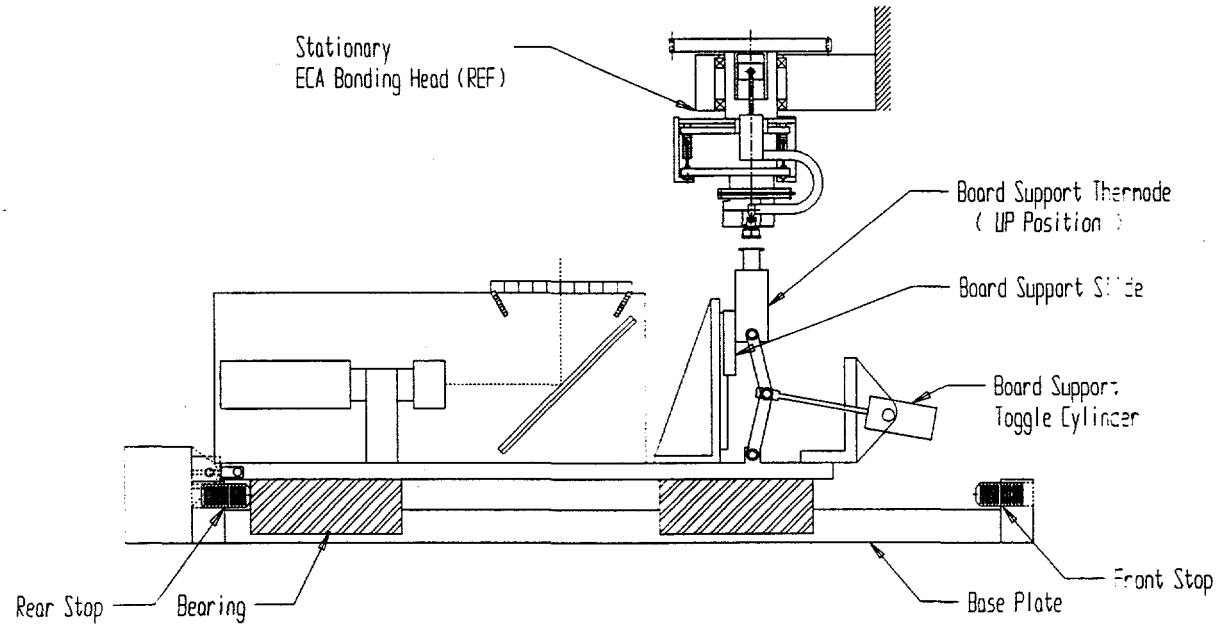


Figure 3 (b): The lower camera and board support subsystem in bonding position

C. Sequence of Operation

The sequence of operation of the testbed is as follows.

1. The operator, through the user interface program, positions the X-Y Table to load the component and substrate.

2. The operator manually loads the substrate and component.

3. Through the user interface program the operator appropriately sets the bonding process parameters, including the upper bonding temperature, lower bonding temperature, upper idle temperature, bonding force, and bonding duration.

4. The operator initiates the bonding cycle through the user interface.

5. The positioning system moves the substrate underneath the downward viewing camera to locate the bond site.

6. The upper heater tool is brought up to the idle temperature and the lower heater tool is brought to its bonding temperature.

7. The component is positioned for pick up by the X-Y Table.

8. The Z axis brings the upper tool down. After vacuum is applied and the component is secured to the tool, the tool with the component moves to the up position.

9. The shuttle positions the component illuminator/camera underneath the suspended component.

10. The Z axis brings the tool down against a hard stop, which puts the component in focus to the component viewing camera.

11. The location and orientation of the component is determined.

12. The component is oriented to match the orientation of the bonding site.

13. The pick up tool and component are brought back to the up position.

14. Based on the location of the bonding site and component, the substrate is positioned underneath the component in alignment with the bond site.

15. The lower heater/board support tool is brought to the heating/support position

16. The Z axis lowers the component onto the bond site and ramps the force up to the bonding force level.

17. The upper heater increases the temperature to the upper bonding temperature level and maintains it until the time elapsed is equal to the programmed bonding time. The heating is then turned off on both the upper and lower heaters.

18. The temperature is monitored by the operator on an oscilloscope. When the temperature reaches to a cool temperature level of less than 120 degrees C the operator initiates lift off through the user interface program.

19. The vacuum is turned off to the pick up tool, the Z axis drive reduces the downward force then lifts the upper heater/pickup tool off the bonded component.

20. The lower heater/board support tool is brought to the down position, and the shuttle positions the component/camera underneath the upper heater/pick up tool.

21. The cycle is repeated for the remainder of the parts.

22. The bonded parts are positioned to a location where the operator may unload the parts.

D. System Characterization

A series of tests were performed to characterize the system. The critical items of interest can be generalized into three categories X/Y Alignment, Z Axis Force Output, and Thermal Output.

1. X/Y Alignment

The X/Y Alignment category deals with the system components and functions, which are critical to aligning the bumps on the chip to the pads on the board. The program dealt only with features of .008 inch diameter on 0.02 inch pitch spacing so that a final misalignment of ± 0.001 inch was acceptable. The following are the tests performed for X/Y Alignment characterization.

a. X/Y Laser Measurements

On August 11, 1997 the X-Y Table was calibrated with a laser interferometer. The test was performed in accordance with ANSI/ASME B89.1.12 M-1985 in compliance with MIL-STD-45662A and with standards traceability to National Institute of Standards and Technology (NIST) number 821/254855-95. The laser interferometer traceability number is 08A014/9002. A bi-directional run with the measuring point at both the center of the table and the approximate location of the bonding pads, work area, were performed. X/Y squareness and repeatability was also checked after every run with an 8 X 6 inch granite square having serial number 33010.

The linear displacement accuracy over a range of 280mm for the X axis and 250 mm for the Y axis was found to be 0.032 mm and 0.016 mm, respectively. The repeatability is ± 0.002 mm. The orthoganality was 0.005 mm over 6 inches. Figures 4a-4d shows the data plot of the X and Y axis errors both for the measuring point at the center of the axis and at the work area.

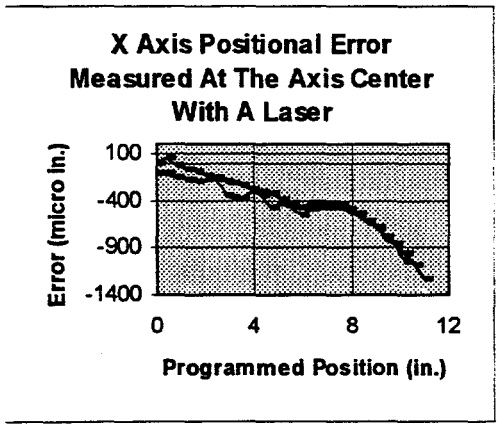


Figure 4a: X Axis Positional Error Measured at the Axis Center

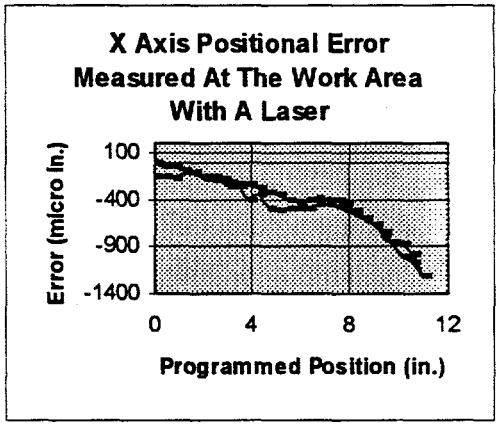
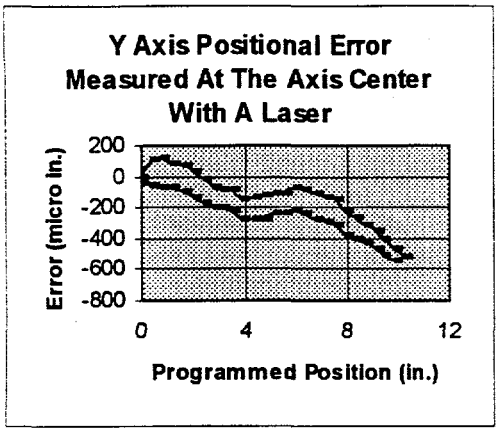


Figure 4b: X Axis Positional Error Measured at the Work Area



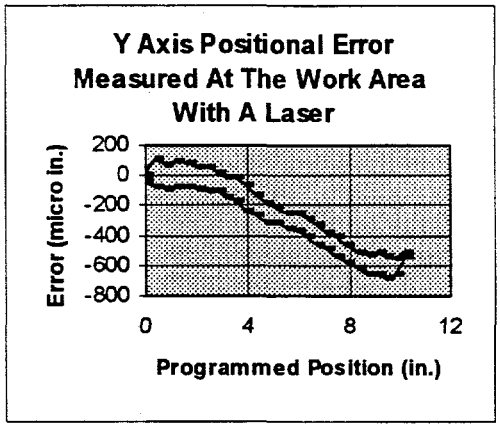


Figure 4c: Y Axis Positional Error Measured at the Work Area

Figure 4d: Y Axis Positional Error Measured at the Axis Center

Figure 4 (a)-(d): Various laser interfermetry measurements of the X and Y axis errors along a programmed position. Measurements were taken on each axis at both the center and at the location on the axis where the circuit board substrate was held for bonding.

b. Repeatability of Locating A Stationary Component

A test was run to characterize the repeatability with which the upper looking camera could locate a component as it would for a component bonding process. In preparation for the test the component picked from the component nest and initially located by the upward looking vision system iteratively rotated the component to align it to the measurement coordinate system. The test results show that for a sample of 22 vision location trials both the X and Y axis measurement repeatability fell within ± 0.5 μm, the theta axis was within 0.008 degrees. Table 1 below shows the data collected during this test.

Table 1: X, Y, and Theta Axis Vision Measurements of A Stationary Component

Trial #	X Location (m)	Y Location (m)	Theta Location (deg)
1	43	54	0.005
2	43	54	0.005
3	42	55	-0.005
4	43	54	0.005
5	43	54	0.005
6	43	54	0.005
7	42	54	0.010
8	43	55	0.000
9	43	54	0.005
10	43	54	0.005
11	43	54	0.005
12	43	54	0.005
13	43	54	0.005
14	43	54	0.005
15	43	54	0.005
16	43	54	0.005
17	43	55	0.000
18	43	54	0.005
19	43	55	0.000
20	43	54	0.005

21	43	54	0.005
22	43	54	0.005

c. Alignment Repeatability with Z Move

This test was used to determine the influence on X and Y axis location repeatability after the component has been moved up and down along the Z axis. To begin the test the component was initially picked, located, and rotated iteratively to achieve squareness with the measurement system which is the upward looking vision system. The total of 30 trials and measurements were made. For each trial the Z axis brought the component first up then back down, and finally the component location in X, Y, and Theta was determined by the upward looking camera. The test results show that for a sample of 30 trials, the X axis repeatability fell within ± 6 μm, the Y axis measurement repeatability fell within ± 1 μm, and the theta axis repeatability within ± 0.028 degrees. Table 2 below, shows the data set for this test.

Table 2:X, Y, and Theta Axis Position Measurement of A Component After Z Axis Up/Down Motion.

Trial #	X Location (μm)	Y Location (μm)	Theta Location (deg)
1	52	24	-0.067
2	52	25	-0.067
3	52	25	-0.067
4	52	25	-0.067
5	52	26	-0.057
6	49	25	-0.057
7	50	25	-0.041
8	58	26	-0.052
9	58	26	-0.052
10	49	24	-0.041
11	59	26	-0.057
12	54	26	-0.021
13	49	24	-0.041
14	58	26	-0.046
15	48	25	-0.062
16	56	26	-0.026
17	56	25	-0.021
18	58	26	-0.041
19	59	26	-0.057
20	60	25	-0.046
21	50	26	-0.031
22	51	25	-0.077
23	52	26	-0.057
24	52	25	-0.067
25	50	25	-0.052
26	49	26	-0.041
27	52	26	-0.057
28	51	26	-0.041
29	52	25	-0.067
30	50	26	-0.041

d. Alignment Repeatability with Shuttle Move

This test was used to determine the X and Y axis component location repeatability as a function of shuttle movement. To begin the test, the component was initially picked, located, and rotated iteratively to achieve squareness with the upward looking camera. A total of 30 trials and measurements were made. For each trial the camera shuttle was brought out then back in, and the component location in X, Y, and theta was determined by the upward looking camera. The test results show that for a sample of 30 trials both the X axis component location repeatability fell within ± 3.5 μm, the Y axis measurement repeatability fell within ± 5 μm, and the theta axis within ± 0.023 degrees. Table 3 below, shows the data set for this test.

Table 3:X, Y, and Theta Axis Component Location Repeatability after Shuttle Motion.

Trial #	X Location (μm)	Y Location (μm)	Theta Location (deg)
1	47	27	0.041
2	48	19	0.057
3	47	21	0.067
4	47	20	0.062
5	48	18	0.052
6	47	22	0.067
7	46	22	0.062
8	46	22	0.062
9	46	22	0.067
10	48	22	0.046
11	46	22	0.062
12	46	22	0.062
13	46	23	0.067
14	47	24	0.062
15	47	23	0.062
16	46	24	0.072
17	47	25	0.067
18	47	25	0.062
19	49	20	0.052
20	49	17	0.026
21	43	19	0.041
22	50	19	0.041
23	43	18	0.052
24	49	19	0.057
25	48	21	0.057
26	47	23	0.062
27	47	25	0.062
28	46	25	0.072
29	47	27	0.036
30	49	27	0.041

e. Alignment Repeatability with Thermal Cycling

This test was used to determine X and Y axis component location repeatability as affected by bonding head thermal cycling. To begin the test the component was initially picked, located, and rotated iteratively to achieve squareness with the measurement system which is the upward looking vision system. A total of 30 trials and measurements were made. For each trial the bonding tool was programmed to cycle its temperature from an idle temperature of 70 degrees C to a bonding temperature of 315 degrees C, and the component location in X, Y, and theta was determined by the upward looking camera. The test results show that for a sample of 20 trials the X axis repeatability fell within ± 6.5 μm, the Y axis measurement repeatability fell within ± 10 μm, and the theta axis within ± 0.039 degrees. Table 4 below, shows the data set for this test.

Table 4: X, Y, and Theta Axis Vision Measurements of A Component with the Upper Bonding/Pick Up Tool Repeatedly Thermal Cycled

Trial #	X Location (μm)	Y Location (μm)	Theta Location (deg)
1	-54	-15	-0.067
2	-48	5	-0.088
3	-42	5	-0.082
4	-38	5	-0.057
5	-47	-4	-0.036
6	-43	-1	-0.046
7	-38	1	-0.072
8	-38	1	-0.067
9	-41	-2	-0.077
10	-41	-2	-0.072
11	-43	-3	-0.072
12	-42	-2	-0.067
13	-40	-3	-0.067
14	-46	-6	-0.103
15	-41	-4	-0.067
16	-37	-4	-0.026
17	-40	-5	-0.077
18	-40	-6	-0.077
19	-44	-7	-0.082
20	-42	-7	-0.057

2. Thermode Temperature Control

The following characterizes the repeatability and accuracy with which the programmed thermal outputs are delivered from the upper and lower thermode heaters.

a. Upper Thermode Temperature Control

The upper thermode heater was characterized by running a bonding profile programmed from an idle temperature of 70 degrees C to a bonding temperature of 315 degrees C for 30 seconds, and with a cooling period to the room ambient temperature. Temperature was measured by type K thermocouples both at the control point on the thermode heat ring and at the center of the thermode-bonding surface. The thermocouple signal from the control point was conditioned through the feedback loop of the thermode driver card and delivered to a Tektronix 2430A oscilloscope. The Thermocouple signal from the bonding surface was conditioned through an Omega Om5-LTC-K2-C linearized signal-conditioning module to a channel on the oscilloscope. It should be noted that the signal from the control point was not linearized nor adjusted with cold junction compensation while the bonding surface thermocouple signal had both corrections and was therefore accurate to $\pm$ 0.025%.

The bonding surface thermocouple was held in place by resting the bonding tool on a .75 inch diameter insulating surface and sandwiching the thermocouple between the two surfaces. Figure 5 below shows the measurements from the 2 thermocouples.

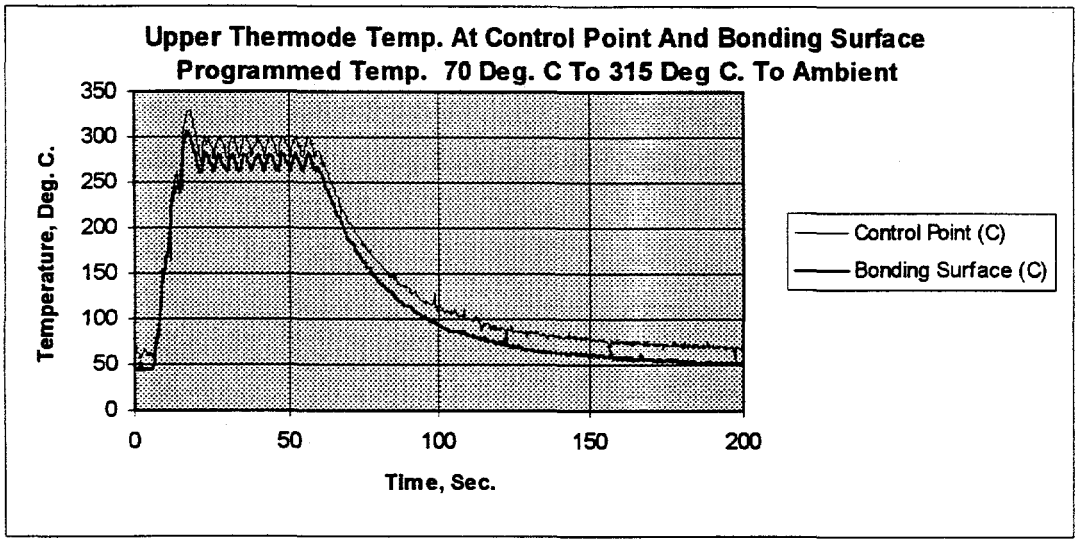


Figure 5: Upper Thermode Temperature at Control Point

Table 5 below shows the data gathered from the upper thermode temperature measurements. Note that the uncertainty in measurements from the scope was about $\pm$0.1 degrees C. for temperature, and $\pm$0.2 seconds for time.

Table 5: Upper Thermode Temperature Measurements at Control Point and Bonding Surface

	Ambient	Idle	Bond	Oversht	Max	Min	Ramp	Period	Half Life
Cntrl Pt	47	63	289	330	302	276	9.4	4.2	18.8
Bnd Sf.	27	43	272	306	281	262	10	4.2	18

The following definitions apply to the above Table.

Cntrl Pt - The reading measured by the data acquisition system at the control point.
Bnd Sf. - The reading measured by the data acquisition system at the bonding surface.
Ambient - Temperature in degrees C when no power is applied.
Idle - Temperature when the thermode is programmed for 70 degrees C.

Bond - Average steady state temperature over a 50 second dwell where the thermode is programmed for 315 degrees C.
Oversht - Peak overshoot temperature in degrees C.
Max - Maximum steady state temperature in degrees C when programmed for 315 C.
Min - Minimum steady state temperature in degrees C. when programmed for 315 C.
Ramp - Time, in seconds, to ramp from the idle temperature to the average bond level.
Period - The period in seconds of the steady state oscillations at the bonding temperature.
Half Life - The time for the exponentially decaying cool down cycle to reach one half the convergence temperature

b. Lower Thermode Temperature Control

The lower thermode heater was characterized by running a bonding profile programmed from the ambient temperature to a bonding temperature of 120 degrees C. Temperature was measured by K type thermocouples both at the control point and at the center of the thermode-bonding surface. The thermocouple signal from the control point was conditioned through the feedback loop of the thermode driver card and output to a Tektronix 2430A oscilloscope. The thermocouple signal from the bonding surface was conditioned through an Omega Om5-LTC-K2-C linearized signal-conditioning module to a channel on an oscilloscope. It should be noted that the signal from the control point was not linearized nor adjusted with cold junction compensation while the bonding surface thermocouple signal had both and was therefore accurate to $\pm 0.025\%$.

The bonding surface thermocouple was held in place by applying a .75 inch insulator with its surface sandwiching the thermocouple to the thermode-bonding surface. Figure 6 below show the measurements from the 2 thermocouples

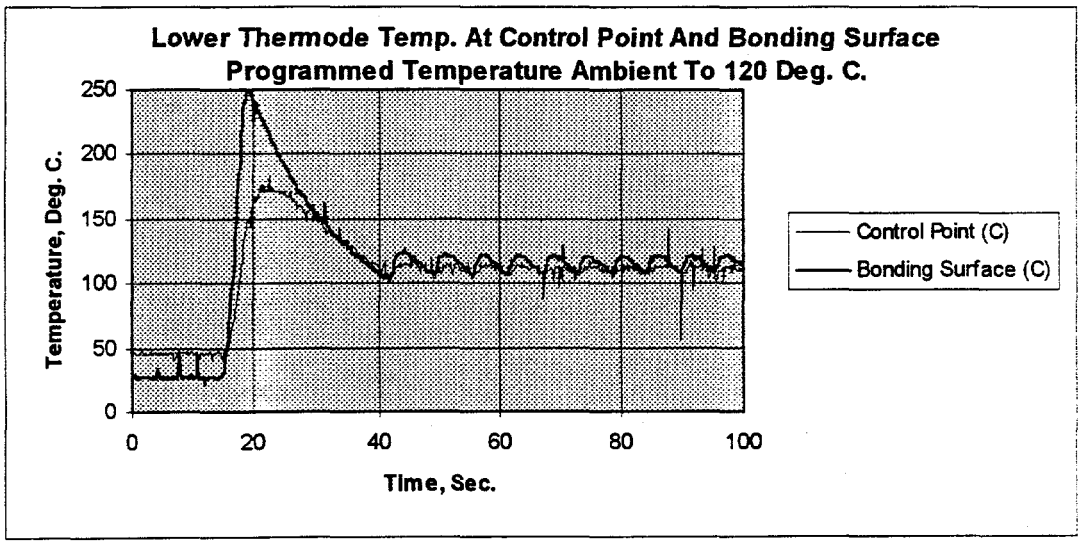


Figure 6: Lower Thermode Temperature at Control Point and Bonding Surface

Table 6: below shows the data gathered from the lower thermode temperature measurements. Note that the uncertainty in measurements from the scope was about ± 0.1 degrees C for temperature, and ± 0.1 seconds for time.

Table 6: Lower Thermode Temperature Measurements at Control Point

	Ambient	Bond	Oversht	Max	Min	Ramp	Recover	Period
Cntrl Pt	44	115	248	123	106	2.1	22.8	4.2
Bnd Sf.	26	110	172	113	106	3.1	19.8	4.2

The following definitions apply to the above Table.

Cntrl Pt - The reading measured by the data acquisition system at the control point.
Bnd Sf. - The reading measured by the data acquisition system at the bonding surface.
Ambient - Temperature in degrees C when no power is applied.
Bond - Average steady state temperature programmed for 120 degrees C.
Oversht. - Peak overshoot temperature in degrees C.
Max - Maximum steady state temperature in degrees C. when programmed for 120 C.
Min - Minimum steady state temperature in degrees C when programmed for 120 degrees C
Ramp -Time required in seconds to change the temperature from ambient to the bond level.
Recover -Time to recover from peak overshoot to first steady state minimum point
Period -The period in seconds of the steady state oscillations at the bonding temperature.

3. Z Axis Force Output

The Z axis Force output deals with the repeatability and accuracy with which a uniform normal load can be placed on the chip during bonding with negligible side loads and torques applied. This was important because the process required a bond line thickness that was greater then .002 inches in order to achieve acceptable flow of the underfill encapsulant. In order to achieve acceptable bond line thickness and uniformity, the equipment for components run in this project required a bonding force of about .5 lb, with uniform force distribution so that the bond line did not vary by more than ± 0.0002 inches from nominal. This bond line thickness controll of ± 0.0002 inches, though achieved in the production of the sample test vehicles, may not prove necessary under production conditions. Further experimental and test work is indicated to further define the requirement for such a bond line control in production.

Another requirement for the bonding forces and torques is maintaining proper chip bump to substrate pad alignment. This is because any significant side loads or torques applied to the chip may cause placement misalignment between the component and substrate.

In order to characterize the Z axis force control performance, 2 types of bonding tests were conducted. The first bonding test consisted of bonding chips onto a known flat glass substrate and measuring the bond line thickness uniformity. This test was most useful in determining if the system met specification. The second test consisted of utilizing an unique 6 degree of freedom (dof) force/torque sensor to measure both the dynamic and static forces exerted onto a chip by the Z axis force control function. Since acceptable placement alignment were achieved with the bonder, this test was useful for indicating what minimal side loads or torques would be acceptable for bonding.

a. Bonding Tests

For this test a set of components with the PMC material were received from IBM Endicott. In addition, flat, glass substrates were also used. The procedure consisted of first characterizing the bonding plane of the PMC bump surface by placing the components bump side down onto a surface plate and measuring the surface plane with a 50 millionths of an inch indicator. The bonding surfaces of the glass substrates were also characterized in the same manner except that the glass was placed bottom side down onto the surface plate. After bonding the chip onto the glass substrate, the relative heights of the glass surface and the backside of the component were measured on the surface plate with the 50 millionths indicator.

The results for several bonds indicated that with components having a $\pm$.0001 inch wedge between the PMC bump surface and the top surface of the component, the total bond line thickness was within $\pm$.0002 inches. As stated above, further exploratory work is indicated in the domain of bond line control requirements.

b. Six Degree of Freedom (DOF) Dynamic Force/Torque Measurements

The 6 dof force / torque sensor used was an ATI Nano transducer. The range and resolution of the transducer is listed below.

Sensing Ranges:

Fx, Fy:	$\pm$3 lb
Fz:	$\pm$5 lb
Tx,Ty,Tz:	$\pm$1 in-lb

Resolution:

Fx,Fy:	.05 oz
Fz:	.1 oz
Tx,Ty,Tz:	.008 in-oz

Fz is the normal Z force, Fx and Fy are the side loads and Tx, Ty, and Tz are the torques about the respective axes.

The measurement procedure consisted of mounting the sensor onto the lower thermode and holding it with vacuum. The upper thermode was brought down onto the sensor as in a bonding sequence. In this step, the full mechanical sequence of the Z axis was performed, however, since the sensor could not operate above 50 degrees C, the thermodes were not cycled thermally and the expectedly small, thermal expansion effects on the Z axis subsystem performance was not measured.

Twelve different bond force settings ranging from .559 lbs to 2.508 lbs. were run. Figure 7 below shows the typical Z axis bonding force profile from touch down to lift off at a .56 lb programmed force. At time 1.7 seconds the sensor reads 0 lbs because the tool has not touched down on the sensor. When the tool touches down on the part the force exerted is in the negative direction. After lift off, at about 13.2 seconds into the profile, the sensor once again reads 0 lbs because the tool is no longer contacting the sensor.

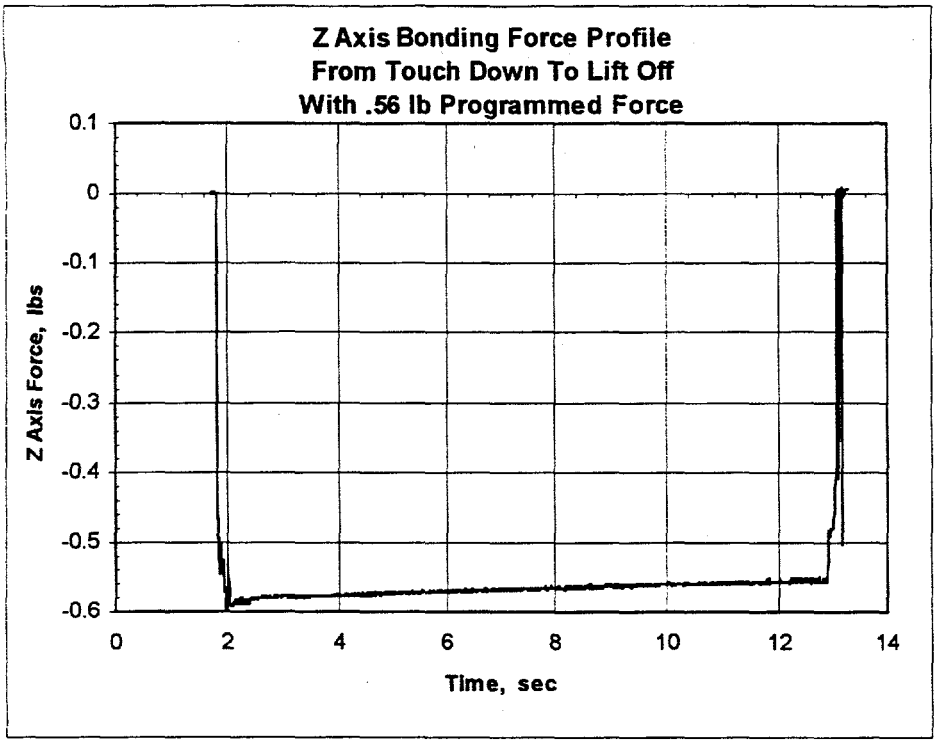


Figure 7: Z axis bonding Force Profile from touch down to lift off of the bonding tool onto the sensor with a .56 lbs programmed force

Table 7 below lists the commanded force with the actual measured Z axis output along with the peak torques and forces. Note that force Fs, is the magnitude of the side load force made up of the Fx and Fy components and Ts is the magnitude of the torque composed of the Tx and Ty components.

Table 7: Z axis and Side Load Force/Torque Performance

Fz Cmd., lbs	Fz, Meas., lbs	Residual (Fz) lbs	Fz, % Overshoot	Peak Fs, lbs	Peak Tz, in-lbs	Peak Ts, in-lbs
.559	.567	.008	5%	.047	.033	.062
.736	.73	-.006	9%	.033	.037	.082
.913	.897	-.016	12%	.043	.042	.08
1.091	1.072	-.019	12%	.063	.037	.067
1.268	1.26	-.008	12%	.076	.047	.08
1.445	1.471	.026	10%	.036	.059	.072
1.622	1.65	.028	10%	.078	.072	.107
1.799	1.81	.011	11%	.045	.068	.153
2.154	2.15	-.004	12%	.091	.013	.103
2.331	2.325	-.006	13%	.056	.014	.144
2.508	2.494	-.014	13%	.081	.087	.105

Over the whole operable range of the system the standard deviation of the commanded force to the actual steady state force, calculated through the standard deviation of the residuals from best fit line, is .016 lbs. The peak overshoot was 13%. The peak side load force was below .081 lbs. The peak Tz and Ts were .087 and .144 in-lbs, respectively. Note that for this project investigation the actual range of force used was between .5 and .9 lbs. Within this range the max Fz overshoot was 9%, the peak Fs was .047 lbs, the peak Tz was .042 in-lbs, and the peak Ts was .082 in-lbs.

The following 4 figures show in more detail the relationship between the programmed force with the measured Fz, Fz overshoot, Peak Fs, Peak Tz, and Peak Ts.

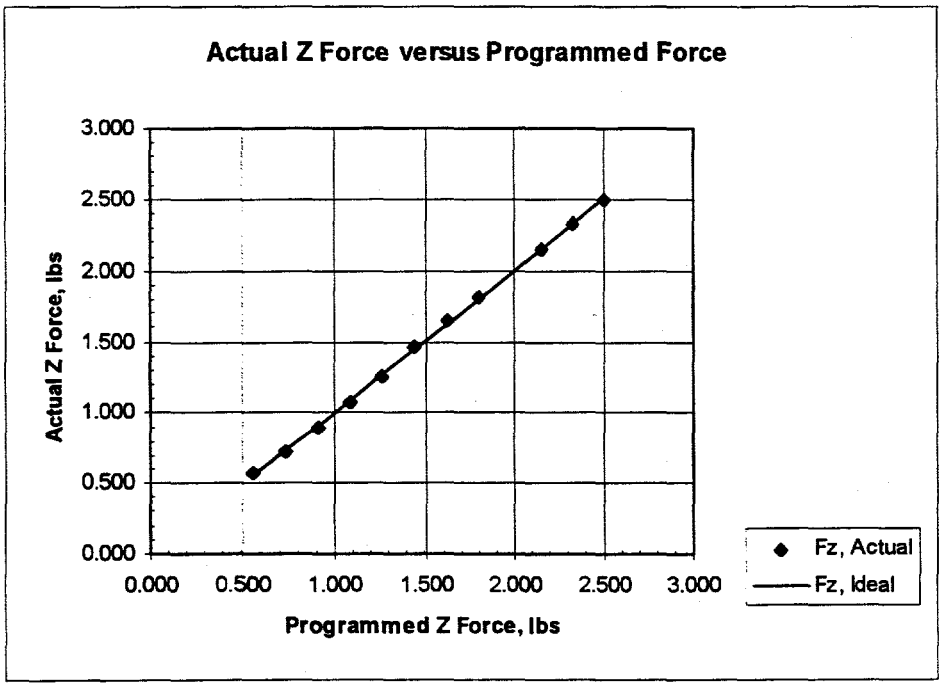


Figure 8: Actual Z force versus the programmed force

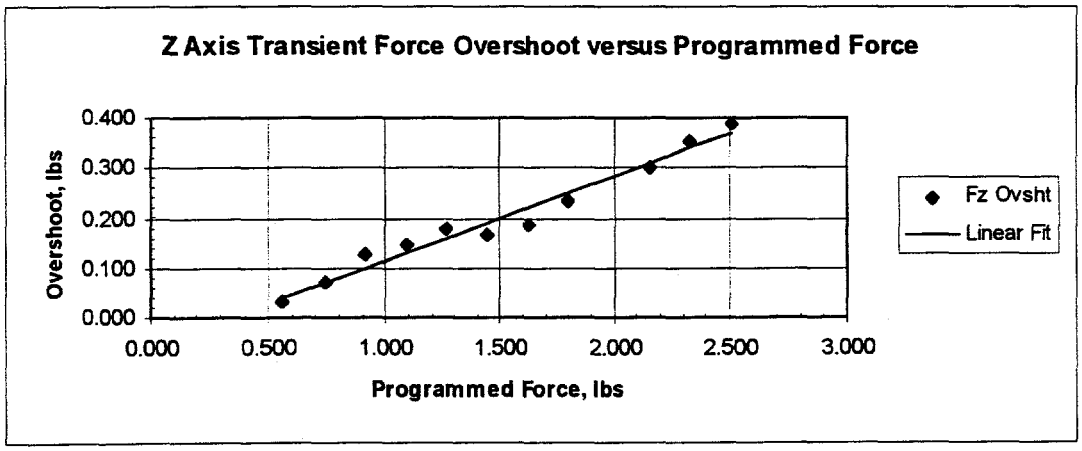


Figure 9: Z axis transient force overshoot showing linear dependence with the programmed bonding force

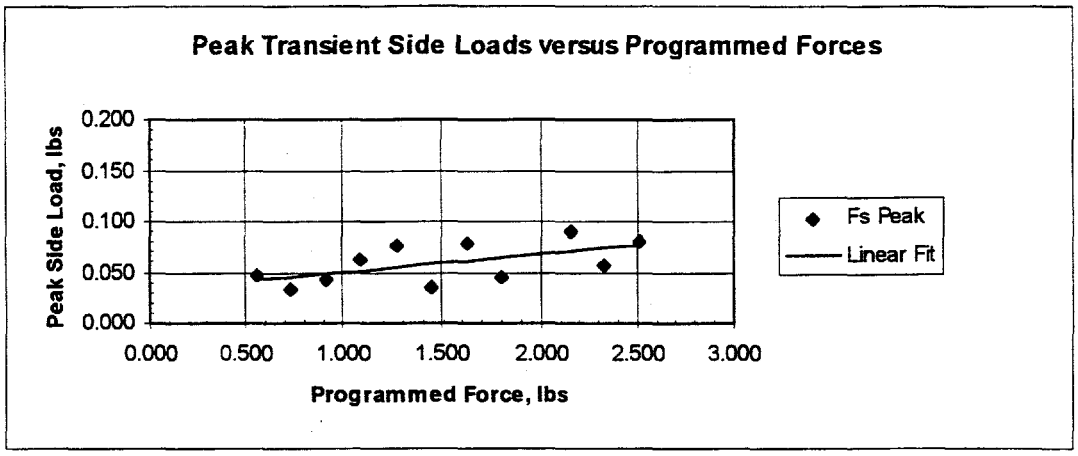


Figure 10: Peak transient side load force versus the programmed bonding force

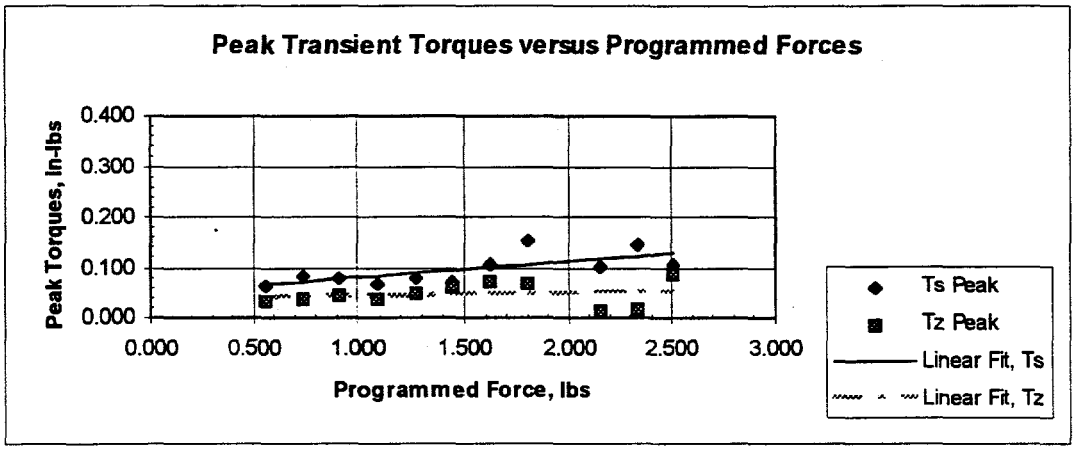


Figure 11: Peak transient torques Tz and Ts versus the programmed bonding force

SECTION IV: PROCESS DEVELOPMENT SUPPORT

A. Key Activities

This section describes the major elements of the process development support provided by Universal Instruments under the general direction of IBM Endicott. The activities were undertaken to aid the research work of IBM. In addition, some process development support was carried out for IBM Yorktown Heights to aid their investigations. All of the activities described below utilized personnel, equipment and facility resources at UIC

1. Peg Bonding

In order to characterize bulk properties of the PMSP, Universal built a bench top peg bonding system. The figure below shows the peg bonder in its entirety. The system bonds the lower and upper pegs that are held in place by a split bushing inserted in a thermal ring. The thermal ring is part of a closed loop thermode heating system like the one incorporated into the Automated Testbed. The thermode assembly is counterbalanced and free to move up and down along a Z axis slide. A known load weight is applied to the thermode assembly to apply a specific bonding force. During bonding, the pegs are supported by an insulated support post under the known load weight.

The bonding software controls the ramp time, dwell time, and temperature of the thermode. In operation an individual must perform the following steps:

1. Raise the Z axis to an up position with the load weight off
2. Insert the pegs with the split bushing into the thermode ring
3. Lower the Z axis until the lower peg contacts and is supported by the lower support post
4. Apply the desired load weight
5. Program the desired bond settings and execute the program
6. Appropriately cool the bonded pegs.
7. Remove the load weight, raise the Z axis, and remove the pegs.

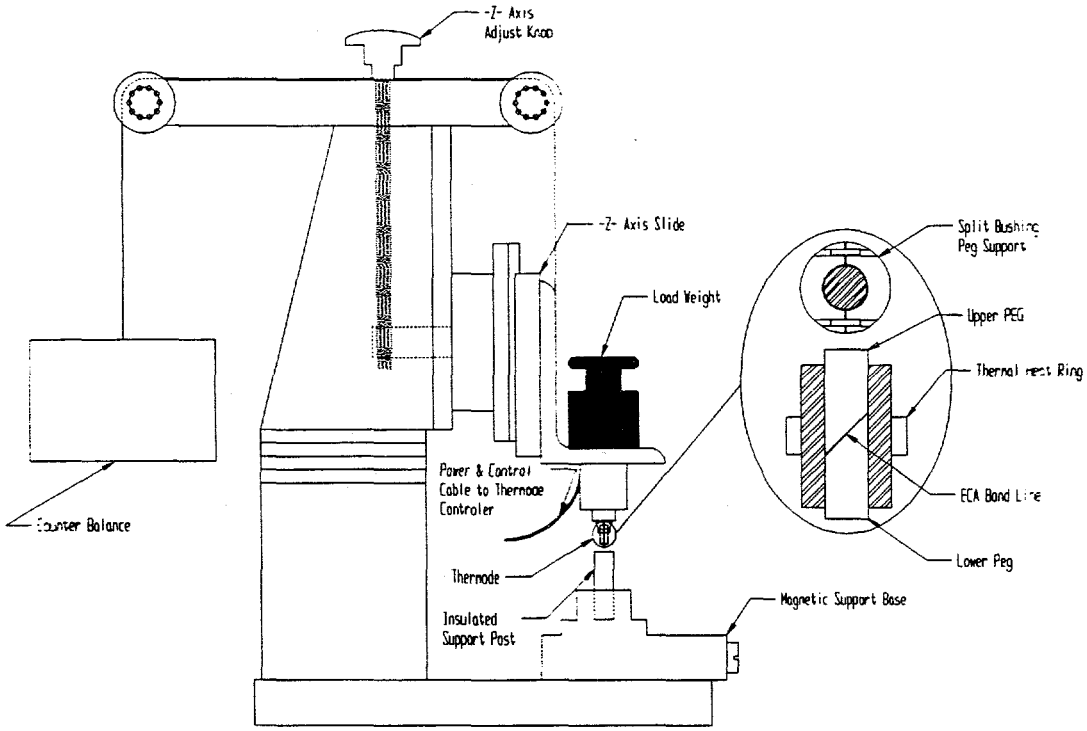


Figure 1: The peg bonding system with a magnified view of the Split Bushing Peg Support and the lower and upper pegs mounted in the support.

2. Bonding Runs

This activity consisted of bonding work performed on the automated bonding test bed developed by and located at UIC. For this work various process parameters including upper thermode idle and bonding temperature, lower thermode idle and bonding temperature, bonding force, lift off temperature, bonding temperature ramp rate, cool down ramp rate, and bonding dwell time, were varied. In addition, bumped chip lot sets were varied and chemical enhancements were investigated. Some of this work was performed in conjunction with the required bonder modifications.

3. Pull Tests

This activity utilized an Instron® tensile testor to perform destructive pull strength experiments on bonded chips without encapsulation. The procedure consisted of adhering a peg to the topside of a bonded chip. The substrate would then be mounted onto a floating X/Y stage in the Instron® with an open pocket plate clamped around the edges of the bonded chip so that as the chip was pulled by the peg, the stress and displacement fields are experienced at the adhesive joints interfaces. A figure of the floating X/Y stage is given below.

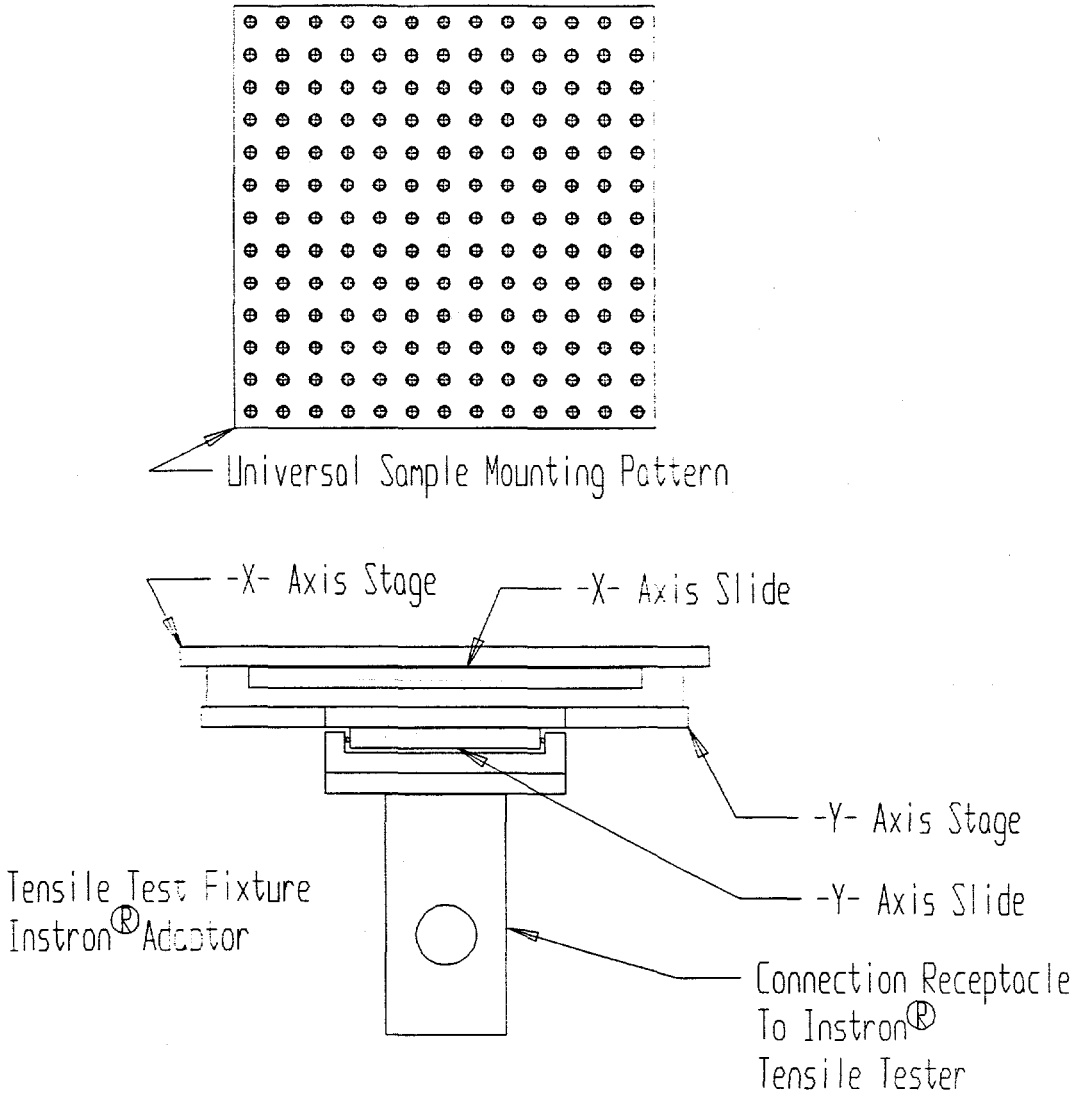


Figure 2: Floating X/Y stage and mounting plated used for pull testing on the Instron® To remove side loads during pull tests.

4. Encapsulation

The process of encapsulation required the use of hot plates and ovens to underfill and cure encapsulant material. Depending on the encapsulant material used, the cure time and temperature was varied.

5. Equipment modifications

The equipment and its operation were modified to enable testing and process development. Included were software changes, bonding head alterations, and vision system upgrades.

6. Fixtures

A substantial number of fixtures were made for both IBM Endicott and Yorktown Heights to facilitate the above activities.

B. Activity Log 2/12/97- 11/7/97

The following list shows a representative example of some of the process development support activities carried out through the 1997 period.

1. Bonding Run Test 2/12/97

Performed bonding feasibility tests with the following common settings: upper/lower bonding temperature 120 degrees C/285degrees C; upper/lower idle temperature of 70degrees C/70 degreesrees C; Bonding time of 30 seconds. The following table summarizes the settings:

Run	Substrate	Paste Type	Force (lb)	Servo Valve (PSI)
1	BT-Board	D	.7	2.2
2	BT-Board	D	.7	2.2
3	BT-Board	C	.7	2.2
4	BT-Board	C	.7	2.2
5	BT-Board	D	.4	1.4
6	BT-Board	D	.4	1.4
7	BT-Board	C	.4	1.4
8	BT-Board	C	.4	1.4
9	BT-Board	D	1	3.3
10	BT-Board	D	1	3.3
11	BT-Board	C	1	3.3
12	BT-Board	C	1	3.3
13	Glass	D	1	3.3
14	Glass	D	1	3.3
15	Glass	D	.7	2.2
16	Glass	D	.4	1.4

2. Bonding Run and Encapsulation Test 2/27/97

Performed bonding and encapsulation feasibility testing to help determine best process or dominant process variables and trends. The common settings used for the boards are upper/lower bonding temperature of 120 degrees C/285degrees C; upper/lower idle temperature of 70degrees C/70 degrees C; and Bonding time of 30 seconds. There were two bonding sites for each board for a total of 22 board sites. Five of the boards were not encapsulated at UIC. There were 7 bonds performed on glass substrates with no encapsulation. The following table summarizes settings used.

Substrate	Paste	Chip	Underfill	Force Cmd	Servo Valve,psi	Oven 1 Time/Temp	Oven 2 Time/Temp
Board 1	D	Stitch	None	630	1.1	NA	NA
Board 2	D	Blank	None	780	2.3	NA	NA
Board 3	D	Stitch	4511	780	2.3	26min/80 C	240min/130 C
Board 4	D	Stitch	Recap	780	2.3	60min/80 C	NA
Board 5	D	Blank	4511	780	2.3	26min/80 C	240min/130 C
Board 6	C	Stitch	None	780	2.3	NA	NA
Board 7	C	Stitch	4511	780	2.3	26min/80 C	240min/130 C
Board 8	C	Stitch	Recap	780	2.3	60min/80 C	NA
Board 9	D	Stitch	None	630	1.1	NA	NA
Board 10	D	Stitch	None	780	2.3	60min/80 C	NA
Board 11	D	Stitch	Matsushita	780	2.3	22min/80 C	91min/130 C
Board 12	C	Stitch	Matsushita	780	2.3	NA	NA
Glass 1	D	Stitch	None	630	1.1	NA	NA
Glass 1B	D	Blank	None	630	1.1	NA	NA
Glass 2	D	Stitch	None	780	2.3	NA	NA
Glass 2B	D	Stitch	None	780	2.3	NA	NA
Glass 3	D	Stitch	None	910	3.2	NA	NA
Glass 4	C	Stitch	None	780	2.3	NA	NA
Glass 5	C	Stitch	None	910	3.2	NA	NA

3. Equipment/Software Modifications 3/6/97-3/13/97

Modified equipment configuration to perform bonding work for IBM Yorktown Heights. These included the following changes to accommodate their wafer substrates and components.

- Changed bonding coordinates
- The up position of the lower thermode was altered by 0.007 inches.
- The locating edges of the wafer holder were shimmed to increase accuracy.
- Tested the difference in locating the chip between the automatic and manual modes.

4. Bonding Run 3/25/97

Performed bonding and encapsulation feasibility tests to help determine best process or dominant process variables and trends. The common settings used for the boards are lower bonding temperature of 120 degrees C; upper/lower idle temperature of 70 degrees C; bonding time of 30 seconds, and Paste D bumped chips. Each board had two sites while the glass slides had one site per slide. The following table summarizes the settings used.

Site	Substrate Type	Chip	Underfill	Bond Time, sec	Force lb	Force Cmd	Servo Valve,psi	Bond Temp, C	Oven Time/Temp
U1-a	Board	Blank	4511	18	.4	630	1.2	250	24hr/125 C

U1-b	Board	Blank	4511	18	.4	630	1.2	300	24hr/125 C
U2-a	Board	Blank	4511	68	3	780	9.7	250	24hr/125 C
U2-b	Board	Blank	4511	68	3	780	9.7	300	24hr/125 C
U3-a	Board	Blank	4511	18	3	780	9.7	250	24hr/125 C
U3-b	Board	Blank	4511	18	3	780	9.7	250	24hr/125 C
U4-a	Board	Blank	4511	18	.4	630	1.2	250	24hr/125 C
U4-b	Board	Blank	4511	18	.4	630	1.2	250	24hr/125 C
1	Board	Blank	None	18	.4	630	1.2	250	NA
2	Board	Stitch	None	18	.4	630	1.2	250	NA
3	Board	Blank	None	68	.4	630	1.2	250	NA
4	Board	Stitch	None	68	.4	630	1.2	250	NA
5	Board	Blank	None	18	.4	630	1.2	300	NA
6	Board	Stitch	None	18	.4	630	1.2	300	NA
7	Board	Blank	None	68	.4	630	1.2	300	NA
8	Board	Stitch	None	68	.4	630	1.2	300	NA
9	Board	Blank	None	18	3	1880	9.7	250	NA
10	Board	Stitch	None	18	3	1880	9.7	250	NA
11	Board	Blank	None	68	3	1880	9.7	250	NA
12	Board	Stitch	None	68	3	1880	9.7	250	NA
13	Board	Blank	None	18	3	1880	9.7	300	NA
14	Board	Stitch	None	18	3	1880	9.7	300	NA
15	Board	Blank	None	68	3	1880	9.7	300	NA
16	Board	Stitch	None	68	3	1880	9.7	300	NA
glass 1	glass	Stitch	None	18	.4	630	1.2	230	NA
glass 2	glass	Stitch	None	18	.4	630	1.2	280	NA
glass 3	glass	Stitch	None	68	3	1880	9.7	280	NA
glass 4	glass	Stitch	None	18	3	1880	9.7	230	NA

5. Bonding Run 4/3/97

Modified system to bond with altered temperature ramp and cool down rates. Bonding was performed to determine the effect of variable ramp and cool down rates. The common settings used for the boards are upper/lower bonding temperature of 120 degrees C/285degrees C; upper/lower idle temperature of 55degrees C/55 degrees C; bonding dwell time of 30 seconds; bonding force of 1.78 lb; and paste C blanket chips from wafer 12. The two rates selected were a fast ramp rate of 25 degrees/sec and a slow rate of 2 degrees/sec. The substrate type was the standard two-site circuit board and also glass slides. The following are the other variable settings that were used.

Sites 1: Slow ramp up and fast cool down
Sites 2-4: Slow ramp up and slow cool down
2 glass slides: Slow ramp up and slow cool down
Sites 5-6: Fast ramp up and slow cool down
2 glass slides: Fast ramp up and slow cool down
Sites 7-10: Fast ramp rate and fast cool time
Site 11: Fast ramp rate and slow cool time

6. Process Development Meeting 4/11/97

Process review and planning meeting discussing the T-1 build, Design of Experiments (DOE), and Response Surface Analysis (RSA) tests.

7. Bonding Run 4/18/97

Performed further bonding runs to study the effects of ramp rate and smooth lift off after the dwell period. Common settings used for the boards are upper/lower bonding temperature of 120 degrees C/285degrees C; upper/lower idle temperature of 50degrees C/50 degrees C; bonding dwell time of 30 seconds; bonding force of 1.78 lb; and paste C blanket chips from wafer 12.
Site 1: Ramp time of 110 seconds with no cooling period before lift off.
Site 2: Ramp time of 110 seconds with no cooling period before lift off
Site 3: Ramp time of 110 seconds with no cooling period before lift off
Site 4: Ramp time of 110 seconds with cooling period before lift off
Site 5: Ramp time of 110 seconds with cooling period before lift off
Site 6: Ramp time of 8 seconds with cooling period before lift off
Site 7: Ramp time of 8 seconds with cooling period before lift off
Site 8: Ramp time of 8 seconds with cooling period before lift off

8. Visual and X-Ray Inspection of Chips 4/23/97

Performed visual and X-ray inspection of 8 chips from wafer 7 prior to bonding on the laboratory benchtop system. The chips were bumped with paste D and were of the blanket type. The following are the results, where the bump numbers reflect the bump identification number which uniquely describes each bump:
Visual Inspection Results.
Chip A: Missing bumps 3, 67, and 55.
Chip B: Missing bumps 117, 12, and 13
Chip C: Missing bumps 52 and 204. 50-80% - 73, 129,130,222,29,20,25. 30-70% - 103.
Chip D: Missing bumps 18, 19, and 221. 50-80% - 186, 204, 217, 219. 30-70% - 101.
Chip E: Missing Bump:14, 15. 10-30% - 137, 139. Tumor - 137, 139
Chip F: 10-30% missing - 65. Satellite - 117
Chip G: Missing bump - 10, and 89. 10-30% missing -14. Tumor - 28.
Chip H: Missing bump - 9, 75, 42, 44
X-Ray Inspection Results
Chip A: No results, chip was damaged.
Chip B: 10% missing on right side - bump 1. 20-40% missing on right side - bumps 3-7. Other bumps missing volume on right side.
Chip C: Various bumps missing silver on right side
Chip D: Missing Data
Chip E: Void in the center of bump 122
Chip F: Missing silver on left side of various bumps.
Chip G: Missing silver on left side of a couple of bumps
Chip H: Missing silver on right side of various bumps

9. Equipment Modifications and Bonder Temperature Characterization 4/30/97

Wired the temperature feedback output from the thermode amplifier to the analog input channel 3

of the Precision Microcontrol DCX card. System software was modified to read the analog input signal and respond accordingly. Input values were verified with the scope. Performed a run at bond temperature of 285/120 degrees C, Idle temperature of 50/50 degrees C, bonding time of 30 seconds and bonding force of 800 gms. The chip had been prebonded and a thermocouple measured the profile at the bonding interface on the board. The following are the results of the temperature measurements:
Bonding Temperature: 258 degrees C ±8 degrees C
Overshoot Temperature: 278 degrees C with a delta of 20 C from steady state value.
Ramp time 25.4 degree C/sec
Cooling time to 177 degrees C: 10.5 seconds
Cooling time to 120 degrees C: 23.3 seconds
Cooling time to 73 degrees C: 50 seconds

10. Bonding Run and Pull Tests 5/1/97 -5/2/97

Performed bond and pull tests to study the results of chips from Paste C wafer 13, bond times and lift off temperature effects. For bonds on sites 1-4 the bonding temperature was 285/120 degrees C; idle temperature of 50/50 degrees C; bonding force of 690 gm; and a cool time of 50 seconds which corresponds to a lift off temperature of 75 degrees. Sites 1-4 had a 60 second bond time while sites 5-6 had a 10 second bond time.

Ran tests to see the effect of the lift off temperature while keeping the bonding time constant at 30 seconds. Sites 7-9 had a lift off temperature at 258 degrees C. Sites 10- 12 had a lift off temperature of 120 degrees C. Sites 13-15 had a lift off temperature of 70 degrees C.

The Instron® pull test results (lb) for sites 1-4: 21.88, 19.50, 22.26, 20.55; average: 21.05 and standard deviation: 1.09.
For sites 5-6 the pull strengths (lb):14.18 and 13.58; average: 13.88.
For sites 7-9 the pull strengths (lb):18.77, 13.55, and 15.79; average: 16.02 and standard deviation: 2.62.
For sites 10-12 the pull strengths (lb):17.14, 22.67, and 19.17; average:19.66 and standard deviation: 2.8.
For sites 13-16 the pull strengths (lb):20.13, 23.0, and 17.87; average: 20.34 and standard deviation: 2.58.

11. Bonding Run and Pull Tests 5/6/97

Performed bonding and pull tests to determine the effect of rapid forced cooling with a cold flow of air applied to the bond site just subsequent to the end of the bonding temperature dwell and prior to bonding tool lift off. The general conditions were a idle temperature of 50/50 degrees C, bonding temperature of 285/120 degrees C, bonding time of 60 seconds; lift off temperature of 120 degrees C, and bonding force of 690 gm. All of the boards were cleaned with DI H_2O and IPA. The chips were taken from wafer 13. They were blank with paste C screened. Prior to bonding the passive or normal cooling time and active cooling time were measured to be 25 seconds for the passive cooling time and 7.8 seconds for the active cooling time.

The following are the various cooling methods and pull force results:
Site 1: With passive cooling, pull strength of 18.63 lb.
Site 2: With active cooling, pull strength of 25.02 lb.
Site 3: With passive cooling, pull strength of 25.82 lb.

Site 4: With active cooling, pull strength of 16.74 lb.
Site 5: With passive cooling, pull strength of 19.82 lb.
Site 6: With active cooling, pull strength of 21.04 lb.
For passive cooling results, average pull strength of 21.42 lb, with standard deviation of 3.85.
For active cooling results, average pull strength of 20.94 lb, with standard deviation of 4.15.

12. Bonding Run and Pull Tests 5/8/97

Ran 4 more bonds to increase the data set of the passive versus active cooling data. With same general conditions as on 5/6/97 the following are the results:
Site 1: With passive cooling, pull strength of 17.27 lb.
Site 2: With active cooling, pull strength of 25.02 lb.
Site 3: With passive cooling, pull strength of 25.82 lb.
Site 4: With active cooling, pull strength of 16.74 lb.

Further bonds were made for a preliminary check of the new and old screened wafers. Chip samples were taken from the following wafers:
Wafer 21: Stitched and screened on 5/7
Wafer 18: Blank and screened on 5/7
Wafer 12: Blank and screened on 2/12.

The bonding conditions used were the same as for the first four sites with passive cooling. The following are pull test results from the subsequent bonds:
Site 5: With wafer 21, pull strength of 18.4 lb.
Site 6: With wafer 21, pull strength of 19.55 lb.
Site 7: With wafer 21, pull strength of 17.90 lb.
Site 8: With wafer 21, pull strength of 19.80 lb.
For wafer 21, average pull strength of 18.91 lb, and standard deviation of .9.

Site 9: With wafer 18, pull strength of 16.61 lb.
Site 10: With wafer 18, pull strength of 22.39 lb.
Site 11: With wafer 18, pull strength of 19.79 lb.
For wafer 18, average pull strength of 19.6 lb, and standard deviation of 2.89.

Site 12: With wafer 12, pull strength of 22.9 lb.
Site 13: With wafer 12, pull strength of 14.93 lb.
For wafer 18, average pull strength of 18.92 lb, and standard deviation of 5.64.

13. Board Interface Failure Analysis 5/8/97

With the board/chip samples that had been pulled apart during the period of 5/1-5/7, measured the amount of board interface failures after the destructive pull tests. By understanding the correlation between the board interface failures and the pull strength results it was hoped that an understanding of the joint failure modality could be better understood. The measurements were taken by visually counting the board interface failures under a microscope. The following Table gives the board interface failure counts per site with the date that the site was bonded:

Date	Site	Board Failures		Date	Site	Board Failures		Date	Site	Board Failures
5/1	1	149		5/1	11	98		5/6	6	43
5/1	2	70		5/1	12	121		5/8	1	148
5/1	3	49		5/1	13	96		5/8	2	80
5/1	4	91		5/1	14	126		5/8	3	134
5/1	5	173		5/1	15	168		5/8	4	113
5/1	6	148		5/6	1	59		5/8	5	160
5/1	7	194		5/6	2	122		5/8	6	196
5/1	8	175		5/6	3	26		5/8	7	143
5/1	9	189		5/6	4	61		5/8	8	128
5/1	10	150		5/6	5	171				

14. Bonding, and Encapsulation Tests 5/8/97

Performed 7 bonds and encapsulations to evaluate the performance of various encapsulants. The general conditions used were bond temperatures of 285 degrees C/120 degrees C; idle temperatures of 50/50; lift off temperature of 120 degrees C; 60 second bonding dwell; and 690 gm bonding force. The following are the various encapsulant conditions used:
Sites 1-2: 4511, cure temperature of 130 degrees C for 4 hours
Sites 3-4: 4526, cure temperature of 125 degrees C for .5 hours
Sites 5-7: Matsushita, cure temperature of 130 degrees C for 1.5 hours.

15. Bonding, and Encapsulation Tests 5/8/97

Ran bonds and performed pull tests to determine the effects of lift off temperature. Ten bonds were ran with the following conditions: bond temperature of 285/120 degrees C, idle temperature of 50/50 degrees C, a bond force of 690 gm, and a dwell time of 60 seconds. All the chips used were blank with paste C from wafer 13. Sites 1- 5 had a lift off temperature of 150 degrees C, while sites 6-10 had a lift off temperature of 100 degrees C. The following table summarizes the pull test results from the bonds:

Site	Pull Strength, lb		Site	Pull Strength, lb		Site	Pull Strength, lb
1	22.17		4	17.49		7	20.56
2	14.41		5	18.02		8	22.6
3	19.45		6	20.17		9	19.33

Note Site 10 had no pull strength due to a failure of pull tester.

16. Design of Experiment (DOE) Run 5/13/97

A set of bonds were made for a DOE in preparation to a T1 build. The general conditions that were kept constant were the idle temperature of 50/50 degrees C, lift off temperature of 70 degrees C, lower thermode bond temperature of 120 degrees C, and blanket wafer 18 chips with paste C bumps. There were two levels of upper bonding temperature, 250 and 320 degrees C, two levels of bonding force, 318 and 908 gms, and two levels of bonding dwell time, 10 and 60 seconds. The following table shows the various conditions with pull test results of the bonds.

Site	Upper Bond Temp, Degrees. C.	Bond Force, gm	Bond Dwell, sec	Pull Force, lb
1	250	318	10	.7
5	250	318	60	4.29
6	250	318	60	1.57
9	250	908	10	9.7
10	250	908	10	12.7
13	250	908	60	16.9
14	250	908	60	17.3
17	320	318	10	4.85
18	320	318	10	7.14
19	320	318	10	4.91
20	320	318	10	5.42
21	320	318	60	5.4
22	320	318	60	5.29
23	320	318	60	8.05
24	320	318	60	5.21
25	320	908	10	9.58
26	320	908	10	5.85
27	320	908	10	17.14
28	320	908	10	13.85
29	320	908	60	14.35
30	320	908	60	18.63
31	320	908	60	21.04
32	320	908	60	26.74
33	320	908	10	14.10

17. Bonding, Bond Line Thickness, and Temperature Profile Tests 5/15/97

Bonded several wafer 18 chips onto glass slides with the previous DOE settings in order to study the bond line achieved with the various force, upper bond, and dwell time settings. The following are the settings and the bond line results:

Site	Upper Bond Temp, Degrees. C.	Bond Force, gm	Bond Dwell, sec	Bond Line, mils
1	285	690	60	2.1
2	320	908	60	1.3
3	320	908	10	1.5
4	250	908	60	1.2
5	250	308	60	2.6

Performed temperature profile measurements on prebonded board to determine passive cooling time and temperate ramp times for various process variable settings. For the settings, Idle temperature of 50/50 degrees C; bond temperature of 320/120 degrees C, bond time of 60 seconds and bonding force of 690 gm, the cooling times were the following:

For cool down to 180 degrees C: 14 seconds
For cool down to 150 degrees C: 20 seconds
For cool down to 120 degrees C: 29 seconds
For cool down to 100 degrees C: 38 seconds
For cool down to 70 degrees C: 69 seconds

The passive cool time measurements for bond temperature setting of 250/120 degrees C were also measured. The cool times were the following:
For cool down to 180 degrees C: 8 seconds
For cool down to 150 degrees C: 15 seconds
For cool down to 120 degrees C: 24 seconds
For cool down to 100 degrees C: 35 seconds
For cool down to 70 degrees C: 50 seconds.

18. T1 Board Run 5/16/97

For the T1 build a total of 40 chip bonds were made. Each board had 2 bond sites. The settings used were bond temperature of 285/120 degrees C, idle temperatures of 50/50degrees C, bond force of 690 gm, and a bond time of 60 seconds. The chips used were paste C, blank from wafer 18. The underfill used was an IBM developed recap encapsulant.

19. Bond Line Tests 5/20/97

To complete all of the cases for the T1 build on 5/16, 4 additional bonds were made on glass with same conditions as except that the chips used were stitch, from wafer 21 with paste C. The following table shows the variable conditions and bond line results:

Site	Upper Bond Temp, Degrees. C.	Bond Force, gm	Bond Dwell, sec	Bond Line, mils
1	250	318	10	2.4
2	250	908	10	2.5
3	320	318	10	2.6
4	320	318	60	1.6

20. Bond Line Tests 5/23/97

Two bonds were made to determine subsequent bond line thickness with the following settings: idle temperatures of 50/50 degrees C, bonding temperatures of 285/120 degrees C, bonding force of 690 gm, bonding time of 60 seconds, and a lift off temperature of 70 degrees C. The chips used were the same as the ones used on 5/20. Both bonds on glass produced a bond line of 1.1 mil.

21. Repeat Portion of DOE 5/28/97

Portions of the DOE from 5/13 were repeated. The conditions were the same except that blank paste C chips from wafer 22 was used. The table below summarizes the results.

Site	Upper Bond Temp, Degrees. C.	Bond Force, lb	Bond Dwell, sec	Pull Force, lb
1	250	.7	60	5.86
2	250	.7	10	no result
3	320	.7	10	9.10
4	320	.7	60	12.35

No result for site 2 due to sample breakage while attempting to perform the pull test.

22. Bonding Run and Pull Tests 6/3/97

Test was performed to qualify chips from newly screened wafers. One wafer, 24, was stitch, while the others 22, 23, and 17 were blank. The settings were an idle temperature of 50/50 degrees C, bonding temperatures of 285/120 degrees C, dwell time of 60 second, bonding force of 690 gm, and lift off temperature of 70 degrees C. The following are the pull test results of the bonds for the various wafers.

Site	Wafer #	Pull Force, lb		Site	Wafer #	Pull Force, lb
1	17	14.26		9	23	17.29
2	17	19.42		10	23	15.42
3	17	20.46		11	23	19.09
4	17	11.96		12	23	21.19
5	22	12.89		13	24	22.48
6	22	14.19		14	24	22.85
7	22	19.05		15	24	16.88
8	22	9.07		16	24	22.87

From the data above the following average and standard deviations are calculated:
wafer 17: average of 16.53 lb., standard deviation of 4.11
wafer 22: average of 13.80 lb., standard deviation of 4.1
wafer 23: average of 18.25 lb., standard deviation of 2.5
wafer 24: average of 21.27 lb., standard deviation of 2.93

23. 2nd DOE On 6/4/97

A second DOE was run with the following factors and levels:
Bonding time (sec):20, 40, 60
Upper bonding temperature (C): 265, 285, 305
Bonding force (gm): 500, 600, 700
Lift off temperature (C): 70, 120

The constant settings included an idle temperature of 120/120 degrees C, lower bonding temperature of 120 degrees C, blank chips from wafer 23.

Besides taking pull force measurements the resistance's of the nets at 4,1, 2, 3, and 15 were taken and recorded as R1, R2, R3, R4, and R5 respectively. The table below gives the levels for the various bonding sites.

Sites	Bond Time, sec	Bond Temp, C.	Force, gm	Lift Temp, C
1-4	40	305	700	120
5-8	60	285	700	70
9-12	60	305	500	70
13-16	60	265	600	120
17-20	20	305	600	70
21-24	20	285	500	120
25-28	40	265	500	70
29-32	40	285	600	70
33-36	20	265	700	70

The table below gives the resistance and pull force measurements for the various sites.

Site	R1, mΩ	R2, mΩ	R3, mΩ	R4, mΩ	R5, mΩ	Pull Strength, lb
1	46	48	51	47	59	10.21
2	50	50	50	52	61	15.50
3	45	76	48	51	60	21.34
4	48	48	51	53	61	18.14
5	49	48	48	51	63	23.11

6	48	47	53	53	62	14.80
7	52	51	50	53	67	18.86
8	55	53	53	58	66	17.43
9	69	66	66	64	92	22.59
10	61	59	64	69	90	20.07
11	48	49	51	52	62	23.19
12	53	52	55	58	65	21.13
13	53	52	51	54	67	16.76
14	51	49	56	59	70	13.21
15	53	54	56	58	74	19.98
16	60	58	58	64	79	13.43
17	60	open	60	61	81	17.13
18	55	52	54	58	72	15.71
19	58	59	59	58	81	21.09
20	56	56	58	60	78	19.62
21	61	84	60	62	83	12.46
22	62	58	60	64	82	10.72
23	56	56	58	59	70	11.42
24	53	52	50	54	43	11.09
25	55	55	55	55	75	6.46
26	54	54	55	61	74	7.1
27	57	59	56	57	83	9.43
28	54	58	61	62	80	10.72
29	57	58	57	58	85	17.98
30	63	60	63	66	87	12.3
31	54	55	55	56	77	16.1
32	60	59	59	62	80	14.60
33	55	51	51	56	42	0.0
34	50	51	51	55	65	9.2
35	59	58	58	59	80	8.99
36	56	55	55	60	75	12.76

24. Bond Line Tests 6/5/97

Bonded chips onto glass with conditions used on 6/4 in order to measure bond line thickness. Used wafer 23, blank chips with paste C. The table below lists the various settings with the measured bond line thickness.

Site	Upper Bond Temp, Degrees. C.	Bond Force, gm	Bond Dwell, sec	Lift Off Temp, C	Bond Line, mils
1	285	700	40	70	2.8
2	305	500	60	70	2.8
3	265	600	60	120	2.7
4	305	600	60	70	2.7
5	285	500	20	120	3.1
6	265	500	20	70	3.0
7	285	600	40	70	2.7

8	265	700	20	70	2.9
9	305	700	40	120	2.7

25. Response Surface Analysis (RSA) Run 6/17/97

After IBM determined that the dominant process settings were bonding force and bonding temperature, an RSA test was performed to more fully analyze these 2 variables. The general conditions used for the test were an idle temperature of 50/50 degrees C, a lower bonding temperature of 120 degrees C, and a lift off temperature of 70 degrees C. The upper bonding temperature had three levels: 275, 295, and 315 degrees C. The bonding force had 4 levels: 300, 500, 700, and 900 gms. The table below shows the various levels with the pull strength results.

26. Bonding, Pull, and Encapsulation Tests 6/18/97

Site	Upper Bond Temp, Degrees. C.	Bond Force, gm	Pull Force, lb		Site	Upper Bond Temp, Degrees. C	Bond Force, gm	Pull Force, lb
a	315	300	16.86		24	315	500	21.08
b	315	300	17.04		25	315	900	19.89
1	315	300	9.30		26	275	300	9.09
2	295	500	18.29		27	295	900	19.02
3	275	500	11.55		28	295	700	18.04
4	315	300	20.81		29	315	700	22.73
5	295	500	16.77		30	295	300	16.75
6	315	300	21.17		31	315	700	23.77
7	275	700	16.82		32	315	900	15.58
8	315	500	9.35		33	315	700	19.17
9	295	700	7.71		34	275	900	18.92
10	295	300	16.07		35	295	300	16.72
11	315	300	12.26		36	275	300	10.38
12	275	900	11.61		37	275	700	19.53
13	295	500	10.05		38	315	900	20.05
14	275	500	12.48		39	295	700	20.85
15	275	500	14.96		40	295	900	17.10
16	315	700	6.81		41	315	500	13.13
17	275	900	18.92		42	315	500	16.18
18	295	900	15.32		43	275	300	8.85
19	295	300	17.59		44	295	900	20.62
20	275	700	19.6		45	295	700	20.08
21	275	900	19.26		46	275	700	12.78
22	275	300	13.51		47	315	900	19.50
23	295	500	14.98		48	275	500	10.44

Performed 4 additional bonds with chips from wafer 18 and with paste C. that had been soaked in IPA fumes from 5/12/97. The bonding conditions were bonding temperatures of 285/120 degrees

C, idle temperatures of 50/50 degrees C, bonding force of 700 gm, bonding time of 60 seconds, and a lift off temperature of 70 degrees C. The pull test results for sites 49-52 in order are 18.21 lb, 18.36lb, 14.48lb, and 20.46 lb.

Three more bonds were made with the above settings except that that the wafer 18 chips had not been soaked in IPA fumes. The pull test results for sites 53-55 in order are 10.21 lb, 16.96 lb, and 15.81 lb.

27. Various Bonding and Encapsulation Tests 6/18/97

The results of the RSA determined the settings for chips from wafer 24, stitch with paste C. The general settings were idle temperatures of 50/50 degrees C, lower thermode temperature of 120 degrees C, bonding time of 60 seconds, lift off temperature of 120 degrees C, and bonding force of 700 gms. The pull force results with the upper bonding temperature setting are given below for the 6 bonds.

Site 1, 315 C: 20.17 lb
Site 2, 315 C: 23.00 lb
Site 3, 305 C: 15.94 lb
Site 4, 305 C: 19.55 lb
Site 5, 295 C: 15.77 lb
Site 6, 295 C: 18.23 lb.

With the above settings and an upper bonding temperature of 315 degrees C, bonded 6 more chips and encapsulated with 3 different encapsulant materials. Sites A and B were encapsulated and cured with Matsushita materials. Sites C and D were encapsulated and cured with Recap. Sites E and F were encapsulated and cured with Chip Coat.

Performed 5 bonds to determine the effect of upper idle temperature conditions. Besides the upper idle temperature, all of the bonding conditions were the same as the 6 previous bonds, with an upper bonding temperature of 315 degrees C. The various programmed values for idle temperature and corresponding pull test results for the sites are listed below.

Site 7, with upper idle temperature of 100 C:	13.26 lb
Site 8, with upper idle temperature of 100 C:	12.40 lb
Site 9, with upper idle temperature of 180 C:	19.22 lb
Site 10, with upper idle temperature of 180 C:	14.36 lb.
Sites 11-12 with upper idle temperature of 315 C:	No Instron® test, chips fell right off.

Performed further bonding tests with wafer 24. Listed below are the conditions and Instron pull test results.
Sites 13 and 14, with 315/120 bonding temp, 50/50 idle temp, 700 gm force, 60 sec dwell, 70 lift off: 5.81 lb and 5.81 lb
Sites 15 and 16, same settings as above except bond temperature of 295/120: 7.99 lb and 15.88 lb.
Sites 17 and 18, same as sites 13 and 14 except with 30 second dwell: 19.59 lb, and 19.76 lb.
Sites 19 and 20, same as sites 13 and 14 except no bottom side heating: 18.12 lb and 15.47 lb.

28. Bonding and Encapsulation Tests 6/23/97

Performed 4 bonds with encapsulation. General bonding conditions were: idle temperatures of

50/50 C, bond temperatures of 315/120 C, bond time of 60 sec, force of 700 gm, and a lift off temperature of 70 C. Chip sites a and b were encapsulated with Hysol 4511, while sites c and d were encapsulated with Hysol 4526. Used wafer 24 stitch with paste C.

Bonded 18 more wafer 24 chips with the above settings with exceptions noted in table below.

Site	Condition	Pull Force, lb		Site	Condition	Pull Force, lb
1	No bottom side heating	16.86		10	315 C temp, 30 sec dwell	21.08
2	No bottom side heating	17.04		11	315 C temp, 60 sec dwell	19.89
3	30 sec bond time	9.30		12	315 C temp, 30 sec dwell	9.09
4	30 sec bond time	18.29		13	No bottom side support	19.02
5	60 sec bond time	11.55		14	No bottom side support	18.04
6	60 sec bond time	20.81		15	No special condition	22.73
7	295 C temp, 60 sec dwell	16.77		16	No special condition	16.75
8	295 C temp, 60 sec dwell	21.17		17	No special condition	23.77
9	315 C temp, 30 sec dwell	16.82		18	No special condition	15.58

29. Bonding, Encapsulation, and Adhesion Tests 7/2/97

Bonded chips from various wafers. Some of the chips had been refrigerated while others had been oxygen plasma cleaned before photolithography. The standard process settings from 6/3 were used except where noted. The following lists the process differences between the sites.
Sites 1-4: Used wafer 20, blank chips with paste C, refrigerated at 4 degrees C for 2 months.
Sites 5-8: Used wafer 24, stitch chips with paste C, refrigerated at 4 degrees C for 2 months; 30 sec bond time
Sites 9-12:Used wafer 24, stitch chips with paste C, refrigerated at 4 degrees C for 4 months;
Sites 13-16:Used wafer 25 stitch chips with paste C, refrigerated at 4 degrees C for 4 months; bumps were screened on with 3 passes at 40 PSI; wafer was oxygen plasma cleaned before photolithography.
Sites 17-20:Used wafer 25 stitch chips with paste C, refrigerated at 4 degrees C for 4 months, bumps were screened on with 3 passes at 40 PSI.

The following table gives the pull test results:

Site	Wafer #	Pull Force, lb		Site	Wafer #	Pull Force, lb
1	20	18.27		11	24	14.71
2	20	20.85		12	24	17.35
3	20	19.88		13	25	17.77
4	20	21.29		14	25	14.24
5	24	18.03		15	25	18.78
6	24	14.61		16	25	15.73
7	24	16.83		17	26	17.17
8	24	19.34		18	26	11.76
9	24	19.27		19	26	15

10	24	20.58		20	26	15.06

30. Adhesion Enhancement Tests 7/2/97

Chips were bonded after 4 different types of adhesion enhancers DT, MPP, MTS, and MEA, were applied to the circuit boards. The general bonding conditions used included idle temperatures 50/50 C, bonding temperatures of 315/120 degrees C, bonding force of 700 gm, 60 sec bonding time, and 70 degree C lift off temperature. The boards were cleaned for 30 minutes using UV ozone, dipped 3 passes each for 5 minutes, rinsed in solvent and air dried.

The machine settings used were bonding temperatures of 315/120 degree C, idle temperatures of 50/50degree C, bonding force of 700 gm, bonding time of 60 sec., and lift off temperature of 70 degrees C. The type of adhesion enhancers used at each site are given below:

Sites 1 and 2: DT	Sites 5 and 6: MTS	Sites 9 and 10: DT
Sites 3 and 4: MPP	Sites 8 and 8: MEA	Sites 11 and 12: MPP

Sites 1-8 were later encapsulated with 4526. Sites 9-12 were pull tested. The pull test results are given in order: 17.86 lb, 24.78 lb, 21.44 lb, and 24.81 lb.

31. Bonding, Encapsulation, and Cleaning Tests 7/8/97.

22 chips were bonded using various encapsulation, UV ozone cleaning and age tests. The table below summarizes the conditions and pull test results where applicable.

Site	Condition (Temp in C; Time in sec; Force in gm)	Pull Force, lb
1	Bond Temp-315/120, Force-700gm, dwell-60sec, Lift Temp-70, wafer 24	NA-encap. w/ 4526
2	Bond Temp-315/120, Force-700gm, dwell-60sec, Lift Temp-70, wafer 24	NA-encap. w/ 4526
3	Bond Temp-285/120, Force-700gm, dwell-60sec, Lift Temp-70, wafer 12	19.91
4	Bond Temp-285/120, Force-700gm, dwell-60sec, Lift Temp-70, wafer 12	21.48
5	Bond Temp-285/120, Force-700gm, dwell-60sec, Lift Temp-70, wafer 13	19.96
6	Bond Temp-285/120, Force-700gm, dwell-60sec, Lift Temp-70, wafer 13	NA- debonded
7	Bond Temp-315/120, Force-700gm, dwell-60sec, Lift Temp-70, wafer 20	16.99
8	Bond Temp-315/120, Force-700gm, dwell-60sec, Lift Temp-70, wafer 20	22.81
9	Bond Temp-315/120, Force-700gm, dwell-60sec, Lift Temp-70, wafer 25	15.97
10	Bond Temp-315/120, Force-700gm, dwell-60sec, Lift Temp-70, wafer 25	NA-debonded
11	Bond Temp-315/120, Force-700gm, dwell-60sec, Lift Temp-70, wafer 26	21.57
12	Bond Temp-315/120, Force-700gm, dwell-60sec, Lift Temp-70, wafer 26	15.79
13	Bond Temp-315/120, Force-700gm, dwell-60sec, Lift Temp-70, wafer 25	5.17
14	Bond Temp-315/120, Force-700gm, dwell-60sec, Lift Temp-70, wafer 26	16.82
15	Bond Temp-315/120, Force-700gm, dwell-60sec, Lift Temp-70, wafer 20	22.5
16	Bond Temp-315/120, Force-700gm, dwell-60sec, Lift Temp-70, wafer 20	17.02
17	Bond Temp-315/120, Force-700gm, dwell-60sec, Lift Temp-70, wafer 25	17.79
18	Bond Temp-315/120, Force-700gm, dwell-60sec, Lift Temp-70, wafer 25	17.99
19	Bond Temp-315/120, Force-700gm, dwell-60sec, Lift Temp-70, wafer 25	22.72
20	Bond Temp-315/120, Force-700gm, dwell-60sec, Lift Temp-70, wafer 25	NA-Encap w/ 4526
21	Bond Temp-315/120, Force-700gm, dwell-60sec, Lift Temp-70, wafer 25	NA-Encap w/ 4526

22	Bond Temp-315/120, Force-700gm, dwell-60sec, Lift Temp-70, wafer 25	NA-Encap w/ 4526

32. Process Development Meeting 7/9/97

Participated in a project review and planning meeting with IBM Endicott.

33. Bonding, Pull and Encapsulation Tests 7/14/97

Bonded chips with 315/120 degrees C bonding temperature, 50/50 degrees C idle temperature, 700 gm of bonding force, 60 seconds bonding time, 70 C lift off temperature. The chips used were from wafer 26, stitch paste C, and had 3 pass screening with no plasma cleaning. Both bonds were encapsulated with Recap for resistance vs. curing time tests.

34. Bonding and Encapsulation For Various Tests 7/18/97

Bonded 22 chips using various encapsulation, aging, bonding time adhesion enhancing, and plasma cleaning process steps. The sites and the conditions used are given in the table below.

Site	Condition (Temp in C; Time in sec; Force in gm)
1,2	Bond Temp-315/120, Force-700gm, dwell-60sec, Lift Temp-70, wafer 24 board has MPP applied 3%, wafer 26, stitch chips w/ paste C, pull tested
3,4	Same as above but encapsulated with 4526 and cured at 80 degrees. C.
5,6	Same as above but with wafer 25, stitch chips
7,8	Same as above but with wafer 20 blank chips that had been refrigerated
9,10	Same as above but with wafer 26 chips and encapsulated with 4526 and cured at 150 degrees C.
11-14	Same as above but sent out to have encapsulated and microwave cured
15-18	Same as sites 5.6
19-22	Same as above but with 60 sec bonding time
23,24	Same as sites 9 and 10

The pull test results from the pertinent sites are given in the table below.

Site	Pull Force, lb		Site	Pull Force, lb
1	18.65		17	18.85
2	13.93		18	22.16
7	23.26		19	22.16
8	18.24		20	NA-debonded
15	19.18		21	12.17
16	16.57		22	17.28

35. Bonding and Encapsulation Tests 7/23/97

Bonded 2 chips to study encapsulant flow times. System settings used were 50/50 degrees C idle temperatures, 385/120 degrees C bonding temperatures, 30 sec bonding time, 700 gm bond force, and 70 degrees C lift off temperature. The two bonded chips were encapsulated with Hysol 4511. The flow times were within 2 minutes

36. Bonding and Encapsulation Tests 7/24/97

Bonded more chips with the settings used on 7/23 for encapsulation performance study. The table below lists the various sites with the encapsulant, cure temperature and cure times.

Site	Condition (Temp in C; Time in sec)
7,8	4511, cured at 80 C for 7 hours
15,16	Matsushita, cured at 80 C for 6.5 hours
5,6	4511, cured at 100 C for 6.5 hours
13,14	Matsushita, cured at 100 C for 6.5 hours
3,4	4511, cured at 130 C for 6 hours
11,12	Matsushita, cured at 130 C for 4 hours
9,10	Matsushita, cured at 150 C for 4 hours
17,18	4511, cured at 150 C for 3.5 hours, used blank chips from wafer 22
19,20	Matsushita, cured at 150 C for 3.5 hours, used blank chips from wafer 22
21,22	Saved for rework study, used blank chips from wafer 22
23,24	Saved for CR vs. Strain test, used blank chips from wafer 22
25,26	Matsushita, cured at 150 C for 2.5 hours

37. Bonding and Encapsulation Tests 7/31/97

Bonding and encapsulation tests were done with 12 chips. Some degrees of the chips were cured with a 3 lb load. The bond settings were bond temperatures of 315/120 degrees C, idle temperatures of 50/50 degrees C, bonding force of 700 gm, a 30 second bonding time, and a lift off temperature of 70 degrees C. The table below gives the encapsulant, cure temperature, cure time and chip types used for the various sites.

Site	Condition (Temp in C; Time in sec)
1,2	Hysol 4511, cured at 130 C, wafer 26, paste C chip
3,4	Matsushita, cured at 150 C, wafer 26, paste C chip
5,6	Hysol 4511, cured at 130 C with 3 lb load, wafer 26, paste C chip
7,8	Hysol 4511, cured at 130 C with 3 lb load, wafer 26, paste C chip
9,10	Matsushita, cured at 130 C, wafer 27, paste C stitch
11,12	Matsushita, cured at 130 C, wafer 28, paste C stitch

38. Bonding and Encapsulation Tests 8/5/97

Bonding and encapsulation tests were done with 8 chips. The bond settings were bond temperatures of 315/120 degrees C, idle temperatures of 50/50 degrees C, bonding force of 700 gm, a 30 second bonding time, and a lift off temperature of 70 C. Site 7 and 8 had an upper bond temperature of 330 degrees C. The sites with the wafers used are given below.
Sites 1-3: Wafer 27 stitch with 2 passes of screening
Sites 4-6: Wafer 28 stitch with 2 passes of screening
Sites 7-8: Wafer 26 stitch with 3 passes of screening.

39. Second T1 Build 8/7/97

Bonded and encapsulated wafer 26's stitch chips with the following settings: bonding temperatures of 315/120 degrees C, idle temperatures of 50/50 degrees C, bonding force of 700 gm, bonding time of 30 sec, lift off temperature of 70 C, Matsushita encapsulant, 77 degrees C underfill temperature, and 150 degree C cure temperature for 1.5 hours. For this 2nd T1 build 26 chips were bonded, encapsulated, and cured.

Further bonds and pull tests were done for future rework studies with a rework encapsulant. The bonds performed are summarized below.

- 2 bonds with the above settings using wafer 27 were encapsulated and cured.
- 4 bonds, with the above settings using wafer 20. 2 sites were encapsulated and cured while the other sites pull tested on 8/11/97
- 4 bonds, with the above settings using wafer 12. 2 sites were encapsulated and cured while the other two were pull tested on 8/11/97
- 10 bonds, with wafer 22 using the above settings except that 2 bonds had bonding temperatures of 315/120 C, 4 had 330/120 C, and 4 had 357/120 C. 2 sites were encapsulated and cured while some of the others were pull tested on 8/11/97. Note that the sites that had bonded at 315/120 C were debonded at 185 C for rework study.

40. Bonding and Rework Tests 8/8/97

Rebonded 2 sites that had been debonded on 8/7/97. Rebonded with wafer 22 blank chips with the same settings that were used on 8/7/97. Also took two arbitrary boards from past bonding and pull tests and rebonded wafer 22 blank chips with the same settings as above. The boards were from a lot that had been bonded and pull tested on 6/24/97.

41. Bonding, Rework and Pull Tests 8/11/97-8/13/97

Pull tested the boards that had been bonded on 8/7/97 and 8/8/97. The various sites and pull test results are given in the table below.

Site	Condition (Temp in C, Time in sec; Force in gm)	Pull Force, lb
1	Wafer 12 from bonding work on 8/7/97	17.56
2	Wafer 12 from bonding work on 8/7/97	19.97
3	Wafer 20 from bonding work on 8/7/97	12.02
4	Wafer 20 from bonding work on 8/7/97	14.16
5	Wafer 22 from bonding work on 8/7/97 with the 315/120 C bond temperatures	16.3
6	Wafer 22 from bonding work on 8/7/97 with the 315/120 C bond temperatures	16.99
7	Wafer 22 from bonding work on 8/7/97 with the 330/120 C bond temperatures	20.61
8	Wafer 22 from bonding work on 8/7/97 with the 330/120 C bond temperatures	17.32
9	Wafer 22 from bonding work on 8/7/97 with the 347/120 C bond temperatures	19.81
10	Wafer 22 from bonding work on 8/7/97 with the 347/120 C bond temperatures	21.45
11	Wafer 22 from rebonding work on 8/8/97	11.81
12	Wafer 22 from rebonding work on 8/8/97	13.86

13	Wafer 22 from rebonding work on 8/8/97	14.3

42. Bonding Tests With Modified System 10/17/97

8 sites were bonded, the alignment inspected with X-ray imaging, and later pull tested. The settings used idle temperatures of 70/70 degrees C, bonding temperatures of 315/120 degrees C, bonding force of 700 gm, bonding time of 30 sec., and lift off temperature of 70 C. Specific settings, alignment and pull test results are listed below.

Sites 1,2: Blank chips from wafer 19 with paste C; X-ray showed excellent placement. Chip pull results were 20.5 lb, and 21 lb.

Sites 3,4: Stitch chips from wafer 33B; X-ray images showed acceptable placement alignment. Chip pull results were 14.81 lb, and 17.81 lb.

Sites 5,6: Blank chips from wafer 19 with paste C; X-ray image showed acceptable placement results. Sent the sample bonds to IBM Endicott for contact resistance measurements.

Sites 7,8: Stitch chips from wafer 33B; X-ray images showed acceptable placement results. Sent the sample bonds to IBM Endicott for contact resistance measurements.

43. Stitched Chip Bonding Tests 10/29/97

Bonded and pull tested 4 chips sites. The sites were bonded with idle temperatures of 70 degrees C, bonding temperatures of 315/120 degrees C, bonding force of 700 gm, and bonding time of 30 sec. The boards for all the sites had been baked at 125 degrees C for about 1 hour. Below is the list of the sites and the pull test results.
Site 1: Bonded with wafer 33B, stitch chip; bond broke while adhering the pull test peg on.
Site 2: Bonded with wafer 33B, stitch chip; bond broke while adhering the pull test peg on.
Site 3: Bonded with wafer 19, blank chip, 18.71 lb pull test result.
Site 4: Bonded with wafer 19, blank chip, 17.02 lb pull test result.

44. Bonding, Cleaning, and Pull Tests 11/5/97-11/7/97

Bonded and pull tested 12 chips sites. The sites were bonded with idle temperatures of 70 degrees C, bonding temperatures of 315/120 degrees C, bonding force of 700 gm, and bonding time of 30 sec. The boards for all the sites had been baked at 125 degrees C for about 1 hour. Below is the list of the sites and the pull test results.

Sites 1,2: Bonded with card as is and blank chips from wafer 19. Pull test results were 11.90 lb, and 21.20lb.
Sites 3,4: Bonded with card that was cleaned and with blank chips from wafer 19. Pull test results were 25.37 lb and 21.73 lb.
Sites 4,5: Bonded with card as is and stitch chips from wafer 32. One site broke before pull testing, the other broke at .85 lb.
Sites 6,7: Bonded with card that was cleaned and stitch chips from wafer 32. Pull test results were 1.01 lb and 1.89 lb.
Sites 7,8: Bonded with card that was treated with MPP and stitch chips from wafer 32. Both sites

broke before pull test results.
Sites 9,10: Bonded with cards and chips that were treated with MPP and stitch chips from wafer 32. Both sites broke before pull testing.

SECTION V: COMPUTER AIDED COST SIMULATION TOOL

A. Overview of Investigation

A project was undertaken through the Department of Systems Science and Industrial Engineering at Binghamton University whose purpose was to create a Computer Aided Cost Estimation (CACE) tool and animated simulation program. The deliverable of the research work allows various aspects of the total cost of implementing an PMC based flip chip attachment to be compared with solder based attachment processes.

The CACE tool helps in the understanding of the business case and consequent rationale behind "selling" the PMSP methodology to industry. The relatively complex relationships between the process and processing variables which affect the operational cost are more easily studied through this tool.

By allowing a potential user of the PMC technology to input those variables specific to his anticipated product and factory operating conditions, direct comparisons between the solder and PMC approach for flip chip attachment can be made. Since the input is specific to each customer and assembly application, the results are more readily understood, with a consequently high degree of trust in their results.

The tool is not tied to a specific vendor of deposition machinery and allows the details of processing speed and hardware cost to be entered by the customer. A variety of scenarios can thus be investigated including varying the number of substrates per panel, number of electrical components of differing types per substrate, etc.

The Technical Report submitted by the personnel from Binghamton University follows in this section, with two technical papers presented on the topic immediately following the Technical Report.

In addition to the work to produce the software tool(s), a graduate Masters thesis was produced by Selva Paramasivan, a graduate student working under the guidance of Binghamton University Professors and the members of the DARPA project team. That thesis entitled: **A Computer-Aided Cost Estimation System for Flip Chip attach Alternatives**, can be obtained through the Binghamton University Industrial Engineering Department.

Justification of ECA Use in SMT Assembly via Computer-Aided Cost Estimation and Animated Simulation

A Final Technical Report Submitted To

Universal Instruments Corporation
Binghamton, New York

December 1996

D.L. Santos, Ph.D. and K. Srihari, Ph.D.
Department of Systems Science and Industrial Engineering
Binghamton University
Binghamton, NY 13902-6000

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Report Summary

The objective of this research project was to develop a user friendly computer aided cost estimation (CACE) system which compares the costs of PCB assembly using an electrically conductive adhesive (ECA) process against a variety of solder-based methods for flip chip attach (FCA). The solder-based processes selected for comparison are the Solder Jetting (SJ), Solder On Chip (SOC), and Solder Plating (SP) methods. The CACE system is a product-specific tool which will allow an informed user to input various, pertinent production information (e.g., production hours available, labor rates, product complexity, material costs. etc.) and provides an estimate of production costs for the different FCA methods. This system estimates the cost taking into consideration the activities performed in the Assembly house alone; this is compared against the previous system which estimates the production costs taking into account three major processing stages - board preparation, wafer preparation, and PCB assembly. The improved CACE system was developed in Microsoft Excel 4.0 (as it is highly portable). This project was a sub-contractual effort created for a jointly investigated (Universal Instruments Corporation and International Business Machines Corporation) DARPA-sponsored research grant (TRP Project #DE-FC-04094AL98817) for ECA viability. The budget for the work performed by this Binghamton University team was provided by Universal Instruments Corporation.

Introduction

Universal Instruments Corporation (UIC) and International Business Machines Corporation (IBM) are co-investigators of a DARPA-sponsored research grant to study the viability of using a newly (IBM) developed thermoplastic electrically conductive adhesive (ECA) for flip chip on board (FCOB) interconnections. In this project, UIC is developing the equipment set necessary to use the new material and IBM is continuing with R&D in the area of ECA material improvement. As with the introduction of any new technology or process, economic viability is crucial to its success. This work comes as a sub-contractual effort performed by Binghamton University (BU) to aid in the determination of the economic viability of using ECA for flip chip attach (FCA) versus a variety of solder-based attach methods. The BU team consisted of Dr. D.L. Santos, Dr. K. Srihari, and Mr. Selva Paramasivan (graduate research assistant). This project is directly related to a previous UIC-sponsored project, which focused in developing a software tool in a spreadsheet to estimate the cost of a product[1]. This project began in June 1996 and is now ending in December 1996.

The current software tool is developed in Microsoft Excel 4.0 which provides the user with dialog boxes making the tool extremely user friendly. The tool also provides the user with graphical reports. In the new effort, additional features such as Rework and Yield are taken into consideration. A simulation model is developed in Arena2.1 to validate the outputs (in terms of the equipment sets necessary) which are generated by the CACE tool. This effort was performed by the same co-principal investigators. It was also decided by the principals (both at UIC and IBM) to compare ECA versus a variety of solder-based methods. The methods considered are solder plating (SP), solder jetting (SJ) and solder-on-chip (SOC). A description of these three methods appears in a paper by Paramasivan et al. (1996)[2] and is found in the appendix of this report.

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1 "An Improved Cost Estimation System for Flip Chip Attach Alternatives", D.L. Santos and K. Srihari, Co-Principal Investigators, Final Report Provided to UIC, August 15, 1996.

2 S. Paramasivan, D.L. Santos, M. Snyder, and C. Woychik (1996) "A Computer Aided Cost Estimation System for Flip Chip Attach Alternatives". Paper presented at the International Conference on Industrial Engineering Applications and Practice, Houston, TX, December.

Research Methodology

The research work was a conglomeration of the following three activities:

1. Development of a user friendly CACE system;
2. Case Studies and Sensitivity Analyses;
3. Validation of the CACE system via Animated Simulation.

The major cost factors considered for this improved version are the following:

1. Equipment Cost;
2. Material Cost;
3. Labor Cost;
4. Utility Cost;
5. Rework Cost.

As the placement machine is one of the most expensive pieces of equipment in the assembly line, the model also provides the user with a separate module to define the placement machine of his choice. In addition to the above factors, throughput variables (cycle times, production schedules, etc.) are also taken into consideration to estimate the number of equipment sets needed to meet the demand. For convenience, default values are provided in the model, which are obtained from UIC, IBM, and several other vendors. The CACE tool generates the number of equipment sets needed to meet the demand, which can then be validated by using the developed simulation model.

FCA-CACE System

The Computer Aided Cost Estimating (CACE) system for the cost comparison of the ECA process versus the solder based processes is developed in Microsoft Excel Version 4.0. Dialog boxes are developed to facilitate the CACE system use by the decision-maker. Dialog boxes will allow the decision-maker to be prompted for only the limited/pertinent information (like production hour's available, annual demand, etc.) which is needed for analysis. This makes the CACE system more user friendly as opposed to the earlier version.

The CACE system, after receiving all the required inputs, calculates the different costs associated with the four different assembly processes. An automatic graphical report-generating module is embedded in the CACE system for a better understanding of the behavior of the different variables. The CACE system also informs the user of the assumptions made in developing the model before running the model.

After the model is run, the user is prompted whether to continue to a module which enables the user to change the number of equipment sets needed (at the various processing stages) and see the cost variation in the product instantly with all other information taken from the model. This module is useful to the user when attempting to validate the numbers generated by the CACE tool using the simulation model. The processing stages in the ECA- and Solder-based versions are represented in Figures 1 and 2, below.

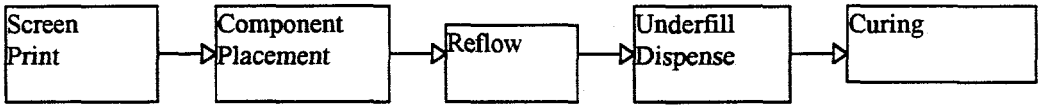

Figure 1. Solder-based FCA Process Flow Diagram

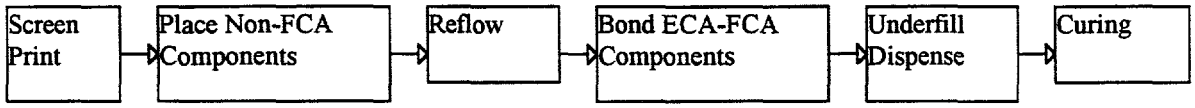

Figure 2. ECA-FCA Process Flow Diagram

The above figures represent the major assembly steps -- other stages considered in the model include cleaning and testing. The reason, of course, that the two process flows are different is that in the use of ECA, the flip chips are bonded (and thus cannot be placed via standard GSM-C4 placement machines). Whereas in solder-based FCA, the GSM-C4 machine can place both the flip chips as well as other surface mount components.

Animated Simulation Model

The entire manufacturing shop floor is considered in the simulation model, which is developed in the simulation software Arena2.1. The main objective in developing the simulation model is to check whether the process, with the number of equipment sets as generated by the CACE system, could meet the given demand in their respective due dates. The CACE system estimates the number of machines at each stage, which are necessary to support production. One thing, which is not performed by the CACE system, is the ability to validate if these (possible) multiple machines at the various stages, when interconnected can operate as a manufacturing system as a whole. The simulation model will help us verify if the system is functioning as a whole. The entire assembly line is typically connected by a conveyor system. As it takes the transient responses into consideration, it gives a more realistic view of the whole system. When the simulation model is run, a decision maker can actually see the PCBs traveling down the assembly line, the

machines being idle, the PCBs waiting in the queue to get processed, etc.. Furthermore, at the end of the simulation run, outputs are obtained to report pertinent validation results like the number of PCB's produced per period, number of PCB's in the queue for bottleneck operations (such as Underfill and Placement), etc..

The boards are assumed to enter the system at a constant rate. Each machine is considered a resource and each stage is considered a Server in the model. A Server might have 2 or 3 resources based on the number generated by the CACE tool. Information such as the number of resources per server, processing time for a board at a specific resource is to be manually entered by the user. Once the information is provided to the model it performs the simulation for the period specified by the user and provides the report.

Case Studies

During the project's duration, the Binghamton University team has performed three case studies. The product types in these case studies are a single chip module laminate (SCM-L), a multi chip module laminate (MCM-L), and a board taken from a major camera producer's product (with three flip chips). A discussion of these case studies has been presented in previous DARPA meetings and it also appears in a forthcoming paper by Santos et al. (1997)[3]. A copy of this forthcoming paper also appears in the appendix of this report.

Conclusions and Future Research

At this point in time, the CACE tool is robust and we have met the major objectives of the research as follows:

1. A user-friendly interface is created;
2. Graphical and sensitivity analysis reports are instantly generated;
2. Simulation models are developed to validate system outputs;

While it may seem that it is narrower in focus (in that it looks at the assembly house only), board preparation and chip preparation are still included. They are included because the user now has the ability to input the cost of supplied chips and boards (and these costs will be different given the different attach methods). We have also included the effect of yield and rework in the cost estimation.

There are three distinct areas where extension of the Binghamton University team's efforts is

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[3] D.L. Santos, S. Paramasivan, M. Snyder, and C. Woychik (1997), "A New Electronics Packaging Process: Justification via Cost Estimation and Animated Simulation". Paper to be presented at the Industrial Engineering Research Conference, Miami, Fl, May.

valuable. First of all, since the DARPA activity is continuing, it is a very reasonable thing to maintain our relationship as we can address suggested changes (or other considerations) in the model if and when they arise. Secondly, significant finding from the SCM-L/MCM-L studies is that the wafer processing (as calculated in the previous CACE model) may be revisited and reengineered (and thus new cost estimations provided). Thirdly, a large-scale study should be performed to analyze a wide variety of product types to get a broader view of the competitiveness of ECA flip chip attach.

APPENDIX

Paper 1:

S. Paramasivan, D.L. Santos, M. Snyder, and C. Woychik (1996) "A Computer Aided Cost Estimation System for Flip Chip Attach Alternatives". Paper presented at the International Conference on Industrial Engineering Applications and Practice, Houston, TX, December.

Paper 2:

D.L. Santos, S. Paramasivan, M. Snyder, and C. Woychik (1997), "A New Electronics Packaging Process: Justification via Cost Estimation and Animated Simulation". Paper to be presented at the Industrial Engineering Research Conference, Miami, Fl, May.

A COMPUTER AIDED COST ESTIMATION SYSTEM FOR FLIPCHIP ATTACH ALTERNATIVES

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Abstract

The electronics manufacturing industry is posed with a number of challenges (like product miniaturization) to meet the high expectations of the customers in today's market. Manufacturing cost is always a major factor to be considered in the process of decision making. Flipchip attach - a relatively new technology for use in product miniaturization - is still in its early stages of implementation; there is a need for justifying its use (in terms of cost) to prove it competitive. This paper describes the development of a product specific Computer Aided Cost Estimation (CACE) tool/system which helps the user compare the costs of utilizing conductive adhesives for flipchip attach (FCA) versus three different solder-based FCA methods.

Keywords

Electronics manufacturing, flipchip attach, conductive adhesives, cost estimation.

Introduction

The drive to miniaturize electronics products has resulted in an increased interest in area-array surface-mount devices such as flipchip attach (FCA) components. The benefits of FCA components include reduced size, better electrical performance, better thermal performance, higher interconnect density, higher I/Os for a given area, and some material cost savings due to the elimination of the package [1]. The choice of a chip connecting technology can have a significant influence on the cost of the product [2]. The industry is in the process of establishing technologies, which will be required for the next 15 years; thus, the ability to implement these technologies as cost effective and competitive products is in question [3]. While flipchip attach is not a new concept - it originated from the controlled collapse chip connection (C4) technology developed by IBM corporation [4] - it has only in recent years been the center of intense study due to the advances made in the surface mount technology arena. Since FCA is not the standard component-to-substrate interconnection method, the focus of the research is to develop a computer aided cost estimation (CACE) tool to compare the costs of four different FCA interconnecting technologies. These technologies are the following: electrically conductive adhesive (ECA), solder-jetting (SJ), solder-on-chip (SOC), and solder-plating (SP). An overview of each of these technologies is provided below. The approach taken to develop the CACE tool is to identify the activities in three major cost-contributing processing centers for each interconnecting technology considered. The CACE is developed as a set of highly interconnected worksheets in a Microsoft Excel workbook application.

Overview of ECA Flipchip Attach

Simply stated, in place of a solder-based attach method, this method involves creating the interconnection between the chip and the substrate using a conductive adhesive material. This method of flipchip attach aims in making the adhesives conduct electricity by embedding metal particles in them. The most commonly used filler material is silver which increases its cost. IBM's recent interest in this area was stimulated when an application required the interconnection of a tungsten component to copper [5]. There is significant interest in this method of flipchip attach because of its compatibility with a wide range of surfaces. Since it is a newly developed process it is yet to be justified in terms of cost and reliability. An important distinction between ECA and solder-based interconnection is that in the use of

ECA, components must be bonded individually, to create the connections while solder-based interconnections can rely on mass reflow. Based upon the times required to bond the components (and the number of components per product), this can severely affect cycle times and, hence, costs.

Overview of Solder-Jet Flipchip Attach

The standard practice of creating the interconnections between electronics components and the substrate relies on the use of solder as the material for interconnection. One of the major challenges for achieving miniaturization of components lies in the deposition of the amount of solder forming the electrical connection. The standard surface mount application of solder is the screen printing process. For the miniaturization required in FCA, screen printing is unacceptable. As a response, this problem has been addressed by other technologies. The solder-jetting method involves the deposition of solder onto a surface using a controlled dispenser (or jet). At present, the two greatest areas of interest in SJ have been the deposition of solder on fine pitch circuit board pads and the bumping of the wafer (and, therefore, chip) with solder. Since the jetting process is capable of producing very uniform solder balls, there has even been some interest in using jetting to produce solder pastes with precise solder ball size distribution control [6].

Overview of Solder-On-Chip Flipchip Attach

As the name implies, the solder-on-chip process places the solder onto the chip; thus, no solder needs to be deposited on the substrate prior to forming the interconnection. This process is in its nascent stages of implementation. In this process, also known as E-3 (Evaporated Extended Eutectic), the flipchip is attached to organic boards without the need for intermediate eutectic (solder) deposits on the board itself [7]. There are a number of advantages to this process. No special tools or methods are required to either fabricate the evaporated bump or surface mount the chips to the boards and no special preparation of the board is necessary. Additionally, it appears that this same E-3 technology can be adapted for joining chips to a variety of other substrate materials. By providing eutectic melting on the bump (and, therefore, the chip) itself, direct joining to organic assemblies are achieved without special processing at the board level. This leads directly to cost reductions and improved wirability at assembly [7].

Overview of Solder-Plated Flipchip Attach

Flipchip applications having extremely fine pitches of 8-10 mils, pose a serious problem of printing eutectic solder onto the pads to form interconnection during the assembly process. This problem is overcome by coating the board pads with solder prior to assembly. The most commonly adopted process for bumping the board in the industry today is the electroplating (or solder-plating) method. The amount of solder deposited is quite critical. The disadvantage of the process is that the electroplating process is not automated which makes the human error factor more pronounced [2]. The 2-4 mil thick solder on the attachment pad takes on a domed shape and must be flattened (a.k.a., coined) prior to placement of the component because solder balls cannot be reliably placed on domed surfaces [8].

Cost-Contributing Processing Houses

The entire manufacturing process studied herein is classified into three cost-contributing houses. We refer to these as the "wafer house," "board house," and the "assembly house." The "wafer house" consists of the processing steps required to prepare the wafer (the wafer is that which is diced to make the individual flipchips) for the PCB assembly. Depending on the interconnection application, different

materials and steps are performed upon the wafer. The "board house" consists of the processing steps required to prepare the substrate for the PCB assembly. Similarly, the steps and materials differ for the different interconnection applications. The "assembly house" refers to the processing steps in the PCB assembly. As discussed above, the ECA components must be bonded to the substrate and thus requiring a separate, additional processing stage in the PCB assembly house. The different process steps in each house identified by interactions with engineers in IBM-Endicott and Universal Instruments Corporation are provided below. The major cost drivers studied in this report are the equipment cost, material cost, labor cost and utility cost - all differently contributing in the various cost-contributing processing houses.

Tables 1-3 provides the processing steps required at the different processing houses for each interconnection technology. An attempt is made in these tables to provide the unfamiliar reader with the number/type of processing steps. It is of considerable note that the different processing steps require different materials, cycle times, equipment sets, etc. While these are all incorporated into the cost model, this paper will not - due to the avoidance of a discussion more lengthy than would be allowed here - delineate or more thoroughly define these other differences.

Table 1. Wafer House Processing Steps

ECA	SOC	SJ	SP
Electroless Process	Evaporation(Solder)	Evaporation(Solder)	Evaporation(Solder)
Screen Print (ECA)	Reflow	Reflow	Reflow
Cure	Evaporation (Tin)	Testing	Testing
Wash	Inspection	Dicing	Dicing
Testing	Dicing	Packing	Packing
Dicing	Packing		
Packing			

Table 2. Board House Processing Steps

ECA	SOC	SJ	SP
Electroless process	Entek process	Entek process	Cleaning
		Solder jetting	Seed/Add plate
		Coining	Inspection
			Immersion Tin/Lead
			Electroplating Sn/Pb
			IInd immersion
			Cleaning
			Coining

Table 3. Assembly House Processing Steps

ECA	SOC	SJ	SP
Screen print*	Screen print*	Screen print*	Screen print*
Mounting comps.*	Mounting comps.**	Mounting comps.**	Mounting comps.**
Reflow*	Reflow**	Reflow**	Reflow**
ECA comp. bonding	Cleaning***	Cleaning***	Cleaning***
Underfill	Underfill	Underfill	Underfill
Curing	Curing	Curing	Curing
Testing	Testing	Testing	Testing

* The screen-printing/mounting/reflow steps concern the placement of solder onto the substrate for the non-FCA (or standard surface mount) components.

** Includes both FCA and non-FCA components.

*** A cleaning step may be required with the use of a solder-based method due to the amount of flux which might be required for use in creating the FCA interconnects.

FCA-CACE SYSTEM

The FCA-CACE system is developed in Microsoft Excel (5.0) in a workbook format. The workbook has the system incorporated as 13 interlinked worksheets. The FCA-CACE system is product specific. In other words, a user must input specific information about a product for which cost is being estimated and compared. The first sheet, which is named "common", receives the information which is common to all the methods considered for comparison. Some information received includes, but is not limited to, the following:

- production hours available (in the different houses):
  - #shifts/day, #hours/shift, #production days/year;
- product specific information:
  - #FCA components, #FCA I/O's, #non-FCA components;
  - annual demand, #products/PCB panel;
  - number of locating fiducials per panel and per product;
- ECA bonding rate, surface mount placement rates;
- unit costs for equipment (default values provided);
- floor space usage per unit equipment (default values provided) ;
- unit costs for materials (default values provided);
- labor rates.

Upon each user entry into the FCA-CACE system, re-calculations are performed. Important modules developed in the system are cycle time estimation modules for placement rates and underfill material dispense - two bottlenecks in the PCB assembly house. For example, costs are instantly recalculated and updated if the user changes the ECA bonding rate from 30 seconds to 10 seconds. The placement machines and bonding machines are based upon Universal Instruments Corporation's (UIC's) GSM (general surface mount) platform which is becoming an industry standard.

The four worksheets (2-5) subsequent to "common" provide a detailed cost-breakdown summary for each interconnection method. Following these, four worksheets (6-9) provide detailed cycle times and throughput breakdown information for each interconnection method. Worksheet 10 provides a side-by-side summary of the costs of the four different interconnection methods. The eleventh worksheet contains a set of graphical charts which illustrate the cost breakdowns. Assumptions for the model use are provided in the twelfth worksheet. The last worksheet contains a detailed set of hints for the user of the FCA-CACE system.

As aforementioned, the cost adders incorporated in this model concentrate on the following four areas (for each processing house): equipment costs, material costs, labor costs, and utility costs. The equipment costs are a function of the estimated equipment sets required to meet production (based on cycle times, annual demands, and production hours available) multiplied by the unit equipment costs. The material costs are a function of the unit material costs, production hours available, and annual demand. Labor costs are a function of the number and type of personnel (distinctions are made between operations personnel, inspection personnel, and maintenance personnel), production hours available, and labor rates. Utility costs are estimated as a function of utility costs ($\$/ft^2$) multiplied by the number of individual equipment sets which is multiplied by their unit floor space.

Summary and Future Work

The CACE system is developed as a product specific tool to understand the cost competitiveness of the ECA flipchip attach method against solder-based methods for a user defined product. A very important feature is its ability to help target areas which need process optimization; an example of this is its ability to aid developers/engineers at IBM and UIC of the importance the ECA bonding rate on the cost per product. Refinements are currently being made to the system to incorporate other pertinent factors like

yield- and rework-related costs. Furthermore, validation of the system's estimation of equipment sets is being performed via (animated) simulation modeling and analysis.

Acknowledgments

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A New Electronics Packaging Process: Justification via Cost Estimation and Animated Simulation

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Abstract

The electronics manufacturing industry is constantly faced with challenges to keep abreast of customer expectations. An ongoing challenge is product miniaturization. Different electronics packaging technologies are emerging which address product miniaturization; one such technology is flip chip attach (FCA) in the surface mount technology (SMT) arena. Flip chip attach concerns the mounting (typically via soldering) of the integrated circuit (IC), or chip, directly to the printed circuit board (PCB) substrate without first encasing the IC within an electronics package. While FCA technology was invented over 40 years ago (with IBM's C4 technology), it has only recently begun to gain increased usage. A new electrically conductive adhesive (ECA) is being developed by IBM for use as the FCA material. In order to justify this new material's use, computer aided cost estimation (CACE) is being utilized to assess the costs of this technology against a variety of solder-based (as the standard attach material) methods. The CACE system as well as the (animated) simulation modeling and analysis used as a validation tool for the CACE system outputs.

Keywords

Electronics Manufacturing, Cost estimation, Animated Simulation, Flip Chip Attach.

Introduction

As microelectronics packaging continues its move toward miniaturization, it is apparent that conductive polymer flip chip interconnection can provide reliable, high-density packaging at a lower cost than alternative technologies (Estes and Kulesza, 1995). Although the previous statement touts conductive adhesives as being a low-cost alternative, potential low-cost claims for this process have yet to be substantiated especially since conductive adhesive use is not widespread and resides more in the developmental area. This effort is taken to understand the cost behavior of a newly developed electrically conductive adhesive (ECA) material for flip chip attach (FCA0 in a PCB assembling facility by developing a computer aided cost estimation (CACE) system. The solder based processes considered for comparison is the following: Solder Jetting (SJ), Solder-On-Chip (SOC) and solder plating (SP). Paramasivan et al. (1996) provides a detailed description of these three solder-based methods. To summarize the distinctions, the three processes differ in the way the solder material is presented for the attach process. In SJ. the pads on the substrate (upon which the leads (or I/O's) of the flip chip components are attached) are deposited with solder via a controlled dispenser (or jet). In SP< the pads on the substrate have solder material placed on them via an electroplating process. In SOC, the solder appears on the chip via a combination of tin (Sn) and lead (pb) depositions. Thus, in the SJ and SP processes considered herein, the solder is placed onto the substrate; SOC has the solder material placed onto the integrated circuit itself.

Though the assembly process is the same for all of the aforementioned solder processes, the die (or flip chip) and the laminate (a.k.a., PCB substrate or board) cost varies significantly – this is because the three methods require different types of processing for the wafer (or chip), board, and PCB assembly areas. While there are, correspondingly, three major cost contributing houses (wafer or chip level; board preparation level; and PCB assembly-house level) and these houses are considerable factors in the overall cost of flip chip based electronics assemblies (Paramasivan et al., 1996), this CACE system is developed from the PCB assembly house viewpoint. Figure 1 presents a flow diagram of the process steps involved in a solder-based FCA process.

In the figure, the "screen printing" step concerns the deposition of solder (in the "component placement" step, both non-FCA and FCA components are placed onto their respective positions via pick-and-place robotic assembly. The "reflow" step is used to reflow the solder (both the screen-printed solder paste as well as the solder via SJ, SP, or SOC for the FCA components) in an oven to make the

interconnection between the components and the substrate. For FCA components, an additional surface mount assembly process is the dispensing of an underfill material beneath the FCA components for environmental protection and other reliability purposes. After underfill dispense, the underfill material must then be cured.

The flow diagram for ECA-FCA is different since, with the use of a conductive adhesive, the FCA component must be bonded to the substrate (as opposed to being placed onto the substrate followed by a reflow process). It is further complicated in that non-FCA components must be placed on a piece of pick-and-place equipment separately from the robotic machinery that bonds the FCA component. These components must have their solder reflowed prior to FCA placement as the ECA material cannot be subject to the reflow process after it is bonded. The ECA-FCA assembly diagram appears as Figure 2.

The CACE system is a product-specific cost estimation tool for a PCB assembly manufacturer. Major inputs to the system will be the following:

-product specific information;
- -no. of flip chips
- -no. of I/O's per flip chip
- -annual product demand
- -no. of non-FCA components
- -etc.

-production information;
- -number of shifts/day
- -number of working days/year

-cost of supplied chips;

-supplied panels (substrates) cost;

-rework percentage rates.

The user also has the ability of altering certain system values, which have been defaulted. Primary examples of these are equipment costs, number of years for depreciation, and equipment floor space usage (to aid in estimating utility costs), equipment cycle times (e.g., screen printing, pick-and-place, ECA bonding rate, etc.).

The system is developed in Microsoft Excel© as a series of linked spreadsheets-this is discussed in more detail below. Based upon the above information, the system then estimates the required number of different equipment at the various processing stages in the PCB assembly house necessary to meet the production. While it is one thing to estimate the required number of equipment to meet quotas at individual processing steps, it as another thing to have an entire, interlinked system validated by this process. Consequently, these estimates of the CACE system are then validated using simulation models of the entire systems (based upon the various CACE system outputs) developed in the Arena© V.2.1 simulation package.

Cost Factors

The major cost factors that the CACE system considers for the assembly house are the following: equipment cost, materials cost, personnel cost, utility cost, and rework cost. A description of these categories now follows.

Equipment Cost

As aforementioned, the equipment costs are estimated by taking into consideration the number of machine sets needed for the given demand. The cost of the placement machine in the assembly process is calculated by the placement machine cost estimation module and the number of machines needed at each stage to meet the demand is calculated using the cycle time of the process performed in the machine and the total number of working hours available to meet the demand. Cycle times are estimated based on the user-supplied inputs. This helps in getting a feel on the impact of process improvements on cost. (This is an important factor for a newly developed process in that the CACE system will allow the study of process improvement areas). The cost of the stencil and squeegee sets used in the assembly house are also included in the equipment cost taking into consideration its life in terms of panels. The depreciation of all machines for one year is considered as the equipment cost per year. The model uses straight-line depreciation over a fine-year horizon which is user defined (and user-alterable).

Materials Cost

The cost of materials include solder paste, flux, nitrogen, underfill, board (applied with appropriate coating) and bumped wafer. The cost of all the above materials are user defined. Nitrogen used in the reflow oven to enhance solderability is an added cost to the assembly house. Additional costs in the assembly house (above other, traditional surface mount assembly lines) are incurred due to the need for batch processing to cure the underfill material.

Utility Cost

In most cost estimation procedures, a factory burden or overhead is included; the major purpose of this category is to capture (or estimate) overhead. The utility cost is estimated as a function of the floor space usage of all equipment required to meet production multiplied by a floor space utility cost per square foot. The user inputs the annual utility cost per square foot. Utility cost also includes the cleaning cost of the panels as estimated by the number of panels multiplied by a user-defined cleaning cost per panel. The cleaning cost of an assembled board per panel should be estimated by the user by considering a number of factors like the type of flux used in the process, reliability expectations of the product, etc. Also, not all PCB assemblies will require a cleaning step, therefore, the model provides the user with a cleaning option to include or exclude the cleaning cost from the assembly house.

Rework Cost

Rework cost is largely dependent on the type of application being considered. Rework after the underfill process is extremely difficult and expensive. The yield is calculated before the underfill stage and the rework cost is calculated by the user-defined input for the rework cost per die.

Initial Cost

Cost information on the initial set up needed for each process is also provided by the model. The costs incurred in the process of setting up the assembly lines are considered as the initial set up cost. It includes the cost of the equipment sets needed for meeting the demand, system proving cost and the training cost of the labor. System proving costs considers labor and material costs.

CACE system Description

The Computer Aided Cost Estimating (CACE) system for the cost comparison of the ECA process versus the solder based processes is developed in Microsoft Excel© V.4.0. Dialog boxes are developed to facilitate the CACE system use by the decision-maker. Dialog boxes will allow the decision-maker to be prompted for only the limited/pertinent information (like production hours available, annual demand, etc.)

which is needed for analysis. An example dialog box appears as Figure 3. This makes the CACE system more user friendly as opposed to an earlier version as discussed by Paramasivan at al.[1996]. The CACE system, after receiving all the required inputs, calculates the different costs associated with the four different assembly processes. A graphical report-generating module (e.g., pie charts, cost curves, sensitivity analyses, etc.) is embedded in the CACE system for increased understanding of the behavior of the different variables. The CACE system also informs the user of the assumptions made in developing the model before running the model.

Validation Via Animated Simulation

The entire manufacturing shop floor (as reflected in Figures 1 and 2 and including cleaning and testing) is considered in the simulation model which is developed in the simulation software Arena© V.2.1. The main objective in developing the simulation model is to validate the results of the CACE system. An important capability of the CACE system is its ability to estimate, among the variety of processes evaluated, the number of machines at each stage which are necessary to support production. One thing which is not performed by the CACE system is the ability to validate if these (possible) multiple machines at the various stages, when interconnected can operate as a manufacturing system as a whole. Thus, when one must justify an advanced manufacturing investment, it is important to study the entire system and not just separate, individual components [Canada and Sullivan, 1989].

By validating the system as a whole, decision-makers can avoid the pitfalls of the "islands of automation" concept. Succinctly states, these arise when a component functions as expected but failures occur when they are not considered as part of a greater system. Verification via simulation of the system can help avoid these "islands of automation" pitfalls.

Computer simulation will not only help to verify that the system will function, but as an added benefit, the animation will allow these proposed systems to be developed and studied in a virtual environment without having to actually create and study an expensive testing facility. When the simulations are run, a decision maker can actually see the following types of activities: PCBs traveling down the assembly line, machines breaking down, machines being idle, etc. Furthermore, at the end of the simulation run, outputs are obtained to report pertinent validation results like the following: number of PCB's produced per period, percentage machine utilization, etc.

Model Description

The components of the assembly line model are the equipment sets in the different stages of the assembly process. The boards are assumed to enter the system at a constant rate. Each machine is considered a server in the model. The parameters of the server such as processing time for one board, board loading time, board unloading time, MTBF, MTTR, etc., can be defined by the user by just clicking on the module. The entire assembly line is typically connected by a conveyor system.

The model is used to check whether the process with the number of equipment sets as generated by the CACE system could meet the given demand in their respective due dates. The output report generated after the simulation run includes details like the average wait time of the PCB at each stage, maximum and minimum number of PCBs waiting to get processed at each stage, etc.

Case Studies

As discussed above, the CACE system is a product-specific application. Examples of two different case studies are the following: SCM-L/MCM-L and a PCB assembly taken from a camera product.

SCM-L/MCM-L

A Single Chip Module Laminate (SCM-L) is a type of electronics packaging format (e.g., a "plastic ball grid array (PBGA)") which has the IC attached to a small substrate (as in Level I electronics packaging; see Figure 4). The PBGA is then attached (as in Level II electronics packaging) to a PCB assembly (board). A Multi-Chip Module Laminate (MCM-L) is a similar type of package, yet there is more than one chip attached at Level I. In this example, the only components are the IC's (there are no non-FCA components). An analysis was performed to study the costs in assembling the PBGA (both in SCM-L and MCM-L formats) with using ECA vs. Solder as the IC attach material. In the study, PBGA annual volumes were varied from 10 sec. To 5 sec., and the number of chip I/O's varied from 119 to 250 (the number I/O's is a factor when considering SJ since this solder-based method applies solder to the substrate per individual I/O site; whereas the other solder-based methods do not).

Camera Product

An analysis was also performed with a PCB assembly taken from a camera product of a major manufacturer of photographic film and photography equipment. In this assembly, three different flip chips (a total of 60 I/)'s) reside on each PCB along with 11 non-FCA SMT components and volumes were varied from 100,000 to two million.

Case Study Results

For the different case studies, costs per board analyses were developed. With few exceptions, the following rankings (lowest to highest cost) were obtained: SOC, ECA, SJ, SP. It is worth mentioning that in every analysis, ECA is of lower-cost than SP. This is important in that SP is most widely used solder-process for these types of FCA applications; SOC and SJ are still very much developmental. Therefore, ECA has shown cost advantages (at least for the products herein), over the "standard" solder-based method. Simulation of the CACE system outputs verified that production levels could be met with the estimated equipment sets.

Conclusion

This effort has been and continues to be performed as part of an effort to understand the cost competitiveness of the ECA flip chip attach method against solder-based methods for a user defined product. In two major case studies, ECA appears to be a viable cost competitor in that it tends to rank just behind SOC (as the overall low-cost process). The majority of the ECA costs can be attributed to the wafer processing level; i.e., the cost of supplied ECA-bumped chips is more expensive than the cost of SOC style chips. As compared to Solder Plating, ECA has a significant cost advantage. This is an important result in that, while three solder-based methods are analyzed, SOC and SJ are (like ECA) in the developmental stages. Solder Plating is essentially the only method widely used in practice. Another point to consider is that ECA provides non-cost advantages over SP which lend strength to the justification of its use. Two of the major non-cost attributes are that ECA is a lead-free (environmentally friendly) material and, in mounting chip-on-glass (e.g., display) applications, electrically conductive adhesives are more conducive to chip mounting.

Another important feature of the CACE system is its ability to help identify areas of process optimization. For example, one contention was that the cost might be significantly reduced if the ECA bonding rate (defaulted at 10 sec./bond) was reduced to 5 sec./bond. The 10 sec./bond rate is one which appears to be reaching a physical limit (fastest bond time) for the ECA material. In the two case study examples, the move from 10sec. To 5 sec. yielded (essentially) no improvement. Thus, indicating that the ECA material developers need not necessarily spend significant effort in trying to determine if the 10 sec. Barrier could be reduced (for these cases). Further analysis has indicated that the main reason why the 5 sec. Bond rate did not yield substantial improvement for these cases was because the ECA bonding step is not the bottleneck operation; underfill is, for these cases, the bottleneck. While the change to 5 sec. Does, of course, improve the speed in which the parts are bonded, it does not have an effect on the speed of the

underfill step. On cases in which ECA bonding is the bottleneck operation, then it would be of benefit to revisit the bond rate parameter. This type of analysis is an excellent example of the CACE system's utility in this project.

Acknowledgements

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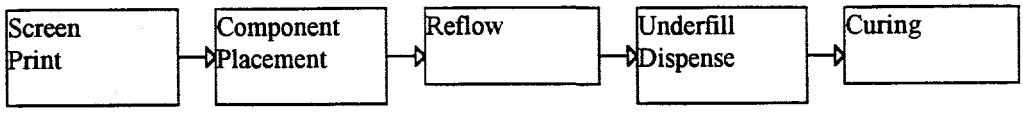

Figure 1. Solder-based FCA Process Flow Diagram

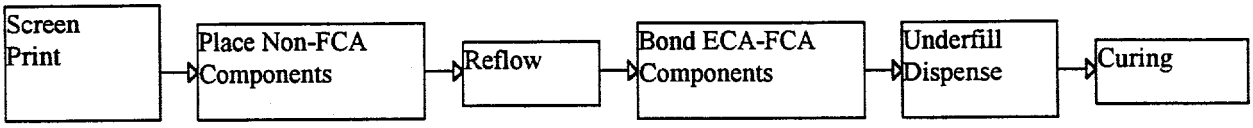

Figure 2. ECA-FCA Process Flow Diagram Figure

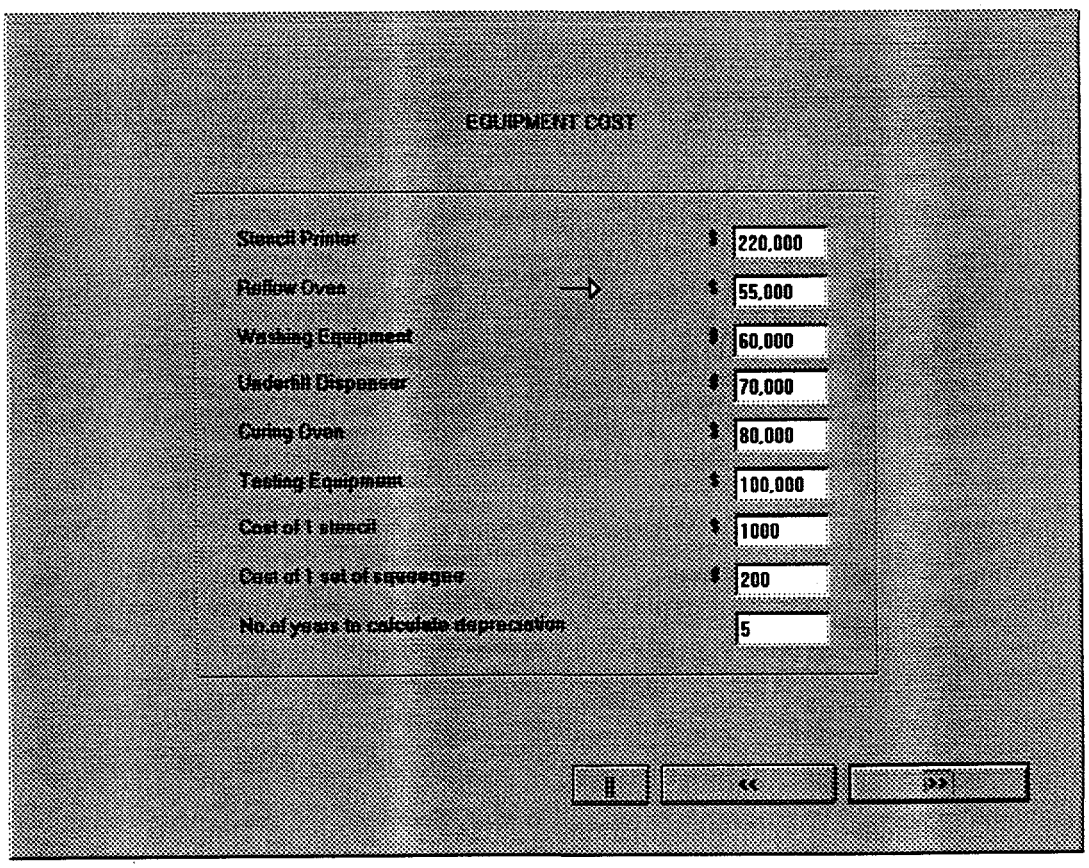

Figure 3; Example CACE System Dialog Box

Level 0: IC chip *Level 1: Packaged Chip* *Level 2: PCB Assembly*

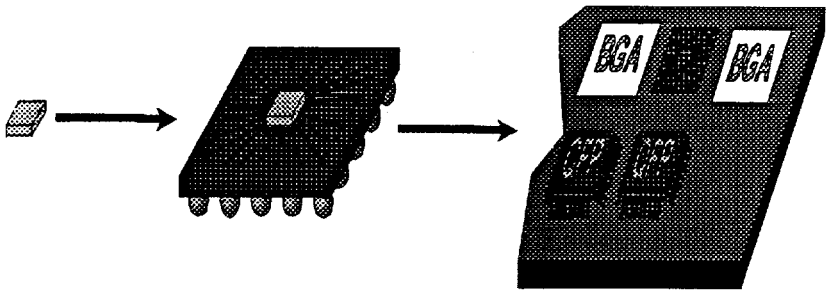

Figure 4. Electronics Packaging Hierarchy

SECTION VI: CONCLUSIONS/FUTURE WORK

A. CONCLUSIONS

As the DARPA PMC project closes, there are several conclusions or inferences which may be drawn as a result of the experimental and development work performed. The latter phases of the project were focused on carrying out PMC bonding process characterization. These bonding tests, carried out in conjunction with the two participating IBM facilities, looked to increase the knowledge base and optimize the process parameters placed under control by the assembly (bonding) machine. Those tests showed positive results in terms of the bonding machine and process being able to create strong, electrically conductive PMC joints. The tests also demonstrated that there remain areas of the process requiring additional development if the process to be transferred to the Electronics Assembly Industry as a viable production process.

At the present time, the use of solder for flip chip attachment is pervasive in the industry. For PMSP material to replace portions of that assembly market, the attributes of the PMSP assembly process must be shown significantly superior to the solder based approach. It will not be good enough that the PMSP process be comparable, it must show that there are sufficient benefits over solder based approaches that industry segments feel compelled to move away from the well known and "comfortable" solder approach to this new PMC approach. The industry will require not only demonstrated performance and total cost viability analysis of the new process, but also a statistically valid set of performance and reliability data.

As a result of the testing carried out at Universal on the Automated PMC Testbed produced under the DARPA contract, the processing parameters showing the highest degree of attached joint strength were the following:

Parameter	**Value**
Chip Idle Temperature	50° C
Substrate Idle Temperature	50° C
Bonding Force	690 grams
Bonding Temperature	315° C
Substrate Bonding Temperature	120° C
Dwell Time	60 sec
Lift Off Temperature	70° C
Total Bonding Cycle Time (Ramp, Dwell, Cool-Down, Lift-Off)	123 sec

In a conventional flip chip solder based assembly process the flip chip is deposited on a pre-fluxed site by the placement machine, and at the conclusion of the placement process, the entire substrate is sent through a reflow oven to melt the solder, creating the joints. It is an example of a sequential placement process followed by a batch reflow process.

The PMC process is sequential inasmuch as the flip chips are placed and bonded one at a time until the assembly process is completed. As a consequence, the bonding time plays a crucial role in the overall time required for substrate population. As an example, the figure below compares the PMSP Process time for assembly with two standard solder based processing modes, the "UFP"

application being for fine pitch components, and the "4SP" being for a lower accuracy, higher speed process.

Task	PMC	Solder (UFP)	Solder (4SP)
Fiducial Find	0.6 sec	0.6 sec	0.6 sec
Pick, Inspect, Place	6.0 sec	6.0 sec	1.3 sec
Flux	N/A	2.0 sec	0.3 sec
Bond: Temperature Ramp	8.0 sec	N/A	N/A
Dwell	38.0 sec	N/A	N/A
Cooldown	20.0 sec	N/A	N/A
Total	**72.6 sec**	**8.6 sec**	**3.2 sec**

From the figures shown in the above table, there exists a substantial difference between the assembly time required by the PMC process as it now exists, and solder based processes against which it competes. In terms of the partitioning of the problem space, the times taken for the temperature ramp up, and the time to cool down, can be attacked by Universal by design refinement of the heating tools. The time at temperature needed to create strong PMC joints is fully dependent on the material properties, and represents an IBM work domain.

The time differential between the competitive approaches to flip chip attachment is large and consequently represents an obstacle to rapid acceptance of the PMC material process under development. There are, however, niche applications where the lead free / zero Alpha particle emission characteristics of the PMC material remain of interest and are expected to act as further incentives for the PMC usage and process development.

B. FUTURE WORK

There are several areas which suggest further work in pursuit of the PMC solution to flip chip non-solder based interconnect.

- It is the intent to provide PMC bumped flip chips and suitable test vehicles to the **Universal Chip Scale Packaging and Large Fine Pitch Direct Chip Attach Consortium.** These chips and test vehicles will allow the material to be evaluated in direct comparison to conventional flip chip attachment methods. With the large membership of the Universal Consortium, the material will be brought to the attention of a large segment of the electronics assembly end user community for possible inclusion in their future products.
- The IBM PMC material is not the only application domain requiring control of the time-temperature-pressure domain. For this reason further work can be done on refinement of the current thermode approach to heating the chips to the bonding temperature.
- The ability to exert fine control over planarity and applied load to flip chip and flip chip like componentry during their assembly process is of interest, and has applications beyond the PMC application under study.
- Refinement of the Computer Aided Cost Estimation (CACE) model is of interest for

several assembly processes, and the tool developed under the DARPA project may be built upon to extend its utility into other regions.

We are expecting that the IBM PMC material will show benefits to the Consortium assemblage and customers will identify appropriate product market opportunities. If so, the knowledge base developed under this program, in conjunction with the operational testbed and hardware produced can be further refined and used as the basis for a production instantiation.

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To: Dr. Bill Bernier, IBM Endicott
From: Dr. Daryl L. Santos, Binghamton University
Date: February 16, 1998
Re: Additional Cost Summaries (10s vs 30s Bond Rates) For DARPA Final Report

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This report is intended to summarize further cost studies of three different types of products, namely, the Kodak Cameo product, an SCM-L and an MCM-L over various two bond rates (10s vs. 30s) and different annual volumes.

Common/major inputs to all studies:

- Uniform production among all working days (250) according to annual volume (e.g., if there are 100,000 boards needed and 100 boards fit on a panel, then the base-line number of panels per day's production is 1,000/250 = 4. This is an important assumption in the model in that the labor consumed is constant (i.e., there's extra daily capacity at smaller production volumes))
- Herein, only non-depreciation added costs are studied
- Wafer and Board Preparation Houses use one 8h shift
- PCB Assembly House uses two 8h shifts
- 5" Wafers are used at $50/wafer
- ECA Material Cost is $0.50/gram
- Labor Rates: Engineering - $35/h; Operator - $35/h; Maintenance - $30/h
- Model only considers cost deltas (e.g., activities (approximately) exactly equivalent among all attach processes, like dicing/packaging wafer, paging assembled boards, etc., are not considered)
- Akin to the above, indirect costs (and any profit markup costs) are not considered but are assumed to be an equal percentage (whatever that percentage may be) among the different attach technologies
- For the ECA process, a separate assembly machine (for C4 application) is required. Note: pick-and-place machines for the other three options can place both the flipchips as well as other components. This assumption is important in that UIC may develop a m/c that has both a thermode head (for the ECA/C4 application) and a standard head for the non-flipchip components – thus decreasing equipment costs (important when depreciation analyses are performed)

What appears to be relevant from the above assumptions, inputs, and attached summary is that relevant cost deltas for ECA are on the same order of magnitude as with the traditional, solder-based processes.

Short Summary on Products Studied

Kodak Cameo Product:

3 flipchips @ 60 (total) flipchip I/O's
11 non flipchip SMT components
small circuit board, therefore 100 boards are made per panel
2 Annual Volumes Studied: 100k, 1M
2 Bond Rates Studied: 10s, 30s

SCM-L

1 flipchip @ 119 I/O's per board
221 boards per panel
2 Annual Volumes Studied: 1, 5M
2 Bond Rates Studied: 10s, 30s

MCM-L

2 flipchip @ 119 I/O's (total) per board
221 boards per panel
2 Annual Volumes Studied: 1, 5M
2 Bond Rates Studied: 10s, 30s

Kodak Cameo Product

		10 Sec				30 Sec
		ECA	SJ	SOC	SP	ECA
100k / Yr	Wafer	$ 400.40	$ 307.60	$ 377.80	$ 307.60	$ 400.40
	Board	$ 277.70	$ 505.20	$ 337.70	$ 1,002.80	$ 277.70
	Assembly	$ 710.70	$ 831.00	$ 711.00	$ 711.00	$ 710.70
	Total	$ 1,388.80	$ 1,643.80	$ 1,426.50	$ 2,021.40	$ 1,388.80
	Total/Board	**$ 13.89**	**$ 16.44**	**$ 14.27**	**$ 20.21**	**$ 13.89**
1M / Yr	Wafer	$ 647.20	$ 511.50	$ 583.00	$ 511.50	$ 647.20
	Board	$ 2,085.40	$ 2,520.00	$ 2,137.70	$ 3,028.50	$ 2,085.40
	Assembly	$ 799.00	$ 954.00	$ 834.00	$ 834.00	$ 812.40
	Total	$ 3,531.60	$ 3,985.50	$ 3,554.70	$ 4,374.00	$ 3,545.00
	Total/Board	**$ 3.53**	**$ 3.99**	**$ 3.55**	**$ 4.37**	**$ 3.55**

SCM-L Product

		10 Sec				30 Sec
		ECA	SJ	SOC	SP	ECA
1M / Yr	Wafer	$ 471.00	$ 365.80	$ 436.40	$ 365.80	$ 471.00
	Board	$ 2,077.70	$ 2,515.80	$ 2,137.70	$ 3,013.40	$ 2,077.70
	Assembly	$ 787.30	$ 940.90	$ 820.90	$ 820.90	$ 794.00
	Total	$ 3,336.00	$ 3,822.50	$ 3,395.00	$ 4,200.10	$ 3,342.70
	Total/Board	**$ 3.34**	**$ 3.82**	**$ 3.40**	**$ 4.20**	**$ 3.34**
5M / Yr	Wafer	$ 823.40	$ 657.10	$ 729.50	$ 657.10	$ 823.40
	Board	$ 10,093.00	$ 11,467.60	$ 10,145.40	$ 12,006.50	$ 10,093.00
	Assembly	$ 1,142.00	$ 1,437.50	$ 1,317.50	$ 1,317.50	$ 1,165.50
	Total	$ 12,058.40	$ 13,562.20	$ 12,192.40	$ 13,981.10	$ 12,081.90
	Total/Board	**$ 2.41**	**$ 2.71**	**$ 2.44**	**$ 2.80**	**$ 2.42**

MCM-L Product

		10 Sec				30 Sec
		ECA	SJ	SOC	SP	ECA
1M / Yr	Wafer	$ 541.40	$ 424.10	$ 495.00	$ 424.10	$ 541.40
	Board	$ 2,077.70	$ 2,515.80	$ 2,137.70	$ 3,013.40	$ 2,077.70
	Assembly	$ 790.70	$ 945.00	$ 825.00	$ 825.00	$ 800.80
	Total	$ 3,409.80	$ 3,884.90	$ 3,457.70	$ 4,262.50	$ 3,419.90
	Total/Board	**$ 3.41**	**$ 3.88**	**$ 3.46**	**$ 4.26**	**$ 3.42**
5M / Yr	Wafer	$ 1,246.40	$ 1,006.50	$ 1,081.20	$ 1,006.50	$ 1,246.40
	Board	$ 10,093.00	$ 11,474.30	$ 10,145.40	$ 12,006.50	$ 10,093.00
	Assembly	$ 1,155.40	$ 1,452.60	$ 1,332.60	$ 1,332.60	$ 1,202.50
	Total	$ 12,494.80	$ 13,933.40	$ 12,559.20	$ 14,345.60	$ 12,541.90
	Total/Board	**$ 2.50**	**$ 2.79**	**$ 2.51**	**$ 2.87**	**$ 2.51**

W/O Dep'n

* Wafer, Board, and Assembly rows are in Total Costs (Material + Utility + Labor) and are in $,000
* Total/Board in $

Above Tables are W/O Depreciation, I've added another set of Tables that include Depreciation on the next page

- On this page w/o, there are minor differences when changing the bond rate from 10 to 30s. an observer should see changes only in the assembly area and, at that, just changes in the utility cost contributions (I.e., while we don't account for the dep'n, the model still accounts for more equipment as increased Utility costs.)

- On the subsequent page, non-insignificant deltas are observed between 10s and 30s when coupled with increased volumes...this is due to the inclusion of equipment costs

Kodak Cameo Product

		10 Sec				30 Sec
		ECA	SJ	SOC	SP	ECA
100k / Yr	Wafer	$ 624.50	$ 440.60	$ 511.00	$ 440.60	$ 624.50
	Board	$ 317.70	$ 605.30	$ 366.30	$ 1,260.90	$ 317.70
	Assembly	$ 941.30	$ 1,019.60	$ 899.60	$ 899.60	$ 941.30
	Total	$ 1,883.50	$ 2,065.50	$ 1,776.90	$ 2,601.10	$ 1,883.50
	Total/Board	**$ 18.84**	**$ 20.66**	**$ 17.77**	**$ 26.01**	**$ 18.84**
1M / Yr	Wafer	$ 871.20	$ 644.50	$ 716.20	$ 644.50	$ 871.20
	Board	$ 2,165.40	$ 2,691.40	$ 2,166.30	$ 3,358.10	$ 2,165.40
	Assembly	$ 1,231.50	$ 1,405.10	$ 1,285.10	$ 1,285.10	$ 1,534.80
	Total	$ 4,268.10	$ 4,741.00	$ 4,167.60	$ 5,287.70	$ 4,571.40
	Total/Board	**$ 4.27**	**$ 4.74**	**$ 4.17**	**$ 5.29**	**$ 4.57**

SCM-L Product

		10 Sec				30 Sec
		ECA	SJ	SOC	SP	ECA
1M / Yr	Wafer	$ 695.00	$ 498.80	$ 569.60	$ 498.80	$ 695.00
	Board	$ 2,117.70	$ 2,615.90	$ 2,166.30	$ 3,271.40	$ 2,117.70
	Assembly	$ 1,016.50	$ 1,144.20	$ 1,024.20	$ 1,024.20	$ 1,167.60
	Total	$ 3,829.20	$ 4,258.90	$ 3,760.10	$ 4,794.40	$ 3,980.30
	Total/Board	**$ 3.83**	**$ 4.26**	**$ 3.76**	**$ 4.79**	**$ 3.98**
5M / Yr	Wafer	$ 1,047.50	$ 790.10	$ 862.70	$ 790.10	$ 1,047.50
	Board	$ 10,213.00	$ 11,739.30	$ 10,202.60	$ 12,536.20	$ 10,213.00
	Assembly	$ 1,707.90	$ 1,861.10	$ 1,741.10	$ 1,741.10	$ 2,236.50
	Total	$ 12,968.40	$ 14,390.50	$ 12,806.40	$ 15,067.40	$ 13,497.00
	Total/Board	**$ 2.59**	**$ 2.88**	**$ 2.56**	**$ 3.01**	**$ 2.70**

MCM-L Product

		10 Sec				30 Sec
		ECA	SJ	SOC	SP	ECA
1M / Yr	Wafer	$ 765.50	$ 557.10	$ 628.20	$ 557.10	$ 765.50
	Board	$ 2,117.70	$ 2,615.90	$ 2,166.30	$ 3,271.50	$ 2,117.70
	Assembly	$ 1,108.10	$ 1,234.40	$ 1,114.40	$ 1,114.40	$ 1,334.60
	Total	$ 3,991.30	$ 4,407.40	$ 3,908.90	$ 4,943.00	$ 4,217.80
	Total/Board	**$ 3.99**	**$ 4.41**	**$ 3.91**	**$ 4.94**	**$ 4.22**
5M / Yr	Wafer	$ 1,470.50	$ 1,139.50	$ 1,214.40	$ 1,139.50	$ 1,470.50
	Board	$ 10,213.00	$ 11,886.00	$ 10,202.60	$ 12,536.20	$ 10,213.00
	Assembly	$ 2,057.90	$ 2,198.70	$ 2,078.70	$ 2,078.70	$ 3,115.10
	Total	$ 13,741.40	$ 15,224.20	$ 13,495.70	$ 15,754.40	$ 14,798.60
	Total/Board	**$ 2.75**	**$ 3.04**	**$ 2.70**	**$ 3.15**	**$ 2.96**