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Low-power multi-chip module and board-level links for data transfer

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ABSTRACT

Advanced device technologies such as Vertical Cavity Surface-Emitting Lasers (VCSELs) and diffractive micro lenses can be combined with novel packaging techniques to allow low-power interconnection of parallel optical signals. These interconnections can be realized directly on circuit boards, in a multi-chip module format, or in packages that emulate electrical connectors. For applications such as stacking of Multi-Chip Module (MCM) layers, the links may be realized in bi-directional form using integrated diffractive microlenses. In the stacked MCM design, consumed electrical power is minimized by use of a relatively high laser output from high efficiency VCSELs, and a receiver design that is optimized for low power, at the expense of dynamic range. Within certain constraints, the design may be extended to other forms such as board-level interconnects.

Keywords: Photonic Interconnects, Low-Power Data Links, VCSELs, Photoreceivers, Micro-optics

MASTER

1. Introduction

New forms of photonic data links and interconnects are enabled by advanced, low-power photonic and optoelectronic devices such as high-efficiency vertical-cavity surface-emitting lasers (VCSELs) and low-power Heterojunction Bipolar Transistor (HBT) photoreceiver circuits. The packaging options for such devices are quite varied, and versatility may be maximized by the use of modular device designs that employ integrated microlens technologies.

The interconnect arrangements which can result from these lasers and photoreceivers may be optimized for selected portions of a design space that can vary by orders of magnitude in allowable power consumption, needed alignment accuracy, and speed of operation. In stacked MCM applications that have been previously presented [1], point-to-point interconnect designs have been optimized for a per-channel power consumption on the order of tens of mW, an MCM-compatible packaging footprint that can be realized in a two-dimensional arrangement with a pitch of less than 0.5 mm (and a misalignment tolerance of ± 25 to ± 50 μm), while operating at a speed of 100 Mb/s for each of many parallel channels.

Other features of the demonstrated design include direct (3.3V) CMOS drive of the lasers and CMOS interface to the photoreceivers, operation of the photoreceiver directly from the 3.3 V CMOS power supply, low latency, non-latched Non-Return-to-Zero (NRZ) operation with rise and fall times of approximately 1.5 ns, and a resulting Bit Error Rate (BER) that is extremely low at the 100 Mb/s data rate. Each interconnect channel thus behaves much like another stage of a digital CMOS design. The above characteristics were demonstrated using implant-isolated back-emitting 980 nm VCSELs and Indium Phosphide (InP) -based HBT receiver circuits in an interconnect system that consumed as low as 42 mW of electrical power [1],[2]. New, more efficient VCSELs [3] and optimized devices within the receiver circuits could reduce that per-channel power consumption to below 15 mW.

The primary advantages of such a high-density, low-power photonic interconnect are the ability to reduce electrical noise, crosstalk, and ground bounce in stacks of multi-chip modules. These advantages are

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particularly apparent when the interconnect enables connection of separable stacked MCM layers, thus avoiding the problems of metal contacting force that are inherent in high density electrical connectors. These advantages may be extended to the electrical circuit board or backplane level if the photonic interconnect can reduce dependence on tuned electrical lines, thus increasing interconnection throughput density while reducing noise. In more specialized connections, the photonic interconnect can provide an extremely high level of isolation between circuits. In such a case, the requirements on interconnect density and data throughput rate may be much lower than for those of the interconnect described here [4], [5].

2. A Low Power Interconnect Demonstration

Interconnects were demonstrated using 980 nm VCSELs and HBT-based InP photoreceivers. In particular, the design of the VCSELs to be used was found to be critical, due to the fact that they were to be driven directly from CMOS circuitry and thus without a prebias current. This would be expected to cause delays in the VCSEL turn-on. Such delays were observed to be very dependent on device design. Small (10 μm) diameter implanted VCSEL devices showed a tendency toward large (100s of ns) turn-on delays due to the presence of a thermal lensing effect [6], which had been previously observed in edge-emitting lasers [7]. Larger (20 μm) diameter designs for the implanted VCSELs showed turn-on delays of less than 1 ns. In addition to the implanted devices, etch-post VCSELs were also investigated. In initial tests, these devices showed lower (0.5 ns) turn-on delays. This, combined with the disadvantages of having to use a large-area implanted device (to reduce delay effects without prebias) makes etch-post and related oxide-confined VCSELs [3], [8] interesting for use in this application. Their overall effect on interconnect performance, and the relative influence of turn-on delay, device capacitance, and optical beam profile was also investigated.

The InP photoreceivers have been described previously [9], [10]. They feature a circuit design that is optimized for large signal operation with optical signals having powers in the range of 0.5 to 2.0 mW. They achieve low electrical power consumption by taking advantage of the relatively large input optical signal and limited dynamic range that would be needed for this application. The InP HBT technology features growth of the HBT active layer structure on InP substrates, and the use of the HBT collector-base junction as a p-i-n photodiode structure. The p-i-n diode was defined to have a 50 μm diameter, and was metallized over the entire surface for efficienct back-illuminated collection of the 980 nm light.

The VCSEL and HBT transmitter devices and receiver circuits are connected by integrated microlenses that collimate and refocus the optical beam that forms each channel. This allows for maximum misalignment tolerance between layers of an MCM stack, minimizes dependence on the separation distance between transmitter and receivers in the MCM layers, and keeps the f-number or numerical aperture requirements on each of the lenses from becoming too stringent. An optical design for a demonstration stack appears in Fig. 1. It is based on GaAs and InP device substrates that each have a thickness of 350 μm. The separation of 850 μm is approximately that which would be encountered in most MCM stacking applications. Simple Gaussian beam approximations indicate that this design can accommodate lens-to-device misalignments of up to 3 μm and level-to-level misalignments of up to 100 μm. This is accomplished by the use of a receiver lens that is larger than the diameter of the optical beam. In this test implementation, the VCSEL lens diameter was 30 μm in diameter with a 100 μm focal length to give a F/ 3.3 lens. The receiver lens diameter was 100 μm, with a focal length of 150 μm, resulting in a F/ 1.5 lens. This yields a corresponding $1/e^2$ beam diameter of 22 μm at the detector, thus placing the beam well within the detector area. In actual practice, the beam is closer to the full 100 μm receiver lens diameter, and may even overfill the lens due to diffraction efficiency limitations and the presence of multiple VCSEL modes.

This limitation in diffractive lens efficiency was found to be particularly true for the etch post lasers. These would be expected to have many more modes and a higher overall beam divergence than the implanted devices, due to the larger lateral optical confinement within the laser structure. This was verified by measuring the maximum CW laser outputs using a 100 μm pinhole at the 850 μm separation distance, and comparing those measurements to the laser power as measured by a large area detector. The percentage of

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light gathered within the aperture was typically 70 to 90 percent for the implanted laser devices, but only 30 to 50 percent for the etch post lasers. Another factor that may have been a limitation was the influence of lithography and etch variations between the two laser fabrication runs.

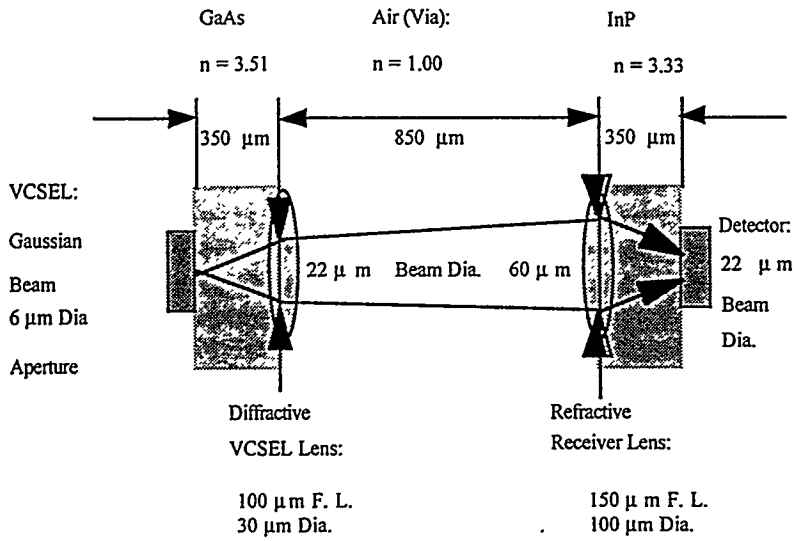


Figure 1 Cross-section of the basic optical design for one channel of a two-layer demonstration interconnect stack using VCSELs and corresponding photoreceivers.

In actual practice (as in Fig. 2), the VCSEL lenses are implemented in the GaAs substrate as etched diffractive lenses, while the photoreceiver lenses are realized as polymer refractive lenses on the InP receiver substrate. The design and fabrication of these lenses are described elsewhere [11], [12]. The alignment tolerance between each VCSEL and its lens is particularly important. Every 1 µm of misalignment between the VCSEL and the lens causes a 10 µm beam offset at the design distance of 850 µm. Accurate front-to-back alignment during the two-sided lithography steps that define the integrated lenses is thus important. The refractive receiver lens alignment is less critical due to the relatively large size of the detector compared to the re-focused beam size at the detector plane.

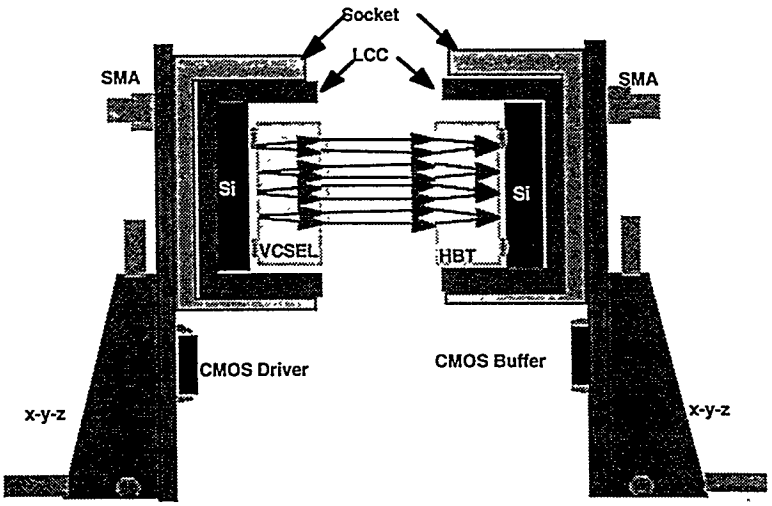
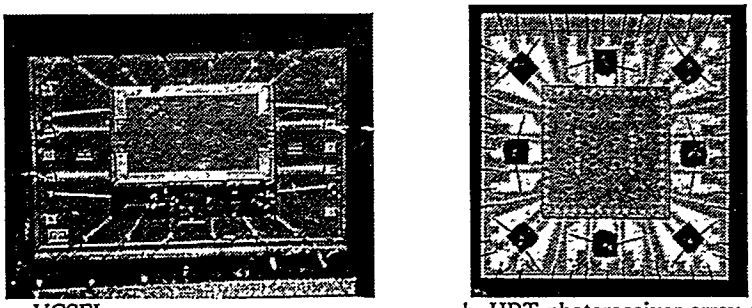


Figure 2 Breadboard test cross section. The lensed VCSEL and HBT can be brought into close proximity for alignment testing. The laser and HBT arrays are directly interfaced to 3.3V CMOS circuits.

3. Previous Demonstration Results with Implanted Lasers

The devices in the cross-section of Fig. 1 were evaluated in the test board arrangement of Fig. 2. The two boards were designed and fabricated to allow for simultaneous testing of up to 16 channels of optically-linked data. These tests were done to determine the performance of the implanted VCSELs and photoreceivers with direct CMOS drive and buffering, and to explore the range of stack alignment tolerance afforded by the optical design of Fig 1.

Laser and photoreceiver die were flip-chip mounted on silicon submounts as in Fig. 3a and Fig. 3b, respectively. These were placed in Leadless Chip Carriers (LCCs), to allow interchange of devices in the board-level interconnect test fixtures. Fig. 3a shows one of the VCSEL die flip-chip mounted on the silicon subcarrier. Here, beads of Indium-alloy solder paste were used to flip-chip bond the 350 μm thick GaAs VCSEL substrate onto the silicon. The 0.5 mm pitch, 4 x 4 diffractive lens array appears on the back (emission) side of the VCSEL die. Similarly, the photoreceiver was mounted (by thermosonic bonding of Au/Pd bumps) on a silicon submount as in the top view of Fig. 3b. Here, separate V_{cc} lines were carried to the LCC for each of the 16 channels on the device die. One ground line and a 140 pF power filter capacitor was provided for every two circuit channels. Wire bonds connect the silicon carrier to the pads of the 28 pin LCC for both the VCSEL and the photoreceiver die.



a. VCSEL array. b. HBT photoreceiver array and supply capacitors.

Figure 3. Transmitter and receiver die flip-chip bonded onto silicon submounts in leadless chip carriers.

The circuit of Fig. 4 shows the electrical schematic of each of the sixteen channels on the circuit board pair. Input data was applied on a 50 Ohm line and SMA connector at the input side of the link. The data signal traveled down approximately 4 inches of microstrip line to a 50 Ohm termination resistor at the input to a CMOS driver. The drivers used were *Integrated Devices* 74FCT163244 3.3V CMOS buffer/driver circuits. Though these circuits were designed to operate at 50 Mb/s, they were used successfully here at 100 Mb/s.

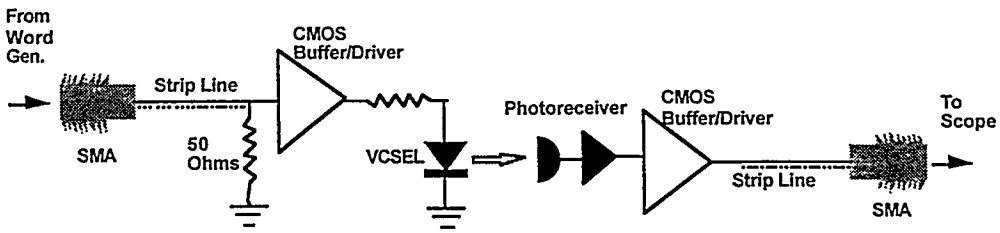


Figure 4. Board-level test circuit schematic for each individual channel.

Untuned line lengths were kept as short and equidistant as possible, and the microstrip lengths were matched within a few tens of picoseconds. A series resistor was used between each driver output and its corresponding VCSEL to control the laser current and resulting output light power. The corresponding photoreceiver response was fed into another 3.3V CMOS buffer/driver, (the same integrated circuit type as that identified above), and the output was sent to a 50 Ohm oscilloscope termination.

Eye diagrams and timing diagrams were used to characterize link integrity and latency. They generally showed that with about 0.9 mW of laser power entering the photoreceiver lens, the links would operate with the desired 1 to 1.5 ns rise and fall times, with jitter values as low as 0.25 ns. Combined link turn-on delay for the implanted lasers (less the CMOS drivers and buffers) and photoreceivers was found to be 3.3 ns. Of this total time, about 1.0 ns of the delay was found to be due to the time needed for the drive signal to reach the laser threshold point. This was mostly associated with limitations on the rise time of the CMOS-driven laser pulse driving the capacitive (25 pF) laser load. Because turn-off delays were generally very short, the turn-on delay translated into a reduced on-state pulse width as the laser power was reduced. This pulse width was then used to characterize misalignment tolerance. The integrated collimation and re-focus lenses of the optical system were found to allow for operation with greater than 9 ns of pulse width over a +/- 25 μm alignment tolerance [1], [2].

4. Demonstration Results for Designs Based on Etch-Post VCSELs

In order to further study the differences between the implanted and etch-post lasers, and to characterize the impact of those differences on interconnect performance, the test board set up of Figs. 2 and 4 was used. Here, etched-post VCSEL devices were substituted for the previous implanted devices, and the interconnect was characterized as described in Section 3.

The basic eye diagram for the interconnects appears in Fig. 5 with an etch-post laser operating at an output power of 3 mW. This condition was obtained for a 3.3V input at the driver IC when the series resistor of Fig. 4 was set to 50 Ohms, giving a 27.5 mA operating current for the laser. Based on pinhole aperture

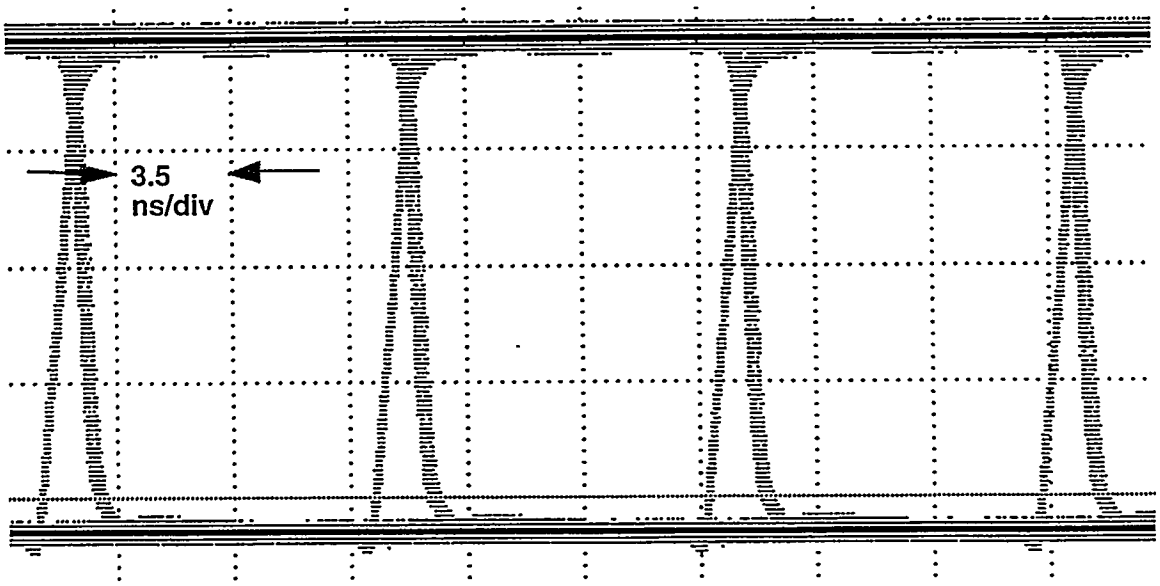


Figure 5. Eye diagram for a board-level test link using an etch-post laser operating at 100 mb/s, where 2 mW of the laser power passed to the receiver. Due to receiver saturation effects, the pulse width for the high or "on" state of the link is greater than the nominal 10 ns period of the signal.

measurements of the laser output, the estimated input laser power to the p-i-n detector on the photoreceiver was 1.98 mW. This higher laser power caused a slight saturation of the receiver, inducing an eye opening that was actually greater than the 10 ns nominal pulse width. This was in contrast to earlier eye diagrams taken with lower (0.9 mW and 0.5 mW) input laser powers that resulted in eye openings of approximately 9 ns and 5.5 ns, respectively [1].

The timing diagram for single pulses of this laser-receiver combination was recorded as in Fig. 6. Here, the electrical signal at various points in the circuit of Fig. 4 was recorded into a digital storage oscilloscope, using a high impedance active FET probe with a frequency response of 3 GHz. Since the same probe was used for each test point, the relative delays associated with single-pulse waveforms could be characterized at each of the stages of the circuit, thus giving information on the delays associated with each component in the interconnect channel. The results in Fig. 6 indicate that, even with the etched post laser and the higher laser output, the combined delay of the laser and photoreceiver was 3.14 ns (as compared with the 3.3 ns delay using the implanted laser operating at 0.9 mW) [1].

Link delay time was further characterized by a direct measurement of the laser turn-on characteristic. This was accomplished by using a fast photodetector and the high impedance FET probe described previously. These results appear in Fig. 7. Here, as with the previous implanted VCSEL, the laser turn-on characteristic was dominated by the time to reach the threshold voltage needed for laser turn-on. This rise time, measured as 1.36 ns, was a function of the capacitance of the laser and its subsequent loading of the CMOS driver and resistor. Laser turn on delay, when compensated as shown for the delay associated with the photodetector (measured by the delay between laser turn-off and detector turn-off) was negligible. It follows that capacitive loading of the driver and resistor was responsible for most of the delay on the laser side of the interconnect.

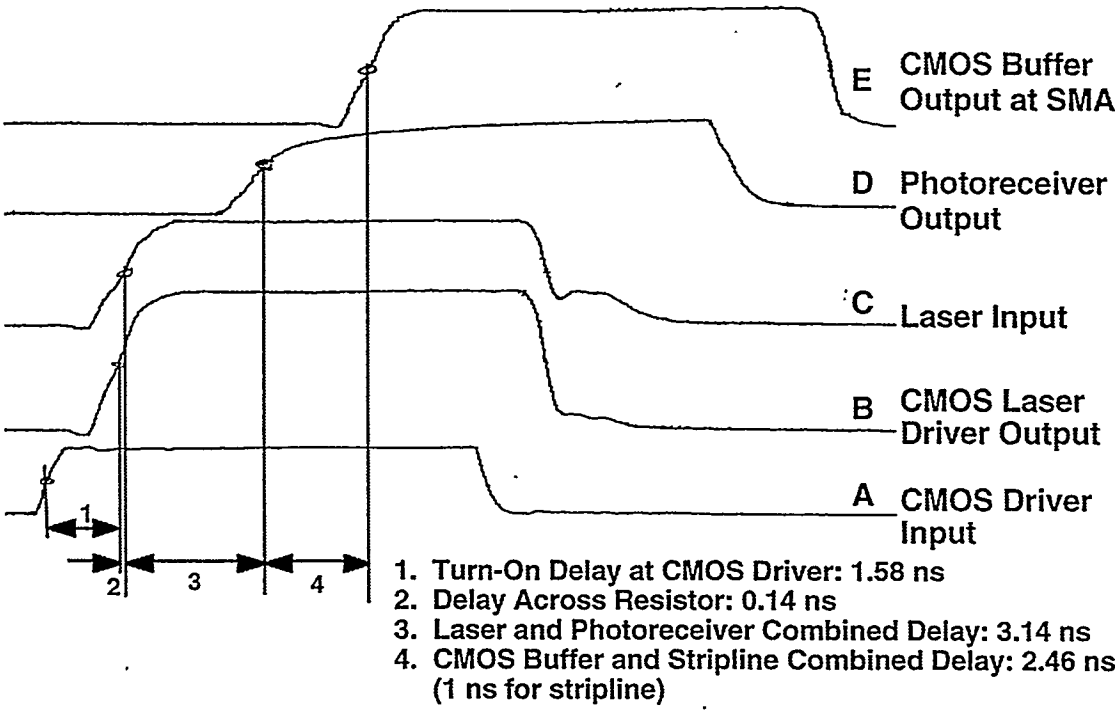


Figure 6. Timing diagram for a board-level test link using an etch-post laser operating at 100 mb/s, where 2 mW of the laser power passed to the receiver. Note that delays are present at each element of the interconnect.

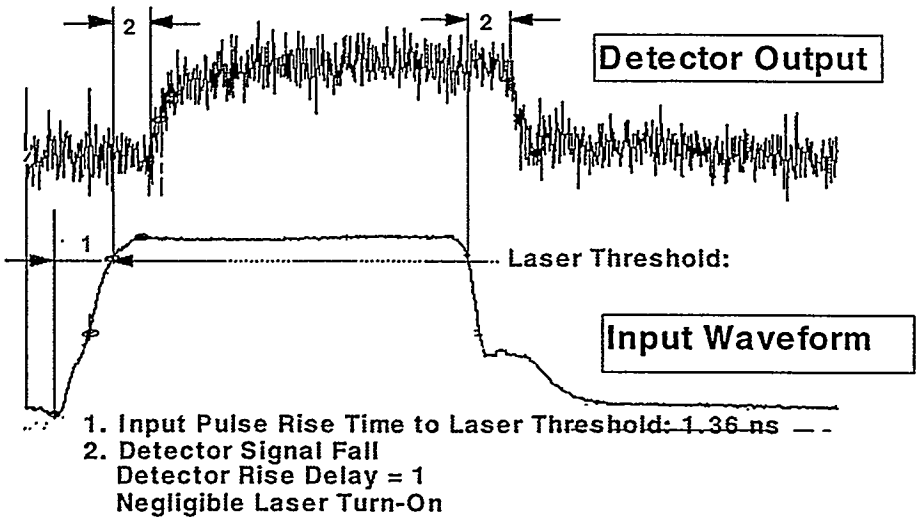


Figure 7. Timing diagram for the single-pulse response of an etch-post in the laser operating in the transmitter test board with an external detector. Delay is dominated by the rise time to reach the laser threshold voltage.

In contrast to a previously reported etch-post VCSEL [6], the etch-post devices used in this test were constructed using a laser with a thin dielectric layer, which thus exhibited a subsequently higher (75 pF) capacitance. The previous etch-post device had been planarized with a thick dielectric layer and thus had an overall capacitance which was well below that of either the 25 pF implanted lasers used in the interconnect demonstration that was summarized in Section 3, or the etch post lasers used here. This higher capacitance, combined with the series current-limiting resistor, caused the laser to be driven with a relatively slow (2 ns) total rise and fall time, and thus negated any potential advantages in turn-on delay that might have otherwise been obtained with the etch-post devices. It should also be noted that the laser turn-on delay only accounted for a small portion of the overall delay associated with the photonic devices, and that the increased laser power (2 mW for this demonstration versus 0.9 mW for the previous results) did not significantly reduce the delay associated with operation of the photoreceiver.

The slight excess "on-state" pulse width of the photoreceiver and buffer output that was indicated by Fig. 5 proved to be advantageous for operation under misalignment conditions. This was tested by adjusting the micrometers (shown schematically in Fig. 2) to move the test boards relative to their optimal alignment points. The induced misalignment would reduce the levels of light into the photoreceiver, and would subsequently increase the turn-on delay of the photoreceiver output. As this signal (indicated by curve D in Fig. 6) is delayed, the trigger point for the CMOS buffer equivalently moves out along the curve, causing the output to engage at a later and later time. Since the receiver and buffer still turns off promptly at laser turn-off, this yields a pulse width at the output that becomes equivalently smaller as misalignment becomes greater. At some point, the photoreceiver output becomes small enough that the buffer will not be triggered. This is indicated by Fig. 8, where pulse width is plotted as a function of misalignment between the laser and photoreceiver for a separation distance of 0.8 mm. If a pulse width of 9 ns is required to maintain interconnect timing margins, then the interconnect can tolerate a total misalignment range of 150 μm (± 75 μm). For a pulse width of 8 ns, the tolerance to misalignment reaches a range of 165 μm. These levels of performance would provide plenty of misalignment tolerance for stacked MCM interconnects, but would be too stringent for board-to-board interconnects. The integrated lens design would also require too small a separation distance to be practical for board-to-board interconnects, as they were only able to collimate the light beam from the VCSEL over a limited (<1 mm) distance.

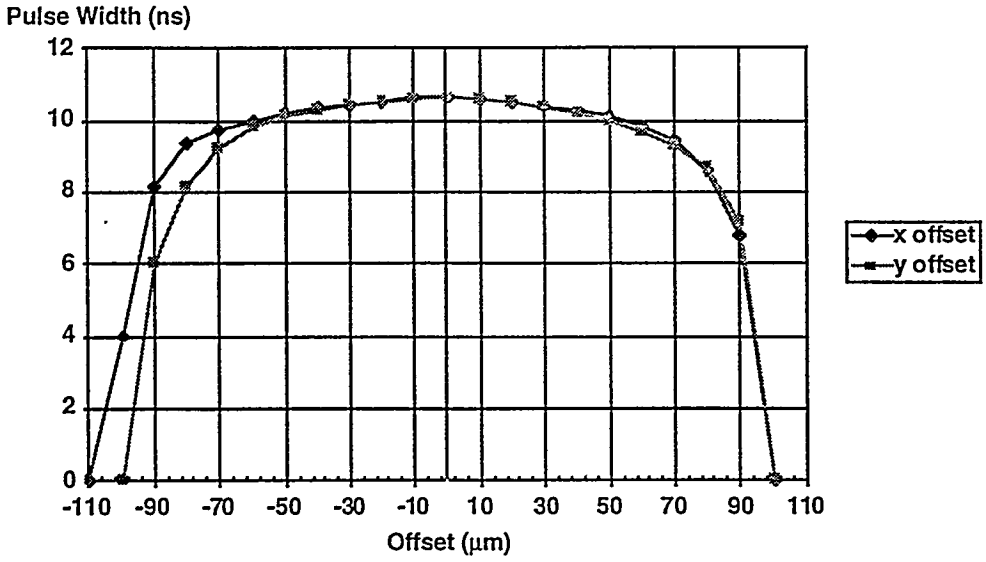


Figure 8. Misalignment tolerance for an etch-post laser operating in the board-level test arrangement with 2 mW into the photoreceiver and a laser-to-receiver separation distance of 0.8 mm.

5. Application to Board-Level Free-Space Point-to-Point Interconnects

In order to enable greater separation distance and alignment tolerance, external refractive microlens arrays were added to the test arrangement. These microlens arrays were dual-sided *Corning* photoform lenses, matched to the 4 by 4 array pattern of the laser and photoreceiver devices. Each of the microlenses featured a focal length of 0.31 mm and a diameter of 0.305 mm. They were mounted onto the LCCs of the VCSELs and HBT photoreceivers using spacers, as indicated in Fig. 9. For these tests the lens arrays were fixed in place by UV-curing epoxy.

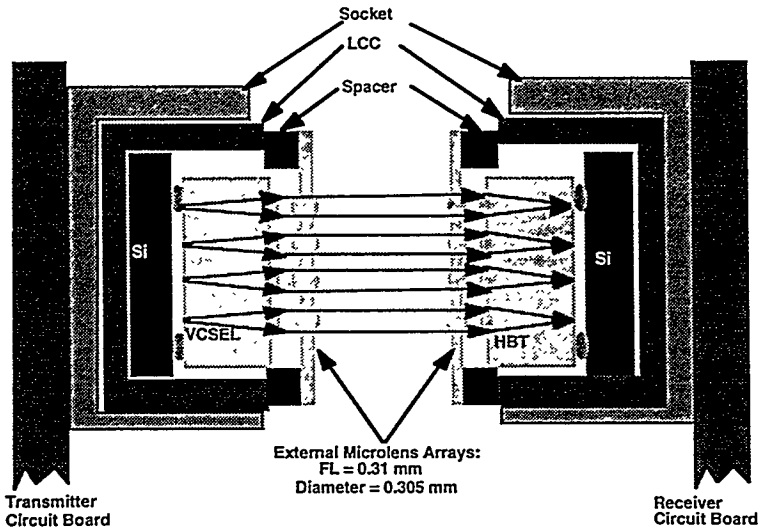


Figure 9. Adaptation of the test arrangement of Fig 4 to determine separation and misalignment tolerance with an external lens array. The external lenses provide collimation of beams over a greater range than can be done using only the integrated lenses.

The combination of integrated and external microlenses collimated the VCSEL beam over a much greater distance than the integrated lenses alone would do. This lens arrangement also tended to give a smaller beam diameter than would otherwise be obtained with a single external lens, thus making maximum use of the collection area associated with the external photoreceiver lens and enabling a correspondingly larger misalignment tolerance.

The externally-lensed VCSEL and photoreceiver arrangement of Fig. 9 was tested using the same pulse width criteria that were used for the misalignment tests of Fig. 8. Here, an etch-post laser which had a peak output of 2.89 mW was used in the test board. Because of the relatively large numerical aperture of the external microlens, all of the light could be assumed to be collected, though it was not assured that all of the light would be refocused into the photoreceiver, due to scattering and spreading related to the multimode VCSEL effects.

Test results for misalignment and separation tolerance appear in Fig. 10. These indicate that the external microlenses extend the range of collimation from approximately 1 mm (which would be used for the previous stacked MCM applications) to the range of 10 mm, which would allow interconnection of circuit boards. Note that the overall range of misalignment that could be tolerated is nearly 200 μm (±100 μm about the maximum pulse width), using an 8 ns pulse width as the acceptance criteria. Note also that this range of misalignment tolerance extends all the way to a separation distance of 10 mm. Though these results indicate that a reasonable in-plane misalignment could be tolerated with the tested microlens arrangement, the displacement of the optimal alignment point with increasing distance is a cause for concern. The measured displacement indicates a misalignment angle of only 2 degrees. Though this could be accommodated by a larger receiver lens diameter (and thus a smaller f-number for the receiver lens), this puts a more stringent requirement on the performance of that lens, and ultimately limits the interconnect density associated with the microlens arrangement. The angular alignment problem associated with the external microlenses of Fig. 9 could be addressed by a connector-based arrangement. This might be as simple as a set of alignment pins and machined spacers at the optical interface on each board, or it might be accomplished in more advanced interconnects by a design that makes use of combinations of microlenses and macro-lenses [13].

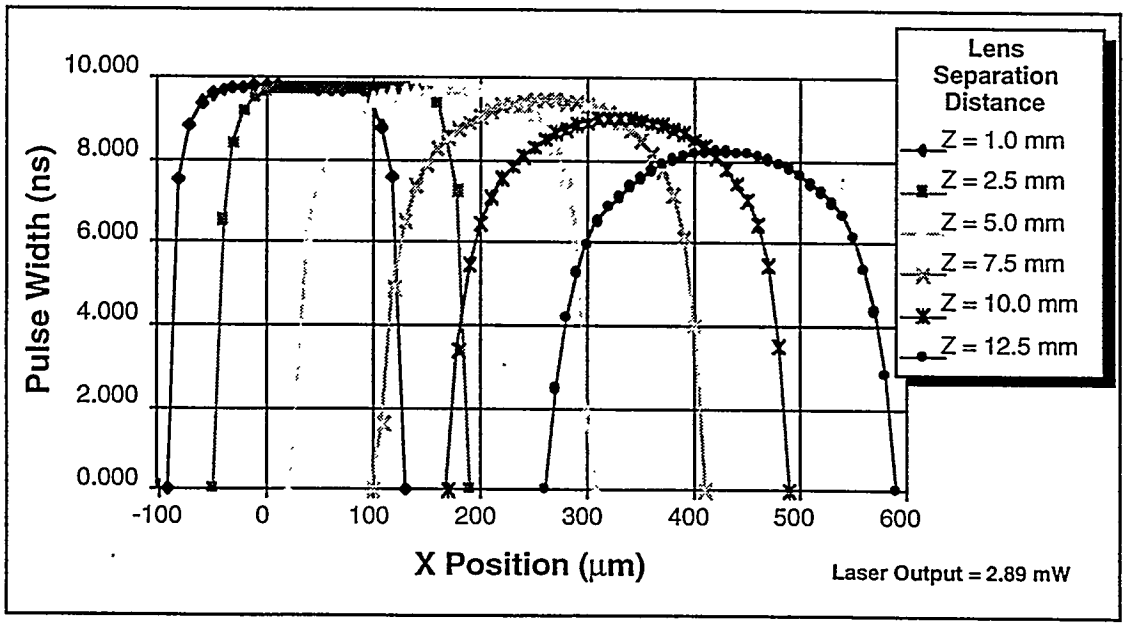


Figure 10 Misalignment tolerance for an etch-post laser operating in the board-level test arrangement with external microlenses to increase separation distance. The offset of the peaks with distance indicates a 2^0 angular misalignment.

6. Conclusion

VCSELs and HBT-based photoreceivers with integrated microlenses have been shown to be suitable for low-power point-to-point interconnections that would be applicable to stacked MCMs. These links have been demonstrated in a test board arrangement that features direct CMOS interface of the laser and photoreceiver devices. The tests have shown fast (1-2 ns) rise and fall times and acceptable timing margins, provided sufficient optical power is maintained. Further tests on these characteristics were found to give similar results for both etch-post and implanted VCSELs, provided that the implanted VCSELs were of sufficient size to prevent delays associated with thermal lens effects. The turn-on delay was found to be negligible for both types of VCSEL devices, when compared to the capacitive and resistive effects that limited the speed at which the input pulse would reach the lasing threshold. It follows that optimal characteristics for a high speed VCSEL which is designed to be operated from zero bias in an MCM-based interconnect are: 1) Low threshold voltage and current, 2) Small area and planarized interconnections for low capacitance, 3) Single-mode or few-mode operation for minimal distortion and spreading of the focused beam when internal microlenses are used.

Test results on a breadboard interconnect also showed that the demonstrated MCM-based integrated lens design could make use of external lenses to extend the range of operation of the links, thus enabling board-to-board interconnection with low power consumption. Suitable control of angle and displacement would be needed in order to accomplish this.

7. Acknowledgments

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