Noise-Resilient and Reduced Depth Approximate Adders for NISQ Quantum Computing

Abstract

The "Noisy intermediate-scale quantum" NISQ machine era primarily focuses on mitigating noise, controlling errors, and executing high-fidelity operations. Therefore, quantum circuits on a NISQ quantum computer require shallow circuit depth and robustness against noise. Approximate computing (AC) is a novel computing paradigm that produces imprecise results by relaxing the need for fully precise or completely deterministic operations; such error-tolerant applications include multimedia, data mining, and image processing. In this paper, we investigate the application of approximate computing in NISQ quantum computing as a mechanism to increase the noise resilience of the quantum adder circuits. We propose five designs of approximate quantum adders designed to reduce depth while making them noise-resilient at the same time. Three designs of approximate quantum adders are with carryout while two designs are without carryout. We have used novel approaches to design these approximate quantum adders that include approximating the Sum just from the inputs (pass-through designs), therefore, these adders have zero depth as no quantum gate is required. The second design style uses a single CNOT gate to approximate the SUM with a constant depth of O(1). We performed our experimentation on IBM Qiskit on seven noise models (thermal, depolarizing, amplitude damping, phase damping, SPAM, bitflip, and readout). Simulation results illustrate that compared to exact cuccaro adder[1] the proposed approximate adder without carryout has improved fidelity in the range of 8.34% (Phase Damping noise) to 219.22% (Bitflip noise). Similarly for proposed approximate adder with carryout the fidelity improves in range of 8.23% (Phase Damping noise) to 371% (Bitflip noise). We also evaluated our proposed approximate quantum adder in terms of various error metrics providing the quantity and frequency of error deviation.

CCS Concepts

• **Hardware → Quantum computation**.

Keywords

quantum adders, approximate computing, noise

1 Introduction

Quantum circuits serve as the basis for constructing quantum algorithms, making them helpful in applications such as quantum information processing, cryptography, image processing, and other scientific computations [8, 13]. Quantum arithmetic circuits are vital to design efficient circuits of quantum algorithms for scientific computing such as variational quantum algorithms for nonlinear problems, simulation of many-body systems, Poisson equation, linear systems of equations HHL, quantum Metropolis sampling, Gibbs state preparation, Singular Value Thresholding or Triangle Finding, and in the widely applicable framework of Quantum Rejection Sampling [5, 6]. In addition, researchers have included dedicated libraries of basic quantum integer arithmetic functions in quantum programming languages such as Microsoft Quantum Development Kit and Quipper [2, 7]. Therefore, quantum arithmetic circuit libraries will help design resource-efficient circuits of quantum algorithms for scientific computing [2, 7]. Further, quantum arithmetic circuits can be potential candidates for future benchmarking of noise models in NISQ machines or future benchmarking of automatic design tools for NISQ machines such as those in [3]. Quantum arithmetic circuits such as adders are already being used as benchmark circuits in NISQ machines [11]. Further, error-aware compilation in IBM's 20-Qubit machines uses adder circuits as benchmark circuits [11].

The quantum hardware available today supports what is known as noisy intermediate-scale quantum (NISQ) computing, which is unsuitable for prolonged operations due to error accumulation [4]. In the current "noisy intermediate-scale quantum" NISQ machine era, a primary focus is on mitigating noise, controlling errors, and executing high-fidelity operations. Therefore, quantum circuits on a NISQ quantum computer require shallow circuit depth and robustness against noise.

The currently existing quantum adders are based on the ripple carry mechanism in which the final carry depends on all the inputs. This long carry path inflates the circuit depth and gate count leading to a proportional rise in noise [1, 14]. The exact quantum adder by Cuccaro et al [1]. is widely used in quantum arithmetic circuits. We referred the design of Cuccaro et al. with output carry as CQA1 and without output carry as CQA0. Another exact quantum adder design proposed by Thapliyal et al. called TPL13 provides resource optimized design for quantum ripple carry adder. To have better comparison with existing work we compare our proposed approximate adder against designs proposed by Cuccaro et al. and Thapliyal et al. [1, 14].

Approximate computing (AC) is a novel computing paradigm that produces imprecise results by relaxing the need for fully precise or completely deterministic operations. Therefore, error-tolerant applications, such as multimedia, data mining, and image processing, often do not require fully accurate results, as imprecise or less-than-optimal results suffice. In the existing literature [12], approximate quantum multipliers are designed based on controlled quantum adders that are focused on optimizing depth and T-count. However, the designs of quantum adders perform controlled additions, therefore, have resource overhead compared to non-controlled quantum addition. Further, it utilizes an uncomputation gate that requires measurement operations, limiting its applicability to the NISQ domain due to increased noise susceptibility due to SPAM errors [10]. Therefore, to the best of our knowledge, no existing designs of uncontrolled (normal) quantum addition use approximate computing applicable to the NISQ domain. Hence, we propose five new designs of quantum approximate adders that have improved noise resilience and reduced circuit depth. This is achieved by removing the carry propagation dependency during the addition operation by applying the principle of approximate computing. Since there is no

carry dependency, each addition of input qubits operates in parallel, resulting in reduced logic gates and depth, thereby increasing noise resilience compared to exact designs of quantum adder circuits. To summarize, we make the following contributions:

- We propose five approximate quantum adders (three proposed adders with carryout, and two proposed adders without carryout) designed using approximate computing to reduce the depth and boost noise resilience.
- Out of the five designs, two are zero-depth parallel adders that do not require any quantum gates because they employ pass-through logic. The other three adders are of constant depth, as they compute the Sum output of the addition using single CNOT gates in parallel.
- We illustrate the superior noise-resilience of the proposed quantum approximate adders by conducting IBM Qiskit-based simulations on seven noise models.
- The proposed approximate adders without carryout improve fidelity in the range of 31.45% to 33.98%, while the proposed approximate adders with carryout improve fidelity in the range of 26.71% to 39.84% compared to exact quantum adder designs in 4-qubit configuration.
- We also assess the error introduced by approximate computing in the proposed adders by error metrics such as NMED and error rate.

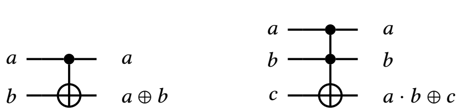
This work is organized as follows: Section 2 provides background on quantum noise sources and error metrics. Section 3 presents the proposed approximate adders with error deviation. Section 4 compares the noise performance of proposed adders.

2 Background

2.1 Quantum Gates

The quantum gates used in this work are explained below.

- CNOT Gate: CNOT gate (or Feynman gate) shown in Figure 1a helps in realizing XOR and XNOR operations by mapping A, B to A, A⊕B.
- Toffoli Gate: Figure 1b shows the mapping of three input A, B, C to three outputs A, B, A·B⊕C. Toffoli gate, also known as CCNOT (double controlled NOT) gate, can achieve AND, NAND, and OR logical operations. It is also the most resource intensive gate used in this work.



(a) CNOT Gate (b) Toffoli Gate

Figure 1: The CNOT and Toffoli gates.

2.2 Quantum Computing Noise Sources

Noise is the main obstacle in the adoption and scaling of quantum computing [10]. The prime source of quantum noise lies in the design and type of quantum computer. We focus on identifying unique noise sources and their impact on proposed designs by using IBM Qiskit [3] commands to inject uncertainty in simulations. We have chosen to model quantum noise in form of probability of incorrect output. Table 1 shows a compilation of noise models used in this work.

Table 1: Description of Noise Models

Model	Description
Thermal	Thermal relaxation error is characterized by time constants related by T1 (thermal relaxation) ≤ T2 (dephasing). We use T1 = 50μs, T2 = 70μs [3].
Depolarizing	It is the probability that a completely mixed state I/2 replaces the state of qubit [10]. We use an error probability of 0.005 for 1-qubit and 0.01 for 2-qubit gates.
Amplitude Damping	This noise occurs due to energy dissipation during operations [10]. We apply probability of 0.01 for 1-qubit gates.
Phase Damping	Phase damping involves the loss of information without energy loss [10]. We use probability of 0.01 for 1-qubit gates.
SPAM	State Preparation And Measurement noise reflects the reliability. In state preparation, error probability of reset to 1 (0.04) is twice the error of reset to 0 (0.02), while measurement error is 0.1 [9]
Bitflip	This noise source flips the qubit from 0 to 1 or vice versa, we use error probability for 1/2 qubit gates as 0.01 [3]
Readout	P(n|m) represents the probability of measuring n when correct output is m. We use P(1|0) = 0.05, P(0|1) = 0.1. [3]

2.3 Error Metrics

In this section, we explain the metrics used to measure the magnitude and frequency of the error introduced by the approximate adders. The most elementary metric is Error Distance (ED), which is the difference between the exact Sum (S_{exact}) and the approximate Sum (S_{approx}). As shown in Equation 2, we utilize ED to create Mean Error Distance (MED) by averaging over the total input combinations (N). Furthermore in Equation 3, normalization of MED by the maximum output across all inputs (S_{max}) reduces the sensitivity of NMED to outliers and variations in the distribution of error distances. NMED is particularly useful because it takes into account the scale and distribution of the error, allowing for fair comparison across different input configurations.

$$ED = \left|S_{exact} - S_{approx}\right| \tag{1}$$

$$MED = \frac{\sum ED}{N} \tag{2}$$

$$NMED = \frac{MED}{S_{max}} \tag{3}$$

Error rate (ER) is another metric used to evaluate the accuracy of an adder by measuring the proportion of incorrect results produced by it. ER is calculated by dividing the number of incorrect output (N_{error}) by the total input combinations (N), as shown in Equation 4. Adder with lower error rate will have errors limited to fewer input combinations, making them suitable for applications such as sensor data acquisition and image/audio filters which care for overall quality and discard outliers.

$$ER = \frac{N_{error}}{N} \tag{4}$$

3 Proposed Designs of Approximate Quantum Adders

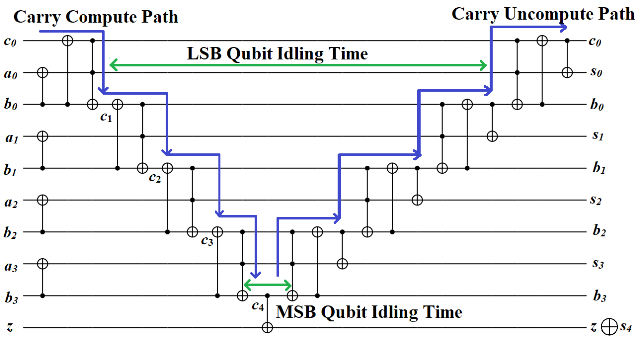


Figure 2: Exact quantum adder by Cuccaro et al [1]. The inputs are in range a_0 to a_4 and b_0 to b_4 while S_0 to S_4 represent Sum bits. The Carry generation path extends from c_0 to c_4, creating higher depth and longer carrypath, increasing the noise susceptibility of carryout. LSB qubits spend much more time idling than MSB, making Sum vulnerable to noise [4].

In this section, we propose five approximate quantum adders to reduce the number of quantum gates and the depth to increase noise resilience. Figure 2 illustrates two root causes of noise in the design of existing quantum exact adders that we address in this work by utilizing approximate computing. First, we approximate the Sum output of the addition of two qubits using only its corresponding inputs. Our approximate adders operate in parallel, as there is no carry propagation during the addition operation. We do not generate intermediate carries and instead focus on creating the final carryout using only the MSB input qubits. These design techniques help generate all qubits of the Sum in parallel, avoiding the issue of idling qubits. In addition, the noise accumulated on carryout is lesser as there is no longer a carry path. Applying these design principles reduces the depth of proposed adders and increases their noise resilience.

Table 2 showcases the Sum and Carry logical equations for the exact quantum adders and the proposed quantum approximate adders. The proposed adders AQA1 and AQA2 are without Carry, whereas AQA3, AQA4, and AQA5 are with carryout. Table 2 also lists the CNOT and Toffoli gate count with their respective depth. The O(1) or constant depth complexity of proposed adders is superior to the O(n) or linear complexity of exact adders.

3.1 Proposed Adders Without Carryout

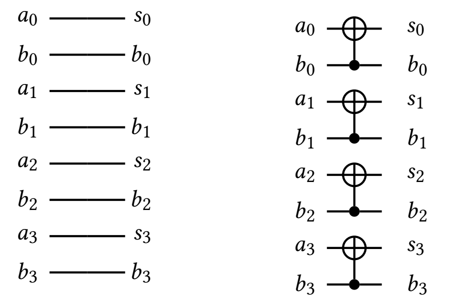
We first design adders without carryout for quantum applications that do not need an output carry. We only approximate the Sum for these adders, keeping the designs simple and with low depth.

(1) *Approximate Quantum Adder 1 (AQA1)*

The easiest way to approximate Sum is by using one of the inputs. In our first design AQA1, we map the input A to Sum and pass the input B unaltered, as shown in Equation 5. As evident from Figure 3(a), the adder is zero depth, and utilizes no quantum gates.

$$s_i = a_i \quad \text{if } 0 \le i \le n-1 \tag{5}$$

(2) *Approximate Quantum Adder 2 (AQA2)*



(a) AQA1: Pass based Zero Depth (b) AQA2: CNOT based Single Depth

Figure 3: Proposed Carryless 4-Qubit Adders. a) AQA1 needs no hardware to pass input A to Sum with input B unchanged. b) Single CNOT gate in AQA2 reduces the error distance.

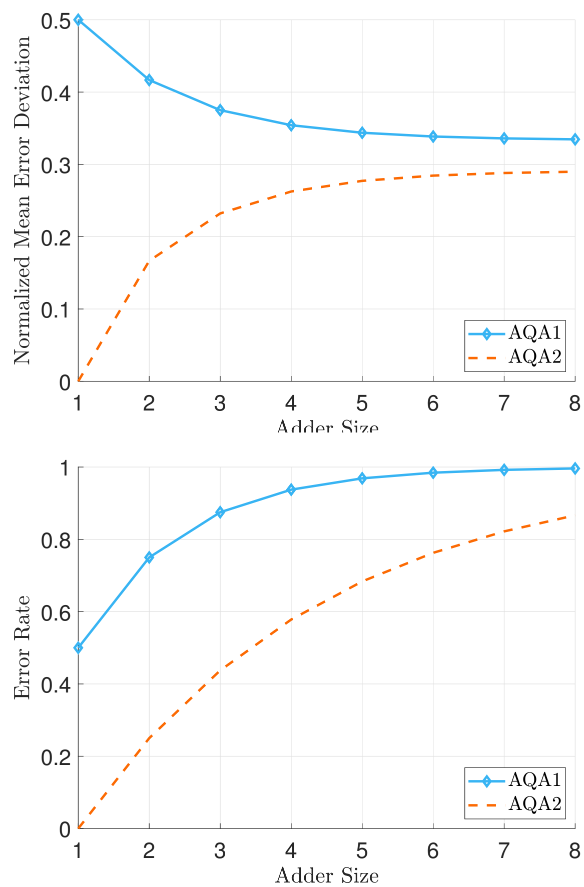


Figure 5: Error Rate of Proposed Carryless Adders.

To create a better approximation than AQA1, we use logical-XOR of the two inputs as depicted in Equation 6. This design is also without carryout, has single depth, and has n CNOT gates for n-qubit input, evident from Figure 3(b). As a result, AQA2 performs better than AQA1 regarding both NMED and error rate, as shown in Table 3. Figure 4 and 5 illustrate the NMED and error rates of the adders AQA1 and AQA2.As evident, the proposed adder AQA2 scales better than AQA1 in the entire range upto eight qubits.

$$s_i = a_i \oplus b_i \quad \text{if } 0 \le i \le n-1 \tag{6}$$

Table 2: Design Characteristics of Exact and Proposed Approximate Adders

Adder Type	Name	Sum	Carry	Qubits	Depth		Count	
					CNOT	Toffoli	CNOT	Toffoli
Quantum Exact Adders	CQA0[1]	$A \oplus B \oplus C_{in}$	N.A.	$2n+1$	$3n+1$	$2n$	$4n$	$2n$
	CQA1[1]	$A \oplus B \oplus C_{in}$	$A \cdot B \oplus B \cdot C_{in} \oplus C_{in} \cdot A$	$2n+2$	$3n+2$	$2n$	$4n+1$	$2n$
	TPL13[14]	$A \oplus B \oplus C_i$	$A \cdot B \oplus B \cdot C_i \oplus C_i \cdot A$	$2n+1$	$3n-2$	$2n-1$	$5n-5$	$2n-1$
Proposed Adders Without Carryout	AQA1	A	N.A.	$2n$	0	0	0	0
	AQA2	$A \oplus B$	N.A.	$2n$	1	0	n	0
Proposed Adders With Carryout	AQA3	A	B_{n-1}	$2n$	0	0	0	0
	AQA4	$A \oplus B$	B_{n-1}	$2n$	1	0	n	0
	AQA5	$A \oplus B$	$A_{n-1} \cdot B_{n-1}$	$2n+1$	1	1	n	1

Table 3: Error Metrics for proposed carryless adders

Error Metric	Qubits	4	8
NMED	AQA1	0.3542	0.3346
	AQA2	0.2625	0.2899
Error Rate	AQA1	0.9375	0.9961
	AQA2	0.5781	0.8665

3.2 Proposed Adders With Carryout

In several applications, the output carry generated from the addition of two inputs is required. Therefore, to design the approximate adder with carryout we explore design strategies to generate it with low depth and minimal gates encountered in the carry path. In the process, we also improve their error metrics.

(1) *Approximate Quantum Adder 3 (AQA3)*

Our first design with an output carry AQA3, is derived from AQA1. The carryout is created from input B's MSB as shown in Equation 7. Figure 6(a) illustrates that it has zero depth and zero gate count. Table 3 shows that inclusion of approximate carry improves the NMED from 0.35 to 0.13 for 4 qubit configuration, although the error rate remains same. Lower NMED value represents that the output will be closer to the exact output.

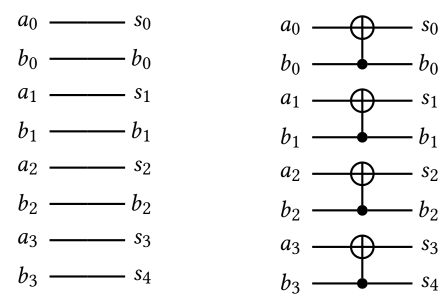
$$s_i = \begin{cases} a_i, & \text{if } 0 \leq i \leq n-1 \\ c_n, & \text{if } i = n \end{cases} \qquad (7)$$
$$c_n = b_{n-1}$$

(2) *Approximate Quantum Adder 4 (AQA4)*

Like in the case of AQA3, we also design AQA4 using AQA2 by reassigning the last qubit of the input B as carryout, as shown in Equation 8. As observable from Figure 6(b), this approach helps ensure the depth remains constant with n CNOT gates for n inputs. The proposed adder AQA4 is worse than AQA3 regarding NMED but has a much superior error rate, as evident from 4.

$$s_i = \begin{cases} a_i \oplus b_i, & \text{if } 0 \leq i \leq n-1 \\ c_n, & \text{if } i = n \end{cases} \qquad (8)$$
$$c_n = b_{n-1}$$

(3) *Approximate Quantum Adder 5 (AQA5)*



(a) AQA3: Pass based Zero Depth

(b) AQA4: CNOT based Single Depth

Figure 6: Proposed 4-Qubit Adders With Carryout which improve the error distance by assigning b_3 to s_4 as carryout.

We next propose approximate adder AQA5, which generates the carryout as $a_{n-1} \cdot b_{n-1}$ to provide a better approximation of the carryout, where a_{n-1} and b_{n-1} are the MSB's of the inputs. We use a Toffoli gate for this purpose as shown in Figure 7. AQA5 provides output carry on a separate qubit for quantum applications that require cascading a larger quantum circuit after the quantum adder. This adder shields the cascaded circuit from input noise sources and provides a high fidelity carryout while freeing one of the inputs for downstream utilization. Table 4 shows that AQA5 is better than both AQA3 and AQA4 in terms of NMED and error rate.

$$s_i = \begin{cases} a_i \oplus b_i, & \text{if } 0 \leq i \leq n-1 \\ c_n, & \text{if } i = n \end{cases} \qquad (9)$$
$$c_n = a_{n-1} \cdot b_{n-1}$$

Table 4: Error Metrics for proposed adders with carry-out

Error Metric	Qubits	4	8
NMED	AQA3	0.1333	0.1255
	AQA4	0.1917	0.1877
	AQA5	0.1167	0.1245
Error Rate	AQA3	0.9375	0.9961
	AQA4	0.6836	0.8999
	AQA5	0.5781	0.8665

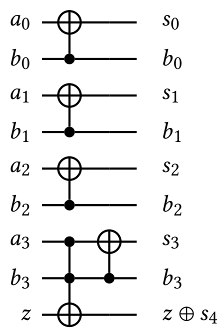


Figure 7: Proposed constant depth 4-qubit adder AQA5. The Sum is generated using logical-XOR, while the Carry is $a_3 \cdot b_3$.

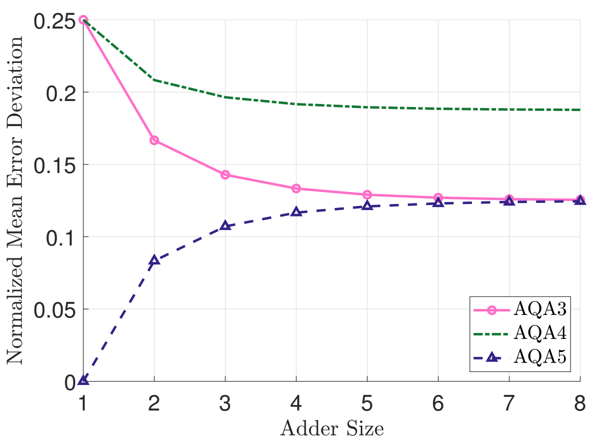


Figure 8: NMED of Proposed Adders with Carryout.

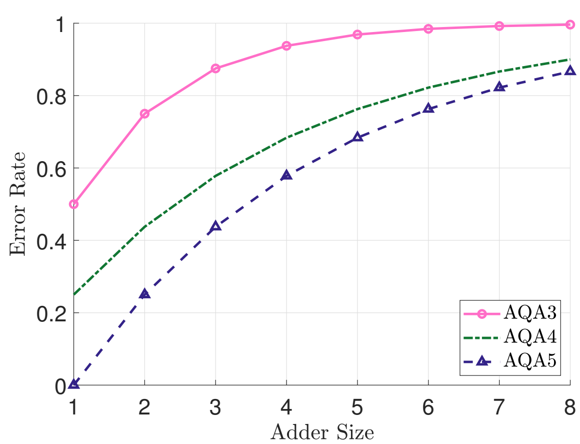


Figure 9: Error Rate of Proposed Adders with Carryout.

The proposed approximate adders reduce the quantum gates to achieve zero or constant depth. Furthermore, unlike exact adders, the output on all Sum qubits gets generated in parallel, with carry-out getting generated using a much shorter mechanism. Both these factors help improve the noise fidelity of proposed approximate adders over exact adders, which we explore in Section 4.

Table 5: Output Probability of proposed 4-qubit Adders without carryout from Noise Simulations

Noise Type	CQA0[1]	AQA1	Impr. % w.r.t. CQA0	AQA2	Impr. % w.r.t. CQA0
Thermal	0.712	0.951	33.57	0.935	31.32
Depolarizing	0.589	0.995	68.93	0.97	64.69
Phase	0.923	1.0	8.34	1.0	8.34
Amplitude	0.776	0.98	26.29	0.961	23.84
Bitflip	0.307	0.98	219.22	0.924	200.98

4 Noise-Resilience Analysis of Proposed Approximate Quantum Adders

To evaluate the noise resilience of the proposed approximate quantum adders, we utilize the probability of obtaining the intended output to measure noise fidelity. To arrive at the output probability, we simulate the adders in a 4-qubit configuration using IBM Qiskit for all 256 input configurations. Then, we divide the number of accurate results by the simulation count (256 in this case). By modifying only the noise model in qiskit simulations and leaving the rest unchanged, we perform the same process for each adder using the seven different noise models. SPAM and readout noise depend on the measurement and input states making them proportional to the qubit count, impacting the exact and approximate adders in the same manner in our study. Due to this, we present the results of five noise models in Tables 5 and 6 for comparison. In the rest of this work, the average output probability is also interchangeably referred to as accuracy (in percentage). To simplify the process of analyzing noise, we split the adders into two categories depending on the presence (or absence) of output carry.

4.1 Comparison of noise resilience of proposed approximate adders without carryout

The adders in Table 5 are the proposed adders without carryout simulated using noise conditions in a 4-qubit configuration. While comparing with exact adder without carry CQA0[1]: **1. Thermal Noise**: AQA1 shows improvement of 33.57%, while AQA2 shows 31.32%. **2. Depolarizing**: AQA1 shows 68.93% and AQA2 shows 64.69% improvement respectively. **3. Phase Damping**: Both AQA1 and AQA2 show improvement of 8.24%. **4. Amplitude Damping**: AQA1 shows improvement of 26.29%, while AQA2 shows 23.84%. **5. Bitflip**: Both adders show high improvement, AQA1 showing 219.22% and AQA2 showing 200.98% respectively. This shows that the proposed adders make good gains over CQA0 in thermal, depolarizing, amplitude damping and bitflip noise models.

Table 6: Output Probability of proposed 4-qubit Adders with Carryout from Noise Simulations

Noise Type	CQA1[1]	TPL13[14]	AQA3	AQA4	AQA5
Thermal	0.663	0.6956	0.953	0.926	0.904
Depolarizing	0.576	0.6292	0.994	0.968	0.917
Phase	0.924	0.9408	1.0	1.0	0.99
Amplitude	0.772	0.8139	0.975	0.961	0.94
Bitflip	0.207	0.263	0.975	0.915	0.814

4.2 Comparison of noise resilience of proposed approximate adders with carryout

For the proposed quantum adders with carryout listed in Table 6, we consider CQA1[1] as the baseline to compare the proposed adders and the more optimized TPL13[14]. While comparing with exact adders: **1. Thermal Noise**: AQA3 shows improvement of 43.74% with CQA1[1] and 37% with TPL13[14], while AQA4 shows 39.67% and 33.12%, and AQA5 shows 36.35% and 29.96% respectively. **2. Depolarizing**: All adders show high improvement. AQA3 showing 72.57% and 57.98% over CQA1[1] and TPL13[14] respectively, AQA4 showing 68.06% and 53.85%, while AQA5 showing 59.2% and 45.74% respectively. **3. Phase Damping**: Both AQA3 and AQA4 show improvement of 8.23% with CQA1[1] and 6.29% with TPL13[14], AQA5 shows 7.14% and 5.23% respectively. **4. Amplitude Damping**: AQA3 shows improvement of 26.3% with CQA1[1] and 19.79% with TPL13[14], while AQA4 shows 24.48% and 18.07%, and AQA5 shows 21.76% and 15.49% respectively. **5. Bitflip**: All adders show high improvement. AQA3 showing 371% and 270% over CQA1[1] and TPL13[14] respectively, AQA4 showing 342% and 247.91%, while AQA5 showing 293.24% and 209.51% respectively. This closely follows the pattern of number of quantum gates and depth in Table 2 with AQA2 having no CNOT gates to AQA4 having n=4, and AQA5 having n+1=5 CNOT gates. AQA6 on the other hand features a Toffoli gate introducing a higher noise impact.

Table 7: Improvement Comparison of proposed 4-qubit Adders with Carryout with existing works

Adder	Impr.% w.r.t.	Thermal(%)	Depolarizing(%)	Phase(%)	Amplitude(%)	Bitflip(%)
AQA3	CQA1[1]	43.74	72.57	8.23	26.3	371.01
	TPL13[14]	37	57.98	6.29	19.79	270.72
AQA4	CQA1[1]	39.67	68.06	8.23	24.48	342.03
	TPL13[14]	33.12	53.85	6.29	18.07	247.91
AQA5	CQA1[1]	36.35	59.2	7.14	21.76	293.24
	TPL13[14]	29.96	45.74	5.23	15.49	209.51

5 Discussion and Conclusion

We have proposed five approximate quantum adders in this work by optimizing the depth and gate count. We have shown that the proposed adders have better fidelity than the existing works by performing quantum simulations on the IBM qiskit platform, conducted using different noise models. Thermal and Bitflip noise hit exact adders the hardest since they have more gates, increasing the likelihood of output deviation. Depolarizing noise applies random pauli operation on the three-axis [10]. Since this error needs to accumulate before affecting output, it impacts exact adders with higher depth and carry path for error accumulation. Phase damping noise, on the other hand, introduces a rotation along the z-axis [10] but has minimal impact on the adders as our input lies on the x-axis. Amplitude damping noise is proportional to the idling time for qubit [4], impacting the exact adders with ripple carry mechanism the severest. As the LSB in cuccaro exact adders must wait for the longest for the reverse computation, its output probability in amplitude damping noise model drops to 0.772. In contrast, the proposed approximate quantum adders are unscathed, as all qubits get processed in parallel. Finally, it is evident that the exact adders leave much to be desired in noise fidelity, and the proposed approximate quantum adders outperform them by a very wide margin. We also study the error characteristics of the proposed approximate quantum adders using metrics such as NMED, and error rate and establish the scalability of proposed approximate quantum adders. Our results illustrate that approximate quantum adders increase noise fidelity while saving quantum gates. They can be very useful in applications such as quantum image processing which are inherently error tolerant and suited for approximate arithmetic. We conclude that the proposed quantum approximate adders can be very beneficial in the NISQ era, with our thorough error and noise analysis helping select an approximate adder suitable for the quantum application.

References

[1] Steven A Cuccaro, Thomas G Draper, Samuel A Kutin, and David Petrie Moulton. 2004. A new quantum ripple-carry addition circuit. *arXiv preprint quant-ph/0410184* (2004).

[2] Alexander S Green, Peter LeFanu Lumsdaine, Neil J Ross, Peter Selinger, and Benoît Valiron. 2013. Quipper: a scalable quantum programming language. In *Proceedings of the 34th ACM SIGPLAN conference on Programming language design and implementation*. 333–342.

[3] IBM Quantum. 2022. *Qiskit noise models.* https://qiskit.org/documentation/tutorials/simulators/3_building_noise_models.html and https://qiskit.org/documentation/stubs/qiskit_aer.noise.ReadoutError.html.

[4] Akshaya Jayashankar, My Duy Hoang Long, Hui Khoon Ng, and Prabha Mandayam. 2022. Achieving fault tolerance against amplitude-damping noise. *Physical Review Research* 4, 2 (2022), 023034.

[5] Yonghae Lee, Jaewoo Joo, and Soojoon Lee. 2019. Hybrid quantum linear equation algorithm and its experimental test on IBM Quantum Experience. *Scientific reports* 9, 1 (2019), 4778.

[6] Michael Lubasch, Jaewoo Joo, Pierre Moinier, Martin Kiffner, and Dieter Jaksch. 2020. Variational quantum algorithms for nonlinear problems. *Physical Review A* 101, 1 (2020), 010301.

[7] Microsoft Quantum Libraries. 2023. *version 0.27.253010.* https://learn.microsoft.com/en-us/azure/quantum/user-guide/libraries/ quantum computing library.

[8] Edgard Muñoz-Coreas and Himanshu Thapliyal. 2018. T-count Optimized Quantum Circuits for Bilinear Interpolation. (9 2018). http://arxiv.org/abs/1809.09249

[9] Paul Nation. 2021. *Improving state prep errors on IBM Quantum systems.* https://nonhermitian.org/posts/2021/2021-11-07-rep_delay.html#summary

[10] Michael A Nielsen and Isaac Chuang. 2002. *Quantum computation and quantum information.* American Association of Physics Teachers.

[11] Shin Nishio, Yulu Pan, Takahiko Satoh, Hideharu Amano, and Rodney Van Meter. 2020. Extracting Success from IBM's 20-Qubit Machines Using Error-Aware Compilation. *J. Emerg. Technol. Comput. Syst.* 16, 3, Article 32 (may 2020), 25 pages. https://doi.org/10.1145/3386162

[12] Sohrab Sajadimanesh, Jean Paul Latyr Faye, and Ehsan Atoofian. 2022. Practical approximate quantum multipliers for NISQ devices. In *Proceedings of the 19th ACM International Conference on Computing Frontiers*. 121–130.

[13] Peter W Shor. 1994. Algorithms for quantum computation: discrete logarithms and factoring. In *Proceedings 35th annual symposium on foundations of computer science*. Ieee, 124–134.

[14] Himanshu Thapliyal and Nagarajan Ranganathan. 2013. Design of efficient reversible logic-based binary and BCD adder circuits. *ACM Journal on Emerging Technologies in Computing Systems (JETC)* 9, 3 (2013), 1–31.