GaAs Thermophotovoltaic Patterned Dielectric Back Contact Devices with Improved Sub-bandgap Reflectance

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Abstract

We demonstrate GaAs thermophotovoltaic (TPV) devices with a patterned dielectric back contact (PDBC) architecture, featuring a dielectric spacer between the semiconductor and back metal contact over most of the back surface for high reflectance, and metal point contacts over a smaller area for electrical conduction. In the TPV application, high sub-bandgap reflectance is needed to reflect unused sub-bandgap photons to the thermal emitter to minimize energy losses in this portion of the thermal spectrum. We explore different PDBC fabrication processes with SU-8 and SiO_2 dielectric spacer layers to maximize sub-bandgap reflectance while minimizing series resistance to increase TPV conversion efficiency. We successfully demonstrate GaAs SU-8 PDBC TPV devices with 2200°C blackbody-weighted sub-bandgap reflectance of 94.9% and 96.5% with and without a front metal grid, respectively. This is 0.7% and 2.3% (absolute) higher than the mean sub-bandgap reflectance of 94.2% for GaAs baseline TPV devices with 100% Au back contact with front metal grid. Lower sub-bandgap reflectance in TPV devices with front grids indicates the front grid induces light scattering leading to additional parasitic absorption in the TPV device. We also show that for higher contact coverage fractions, the PDBC reflectance cannot in general be treated by a linear interpolation using simple 1D transfer matrix method modeling and should be treated instead as a diffraction grating by solving Maxwell's equations in 3D.

Keywords

Thermophotovoltaics, energy storage, infrared reflectance, series resistance, dielectric-point contact mirrors, SU-8 photoresist, free-carrier absorption.

1. Introduction

Thermophotovoltaics[1,2,3,4,5] convert the electromagnetic radiation from a thermal emitter directly into electricity using a photovoltaic (PV) device. Efficiency in solar photovoltaics is affected by various non-controllable factors such as the solar spectrum, cloud cover, sun position, latitudinal location of the solar PV converter, and other environmental factors. In a thermophotovoltaic (TPV) system, the TPV converter is placed close to the thermal emitter, so that TPV efficiency can in principle be controlled by local parameters such as the emitter material, temperature, relative position, and aperture of the thermal emitter[6]. One of the key reasons that TPV devices can achieve higher efficiency than solar PV devices is that the

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unabsorbed sub-bandgap photons can be reflected to the thermal emitter, reheating the thermal emitter, and recovering that energy which would otherwise be wasted. Important TPV applications include solar thermal TPV[7,8,9,10,11,12,13], industrial waste heat recovery[14] and high-temperature energy storage[15,16], which is the focus of the present work.

Different approaches for the reuse of sub-bandgap light in TPV systems include the use of selective emitters[17,18,19,20], selective band edge filters[21], and use of the TPV device as a band-edge filter[22,23,24,25]. Using the TPV device itself as a band-edge filter is appealing for its elegance and simplicity of utilizing the absorbing layer in the device which is already present. The TPV device absorbs above-bandgap photons to create electron-hole pairs but is transparent to sub-bandgap photons. For a direct bandgap semiconductor, the filter can be quite sharp. By using a broadband back surface reflector, most of the sub-bandgap photons can be reflected to the blackbody emitter to minimize parasitic heat loss.

TPV device research has historically focused on absorber bandgaps in the 0.5-0.8 eV range, for lower thermal emitter temperatures, typically in the ≤1100°C range[26]. Recently, Omair et al.[24] demonstrated a 0.7-eV GaInAs TPV device with an efficiency of 29.1% at ~1200°C. However, with higher thermal emitter temperatures, the thermodynamic[27,28] efficiency limits are higher, and higher energy storage densities[14,15] are possible.

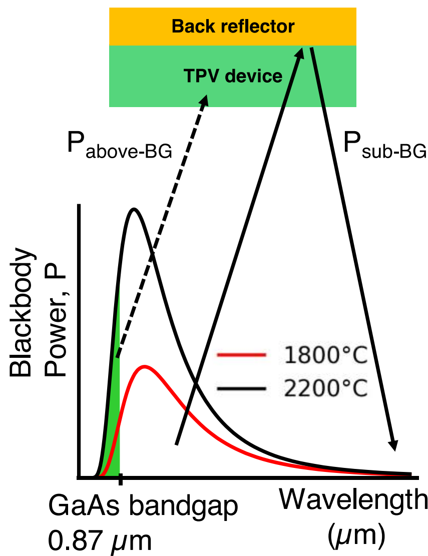

Figure 1. Schematic illustrating a TPV device as a bandgap filter with blackbody power density as a function of wavelength. The green shaded area represents above bandgap photons that can be converted to electricity. The unshaded area represents the sub-bandgap photons that must be reflected to thermal emitter to minimize parasitic loss.

Here, we design, fabricate, and characterize the reflectance and series resistance of TPV devices with a 1.4-eV GaAs[29] absorber which also serves as a band-edge filter, designed for thermal emitter temperatures greater than 1800°C. Even at such high emitter temperatures, only a narrow spectrum of the incident electromagnetic radiation falls in the absorption range of GaAs, as shown in Fig. 1, with a broad sub-bandgap spectrum spanning from 0.87 to 10 μm. These sub-bandgap photons should be reflected to the thermal emitter to minimize parasitic heat loss. We model and characterize the optical and electrical performance of GaAs TPV devices. For ease of comparison of different TPV designs, we extract a weighted sub-bandgap reflectance at a blackbody emitter temperature of 2200°C.

For these higher emitter temperatures and correspondingly higher incident intensities, a higher bandgap GaAs TPV device is preferred[5] in some ways over a lower bandgap TPV device for several reasons. 1) The voltage that can be achieved for a higher bandgap (E_g) cell is a greater fraction of the

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bandgap voltage E_g/q than for cells with lower bandgap. For a given above-gap photon flux and photogenerated current density J_{ph}, the bandgap-voltage offset $W_{oc} \equiv (E_g/q) - V_{oc}$ can be treated as approximately constant with respect to bandgap[30], so V_{oc} is a greater fraction of E_g/q for higher E_g. 2) For a given J_{ph}, for a cell with higher bandgap and higher voltage V, the resistive (I^2R) losses are a smaller fraction of the power generated ($I \cdot V$) by the cell. The practical limit of J_{ph} in concentrator PV or TPV is typically determined by the resistance R that can be achieved by the metal grid technology used and other factors affecting the cell series resistance, and the I^2R resistive power losses that are acceptable, so evaluating different cell bandgaps at a given J_{ph} is reasonable. 3) Finally, GaAs cells can be grown epitaxially on GaAs substrates, which are much less expensive than InP, InSb, and InAs substrates traditionally used for the growth of lower bandgap III-V materials.

There are at least three key challenges in designing a GaAs TPV device: First, the sub-bandgap reflectance of the TPV device weighted by the blackbody thermal spectrum from the emitter must be maximized. In solar PV, interference based back reflectors are demonstrated to enhance photon recycling[31,32,33], and boost open-circuit voltage. These reflectors are usually designed to improve the back reflectance at wavelengths near the bandgap of the active layer. In TPV, the back reflector must be designed for broadband sub-bandgap wavelengths spanning from bandgap of the active layer to mid-infrared. Second, the specific series resistance (R_{series}) must be minimized. The GaAs TPV device operates at a very high current density of 3-6 A/cm^2 depending on emitter temperature and presence of anti-reflection coating. In comparison, typical operating current density in a one-sun GaAs solar PV device is only around 20-30 mA/cm^2. Thus, in a GaAs TPV device, high R_{series} would result in high I^2R_{series} loss, detrimental for TPV efficiency. Third, as with solar PV, the quality of the semiconductor device itself must be at the highest level possible, by minimizing non-radiative recombination, *e.g.*, from trap-assisted and Auger mechanisms, and enhancing photon recycling to increase the device voltage. This paper will focus mainly on the sub-bandgap reflectance challenge, while maintaining performance with respect to R_{series} and material quality.

One of the main factors affecting the sub-bandgap reflectance is absorption in the metal back contact. By inserting a low-refractive-index, low-loss dielectric spacer between the semiconductor and metal, back contact absorption in the metal is reduced[34]. However, since the dielectric spacer materials are insulating, we adopt a patterned dielectric back contact[35,36,37,38] (PDBC) design as shown in Figures 2, 3, with a hexagonal array of vias through the dielectric layer allowing the semiconductor back contact layer to form electrical contact to the metal back contact. Thus, the PDBC reflectance is a combination of reflectance from the dielectric-metal "mirror" region, and the metal point contact "via" region, which typically has lower reflectance. The contact coverage fraction (CCF) is the ratio of metal point contact area to total back surface area. So, 0% CCF is essentially a device with only dielectric spacer layer between the semiconductor back contact layer and the metal back contact with no metal point contacts through the dielectric. And 100% CCF is essentially a device with no dielectric spacer layer and just 100% planar metal back contact on the semiconductor back contact layer. The contact coverage fraction in a PDBC can be adjusted by changing the diameter of metal point contact and/or the spacing between metal point contacts. By linearly interpolating from 0% CCF to 100% CCF, we increase the metal point contact area and simultaneously decrease the dielectric area in the PDBC. So, if we have Au metal point contacts in the dielectric, linearly interpolating

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to a 100% CCF will lead to a 100% Au back contact planar device which will represent the baseline case throughout this study. Swanson et al.[22] demonstrated Si PDBC TPV devices with SiO_2 dielectric spacer with an efficiency of 29% at 2027°C. Similarly, Fan et al.[25] demonstrated a 0.7-eV GaInAs TPV device with gridded back contacts and with air as the dielectric spacer layer, with an efficiency of 31.3% at 1200°C.

In this paper, we investigate SU-8 and SiO_2 dielectric spacers, Ag back metal mirror, and Au point contacts, for high-reflectance PDBC structures in GaAs TPV devices, for thermal emitter temperatures greater than 1800°C. We also explore methods specific to SU-8 and SiO_2 for fabricating PDBC structures that can be transferred to other III-V devices. Finally, we fabricate and characterize the sub-bandgap reflectance and series resistance of GaAs PDBC TPV devices as a function of contact coverage fraction.

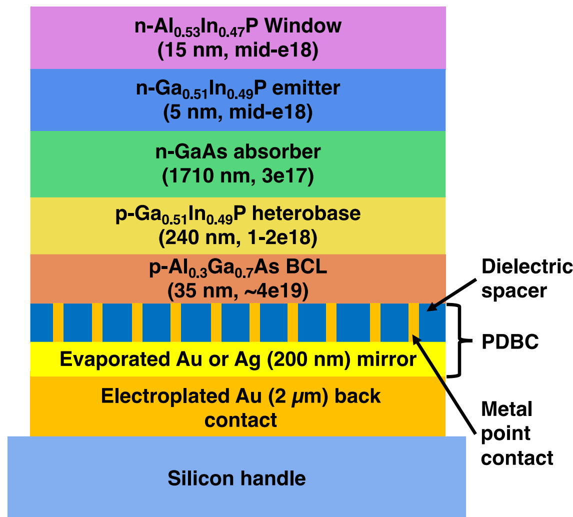
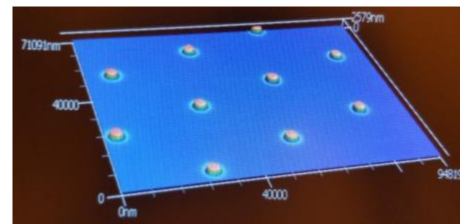
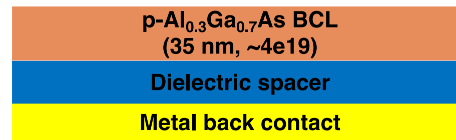


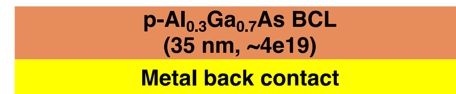
Figure 3. Schematic of GaAs TPV Device with a PDBC on a Si handle. The front contact layer (100 nm GaAs + 200 nm GaInAs) is not shown and is present only beneath the Ni/Au front grids.



(a)



(b)



(c)

Figure 2. Schematic of (a) a patterned dielectric back contact (PDBC) with metal point contacts and dielectric/metal mirror area in three-dimension (b) 0% contact coverage fraction (CCF) back contact; and (c) 100% CCF back contact. In fig. 3b and 3c other GaAs device layers are same as shown in Figure 3.

2. TPV device Modeling

2.1 TPV efficiency as a function of $R_{sub\text{-}BG}$ and R_{series}

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In a TPV system, the thermal emitter is near the TPV device. Ideally, all the unabsorbed above-bandgap and sub-bandgap photons can be reflected to the thermal source to minimize parasitic heat loss. The net power absorbed by the TPV device is the difference between incident power from the thermal emitter and reflected power, and it is this net power absorbed that is used to calculate TPV device efficiency. Accordingly, the simple GaAs TPV efficiency[39] is semi-empirically calculated using Eq. 1-3 where r_s is the characteristic resistance[40], P_{tot} is total blackbody power incident on the TPV device, $P_{sub\text{-}BG}$ is blackbody power incident on the TPV device in the sub-bandgap spectrum, $P_{above\text{-}BG}$ is blackbody power incident on the TPV device in the above bandgap spectrum, calculated at 2200°C blackbody spectrum, and other symbols carry their usual meaning. TPV device efficiency is calculated in Fig. 4 using experimental TPV device electrical parameters from multi-sun current-voltage (I-V) measurement of a GaAs PDBC TPV device at 3.5 A/cm^2, corresponding to the short-circuit current density J_{sc} of a GaAs TPV device for a 2200°C blackbody thermal emitter. $R_{sub\text{-}BG}$ is defined as the sub-bandgap reflectance of the GaAs TPV device, integrated from 0 to 90° angle of incidence, weighted by the 2200°C blackbody spectrum, where $r_{sub\text{-}BG}$ is the sub-bandgap spectral reflectance as a function of wavelength as shown in Eq. 4. Efficiency modeling [Fig. 4] indicates that $R_{sub\text{-}BG}$ has a stronger effect on TPV efficiency than typical values of R_{series} for $R_{sub\text{-}BG}$ greater than 90%. For $R_{sub\text{-}BG}$ above about 95%, an increase of only 1% (absolute) in $R_{sub\text{-}BG}$ is calculated to boost the TPV system efficiency by >3% (absolute). Nevertheless, due to the high operating current density, I^2R_{series} losses can be significant if the series resistance is too high. Thus, both increasing $R_{sub\text{-}BG}$ and reducing R_{series} have significant impacts on improving TPV efficiency.

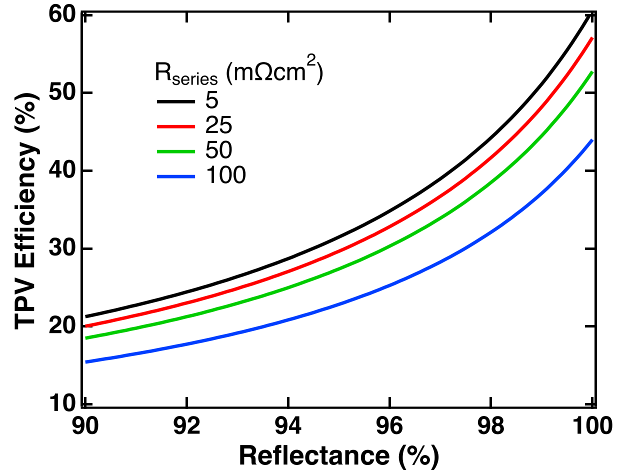

Figure 4. Simple GaAs TPV efficiency as function of $R_{sub\text{-}BG}$ for different R_{series} at 2200°C blackbody spectrum.

$$\eta_{TPV} = \frac{Total\ output\ electrical\ power}{Total\ blackbody\ power\ - Total\ reflected\ power} \tag{1}$$

$$\eta_{TPV} = \frac{V_{oc}\, J_{sc}\, FF_{ideal}\ (1 - r_s)}{P_{tot} - \ (R_{sub-BG} P_{sub-BG}\ +\ R_{above-BG} P_{above-BG})} \tag{2}$$

$$\text{where } r_s = \frac{R_{series}\, J_{sc}}{V_{oc}} \tag{3}$$

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$$R_{sub-BG} = \frac{\int_{\phi 1}^{\phi 2}\int_{\theta 1}^{\theta 2}\int_{\lambda 1}^{\lambda 2} r_{sub-BG} P_{sub-BG} \cos\theta \sin\theta \, d\lambda d\theta d\phi}{\int_{\phi 1}^{\phi 2}\int_{\theta 1}^{\theta 2}\int_{\lambda 1}^{\lambda 2} P_{sub-BG} \cos\theta \sin\theta \, d\lambda d\theta d\phi} \quad (4)$$

2.2 $R_{sub\text{-}BG}$ modeling and dielectric material selection:

As shown above, even a minor boost in $R_{sub\text{-}BG}$ results in a significant improvement in TPV efficiency. To achieve high $R_{sub\text{-}BG}$, we evaluate a GaAs TPV device with PDBC as shown in Fig. 2. The one-dimensional transfer matrix method[41] (TMM) is used to model the sub-bandgap reflectance of GaAs PDBC TPV devices for different dielectric spacers and metal back contacts. The PDBC structure is a 3D structure, requiring a full solution to Maxwell's equations to rigorously model the reflectance, as discussed in the reference 42 and later in this paper. As a zeroth-order approximation however, we initially calculate the reflectance as an interpolation between a 1D 0% CCF [Fig. 3b] and 1D 100% CCF [Fig. 3c] cases using Eq. 5.

For the TMM modeling shown here, a rear heterojunction GaAs TPV device stack as shown in Fig. 2, but with 100% CCF as shown in Fig. 3b, is evaluated using open-source TMM python library[43], at 0-90° angle of incidence. A 0° to 90° angle of incidence is used to model the blackbody radiation environment from the thermal emitter in the final grid-level energy storage TPV application where the photon emission has a Lambertian distribution across all angles. In Fig. 5a, we plot $R_{sub\text{-}BG}$ as a function of dielectric thickness for different dielectrics for 0% CCF (meaning the limit of no pillars through the dielectric) along with $R_{sub\text{-}BG}$ of Au and Ag planar

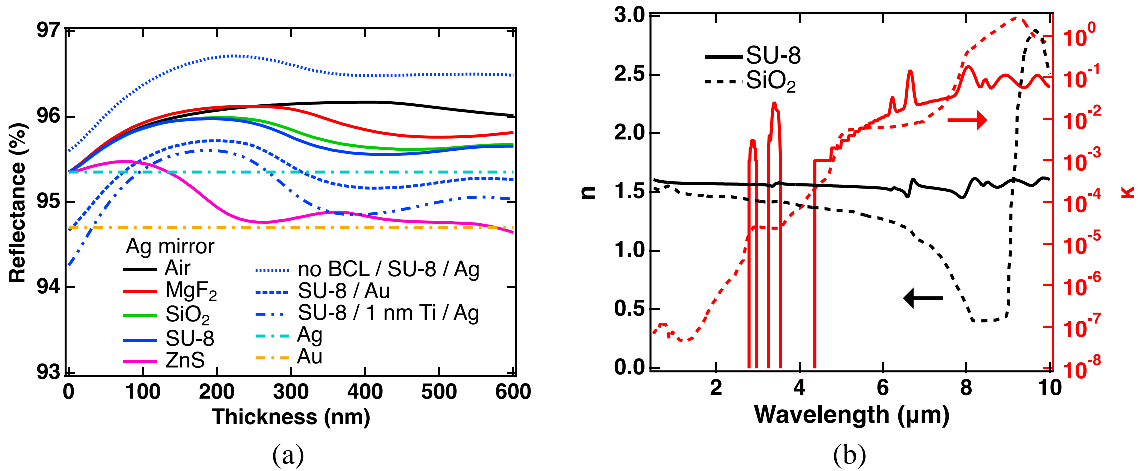

Figure 5. (a) Sub-bandgap reflectance for GaAs TPV device with a dielectric spacer layer between the semiconductor back contact layer and the metal back contact (0% CCF PDBC) as a function of dielectric thickness for different dielectrics with Ag back mirror, SU-8 / Au mirror, 1 nm Ti / Ag mirror, no BCL layer / SU-8 / Ag mirror, only Au, and only Ag mirror. All reflectance is weighted to 2200°C blackbody spectrum integrated at 0°-90° angle of incidence from 0.874 μm to 10 μm wavelength. (b) Optical constants (n, κ) of SU-8 and SiO_2 dielectrics. Real part (n) on the left-axis and imaginary part (κ) on the right-axis. SU-8 optical constants were measured by J.A. Woollam Co. and SiO_2 optical constants were from reference 44.

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mirrors (100% CCF, equivalent to zero dielectric thickness). Ray/geometric optics indicates that the dielectric with the lowest refractive index and extinction coefficient should result in the maximum R_{sub-BG}. Between gold and silver, Ag gives the higher R_{sub-BG}. Amongst the different dielectrics evaluated, air has the lowest refractive index resulting in a maximum R_{sub-BG} of 96.2% at a thickness of 400 nm with Ag mirror behind the dielectric. Similarly, ZnS has the highest refractive index thus resulting in the lowest maximum R_{sub-BG} among the cases in Fig. 5a, of 95.5% at a thickness of 80 nm with an Ag mirror behind the dielectric.

SU-8 is a negative photoresist epoxy polymer that can be spin-coated, photolithographically processed, and hard-baked to remain in the TPV device as a dielectric spacer. Both SiO_2[44] and SU-8 have similar refractive indices [Fig. 5b] and yield similar maximum R_{sub-BG} values of ~96% at a thickness of 205 nm and 195 nm respectively, with an Ag mirror [Fig. 5a]. R_{sub-BG} can be further increased to 96.7% if we can etch away the highly doped and highly absorbing p-AlGaAs back contact layer (BCL) between the contact vias. This p-AlGaAs layer acts as a lateral conduction layer as well as a back contact layer to metal. High doping in the back contact layer leads to lower sheet and specific contact resistance, but also results in increased free-carrier absorption in the sub-bandgap spectrum. For certain low current density TPV applications, the p-GaInP heterobase layer can be designed to act as the lateral conduction layer. In this case, the p-AlGaAs back contact layer can be selectively etched everywhere except the metal point contacts. We refer to this structure as the etched back contact layer (etched BCL) case.

As a special case, the maximum R_{sub-BG} for a GaAs TPV device with SU-8 / 1 nm Ti / Ag mirror is calculated to be 95.6%, just 0.5% lower than the SU-8 / Ag mirror. The 1 nm of Ti is used as adhesion layer between SU-8 and Au or Ag, and has lower reflectance compared to Au or Ag. Even with this 1 nm Ti layer to provide robust metal-to-dielectric adhesion in practical devices, we get an absolute boost in R_{sub-BG} of 0.9% compared to the baseline case of a 100% CCF Au-only back contact.

Based on the TMM modeling and real-world material processing considerations, SU-8 and SiO_2 dielectrics are chosen to demonstrate two different PDBC fabrication methods, which in principle should yield a similar boost in R_{sub-BG} compared to the planar Au back contact with 100% CCF. The TMM modeling indicated that R_{sub-BG} is not highly sensitive to the dielectric spacer thickness, thus any thickness in 150 – 220 nm range is sufficient for SU-8 and SiO_2.

$$R_{sub-BG}(CCF) = R_{sub-BG\ 0\%}(1 - CCF) + R_{sub-BG\ 100\%}(CCF) \quad (5)$$

2.3 R_{series} dependence on contact coverage fraction (CCF)

Series resistance (R_{series}) of the TPV device is a major factor in determining the TPV system efficiency. Due to the reduced contact coverage fraction in a PDBC TPV device, R_{series} of the cell can easily become dominated by the sheet resistance of the PDBC. Babcock et al.[45] calculated the fractional power loss in a PDBC for metal point contacts in a square/hexagonal lattice arrangement in photovoltaic devices. A similar approach is considered in this paper to analyze efficiency loss components for TPV devices and systems.

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Figure 6a shows the fractional resistive power loss in the PDBC of a GaAs TPV device, semi-empirically calculated as a function of CCF for 3 μm and 10 μm point contact diameters, at a current density J of 3.5 A/cm^2 that is representative of a 2200°C blackbody spectrum.

Experimental values of specific series resistivity associated with the back contact have been measured on TPV devices and test structures, to quantify the expected resistive loss for two different back contact architectures. For the case in which the back contact is intact (intact BCL case) in Figure 6b, the lateral conduction layer (LCL) consists of a stack of a 240 nm p-GaInP:Zn (2×10^{18} cm^{-3} Zn-doped) back surface field (BSF) layer, and a 35 nm p-AlGaAs:C (4×10^{19} cm^{-3} C-doped) back contact layer (BCL), giving a net measured sheet resistance of 1030 Ω/sq. The specific contact resistivity (ρ_{cb}) between the Au and BCL is measured to be 1×10^{-6} Ω cm^2. Similarly, the specific contact resistivity between a BCL and PDBC for electroplated Ni/Au point contact and e-beam evaporated 1 nm Ti / 150 nm Au is also measured through a test structure to be 2.2×10^{-5} Ω cm^2.

Since the p-AlGaAs:C back contact layer is heavily doped, it is a strongly free-carrier[46,47] absorbing material. For the case in which the back contact is etched away (etched BCL case) leaving only the p-GaInP:Zn BSF layer as in Fig. 6b, we calculated above that the $R_{sub\text{-}BG}$ can be increased by ~0.9%. However, the p-GaInP:Zn layer alone in this etched BCL case has higher resistance to lateral current transport than the combined p-GaInP:Zn/p-AlGaAs:C layers in the intact BCL case, with measured sheet resistance of 6100 Ω/sq and specific contact resistivity ρ_{cb} at the p-GaInP/Au contact of 2×10^{-5} Ω cm^2. The higher sheet resistance of the etched BCL case, increase resistive losses relative to the intact BCL case, tending to at least partially offset the $R_{sub\text{-}BG}$ reflectance advantage for the etched BCL structure.

Total fractional power loss in the PDBC structure is the sum of lateral conduction loss and contact resistance loss. In both the intact BCL and etched BCL cases, the fractional power loss in the PDBC is dominated by lateral conduction loss. For constant CCF, a smaller contact via diameter results in lower fractional power loss because the smaller metal contacts are spaced more closely together to maintain the same CCF, thus lowering the resistive losses due to lateral transport in the semiconductor. However, the fabrication challenges of forming very small contact vias are ameliorated if larger diameters and larger CCF can be used, at the same contact spacing. Lower CCF is preferred to achieve higher $R_{sub\text{-}BG}$, but higher CCF and closer contact spacing is preferred for lower R_{series}. Thus, for a given contact diameter that is achievable for a specific patterning technology, a trade-off exists in the contact spacing and corresponding CCF that is chosen, to maximize $R_{sub\text{-}BG}$ and minimize R_{series} in the quest for high GaAs TPV efficiency.

Based on the $R_{sub\text{-}BG}$ and R_{series} modeling and practical considerations, a CCF between 1% and 15% is chosen. To study the dependance of R_{series} on point contact diameter, 3 μm, 5 μm, 7 μm, 10 μm point contact diameters are chosen. Any point contact diameter less than 3 μm is hard to implement using i-line (UV - 365 nm) contact photolithography due to tool limitations. Point contact diameters greater than 20 μm would result in high resistive fractional power loss for CCF < 10% and therefore are not chosen. As there are multiple CCF's and point contact diameters under investigation, the spacing between the point contacts (pitch) is fixed at 28.8 μm. This corresponds to different PDBC configurations of 3 μm diameter = 1% CCF, 5 μm = 2.8% CCF,

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7 µm = 5% CCF, 10 µm = 11.2% CCF, with acceptable fractional power loss in the back contact. The process with a p-AlGaAs back contact layer selective etch is not implemented due to predicted high fractional power loss in the back contact which may result in low TPV efficiency.

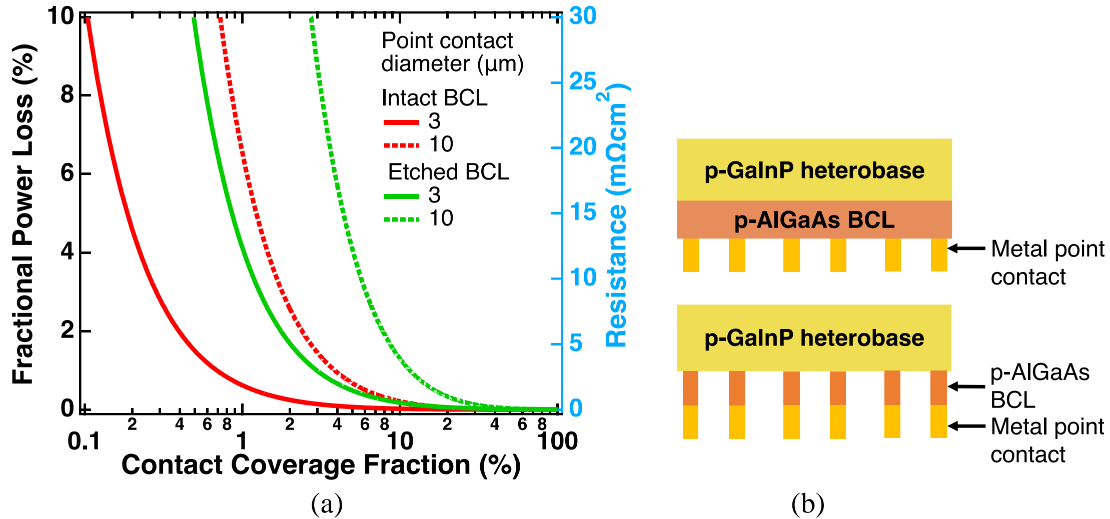

Figure 6. (a) Fractional power loss as a function of contact coverage fraction (CCF) in a PDBC of GaAs TPV device for metal point contact diameter 3 µm and 10 µm, and for p-AlGaAs back contact layer (BCL) intact and selectively etched everywhere except point contacts at J_{sc} 3.5 A/cm^2, typical of 2200°C blackbody spectrum. The secondary y-axis (right side) shows resistance contribution of PDBC at J_{sc}. (b) Schematic illustrating p-AlGaAs BCL intact (top) and p-AlGaAs BCL selectively etched with metal point contact as mask (bottom).

3. Experimental methods

3.1 MOVPE epitaxial GaAs TPV devices

The inverted GaAs devices were grown in a custom-built, atmospheric pressure, metal-organic vapor phase epitaxy (MOVPE) reactor. Single-crystal Si-doped (100) n-GaAs substrates miscut by 2° towards (111)B, were used for all the growths. Standard[48] metal-organic precursors were used in the MOVPE reactor; details can be found elsewhere[32]. As we will describe below, the processing sequence first involves fabrication of the PDBC back mirror. Then the sample was secured to a mechanical handle using epoxy and the growth substrate was removed by chemical etching. Finally, the front grids were deposited, and the individual devices were isolated by wet-chemical etching.

3.2 PDBC fabrication procedures

We explored numerous PDBC fabrication process flows to support selective BCL etching, different dielectrics, different fabrication methods, and other process sequence variations. Detailed discussion on these fabrication process flows, and advantages and disadvantages for each process can be found in a companion article[49] as they are beyond the

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scope of this study. In this study we investigate two specific PDBC fabrication process flows: Process A, in which a planar dielectric layer is deposited first, followed by patterning vias through the dielectric for the metal contact with reduced contact coverage fraction; and Process B, in which photoresist pillars are formed first, followed by blanket deposition of a dielectric layer, and then liftoff of the dielectric layer only in the regions over the photoresist pillars by etching away the photoresist, forming the contact vias through the dielectric. We describe these processes in below in the remainder of section 3 and discuss experimental results from them in section 4.

3.2.1 Process A for SU-8 photoresist as dielectric

Process A refers to a process in which vias are patterned in a continuous dielectric layer to form the metal contact regions with reduced contact coverage fraction. The vias may be formed by patterning holes in photoresist above virtually any deposited dielectric and etching away the dielectric in those regions, or as shown in Fig. 7a, the vias may be patterned by light exposure in a dielectric that is itself a photosensitive resist like SU-8. In this process, SU-8 is spin-coated on the back contact layer, and vias extending through the SU-8 are patterned and developed with photolithography. The p-AlGaAs back contact layer in the vias is electroplated with metals that are advantageous for forming a reflective electrical contact, followed by evaporated or sputtered metal to form the rear mirror. In this study, SU-8 6000.5 is diluted using CPG thinner from Kayaku Advanced Chemicals, Inc. at 60% volume/volume (%v/v) and this composition is hereafter referred as 60% SU-8. The average SU-8 thickness is 223 nm when spin coated at 6000 RPM.

3.2.2 Process B for evaporable dielectric

Process B as shown in Fig. 7b can be used for almost any dielectric deposited by a line-of-sight method such as thermal or electron-beam evaporation. An inversion or negative photoresist is first spin-coated on the back contact layer and is patterned photolithographically and developed to form photoresist pillars of the desired diameter, and which are undercut at their edge. The presence of an undercut, such that the diameter of the photoresist pillar is greater at the top than at the bottom, is essential to provide a clean break in the deposited dielectric at the edge of the pillars, and to remove the dielectric above the pillars (liftoff) by dissolving the photoresist pillars after dielectric deposition. The photoresist pillars are lifted off by agitating the sample for 20 minutes in Remover PG from Kayaku Advanced Chemicals, Inc. heated to 95°C followed by ultrasonicating the sample in Remover PG for 20 mins. This results in a dielectric film with vias where the photoresist pillars once stood. Metal point contacts are then formed in the vias, which may be done in a separate step prior to depositing the back mirror metal on top of the dielectric, or in the same step as the back mirror metal.

Both processes[49] A and B have variations other than the specific sequences shown in Fig. 7, but the processes in Fig. 7 are simple and highly manufacturable, and are the processes used to produce devices in this study.

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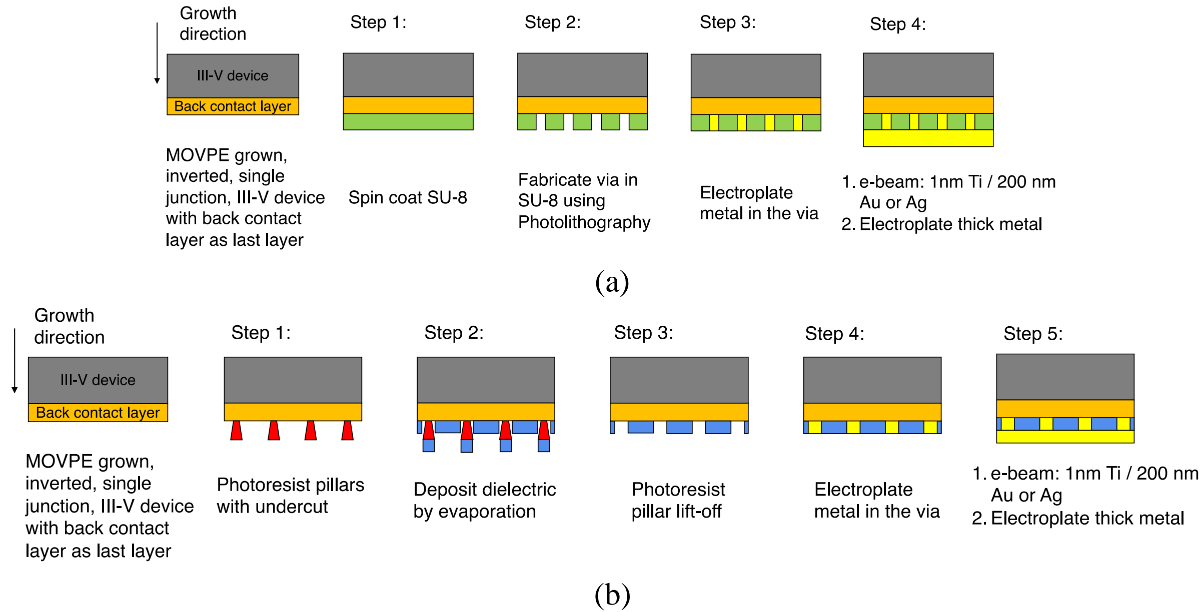

Figure 7. Schematic of PDBC fabrication process flows (a) process A for SU-8 photoresist as dielectric (b) process B for any evaporable dielectrics.

3.3 Point contact and back mirror fabrication

The back mirror is fabricated using evaporated Ag and the point contacts for electrical conduction are fabricated with Au through the dielectric to the AlGaAs back contact layer. Au point contacts to p-AlGaAs:Zn with 3.5×10^{19} cm^{-3} Zn doping showed a very low specific contact resistivity of 1×10^{-6} Ω cm^2 for 100% CCF, measured with circular TLM pads[50]. Electroplated Au point contacts are used instead of Ag point contacts for the following reasons. Electromigration of Ag[51] at very high operating current densities into GaAs emitter can seriously impair the device electrical performance by increasing the non-radiative recombination rate. The final step after device mesa isolation in device fabrication is selective front contact layer etch in 2:1:10 NH_4OH:H_2O_2:H_2O etchant, which will also etch the exposed Ag metal point contacts in the non-epi area, eventually the underlying e-beam evaporated Ag mirror with detrimental effects on the device. However, Au point contacts embedded in the dielectric spacer layer masks the underlying e-beam evaporated Ag mirror, thus preventing unwanted etching and device damage.

Adhesion between dielectric and blanket mirror metal such as Au or Ag was insufficient without an adhesion metal such as Ti or Cr deposited on top of the dielectric, and devices without this adhesion layer either cracked or detached from the substrate during the substrate removal process or during the mesa isolation process. An adhesion layer of 1 nm Ti on top of SU-8, or 2.5 nm Ti on top of e-beam evaporated dielectrics such as SiO_2 resulted in good adhesion and solved this problem. Because of the large reflectance penalty, the adhesion layer

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thicknesses used with each dielectric were made as thin as possible to provide sufficient adhesion and no thicker.

Thus, the blanket metal used for the back mirror in the experiments described below consists of a Ti adhesion layer with either 1 nm or 2.5 nm thickness, followed by 200 nm Ag.

3.4 Inverted device fabrication

After PDBC fabrication, the PDBC side of the GaAs device was bonded to a silicon handle substrate using a low viscosity epoxy[52]. The epoxy was cured at 100°C for 20 minutes on a hot plate. The GaAs substrate was completely etched off in 1:3 NH_4OH:H_2O_2 at room temperature in 20 minutes, revealing the GaInP etch stop layer. The etch stop layer was etched off in undiluted HCl revealing the GaAs/GaInNAs front contact layer. In a first photolithography step, the front grid was defined on the front contact layer using SPR 220 4.5 photoresist from Dow Chemicals followed by electroplating Ni and Au. After a second photolithography step, the devices were masked in photoresist, and were mesa isolated by alternating etching of unmasked device area of arsenide layers with 3:4:1 H_3PO_4:H_2O_2:H_2O etchant, and phosphide layers with concentrated HCl etchant. Finally, the front contact layer was etched off everywhere except beneath the front grids using 2:1:10 NH_4OH:H_2O_2:H_2O to increase the light transmission to the absorber layer.

3.5 Fourier transform infrared spectroscopy (FTIR) reflectance measurement

All measurements are conducted on an integrating sphere (PIKE technologies) coated with diffuse gold using the substitution method. A typical reflectance measurement is constructed from measurements of the following configurations:

1. Light is directed to the sample port with no sample in place.
2. The reflectance standard is placed on the sample port.
3. The sample of interest is placed on the sample port.

These three measurements are used with the tabulated reflectance spectrum of the reference to calculate the sample's reflectance spectrum. We note that the average reflectance of the integrating sphere changes in each case, which we account for with a correction term based on the geometry of the sphere[53] .

We use a NIST standard with a reflectance known to ± 0.3% absolute and have found an uncertainty of 0.4% introduced by sample-to-sample deviations, resulting in a ±0.5% uncertainty on our measurements. Measurements of separate NIST-calibrated samples referenced to our primary NIST standard yield reflectance values within the uncertainty bounds of the tabulated values.

We use a FTIR instrument to measure reflectance at the long wavelengths out to 15 µm that impact the total integrated sub-bandgap reflectance $R_{sub\text{-}BG}$, weighted by the 2200°C blackbody spectrum. For all $R_{sub\text{-}BG}$ values measured by FTIR, the total (diffuse + specular) reflectance is measured at an incident angle of 12° from the normal, from 0.95 to 10 µm wavelength. The short end of this range at 0.95 µm is used instead of the 0.871 µm GaAs

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bandgap wavelength to avoid low-intensity interference fringes in the reflectance spectrum close to the bandgap which may be a result of thickness variation in the GaAs device, and which could artificially lower R_{sub-BG}, even if the device is highly reflective. Similarly, the long end of this range at 10 μm is used as the blackbody power density for >10 μm is negligible. All the R_{sub-BG} values measured by FTIR have a measurement error bar of ± 0.5%, in absolute % reflectance.

4. **Experimental results and discussion**

Figure 8a shows the reflectance of GaAs TPV device structures with no front grids measured using Fourier transform infrared spectroscopy (FTIR) with SU-8 and SiO_2 patterned dielectric back contacts, as well as for a 100% CCF (planar, full metal) Au back contact. The reflectance was measured from 0.6 to 15 μm while Fig. 8a plots the range 0.8 to 2.5 μm to show details more clearly. The contact coverage fraction of the SU-8 PDBC in Fig. 8a was 4.0%, while for the SiO_2 PDBC it was 3.6%. The normalized blackbody spectral irradiance is superimposed on this reflectance plot to indicate that most sub-bandgap blackbody power at 2200°C is distributed between 0.9 μm and 2.5 μm.

Figure 8a shows that the valleys of the reflectance interference fringes for PDBC devices are shallow compared to the device with 100% CCF Au back contact, indicating that absorption observed with a planar Au back contact can be reduced by adding a dielectric spacer. The valleys of reflectance interference fringes for the GaAs SiO_2 PDBC device are lower than for the GaAs SU-8 PDBC device, indicating higher absorption across a broad range of wavelengths. The stronger absorption for the 2.5 nm Ti adhesion layer used with the SiO_2 PDBC device than for the 1 nm Ti in the SU-8 PDBC device is likely a strong contributor to this effect.

Separate studies of the absorptance of Ti films of varying thickness indicate that the magnitude of absorption in Ti films is consistent with the difference in reflectance between the SU-8 and SiO_2 PDBC samples with different Ti adhesion layer thickness. We hypothesize that the dominant cause of the reflectance difference between these specific samples is due to their different Ti layer thicknesses, since modeling of these structures using different Ti thicknesses and the optical constants of SU-8 and SiO_2 shown in Fig. 5b indicates this to be the case, but this hypothesis is as yet unproven.

Figure 8b shows that the ideal 0% CCF GaAs SU-8 PDBC gives the highest experimental R_{sub-BG} of 96.7%. This is a 1.4% absolute improvement compared to the 95.3% measured R_{sub-BG} of the baseline case of 100% CCF Au, and a 2.4% absolute improvement over 94.3% R_{sub-BG} for the same 1 nm Ti / Ag metal stack without SU-8 that was used in the 0% CCF case. The highest R_{sub-BG} measured for the SU-8 patterned back contact is 96.5% at 4.9% CCF, 1.2% higher than the baseline 100% CCF Au, despite the presence of 1 nm Ti in for the PDBC that was not present in the full coverage 100% CCF case.

The highest R_{sub-BG} measured for the GaAs SiO_2 PDBC is 94.7% at 11% CCF which is 0.5% lower than 100% CCF. As discussed above, the thicker 2.5 nm Ti layer is a likely cause of these lower values for these SiO_2 PDBCs.

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The measured R_{sub-BG} is higher than the calculated R_{sub-BG} from ID TMM modeling for both 0% and 100% CCF SU-8 PDBC. For 100% CCF this deviation between measured and calculated R_{sub-BG} is within the measurement error of 0.5%, but the deviation at 0% CCF is significant. This deviation is possible if the optical constants or device thickness used in the calculation do not match the actual device parameters because of non-uniform growth. We note that measured and calculated R_{sub-BG} values agree very well for the 100% CCF 1 nm Ti / Ag device structure indicating good agreement between experimental and modeled device layer thickness and doping in this case.

For both SU-8 and SiO_2 PDBC structures, linear fits to experimental R_{sub-BG} vs. CCF data show a rapid decrease in reflectance with rising CCF, deviating significantly from the calculated 1D TMM model. The linear fits to experimental data in the 4-30% CCF range indicate that at higher CCF, R_{sub-BG} is projected to be lower than even the 100% CCF case, for both SU-8 and SiO_2 PDBCs. This indicates that the PDBC is significantly deviating from the approximations made in the 1D linear interpolation approximation. For via spacing less than ~10 µm, light diffraction in the range of interest for sub-bandgap reflection from the array of metal-filled vias in the dielectric can be significant, scattering light at wider angles than the incoming angular distribution, and thus increasing sub-bandgap absorption in the device[42]. For a constant via diameter, this effect becomes stronger for increasing contact coverage fraction, as the via spacing decreases with rising CCF. So, at higher contact coverage fractions, and particularly for small via diameter and spacing, reflectance from the PDBC structure should be modeled using 3D optical algorithms, such as rigorous coupled-wave analysis (RCWA)[54] and finite-difference time-domain (FDTD)[55] models, rather than simple 1D approximations.

Figure 8c plots the experimental R_{sub-BG} values measured by FTIR for GaAs TPV devices with SU-8 patterned dielectric back contacts, with and without a front grid on the devices. The measured R_{sub-BG} is significantly lower for PDBC devices that have a ~10-µm-thick Au front grid compared to no front grid. This was not expected from first principles, since the gold front grids should in principle also be highly reflective. We note that the trends in R_{sub-BG} as a function of CCF are similar in PDBC devices both with and without front grids. Among samples with a front grid, the highest measured R_{sub-BG} is 94.9% at a 4.0% CCF for GaAs TPV devices with an SU-8 PDBC, which is only 0.5% higher than for a 100% CCF Au back contact device, also with a front grid. The present data in Fig. 8c and its experimental variation is consistent with an explanation based on front-grid light scattering, due for instance, to rougher side walls, inverted trapezoidal finger profile, and resulting light trapping due to thick front grids. The present data cannot confirm if there is an interaction between scattering induced by front grids and the patterned dielectric back contact, or if their effects are simply additive, though that is an area for future investigation.

Figure 8d plots the experimental diffuse reflectance component weighted to 2200°C blackbody spectrum, measured by FTIR for GaAs TPV devices with SU-8 patterned dielectric back contacts, with and without front metal grids on the devices. The diffuse reflectance is significantly lower for samples without front grids than for those with front grids. In particular, for 100% CCF planar Au back contact samples for which there is no patterning of the back contact to add to the diffuse reflectance, the measured diffuse reflectance is within noise limits for the sample with no front grids, and is taken as 0% (*i.e.*, the planar back reflector is mostly

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specular). For the corresponding sample with a planar Au back contact but with front grids, the median diffuse reflectance measured is ~11%. This comparison strengthens the argument that the front grids cause a significant increase in diffuse reflectance, separate from that of the back contact. For PDBC devices, increasing CCF causes an increasing diffuse reflectance component which strengthens the argument that the PDBC should be treated as a three-dimensional diffraction grating.

Figure 9 shows the R_{series} of GaAs PDBC TPV devices as a function of contact coverage fraction. All the devices have the same device structure and differ in the PDBC where the point contact diameter and the CCF are different with a constant point contact pitch of 28.8 µm. The PDBC is made up of SU-8 dielectric spacer, Ni/Au point contact, 150 nm e-beam evaporated Ag, and 2 µm electroplated Au. The additional 2 µm thick electroplated Au is to reduce the backside sheet resistance of the device. The contact resistance of Ni/Au and Au with the p-AlGaAs back contact layer was measured using C-TLM and found to be similar. Also modeling in section 2.3 indicates that the resistive loss contribution of the PDBC is dominated by the sheet resistance loss while the contact resistance loss is minimal.

The device front grids may also contribute significantly to the device R_{series} if they are not optimized to handle the current density generated by the TPV radiation. The front grids are made of electroplated Au with inverted trapezoidal grid fingers with a thickness of ~10 µm, bottom width of ~7 µm, and top width of ~14 µm, and are spaced 190 µm apart. The grid lines are 8 mm long and current is collected by busbars at both ends, effectively halving the distance current must travel along the fingers to 4 mm. The two rectangular busbars are 900 µm wide and 8 mm long. This is a tight grid spacing and a high metal coverage fraction on the front side compared with one-sun solar PV. This corresponds to an R_{series} contribution of about ~2 mΩ-cm^2 in the front grid metal. The semiconductor front contact layer is composed of 100 nm n-GaAs and 200 nm GaInAs and is present only beneath the Au front grid. The contact resistance of Au to the

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front contact layer and p-AlInP window layer is 7×10^{-6} Ωcm^2 and the sheet resistance is 51 Ω/sq as measured using C-TLM pads.

R_{series} was calculated using a generalized optoelectronic model[56] by fitting the dark-IV, external radiative efficiency, and the multiple-suns IV data together. The R_{series} of baseline GaAs TPV device with 100% CCF Au back contact was calculated to be 3.9 mΩcm^2 indicated by blue

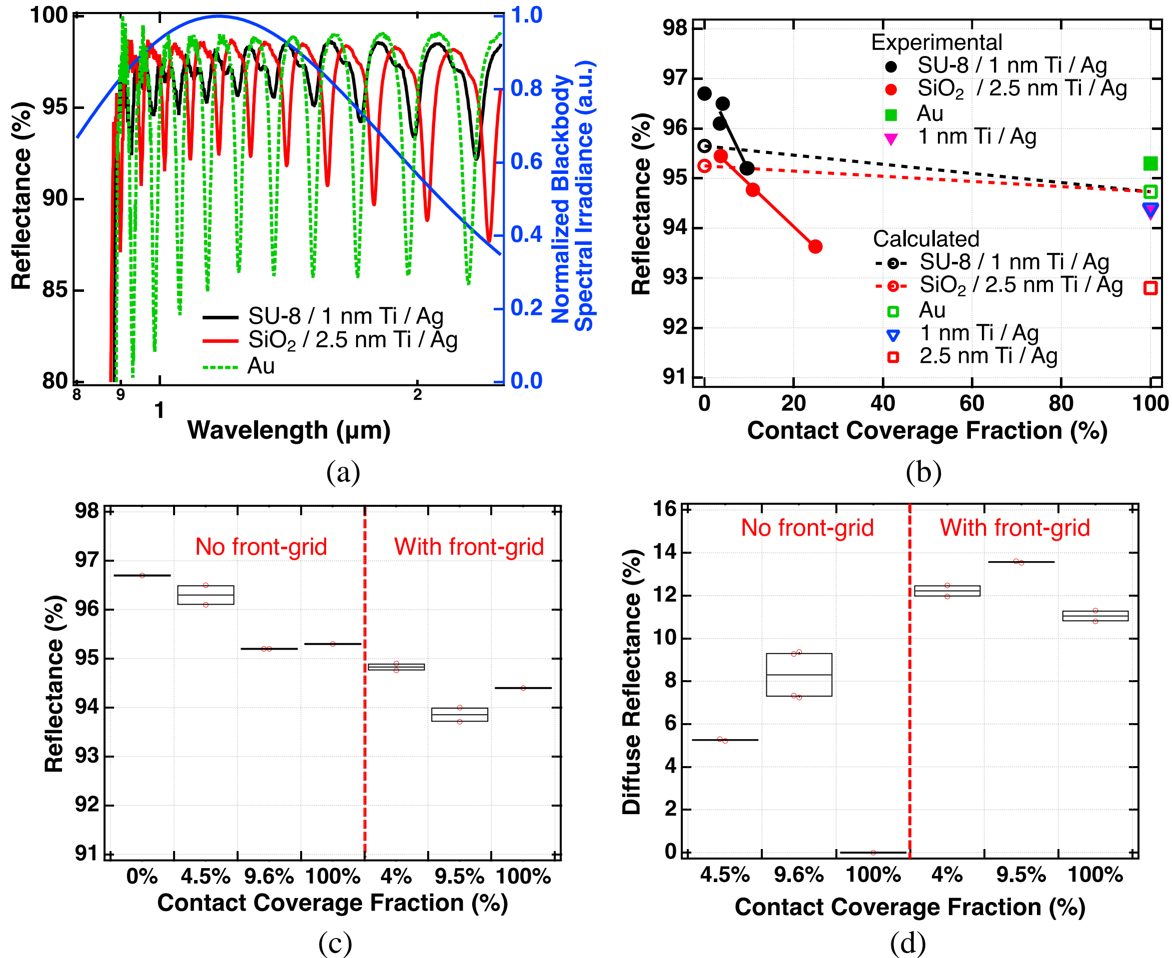

Figure 8. (a) Reflectance of GaAs TPV device with SU-8 and SiO_2 PDBC, without front-grid, at similar contact coverage fraction, as a function of wavelength zoomed in from 0.8 to 2.5 μm where the blackbody spectrum at 2200°C has the most power. The right y-axis is normalized blackbody spectral irradiance at 2200°C. (b) FTIR measured and calculated sub-bandgap reflectance weighted to 2200°C blackbody spectrum as a function of contact coverage fraction for different GaAs TPV devices without front grids. Solid line is linear fit to the R_{sub-BG} data. Dashed line is TMM-calculated weighted reflectance interpolated between 0% CCF and 100% CCF. (c) FTIR measured sub-bandgap reflectance weighted to 2200°C blackbody spectrum as a function of contact coverage fraction (CCF) for GaAs SU-8 PDBC TPV devices with and without front-grids. (d) FTIR measured diffuse component of sub-bandgap reflectance weighted to 2200°C blackbody spectrum as a function of contact coverage fraction (CCF) for GaAs SU-8 PDBC TPV devices with and without front-grids. FTIR R_{sub-BG} has a measurement error bar of ±0.5% absolute.

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dotted line which is one of the lowest R_{series} measured in this study. R_{series} of the PDBC devices decreases with increasing CCF which is consistent with the calculations shown in section 2.3. With increasing CCF, the lateral current path length decreases which decreases the effective PDBC sheet resistance leading to lower resistive loss. The maximum measured R_{series} for a GaAs PDBC TPV device was 8.5 mΩcm^2 for 1% CCF. As $R_{sub\text{-}BG}$ has a stronger impact than R_{series} on TPV efficiency, R_{series} less than 10 mΩcm^2 should still yield a high TPV efficiency.

As discussed in section 2.1, $R_{sub\text{-}BG}$ improvement over 1% leads to a predicted TPV efficiency improvement over 3%. Combining the measured FTIR $R_{sub\text{-}BG}$ and the calculated R_{series}, the GaAs TPV device efficiency can be predicted. The maximum measured $R_{sub\text{-}BG}$ of an electrically inactive GaAs TPV test device with no front-grid at 4.9% CCF is 96.5% which may yield a theoretical TPV efficiency of ~36% at 2200°C thermal emitter temperature. Similarly, $R_{sub\text{-}BG}$ of electrically active GaAs TPV device with front-grid at 4% CCF is 94.9% which would be predicted to yield a theoretical TPV efficiency of ~33% at 2200°C thermal emitter temperature. Assuming both the TPV devices with and without front-grid have a same R_{series} of ~8.5 mΩcm^2.

The recommended optimal parameters for GaAs PDBC TPV devices based on the experimental $R_{sub\text{-}BG}$ and R_{series} are use of SU-8 over SiO_2 dielectric due to the need for a thinner, less absorptive, 1 nm Ti adhesion layer; a CCF in the 1% - 5% range; and a point contact diameter in the 3-10 μm range. This configuration will yield $R_{sub\text{-}BG}$ greater than 96%, provided that lower reflectance with addition of front metal grids can be addressed, R_{series} less than 10 mΩcm^2 for front metal grid thickness greater than 10 μm, and in principle, a GaAs TPV efficiency greater than 33%.

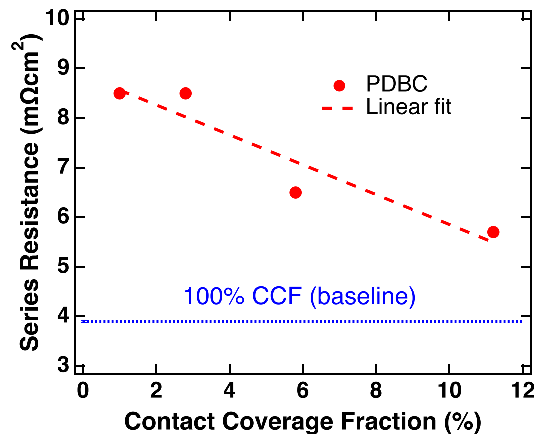

Figure 9. Series resistance of GaAs PDBC TPV devices as a function of contact coverage fraction calculated using optoelectronic model by simultaneously fitting the dark I-V, external radiative efficiency, and multiple-suns IV measurements. The 100% Au planar back contact device series resistance is indicated as dotted blue line.

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5. Conclusion

We have modeled, designed, and fabricated GaAs patterned dielectric back contact (PDBC) thermophotovoltaic (TPV) devices, for high-temperature energy storage, with and without front grids, and measured the long-wavelength reflectance. We have shown that for high TPV conversion efficiency it is essential to maximize the sub-bandgap reflectance and minimize the series resistance. It was found that GaAs TPV devices can be fabricated with patterned dielectric back contacts for improved sub-bandgap reflectance without compromising the electrical back contact. Multiple processing methods to fabricate PDBC structures were explored, which vary according to the dielectric spacer material and the need to etch the back contact layer. We then fabricated GaAs PDBC TPV devices with SU-8 and SiO_2 dielectric layers, as well as with and without front grids to quantify light scattering and reflection from PDBC structures and the front grids.

We measured the total sub-bandgap reflectance using FTIR and found that a GaAs SU-8 PDBC structure with the limiting case of 0% CCF shows the highest $R_{sub\text{-}BG}$ of $(96.7 \pm 0.5)\%$, while PDBC structures with 4.9% CCF still have a very high measured $R_{sub\text{-}BG}$ of $(96.5 \pm 0.5)\%$ with no front-grid. Both values are a >1% absolute improvement over the baseline $R_{sub\text{-}BG}$ of $(95.3 \pm 0.5)\%$ for GaAs TPV devices with 100% CCF Au back contact, with no front-grid. We also show the measured $R_{sub\text{-}BG}$ for GaAs SiO_2 PDBC structures to be lower than the baseline 100% CCF, likely due to the thicker Ti adhesion layer used on SiO_2. The slopes of linear fits to experimentally measured $R_{sub\text{-}BG}$ for GaAs PDBC TPV devices are very high compared to 1D TMM linear interpolation model. This suggests that the array of metal-filled vias in the PDBC exhibits substantial diffraction as well as specular reflection; it thus cannot be approximated by a simple 1D linear interpolation model and should be treated as a diffraction grating. We also show that measured $R_{sub\text{-}BG}$ for GaAs SU-8 PDBC devices with a metal front grid is lower than for test devices without a front grid, likely due to light scattering from the front grid. We experimentally derived R_{series} of the GaAs TPV devices as a function of CCF and the maximum measured R_{series} was ~8.5 $m\Omega cm^2$ at 1% CCF. Combining the FTIR measured $R_{sub\text{-}BG}$ of 94.9% and experimentally derived R_{series} of ~8.5 $m\Omega cm^2$, the predicted TPV efficiency for GaAs PDBC device with 4% CCF and with front-grid is ~33% at 2200°C.

Acknowledgements

The authors thank W. Olavarria, A. Kibbler and J. Carapella for MOVPE growth, and M. Young, J. Buencuerpo, M. Steger, P. Ndione, S. Babcock, Z. Holman, C. Wu, and Z. Yu for useful conversations. This work was authored, in part, by the Alliance for Sustainable Energy, LLC, the manager and operator of the National Renewable Energy Laboratory for the U.S. Department of Energy (DOE) under Contract No. DE-AC36-08GO28308. Funding was provided by the U.S. Department of Energy (DOE): Advanced Research Projects Agency – Energy (ARPA-E) under cooperative agreement DE-AR0000993. The views expressed in the article do not necessarily represent the views of the DOE or the U.S. Government. The U.S. Government retains and the publisher, by accepting the article for publication, acknowledges that the U.S. Government retains a nonexclusive, paid-up, irrevocable, worldwide license to publish or reproduce the published form of this work, or allow others to do so, for U.S. Government purposes.

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