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Award Number	DE-EE0007553	
Project Title	New Approaches to Low-Cost Scalable Doping of Interdigitated Back Contact Silicon Solar Cells	
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Submitting Official Signature	Sumit Agarwal	

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Executive Summary: The goal of this project was to develop novel approaches to patterning of dopants in the rear fingers of interdigitated back contact (IBC) Si solar cells to reduce the cost of manufacturing this high-efficiency-potential cell architecture. The work throughout this project can be divided into four categories: (a) development of dopant patterning technique using laser scribed Si contacts masks that are mechanically aligned with ~10 μm resolution to the underlying Si substrate; (b) measuring dopant spreading profiles in the isolation region between *n*- and *p*-type dopant fingers during plasma-enhanced chemical vapor deposition (PECVD) of doped hydrogenated amorphous silicon (*a*-Si:H) via shadow masks, and dopant desorption and re-adsorption during high-temperature annealing; (c) understanding the role of dopant compensation on the shunt resistance in contaminated isolation regions through analysis of defect-enhanced compensation; and (d) simulation and fabrication of passivated two-sided grid and back-contact solar cells to demonstrate the use of direct dopant patterning in cell fabrication. For the passivated two-sided grid solar cells, masked deposition was used to demonstrate an improvement in the blue response of the cell by creating a shallow front emitter. During development of the masked PECVD patterning process, we measured 3-D dopant profiles using secondary ion mass spectrometry. After deposition, in the masked region, the phosphorus dopant tail was >100 μm at concentrations >10^{19} cm^{-3} while the boron dopant tail was shorter. During high-temperature crystallization of doped *a*-Si:H films to polycrystalline Si (*poly*-Si), phosphorus atoms spread by desorbing from the *poly*-Si surface and re-adsorbing onto intrinsic *poly*-Si on adjacent wafers that were separated by several millimeters. These contamination mechanisms resulted in a decrease in resistivity from ~10^{5} Ω·cm for intrinsic *poly*-Si to ~10^{-1} Ω·cm for contaminated *poly*-Si. Mitigation strategies for each contamination mechanism were developed to maintain a resistivity of ~10^{5} Ω·cm between doped fingers. During fabrication of the 209 cells created during this project, it was found that despite contamination of the IBC gap through the abovementioned mechanisms, high shunt resistances and *FF* ~75% were still reached. Investigation into this led to the discovery of defect-enhanced compensation which exists within highly defective *poly*-Si when net doping concentrations reach the value of defect density (~10^{18} cm^{-3} for many *poly*-Si films). Simulations guided us in the fabrication of IBCs and the cells fabricated were able to meet the year-end goals for BP 2 and 3 of 15% and 17% IBC cell efficiency, as well as the BP 4 goal of a 1% absolute increase in efficiency for PERC-like devices. However, the most efficient cell created during this project of 18.6% fell short of the 21% final project target. While the champion device fell short in V_{oc} and J_{sc}, many devices fabricated were able to reach the necessary goals of ~40 mA/cm^2, ~700 mV, and ~75% FF required for a 21% device. The results generated from this project were disseminated through 11 conference presentations and proceedings. Presentations included oral talks at 2019 IEEE PVSC, 2019 MRS Fall Meeting, 2020 PVSEC-30 and 2021 IEEE PVSC, as well as poster presentations at 2020 IEEE PVSC and 2021 SiPV. The project resulted in 2 peer reviewed publications – one published in IEEE Journal of Photovoltaics and one in ACS Applied Energy Materials. The information gained in this project will aid in development of improved processes for fabrication of high-efficiency solar cells and other areas of the semiconductor device industry as well. The IBC cells will also pave the way for higher efficiency tandem devices. Through further manufacturing of high-efficiency solar cells, more of the world's energy demands can be met through renewable sources, helping to stave off the worst effects that may come about from global climate change.

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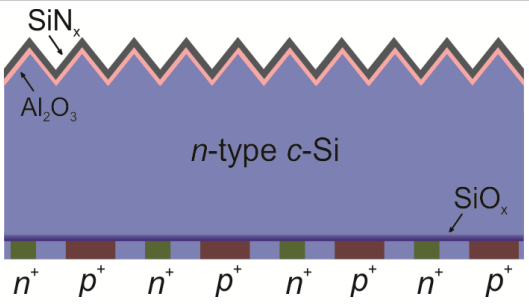

Figure 1: Schematic of an IBC *c*-Si solar cell. The front architecture of the solar cell consists of SiN_x on textured *c*-Si wafer with an Al_2O_3 passivation layer. The n^+- and p^+-doped *poly*-Si contacts are at the back of the cell. A 1–2-nm-thick tunneling SiO_x layer separates the *c*-Si bulk from the doped *poly*-Si contacts. The metal contacts are on the back side are not shown.

I. Background: Ultra-high-efficiency *c*-Si solar cells provide one of the most promising pathways to achieve the $0.02-0.03/kWh levelized cost of electricity target by 2030. Amongst the different types of industrially manufactured designs for *c*-Si solar cells, interdigitated back contact (IBC) cells are the most efficient and can provide ~25% efficiency by reducing recombination and shading losses. At the research scale, IBC cells hold the record efficiencies of single-junction Si solar, with 26.6% efficiency for silicon heterojunction [1, 2] and 26.1% efficiency for polycrystalline silicon on silicon oxide (*poly*-Si/SiO_x) [3-5] passivated contacts. These record high efficiencies motivate researchers to investigate further the potential of this cell architecture in industrial manufacturing. However, this type of cell only accounts for a small fraction of the *c*-Si solar cells that are currently manufactured due to the process complexity and high cost. One of the critical steps in the manufacture of high-efficiency IBC cells is patterned doping of the back contacts, which adds several additional steps compared to the more traditional front-grid architecture. The *poly*-Si/SiO_x contact architecture is the focus of this project, though the patterning method used in Ref. [3] (photolithographically-masked ion implantation) is not preferable due to the high capital cost of ion implantation and many processing steps required for photolithography. Additionally, it has been shown that the region between doped *p*- and *n*-type fingers is of considerable importance [6], so we have characterized it extensively in our studies. In the proposed work, we develop a simpler technique for direct patterning of *p*- and *n*-type *a*-Si:H without photolithography. The proposed method has the potential to be highly scalable for large-area manufacturing, and cost effective.

II. Project Objectives: IBC *c*-Si solar cells require very precise patterning of dopants on the back surface to create contacts for the collection of the electrons and holes. Conventional dopant patterning techniques such as photolithography and ion implantation are either too complicated or too expensive for large-scale manufacturing, preventing the proliferation of IBC *c*-Si solar cells in commercial manufacturing even though such cells have the highest reported efficiency for *c*-Si solar cells. Because of this, it is imperative that simpler and reliable dopant patterning techniques are developed to make such type of cells more competitive with other types of *c*-Si solar cells such as the PERC cells. In the proposed cell design for this PVRD project, the back side of the *c*-Si IBC cell consists of *poly*-Si with alternating n^+- and p^+-doped regions, that are separated by an intrinsic *poly*-Si layer as shown schematically in Figure 1. These doped regions that form the back contacts, generally require patterning during the cell manufacturing process, which consists of numerous and complex steps including photolithography. This additional complexity in processing has prevented production of IBC cells from being scaled up industrially. In this project, we developed a masked plasma deposition patterning process for *p*- and *n*-type *a*-Si:H for direct dopant pattering without photolithography. A simplified process flow

diagram for IBC cell fabrication is shown in Figure 2. The proposed method would be highly scalable for large-area manufacturing, and cost effective. This dopant patterning methodology can also be applied to directly pattern the front emitter such that the poly-Si layer is thicker underneath the metal, but very thin between the metal fingers to improve the blue response of the cells. The goals for each budget period are shown in simplified form below.

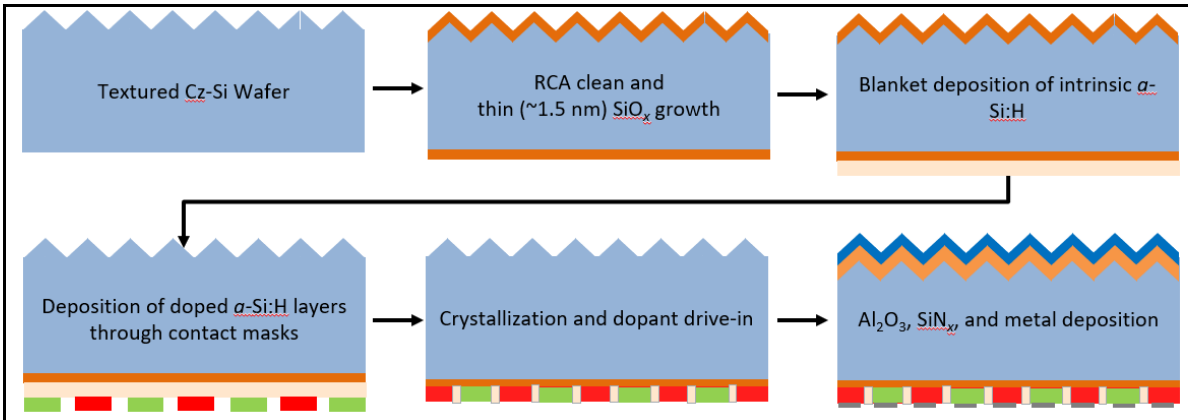

Figure 2: Process flow for the fabrication of an IBC solar cell based on *poly*-Si on SiO_x passivated contacts.

Budget Period 1:

Task 1: (M1-M12) Develop the photo-CVD process.

Subtask 1.1: Modify a plasma CVD tool to introduce an ultra-violet (UV) light source (~250 – 350 nm) that can illuminate an area of 20 × 20 mm^2.

Milestone 1.1 (Quarter 1): Ensure we can measure light emission from the UV source in the ~250 – 350 nm range through a crystal quartz, LiF, or MgF_2 window.

Subtask 1.2: Deposit intrinsic *a*-Si:H films using photo-CVD and demonstrate UV-induced surface activation.

Milestone 1.2 (Quarter 2): Demonstrate the feasibility of UV-induced activation of surface sites on *a*-Si:H to promote surface hydrogen desorption for enhanced reactivity at low temperatures.

Subtask 1.3: Characterize the *a*-Si:H films using vibrational spectroscopy and ellipsometry to determine the structure, composition, and optical constants.

Subtask 1.4: Fabricate proximity masks with 1 mm wide slits and use these masks for patterned *a*-Si:H growth.

Milestone 1.3 (Quarter 4): Deposit 30-50 nm thick, patterned intrinsic *a*-Si:H films and show clear separation between the line patterns with abrupt step edges using profilometry.

Budget Period 2:

Task 2: (M13-M24) Integrate the photo-CVD process with thin film processing for IBC cells in the film Si growth cluster tool.

Subtask 2.1: Design and integrate a UV light source in one of the CVD chambers within the film Si processing cluster tool and/or stand-alone CVD tool with doping capability.

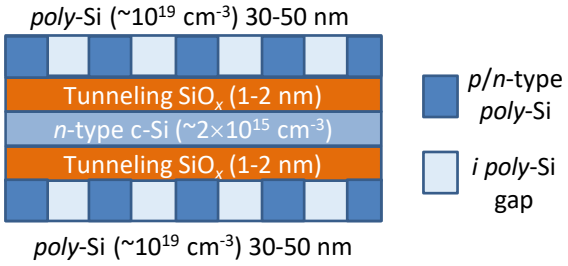

Figure 3: Schematic of the test structure for measure iV_{oc} using the Sinton lifetime tool. Milestone 2.3 (Quarter 8).

Subtask 2.2: Implement and test the photo-CVD process in the cluster tool or/and stand-alone CVD tool (both with doping capability) and reproduce results from the test chamber used in Budget Period 1.

Milestone 2.1 (Quarter 6): Deposit ~10 nm of patterned *a*-Si:H over *c*-Si substrates larger than 20×20 mm and show clear separation between the line patterns with abrupt step edges using profilometry.
Modifications to the SOPO begin after Quarter 7. We also sought a no-cost extension, where Budget Period 2 was be extended out to December 31, 2018 instead of the previous end date of July 30, 2018.

Subtask 2.3: Establish if plasma etching, plasma CVD, or a direct printing technique can be used for patterning of *doped a*-Si:H.

Milestone 2.2 (Quarter 7): Identify the most promising of the three techniques above for patterning and show that we can obtain doping levels of 10^{19} cm^{-3} using SIMS/Hall measurements for the doped lines and resistivity >100 Ω·cm between adjacent lines.

Subtask 2.4: Develop a method for mask alignment for interdigitated patterning for cell fabrication in BP3.
Milestone 2.3 (Quarter 8): Show iV_{oc} >680 mV using the Sinton lifetime tool for patterned test structures (see Fig. 3) fabricated using plasma etching, plasma CVD, or a printing method.

Budget Period 3:

Task 3: (M25-M36) Address the scientific and engineering challenges in process integration including: a) spatial limitations in dopant patterning posed by the most promising technique and b) electronic quality of the patterned contacts.

Subtask 3.1: Employ 2-D simulations using Quokka 2 to optimize the cell design.

Milestone 3.1 (Quarter 9): A quantitative table of limiting factors in cell design using simulations, and a detailed step-by-step plan to incorporate these into fabrication.

Subtask 3.2: Confirm the predictions for cell design obtained from 2-D simulations with experiments and incorporate these parameters into experiment.

Milestone 3.2 (Quarter 10): Optimize the processing conditions, masks, and mask alignment (thermal expansion etc.), to obtain n^+- and p^+-type interdigitated

a-Si:H/poly-Si patterns on *n*-type *c*-Si substrates based on the simulations in Quarter 9, with a dopant concentration above 10^{19} cm^{-3}.

Subtask 3.3: Establish the process conditions for lines with active dopant concentration of above 10^{19} cm^{-3}, and low contact resistances for the *p*-PERC architecture.

Milestone 3.3 (Quarter 11): Demonstrate the dopant patterning technique developed for front emitter of *p*-PERC cells for fabrication of shallow emitters.

Subtask 3.4: Create p^+-poly-Si/intrinsic-poly-Si/n^+-poly-Si patterned contacts using a physical mask set that provides regions of *p*- and *n*-type Si of approximately equal widths, separated by an intrinsic *poly*-Si gap of few MΩ/□, with a pitch of about 1 mm.

Milestone 3.4 (Quarter 12): Using masked PECVD patterning, show 15% efficient IBC cell structures (see Fig. 4) with a total pitch of ~1 mm and increase *p*-PERC cell efficiency by 0.5% absolute compared to a baseline architecture without patterned doping.

Budget Period 4:
Task 4: (M37-M48) Address bottlenecks in cell efficiency to reach a target high efficiency of ~21%.

Subtask 4.1: Address bottlenecks that limit cell efficiency and mitigate losses due to imperfect pattern alignment of the metal fingers.

Milestone 4.1 (Quarter 14): Demonstrate *c*-Si IBC cell with 17% efficiency.

Subtask 4.2: Optimize the line doping method for *p*-PERC architecture to reduce line width from 200 to 150 mm for 50-70 mm metal fingers.

Milestone 4.2 (Quarter 15): Using surface profiling with SIMS, verify that the heavily doped *n*-type region of the emitter for the *p*-PERC cell is ~150 mm wide.

Subtask 4.3: Address in detail the whole set of engineering issues related to reaching 21% efficiency, and specific to this patterning technique: doping non-uniformity over 20×20 mm area, edge isolation, reduced shunting by properly engineered gap between *n*- and *p*-contacts, contact metallization and its patterning.

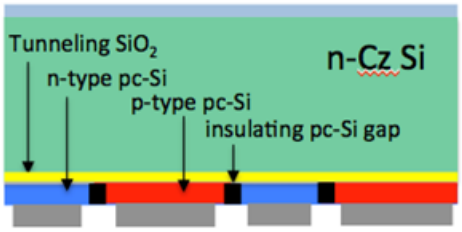

Figure 4: Schematic of the IBC *c*-Si solar cell structure. Front texture is not shown for simplicity.

Milestone 4.3 (Quarter 16): Obtain a 20×20 mm^2 *c*-Si IBC cell with certified efficiency of ~21%. Use patterned doping to increase PERC cell efficiency by 1% absolute compared to a non-patterned baseline.

Final Deliverable (Budget Period 4): Fabricate a 21% efficiency 20×20 mm^2 IBC *c*-Si solar cell ($V_{oc} \approx 690$ mV, $J_{sc} \approx 40$ mA/cm^2, FF ≈ 75%) using patterned doped *poly*-Si layers based on the photo-CVD technique.

III. Project Results and Discussion

III.A Photopatterning of Doped *a*-Si:H

Our original goal was to achieve photo-assisted deposition of *a*-Si:H through a shadow mask. Through a very comprehensive survey of the literature, we have concluded that photo-desorption of surface H from a *c*-Si surface requires 8 eV photons (see Figure 5). In addition, the cross section of the photo-desorption process is extremely low, ~2.8×10^{-21} cm^2/photon. This means that ~10^6, 8 eV photons are required to desorb one H atom from a surface -SiH bond. Only an F_2 excimer laser can provide such a high light intensity at 8 eV (157 nm). Due to the lack of availability of such commercially-available light sources, photo-deposition of *a*-Si:H from SiH_4 is not feasible for commercial-scale processing of solar cells. Therefore, we changed the focus to photo-assisted etching of *a*-Si:H using UV light in the 200-300 nm range in a Cl_2 atmosphere. The photo-assisted etching process can be very rapid with a source power density of ~50 mW/cm^2 in the 200-300 nm range, which can be readily achieved through a variety of light sources. A high-power Xe flash lamp was custom-designed with Resonance Ltd. to introduce 240 nm light into the chamber at ~30-40 mW/cm^2, and installed onto the surface analysis chamber equipped with *in situ* attenuated total reflection Fourier transform infrared spectroscopy setup to directly monitor the etching of the *a*-Si:H film (see Figure 6).

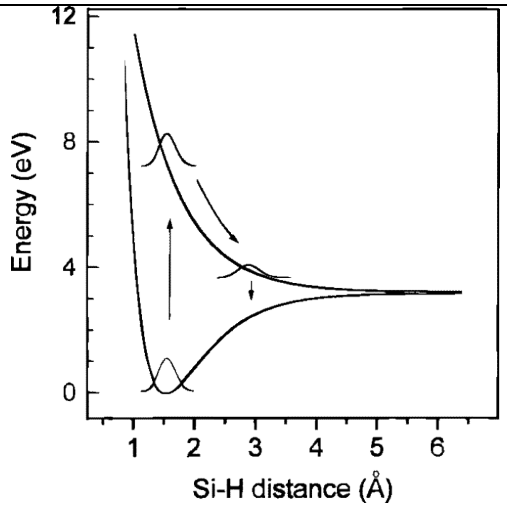

Figure 5: *Ab initio* potential energy surfaces for the σ → σ* transition for the Si-H bond on H-terminated Si(100), and snapshots of the wave function at the moments of resonant excitation and electronic quenching. Figure reproduced from Vondrak and Zhu, *J. Phys. Chem. B* **103**, 4892 (1999).

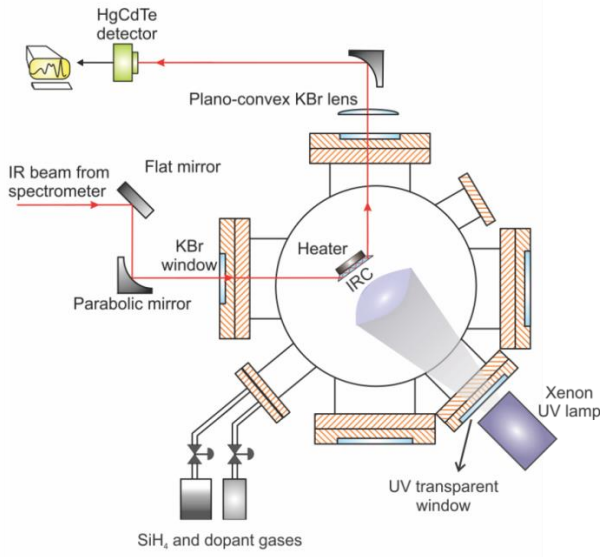

Figure 6: Schematic representation of the plasma-assisted CVD chamber equipped with the Xe lamp providing the UV light necessary for photo-assisted CVD (highlighted in purple). The surface species present on the IRC are probed by in situ attenuated total reflection Fourier transform infrared spectroscopy.

Prior to studying the effect of UV light on etching of *a*-Si:H, we started out with first optimizing patterning of *a*-Si:H from a SF_6/Ar plasma with a contact mask made from laser ablation and subsequent wet-etching of ~180-μm-thick *c*-Si wafers. An example of such a mask is shown in Figure 7a and the corresponding pattern transfer is shown in Figure 7b. The pattern transfer was measured based on the difference in reflectivity

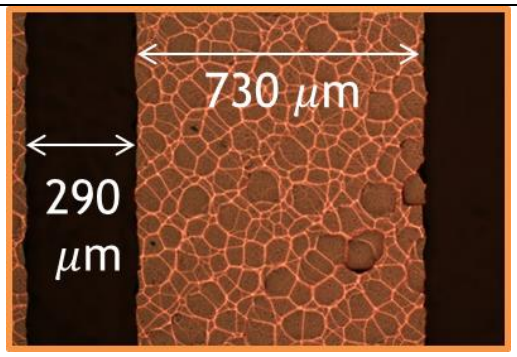

Figure 7a: Optical image of the Si hard mask used for pattern transfer onto the underlying *a*-Si:H film. The open line width is ~290 μm with ~730 μm covered area. The Si wafer thickness is ~180 μm.

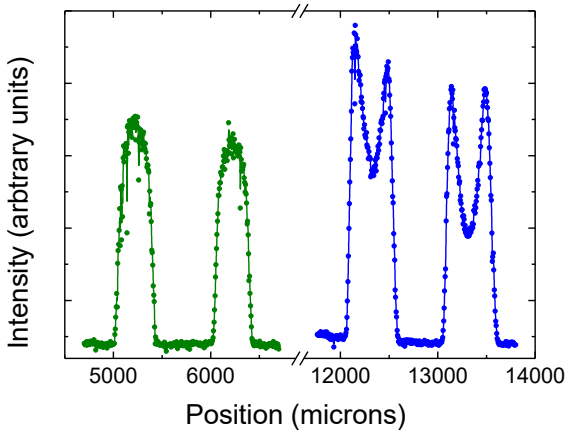

Figure 7b: Reflectivity measurements along two line patterns corresponding to the mask shown in Figure 5a. The profile on the left (—) corresponds to a 180 μm spacer between the mask and the substrate, and the line profile on the right (—) corresponds to a contact mask.

between *a*-Si:H and glass. As can be seen in Figure 7b, sharp line widths can be obtained through direct plasma etching of *a*-Si:H using a hard shadow mask placed in close proximity (~180 μm) or in direct contact with the substrate. Subsequently, we turned our attention to photo-assisted etching in a Cl_2 atmosphere with a high-power Xe flash lamp to improve this result obtained from SF_6/Ar plasma etching and demonstrate that a higher etch fidelity could be obtained using UV photo-assisted etching of *a*-Si:H in a Cl_2 plasma. However, we did not observe any significant and reproducible differences in the etching of a-Si:H with either Cl_2/Ar or SF_6/Ar plasma. At this point, we decided to experiment with a direct deposition approach of doped *a*-Si:H with the type of shadow masks shown in Figure 7a.

III.B Development of Masked PECVD Patterning

Precision is integral to the patterning of the doped fingers at the rear of IBC cells. However, many current techniques are so complicated that they become prohibitively expensive. Because of this, we developed a patterning method which is both simple and effective, requiring cheap ceramic pins and silicon shadow masks. The fabrication and alignment processes of the dopant patterning masks are described below.

III.B.i Pin Alignment of Shadow Masks

We developed a method that allows us to precisely align hard shadow masks made from laser ablation of *c*-Si wafers followed by etching in a KOH solution. For sample alignment, we place round, precisely-machined (2 mm ± 010 μm) ceramic pins into complementary holes in the mask and substrate (see Figure 8) to hold the mask and substrate together during the depositions of doped *a*-Si:H and similar masks for deposition of metal contacts. This process was shown through photoluminescence

measurements not to cause damage to the substrate from repeated scraping with the mask.

Using the laser ablation and KOH etching method, we define alignment holes (see Figure 9 inset) 2 mm wide in the mask along with the pattern to be transferred to the substrate. Due to the tight fit required to prevent relative motion between the mask and substrate, circular holes were initially tested to fit snugly with the alignment pins. However, because the KOH solution etches Si anisotropically, favoring the [100] planes, perfectly circular holes could not be obtained, and it was decided that square holes with edges aligned with the [100] crystallographic planes would work best to obtain sharp edges. With this alignment technique, sharp edges in the square holes can be obtained and alignment precision of ~10 µm can be obtained (see Figure 9).

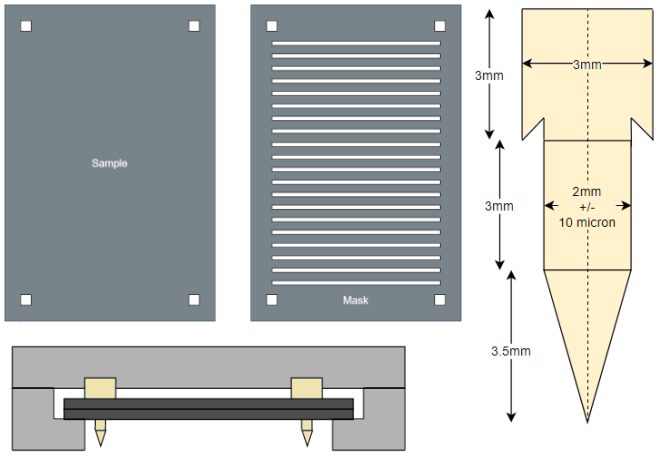

Figure 8: Schematic showing the substrate (top left), the c-Si hard mask (top middle), and the ceramic alignment pin (right). The alignment pin is inserted into the 4 square alignment holes in the substrate and the mask, and mounted onto the deposition stage in the PECVD chamber (bottom).

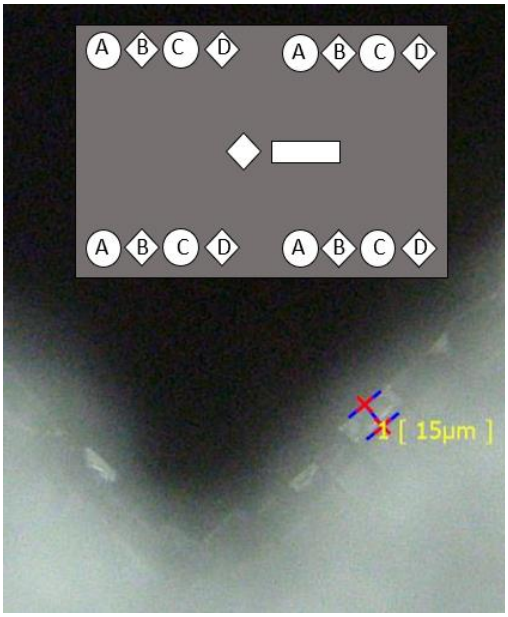

Figure 9: Tested shapes of alignment holes and the 15 µm fit achieved with the square hole shape (micrograph).

III.B.ii Sample Preparation

Samples fabricated for this project varied significantly in purpose and in structure, but underwent many of the same processing steps and consisted of roughly the same materials throughout. *n*-type Czochralski (*n*-Cz) Si(100) wafers with ~3 Ω·cm resistivity, ~180 µm in thickness, were cut into pieces and etched in 22.5% aqueous KOH to planarize the surface and remove the saw damage. The *c*-Si wafers then underwent standard cleaning steps of piranha, RCA 1, and RCA 2 followed by etching in 1% HF to remove the oxide formed by the RCA 2 step. A dry, thermal SiO_x film either ~1.5 nm thick for cells or ~70 nm thick for insulation between the *poly*-Si film and the *c*-Si substrate was then grown in a quartz tube furnace at 1100 °C at atmospheric pressure in an O_2 ambient at a flow rate of 3000 standard cm^3/min (sccm). Subsequently, on one side of the wafer, a ~50 nm film of intrinsic *a*-Si:H was deposited on the SiO_x via a SiH_4/H_2 capacitively-coupled, radio-

frequency (rf) plasma operated at 13.56 MHz at a pressure of 1 Torr. The oxidized *c*-Si wafers were placed on the grounded electrode kept at 300 °C. The input power to the plasma was 8 W, with the gas flow rates set to 2 and 100 sccm for SiH_4 and H_2, respectively. Following deposition, the *a*-Si:H films were annealed in a quartz tube furnace in an N_2 ambient. The furnace temperature was ramped from 200 to 850 °C over 3 hr, followed by a 30 min annealing step at 850 °C to convert the *a*-Si:H to *poly*-Si via solid phase crystallization. The films then underwent a passivation step, which entails a ~15 nm film of Al_2O_3 grown by atomic layer deposition at a temperature of 150 °C from trimethyl aluminum and water, followed by annealing for 20 min at 400 °C in forming gas (1:9 H_2:N_2), and subsequent removal of Al_2O_3 film by an HF dip as described in [26].

Samples with patterned, doped *poly*-Si were created identically to the above full-area intrinsic *poly*-Si structures, with the addition of doped *a*-Si:H fingers on top of the intrinsic *a*-Si:H by masked PECVD, then crystallizing the structures at 850 °C as described above. Phosphorus- or boron doped *a*-Si:H fingers, with different gap spacings between them, were plasma-deposited through the Si contact masks at the same conditions as the intrinsic *a*-Si:H above, but with the addition of 1 sccm of B_2H_6 (2.6% in H_2) or 1 sccm of PH_3 (3% in H_2). Electrical contacts to the *poly*-Si films were formed by thermal evaporation of 1 µm thick Al in a tool with a base pressure of ~10^{-7} Torr via a Si mask matching the plasma-deposited 2D doping patterns.

III.C Dopant Spreading Mechanisms During Cell Fabrication

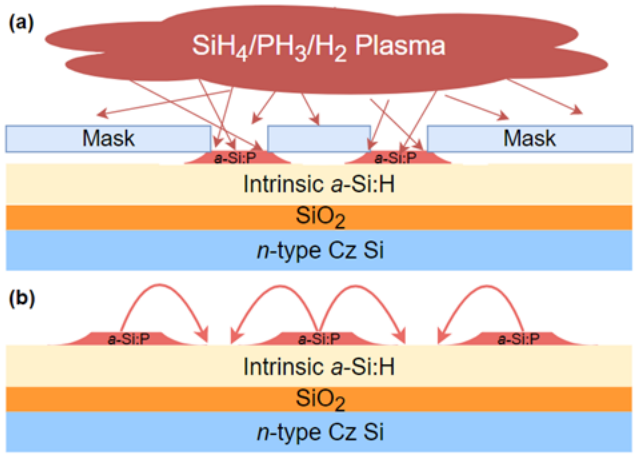

Figure 10: Schematic showing the possible contamination mechanisms of the intrinsic *poly*-Si isolation region during cell processing. (a) Dopant radicals within the plasma can spread underneath the mask to deposit into the intrinsic isolation region. (b) Dopants can desorb from the surface of the doped *a*-Si:H films during high-temperature annealing, re-adsorb onto the intrinsic *a*-Si:H film, and diffuse inward.

Though the contact masks aligned with ceramic pins described above to provide precise alignment of dopant patterns to the substrate, we discovered multiple mechanisms throughout processing leading to spreading of dopant atoms into the region separating the doped finger patterns (see Figure 10). During plasma deposition of doped *a*-Si:H, radicals within the plasma spread underneath the mask leading to deposition onto the masked region. Additionally, during high-temperature annealing, dopants desorbed from the surface and redeposited onto intrinsic regions of the *poly*-Si film. We developed methods to mitigate such contamination and describe these in the following sections.

III.C.i Dopant Spreading During Masked Plasma-Enhanced Chemical Vapor Deposition

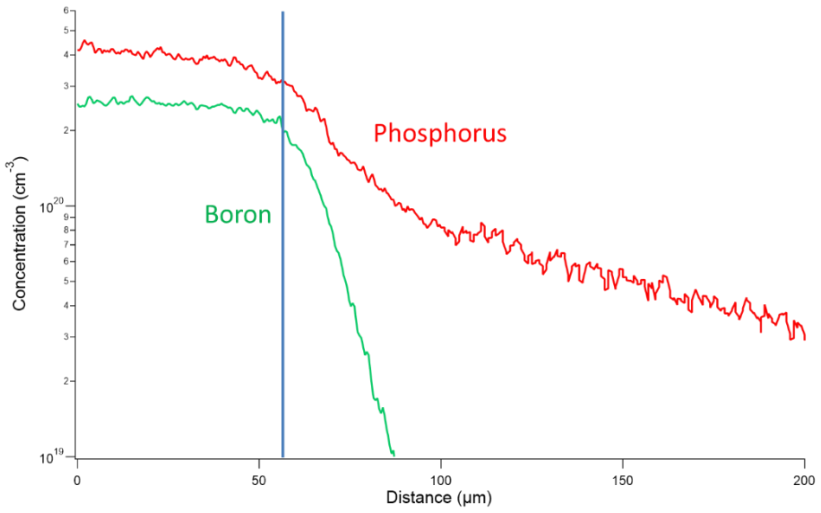

Figure 11: Lateral TOF-SIMS profiles of the edges of phosphorus (red) and boron (green) doped *a*-Si:H fingers. The much sharper drop in concentration for the boron doped sample indicates much less spreading during masked PECVD.

Because dopant radicals within the plasma phase have random trajectory and a gap on the order of ~10 μm exists between the mask and substrate, there is a possibility that radicals could enter between the two and spread into the intrinsic gap region before sticking to the intrinsic *a*-Si:H surface. Additionally, dopants may migrate along the surface after sticking through surface diffusion, as shown through literature [7, 8]. The latter mechanism should not however lead to long range migration as observed in our experiments. To test this effect, we first patterned doped *n*-type fingers onto an intrinsic *a*-Si:H substrate and capped it with an additional layer of intrinsic *a*-Si:H to eliminate measurement artifacts as the surface may get modified after exposure to atmosphere. Time-of-flight secondary ion mass spectrometry (TOF-SIMS) was used to map out the dopant concentration in 3D space within the sample. These profiles were averaged along the depth into the film, and Figure 11 shows the averaged 1-D lateral dopant profiles for boron (green) and phosphorus (red). The phosphorus profile extends over 100 μm under the mask edge denoted by the vertical blue line, causing contamination of the intrinsic *a*-Si:H region. While the boron profile does extend past the mask edge, the spreading is not nearly as drastic as with phosphorus, so spreading of boron is deemed less harmful to the intrinsic *poly*-Si region.

III.C.ii Desorption and Re-adsorption of Dopants During High Temperature Annealing

High-temperature annealing steps are required in *poly*-Si/SiO_x passivating contact processing, which can lead to segregation of dopants to the surface, followed by desorption into the gas-phase, and re-adsorption on surrounding surfaces. To understand gas-phase dopant migration, the experiment entailed crystallizing blanket layers of intrinsic *a*-Si:H alongside blanket phosphorus-doped layers of *a*-Si:H in the annealing furnace as shown in Figure 12. All *a*-Si:H films were grown on *c*-Si with an insulating oxide layer so that following the crystallization anneal at 850 °C, evaporated aluminum TLM patterns could be deposited onto the intrinsic samples to measure resistivity without influence of the lightly-doped *c*-Si base. Resistivities much lower than ~10^5 Ω·cm previously measured for intrinsic films would indicate that gas phase dopant migration is occurring. On the other hand, resistivities on the same order of magnitude would indicate that gas phase transfer is not significant. In Figure 12, sample A, which is upstream and farther away from the doped *n*-type sample, has the

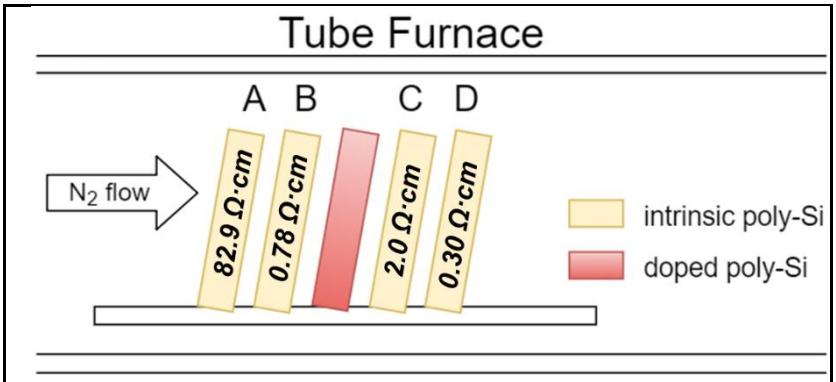

Figure 12: Schematic of samples as they would sit in the tube furnace during the crystallization anneal. Samples are shown with the intrinsic film facing the doped sample and gas flow direction is indicated.

highest resistivity, while resistivities for samples B and C are roughly the same. The resistivity for sample D is a bit lower than B and C. The resistivity values in Figure 12 are at least three to five orders of magnitude lower than for an intrinsic *poly*-Si film, indicating that gas phase dopant migration does indeed occur and significantly spreads phosphorus over distances of several millimeters, which much wider than typical IBC gap spacings. So, this phenomenon must be considered as a significant contributor to contamination. A similar experiment was conducted with a boron-doped film instead of phosphorus, but the resistivities of the intrinsic wafers remained on the order of purely intrinsic films, showing that gas phase transfer of boron is not a concern. This is consistent with the literature which shows that surface boron on *c*-Si is stable up to nearly 1000 °C [9].

III.C.iii Mitigation of Dopant Spreading

To address the issues of contamination of the *poly*-Si isolation region discussed above, we first attempted to mitigate the effect of gas phase dopant transfer. This was accomplished by using capping layers of either *a*-Si:H or SiO_2 during the crystallization annealing step. Intrinsic *a*-Si:H was used not only to prevent dopants from directly effusing from the surface, but also to reduce the concentration of dopants at the surface as they diffuse throughout the underlying film. The SiO_2 capping layer would have to be removed during HF etching in later processing steps.

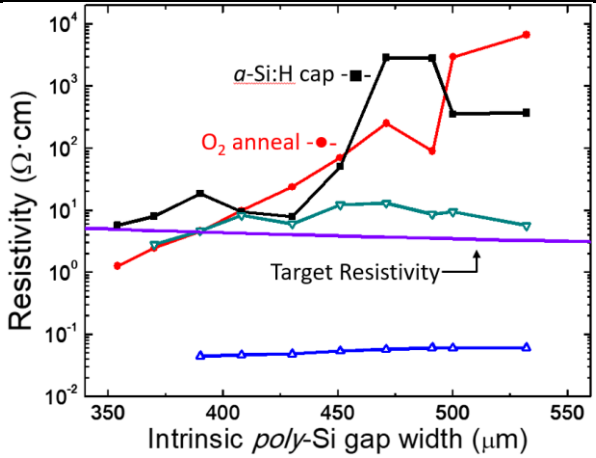

Figure 13: Resistivity measurements of the intrinsic *poly*-Si gap between *n*-type fingers. The purple curve represents the resistivity as a function of gap width required for a total shunt resistance 100 times greater than the characteristic cell resistance. The data in blue and teal represent respectively, the high and low extremes of resistivity values for samples with no mitigation with a capping later. The data in black and red show resistivities of samples which were annealed with a capping layer of either intrinsic *a*-Si:H and *in situ* grown thermal SiO_x, respectively.

The results of these two experiments are shown in Figure 13. For high gap widths, both capping layers maintain a high resistivity within the intrinsic isolation region, well above the highest resistivity values obtained for samples with no capping layer. The devices we fabricated have a ~150 μm wide intrinsic *poly*-Si region between the phosphorus- and boron-doped

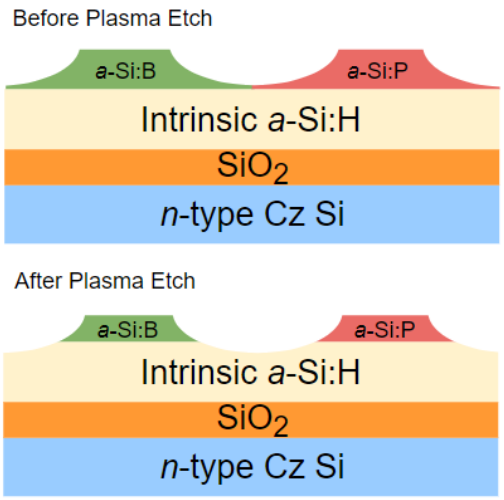

Figure 14: Schematic cross section of doped fingers before and after using an SF_6 plasma to remove the top few nanometers of *a*-Si:H from the surface of the film, clearing dopant tails out of the intrinsic gap region.

fingers. While significant dopant spreading would still occur at these smaller dimensions, we show later in this report that there is an inherent dopant compensation mechanism, which can lead to a significantly high resistivity. In contrast the measurements in Figure 13 are for two adjacent phosphorous-doped fingers with no compensation.

Once a sufficiently effective strategy was developed to mitigate gas phase transfer of phosphorus, we turned to develop a strategy to reduce the effect of dopant spreading during masked PECVD. One method to mitigate the effect of this spreading is to perform a dry plasma etch of the surface to uniformly remove the top few nanometers of both the intrinsic and the doped *a*-Si:H. Because the thickness of the doped *a*-Si:H extending underneath the mask decreases significantly as the distance from the mask edge increases, the dopant tail can be removed completely, while leaving the intentionally doped region almost entirely intact (see Figure 14). This was accomplished through a reactive ion etching (RIE) step after deposition of the doped fingers using an SF_6 plasma at a pressure of ~0.1 Torr and 5 W of plasma power for 2 s. After etching the surface, the samples were annealed to convert the *a*-Si:H to *poly*-Si in three different ways. Some samples were protected with an additional intrinsic *a*-Si:H capping layer, and those without a capping layer were annealed in either N_2 or O_2 ambient. After crystallization, aluminum pads were evaporated onto the doped fingers, and the resistivity of the intrinsic *poly*-Si isolation region was measured across different widths. The results are shown in Figure 15 and indicate that all samples that were pre-etched with no *a*-Si:H capping layer had a highly resistive intrinsic *poly*-Si isolation region, with resistivity on same order as the intrinsic poly-Si films prior to dopant patterning. However, in Figure 15, the samples onto which the intrinsic *a*-Si:H cap was deposited before crystallization show resistivities which drop drastically as the gap

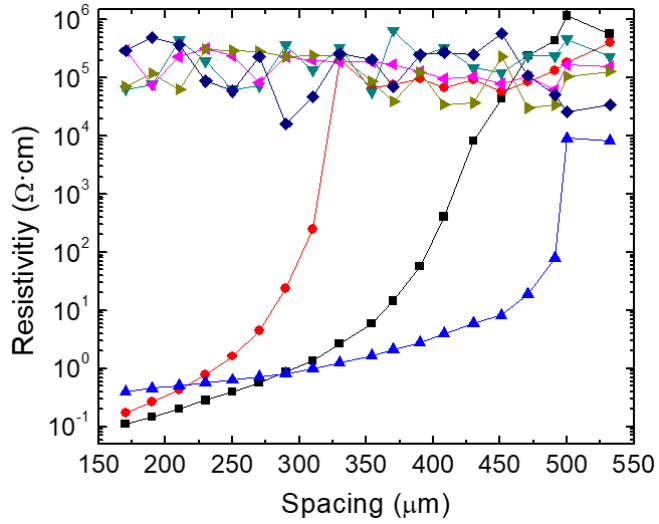

Figure 15: Resistivity of the intrinsic *poly*-Si isolation region for samples that were plasma etched following the PECVD of phosphorus doped *a*-Si:H fingers. A drastic drop in resistivity occurs at decreasing spacings for samples on which an intrinsic *a*-Si:H cap was deposited before crystallization (red, blue, and black) while the others had no cap and were crystallized in either N_2 or O_2 ambient.

width decreases. One possible explanation for this is that in a SiH_4/H_2 plasma deposition process H radicals in the plasma etch the top layer of the patterned *a*-Si:H substrate forming volatile hydrides of Si, P, and B, which desorb, dissociate in the plasma, and redeposit on the *a*-Si:H surface including the intrinsic regions [10, 11]. Since the doping levels for B and P in *a*-Si:H are different, and the sticking coefficients of the radicals formed from the dissociation of their hydrides are different, dopant compensation does not occur after redeposition in the intrinsic *a*-Si:H region. The investigation into these dopant contamination mechanisms and the mitigation strategies developed comprised the first manuscript to come out of this project.

III.C.iv Simulation and Confirmation of Gap Compensation Preventing Shunt

Additionally, simulations were performed to better understand the effect of dopant compensation in the *poly*-Si isolation region. We have developed simulations of radical transport between the *c*-Si hard mask and substrate during masked PECVD. Once we understood how the intrinsic isolation region becomes contaminated during cell processing and fabricated our first batches of IBC cells, we noticed that despite contamination of the entire isolation region with dopants as shown by SIMS measurements, excessive shunting of the devices was rarely seen in current-voltage and Suns-V_{oc} measurements. This led us to investigate the possible reasons why high levels of dopants throughout the *poly*-Si isolation region would not lead to low shunt resistance, as expected. Though we recognized that compensation would occur at the point where the concentrations of opposing dopant types were exactly equal, this should be such a precise location within the film that it would have hardly any isolation effect at all, especially given the inhomogeneities which could exist within the film doping. What is observed, however, is a high shunt resistance for complete devices, not just for our devices, but also the record 26.1% POLO device from ISFH, which also exhibited high degrees of dopant contamination across a much narrower 30 µm isolation region [*4*].

Because of this, we investigated the possible causes for prevention of shunting between the doped fingers when significant dopant contamination is seen in the isolation region. Considering that *poly*-Si is a highly defective material because of the disordered regions between individual crystalline grains, we considered the possibility of these defects capturing charge carriers, preventing conduction through the material. The capture of charge carriers at grain boundary defects is known in the literature [12-15] and it has been shown that such capture results not only in a reduction of free carrier concentration, but also a significant decrease in mobility due to the formation of a potential barrier at the grain boundaries [16].

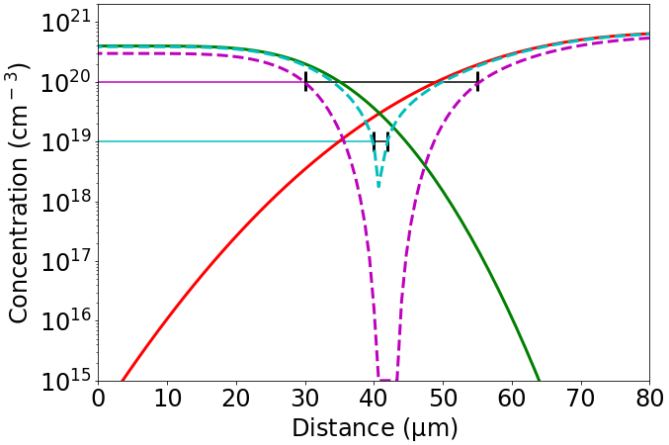

Figure 16: Simulated lateral profiles of boron (green) and phosphorus (red) extending into an intrinsic isolation region and overlapping in the middle. The dashed lines represent the net free carrier concentration for assumed trap densities of 10^{19} cm^{-3} (blue) and 10^{20} cm^{-3} (purple). Black lines represent the width of the compensated region for each level of trap defect density.

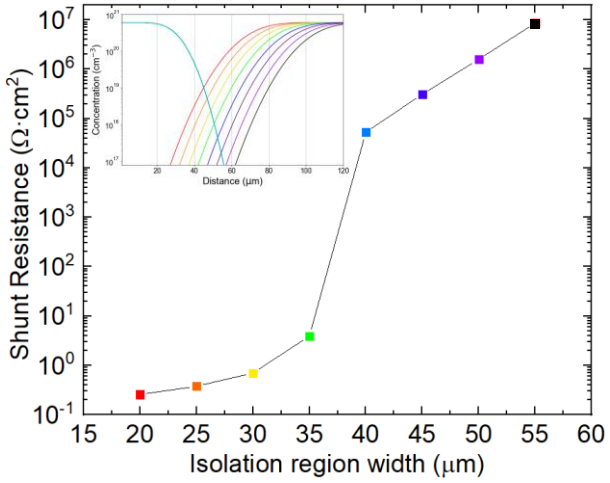

Figure 17: Shunt resistance for different isolation region widths, δ, between *n*- and *p*-type fingers. The colors of each point correspond to the color for the phosphorus concentration profiles on the right hand side in the inset. The boron concentration profile is shown in cyan on the left side of the inset.

Figure 16 demonstrates a simple example of how trap defects significantly reduce the net free carrier concentration, n_{eff}, of two dopants. Error function profiles of boron (green) and phosphorus (red) overlap one another, and the n_{eff} concentrations (dashed lines) are shown for trap defect concentrations of 10^{19} cm^{-3} and 10^{20} cm^{-3}. The net free carrier concentration drops drastically when the net doping concentration reaches the trap defect concentration, creating a region of fewer free carriers than traps which results in a significantly higher resistivity. In Figure 16, comparing the blue curve to the purple curve also shows that increasing the trap defect concentration by an order of magnitude not only drastically decreases n_{eff} at the point of overlap, but also increases the width of the compensated region from ~3 to ~25 µm. This increase in compensated region width allows for much greater total resistance across the isolation region.

Carrier transport in the contaminated isolation region between the *p*- and *n*-type fingers is a three-dimensional problem, but for simplicity we conducted one-dimensional calculations assuming uniform dopant concentration throughout the thickness of the *poly*-Si film. For a high shunt resistance, the *p-i-n* structure can most simply be modelled as a resistor, considering drift currents from applied bias, but not diffusion current, space charge effects, or emission of carriers from trap states. Dopant profiles input into the simulation were based on lateral TOF-SIMS data or assumed to be an error function spreading from the edge of the mask defining the intentionally doped fingers. From previous experiments, we find that ~10% of boron atoms and ~30% of phosphorus atoms are active for total dopant concentrations in *poly*-Si of 10^{20} – 10^{21} cm^{-3} [17]. To account for trap states in *poly*-Si [14] we subtract the trap density, N_t, from the net active dopant concentration to determine the effective carrier concentration, n_{eff} (see Figure 1b). The local resistivity in the *p-i-n* structure was obtained either from the literature [12, 13, 18] or estimated based on the carrier concentration and mobility in *poly*-Si.

Following the resistivity calculation of each resistor in series from the local n_{eff}, the total shunt resistance, R_{shunt}, was determined by using the expression,

$$R_{shunt} = \frac{W_p}{2t}\int_0^{\delta} \rho(x)dx, \quad (1)$$

where r (x) is the local resistivity, W_p is the pitch, and t is the film thickness. In all resistor simulations, W_p and t were fixed at 1 mm and 100 nm, respectively. We calculated the total shunt resistance for different values of isolation region width, d, over the range of 20 – 55 µm [5, 6, 19] and for different dopant diffusion lengths in the *poly*-Si isolation region, $L_{diff} = \sqrt{D_{eff}t}$, where D_{eff} is the effective diffusivity of the dopant in *poly*-Si and t is the time over which the diffusion occurs. For diffusion at

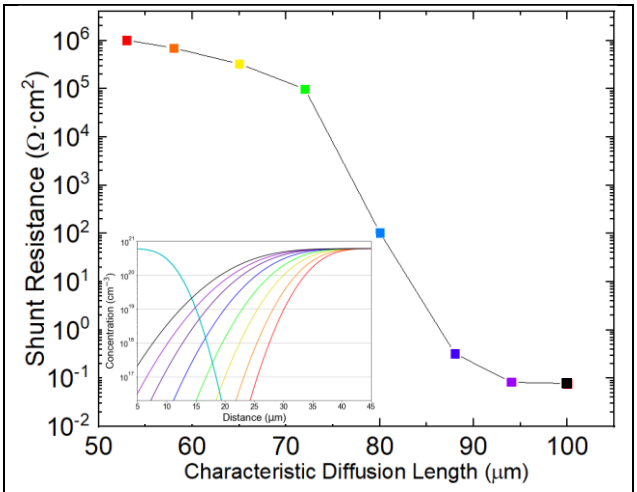

Figure 18: Shunt resistance across the gap region for different n-type finger L_{diff} for constant *p*-type L_{diff} and constant isolation region width. The inset graph shows a representative overlap between the two dopant profiles, with increasing *n*-type L_{diff} from the red to the black curve.

temperatures >1000 °C, this corresponds to D_{eff} ~10^{-10} – 10^{-9} cm^2/s and t ~10^3 s to achieve L_{diff} ~10 µm. To apply the resistor model more generally for aiding in design of IBC cells, we consider how the width of the region between doped fingers will affect R_{shunt} across the isolation region. We varied d over the range of 20 – 55 µm as ~10 – 100 µm is on the order of commonly used distances between the *p*- and *n*-type fingers of IBCs. L_{diff} of the *n*-type tail was varied over the range of 50 – 100 µm, corresponding to diffusivities of phosphorus, D_P ~10^{-10} cm^{-2}/s [4, 20, 21] and diffusion times, t_{diff} ~ 1 hr. For high temperature, >1000 °C, annealing of *poly*-Si/SiO_x passivated contacts, these values for L_{diff} are reasonable. However, specific values can differ significantly depending on the annealing temperature, *poly*-Si grain size, and doping level in *poly*-Si [22-26]. In these simulations, we assume a trap density, N_t = 10^{18} cm^{-3}, in *poly*-Si.

Figure 17 shows the calculated R_{shunt} as a function of *poly*-Si isolation region width for error-function-shaped dopant concentration profiles for the *p*- and *n*-type doped fingers. These profiles are similar to those that are observed for IBC devices fabricated with ion implantation followed by high-temperature annealing [4, 27]. A large increase in the shunt resistivity from <1 to >10^5 Ω·cm occurs for the isolation region widths between 35 – 40 µm. As can be seen in the inset of Figure 17, the concentration at the point at which the dopant profiles intersect is less than N_t for isolation region widths, d < 40 µm. Though the net dopant concentration should be negligible right at the single point where the active *p*- and *n*-type dopants are equal in concentration, the width of the region over which the net dopant concentration is below N_t is much higher when d < 40 µm. This wider region allows for a greater chance that the compensated region will truly isolate the doped regions from one another.

Figure 18 shows the shunt resistance for different values of L_{diff}, for a constant isolation width, d. This curve follows a very similar pattern to that seen in Figure S2. Literature values for diffusivity of phosphorus and boron in *poly*-Si vary by several orders of magnitude depending on the method of formation of *poly*-Si, dopant concentration, deposition temperature, grain size, and other factors. The diffusivities range from 10^{-15} – 10^{-12} cm^2/s and 10^{-19} – 10^{-9} cm^2/s for boron and phosphorus, respectively [20, 22, 23, 25, 28-30]. These values depend strongly on the *poly*-Si annealing temperature. Therefore, if a smaller isolation region width, d, between doped fingers is desired, it may be necessary to reduce process temperature or diffusion time significantly

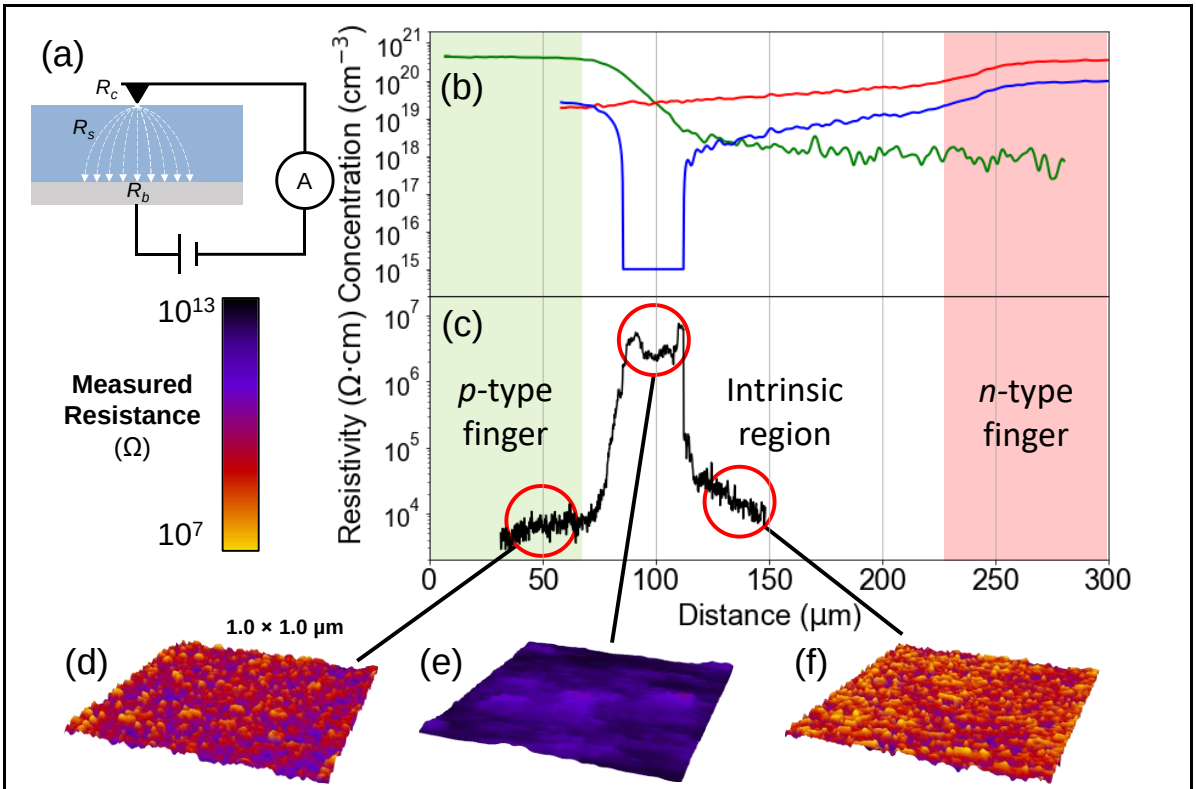

Figure 19: (a) Schematic of SSRM setup. (b) TOF-SIMS measurements of overlapping *p*- (green) and *n*-type (red) PECVD *a*-Si:H tails with calculated n_{eff} (blue). All curves have been smoothed to reduce noise. (c) Resistivity as a function of distance between the *p*- and *n*-type fingers measured by SSRM. (d-f) SSRM heat maps showing measurements of resistance in three 1 μm^2 portions of the ~175 μm wide intrinsic *poly*-Si isolation region: a region dominated by boron (d), a compensated region where dopant concentration is nearly equal (e), and a region dominated by phosphorus (f).

In addition to simulations with error function profiles, we simulated how this trap-assisted dopant compensation effect would create an insulating region for our experimentally measured dopant profiles, and we compared these simulations to the experimentally measured resistivity in the *poly*-Si isolation region using scanning spreading resistance microscopy (SSRM) (see Figure 19a). Figure 19b shows two superimposed profiles of boron (green) and phosphorus (red) measured using TOF-SIMS assuming an isolation region width equal to our initial IBC solar cells (~175 μm). The blue curve shows the simulated resistivity corresponding to the experimentally measured dopant profiles. Figure 19b shows local resistivity across the isolation region of one IBC cell with these dimensions, as measured by scanning spreading resistance microscopy (SSRM). The regions of low free carrier concentration and high resistivity line up quite well for an assumed trap density of ~7.5 × 10^{18} cm^{-3}. The results of these simulations, combined with the SSRM measurements confirm that a high resistivity region does exist because of compensation between the dopant tails extending from each patterned finger. Also defects in *poly*-Si play an essential role by enhancing the width of the isolation region.

III.C.v Diode Simulations of Overlapping Dopant Tails

A region where oppositely doped regions contact one another naturally forms a space charge region with a diode behavior rather than a resistor. We also considered the *I-V* behavior such structures by solving the drift-diffusion and Poisson equations using finite element method based simulations. In these simulations, we assumed

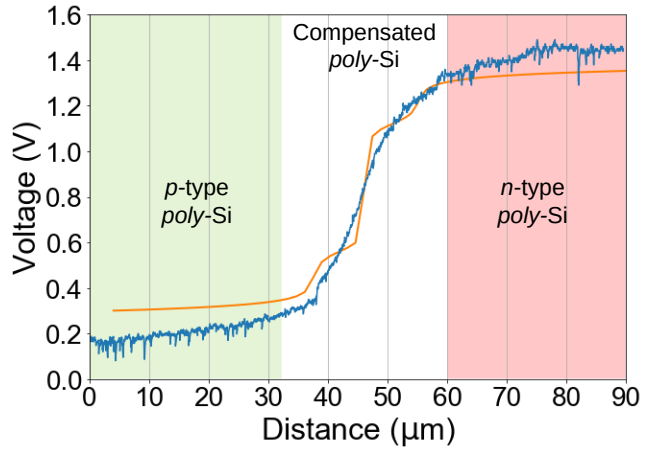

Figure 21: KPFM scan across the *poly*-Si isolation region of an IBC test structure (blue) compared to a simulated potential profile of overlapping error function profiles (orange). The left side shaded in green corresponds to the region of the intrinsic gap contaminated primarily by boron (green) while the right side shaded in red corresponds to the region of the intrinsic gap contaminated primarily by phosphorus (red).

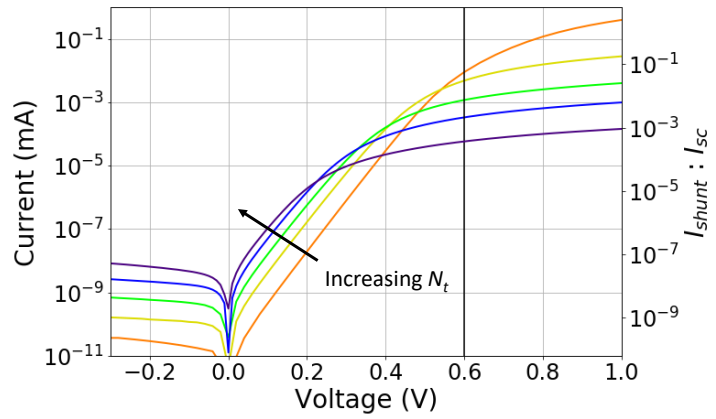

Figure 21: Current-voltage plots of simulated *p-i-n* diodes for various levels of trap defect density, N_t = 2.3×10^{17} (orange), 3×10^{17} (yellow), 4.95×10^{17} (green), 9×10^{17} (blue), and 2.3×10^{18} cm^{-3} (purple).

overlapping error function-shaped profiles of boron and phosphorus with the entire region containing a defect density N_t which was split between six types of shallow hole traps and electron traps. Mid-gap defect states would be more representative of dangling bonds that exist at grain boundaries in *poly*-Si, but this led to convergence problems in the simulations. Therefore, the trap defects were set at approximately 0.275, 0.333, and 0.385 eV from the valence and conduction band edges, respectively. This allows for physically reasonable capture and emission of carriers by the traps, while maintaining symmetry within the bandgap, much like a mid-gap state.

Figure 20 shows the potential profile measured with Kelvin probe force microscopy (KPFM) of a structure much like that described in the previous sections, with overlapping dopant tails of opposing dopant types. The blue line is the local work function across the isolation region of an IBC-like test structure. The orange curve is a simulated potential profile of a similar structure with error function-shaped dopant profiles. The measured KPFM potential profile shows a steep increase in potential over ~20 µm, which is of the same width as the high-resistivity region measured with SSRM and simulated with effective carrier concentration.

To determine the effect of defect density on the diode behavior of the isolation region, we perform the diode simulations for different defect densities. Figure 21 shows the results of these simulations for defect densities between 2.3 × 10^{17} cm^{-3} and 2.3 × 10^{18} cm^{-3}. From these results, we can clearly see that increasing the trap defect density by one order of magnitude results in a decrease of diode current by 2 orders of magnitude for a common cell operating current of 0.6 V, indicating again that a higher defect density is preferrable to prevent excessive shunt current across this isolation region. The simulations described above, combined with the surface probe microscopy measurements led to the second manuscript to come out of this project.

III.C.vi Fitting of PECVD Profiles to Monte Carlo Simulations

During masked PECVD, we hypothesized spreading of dopant atoms occurs through many reflections from the substrate and mask surfaces as shown schematically in Figure 22.

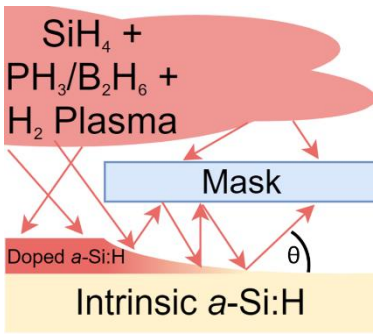

Figure 22: Schematic representation of dopant transport between the mask and substrate during masked PECVD. Radicals can reflect multiple times before sticking to either surface.

To simulate this dopant spreading, we developed a Monte Carlo algorithm for many dopant radicals entering the high aspect ratio mask-substrate gap. Each radical entering the gap will contact the substrate or mask surface, reflecting multiple times at angles determines by Lambert's cosine law. At each step, there is a finite probability of the dopant radicals sticking to either surface. The spread of the dopant atoms is mapped to determine the overall profile. This process results in an exponential decrease in doping concentration moving away from the mask edge [31]. Results of this study can be seen in Figure 23 where a Monte Carlo simulation of boron radicals was fitted to a *p*-type dopant tail by adjusting the input parameters of mask-substrate separation width and sticking coefficient. Matching the simulated dopant profiles with the measured lateral profiles enables us to gain further insight into the masked PECVD process by which our cells are patterned. These simulations can be used to predict the dopant spreading profiles for different mask dimensions.

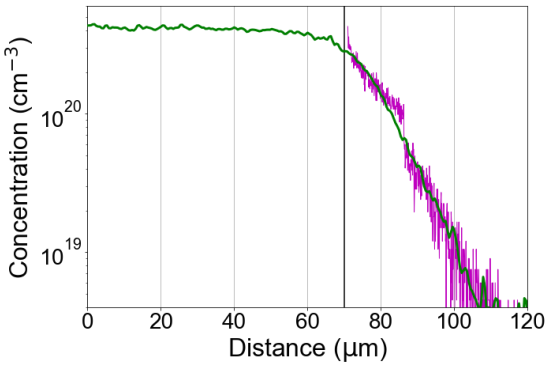

Figure 23: A comparison between a measured SIMS profile of a boron tail past the mask edge (green) and a Monte Carlo simulation result (purple). The mask edge is represented by the vertical line at ~ 70 µm.

III.D Cells Fabricated Over the Course of the Project

Throughout the course of this project, we fabricated 209 cells to demonstrate the efficacy of masked PECVD as a patterning method not only for IBC cells, but also for localized doping of the front contacts for PERC-like devices. We performed initial simulations to guide in the development of optimal IBC design using the Quokka 2 simulation software developed by Andreas Fell at Australian National University [32]. Below we discuss results of IBC as well as PERC-like devices. IBC devices show considerable improvement over the course of the project, increasing in efficiency by 28% relative to early results. PERC-like devices patterned using masked PECVD demonstrate increased efficiency compared to non-patterned devices as well.

III.D.i Optimization of Cell Design with Quokka 2 Simulations

The Quokka simulations allow the user to choose between two sided and one-sided devices, spatial dimensionality of the simulation, and type of simulation to be run. Types of simulations include solving for cell parameters at the maximum power point, light and dark I-V curves, quantum efficiency, Suns-V_{oc}, and series resistance

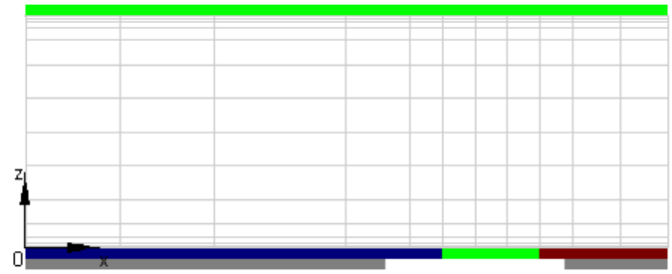

Figure 24: Schematic of the unit cell solved within Quokka including the unit mesh across which equations are solved. Green represents non-conductive boundaries, while blue and red regions represent the emitter and back surface field, respectively. The gray layer represents the metal.

Table 1: Values of parameters input in Quokka simulations

Parameter	Input Value
τ_{bulk}	1 ms
ρ_{bulk}	2 Ω·cm
W_p	600 µm
W_n	200 µm
$J_{0,front}$	3 fA/cm^2
$J_{0,gap}$	5 fA/cm^2
$J_{0,p}$	30 fA/cm^2
$J_{0,n}$	3 fA/cm^2
$R_{sheet,p}$	1000 Ω/sq
$R_{sheet,n}$	60 Ω/sq

calculations. Figure 24 shows an example cross section of the structure simulated for IBC cells in Quokka. Shown in Table 1 are are input parameters values for bulk *n*-type Cz Si wafer, quality of surface passivation, and electrical properties of films related to IBC cells. For the following simulations, only the light I-V curve sweep was performed to obtain V_{oc}, J_{sc}, fill factor, and cell efficiency. An all rear contact cell was used for the following simulations, with a wafer thickness of 180 µm, IBC pitch of 1 mm, and an *n*-type base of 3 Ω·cm resistivity. The assumed values are chosen because they fall within the range of typical values which our group obtains for each parameter. $J_{0,front}$, $J_{0,gap}$, $R_{sheet,n}$, $R_{sheet,p}$, ρ_{gap}, and finger dimensions at the rear of the cell were each tested for their effect on J_{sc}, V_{oc}, fill factor, and efficiency.

Figures 25 and 26 show results for V_{oc} and efficiency of the simulated devices when passivation quality of the *poly*-Si isolation region and the front surface, respectively, were varied. From this, we see that the V_{oc} and efficiency are resistant to changes in $J_{0,gap}$ up to ~100 fA/cm^2. On the other hand, V_{oc} drops considerably when $J_{0,front}$ is increased above ~10 fA/cm^2, and results in an especially drastic drop in efficiency above ~100 fA/cm^2. These results are physically reasonable since the change in V_{oc} with surface passivation should be proportional to the area of each surface, and the isolation region surface is considerably smaller than the front surface. From this, we infer that passivation of the front surface is much more essential to maintain a high efficiency than the passivation of the *poly*-Si isolation region on the back.

The simulations also reveal that while ultra-high quality passivation of the isolating *poly*-Si region is not essential, this region must have a high resistivity to present shunt losses in the cell. Figure 27 shows simulation results for the V_{oc}, *FF*, and efficiency as a function of the resistivity of the *poly*-Si isolation region. If the resistivity between doped fingers is lower than ~100 Ω·cm, a significant drop in efficiency occurs due to decreased V_{oc} and *FF*. The results in Figures 25-27 guided our cell processing approach to maintain high resistivity in the region between the doped fingers.

We also performed simulations to determine the optimal finger dimensions for the rear side of the cell. For a given cell pitch, the finger dimensions can be uniquely defined by setting an isolation poly-Si region's width and the relative ratio of *p*-type and *n*-type finger widths, W_p/W_n. This ratio influences all the major cell parameters, as shown in Figure 28. While V_{oc} decreases for larger W_p/W_n ratios due to the lower passivation quality of *p*-type fingers, compared to *n*-type fingers and the intrinsic isolation region, the J_{sc} increases, which enables an overall increase in cell efficiency as the W_p/W_n ratio approaches ~3.

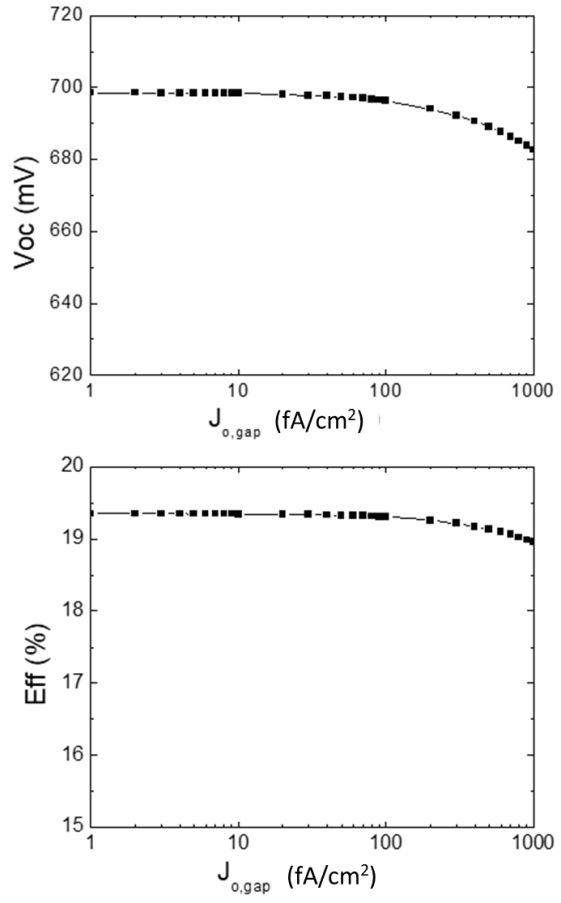

Figure 25: V_{oc} and cell efficiency as a function of recombination current in the *poly*-Si isolation region at the back of an IBC device.

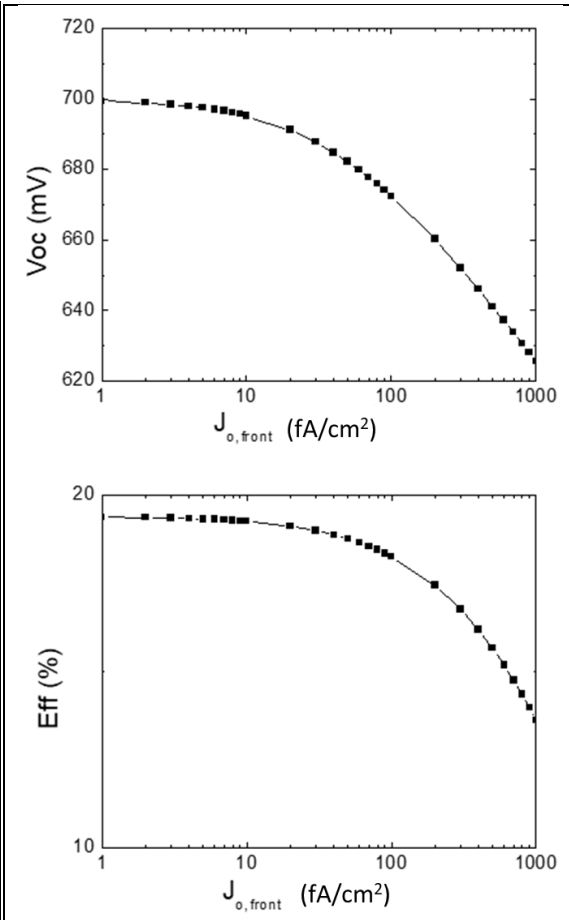

Figure 26: V_{oc} and cell efficiency as a function of recombination current in the front surface.

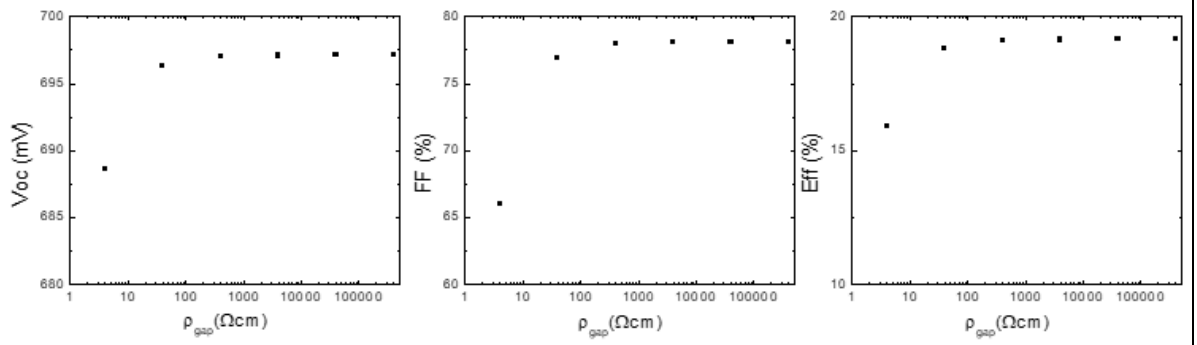

Figure 27: V_{oc}, fill factor, and the cell efficiency as a function of the resistivity of the *poly*-Si isolation region in an IBC device.

This optimal W_p/W_n ratio of ~3 is due to the differences in the because the majority carriers within the *n*-type base are electrons, and it is easier for electrons to reach the narrower fingers than for holes to reach the *p*-type fingers. Thus, a larger *p*-type finger is desired for *n*-type base devices. It is also clear from these results that a narrower gap is better in general, but the difference in efficiency between gaps of 20 µm and 50 µm is minimal.

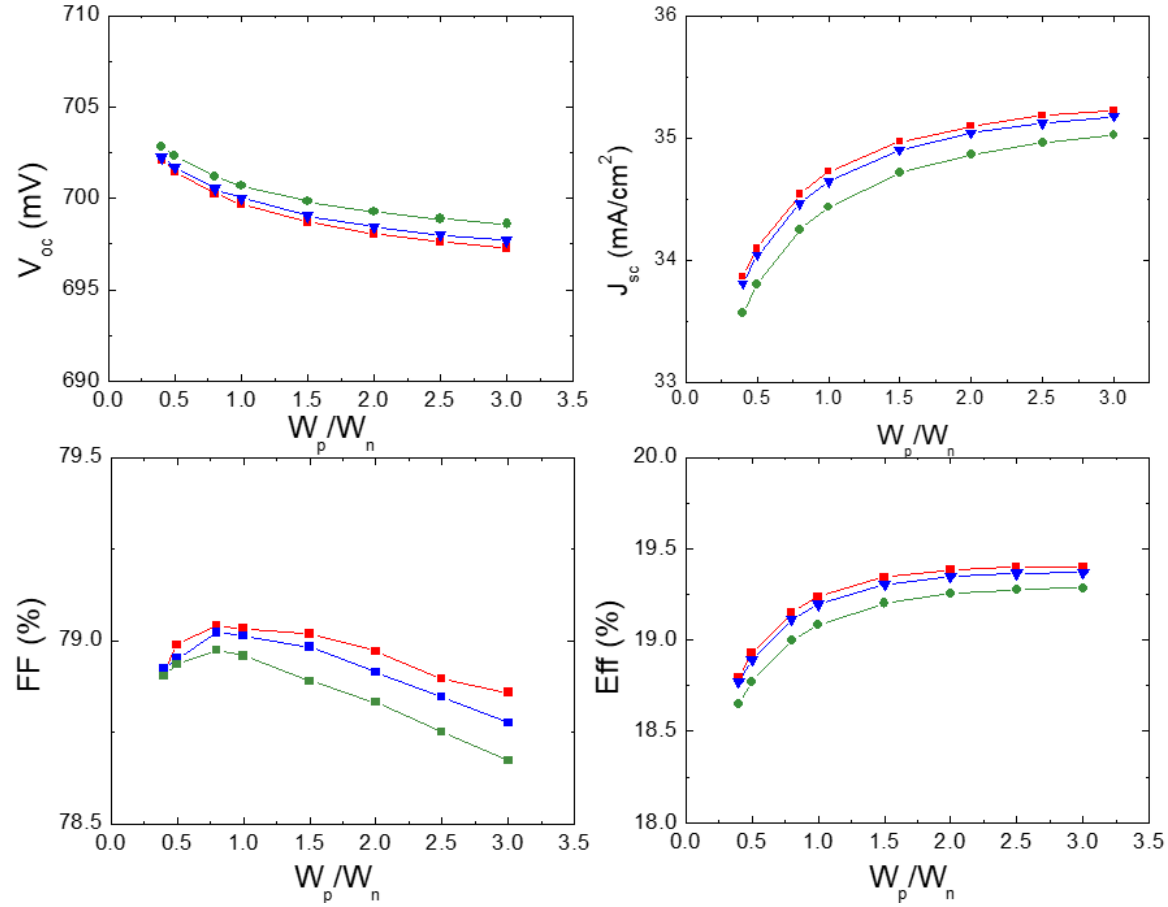

Figure 28: Simulation results showing the effect of *p*- and *n*-type contact area ratio on (a) Voc, (b) Jsc, (c) fill factor, and (d) efficiency for three different gap widths: 20 µm (red), 50 µm (blue) and 100 µm (green).

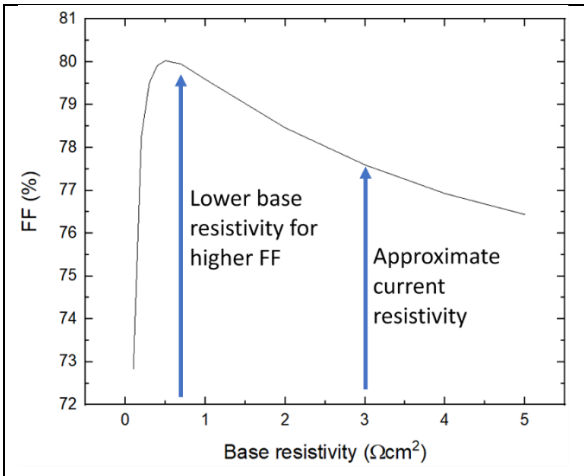

Figure 29: Simulated fill factor as a function of base wafer resistivity. A maximum in *FF* is achieved when resistivity is approximately 0.5 Ω·cm, enabling a roughly 2% higher *FF* by switching to low resistivity wafers.

Finally, we performed a study to determine the effect of the resistivity of the base wafer on the *FF* of the final device. Figure 29 shows that there is a clear maximum in *FF* for wafer resistivity ~0.5 Ω·cm. Compared to our typical wafer resistivity of ~3 Ω·cm, *FF* could be improved by 2% absolute by decreasing the resistivity to reduce series resistance effects. Though this was not tested throughout our cell fabrication studies, it does provide an additional way to move forward for increased cell efficiency.

Overall, these simulations have provided goals to maximize the efficiency of an IBC cell architecture. Though these simulations were based on an IBC cell structure which assumes a diffused emitter and not *poly*-Si/SiO_x passivating contacts, the trends shown here

should be applicable to our specific device structure. By using these simulations as guidelines, we were be able to improve our cell designs and understand what our limits are with many parameters which are under our control.

III.D.ii Interdigitated Back Contact Solar Cells

III.D.ii.1 Pathway to 15%

Table 2: Summary of IBC cell parameters.

Year	J_{sc} (mA/cm^2)	V_{oc} (mV)	FF (%)	Eff (%)
Top 3 **2018** Cells	**29.3**	**695.6**	**73.8**	**15.1**
	28.3	701.5	71.3	14.1
	28.2	682.4	73.6	14.1
	28.6	690	70.4	13.9
	27.2	704.5	72.1	13.8
Top 5 **2021** Cells	**37.8**	**648.5**	**75.7**	**18.6**
	37.1	644.9	73.6	17.6
	38.0	652.7	68.7	17.1
	34	662.1	75.9	17.1
	35.0	642.5	74.3	16.7

Our initial devices had intrinsic *poly*-Si isolation region widths ranging from ~175 to 500 µm. These wider spacings were chosen to demonstrate a proof of concept for the dopant patterning technique. Additionally, for ease of processing, the devices had a planar front side. The results for the three most efficient devices fabricated in 2018 are shown in Table 2. Due to the planar front surface of the devices the short-circuit current density, J_{sc} was low, but front surface passivation is better, resulting in an open circuit voltage, V_{oc}, of ~700 mV. The *FF* is limited by series resistance in devices perhaps as a result of the large isolation region or inconsistencies in the tunneling SiO_x between the *poly*-Si and the *c*-Si. From these batches of planar devices, we were able to reach a high efficiency of 15.1%, completing the BP 3 milestone.

III.D.ii.2 Pathways to 17%

To improve on these devices, the front surface was changed from planar to a random pyramid texture to improve light capture and to increase J_{sc}. Additionally, the width of the rear isolation region was decreased to lower series resistance, while employing the gap contamination mitigation strategies discussed in section III.C.iii. The last major change in processing was the development of cells from pre-grown LPCVD *poly*-Si supplied by Fraunhofer Institute for Solar Energy Systems. Figure 29 shows the device processing sequence.These LPCVD *poly*-Si cells not only have a much more consistent tunneling oxide thickness than was achieved at NREL, but they also demonstrate consistently good passivation, with iV_{oc} ~730 mV. The process sequence involves deposition of doped *a*-Si:H using direct patterning, drive-in of dopants with a high temperature annealing step, followed by passivation and metallization. However, the thick ~200 nm intrinsic *poly*-Si requires thicker doped *a*-Si:H to reach the levels of doping required in our cells. The longer deposition time in turn leads to significantly more shunting because dopants can diffuse farther out into the *poly*-Si isolation region. Another factor that possibility contributes to the higher shunt losses is the lower density of trap defects LPCVD *poly*-Si which has larger grain sizes compared to our in-house

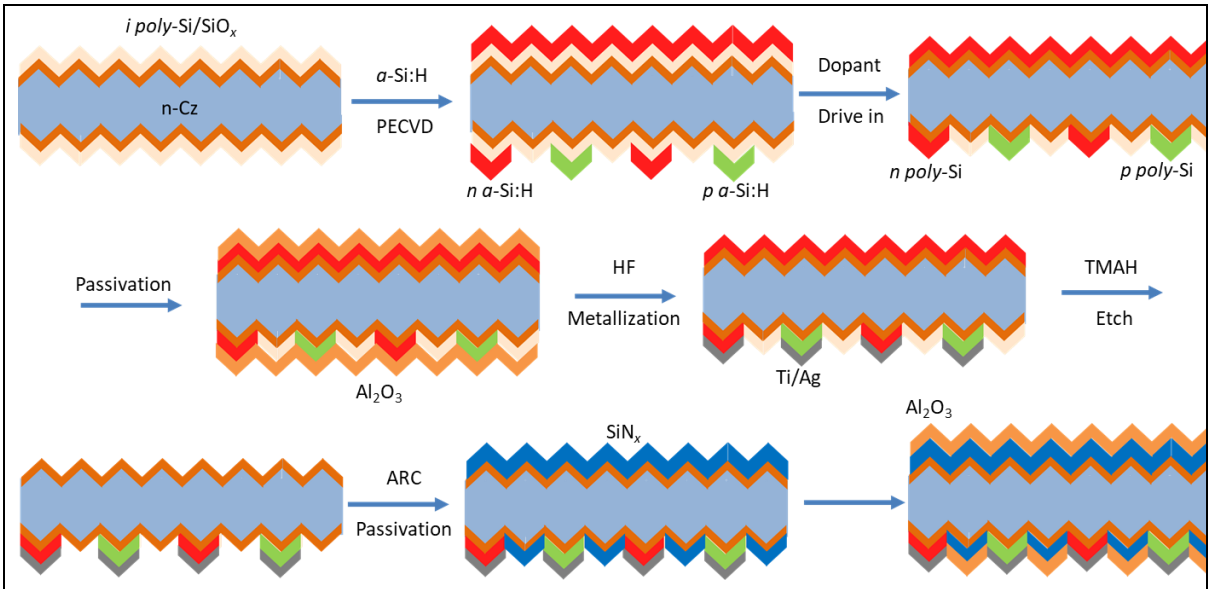

Figure 29: Flow diagram of the process used to fabricate the highest efficiency device of 18.6%. Pre-grown LPCVD *poly*-Si is doped with in-house plasma-deposited *a*-Si:H and annealed to drive in the dopants. Following metallization, the 200 nm thick *poly*-Si at the front of the device and between the rear fingers is etched away with a TMAH solution. The cell is re-passivated with SiN_x and Al_2O_3 and a forming gas anneal to complete the device.

PECVD *poly*-Si. As discussed earlier, the trap defects enhance the dopant compensation effect. To resolve the shunting issue in the LPCVD IBC cells, a combines SF_6 plasma reactive ion etching and tetramethylammonium hydroxide etching process was used to completely remove any *poly*-Si from the gap between doped fingers. A thick front *poly*-Si in the device also reduces the J_{sc} through parasitic absorption. After the poly-Si layer was removed, the surface was re-passivated with a SiN_x/Al_2O_3 stack followed by annealing in forming gas. These cells reached a high efficiency of 18.6%, our current record, shown in Table 2. The completely in-house fabricated IBC cells reached a J_{sc} as high as 39 mA/cm^2 and *FF* ~ 75%, with several cells > 17% efficiency, but the efficiency was limited by low a V_{oc} of ~650 mV.

Figure 30 shows the current-voltage curves of the best 5 cells fabricated over the course of this project. All cells are limited by lower J_{sc} than should be expected for high degrees of light capture. A 40 mA/cm^2 J_{sc} or higher is more in line with top-performing cells. Additionally, these cells suffer from lower V_{oc} than desired, where 700 mV or higher is more appropriate. These cells were all fabricated in 202.

Since both J_{sc} and V_{oc} are interdependent, poorer light trapping could be limiting V_{oc} or poor passivation could be limiting J_{sc}. Figure 31 shows quantum efficiency and reflectance curves of the 18.6% cell. The shape of the internal and external quantum efficiency curves indicates good light capture for all wavelengths, since no specific wavelength range is limiting the J_{sc}. However, we expect that the quantum efficiency should level off at close to 100% rather than 90%. Because the internal (green) and external (blue) QE curves are quite similar, the cell is collecting almost all the carriers which are absorbed within it. The reflectance curve (orange) shows close to zero reflectance for most wavelengths, so most incident light is entering the cell rather than reflecting away from it. This indicates that although the cell is likely capturing light well, it is not able to collect the generated charge carriers well at the contacts. This could be a result of recombination within the device before the carriers can be captured or by series resistance effects reducing the current collected.

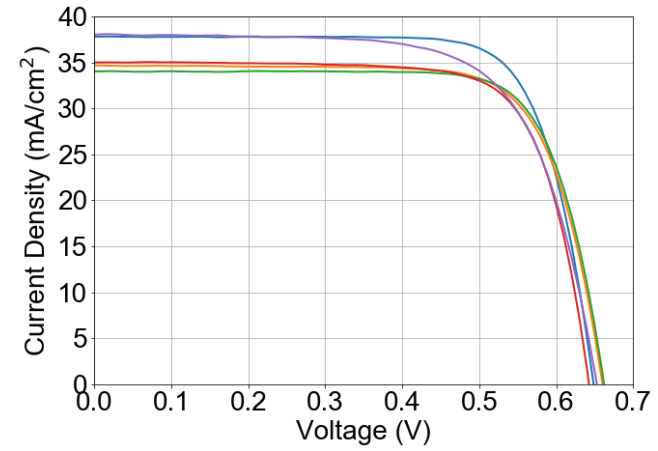

Figure 30: Current-voltage curves of the five most efficient cells fabricated throughout this project. Cells are limited by low J_{sc} and V_{oc}, but demonstrate good fill factor which could be improved with adjustment of cell dimensions.

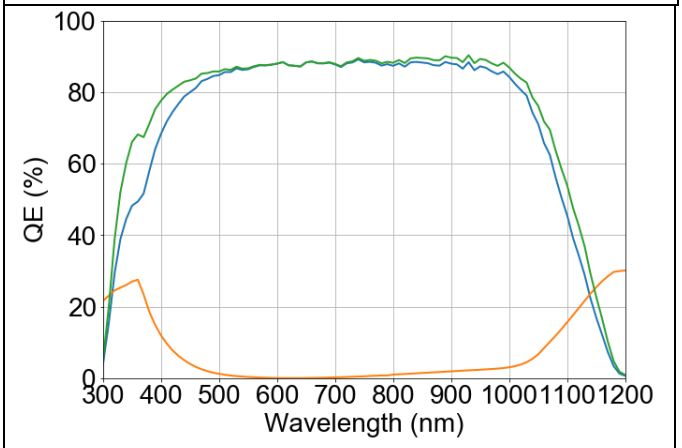

Figure 31: External quantum efficiency (blue), reflectance (orange), and internal quantum efficiency (green) of the 18.6% efficient cell fabricated in this project. The shape is in line with good light capture across the spectrum, but is shifted downward by ~10% for all values.

Figure 32 shows the the photoluminescence (PL) image of the best device, 18.6% efficiency, which we can use to identify if the V_{oc} is the limiting factor in the device performance. Though the cell area is uniformly bright, indicating that no specific part of the cell is causing poor passivation, it is not as bright as other higher performing cells. Additionally, the region surrounding it is darker, whereas this region should normally be brighter than the cell area. These observations point to the idea that poor passivation is the cause of the reduced V_{oc} as well as the low J_{sc}.

III.D.ii.2 Pathways Towards Final Goal of 21%

To achieve the highest J_{sc}, V_{oc}, and *FF* values in a single device, better process optimization would be needed. The most promising pathways to achieve 21% efficiency is to utilize the pre-grown LPCVD *poly*-Si. By using this more standardized starting point, we can eliminate variations introduced during earlier steps, especially the growth of the tunneling oxide which has limited performance for many baseline devices. Additionally, with the shunting issue mitigated by the RIE/TMAH etching step and repassivation, narrower IBC gap widths could be used to improve series resistance and thus fill factor of the devices.

III.D.iii PERC-Like Solar Cells

While the primary focus of this project was developing patterning techniques for IBC cells, another goal was to apply said patterning technique to local doping beneath the front metal grid for PERC-like devices. To determine the effect of this dopant patterning technique on the performance of PERC-like devices, a simple study was conducted comparing locally-doped devices patterned with contact masks to uniformly-doped cells. The devices fell into three categories: devices with uniformly thin ~15 nm front *poly*-Si, devices with uniformly thick ~40 nm front *poly*-Si, and devices with thick ~40 nm *poly*-Si beneath the front metal grid and thin ~15 nm front *poly*-Si everywhere else. Table 3 contains the J-V parameters for all PERC-like cells,

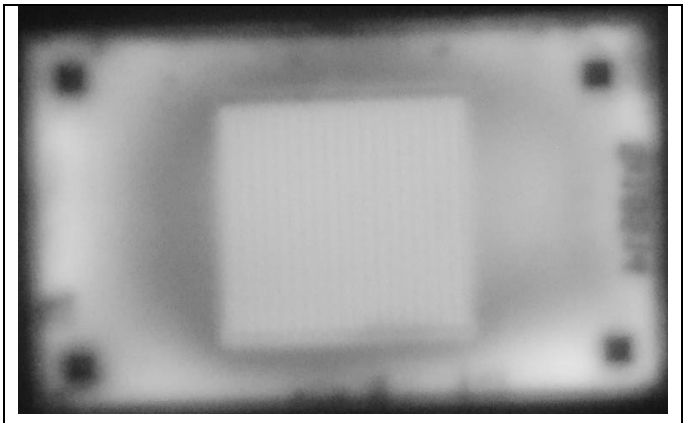

Figure 32: Photoluminescence image of the 18.6% cell. The square cell area is uniformly bright, but a dark halo surrounds it.

while Figure 33 shows three current-voltage curves of the top cell of each type of PERC-like device fabricated.

From these results, it is clear that the locally doped cells are an improvement over both types of uniform cells, largely as a result of the fill factor losses that the uniform cells have. While it was expected that the locally-thick *poly*-Si cells would outperform the uniformly-thick cells in J_{sc} and the uniformly thin cells in V_{oc}, the J_{sc} and V_{oc} values are fairly close among them all. We attribute the series resistance seen in the thin front *poly*-Si cells to higher sheet resistance at the front and the shunting seen in the thick front *poly*-Si cells to wrap around of excess *n*-type *poly*-Si to contact the *p*-type *poly*-Si at the rear of the devices. While these results do meet the milestone demonstrating the applicability of the masked PECVD patterning technique to PERC-like devices, more work should be completed to increase the efficiency of these locally-thick devices above 20%.

Table 3: *J-V* data of PERC-like devices with front *poly*-Si thickness comparison

***Poly*-Si thickness**	**J_{sc} (mA/cm^2)**	**V_{oc} (mV)**	**FF (%)**	**Eff (%)**
40 nm	37.91	693	57.23	15.04
	36.58	692	67.80	17.16
	36.32	693	68.38	17.21
15 nm uniform / 40 mn local	36.41	696	68.17	17.28
	37.55	698	70.97	18.60
	37.56	699	72.74	19.10
15 nm	37.73	694	65.24	17.08
	37.87	692	54.12	14.18
	37.37	688	59.17	15.21

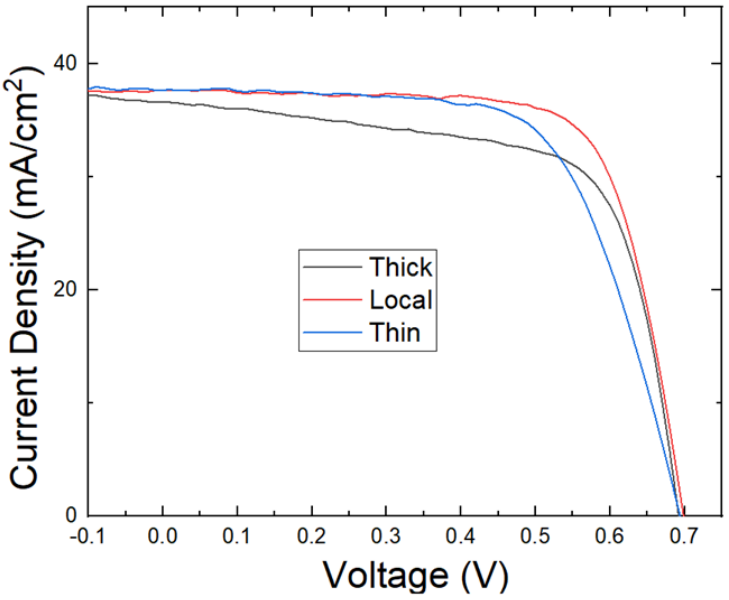

Figure 33: Current-voltage curve of the top PERC-like devices fabricated in each category of uniformly thick (black) front *poly*-Si, uniformly thin (blue) front *poly*-Si, and locally thick (red) front *poly*-Si.

III.F Milestones progress report

Milestone Number	Milestone Description	Target Completion Quarter	Final Remarks
1.1, 1.2, 1.3	Measure the light intensity from the UV source at the light source to substrate distance using a fiber optic cable coupled to a UV-visible (UV-Vis) spectrometer used for emission spectroscopy. Ensure we can measure light emission from the UV source in the ~250 – 350 nm range through a crystal quartz, LiF, or MgF2 window. A >100-fold increase in light intensity in this region above the instrument noise level will prove effectiveness of the UV light source. Demonstrate the feasibility of UV-induced activation of surface sites on a-Si:H to promote surface hydrogen desorption for enhanced reactivity at low temperatures. Verify surface hydrogen desorption and surface reaction of silanes using in situ ATR-FTIR spectroscopy. Specifically, monitor the integrated infrared absorbance for the surface SiHx (x = 1,2,3) stretching modes at ~2100 cm 1. A ~50% decrease in integrated absorb Deposit 30-50 nm thick, patterned intrinsic a-Si:H films and show clear separation between the line patterns with abrupt step edges using profilometry. Show a step edge width of ~20-30 µm for a 1 mm line.	Q1-Q4	Due to the lack of availability of commercially-available F_2 excimer laser light sources, photo-deposition of *a*-Si:H from SiH_4 was deemed unfeasible for commercial processing of solar cells. Changing to photo-assisted etching of *a*-Si:H using using UV light in a Cl_2 atmosphere. Sharp line widths were achieved by patterning through Si shadow masks. However, no significant and reproducible differences in the etching of a-Si:H with either Cl_2/Ar or SF_6/Ar plasma were observed. The direction was switched to a direct deposition of doped *a*-Si:H through shadow masks for the rest of the project.
2.1, 2.2, 2.3	Deposit ~10 nm of patterned a-Si:H over c-Si substrates larger than 20×20 mm and show clear separation between the line patterns with abrupt step edges using profilometry. Show a step edge width of ~20-30 µm or less. Essentially, reproduce the result achieved in Quarter 4, but in a film Si tool with doping capability. Identify the most promising of the three techniques above for patterning. Show that we can obtain doping levels of 1019 cm-3 using SIMS/Hall measurements for the doped lines and resistivity >100 □·cm between two adjacent lines. Show iVoc >680 mV using the Sinton lifetime tool for patterned test structures (see Fig. 1) fabricated using plasma etching, plasma CVD, or a printing	Q5-Q8	Masked PECVD was identifies as the most promising patterning technique, obtaining active doping levels ~10^{20} cm^{-3} for doped lines. iV_{oc} > 690 mV and > 710 mV were achieved for *p*- and *n*-type films, respectively. Initially, gap contamination led to low gap resistivity, but mitigation strategies reported in published manuscript maintain gap resistivity >100 Ω·cm. Manuscript describing production of IBC cells

	method. Specifically, the test structure will consist of a n-type c-Si wafer (float-zone or Czochralski; polished or saw damage removed, ~2□10^{15} cm^{-3}), with a 1-2 nm thick tunneling SiOx layer grown thermally on both sides of the wafer, with 30-50 nm of p-type or n-type poly-Si (~10^{19} cm^{-3}) lines on both sides. Produce one peer-reviewed publication summarizing the method for dopant patterning.		using masked PECVD for patterning is in production.
3.1, 3.2, 3.3, 3.4	A quantitative table of limiting factors in cell design using simulations, and a detailed step-by-step plan to incorporate these into fabrication. Optimize the processing conditions, masks, and mask alignment (thermal expansion etc.), to obtain n+- and p+-type interdigitated a-Si:H/poly-Si patterns on n-type c-Si substrates based on the simulations in Quarter 9, with a dopant concentration above 10^{19} cm^{-3}. Demonstrate the dopant patterning technique developed for front emitter of p-PERC cells for fabrication of shallow emitters. Characterize the dopant depth profile and lateral profile and show that the width of the additional doped finger is ~200 µm. Demonstrate a p- and n-doped pattern structure on a c-Si wafer, separated by an intrinsic or compensated gap, with lateral transition length of < 50 µm from n-type or p-type to intrinsic a-Si:H/poly-Si as determined with x-ray photoelectron spectroscopy or secondary ion mass spectroscopy elemental mapping. Show 15% efficient IBC cell structures (see Fig. 2). The back contacts in these IBC cells will consist of 30-50 nm n-type and p-type patterned poly-Si lines that are separated by an intrinsic or compensated poly-Si gap with a total pitch of ~1 mm. These doped layers will be grown on top of a 1-2 nm tunneling oxide layer. Finally, the doped layers will be metalized to measure IBC cell efficiency. Using similar doping methods, increase p-PERC cell efficiency by 0.5% absolute compared to a baseline architecture without patterned doping. Publish at least 1 peer-reviewed journal article in BP3.	Q9-Q12	Simulations in Quokka 2 demonstrate finger width ratio and gap width criteria for achieving high efficiency IBC cells. PERC-like devices were fabricated using the masked PECVD patterning technique and reached efficiencies >19% for cells with locally-doped front grids showing efficiency increase of >0.5% over uniform front doping. 15% efficient IBC cells were demonstrated with the stated patterning technique. A manuscript describing the contamination mechanisms and mitigation thereof was published in the IEEE Journal of Photovoltaics.

Final deliverable	Demonstrate c-Si IBC cell with 17% efficiency. Using surface profiling with SIMS, verify that the heavily doped n-type region of the emitter for the p-PERC cell is ~150 µm wide. Obtain a 20×20 mm^2 c-Si IBC cell with certified efficiency of ~21%. Use patterned doping to increase PERC cell efficiency by 1% absolute compared to a non-patterned baseline. Publish at least 1 peer-reviewed journal article in BP4.	Q13-Q16	Several IBC cells with > 17% efficiency up to 18.6% have been demonstrated using the masked PECVD patterning technique. Though J_{sc} and V_{oc} are lower than expected, FF . Plans are in place to reduce the width of the intrinsic isolation region to improve performance of the cells and increase efficiency to reach the 21% goal.

IV. Conclusions: Our goal in this project was to develop a novel patterning technique for the rear dopants of interdigitated back contact (IBC) and two-sided silicon solar cells which would be more scalable and lower cost than current patterning techniques such as photolithography. A scalable and more cost-effective patterning technique would be more industrially viable and enable high-efficiency IBC cells to be adopted into wider production than they currently are. To accomplish this, the first technique attempted was photo-assisted deposition of doped *a*-Si:H through a shadow mask, but literature review found this to be too difficult of a task due to the extreme intensity of high-energy photons required to desorb even one H atom from the surface. After switching the direction towards photo-assisted etching of hydrogenated amorphous silicon (*a*-Si:H) using UV light, no reproduceable differences were observed in the etching of *a*-Si:H for either Cl_2/Ar or SF_6/Ar plasma, so the direction was switched again. The final patterning technique decided upon was masked plasma deposition of doped *a*-Si:H using shadow masks. Using these shadow masks as patterning tools for plasma-enhanced chemical vapor deposition (PECVD) of doped *a*-Si:H, it was demonstrated that such patterns can be achieved, with high implied open-circuit voltages (iV_{oc}), but that spreading of dopants also occurs during cell processing which could lead to cell shunting. These contamination mechanisms - spreading beneath the contact mask during *a*-Si:H deposition and desorption/readsorption during high-T annealing – were thoroughly investigated and mitigation strategies were developed for each, resulting in the projects first publication. Numerous simulations were performed in the Quokka 2 solar cell simulation software to optimize the design of IBC cells to be fabricated. Following fabrication of initial devices, it was found that despite contamination by dopants through the mechanisms mentioned above, shunting did not always occur across the IBC isolation region. This effect was studied further through scanning probe microscopy measurements of IBC structures and simulations of the contaminated isolation region, showing that a compensation effect can prevent shunting despite contamination of the entire region resulting in the second publication from this project. Throughout the project, 209 IBC and two-sided solar cells were fabricated using the masked PECVD patterning technique, resulting in several devices with efficiencies >17% and one reaching 18.6% following etching back of the isolation region, but none reaching the project end goal of 21%. Utilizing the masked deposition technique allowed the two-sided devices to increase in efficiency by >1% compared to non-patterned devices. Overall, the novel technique developed in this project shows promise as a patterning technique for both IBC cells and two-sided devices, though significant optimization is required.

V. Budget and Schedule

Spending Summary By Budget Category

Budget Categories Per SF424-A	Approved Budget per SF-424A					Actual Expenses	% of Project
	BP1	BP2	BP3	BP4	Total Budget	Cumulative Actuals	% of Project
a. Personnel	49,704	50,245	50,793	51,343	202,085	**193,790.60**	31.51%
b. Fringe	21,518	22,067	22,625	23,194	89,404	**109,672.43**	17.83%
c. Travel	3,000	4,000	1,200	1,200	9,400	**5,594.10**	0.91%
d. equipment	0	0	0	0	0	**17,076.81**	2.78%
e. Supplies	8,973	8,973	3,961	3,674	25,581	**215,940.21**	35.11%
f. Contractual	49,940	50,018	50,030	47,153	197,141	**0.00**	0.00%
Total Direct Charges	$133,135	$135,303	$128,609	$126,569	523,616	**542,074.15**	
Indirect Costs	$28,131	$22,175	$20,431	$20,647	91,384	**72,925.85**	11.86%
Total Charges	$161,266	$157,478	$149,040	$147,216	615,000	**615,000.00**	100.00%
DOE Share	$161,266	$157,478	$149,040	$147,216	$615,000	**615,000.00**	$615,000.00
Cost Share	$17,918	$17,498	$16,560	$16,357	$68,333	**68,333.00**	$68,333.00
Cost Share Percentage	10%	10%	10%	10%	10%	**10%**	10.00%
Total	$179,184	$174,976	$165,600	$163,573	$683,333	**$683,333.00**	$683,333.00

VI. Path Forward: There are numerous paths forward resulting from the work completed in the course of this project, including further investigation into the behavior of the contaminated IBC gap, spreading of radicals during PECVD patterning, and development of improved IBC processing using masked PECVD as the dopant patterning method. In particular, more detailed simulations of the defective *p-i-n* junction would be applicable not only to *poly*-Si/SiO_x IBC devices, but also to other semiconductor devices such as fast switching diodes used for signal transmission [33]. The behavior of radicals within the plasma phase and at the surfaces during PECVD should be further investigated in more precise manners such as in pillar-hall structures to estimate more accurately the sticking coefficients of certain radical species. Lastly, if the IBC fabrication processes developed in this project can be optimized through finger dimension changes, film optimization, and improved repeatability, then masked PECVD may prove to be a cheap, scalable method for patterning such high-efficiency devices. For further research, perovskite/Si tandem cells are a popular field of study that show promise as a simple and inexpensive method for breaking past the limits of single junction silicon devices [34, 35]. Utilization of masked PECVD as a patterning technique for the rear dopants of the Si bottom cell may be the low-cost complement to the simple liquid processing of the perovskite top cell, leading to further advances within the tandem architecture for high-efficiency IBCs. Finally, the results which we showed for patterning of the front dopants on PERC-like devices could be easily adapted into fully-additive industrial processing for locally-doped front emitters, without the need for any subtractive processing.

VII. Publications Resulting from This Work

This work was presented at five different conferences, one of which was an oral presentation at the IEEE Photovoltaics specialists conference. One manuscript was recently submitted to the Journal of Photovoltaics.

Conference Presentations					
Full Author List	**"Paper Title"**	**Poster/ Oral**	**Session/Symposium/ Conference**	**Conference Location**	**Dates**
Matt Hartenstein, William Nemeth, Vincenzo LaSalvia, Matthew Page, Paul Stradins, Sumit Agarwal	*Development of Low-Cost, Scalable Doping Techniques for Interdigitated Back Contact Crystalline Silicon Solar Cells*	Poster	28th Annual NREL Silicon Workshop	Winter Park, CO	Aug-18-2018
Matthew B. Hartenstein, William Nemeth, Vincenzo LaSalvia, Steve Harvey, Matthew Page, David Young, Paul Stradins, and Sumit Agarwal	*Understanding and Mitigating the Contamination of Intrinsic poly-Si Gaps in Passivated IBC Solar Cells*	Oral	46th IEEE Photovoltaic Specialists Conference (PVSC)	Chicago, IL	June 16-21, 2019

Matthew B. Hartenstein, William Nemeth, Vincenzo LaSalvia, Steve Harvey Matthew Page, Paul Stradins, and Sumit Agarwal	*Development of Mechanically-Aligned, Masked Plasma Deposition for Simpler Patterning of Interdigitated Back Contact Crystalline Silicon Solar Cells*	Poster	Rocky Mountain Chapter of AVS	Westminster, CO	Sep-11-13, 2019
Matthew B. Hartenstein, William Nemeth, Vincenzo LaSalvia, Steve Harvey, Matthew Page, David Young, Paul Stradins, and Sumit Agarwal	*Understanding and Mitigating the Contamination of Intrinsic poly-Si Gaps in Passivated IBC Solar Cells*	Oral	Materials Research Society Fall Meeting	Boston, MA	Dec-2019
Matt Hartenstein, William Nemeth, Vincenzo LaSalvia, Matthew Page, Steve Harvey, David Young, Sumit Agarwal, Paul Stradins	*Effect of Dopant Compensation on the Conductivity of the Intrinsic poly-Si Isolation Region in Passivated IBC Silicon Solar Cells*	Poster	47th IEEE Photovoltaic Specialists Conference (PVSC)	Online	Jun-2020
Matthew B. Hartenstein, William Nemeth, Caleb Stetson, Vinnie LaSalvia, Steve Harvey, Matthew Page, CS Jiang, Mowafak Al-Jassim, Sumit Agarwal, Paul Stradins, David L. Young	*Dopant Compensation in Intrinsic poly-Si Gap of Passivated Interdigitated Back Contact Si Solar Cells*	Oral	PVSEC-30	Korea/ Online	Dec-2020
Matt Hartenstein, William Nemeth, Vincenzo LaSalvia, Matthew Page, Steve Harvey, David Young, Sumit Agarwal, Paul Stradins	*Dopant Compensation Within the Intrinsic poly-Si Isolation Region in poly-Si/SiOx Passivated IBC Si Solar Cells*	Poster with Oral Overview	SiPV	Online	Apr-2021

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"*Trap-Assisted Dopant Compensation Prevents Shunting in Poly-Si Passivating Interdigitated Back Contact Silicon Solar Cells*," Matthew B. Hartenstein, Caleb Stetson, William Nemeth, Vincenzo LaSalvia, Steven P. Harvey, San Theingi, Matthew Page, Chun-Sheng Jiang, Mowafak M. Al-Jassim, David L. Young, Sumit Agarwal, and Paul Stradins, *ACS Applied Energy Materials* **4**, 10774 (2021).

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