Sub-Kelvin High-Mass CCD Detectors for Dark Matter & Neutrino Searches: Technical Report

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1 Progress toward sub-Kelvin CCD

This project aims to achieve two synergistic goals: 1) Develop a high mass low temperature CCD detector to measure charge transfer efficiency at sub-kelvin temperatures. 2) Use alternating surface bias at low voltages to produce NL phonons at the same rate as CDMS HV but without the need for HV bias. This will allow for a non-invasive NL amplification and paves the way for future single electron resolution large mass DM or CEνNS detectors. Below we outline our proposed work program and expected deliverables at each stage of the project.

The first few months of the project were spent to troubleshoot unexpected oscillations that we observed in our ionization readout. We found that those oscillations were due to the amplifier output stage coupling to the feedback. We are using high impedance wiring compared to CDMS II wiring. CDMS wiring consisted of low impedance Cu striplines. The charge readout electronics consists of a cold FET whose drain and source channels are carried via long wires to the warm electronics including a standard large bandwidth Cascode circuit. Our drain and source wires are twisted Be-Cu thin wires with much larger impedances and are more prone to oscillations. We found that by using zero-pole compensation technique at the warm end and adding larger capacitances to the integrator stage of the charge amplifier circuit (at the expense of smaller bandwidth), we can remove the oscillations and achieve similar noise performance as was demonstrated with CDMS II readout (Fig **??**). Our ionization readout noise performance is now totally adequate to measure Charge Transfer Efficiency (CTE). Additionally, we can now study leakage current down to $\sim$ fA level considering the 40 MΩ feedback resistors.

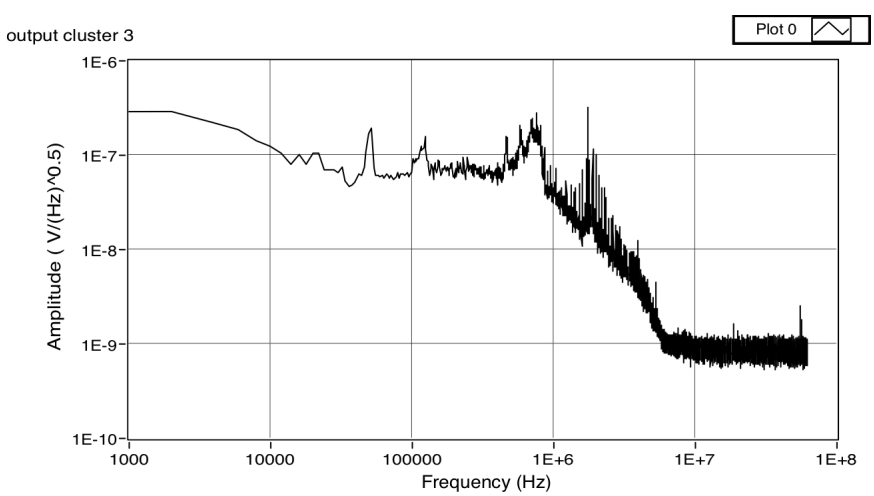

Figure 1: Noise spectrum obtained with new higher impedance wiring utilizing CDMS cold FET readout. The 10^{-7} V/$\sqrt{Hz}$ level is low enough to reach the level required for direct leakage current measurement in CDMS type detectors.

As we had planned in the original proposal we proceeded with fabricating a single-sided phonon-mediated 100 g Si detector. One face of the detector was processed with CDMS phonon readout architecture and separated into 4 independent channels for position reconstruction as shown in

Fig.**??** (right). The detector has a different interface structure than standard SuperCDMS detectors in that it doesn't include any amorphous layer between the phonon sensors and the substrate. In a previous study we had shown that the leakage performance for this new interface is similar or superior to the standard CDMS Si detectors (to be published soon). The opposite face of the detector was left bare and polished and a CCD electrode was fabricated on a PCB board as shown in Fig. **??**(left). The CCD electrode will come in contact with the bare surface of the detector via a gap of 25 microns using a ring shape regular paper as shown in Fig.**??** (middle). We have simulated the filed inside the crystal and confirmed that the presence of this thin vacuum gap doesn't affect the E-field inside the crystal and allows to test different electrode structures with a single detector.

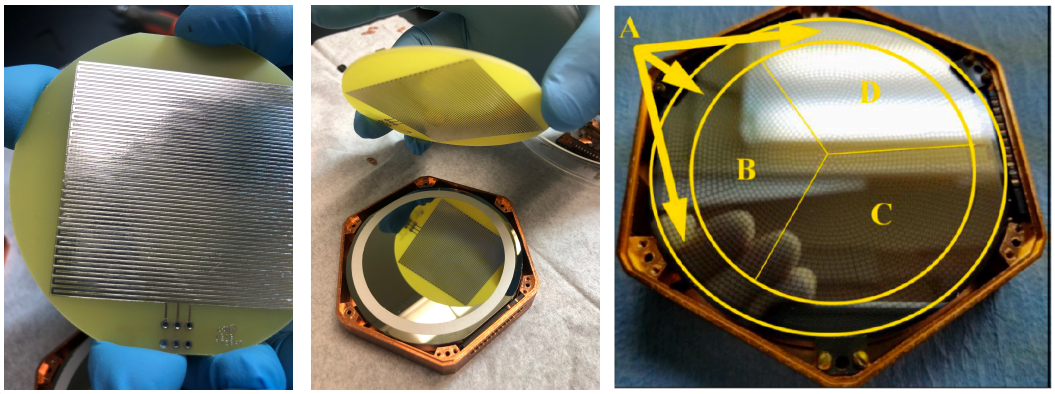

Figure 2: (Left) CCD geometry laid on a PCB board. Two combs of alternating bias electrodes are interleaved with ground electrode that meanders between the two sets. (Middle) The electrode is positioned on the polished surface of a 7.5 cm diameter and 1 cm thick Si detector and separated from the substrate via a gap of 25 microns provided by a paper ring. (right) The other surface of the Si substrate is processed with standard CDMS tungsten based Transition edge sensors.

The detector and electrode assembly were installed at the cold stage of our dilution refrigerator Fig.**??** (right). We had to drive the bias electrodes using alternating high frequency voltages (1 V at 10 MHz). In order to compensate for the losses through the fridge wiring a driver electronics circuit was designed and manufactured Fig.**??** (left). We have had one fridge run with this configuration but found that the driver circuit heats up the 10 mK stage of the fridge. We have found the source of this heating and planed to run the device again.

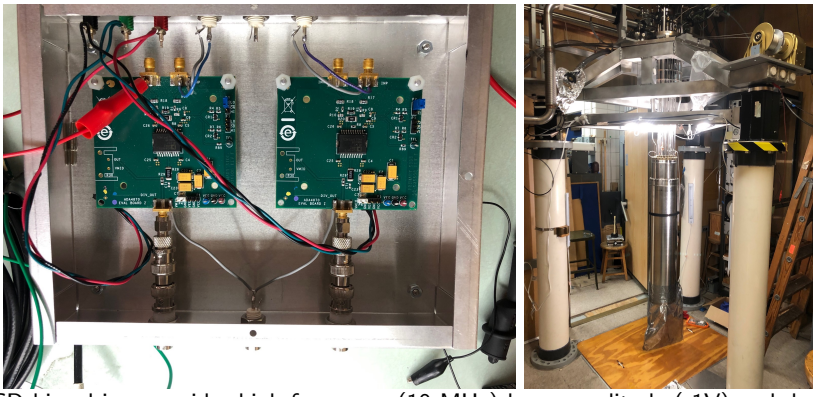

Figure 3: (Left) CCD bias driver provides high frequency (10 MHz) large amplitude (1V) and designed to compensate for the siginifcant losses through the fridge high impedance wiring. (Right) TAMU 400 μW setup

Using this device geometry, we can estimate the Neganov-Luke phonon generation efficiency at the surface by alternating field and thus, estimate the CTE along the surface of the detector. Provided that we find this parameter from this setup, we can design a full scale large mass CCD

wherein, we directly measure ionization transport using ionization readout.

Since the completion of the equipment needed for operating the large CCD in our fridge and our initial refrigerator runs to demonstrate the feasibility of alternative high frequency biasing scheme, we have experienced a sharp increase in the cost of liquid helium. Fortunately, our group has recently acquired a new cryogen-free dilution refrigerator with similar cooling power than our old 'wet' refrigerator. The new fridge is currently begin commissioned and has recently accommodated a standard CDMS style phonon detector with successful sensor readout. We will continue this R&D in our new setup and once we demonstrate NL phonon amplification with the alternating bias i.e. the principle behind this project, we will submit a new proposal at the next DOE FOA to demonstrate full large mass sub Kelvon CCD.