Loss of Utility Detection Capabilities for Today's Utility Interconnected Photovoltaic Inverters

Sigifredo Gonzalez
Jeffrey Zirzow
Nicholas Gurule
Sandia National Laboratories

Michael Ropp
Chris Mouw
Northern Plains Power Technologies

Gregory Kern
SunPower Inc.

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U.S. DEPARTMENT OF ENERGY

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Agenda

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Unintentional Islanding

- *What is this phenomena and how can it occur?*

Methods to prevent unintentional islanding from occurring

- *Categorizing the different methods of unintentional islanding algorithms*
- *Modeling efforts designed to quantify the effectiveness of combining different categories of UI algorithms.*

Implementing Electrical Power System support capabilities

- *EPS support capabilities introduce increased testing requirements*
- *Combining ride-though requirements with regulation functions*

Quantifying the balance for a sustained Island

- *Resonating reactive loads and resistive load requirements*
- *Calculating the islanded voltage and frequency values*

Unintentional Islanding

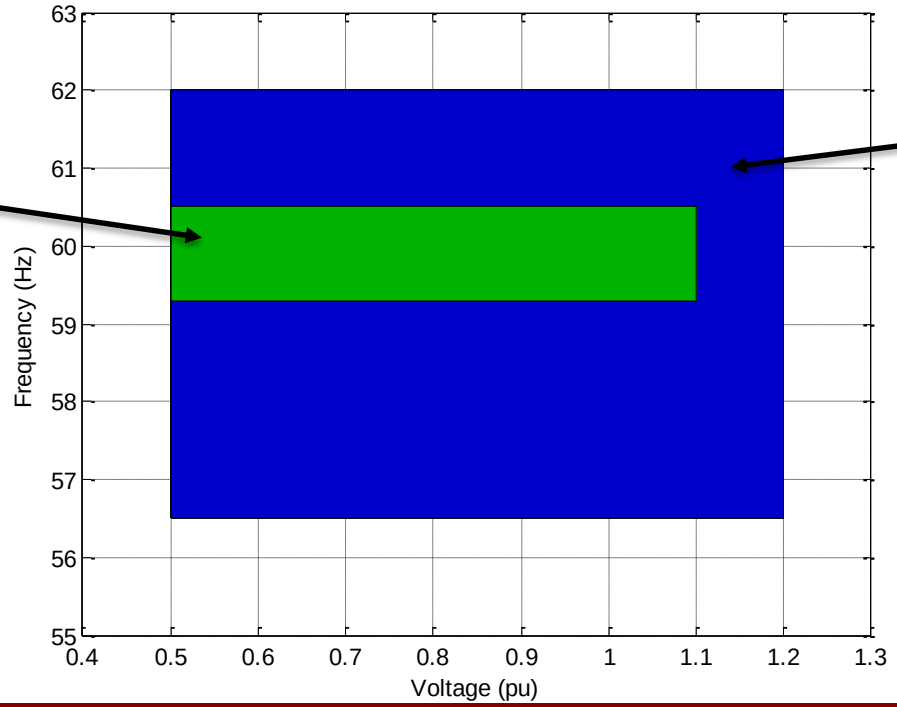
What is this phenomena and how can it occur?

The supporting of loads by a distributed energy resource that is not under control of the electrical power system (EPS) and usually occurs when a protection device isolates the generation and load.

- *The renewed interest is spurred by: the increasing level of penetration on distribution feeders, ride-through requirements, and EPS support functions.*

IEEE 1547-2003

IEEE P1547-2017



Categorizing the Unintentional Islanding Methods

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UI Class 1: produces an output perturbation in positive-sequence fundamental frequency or phase that is specifically for island detection and grows continuously as frequency error increases. No dead zone

UI Class 2: produces an output perturbation in positive-sequence fundamental frequency or phase that is specifically for island detection and grows with frequency, but not continuously to the trip bands.

UI Class 3: produces an output perturbation in positive-sequence fundamental frequency or phase, the magnitude of which does NOT grow with increasing frequency error or is NOT specifically designed for island detection.

Categorizing the Unintentional Islanding Methods

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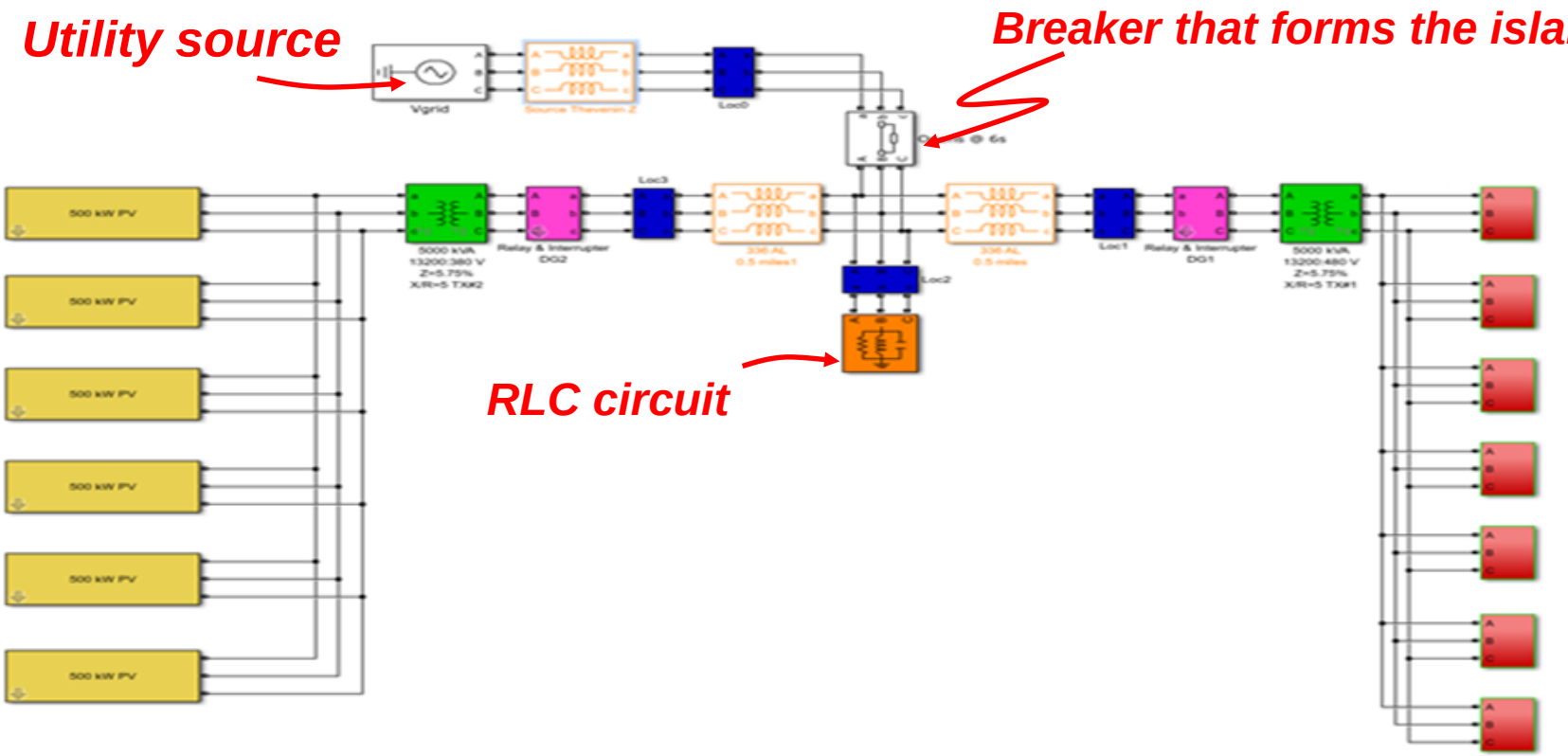
UI Class 4: produces an output perturbation at a harmonic (not fundamental) frequency that is specifically for the purpose of detecting an island.

UI Class 5: relies on passive methods (such as RoCoF or vector shift) or advanced signal processing of voltage or current measurements to detect island formation, which drives frequency to trip limits.

UI Class 6: manipulates the negative sequence current for the purpose of island detection. This may be achieved by several means, including altering individual phase current magnitudes or dithering the phase angle separation between the three output current phases

Modeling Circuit



Unintentional Islanding Method Combination Results

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ROTs > 2 s: total cases found

Vs	Amount of Class 1 DG			
	10%	25%	50%	75%
1A				
2	1	0	0	0
3	3	0	0	0
4	1	0	0	0
5	3	0	0	0
6	0	0	0	0

Vs	Amount of Class 2 DG			
	25%	50%	75%	90%
1	0	0	0	1
1A	0	0	0	0
3	20	7	13	
4	5	11	7	
5	15	15	11	
6	0	21	10	

Vs	Amount of Class 5 DG			
	25%	50%	75%	90%
1	0	0	0	3
1A	0	0	0	3
2	12	15	15	
3	24	26	23	
4				
6	3	24	20	

Load factor range: 54% to 120%@ 2% resolution
Power Factor range: .5 to .98 @ .02 resolution
Loading ranges resulted in 840 simulations for each test case

Results: If class 1 inverter was 25% or more on any combination, then no ROT > 2 sec and islanding is highly unlikely. This could relax the 67% guideline rule to a value as low as 25%.

Changes to Unintentional Islanding Test Procedure

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Test sequence to be repeated for each test condition listed below

TEST CONDITIONS FOR UNINTENTIONAL ISLANDING TESTING

Test condition	Functions active during Unintentional Islanding Test
1	IEEE P1547 default settings
2	SPS, RR, FW
3	VV, RR, FW, VW
4	Watt-Var, RR, FW, VW
5	SVar, RR, FW, VW

For each Test Condition from table
- 14 individual tests
- Repeated at 25% rating of DER
- Repeated for each test condition

Minimal number of tests:
14 x 2 x 5 = 140

RLC Circuit Method

Alternative method demonstrates RLC circuit is correctly connected by disabling UI method and creating an island, then enabling method and verifying method is sufficient at preventing an island

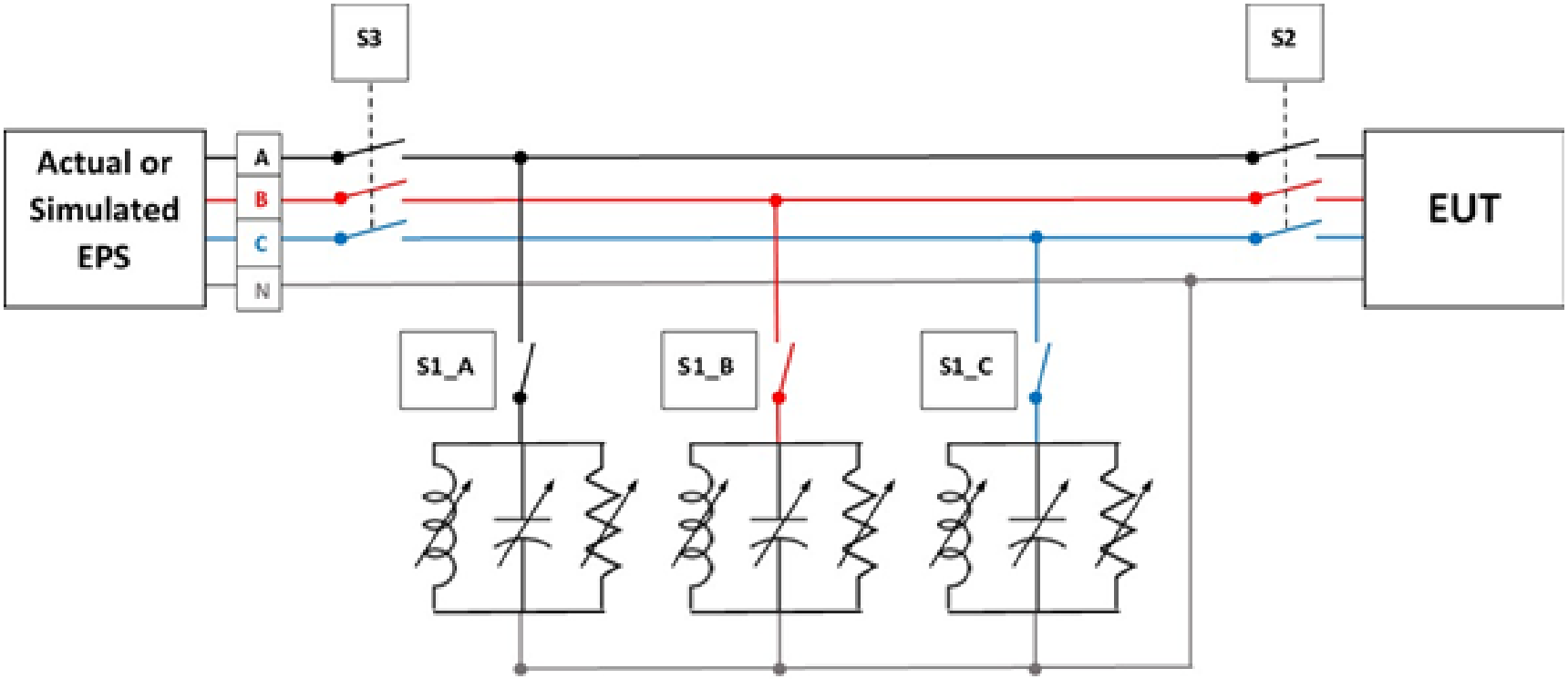
NEW ANTI-ISLANDING TEST REQUIREMENTS

Anti-islanding algorithm status	Number of tests
disabled	3
enabled	3

Minimal number of tests
6 x 2 x 5 = 60*****

*** 57% reduction in number of tests**

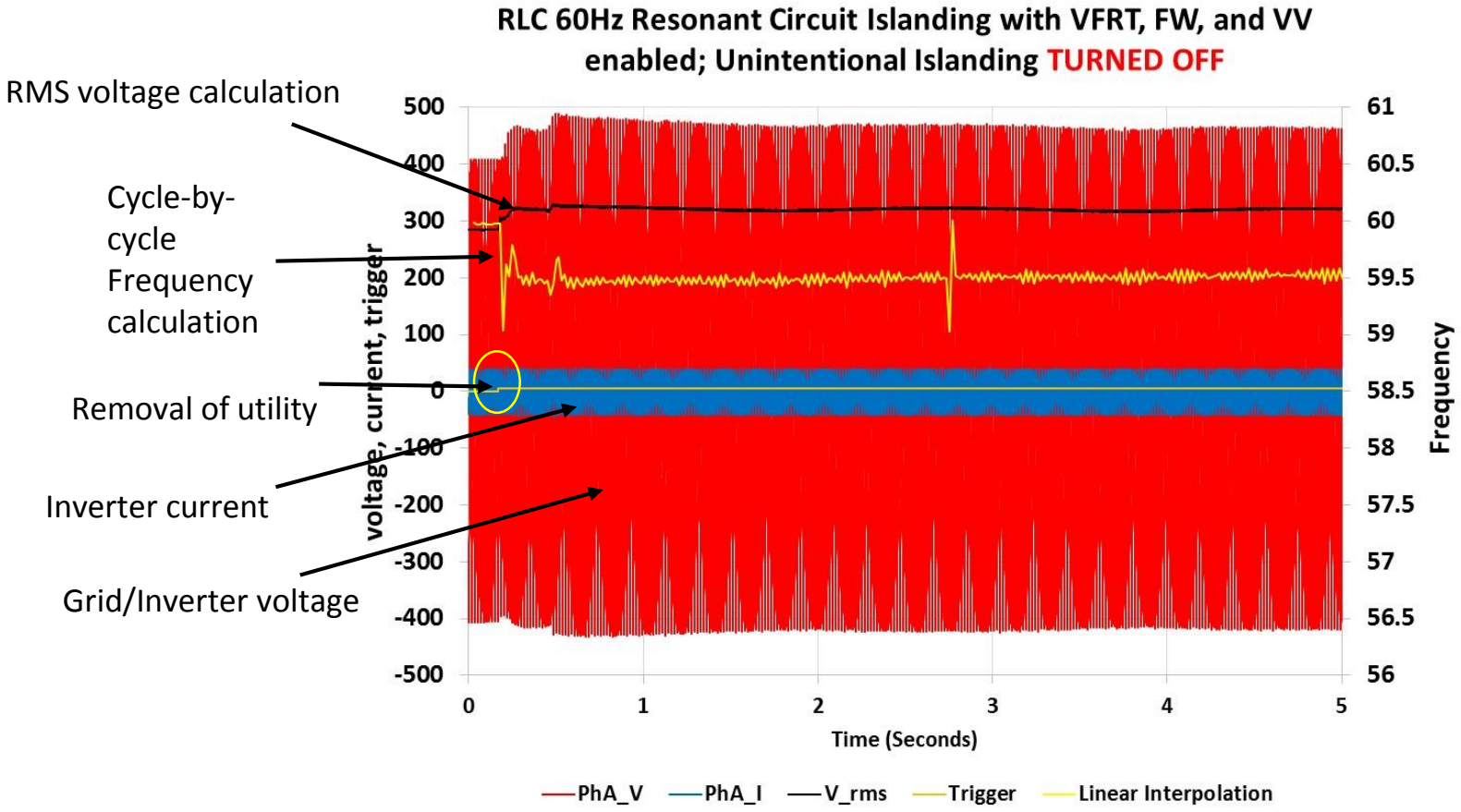
RLC circuit for Unintentional Islanding Tests



Using RLC circuit

Alternative method demonstrates RLC circuit is correctly connected by disabling UI method and creating an island, then enabling method and verifying method is sufficient at preventing an island

RLC circuit Unintentional Islanding Test Results

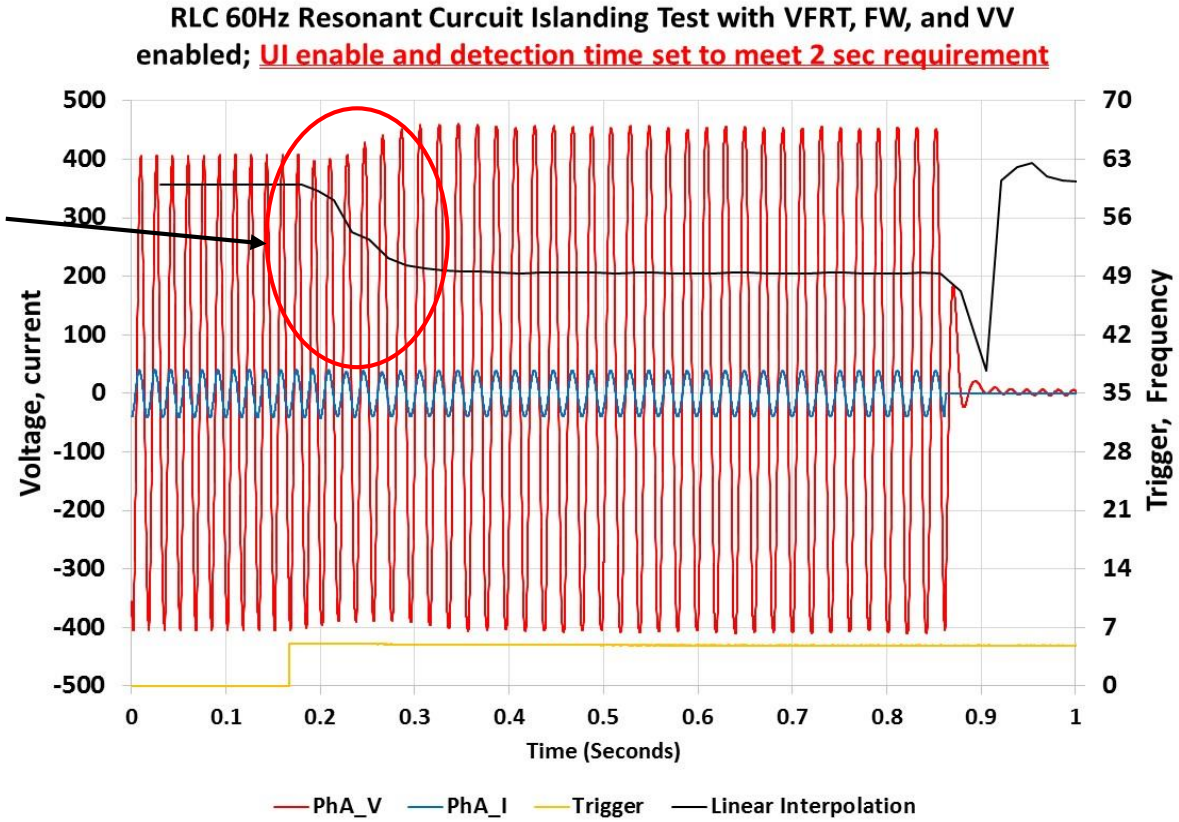


With UI algorithm ***OFF***– DER runs-on with minimal voltage and frequency variation, indicating decent load balance.

Validates RLC circuit is configured correctly

RLC circuit Unintentional Islanding Test Results

AI algorithm drives Frequency beyond Disconnect point



With UI algorithm ***ON***– DER pushes frequency and inverter responds favorably and de-energizes, well within the 2 second requirement.

Validates unintentional islanding method identifies loss of utility

Permissive Signal circuit for Unintentional Islanding Tests

Using Permissive Signal circuit

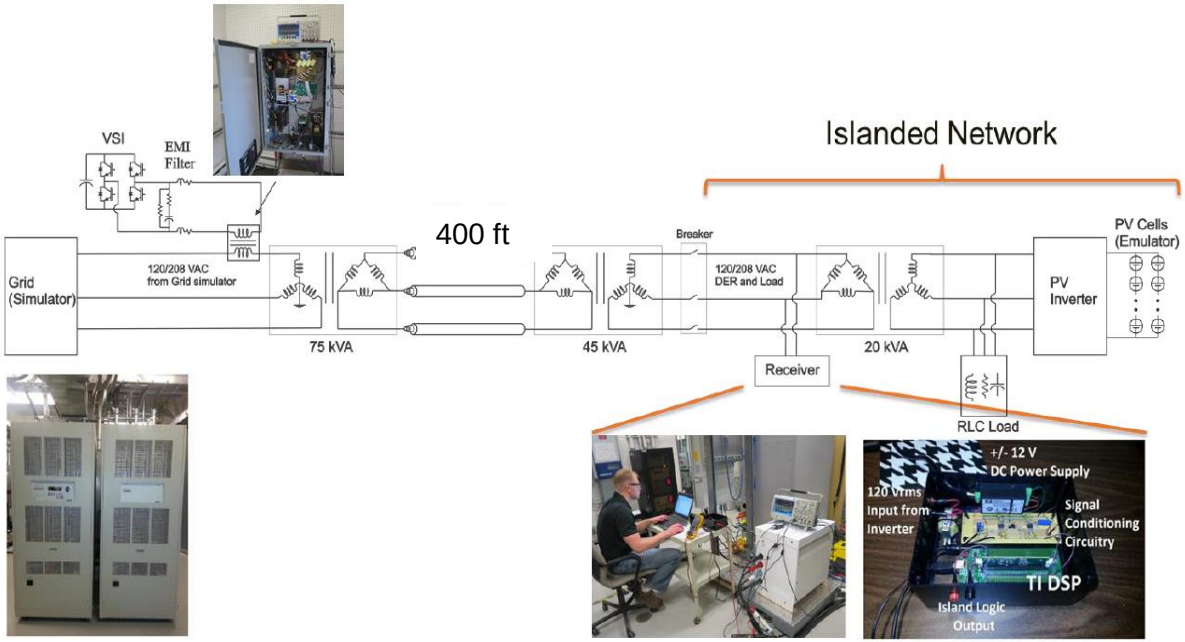
To validate the unintentional islanding capability of this method, only the communication path of the permissive signal is interrupted. The EUT interprets the loss of signal as loss of utility and ceases to energize the utility. This test applies to PLCP-based methods only.

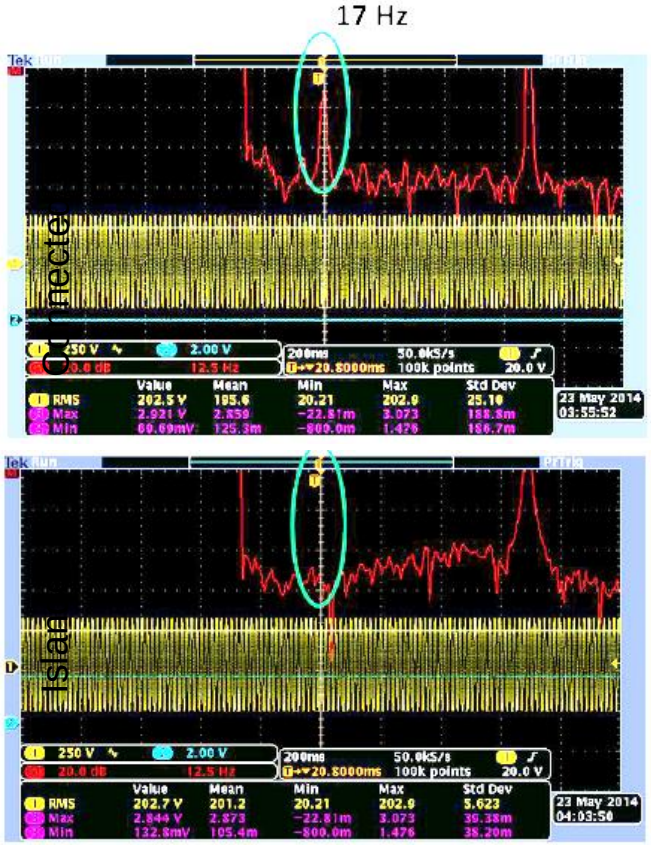
Number of tests:

Propose conducting 5 tests and if EUT ceases to energize upon removal of signal unintentional islanding testing is complete.

Permissive Signal Demonstration

- How can inverters detect unintentional islands and faults?
  - Demonstrated subharmonic power line carrier (PLC) islanding detection
  - Discrete-time Fourier algorithm implemented in low cost processor and analog circuit detected loss of utility in under 400 msec on average (Patent)





Island Power Balance Requirements

- **FOR A SUSTAINED ISLAND TO EXIST**
  - **Active power balance**
  - **Reactive power balance**

$$V_{Island} = V_{EPS} \times P_{Gen} / P_{Load}$$

V_{island}		F_{island}
Constant current	Constant power	Frequency with reactive balance
$V_{Island} = V_{EPS} \times P_{Gen} / P_{Load}$	$V_{Island} = V_{EPS} \sqrt{P_{Gen} / P_{Load}}$	$F_{Island} = F_{EPS} \sqrt{(Q_L + Q_{Lder}) / (Q_C + Q_{Cder})}$

Quality Factor calculations utilizing reactive power components

$$QF = \frac{\sqrt{(Q_L + Q_{Lder}) \times (Q_C + Q_{Cder})}}{P_{Load}}$$

(Stored energy to load ratio)

Impact: load and generation information can be used to determine islanded voltage and frequency values and for screening purposes.

Summary of Unintentional Islanding Status

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- **PENETRATION MODELING ASSESSMENTS**
  - **Potentially identify areas of concern**
  - **Provide info for screening process**

- **UNINTENTIONAL ISLANDING TEST PROCEDURE**
  - **Addresses EPS support functions and capabilities**
  - **Alternative method addresses onerous issue**

- **ISLANDED LOAD AND GENERATION PARAMETERS**
  - **Provides screening information**
  - **Potential for determining islanded voltage and frequency values**

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THANK YOU