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The Cibola Flight Experiment

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ABSTRACT

The Cibola Flight Experiment (CFE) is an experimental small satellite carrying a reconfigurable processing instrument developed at the Los Alamos National Laboratory that demonstrates the feasibility of using FPGA-based high-performance computing for sensor processing in the space environment. The CFE satellite was launched on March 8, 2007 in low-earth orbit and has operated extremely well since its deployment. The nine Xilinx Virtex FPGAs used in the payload have been used for several high-throughput sensor processing applications and for single-event upset (SEU) monitoring and mitigation. This paper will describe the CFE system and summarize its operational results. In addition, this paper will describe the results from several SEU detection circuits that were performed on the spacecraft.

I. INTRODUCTION

There is growing interest in using ***SRAM-based*** FPGAs within space systems due to low non-recurring engineering (NRE) costs, compressed life cycles and reduced costs (compared to ASICs), computational performance advantages, and reconfigurability. The ability to reconfigure SRAM-based FPGA devices after the spacecraft has launched allows them to be updated to accommodate evolving mission objectives, process data from multiple sensors, incorporate new scientific knowledge into the computational algorithms, or even to fix faults within the system. A variety of projects have demonstrated the benefits of using these FPGAs in spacecraft [1], [2]. Specific examples include the Mars rovers which use FPGAs for motor control and landing pyrotechnics [3] and the Australian satellite FedSat, which uses FPGAs as part of its high performance computing payload [4], [5]. While SRAM-based FPGAs offer a number of unique benefits for spacecraft electronics, they are susceptible to single event effects (SEE). SRAM-based FPGAs contain a large number of internal memory cells that can be upset by high energy particles. These include memory cells for user flip-flops, internal block memory, and for configuration memory. Single event upsets (SEUs) within the configuration memory are especially challenging as these upsets may change the programming of the FPGA. Any system that incorporates SRAM FPGAs in a high radiation environment such as space must provide a strategy for mitigating against such SEUs.

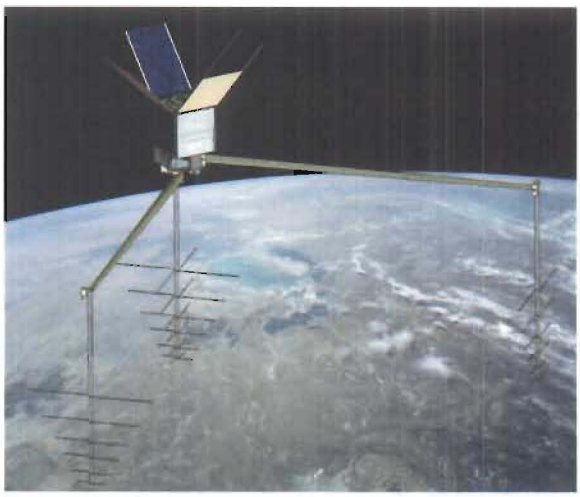

Figure 1: The Cibola Flight Experiment Satellite. http://www.n2yo.com/?s=30777

The Cibola Flight Experiment (CFE), illustrated in Figure 1, was funded by the Department of Energy and developed by Los Alamos National Laboratory. It is a technology pathfinder mission to investigate the use of

SRAM-based FPGAs as space-based reconfigurable processors [6]. The CFE instrument uses the reconfigurable logic to perform high throughput RF sensor processing. The real-time processing demands of this system are immense and cannot be performed using multi-processing with traditional radiation hardened processor architectures. This platform also incorporates a number of techniques for detecting SEUs and mitigating the effects of SEUs within the FPGAs. This paper will describe the CFE system and the results of several SEU detection experiments operating on the satellite.

II. SATELLITE BUS

The satellite bus that hosts the CFE payload was procured from Surrey Space Systems Technology, Ltd. (SSTL) of Surrey, United Kingdom, based upon SSTL's disaster monitoring constellation (DMC) and TOPSAT mission satellite designs [18]. The bus was designed to be 60.9x60.9x96.5cm in its stowed configuration with a mass of 160 kg, the maximum allowable by the launch vehicle.

The CFSat spacecraft structure is based on Aluminum and Aluminum Honeycomb panels, and includes a stack of "MicroTray" modules traditionally used by SSTL on all its micro satellites to house the spacecraft electronics and to provide structural support. The spacecraft employs an essentially cold biased, passive thermal control system with heater backup for emergency situations. Two body-mounted radiators are used to remove the excess payload heat.

The spacecraft is 3-axis stabilized, using a pitch momentum wheel and yaw reaction wheel, and dual redundant 3-axis magnetorquers. Pointing stability was nominally intended to be ±0.5 deg of nadir with pointing knowledge to 0.1 deg provided by dual redundant star trackers. Unfortunately, because of star camera powered on exposure to the Sun due to loss of attitude control during the numerous on-board computer crashes and rebooting, the star cameras are now only able to detect stars during daylight periods. Thus, nominally for up to 60 percent of the orbit, the attitude control system is incapable of maintaining the original design pointing stability with magnetometers alone. A GPS receiver is carried for location knowledge, and also to provide the accurate spacecraft pulse per second to the payload. However, SSTL is currently exploring the potential use of the GPS receivers to provide additional CFESat orientation information to the attitude control system in hopes of being able to recover additional attitude stability.

The CFESat power system is comprised of two body mounted and 4 deployable triple-junction, GaAs solar panels and a single ABSL LiLion battery. A raw 28V bus is distributed to both the spacecraft and payload, alongside a regulated 5V bus for the spacecraft. The system was designed to deliver over 110W orbit average to the platform and payloads, with 30W for the platform, and approximately 85W available for payload operations. However, due to an underperformance of the power system as well as recent loss of power production due to attitude instability, power management to maintain the battery voltage above 50% depth of discharge requires the payload to be turned off essentially every orbit when the solar beta angle is less than +/- 20 deg, even when the payload is only in the nominal 55W SEU detection mode during the rest of the orbit.

III. CFE INSTRUMENT DESIGN

The CFE payload is comprised of the three main components: 1) payload RF log-periodic antennas, 2) 4 radio receivers and 3) payload processor.

The 4 log-periodic array (LPA) antennas include two crossed LPA antennas mounted on the nadir spacecraft deck and two single LPA antennas mounted to the 4m deployable booms provided as part of the spacecraft bus (Figure 1). The antennas were fabricated under contract to L'Garde, Inc with antenna design and engineering support provided by LANL. The antenna mast design was based upon the same inflatable mast structure that L'Garde designed and demonstrated on the ground for a NASA solar sail demonstration. Each antenna mast is comprised of a Kevlar fabric impregnated with a temperature sensitive, rigidizable resin that is deployed by inflation. Each antenna assembly weighed 2.1 kg and was approximately 16 x 16 x 6 cm in dimension when stowed. Inflated, each antenna was to be 2.4m in length. Unfortunately, only one of the three antenna masts inflated correctly, potentially due to the RF cable bundle being too tightly constrained interior to the antenna masts. The other two masts inflated about half way before they stalled and vented, leaving the antenna elements in a non-optimal orientation.

A. Payload Architecture

The architecture of the processing payload of CFE is shown in Figure 2. As seen in this figure, the CFE payload includes an R6000 microprocessor, spacecraft communications interface, a digitally controlled radio tuner, a two channel, 12- bit, 100 MHz analog to digital converter, three reconfigurable computing processors using Xilinx Virtex FPGAs, and nonvolatile memory to store program and FPGA configuration data.

The RAD6000 30 MHz microprocessor, a radiation hardened R6000 processor supplied by BAE, controls all of the payload digital modules and manages payload

communications with the vehicle. The processor includes 8 Mbytes of radiation-hardened SRAM and executes the VxWorks operating system. Although this processor and its associated SRAM are radiation-hardened, the processor architecture is almost two decades old and does not have the computational power necessary to perform continuous real-time on-board sensor processing.

intermediate frequency (IF) ADC inputs; this provides input from all four antennas simultaneously to the reconfigurable processors.

The analog IF is sampled at 100 MHz with 12-bit resolution. The outputs from the payload ADCs are distributed across a network of point-to-point 200Mbyte/sec (32 bit x 50 MHz) LVTTL buses derived from the Front Panel Data Port (FPDP) specification.

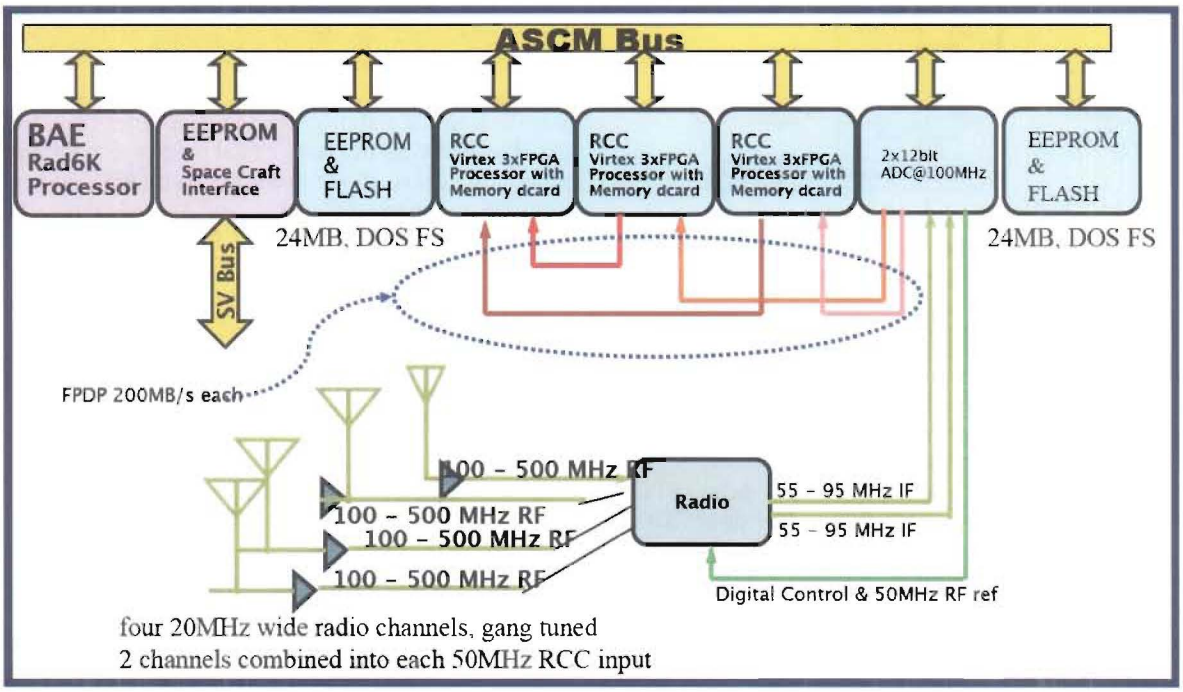

Figure 2: Architecture of the CFE reconfigurable processing instrument.

The payload uses both EEPROM and flash memory for nonvolatile storage. Three banks of 1 Mbyte of EEPROM are available to store the operating system and binary user code objects for the microprocessor. Two banks of flash memory (24 Mbytes each) store compressed configuration bitstreams used to configure the Xilinx Virtex devices. More than 20 uncompressed FPGA bitstream configurations can be stored in each flash memory module. Error control coding (ECC) is incorporated to mitigate SEUs that occur during read or write operations in the nonvolatile memory.

The RF VHF/UHF tuner was designed and built at Los Alamos. It includes four RF channels, each connected to a distinct LPA antenna, which can be "gang" tuned by microprocessor command between 100 and 500 MHz. This configuration is designed to make high fidelity interferometric measurements from a single lightning pulse. All four RF channels have an instantaneous bandwidth of 20 MHz. Two RF channels are combined into each of the 50 - 100 MHz ADC data cascades through the three reconfigurable computers. Two reconfigurable computers each receive one channel of ADC data for preliminary processing, while the third RCC combines the two intermediate results into a final measurement.

The processing payload was built around three reconfigurable computer (RCC) modules used to perform processing duties for a variety of experiments (see Figure 3). Each RCC module uses three Xilinx Virtex XQVR1000 CG560 FPGAs as the data processors. The FPGAs are organized in a ring and each has identical pin definitions so they may share configuration files. This design strategy reduces the amount of nonvolatile memory needed for FPGA configurations, reduces the required uplink bandwidth, and provides for greater reliability through redundancy. In addition, complex designs only need to be designed and verified once thus reducing design time on the ground. The nine FPGAs provide over 9 million system gates and over 1 Megabyte of block RAM memory.

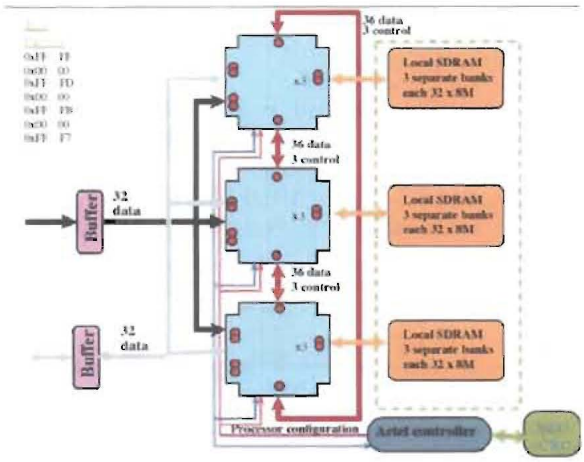

Figure 3: Architecture of the Virtex (the 3 blue blocks) based reconfigurable computer module.

Each Virtex FPGA has 3 banks of independent memory; each bank is comprised of four Hyundai 64 Mb SDRAMs organized as 8 M x 32-bit wide for a total of 288 Mbytes per module. Each RCC module also has microprocessor access through a radiation tolerant Actel RT54SX32S device that acts as a microprocessor interface and board controller. The Actel FPGA provides watchdog monitoring for the three Xilinx FPGAs as well as a configuration interface, which aids in CFE's FPGA SEU mitigation scheme. While the use of Virtex FPGAs in this system may seem old when compared to FPGAs available today, the Virtex 1000 FPGA family was the most complex and dense FPGA available when the CFE system was first conceived. Since all satellite systems go through an extensive design, qualification, and testing procedure, the components used on orbiting satellites typically lag far behind the components available commercially. Furthermore, the Xilinx Virtex FPGA was the first SRAM-based FPGA to go through extensive reliability evaluation for radiation environments [7].

One elegant feature of this reconfigurable architecture is its testability. In the design phase, the first 'experiment' completed was a built-in-test (BIT) application that configured the Virtex devices with a test suite that can test the processor ring bus, memory busses, module I/O, and the SEU mitigation circuit (discussed in the next section) for hardware faults. Each colored dot within the Virtex FPGAs in Figure 3 represents a stimulation or verification circuit for a subsystem interface. Fault coverage includes stuck-at faults, as well as signal integrity faults such as crosstalk and ground-bounce. The busses are all exercised at full rate simultaneously to generate worst case operating conditions. Further, software controllable circuits are incorporated that consume large amounts of power in order to stress test the power system. This BIT application was used extensively in development and verification on the ground, but was also the first experiment run on-orbit to verify successful operation.

B. SEU Mitigation

One of the biggest risks that must be addressed when using SRAM-based FPGAs in a satellite is radiation introduced SEUs in the device. The CFE team investigated and developed techniques at the system level and application level for providing reliable operation of the SRAM-based FPGAs. First, the RCC boards used the QPro Virtex radiation tolerant FPGAs [8]. These FPGAs use an epitaxial process that provides immunity against single event latch-up (SEL, an acute destructive failure) to an LET of 125 MeV/mg/cm2. The .25 micron process provides for approximately 100 K Rad(Si) total ionizing dose (a chronic and destructive radiation effect). These FPGAs are not, however, immune to SEUs within the user flip-flops, memories, and configuration data. To detect and repair SEUs within the configuration memory, the CFE system employs a form of configuration scrubbing [9].

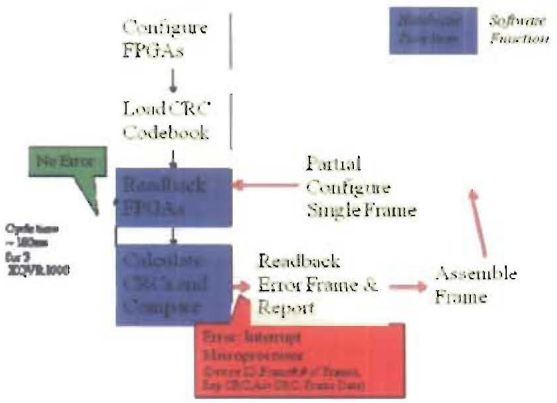

Figure 4: Configuration scrubbing design for detecting and repairing SEUs in the Xilinx Virtex.

Configuration scrubbing, shown in Figure 4, is accomplished at the system level with the use of the radiation tolerant fused-based Actel FPGA. This device detects configuration SEUs by continuously reading the bitstream on each FPGA device through configuration readback. A cyclic-redundancy check (CRC) is calculated "on-the-fly" for each frame of a configuration bitstream. This calculated CRC is compared against the codebook CRCs that are pre-calculated on the ground. When an upset is detected by a CRC mismatch, a microprocessor interrupt is generated causing a reconfiguration of the upset frame from the onboard flash memory. When an SEU is detected, the exact bit that is upset and a timestamp is inserted into the telemetry. The use of configuration

scrubbing prevents the accumulation of configuration upsets in order to significantly reduce the probability of having concurrent multiple configuration upsets.

In addition to configuration scrubbing, a variety of application-specific mitigation techniques have been developed for CFE. Specific techniques that have been applied include half-latch removal [10] and triple modular redundancy (TMR) [11], [12]. Half-latch removal involves the substitution of weak keeper circuits, which cannot be observed in the configuration bitstream, with logic structures for supply constant logic '1' and '0' values to the circuit. A tool for automatically applying TMR to a user design was also created [13]. This tool triplicates circuit resources and inserts majority voters to isolate any single upset caused by a configuration SEU. This tool provides the ability to "partially" mitigate user circuits when TMR proves too costly in hardware resources. These tools can be used on new FPGA architectures for future missions.

C. Managing Instrument Reconfiguration

Configuration of CFE from the ground offers an extremely flexible instrument for operating a variety of experiments. It also introduces complexity in the instrument, data transport, and data management at the ground station. To conduct each experiment, unique software runs on the RAD6000 microprocessor, unique configuration bitstreams are loaded into the Virtex FPGAs, unique SEU CRC codebooks are loaded into the SEU detection circuit, and unique telemetry packets are transmitted to the ground station which must be able to process the unique packets. This represents a large amount of complexity and can introduce risk. The risk can be tolerated on the instrument because the vehicle can reset or power cycle the instrument. Further, the instrument can boot directly from the vehicle mass memory if the internal nonvolatile memory is corrupted.

This complexity is managed by building flexibility into the entire system architecture: dynamic linking, dynamic command dictionaries, on-board storage of configurations, and hierarchical telemetry packet structures.

One unique feature of the software architecture is the ability to dynamically link object code while in orbit. This is an unusual feature for software designs operating in space, but it allows new software to be uploaded without reloading unchanged software components. The base operating system, command processors, and SOH tasks are linked together into a single image. Application specific code is uploaded and stored separately, then linked dynamically at execution time. This allows the uplink communications channel to be used efficiently by eliminating the need to upload unchanged software. This dynamic object linking also allows the processor RAM to be conserved by only linking code for the currently running experiment rather than linking code from all experiments.

The CFE software architecture also supports an unusual dynamic command dictionary. The command dictionary has approximately 75 static commands defined. This dictionary has a command that inserts (and removes) additional commands into a table that can support up to 1024 commands. This allows operators and designers to conceive of new experiments, upload the object code, FPGA configurations, and insert new commands in the dictionary to execute the new experiment. These features enhance reliability by preventing bugs from migrating into the operational codes during whole system rebuilds.

Each experiment is managed independently since the instrument does not support running multiple experiments concurrently. While it is possible to do so, no protection is built in to prevent contention at the FPGA or RAD6000 between the experiments. To keep the system manageable, the instrument is reset between each experiment. This establishes a 'clean' operating environment for each experiment and assures that no bugs migrate from one experiment to another. Further, this approach simplifies ground based analysis by grouping the data from an experiment into a single archive file. Data in transported in application specific packets. The packet design is hierarchical: the highest level has a fixed definition. Approximately 30 unique sub-packet definitions exist; each can have its own size, up to 2kbytes, and subfield definition. New application specific packets can be defined in the application code. Corresponding additions are needed for the analysis software in the ground segment.

Before deploying an experiment to the spacecraft, operation is verified on full fidelity engineering models of the instrument. This test-bed aids in verifying the correct deployment of the experiment, operations and telemetry collection, and correct analysis by the ground segment. Next, the experiment is characterized for its run-time parameters: SOH data production, science data production, peak energy consumption, average energy consumption, and total energy consumption. These attributes, along with mission objectives set by the science team, are used by the satellite operators for mission planning. The operators determine the sequence of experiments to be conducted given the anticipated energy available due to the solar Beta angle as well as the availability of memory in the data recorder.

D. State-of-Health Reporting

The CFE instrument, as a technology pathfinder, is extensively monitored. Regular monitoring of state of heath (SOH) parameters occurs at programmable intervals. The SOH data is organized into four tiers of information, labeled 0 to 3. These tasks run at priority levels above the experiment application priority. Each tier has an associated task running on the RAD6000 processor that gathers the information at the specified interval, which is set by command. Generally, the rate of reporting declines as one moves up the data hierarchy. Tier 0 is typically reported very 10 s and reports information related to the commands received, whether any commands were missing or corrupted, and the amount of data transmitted on the SOH and DATA links to the vehicle. A RAD6000 processor load factor is also reported.

The tier 1 task reports 24 temperatures (9 of which are diodes in the Virtex silicon), 13 currents, and 8 voltages. Tier 1, which typically cycles every 30 s, also performs a test against a table of limits that can be set by command. If any parameter exceeds the limits (upper or lower), the payload asserts a *panic* discrete signal to the space vehicle. The space vehicle has three responses that can be set by command: a hard instrument reset, power off the instrument, or no response.

The tier 2 task reports the hardware state throughout the instrument. Every register on each module is recorded and transmitted in the telemetry. The only exceptions are the registers in the processing FPGAs, since they change with every application, they are not reported from the SOH task. Instead, those are reported from within the application layer. This task typically cycles with a 1 min. interval.

Tier 3 reporting covers the operating system. The number and state of tasks is reported, and memory utilization is reported. The number and state of command processors is reported. If any task is in the suspended state, this task asserts the *panic* signal noted above. Also, this task is responsible for clearing the watchdog timer. If this task fails to clear the timer, a hardware circuit asserts the *panic* signal.

E. Thermal Management

A major design concern of CFE was the instrument and satellite's ability to adequately manage the heat generated by the FPGAs. While FPGAs are efficient in terms of watts/operation, absolute power consumption can be significant. Some CFE experiments require FPGA designs that consume more than 7 W in a single FPGA (~25W in a module, up to 155W peak in the instrument, 45W standby) which can be extreme for a space instrument in vacuum. Further, the orbit environment includes wide temperature fluctuations due to solar exposure and Earth shading. The variation in power consumption by various reconfigurable experiments and the wide thermal dynamics create thermal cycles that must be carefully managed.

Managing the frequency and depth of these thermal cycles is critical for two reasons. First, timing performance of the FPGA design is governed to a maximum temperature limit. For a high reliability design like a space instrument, the manufacturer de-rates the timing estimation in order to guarantee performance at high temperature (125C). By effectively designing the thermal system and managing operations to keep temperature below 70 Celsius, the devices can be used as though they are the fastest speed grade.

Second, thermal cycling is a primary contributor to instrument wear and eventual failure. Due to unavoidable, small mismatches in various material coefficients of thermal expansion (CTE) each thermal cycle introduces stress on the mechanical assembly. The stress on the package becomes more severe as the temperature cycle depth becomes more extreme. The most important mechanical interface for CFE is the printed circuit board to FPGA package interface. Due to the large package size (42x42mm), the stress on corner pins is the primary mechanical failure point. Two strategies were employed to minimize these thermal risks. First, an exotic printed circuit board material, Thermount, was used that more closely matched the thermal properties of the FPGA package and hence reduces CTE mismatch.

In addition, a system of heat pipes is used to transport heat from the FPGAs to the spacecraft radiators to limit maximum temperatures. The heat pipes, shown in Figure 5, are passive and particularly well suited for this application. Found in commodity personal computers, heat pipes use a working fluid, typically water that goes through phase changes, in order to transport large amounts of heat very efficiently. The heat pipes employed in CFE can transport more than 5W with less than 1 degree Celsius temperature drop across the pipe. The heat pipes use capillary action for fluid flow so that they operate in the absence of gravity. Also, when cold, the working fluid freezes and the pipe switches "off". The fluid is at low pressure and does not fill the pipe, so freezing does not cause damage. This feature allows the pipe to perform like a passive thermostat by only conducting heat when above the turn-on temperature; this reduces cold extremes in the temperature cycles.

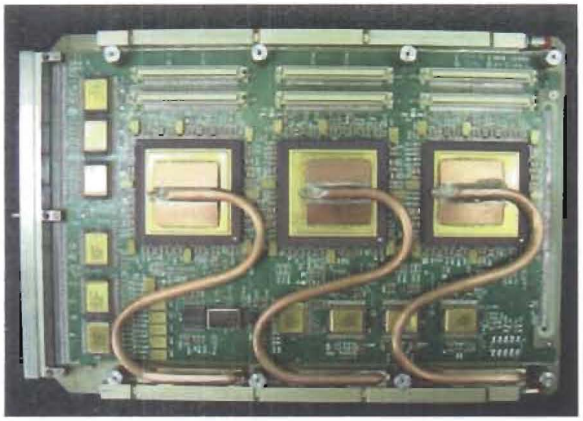

Figure 5: Reconfigurable computer with heat pipes.

Another important consideration on CFE is energy management. All power on the spacecraft is generated from solar panels and stored in Lithium-Ion batteries. The power available to the payload is limited by the energy generation from these panels and that stored in the batteries. The FPGA configurations must be carefully scheduled to insure that the FPGA power consumption does not exceed the energy production for extended periods. These operational cycles result in discharge cycles on the spacecraft batteries and represent the primary wear mechanism of the entire satellite. Similar to the thermal cycling mentioned above, the battery lifetime is determined by the number and depth of charge/discharge cycles, as well as the operating temperature. Ideally, the battery must be kept between 0 and 20 Celsius, the nearer 20C the better.

Due to the configurability of the CFE payload, energy consumption is extraordinarily variable. Because many experiments use more than the average energy available, the payload is put into standby or switched off entirely to comply with the energy budget. High-throughput, high-power applications are mixed with other low-power experiments to keep the average energy consumption within an acceptable range. Power intensive designs run when more energy is available, while lower power applications run when constraints dictate. The highly dynamic power profile contributes to the thermal cycling and stresses the thermal management system.

IV. CFE LAUNCH AND ON-ORBIT RESULTS

The SSTL satellite bus was delivered from the UK to LANL on May 31st, 2006. Integration of the LANL payload occurred on June 15th, 2006 (Figure 6). Following the fully integrated functional and environmental testing, CFE was shipped to Cape Canaveral for integration to the STP-1 mission satellite stack. CFE was one of four satellites mated to the EELV secondary payload adapter (ESPA) ring (Figure 7) and one of six satellites launched. CFE was launched into a circular low-earth orbit (560 km, 35.4 degrees inclined) on March 8, 2007 (March 9 UTC) aboard a

Figure 6: Integration of the LANL payload and the SSTL satellite bus, June 15th, 2006.

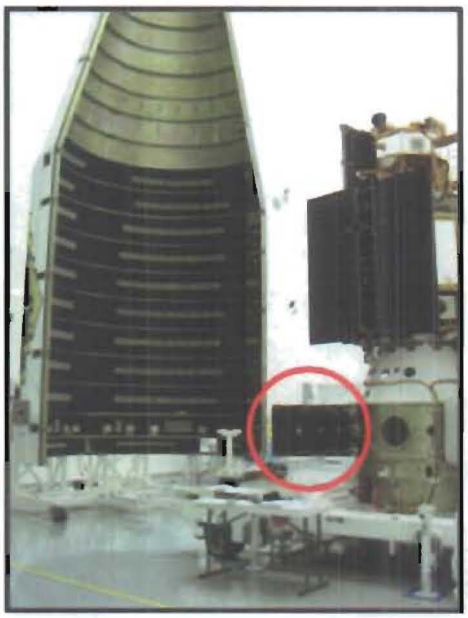

Figure 7: CFE mated to the STP1 ESPA ring.

Lockheed Atlas-5 Medium rocket (STP1 shown in Figure 8) [1]. Ground station connectivity was established quickly after the launch, and communication with the satellite has been consistent over more than two years of flight time.

Figure 8: STP-1 Atlas 5 Medium launch on March 8, 2007.

Since its launch, CFE has received configuration data from the ground more than three dozen times, both refining and increasing the portfolio of experiments within the reconfigurable payload. Over 30,000 experiments have been performed, where an experiment is the configuration of one or more Virtex devices and collection of data that is transmitted to the ground. This section will summarize the operation of the CFE payload in space, including power and thermal performance, SEU rates, and design applications.

A. SEU Rate

Several studies were performed to estimate the upset rate of the FPGAs in the 560 km low-earth orbit [14], [15]. These estimates were made using the CREME96 modeling environment and results from radiation testing on Xilinx Virtex devices [7]. The estimated SEU upset rates for the Virtex in this low-earth orbit are summarized in Figure 9. The estimated SEU rate varies from 0.5 SEUs per device day (solar max, best case estimate) to 26 SEUs per device day (solar minimum, peak trapped protons). All SEUs within the device have been logged during the CFE lifetime to measure the actual SEU rates of the system. Through configuration scrubbing, 849 SEUs have been detected over 3160 device days resulting in an average upset rage of .268 upsets per device day. The SEU upset rate is lower than the best case estimate and much lower than any worst-case conditions. With nine FPGAs in the payload, CFE averages 2.4 SEUs per day of operation.

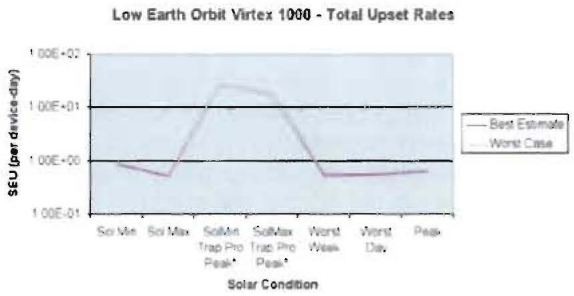

Figure 9: Forecast CFE SEU rate for a variety of scenarios, CREME96.

The SEUs do not occur uniformly as the spacecraft orbits the earth. Figure 10 shows the SEU rate for CFE broken down into latitude and longitude tiles. As expected, the vast majority of SEUs occur in the South Atlantic Anomaly (SAA). This is the region where the Van Allen radiation belt passes closest to the Earth's surface due to irregularities in the Earth's magnetic field.

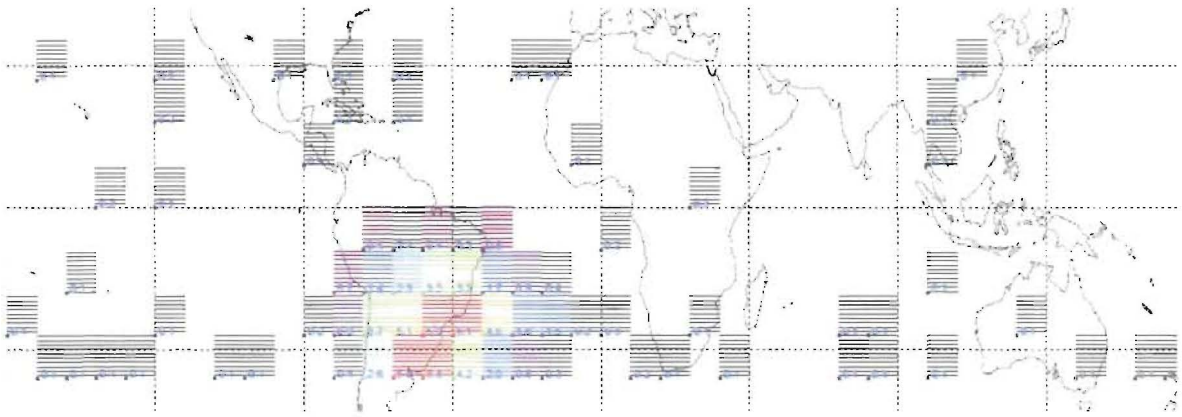

Figure 10: SEUs per device day in 9° latitude / longitude tiles.

Another approach to understanding SEU impact is to examine the time between their occurrences. This determines if upsets occur in 'flurries' or if perhaps multiple upsets are occurring due to a single ionizing particle. Figure 11 illustrates the time between SEUs. Note the regular peaks as the spacecraft passes through the SAA. The peaks are not perfectly periodic from orbit to orbit because the SAA is not exactly symmetric relative to the CFE orbit. The 24 hour peaks are close but not exactly periodic due to precession of the orbit.

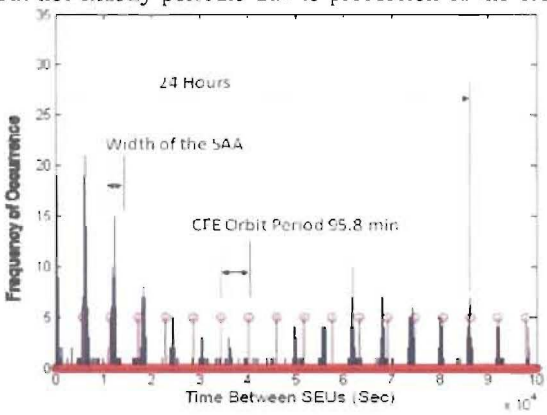

Figure 11: Histogram of the time interval between SEUs. Note the peaks as CFE passes through the SAA.

The width of the peaks represent the time duration for the spacecraft to pass through the SAA region. Not visible in the plot are 3 events that are apparent multiple bit upsets (MBUs) from a single ion. On three occasions, two upsets were detected in the same device in adjacent frames at the same time, which strongly suggests they relate to the same event. The rate at which these MBUs occur, and their severity, influences the reliability of redundancy techniques employed to enhance reliability. An underlying assumption for many approaches, including the popular TMR, is that only one fault is present in the FPGA at any instant. It is assumed that scrubbing will be fast enough to repair a fault before another occurs. On extremely rare occasions, MBUs may introduce errors even in circuits protected by TMR.

B. Signal Processing Experiments

Several CFE signal processing payload experiments have been uploaded to reconfigurable platform and executed on the FPGAs. These signal processing experiments interface directly to the on-board ADC to process sampled data from the satellite antennae. Examples of this class of circuits that have been run on the satellite include several software defined radios (SDR), demodulators, decoders, and high-throughput FFT engines that exceeded a sustained computation rate of 10 Gops per second. The performance of the payload is two to three orders of magnitude better than what can be expected from *currently available* radiation hardened microprocessors.

One signal processing experiment is a 500 kbps QPSK receiver implemented on a single FPGA of the CFE reconfigurable computer (see Figure 12). The purpose of this experiment was to demonstrate a practical communications application using CFE's radio receiver and computing hardware. The experiment was successfully deployed and tested on-orbit in November 2008. A 500-kbps link was established between a transmitting ground station and CFE, with error free communication during the majority of the pass.

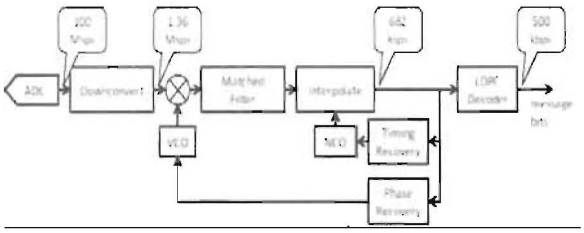

Figure 12: One example CFE application, a 500 kbps QPSK demodulator and LDPC decoder.

The spectrum of the transmitted signal can be seen, along with substantial interference, in Figure 14. The receiver timing offset, frequency offset, and automatic gain control (AGC) are also shown. Figure 13 shows the constellation diagram collected on-orbit. This experiment demonstrates the performance and flexibility that reconfigurable processing can offer.

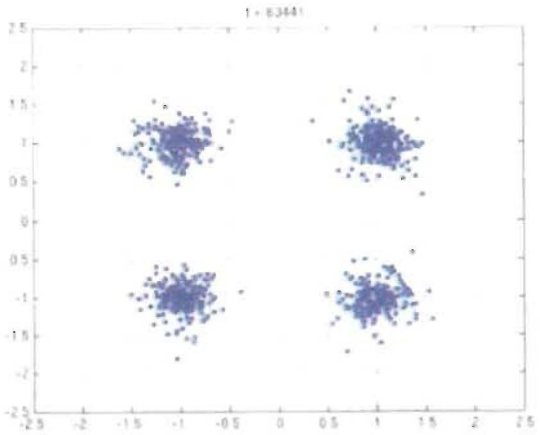

Figure 13: Constellation diagram of the QPSK signal received on CFE.

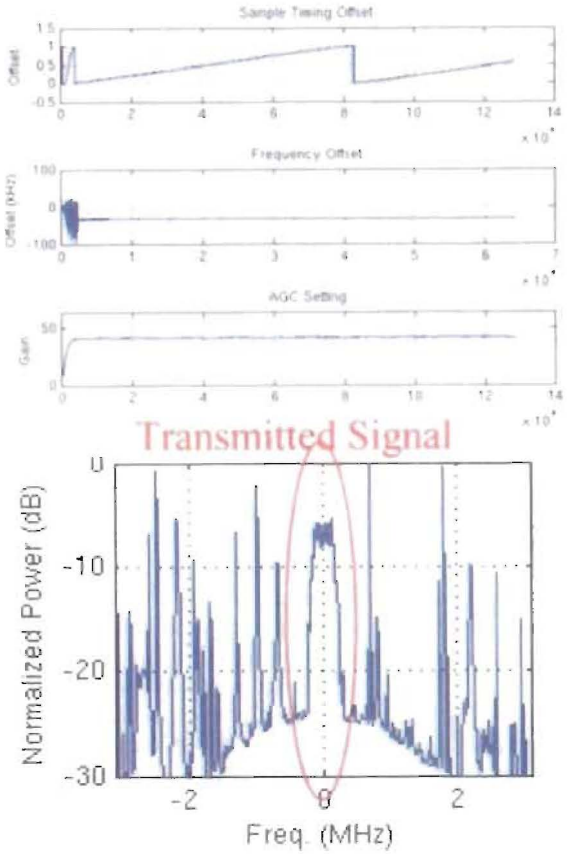

Figure 14: Spectrum of transmitted QPSK signal along with the timing, frequency, and automatic gain tracking output from the demodulator.

C. State-of-Health

Reviewing the state-of-health telemetry from the payload is helpful for evaluating the effectiveness of the overall design. To appreciate the dynamic operating environment experience by the payload, consider Figure 15. It shows the daily and accumulated number of power cycles and experiments (FPGA configuration cycles) executed on the payload. The payload has undergone more than 4000 power cycles. This is, in part, due to the concept of operations early in the program during commissioning, but mostly due to overall system energy management.

The dynamics can be more fully appreciated by examining the current consumption on one of the reconfigurable processor modules, as shown in Figure 16. This plot illustrates the consumption for *just* the 2.5 V supply, not the 3.3 or 5.0 V supplies on a *single* module. The maximum peaks in current consumption correspond to different experiments that

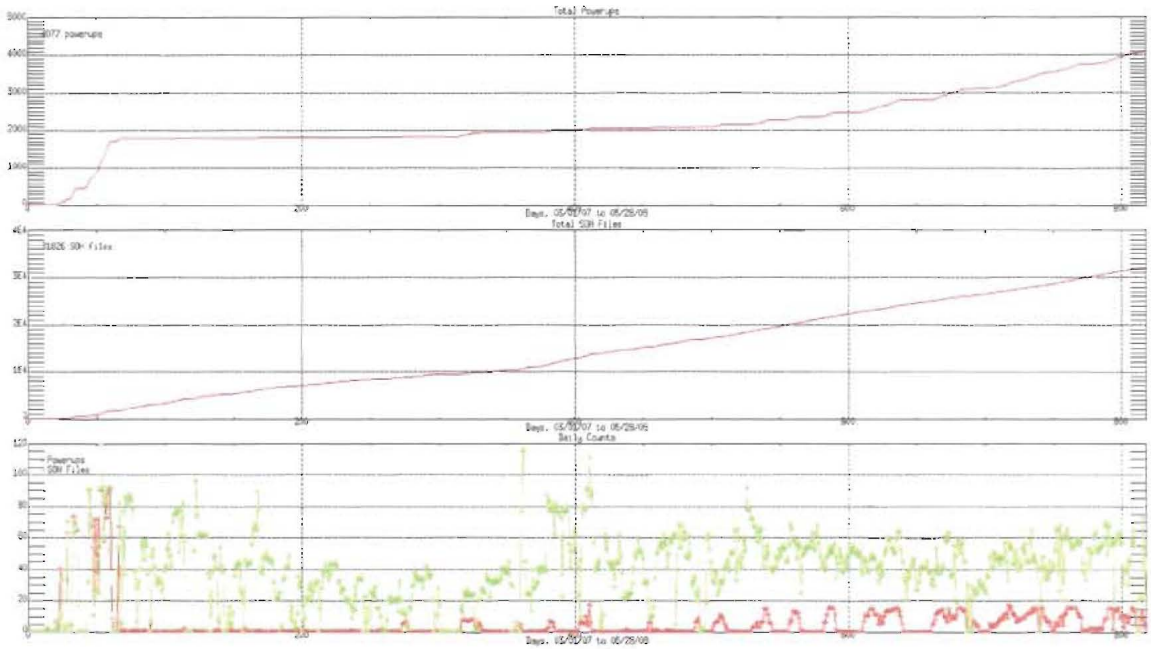

Figure 15: Cumulative and daily payload power cycles and experiments conducted (represented by SOH files). Top plot: accumulated power cycles. Mid plot: accumulated experiments. Bottom: Green is daily number of experiments conducted; red is daily number of power cycles.

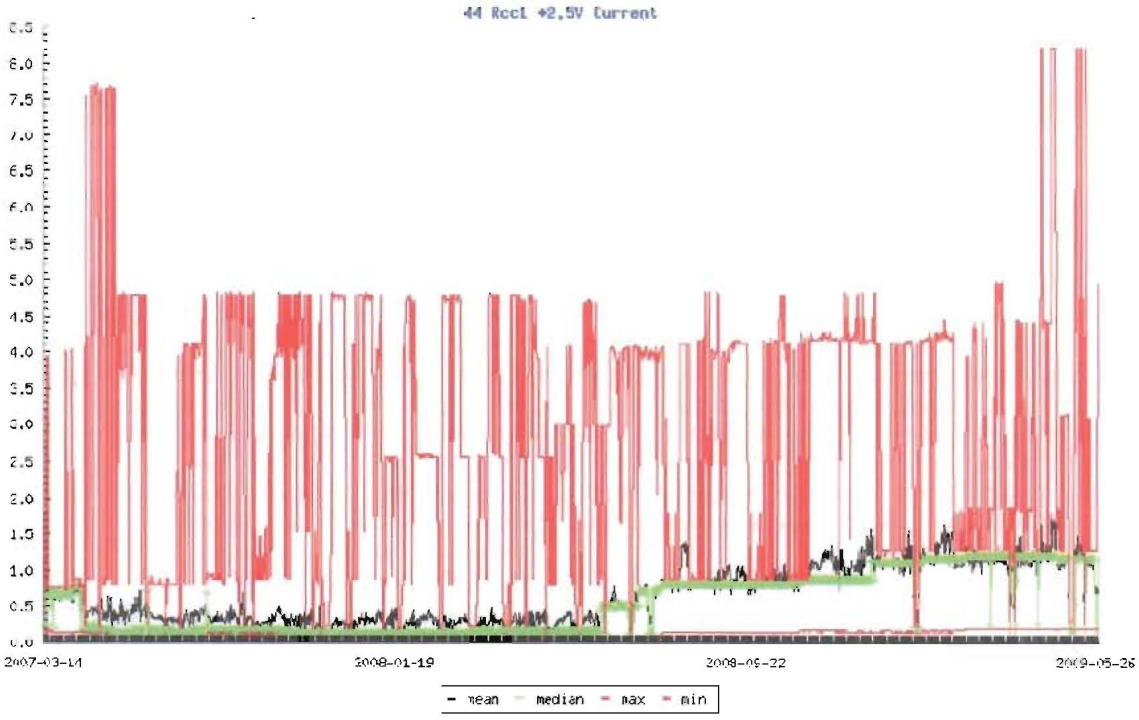

Figure 16: Daily mean (black), median (green) and max and min (red) amperage source from the 2.5V supply and consumed on reconfigurable processor module 1. Note the extreme dynamics and the implications for thermal management.

are executed on the platform. These experiments, however, are not run for long periods of time as there is not sufficient energy to sustain them. (Note the relatively low mean current consumption.) Extreme dynamics in power consumption mean extreme dynamics must be managed thermally as well. Figure 17 displays the die temperature history of one of the FPGAs to demonstrate the temperature fluctuations experienced by the reconfigurable computing boards. While the median temperature of the die is kept within a reasonable operating regime (between 5C and 25C), the minimum and maximum measured temperatures are wider, between -5C and 35C. The relatively benign temperature swings maintain the reliability of the mechanical assembly as well as allow the use of these FPGAs as the 'highest' speed grade devices, making algorithm design much easier.

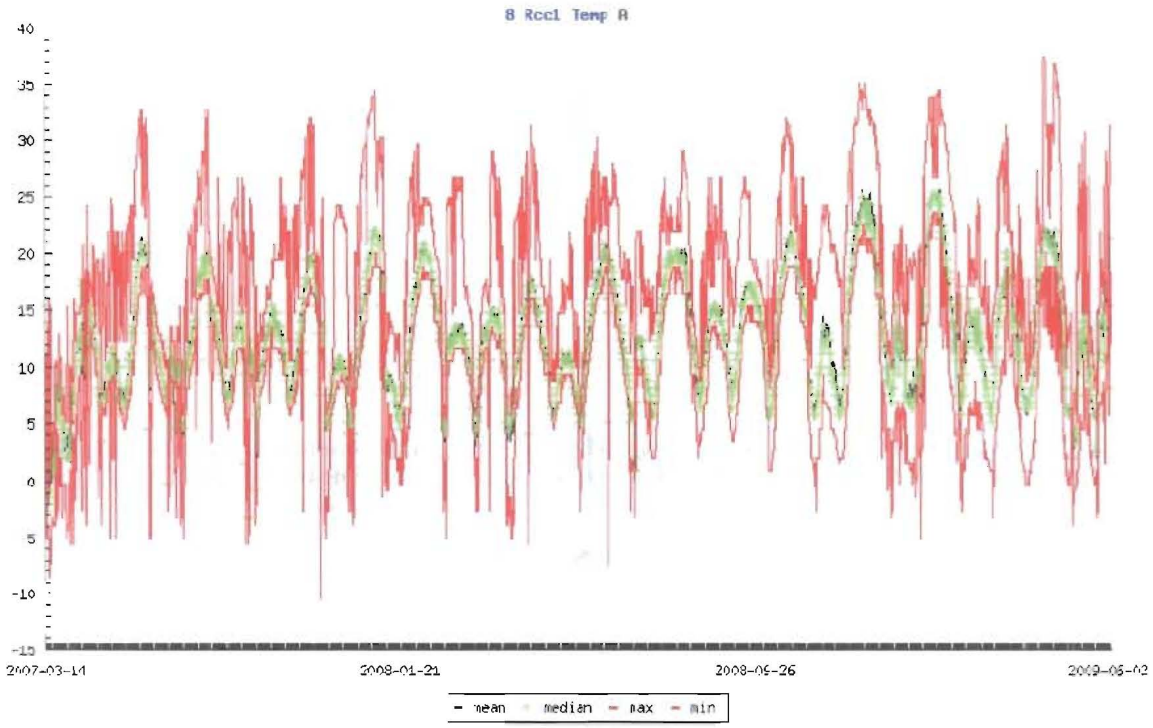

Figure 17: Die temperature profile for FPGA A on module 1 (C) vs. days in orbit.

V. CONCLUSIONS

The reconfigurable computing architecture within CFE has performed very well and continues to be used for a number of reconfigurable computing experiments. Future experiments include real-time SEU mitigation tests, lightning and ionosphere studies, communications experiments, and other signal processing tests.

The RCC modules within the CFE and the SEU mitigation approach used to protect them have proven successful. Several useful design techniques are worth mentioning. A symmetric layout was used for all FPGAs allowing the same bitstream to be used for any FPGA. This symmetric layout was helpful in simplifying the design and reuse of bitstreams across the platform. The dynamic command dictionary and on-orbit run-time linking was very effective for allowing run-time scheduling and uploading of new FPGA bit streams and the SEU scrubber design worked flawlessly. While the Xilinx Virtex FPGAs have worked very well for this experiment, newer FPGA architectures will have a big impact on computational density and power. Specifically, the DSP48 primitives found in Virtex II and successor FPGAs would significantly reduce the size and power of the signal processing circuits used in this system. Also, the high speed serial I/O found on current generation FPGAs would significantly reduce the number of I/O pins needed for inter-FPGA communication. Even more importantly, a high speed serial network incorporating a runtime reconfigurable cross-point switch would allow the network topology to change for each application. This increased flexibility would allow the FPGAs to be used more efficiently than a hardwired network

topology. This approach also increases the robustness of the system by allowing degraded or failed components to be gracefully removed from the system. A number of FPGA architectures succeeding the Virtex have been qualified for space operation and can be used on future missions. CFESat, as a technology pathfinder, has effectively demonstrated the importance of high-performance reconfigurable computing.

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