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Production and performance of the silicon sensor and custom readout electronics for the PHENIX FVTX Tracker

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Abstract

The Forward Silicon Vertex Tracker (FVTX) upgrade for the PHENIX detector at RHIC will extend the vertex capability of the central PHENIX Silicon Vertex Tracker (VTX). The FVTX is designed with adequate spatial resolution to separate decay muons coming from the relatively long-lived heavy quark mesons (Charm and Beauty), from prompt particles and the longer-lived pion and kaon decays that originate at the primary collision vertex. These heavy quarks can be used to probe the high density medium that is formed in Au+Au collisions at RHIC. The FVTX is designed as two endcaps. Each endcap is comprised of four silicon disks covering opening angles from 10 to 35 degrees to match the existing muon arm acceptance. Each disk consists of p-on-n, silicon wedges, with ac-coupled mini-strips on 75μm radial pitch and projective length in the phi direction that increases with radius. A custom front-end chip, the FPHX, has been designed for the FVTX. The chip combines fast trigger capability with data push architecture in a low power design.

Keywords: Silicon Microstrip, Silicon Vertex Tracker, CMOS ASIC, Heavy Quarks, Quark Gluon Plasma

1. Introduction

The PHENIX Experiment (**P**ioneering **H**igh **E**nergy **N**uclear **I**nteraction e**X**periment) has been collecting data at the Relativistic Heavy Ion Collider at Brookhaven National Laboratory since the year 2000. The experiment is designed to study high energy collisions of heavy ions and protons. One of the most exciting areas of research at RHIC is centered on the discovery and exploration of the properties of the Quark-Gluon-Plasma created in central Au+Au collisions at center of mass energy, $\sqrt{s} = 200$ GeV. The Forward Silicon Vertex Tracker (FVTX) is designed to enhance the capability of the PHENIX experiment to explore the characteristics of this dense plasma. The detector will also be a key element in the proton spin investigations [1].

The FVTX will extend the vertex capability of the central barrel, the PHENIX Silicon Vertex Tracker (VTX), to forward and backward rapidity, (η). The FVTX will also extend the reach in the low momentum-fraction region, (x). The detector is designed with adequate spatial resolution to separate decay muons coming from the relatively long-lived heavy quark mesons (Charm and Beauty), from prompt particles and the longer-lived pion and kaon decays that originate at the primary collision vertex. The heavy quarks, which are created during the formation of the plasma, can be used, through their decay products, to probe the high density medium that is formed in Au+Au collisions at RHIC.

2. The FVTX Tracker

The FVTX is designed as two endcaps to be installed on either end of the PHENIX barrel tracker. Each endcap is comprised of four silicon disks covering opening angles from 10 to 35 degrees to match the

existing muon arm acceptance. An exploded view of half of one arm of the tracker is shown in Fig. 1. A disk is comprised of 48 silicon wedges, each of which covers 7.5 degrees of acceptance. A wedge consists of p-on-n silicon sensors, 320 μm thick, with ac-coupled mini-strips implanted on 75μm radial pitch and projective length in the phi direction that increases with radius. The strips vary from 3.5 mm in length at the inner radius to 11.5 mm in length at the outermost radius. The sensor is divided into two independently read-out halves that each cover 3.75 degrees. There is a physical gap that runs down the centerline of the sensor that separates the left-hand and the right-hand strips. The total number of instrumented strips in the FVTX is just over 1.1 million. The sensors have been fabricated in prototype quantity by Hamamatsu Corporation. We have qualified the prototype sensors on a probe test station, and they meet all our quality acceptance criteria. A sensor in an assembly jig is shown in Fig. 2.

3. The FPHX readout chip

A custom 128 channel front-end chip, the FPHX, has been designed for the FVTX. The chip was optimized for fast trigger capability, a trigger-less data push architecture, and low power consumption. The chip has been fabricated in prototype quantity in the TSMC (Taiwan Semiconductor Manufacturing Company) 0.25 μm CMOS technology. The analog section consists of an integrator/shaper stage followed by a three bit ADC. Many of the setup parameters of the front end are programmable via a LVDS serial slow controls line pair. Adjustable parameters include gain, threshold, rise and fall time, input transistor bias current, channel mask, plus several additional fine tuning parameters. Nominal setup parameters include integrator/shaper gain of 100 mV/fC, > 800 mV dynamic range, 60 ns rise time at the shaper output, and 2000 electron threshold at the first comparator. All analog functions were exercised on a test stand and the measured values are very close to pre-submission simulation and specification. One exception is the threshold dispersion across the 128 channel chip, which is wider than anticipated at approximately 250 e's. Changes have been incorporated to increase the size of the integrator and shaper to try to reduce the dispersion in the next prototype round of chips. The average noise at the shaper output is measured to be 400 to 500 e's depending on input capacitance.

The FPHX operates in a data push format. It has been designed to process up to four hits within one RHIC beam crossing, or 106 ns. A fully processed hit pattern is zero-suppressed, contains a 7-bit time stamp, 7-bit channel id, and a 3-bit ADC value. The data word is output over two LVDS serial lines at up to 200 MHz clock rate. The total power consumption of the FPHX is 390 μW per channel.

An FVTX wedge assembly, consisting of a high density interconnect board, a silicon sensor and 13 FPHX chips, was assembled and wire bonded. The noise response across 13 chips is shown in Fig. 3. The decreasing noise as a function a function of chip id is indicative of the decreasing strip length on the sensor. All the design functions of the FPHX have been demonstrated successfully and the chip appears to operate in a stable fashion under a variety of setup conditions.

References

[1] M.L. Brooks et. al., Technical Design Report of the Forward Silicon Vertex, Brookhaven National Laboratory, June 27, 2007.

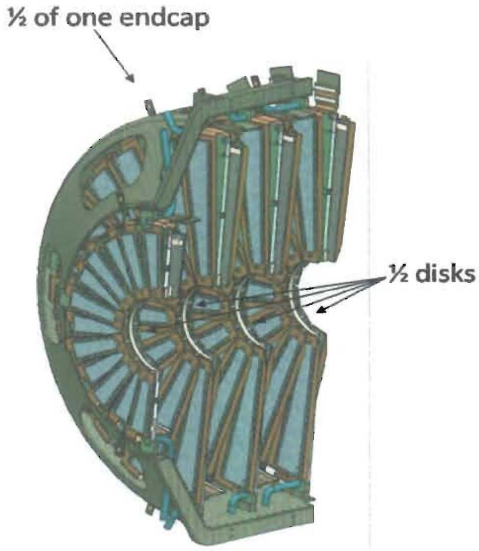

Fig. 1 Exploded view of one quarter of the FVTX.

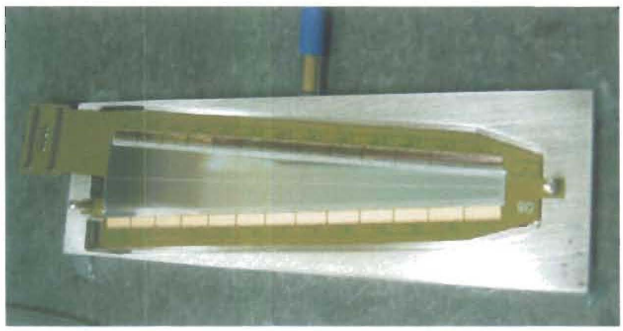

Fig. 2 FVTX wedge assembly with sensor and 13 FPHX chips.

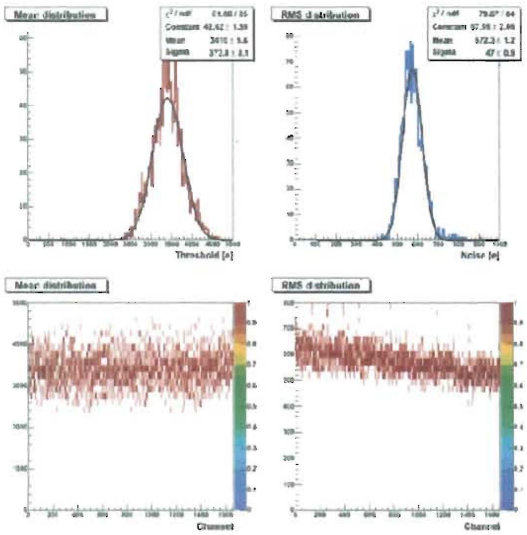

Fig. 3 Preliminary measure of the threshold dispersion and noise across 13 chips.