Printability and inspectability of programmed pit defects on the masks in EUV lithography

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ABSTRACT

Printability and inspectability of phase defects in EUVL mask originated from substrate pit were investigated. For this purpose, PDMs with programmed pits on substrate were fabricated using different ML sources from several suppliers. Simulations with 32-nm HP L/S show that substrate pits with below ~20 nm in depth would not be printed on the wafer if they could be smoothed by ML process down to ~1 nm in depth on ML surface. Through the investigation of inspectability for programmed pits, minimum pit sizes detected by KLA6xx, AIT, and M7360 depend on ML smoothing performance. Furthermore, printability results for pit defects also correlate with smoothed pit sizes. AIT results for patterned mask with 32-nm HP L/S represents that minimum printable size of pits could be ~28.3 nm of SEVD. In addition, printability of pits became more printable as defocus moves to (-) directions. Consequently, printability of phase defects strongly depends on their locations with respect to those of absorber patterns. This indicates that defect compensation by pattern shift could be a key technique to realize zero printable phase defects in EUVL masks.

Keywords: EUVL, mask, phase, defect, pit, printability, inspectability, S-Litho

1. INTRODUCTION

Extreme ultraviolet lithography (EUVL) is the most leading lithography technology for high volume manufacturing (HVM) of sub-30-nm node devices [1-3]. In addition to EUV source and resist issues, preparation of defect-free mask is one of the top critical concerns for the launch of EUVL into HVM. To achieve this goal, we need to minimize defect generation during blank preparation and mask process and then remove or compensate printable defects by repair and modification of pattern design. However, introduction of mask inspection and defect review infrastructure on time is still uncertain. Hence, study to define practical printability of mask defects is very essential in EUVL. Compared with amplitude defects located in absorber and patterns, printability of phase defects originated from substrate and ML in EUVL blanks is hard to be estimated since they may not be visible on the mask and not repairable [4-6]. The printability of phase defects depends on defect type, size, location, ML process, etc.

From the defect pareto of ML blanks from commercial suppliers shown in Fig. 1, 70-80% of blank defects are originated from the substrate. Accordingly, substrate defects including pit and bumps (particle) are the most dominant defects in EUV blanks. By the way, two suppliers show distinctive distribution of defect types, one is bump dominant and the other is pit dominant. Dominant defect types could be determined by polishing techniques and ML deposition conditions. In the previous work, we reported that smoothing performance of substrate defects by ML depends on deposition conditions and it results in discrepancies on the defect printability at EUV and inspectability at DUV [7].

In this paper, we investigate the printability and inspectability of phase defects, especially originated from substrate pits. Theoretically, pit and bump on ML blank with ~3 nm in height or depth could be a source of phase defect in EUVL mask since it corresponds to the dimension of out-of-phase condition (3.36 nm) as shown in Fig. 2. This value is much smaller than that of optical binary mask used in ArF lithography (175 nm). Therefore, quantity and size of substrate defects should be controlled more tightly in EUVL. For comparative study for programmed pit defects on various situations, we fabricated four programmed defect mask (PDM) using different ML sources from different suppliers.

KLA6xx, AIT, M7360, as well as simulations are used to evaluate printability and inspectability of programmed pits.

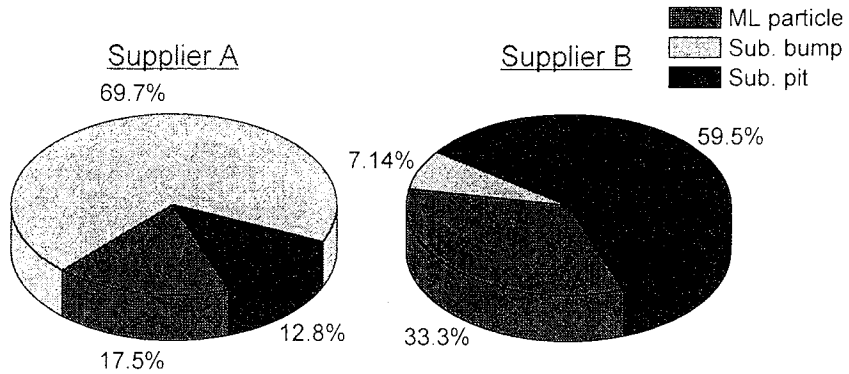

Fig. 1. Defect pareto of ML blanks from two suppliers.

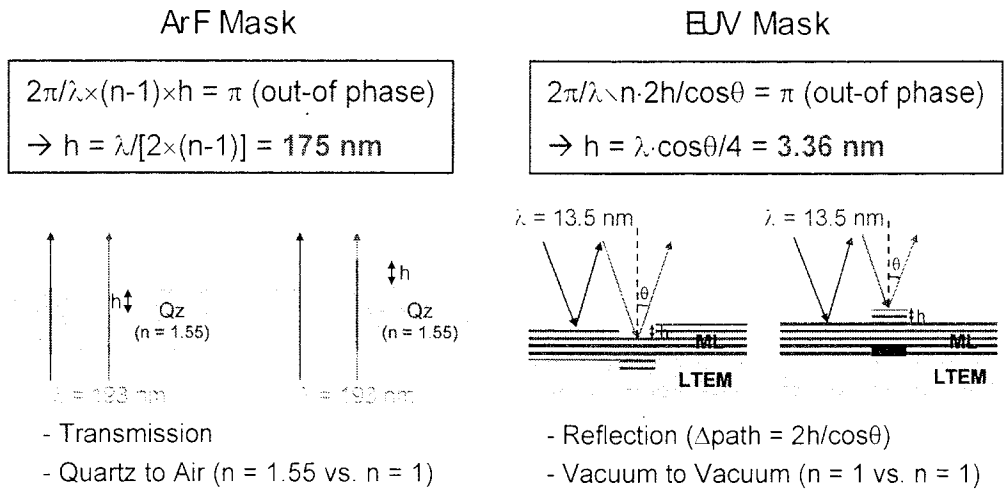

Fig. 2. Phase effects depending on defect size.

2. EXPERIMENTAL PROCEDURE

For the defect printability simulation for substrate pits, we adopted Sentaurus-Lithography (S-Litho) EUV software, which is capable of waveguide algorithm, a kind of rigorous coupled wave analysis (RCWA) method. Basically, exposure conditions of ASML pre-production tool (PPT), a numerical aperture (NA) of 0.25, a degree of coherence (σ) of 0.8, and an incident angle (θ) of 6° with a 4x system, were applied in the simulations [8]. The optical constants, i.e., the refractive index n and the extinction coefficient k, are obtained from the measurement of samples from blank suppliers at the Advanced Light Source (ALS) BL 6.3.2 at Lawrence Berkeley National Laboratory (LBNL). For calculating reliable printability results, SEVR59 resist parameters from Synopsys and IMEC were used for simulating resist image [9]. In the simulation models for propagating ML distortion by pits, it is assumed that substrate pits became locally distorted with inverse Gaussian-shaped profile in three-dimensional geometry.

In order to evaluate programmed pits on the substrate, we designed inspection-friendly layouts consisting of unit cells with different sizes of pit array. In Fig. 3, each unit cell includes 20 programmed pits with different sizes from 10 to 200 nm. Four masks (Mask A, B, C, and D) with programmed substrate pits using different ML sources (MLs from supplier A and B, SEMATECH, and Samsung) were fabricated and used for defect printability study (Table. 1). The four programmed defect masks (PDMs) could be expected to have different printability and inspectability for programmed

pits due to their different smoothing efficiency resulted from each ML deposition technique. Original pit depth on the substrate was ~16 nm for Mask A, C, and D and ~5 nm for Mask B. For printability and inspectability study, actinic inspection tool (AIT) in LBNL was used to evaluate printing images of pits on ML as well as on patterned masks. AFM is also utilized to measure real pit sizes before and after ML depositions. In addition, M7360 in SEMATECH and Teron6xx in KLA-Tencor were used to compare inspection capability for programmed pits on ML blanks. Table 1 summarizes status of inspection activities and some items are still in progress. In this paper, we will show inspection results which have finished and compare the results of 4 PDMs.

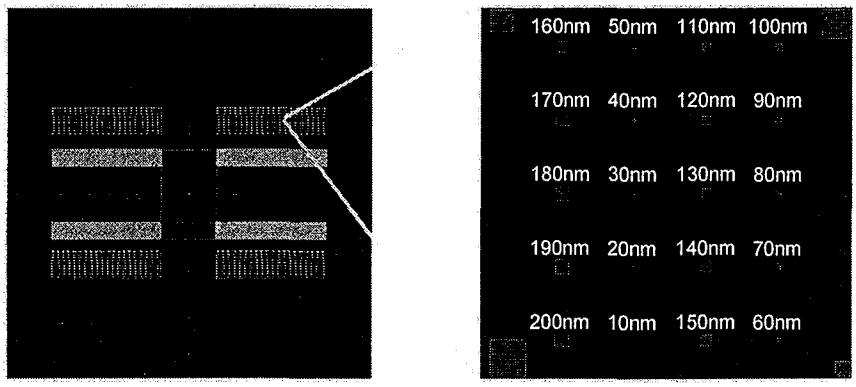

Fig. 3. Layout design for programmed pit defects.

Table 1. Mask types for analyzing programmed pit defects.

Type	ML deposition	Original pit depth	ML				Pattern		
			AFM	M7360	AIT	KLA6xx	AIT	Insp. (257/193)	ADT
Mask A	Supplier A	~16 nm	Done	N/A	Done	Done	TBD	TBD	TBD
Mask B	Supplier B	~ 5 nm	Done	Done	Done	Done	TBD	TBD	TBD
Mask C	SEMATECH	~ 16 nm	Done	Done	Done	Done	TBD	TBD	TBD
Mask D	Samsung	~ 16 nm	Done	Done	Done	N/A	Done	TBD	TBD

3. RESULTS AND DISCUSSION

3.1. Pit smoothing performances by ML deposition

In the ML deposition process, the degree of smoothing for programmed pits was governed by incidence angles of deposition on the substrate [7]. Two PDM samples applying different incidence angles, which are normal incidence (θ = 0°, A) and tilted incidence conditions (θ = 55°, B), are prepared as shown in Fig. 4. Schematics of ion beam sputtering tools visually show different paths of sputtered atoms on the substrate with different deposition angles. As a result, AFM results of width (approximated by using full width half maximum, FWHM) and depth for corresponding samples show that two PDMs have different smoothing trends compared to original sizes before deposition. Consequently, ML deposition with tilted incidence angle exhibits better smoothing efficiency on pit defects.

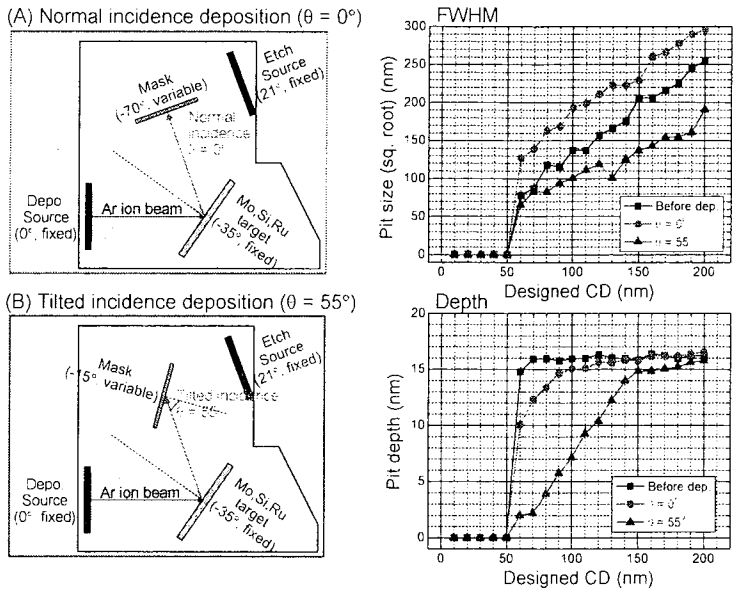

Fig. 4. Schematics of ion beam sputtering tools and AFM analysis results for programmed pit defects

3.2. Simulations: effects of ML smoothing

In order to predict minimum size of printable pit defects on 32-nm HP L/S patterns, various models with different depth of programmed pits (each model has a different smoothing efficiency) were quantitatively analyzed as function of pit depths on either ML surface or substrate (Fig. 5). In this simulation scheme, widths of pits are fixed at 50nm as a FWHM value. All pits were located at central position in space area between absorber patterns. According to the simulation results with resist images, pits with < 20 nm in depth on substrate would not be printed on the wafer if they could be smoothed by < 1 nm in depth on ML surface, with a ±10 % tolerance from the target CD in L/S patterns.

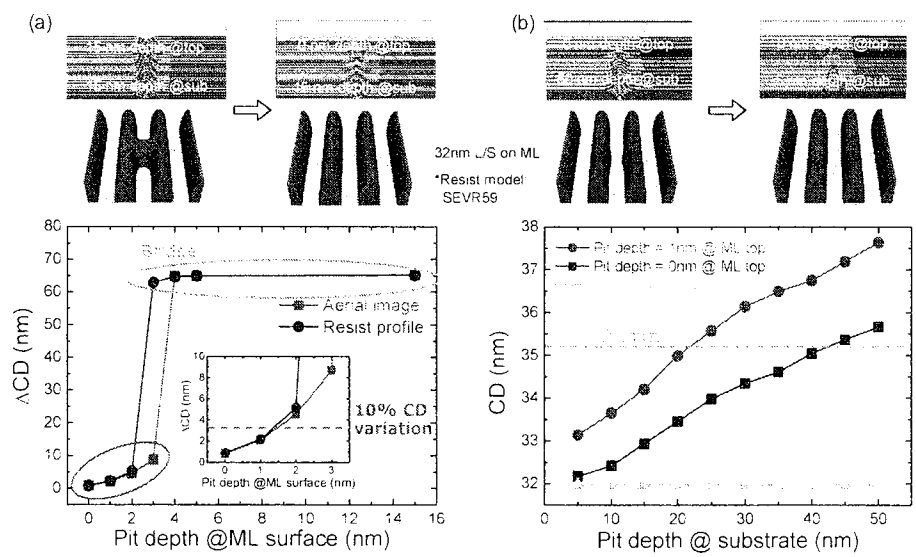

Fig. 5. Simulation models for pit smoothing and CD variations on the 32-nm HP according to corresponding pit sizes.

3.3. AFM analysis: pit depth and width after ML deposition

In the previous section, it concluded that incidence angle of deposited atoms is one of the critical factors which affect ML smoothing performance. To compare smoothing efficiencies for four PDM samples in Table 1, depths and widths of programmed pits on ML surface were measured by AFM. From measured depths and widths, the pit size can be converted to spherical equivalent volume diameter (SEVD) by using Gaussian defect scheme as follows:

$$(SEVD)_{Gaussian} = 2\left(\frac{3h_0(FWHM)^2}{16\ln(2)}\right)^{\frac{1}{3}}$$

$$pit\ depth = h_0$$

$$pit\ width = FWHM$$

All measured data from AFM were plotted as a function of designed pit size in Fig 6. Comparing SEVD values of four PDM samples, it was revealed that each PDM after ML deposition shows different smoothing efficiency depending on deposition condition. As a result, mask A exhibits the best smoothing efficiency on pits compared to other masks. However, mask B shows the least smoothing efficiency even it has relatively shallow depth (~5 nm) of pits on the substrate.

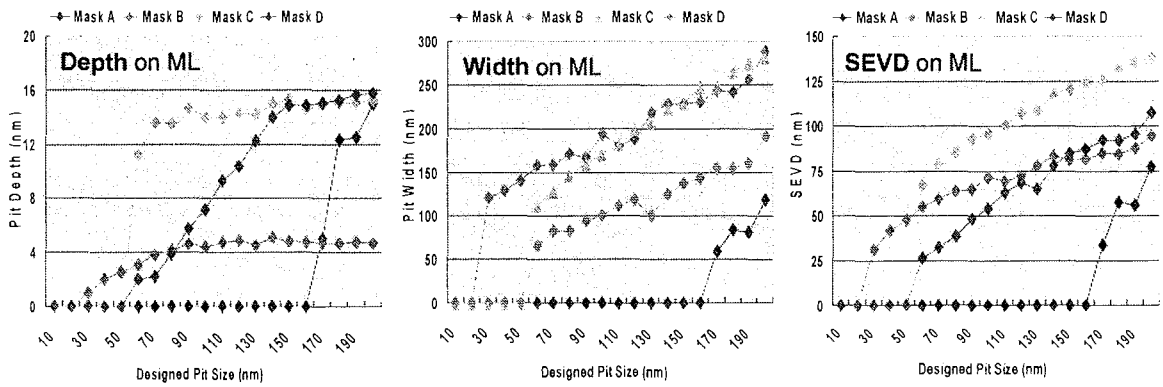

Fig. 6. Measured depth, with, and converted SEVD of programmed pits by AFM

3.4. Inspection visibility and printability of programmed pit defects

We compared inspection visibility and printability for four PDM samples (Mask A-D) by applying KLA6xx, AIT, and M7360 inspection tools and simulating aerial images for specific cases. Fig. 7 shows visual images and minimum sizes of visible pits on four PDM samples from inspection tools. In order to efficiently compare visibilities with different inspection tools, only review images (not inspection mode) were considered to determine minimum detection sizes for each case. In other words, inspection visibility of pit defects in Fig. 7 might be different from defect inspectability with threshold values. However, it is expected that minimum size of visible pits could safely extend minimum size of detectable pits. According to the inspection visibility results from KLA6xx, AIT, and M7360, it was found that KLA6xx can detect smaller pits compared to other inspection tools. As we previously described, minimum sizes of visible pits for four masks also mainly depend on ML smoothing performances. Therefore, most of programmed pits on mask A could be sufficiently smoothed and corresponding minimum detection sizes for KLA6xx and AIT are larger than other cases. On the other hand, minimum sizes of visible pits on mask B are smaller than other cases due to lower smoothing efficiency.

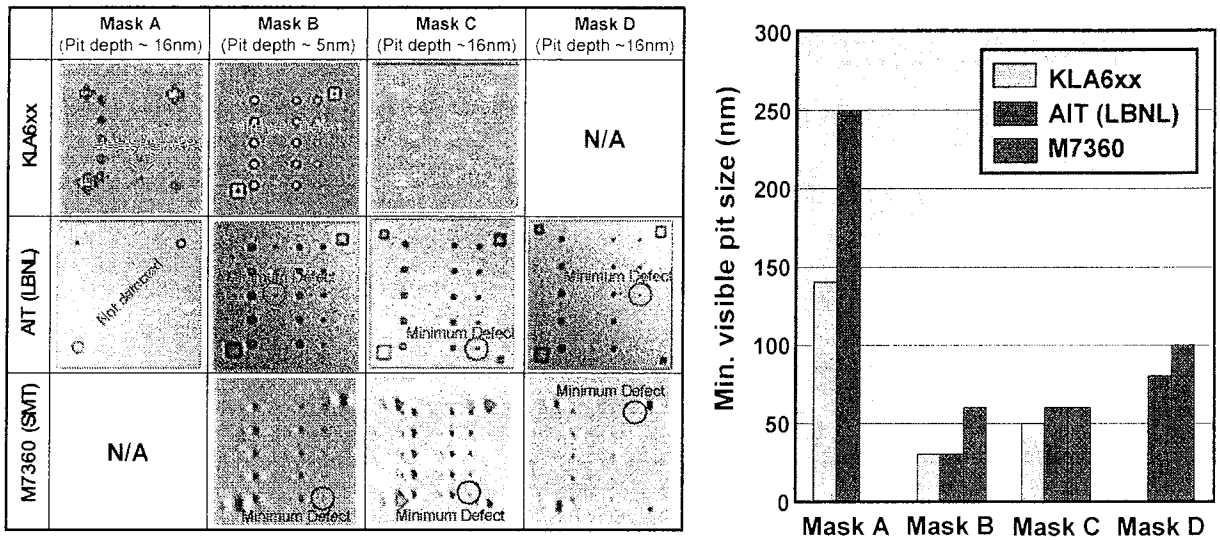

Fig. 7. Comparison of inspection visibility of KLA6xx, AIT, and M7360.

Fig. 8 shows correlations of defect printability between AIT images and simulated aerial images on the equivalent positions for programmed pits. According to the designed layout for programmed pits, ~60 nm sized pits on mask B, C, and D were selected to analyze defect printability simulation. The case of mask A was skipped since no pits were observed by AIT as shown in Fig. 7. Comparing calculated SEVD values for ~60 nm pits on ML, it was reasonably explained that pits are likely to be more printable with increasing SEVD. Moreover, the observation of AIT images are consistent with simulated aerial images based on measured data by AFM. Interestingly, for the case of mask B, shallow pit with 3 – 3.75 nm in depth shows a general ring-shaped pattern on the simulated aerial image [10]. This characteristic is ascribed to out of phase condition in pit depth as shown in Fig. 2. As a result, smaller pits are shown in AIT images due to its maximized phase effects.

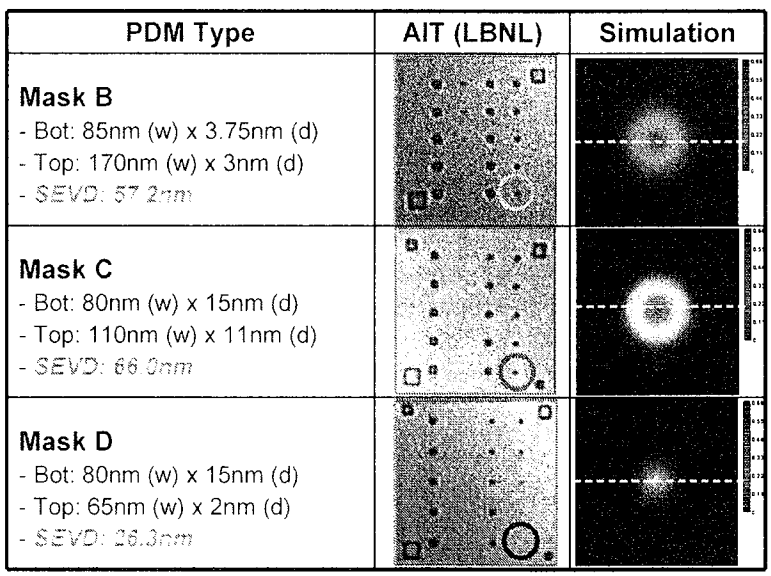

Fig. 8. Correlation of defect printability between AIT images and simulated images.

3.5. AIT: Printability of pit defects on 32nm HP L/S pattern

As we previously mentioned, inspection visibility and printability for four types of PDM without patterning were analyzed and compared according to the degree of ML smoothing efficiency. In an attempt to obtain minimum size of printable pits on real patterns, we deposited 70-nm-thick TaN absorber layer on mask D and fabricated patterned mask consisting of 32nm HP L/S. When we designed layouts for making PDM, original pit array unit on substrate was slightly misaligned along the y-axis. Our design concept can be successfully directed various situations from the best case (fully covered pits by absorber) to the worst case (fully exposed pits on ML). In Fig. 9, it can be clearly seen that the AIT images of programmed pits on the 32nm HP L/S have a totally different behaviors according to the pit locations with respect to the absorber patterns. For fully exposed pits on ML surface (Case I), minimum size of printable pit is 48.8nm-width and 4.4nm-depth on ML surface, which corresponds to 28.3nm of SEVD. As programmed pits approaches to the absorber pattern, their printability is getting smaller than case I. For partially covered pits by absorber (Case II), minimum size of printable pits increased to 73.7nm-width and 6.5nm-depth on ML surface, which corresponds to 43.0nm of SEVD. For fully covered pits by absorber (Case III), all programmed pits become not printable since it is located under the absorber. These results indicate that defect compensation by using pattern shift technique might be a promising solution to reduce printable phase defects.

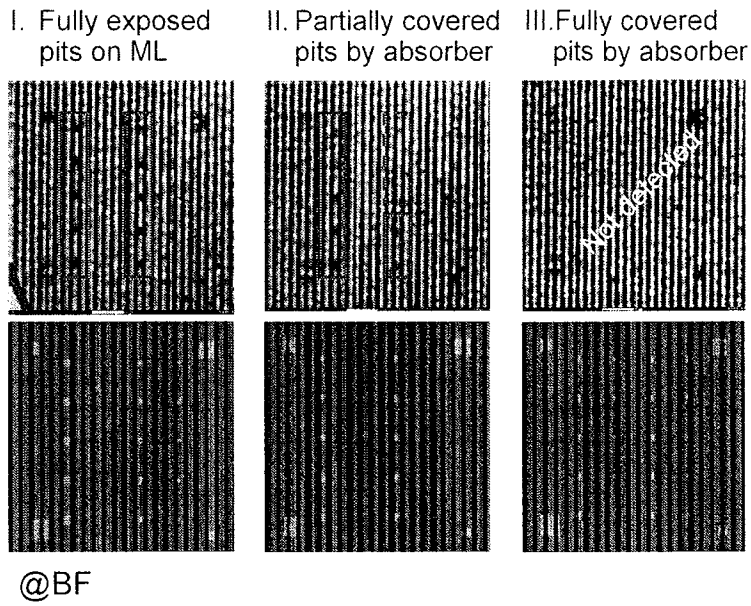

Fig. 9. AIT images according to the programmed pit positions on the HP32nm L/S patterns. (BF indicates best focus at AIT)

Generally, printability of phase defects (pit and bump types) is strongly influenced by defocus variation during ADT exposure. These results are also observed with AIT as shown in Fig. 10. Through-focus analyses with AIT for case I and III show that programmed pits become more printable at (-) defocus. Specifically, hidden programmed pits fully covered by absorber at best focus could appear on the images by using through-focus analysis. These results indicate that DOF should be a critical factor to realize defect compensation by pattern shift technique during ADT exposure.

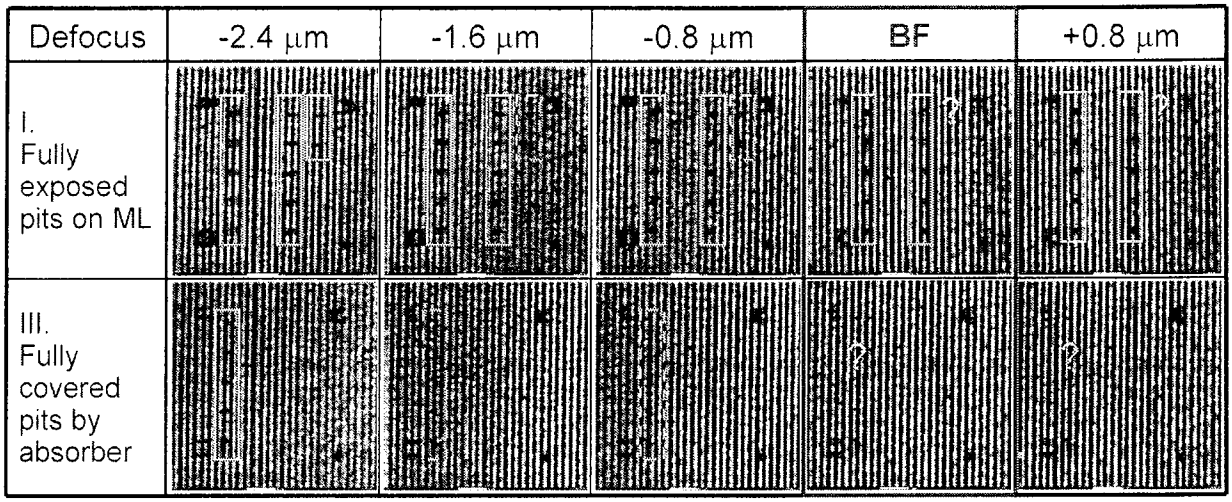

Fig. 10. AIT images according to the defocus variations on the HP32nm L/S patterns. (BF indicates best focus at AIT)

4. CONCLUSIONS

Printability and inspectability of programmed pits were investigated by simulations and experiments using PDMs. According to printability simulation on 32-nm HP L/S, minimum printable sizes of pits were strongly dependent on the degree of smoothing and original pit depth on the substrate. Through the quantitative analysis of defect inspectability, minimum detectable size of programmed pits depends on ML source due to the difference in smoothing efficiency and also depends on the types of inspection tools. AIT results with 32-nm HP L/S shows that minimum printable size of pits could be ~28.3 nm of SEVD. In addition, through-focus analysis indicates that pits become more printable at (-) defocus. Consequently, printability of phase defects strongly relies on their locations with respect to those of absorber patterns. This indicates that defect compensation by pattern shift could be a key technique to minimize printable phase defects.

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