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## Cibola Flight Experiment

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**Abstract.** Los Alamos National Laboratory is building the Cibola Flight Experiment (CFE), a reconfigurable processor payload intended for a Low Earth Orbit system. It will survey portions of the VHF and UHF radio spectra. The experiment uses networks of reprogrammable, Field Programmable Gate Arrays (FPGAs) to process the received signals for ionospheric and lightning studies. The objective is to validate the on-orbit use of commercial, reconfigurable FPGA technology utilizing several different single-event upset mitigation schemes. It will also detect and measure impulsive events that occur in a complex background.

Surrey Satellite Technology, Ltd (SSTL) is building the small host satellite, CFESat, based upon SSTL's disaster monitoring constellation (DMC) and Topsat mission satellite designs. The CFESat satellite will be launched by the Space Test Program in September 2006 on the US Air Force Evolved Expendable Launch Vehicle (EELV) using the EELV's Secondary Payload Adapter (ESPA) that allows up to six small satellites to be launched as 'piggyback' passengers with larger spacecraft.

### Introduction

Space sensors have evolved from the basic simple analog devices first flown in the 1960's with minimal data to process to the more sophisticated sensors capable of producing the exciting information that is becoming commonplace. As computing power on the ground becomes more and more powerful, there is a desire to process

this space data with state-of-the-art, ground-based computing facilities. However, since data downlink speeds cannot match the increase in processor speeds, it is not possible to downlink the data effectively to ground-based computers for processing. Thus, the only way to manage large quantities of data collected on orbit is by moving the processing to the spacecraft and

downlinking data products instead of raw data. Unfortunately, hardened space processors that would normally do the onboard processing typically lag ground-based processors by 10 years.

Since 1998, Los Alamos National Laboratory (LANL) has been assessing commercial Xilinx SRAM based Field Programmable Gate Arrays (FPGAs) for use in space-based, on-board data processors. Radiation testing has verified that radiation tolerant Virtex FPGAs offered by Xilinx offer good total ionizing dose (TID) and single event latchup (SEL) performance, but they are sensitive to single event upsets (SEU) [1,2]. In order to use Xilinx FPGAs, careful system designs are required to compensate for the device sensitivity [3, 4, 5 and 6]. Since SRAM-based FPGAs can be reprogrammed, the same FPGA-based system can be reused for various tasks by simply changing the designs held in the FPGAs. Systems such as this can provide the computation speed of application-specific hardware at a fraction of the cost while providing flexibility and reprogrammability.

Based upon this extensive ground testing and characterization at accelerators, Xilinx Virtex FPGAs are considered to be at the NASA test readiness level of 5 for use in near Earth Orbit where radiation effects impact space electronics. LANL is developing a space-based payload, called the Cibola Flight Experiment (CFE), to be hosted on a SSTL satellite bus ready for space launch in September, 2006. This flight demonstration will raise the test readiness level to 7-8 for these devices making them a reasonable risk for use by other near Earth space missions in the future.

## System Overview

### *Payload*

The primary project objective is to demonstrate the space utility of Xilinx Virtex FPGAs by testing several different types of upset mitigation schemes as well as to characterize the robustness of these chips over a wide range of temperatures. The secondary project objective is to add a radio to the input of the RCC on-board processor and to detect and measure impulsive events that occur in a complex background.

The CFE payload consists of a power converter supply, radio tuners, and digital processing hardware including: analog to digital converters (ADC), reconfigurable computers (RCC) using Xilinx Virtex FPGAs, memory, spacecraft interface communications, and a microprocessor (R6000) [3]. Four 20 MHz RF channels tunable in the VHF and UHF frequencies are ganged tuned to an intermediate frequency (IF) in the range of 55-95 MHz. The four IF channels are sampled at 100 MHz with 12-bit resolution. The digital IF is transmitted to a network of 9 Virtex XQVR1000 reconfigurable FPGAs that are used to process the intermediate frequency (IF) for ionospheric and lightning studies. The approximate payload dimensions are 38x36.x23cm.

SEAKR Engineering, Inc. is under contract to fabricate the 28V converting power supply, which is based upon their solid-state data recorder and processor product line supplies. The power supply will convert space platform unregulated and unfiltered primary 28V DC input power to regulated secondary DC power of voltage types +15V,  $\pm 5V$ , +3.3V and

+2.5V for the analog and digital electrical circuits.

The CFE payload also has 4 log-periodic array (LPA) antennas. Two crossed LPA antennas are mounted on the nadir spacecraft deck and two single LPA antennas are mounted to deployable booms provided as part of the spacecraft bus. The antennas are being fabricated under contract to L'Garde, Inc and will be based upon the same inflatable mast structure that L'Garde has designed and demonstrated on the ground for a NASA solar sail demonstration. Each antenna will weigh 1.4 kg and will be 14 x 16 x 6 cm in dimension.

### ***Satellite Bus***

SSTL, will create the satellite platform that will be used to carry the CFE payload developed by LANL. The contract with SSTL is valued at USD 11.8 million with delivery of the spacecraft to LANL for payload integration in 22 months. The satellite platform is based upon SSTL's proven microsatellite bus that has been evolving through 23 different satellite missions. The Cibola platform draws heavily on the engineering performed on the 4 DMC satellites launched in 2002 and 2003 and also on the Topsat mission due for launch in 2005.

The CFE spacecraft is an enhanced micro satellite designed to fit within the ESPA volume requirements of 60.9x60.9x96.5cm (Figure 1). The spacecraft weighs 165kg, of which 32kg is payload. The spacecraft has four deployable and two body-mounted solar panels (Figure 2). The structure is based on Aluminum and Aluminum Honeycomb panels, and includes a stack of "MicroTray" modules traditionally

used by SSTL on all its micro satellites to house the spacecraft electronics and to provide structural support [7]. The spacecraft employs a fully passive thermal control system. Two body-mounted radiators will be used to remove the excess payload heat.

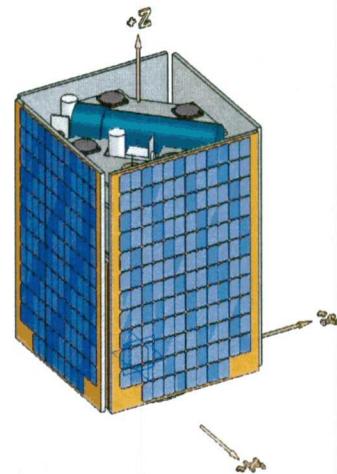


Figure 1: Early conceptual drawing of CFESat with the solar arrays stowed for flight.

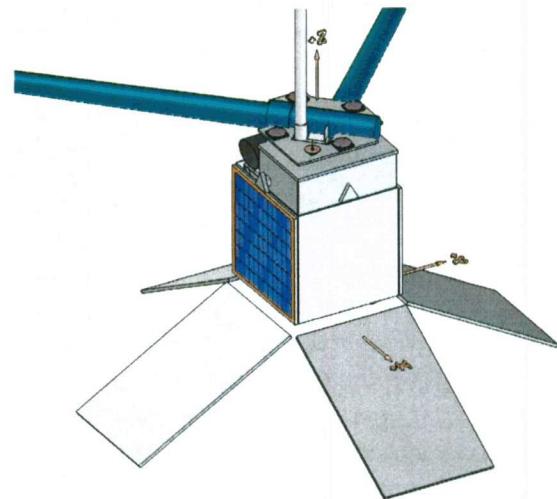


Figure 2: Early conceptual drawing of CFESat with the solar arrays and booms deployed after launch.

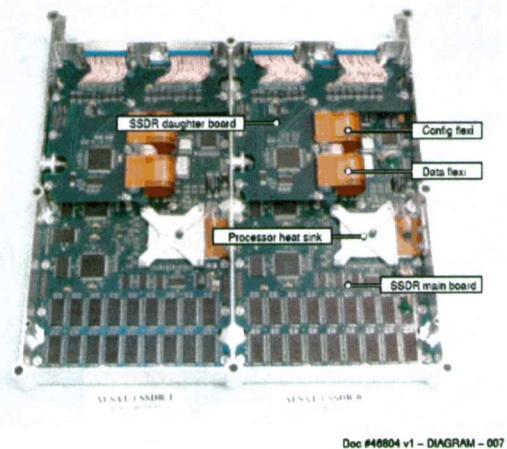


Figure 3: Dual solid-state data recorders mounted in a “MicroTray”.

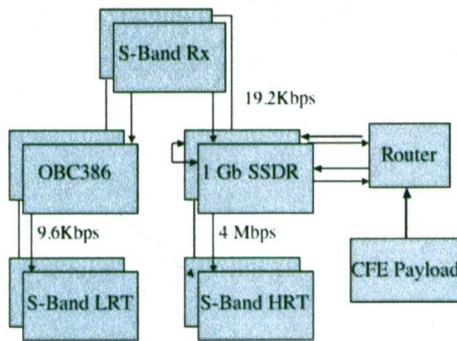


Figure 4: Spacecraft to payload architecture.

The data handling system employs a dual redundant Control Area Network (CAN) bus for distribution of telemetry and telecommands, as well as small file transfers and bootloading. Two functionally redundant OBC386 on-board computers are used to monitor spacecraft state-of-health, schedule payload support, communication, power management, spacecraft logging, attitude control, and file uploads. Two functionally redundant solid-state data recorders (SSDR), each providing 1Gbit of solid-state storage, will be integrated to the payload by means of a new router system and will be used to store the collected data for downlink as well as

act as temporary storage for uplinked commands to the payload.

The spacecraft is 3-axis stabilized, using a pitch momentum wheel and yaw reaction wheel, and dual redundant 3-axis magnetorquers. Pointing stability will be maintained to  $\pm 0.5$  deg of nadir with pointing knowledge to 0.1 deg provided by dual redundant star trackers. A GPS receiver is carried to aid navigation, and also to provide an accurate spacecraft clock.

The power system comprises two body mounted and 4 deployable triple-junction, GaAs solar panels and a LiLion battery. A raw 28V bus is distributed to both the spacecraft and payload, alongside a regulated 5V bus for the spacecraft. Lines are electronically switched and over-current protected with electronic switches. The system delivers over 110W orbit average to the platform and payloads, with 30W for the platform, and approximately 85W available for payload operations.

The telemetry and telecommand system employs S-band with a CPFSK 19.2kbps uplink, and a 38.4kbps BPSK and a 4Mbps QPSK downlink. The data handling system employs a dual redundant Control Area Network (CAN) bus for distribution of telemetry and telecommands, as well as perform small file transfers and bootloading.

Two telescoping booms will be deployed from the spacecraft supporting the two single LPA payload antennas after the solar panels are deployed.

#### *Ground Segment*

The ground station will be located at Los Alamos National Laboratory. It will be

comprised of a 3.7m tracking dish, which includes both S-band TT&C as well as the S-band high-speed payload downlink and an SSTL provided equipment rack comprised of the RF Transmitter and Receiver, Power Amplifier, Modems and baseband switching. Because the latitude of the groundstation is similar to the inclination of the orbit 5-6 contacts per day will be available for spacecraft commanding and data downlink.

When in range of the groundstation, the tracking computer displays the position of the satellite, antenna pointing information and the characteristics of the satellite transit. Precise timing for the tracking computers is derived by a dedicated SGR-10 GPS receiver. The S-band uplink at 19.2kbps is generated using a VHF exciter through an upconverter to a high power amplifier (HPA) with low-loss coaxial cable to the tracking antenna feed. The S-band downlink from the antenna feed passes through a low noise amplifier (LNA) and Band Pass Filter on the antenna mount to a down-converter to 70 MHz and then into a demodulator and protocol decoder to provide telemetry and payload data output. Spacecraft operation will be highly autonomous with the exception of command generation.

The uplink instructions are generated using PC-based software for coding and transmission to the satellite. The downlink telemetry is decoded and displayed using PC-based software. The telecommand, telemetry & payload data to-and-from the satellite and the Mission Control computers are managed via a Mission Control Ethernet local area network (LAN).

### Launch

The U.S. Department of Defense Space Test Program (STP) is including the CFE satellite as part of the STP-1 space flight mission. The STP-1 mission goal is to provide space-flight opportunity for a maximum number of DoD Space Experiments Review Board payloads on a single launch. CFE was ranked #2 in the 2000 DoD SERB competition, thus, qualifying for inclusion on this flight.

The DoD Space Test Program is responsible for the integration of seven satellites into a single payload stack and launch of the STP-1 mission. The STP-1 mission is scheduled for launch in September 2006 on a medium-class Lockheed-Martin Atlas-V, a U.S. Air Force EELV, using ESPA to allow 5 small satellites to be launched as "piggyback" passengers with the larger Orbital Express primary spacecraft.

The STP-1 mission will deploy satellites into two different orbit planes. CFESat will be deployed into a 560 km circular, 35.4 degree inclined orbit with 3 other ESPA class satellites. The expected on-orbit lifetime is expected to be about 4 years.

### Summary

LANL has designed an aggressive space experiment that will demonstrate the space utility of Xilinx Virtex FPGA for on-board space processing. Since these FPGAs suffer from single event upsets, the CFE payload will be used as an on-orbit test bed to validate various upset mitigation techniques as well as test the part robustness when used in space applications. This flight demonstration will raise the test readiness level for these devices to 7-8 making them a reasonable risk for use by other space

missions in near Earth orbit.

LANL has partnered with SSTL who will produce the space platform that will host the CFE payload. The satellite platform is based upon SSTL's proven microsatellite bus that has been evolving through 23 different satellite missions and draws heavily on the engineering performed on the recent DMC satellites and also on the Topsat mission. SSTL is on an aggressive schedule to design, fabricate, test and deliver the spacecraft to LANL in 22 months.

CFESat is slated for launch in September 2006 on the STP-1 mission. STP is providing launch services for CFE project. CFESat will be attached to a slot on the ESPA ring with 4 other satellites and will be released into a 560 km circular, 35.4 degree inclined orbit with 3 of the other ESPA class satellites. All CFE satellite operations will be performed at LANL utilizing the LANL groundstation.

### Acknowledgements

The Department of Defense Space Test Program provides spaceflight for research & development (R&D) payloads approved by the DoD Space Experiments Review Board (SERB), as well as prototype operational systems. STP builds, tests, integrates, launches, and operates on-of-a kind spacecraft and DoD satellite payloads. They are the sole provider of integration, launch, and operations for DoD payloads flying on the Space Shuttle and International Space Station.

This work would not be possible without the dedicated efforts of both the Cibola Flight Experiment team and the SSTL satellite team and the support of the

management at both of these institutions. This work is funded by the United States Department of Energy.

### References

1. E. Fuller, M. Caffrey, P. Blain, C. Carmichael, N. Khalsa, and A. Salazar, "Radiation test results of the Virtex FPGA and ZBT SRAM for space based reconfigurable computing", in *MAPLD Proceedings*, September 1999.
2. E. Fuller, M. Caffrey, A. Salazar, C. Carmichael, and J. Fabula, "Radiation testing update, SEU mitigation, and availability analysis of the Virtex FPGA for space reconfigurable computing", in *3rd Annual Conference on Military and Aerospace Programmable Logic Devices (MAPLD)*, 2000, p. P30.
3. M. Caffrey, "A space-based reconfigurable radio", in *Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA)*, T. P. Plaks and P. M. Athanas, Eds. June 2002, pp. 49-53, CSREA Press.
4. C. Carmichael, M. Caffrey, and A. Salazar, "Correcting single-event upsets through Virtex partial configuration", Tech. Rep., Xilinx Corporation, June 1, 2000, XAPP216 (v1.0).
5. Paul S. Graham, M. Caffrey, Michael J. Wirthlin, D. Eric Johnson and Nathan H. Rollins, "Reconfigurable Computing in Space: From Current Technology to Reconfigurable Systems-on-a-Chip", IEEE Aerospace Conference, March 8-15, 2003, Big Sky, MT
6. Michael J. Wirthlin, Darrel Eric Johnson, Nathan H. Rollins, Michael

Paul Caffrey and Paul Stanley Graham,  
“*The Reliability of FGA Circuit Designs  
in the presence of Radiation Induced  
Configuration Upset*”, IEEE Symposium  
on Field-Programmable Custom  
Computing Machines, April 8-11, 2003,  
Napa, CA, USA

7. Sweeting M N., “*Micro satellite and  
Mini satellite Programmes at the  
University of Surrey for Effective  
Technology Transfer & Training in  
Satellite Engineering*”; Proc. of Int.  
Symp. on Satellite Communications and  
Remote Sensing, 20-22 Sept 1995,  
Xi'an China.