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Assessment of Solder Interconnect Integrity in Dismantled Electronic Components from N57 and B61 Tube-Type Radars

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Assessment of Solder Interconnect Integrity in Dismantled Electronic Components from N57 and B61 Tube-Type Radars

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Abstract

Aging analyses were performed on solder joints from two radar units: (1) a laboratory, N57 tube-type radar unit and (2) a field-returned, B61-0, tube-type radar unit. The cumulative temperature environments experienced by the units during aging were calculated from the intermetallic compound layer thickness and the mean Pb-rich phase particle size metrics for solder joints in the units, assuming an aging time of 35 years for both radars. Baseline aging metrics were obtained from a laboratory test vehicle assembled at AS/FM&T; the aging kinetics of both metrics were calculated from isothermal aging experiments.

The N57 radar unit, interconnect board solder joints exhibited very little aging. The eyelet solder joints did show cracking that most likely occurred at the time of assembly. The eyelet, SA1126 connector solder joints, showed some delamination between the Cu pad and underlying laminate.

The B61 field-returned radar solder joints showed a nominal degree of aging. Cracking of the eyelet solder joints was observed. The Pb-rich phase particle measurements indicated additional aging of the interconnects as a result of residual stresses. Cracking of the terminal pole connector, pin-to-pin solder joint was observed; but, it was not believed to jeopardize the electrical functionality of the interconnect.

Extending the stockpile lifetime of the B61 tube-type radar by an additional 20 years would not be impacted by the reliability of the solder joints with respect to further growth of the intermetallic compound layer. Additional coarsening of the Pb-rich phase will increase the joints' sensitivity to thermomechanical fatigue.

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1. Introduction

1.1 Evaluation Objectives

The Stockpile Lifetime Extension Program (SLEP) targeted the tube-type radar units from B61-0 weapon systems for continued use in the nuclear weapons stockpile. The functionality of the solder interconnects used within the electronic assemblies was considered an important factor toward certifying these units for additional service life. Therefore, an assessment was made of the aging of solder joints found in tube-type radar systems. This assessment was based upon data obtained from hardware taken from fielded weapons. The initial step was to perform a qualitative survey of selected solder joints in a search for gross-level defects. Such defects would include cracks or deformation to the solder as well as damage to the laminate or lead materials. A quantitative assessment was then performed that examined specific microstructural properties of the solder joints. Suitable metrics were selected that pertained to aging-sensitive features of the microstructure. These metrics provided a means to quantify the extent of aging by the solder joints as a function of environmental variables—time and temperature parameters.

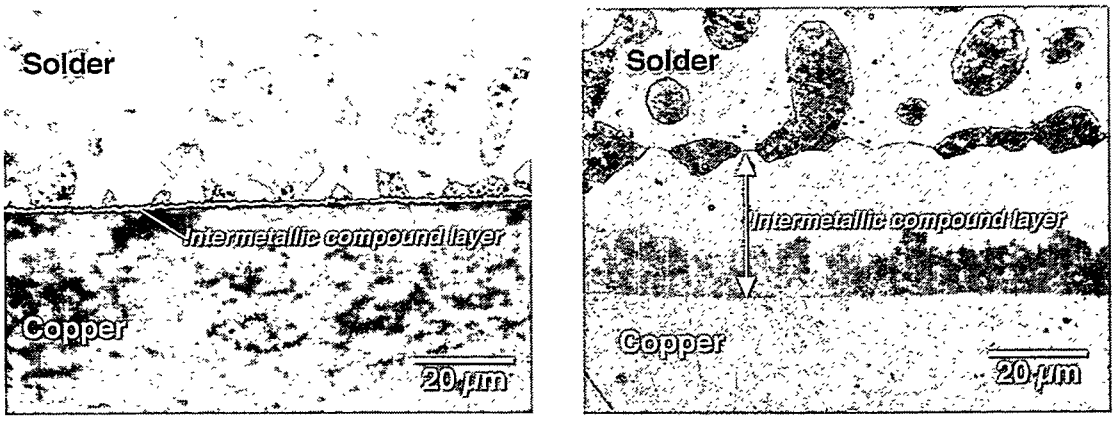
A follow-up evaluation would use the acquired data and predict the extent of further aging over *future* stockpile service life. The aging models would be exercised so as to project future changes to the solder microstructure, based upon an assumed matrix of environmental (stockpile) conditions.

The electronic circuit boards used in the B61 tube-type radars are conventional through-hole technology. The conductive features of the circuit boards (pads, lands or traces as well as the hole walls and eyelets) were *copper (Cu)*. The component lead materials (or solderable coatings over the lead materials) were also Cu, or a Cu-coated Fe-based alloy. The solder used in these assemblies was one of two likely Sn-Pb compositions, either the eutectic material, 63Sn-37Pb (wt.%) or the off-eutectic alloy, 60Sn-40Pb. A third composition, 50Sn-50Pb, was also possible. The melting properties of these alloys are:

1. 63Sn-37Pb, $T_{solidus} = T_{liquidus} = 183°C$;
2. 60Sn-40Pb, $T_{solidus} = 183°C$, $T_{liquidus} = 188°C$; and

3. 50Sn-50Pb, $T_{solidus}$ = 183°C, $T_{liquidus}$ = 212°C.

An important feature of joints formed between Sn-based solders and Cu is an intermetallic compound reaction layer that forms at the interface between the two materials (Figure 1a) [1].



(a) (b)

Figure 1. Optical micrograph of the intermetallic compound layer that forms between the 63Sn-37Pb solder and Cu substrate: (a) as-soldered condition and (b) isothermally aged for 402 days at 170°C.

The intermetallic compound layer forms initially through contact between the molten solder and the Cu substrate. Once the solder has solidified, the layer may continue to thicken, albeit more slowly, by means of solid-state diffusion processes. The effects of solid-state growth of the intermetallic compound layer under elevated temperature conditions are illustrated by the micrograph in Figure 1b. This particular sample was exposed to a temperature of 170°C for 402 days as part of an accelerated aging test. Two sublayers were observed to form as part of the overall intermetallic compound layer. The darker layer adjacent to the Cu has the stoichiometry of Cu_3Sn, while that neighboring the solder field had the Cu_6Sn_5 chemistry. The rate of growth exhibited by the intermetallic compound layer (and sublayers, as well) increases with temperature for a prescribed time interval. Moreover, the growth is not significantly affected by residual stresses generated in the joint [2]. Therefore, the intermetallic compound layer thickness, together with knowledge of the growth kinetics, provides a means of measuring the cumulative temperature exposure experienced by the solder joint through its lifetime.

A second property of Sn-Pb solder, which can also serve as an aging metric, is the size distribution of the Pb-rich phase particles located in the Sn matrix shown in Figure 2. The Sn-rich matrix is essentially pure Sn, as there is a negligible solubility of Pb in it. On the other hand, the Pb-rich phase particles typically have a finite solubility limit for Sn of 5-10%. The amount of Sn dissolved in the Pb-rich particles depends upon the cooling rate of the solder after solidification. Typically, over the service time of a solder joint, the Pb-rich phase particle contains between 0 and 5wt.% Sn.

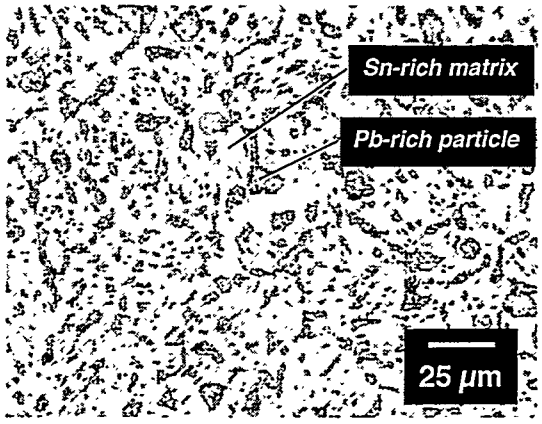


Figure 2. Optical micrograph of the microstructure of the 63Sn-37Pb solder. The dark areas are the Pb-rich phase particles; the light matrix is the Sn-rich phase.

An aging-related characteristic of the Pb-rich phase particles is that they coarsen and become fewer in number with time. The coarsening process is based on one or more diffusion processes and, thus, is thermally activated. That is, the rate of coarsening increases with temperature. Therefore, the Pb-rich phase coarsening property provides an independent assessment of the extent of aging experienced by the solder joint. However, the coarsening process is also sensitive to mechanical deformation introduced into the solder by externally applied loads and/or residual stresses. It is this stress-enhanced coarsening component that gives rise to thermal mechanical fatigue deformation and, ultimately, fracture of Sn-Pb solder joints [3].

When applied to field-returned hardware, the above analyses can be used to establish two important benchmarks. First, those data can describe the extent of aging to the solder joints resulting from the combination of (1) next-assembly manufacturing processes that exposed the

completed joint to elevated temperature conditions and (2) the time-temperature exposure history of the joint in the stockpile. Second, the "status" of the solder joints provides a starting point or initial condition from which predictions of solder joint aging can be made with regards to *future* stockpile service. The latter predictions would, of course, require knowledge of anticipated time-temperature stockpile conditions.

In the study described in the following report, an evaluation was performed to determine the extent of solder-joint aging in a stockpiled B61-0 tube-type radar. A qualitative assessment of a field-returned unit was used to identify large-scale defects in the solder joints. Then, the quantitative analyses were performed with regards to the two aging metrics of the solder joints: the thickness of the intermetallic compound layer and the Pb-rich phase particle-size distribution. These data, when combined with the suitable kinetics models, were used to calculate an effective or *cumulative* aging temperature to which the solder joints were exposed, assuming that the solder joints were *35 years old*. Recall that the computed aging temperature would represent the entire temperature history of the solder joints, starting at the time that the joint solidified. Therefore, elevated temperature environments resulting from next-assembly operations as well as the effects of stockpile storage would be included in that cumulative aging temperature value.

Unfortunately, micrographic records taken of the solder joints at the time of fabrication and/or testing were not archived (or were not taken at all in the course of product development). Therefore, it was necessary to establish a database of "as-fabricated" solder joint microstructures—the joints having been made by techniques that would closely mimic those used to make the fielded hardware. These baseline values served as the initial conditions for the kinetics expressions describing respectively intermetallic compound layer growth and Pb-rich phase particle-size coarsening. Further changes to those microstructural features were then computed for a 20-year lifetime extension of the component as a result of storage in an assumed isothermal environment.

1.2 Baseline Properties and Rate Kinetics Expressions

The intermetallic compound layer thickness and Pb-rich phase particle-size distribution were the quantitative metrics with which to assess the extent of aging of the solder joints. The degree of aging was based upon *changes* in these parameters. Therefore, it was necessary to establish the baseline quantities for these parameters that, when added to the process kinetics expressions, would allow the latter to be used to calculate the evolution of those respective metrics.

In the absence of archived micrographs of the solder joint starting microstructures, the initial or "as-fabricated" values were determined by the assembly of a present-day test vehicle. The test vehicle circuit board selected for this analysis is shown in Figure 3. The circuit board is a double-layer, 1.59 mm (0.0625 in.) thick card made of FR-4 epoxy-glass laminate. The conductor patterns (hole walls, pads, and surface strips) were formed from built-up Cu. The Cu conductor nominal thicknesses were 0.099 mm (0.0039 in.) on the surfaces and 0.040 mm (0.0016 in.) on the plated through-hole walls. The printed wiring board was designed with the following leaded devices:

1/4 W Resistor (small)	Qty.=18
1/2 W Resistors (large)	Qty.=6
CK0 Capacitors (tombstone)	Qty.=10
16-Pin Ceramic DIPs	Qty.=2
16-Pin Plastic DIPs	Qty.=1
TO5 Transistors	Qty.=5
TO18 Transistors	Qty.=2

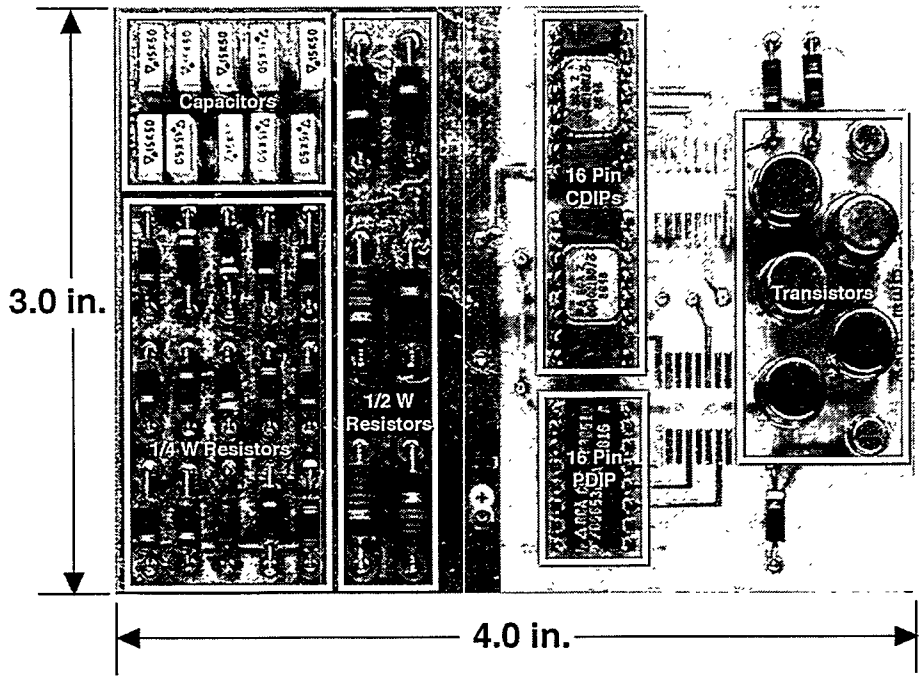


Figure 3. Photograph of the test vehicle used to establish the "as-fabricated" solder joint microstructural features of Cu/solder intermetallic compound layer thickness and the Pb-rich phase particle distribution.

The test vehicles were assembled by hand soldering. The operators were personnel from the AlliedSignal FM&T plant in Kansas City, Missouri, and had been trained and certified in the soldering of circuit board assemblies. Flux-core 63Sn-37Pb (wt.%) solder wire was used. The flux was a rosin-based, mildly activated (RMA) material. The components were inserted into the proper holes; the leads were soldered from the bottom.

Two such training boards were assembled; one circuit board had the solder joints immediately cross-sectioned, thus providing the as-fabricated condition. The second circuit board was subsequently exposed to thermal cycling conditions:

0°C ↔ 100°C
5.2C°/min ramps
15 min holds at limits
1623 cycles

The thermal cycling exposure was performed in order to obtain an evaluation of the effects of a controlled thermal cycle on the solder joints. Both the qualitative appearance of the solder joints as well as changes to the quantitative metrics of intermetallic compound layer thickness and Pb-rich phase-particle size were assessed. The analysis results of the thermally cycled boards will be described in a follow-up report.

The intermetallic compound layer thickness and Pb-rich phase size data from the solder joints on the as-fabricated test vehicles provided the respective baseline properties against which to compare the solder joint microstructures on the fielded B61 and N57 units. It was also necessary to have the appropriate rate kinetics equations that are required to predict changes to the intermetallic compound layer thickness and Pb-rich phase particle-size distribution as a function of aging time and temperature. It was assumed that the process kinetics responsible for each of the two properties could be described by the following expression:

$$x = x_o + A\, t^n \exp(-\Delta H/RT) \quad , \qquad (1)$$

where:

x is the parameter of interest, either the intermetallic compound layer thickness (m) or the mean Pb-rich phase-particle size (mm^2);
x_o is the starting or baseline parameter of each of the respective metrics (as determined from solder joints on the as-fabricated test vehicle);
A is the pre-exponential constant ($m\text{-}s^{1/n}$);
t is the time parameter (s);
n is the time exponent;
ΔH is the apparent activation energy (J/mol);
R is the universal gas constant (8.314 J/mol-K in MKS units); and
T is the temperature (degrees Kelvin).

A useful variation of Equation 1 is obtained by taking the logarithm of the expression, resulting in Equation 2 below:

$$\ln (x - x_o) = \ln A + n\ln(t) - \Delta H/RT \quad .$$

Experimental data could be fit to Equation 2 by performing a multivariable, linear regression analysis. The independent variables were ln(t) and 1/T; the dependent variable was $\ln(x - x_o)$. The output of the data was intercept, lnA, and the slopes of the two independent variables—the time exponent, n, and the parameter, $\Delta H/R$. The latter slope value was multiplied by R to arrive at the apparent activation energy. Separate expressions based upon Equation 2 were developed for each of the intermetallic compound layer growth and Pb-rich phase particle coarsening processes.

2. Experimental Procedures

2.1 Printed Circuit Boards for the Baseline Data Analysis.

Figure 4 is a photograph of the baseline circuit board. The location of the cross-sectioned solder joints used in the analyses is also shown in the figure. Table 1 lists the cross-section numbers, #1 - #5 and #7, used in the evaluation. The #6 section joints were omitted from the quantitative analyses. Table 1 also provides a description of the solder joints and the number of solder joints that were analyzed per each section. The cross-sectioned joints were mounted and metallographically polished to reveal their respective microstructures.

The analyses of the intermetallic compound layer thickness and Pb-rich phase particle distributions were established in an earlier investigation of solder joints in field-returned, electronic components [4]. The protocols used in the current study are briefly outlined below.

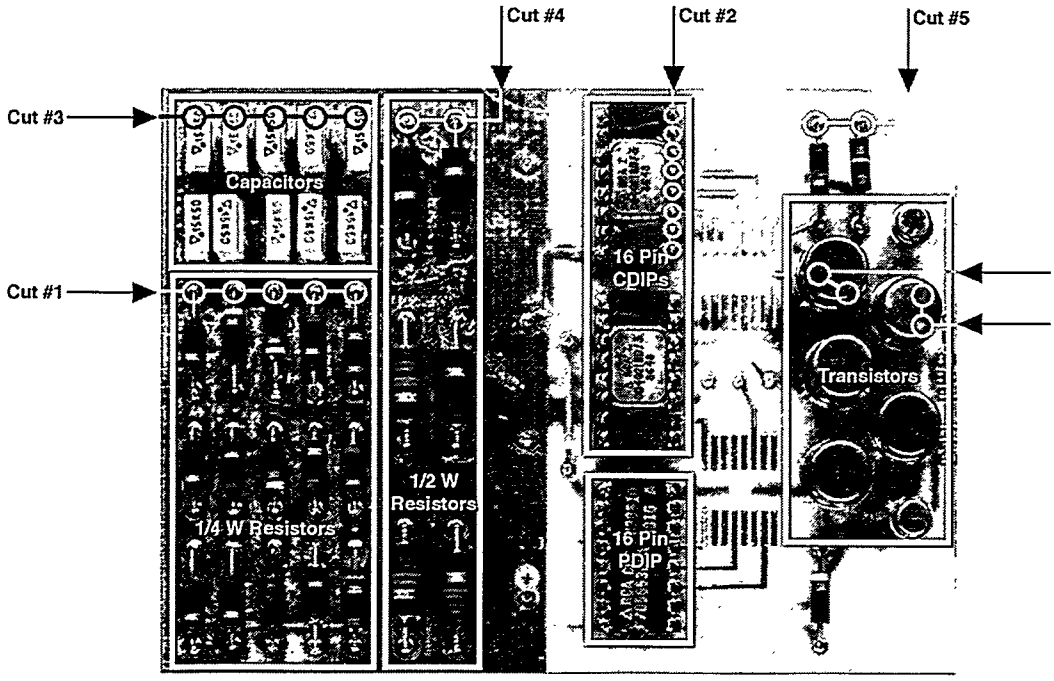


Figure 4. Photograph of the baseline properties, test vehicle showing the locations of components and their solder joints that were used for metallographic cross sections and analysis of the solder joint metrics.

Table 1
Section, Component and Quantity
of Solder Joints Providing the Baseline Parameters

Section	Component	Quantity
#1	1/4 W resistors	3 joints (of 5)
#2	16-Pin Ceramic DIP	3 joints (of 8)
#3	CK0 capacitors	5 joints (all)
#4	1/2 W resistors	2 joints (all)
#5	1/4 W resistors	2 joints (all)
#7	TO18 transistors	2 joints (all)

2.1.1 Intermetallic Compound Layer Thickness

Figures 5a and 5b show a schematic diagram of the two configurations of through-hole solder joints found in the test vehicle. The same analysis scenario was used in this part of the study. Two locations were cited for intermetallic compound layer thickness measurements; the first location was designated "A" and was at the interface between the solder and the Cu at the annular bonding pad area. The second location, "B," was the solder/Cu interface along the wall of the interior of the hole. The latter thickness measurements were taken in an effort to determine whether differences in the layer thicknesses could be identified between the two locations. However, in order to make such a comparison, it was necessary that the through-hole solder joint sections be made as close as possible to the hole centerline. This stipulation would minimize the hole wall data ("B") from being skewed to values that were larger than the actual case.

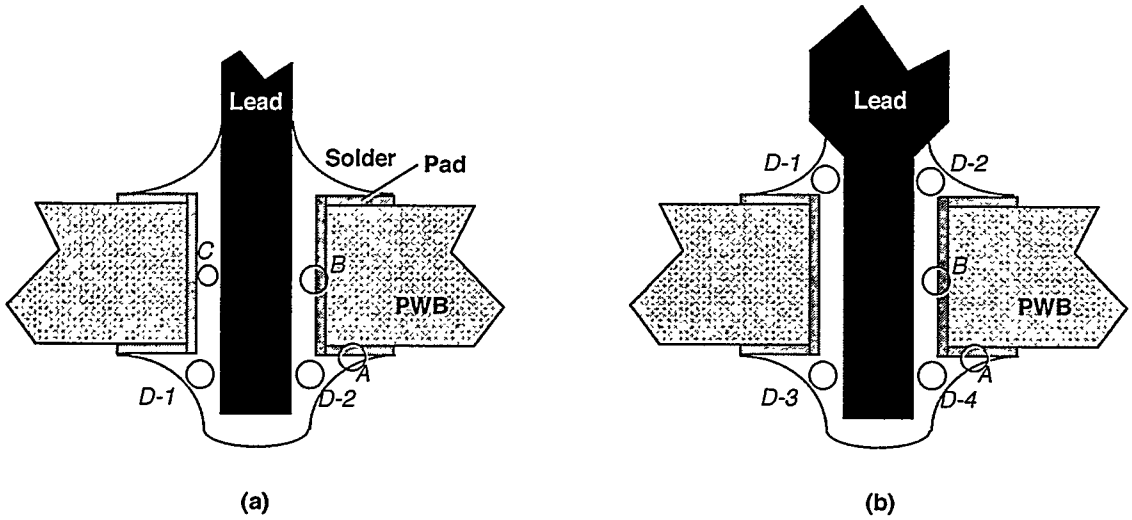


Figure 5. Schematic diagram of (a) a standard through-hole solder joint and (b) dual in-line package (DIP) solder joint having constructions representative of the solder joints in the baseline test vehicle. The locations of the intermetallic compound layer measurements were A (bonding pad) and B (hole wall). The Pb-rich phase size distribution analyses were performed on micrographs taken at the respective "D" locations in the solder fillets and in the hole interior at location C.

The intermetallic compound layer thickness was measured from a single, 1000x optical micrograph taken at the respective location. The sample had been etched to clearly define the intermetallic compound layer structure. Thirteen measurements were made per micrograph. When separate sublayers of Cu_3Sn and Cu_6Sn_5 were observed, the thickness of each sublayer, along with the total thickness, were measured. Generally, the Cu_3Sn sublayer was absent so only the measurement of the Cu_6Sn_5 layer was made. The data were comprised of the mean thickness and an "error term" based upon $\pm$ one standard deviation of the 13 measurements. The thickness values from each joint were combined with those from similar joints in that section in order to establish a single baseline, intermetallic compound layer thickness for that particular solder joint configuration.

The above analysis determined the baseline or as-fabricated intermetallic compound layer thickness per component. It was necessary to establish a reaction kinetics equation that described solid-state growth of the intermetallic compound layer as a function of the time and temperature aging conditions. The test specimens used in this study were 63Sn-37Pb/Cu couples.

The substrates were oxygen-free, high conductivity (OFHC) Cu tabs measuring 0.635 x 0.635 x 0.159 cm. The Cu composition was verified by atomic emission spectroscopy to have contaminant levels of less than the following values: 40 ppm Ag, 50 ppm Al, 10 ppm Mg, 30 ppm Mn, and 10 ppm Si (with an error of a factor of two). The surface from which the thickness values were taken was optically polished.

Each Cu tab was coated with solder by the following process. First, the substrate was solvent degreased, rinsed and dried of any remain solvent residues. The tab was then coated with a water soluble, organic acid flux to assist solder wetting/spreading. Second, the specimen was dipped it into a molten 63Sn-37Pb bath that was at a temperature of 215°C, and held there for a time duration of 5 s. Samples were then thermally aged in air furnaces capable of a temperature stability of $\pm$0.5°C. The temperature conditions were 70°C, 100°C, 135°C, and 170°C. The time periods ranged from 1 to 400 days with a tracking error of $\pm$30 min.

The extent of intermetallic compound layer growth in each of the aged samples was determined by optical microscopy on metallographic cross sections. The tab was sectioned into two pieces. One of the pieces was then ground and polished to produce a metallographically flat surface that revealed the intermetallic compound layer. Measurements of the layer thickness were performed on four, 1000x micrographs taken along the solder/substrate interface. The resolution limit for the measurements was 0.3 μm. Ten data were taken per each photograph for a total of 40 data points per aging time/temperature condition. An ancillary study concluded that using more than 40 data points did not significantly improve the precision associated with each mean thickness value.

Although data were taken from samples aged at all four aging temperatures, only those results obtained from heat treatments at the two lower temperatures—70°C and 100°C—were used in the multivariable calculation. This approach was taken because preliminary analyses showed a slight, yet significant temperature dependence to the kinetics parameters. This artifact suggests that the same diffusion mechanism and hence, apparent activation energy, would not

prevail throughout the tested temperature regime. Therefore, since it was anticipated that stockpile aging would take place under conditions more akin to the lower temperatures, only those data were used to develop the kinetics equation for predicting intermetallic compound layer growth using the format provided by Equation 2.

2.1.2 Pb-Rich Phase Particle-Size Distribution

Figures 5a and 5b show the locations in the solder joint that were analyzed for the Pb-rich phase particle sizes. In the case of the solder joints labeled Section #1, 1/4 W resistors; Section #2, 16 Pin Ceramic DIP; Section #4, 1/2 W resistors; and Section #5, 1/4 W resistors, photos for particle-size measurement were taken of both profiles of the top-side fillet ("D-1" and "D-2") and bottom-side fillet ("D-3" and "D-4") as well as the hole interior ("C"). This case is illustrated in Figure 5b. The top-side fillets were those next to the component. The bottom-side fillets were located on the circuit board side opposite to the device body. These three different locations were selected in order to determine whether differences in the Pb-rich phase particle could be distinguished between them.

In the case of sections #3 and #7 that show the CK0 capacitor and TO18 transistor solder joints, respectively, the 500x photographs were taken of the two fillet profiles on the bottom of the joint only; those locations were designated "D-1" and "D-2." The Pb-rich phase size was also measured in the hole interior ("C"). The photomicrograph was taken of the as-polished sample (i.e., no etching treatment was performed).

Quantitative image analysis was performed on the 500x magnification photomicrographs to determine the distribution of sizes present in the solder joint. The photomicrographs were digitized for analysis by a commercial software package. The Pb-rich particle-size distributions were graphically displayed as a series of histograms that exhibited the particle counts as a function of bin location—each bin representing a particle-size window. The measurements were also assessed for an overall mean particle size as represented by the area footprint of the particle.

A standard deviation value, maximum particle size, number of particles within the viewed area, and the total area percent covered by the Pb-rich phase particles were also provided by the analysis routine.

The kinetics of the Pb-rich phase particle coarsening process were determined as follows. The samples used previously to determine the intermetallic compound layer growth kinetics at 70°C and 100°C were retrieved for this exercise. Optical micrographs were taken of the solder microstructure at two locations (designated arbitrarily as A and B), using a magnification of 500x. Earlier analyses had determined that the 500x magnification was suitable for maximizing detection of the particles [4]. An analysis at higher magnifications would cause the sampling area to be smaller than the feature variation dimension in the particles, thereby increasing the likelihood of viewing an area that was not representative of the overall Pb-rich phase distribution. The use of a lower magnification caused the smaller particles to be lost to the resolution limit of the imaging software/computer hardware capabilities.

The images were digitized and a record made of the Pb-rich phase particle-size distributions at the two locations. Those two distributions were combined to represent the particular aging condition. The parameters displayed by the quantitative analyses were the mean and standard deviations of the measurements. The mean particle sizes as a function of aging time and temperature were fit to an equation similar to Equation 2 using the multivariable linear regression analysis. This fit allowed for the computation of the parameters A, n, and ΔH to develop a predictive expression for phase coarsening as a function of time and temperature parameters.

2.2 N57 Analysis

The N57 tube-type radar units (P/N 300922) were nearly identical to the B61 tube-type radars (MC1828) that were the target component of this study. The N57 hardware was used to establish analysis protocols prior to reception of the B61 units. One channel section was examined. Immediate access was available to the interconnect (or junction) circuit board (1433983-6, BBN-2912-H4) that straddles the two separate-channel assemblies (Figure 6). The solder joints formed between the junction board and an SA1126 connector soldered to it were similarly investigated. Lastly, the terminal/pole connector (1433806-3, BBN-2479-E4) solder joints were extracted from the top of the assembly for study.

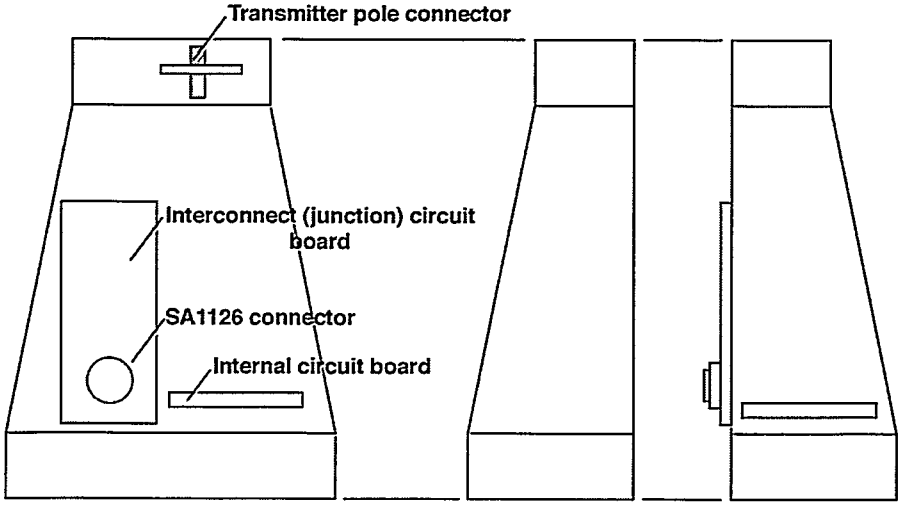


Figure 6. Schematic diagram of the location of the interconnect (junction) circuit board and transmitter-pole connector solder joints in the N57 and B61 tube-type radars.

The junction circuit board was removed from the unit. A protective elastomer layer had been placed on the board at the time of assembly; this layer obscured a visual assessment of the solder joints, necessitating that the solder joints be cross-sectioned. The circuit board was built with Cu, plated-through holes measuring 0.070 in. in diameter (Figure 7). The holes were also fitted with a Cu sleeve or eyelet that, itself, had a nominal thickness 0.006 in. The eyelet was inserted into the hole and swaged at either end to secure it into place (PS 9914002). The lead and

eyelet were then hand soldered together into the circuit board hole. The leads were a Cu-plated, Fe-based alloy measuring 0.031 in. in diameter. It was clear from the construction of the printed circuit board that the Cu hole plating and Cu eyelet provided redundant electrical conduction paths.

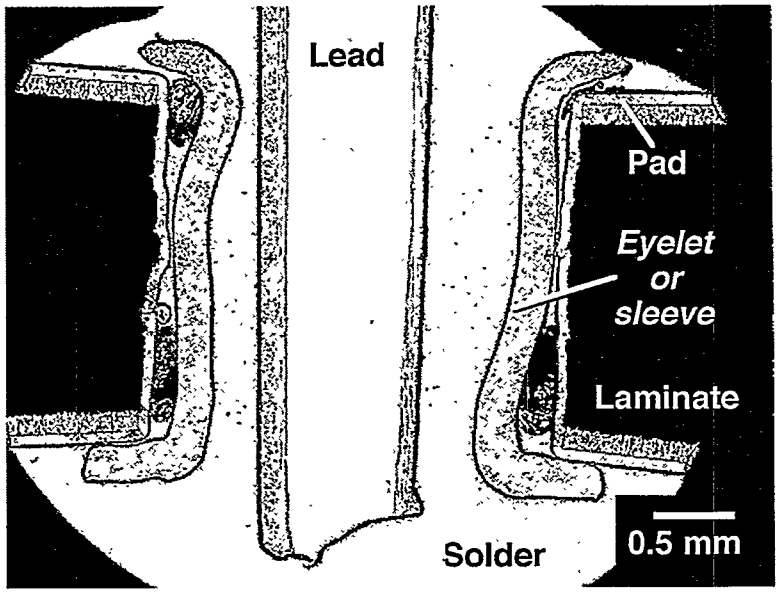


Figure 7. Optical micrograph of the through-hole solder joints from the junction circuit board of the N57 radar unit. The eyelet or sleeve structure is identified.

Five segments were cut from the circuit board, mounted and metallographically prepared for examination. The first two segments, which included 11 solder joints from segment #1 and 6 solder joints from segment #2, were used largely for qualitative observations of the joint structures. The remaining three segments received more thorough qualitative and quantitative evaluations. The number of solder joints for those specimens was:

1. segment #3, 3 joints,
2. segment #4, 4 joints, and
3. segment #5, 2 joints.

The qualitative assessment of the solder joint microstructures included a search for evidence of manufacturing defects such as poor solderability and void formation. The solder joints were further examined for evidence of longer term, aging, related defects such as cracking caused by overstress or fatigue loading as well as corrosion activity.

The quantitative assessment of the solder joint microstructures examined the thermally activated aging phenomena of (1) intermetallic compound layer growth at the solder/Cu feature interfaces and (2) coarsening of the Pb-rich phase particles present in the Sn-rich matrix. Figure 8 is a schematic diagram of the junction board solder joints, showing the locations at which the intermetallic compound layer measurements were taken—E, at the mid-plane position of the hole wall and F, at the bonding pad/solder interface away from the edge of the sleeve. At each interface, a 1000x magnification micrograph was taken. The intermetallic compound layer thickness was measured at 13 locations along that interface. The intermetallic compound layer thickness was designated by the mean of the 13 values and an error term determined from $\pm$ one standard deviation.

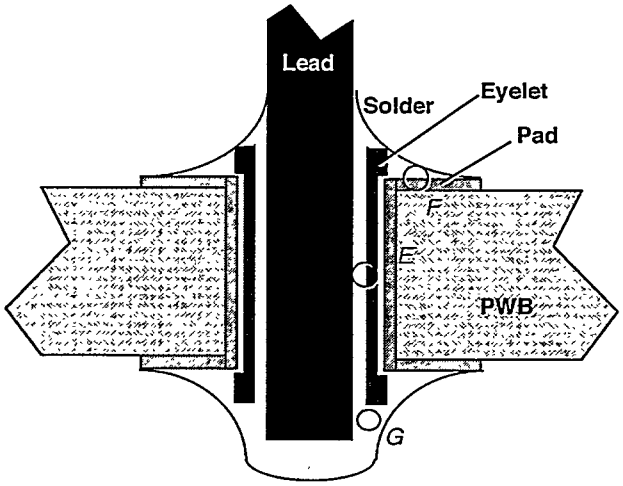


Figure 8. Schematic diagram of the through-hole solder joint on the N57 junction circuit board, indicating the locations at which the intermetallic compound layer thickness (E, hole wall and F, the bonding pad Cu strip) and Pb-rich phase particle-size distribution (G, bottom-side fillet) were made.

The Pb-rich phase particle-size distribution was measured at a single location designated by the letter "G." That location was in the solder fillet (section) at the bottom of the joint. Quantitative image analysis software was used to assess the particle-size distribution from a 500x magnification micrograph taken of the solder microstructure near to the center of the fillet. To support subsequent statistical analyses, a mean particle (area) size and associated standard deviation were calculated to represent the particle-size distribution at the particular location.

It was surmised that the joints made between the lead components and the interconnect circuit board were made by soldering from the top side of the board. This conclusion was drawn from two observations. First, the leads were straight in the hole; the leads had not been clinched as would be required when soldering from the back side to prevent the component from falling off of the board. Second, the leads had been clipped prior to completion of the solder joint, leaving a minimal length that would not have been sufficient to prevent the component from falling off of the board if soldered from the bottom.

The pins of an SA1126 connector were also soldered to the junction board. Because of the geometry of the connector, connector pins were soldered from the bottom side of the circuit board. The pins measured 0.039 in. in diameter and were soldered into holes in the printed circuit board having the same dimensions and construction as noted above. Six-pin solder joints were examined in the study. First, the solder joints were qualitatively assessed for outward signs of mechanical damage. Then, the solder joints were exposed to quantitative analysis of intermetallic compound layer thickness (pad site only) and the Pb-rich phase particle-size distributions. In the latter case, 500x photomicrographs were taken of both the bottom-side and top-side fillets for subsequent evaluation of the Pb-rich phase-particle size.

The solder joints of the terminal pole connector assembly (1433806-3) were evaluated. Photographs of cross sections of the connector and "pin-pin" solder joints are shown in Figures 9a and 9b, respectively. The pin-pin connection is a solder joint made between the pin that emanates from the connector proper and is solder attached to a second pin that leads into the radar assembly body. Examination of the pin-pin connection and solder joints within the connector was largely qualitative with the exception that the Pb-rich phase particle-size distribution was evaluated for the pin-to-pin solder joints using 500x magnification photomicrographs of the solder within the fillet.

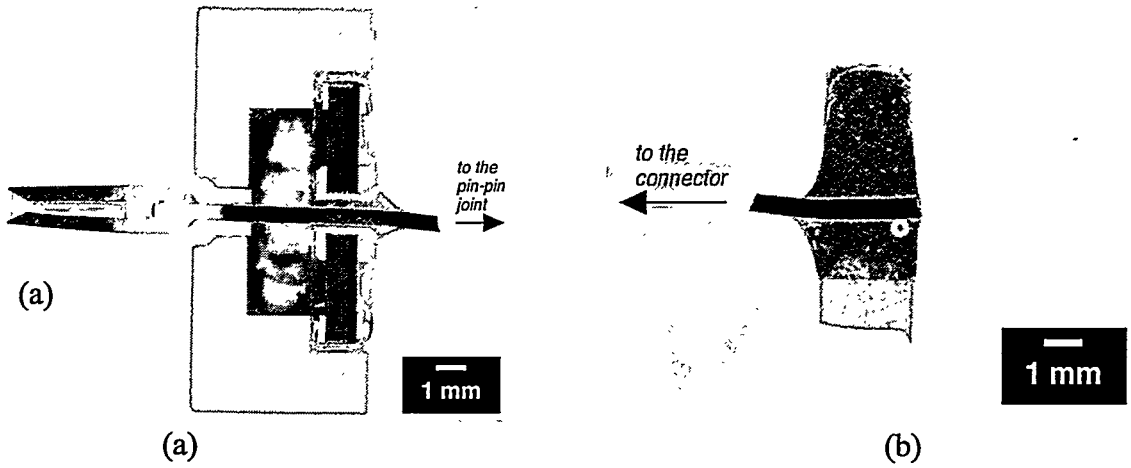


Figure 9. Cross sectional views of the (a) connector structure and (b) "pin-pin" solder joints of the terminal/pole connector assembly.

2.3 B61 (0) Analysis

An MC1828 radar assembly from a dismantled B61-0 unit was obtained for the analysis. The two halves were separated; one half was archived, while the other was used in the study. The radar half-unit that was evaluated was comprised of the five-segment stack from top-to-bottom: (1) 1440084-27, BBN3645-L9; (2) 1440097-4, BBN4797-L9; (3) 1440098-9, BBN5019-E9; (4) 1440099-4, BBN4825-K9; and (5) 1440100-4, BBN4753-G9. The solder joints in the "left-side" terminal/pole connector (1440097-3, BBN4797), located in the first segment, were also evaluated.

As in the N57 unit, the interconnect printed circuit board (1433983-6) was located between the two radar halves; a section of the circuit board adjacent to segment #2 in the stack (above) was cut from the board. The cross-sectioned solder joints were analyzed in the manner illustrated in Figure 10. Five solder joints were analyzed from segment #1, while three solder joints were evaluated from each of the two segments designated as #2 and #3, for a total of 11 solder joints that were assessed from the interconnect board.

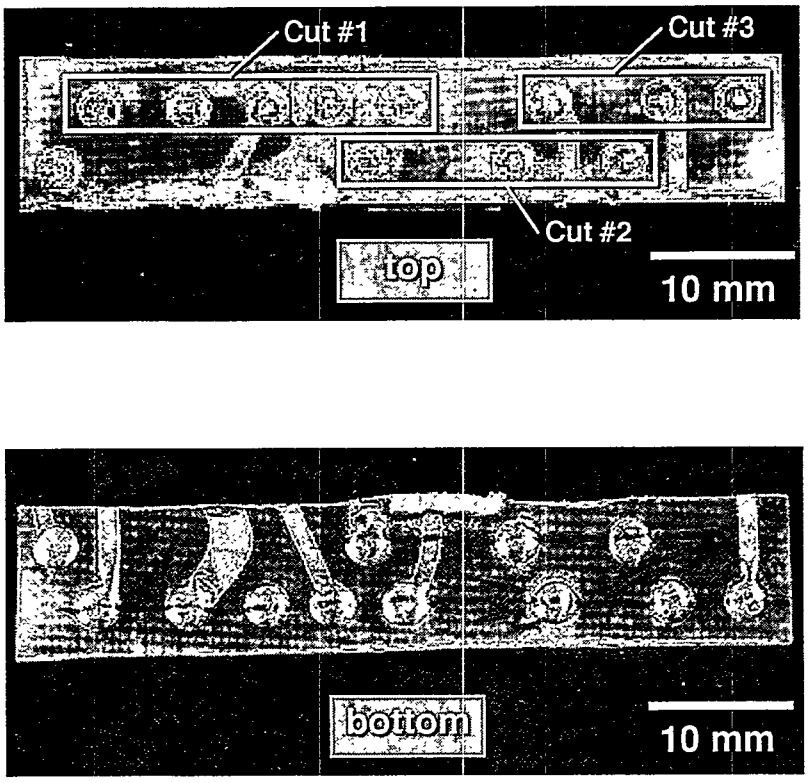


Figure 10. Photograph of the interconnect circuit board segment removed from the MC1828, B61-0 radar. Solder joints targeted for quantitative analysis were those from each of three cuts, #1, #2, and #3.

The interconnect circuit-board solder joints were evaluated by the following procedure. The solder joint microstructures were quantitatively assessed for (1) intermetallic compound layer growth at the solder/Cu feature interfaces and (2) coarsening of the Pb-rich phase particles present in the Sn-rich matrix. As was illustrated in Figure 8, the intermetallic compound layer measurements were made at location E—a point at the mid-plane position of the hole wall—and at location F at the bonding pad/solder interface away from the edge of the sleeve. At each interface, a 1000x magnification micrograph was taken; the intermetallic compound layer thickness was measured at 13 locations along that interface. The intermetallic compound layer thickness was designated by the mean of the 13 values and an error term determined from $\pm$ one standard deviation.

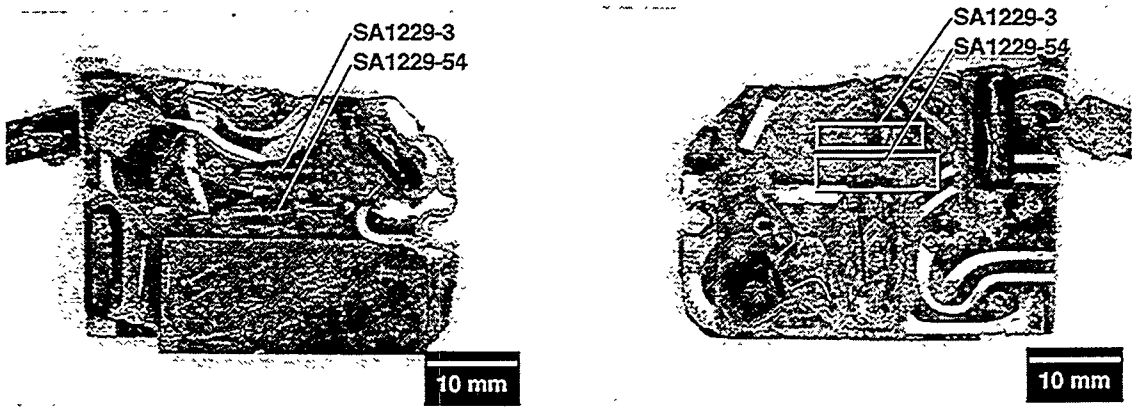
The Pb-rich phase particle-size distribution was measured at two locations. The first site, designated by the letter "G," was in the solder fillet (section) at the bottom of the joint and

similarly shown in Figure 8. The second site, denoted as "H," was located in the top-side fillet (single quadrant of view). As described above, quantitative image analysis was performed on 500x magnification micrographs taken of the solder microstructure near the center of the respective fillets. Statistical parameters included the mean particle (area) size and standard deviation.

The solder joints of the leaded devices were most likely made by a soldering operation performed on the top side of the board. This conclusion was drawn from the same characteristics as described in the N57 analysis above. The SA1126 connector solder joints were made to the circuit board from the bottom. The top side of the joints would have been inaccessible because of the connector structure.

A circuit board was extracted from the fourth segment (1440099-4) of the radar stack. The potting material was removed (mechanically) to expose both sides of the circuit board. Figure 11 shows those two surfaces. Low-magnification, stereo microscopy confirmed that there was no apparent damage caused to the solder joints as a result of removing the potting material. The solder joints from the two resistors designated SA1229-3 and SA1229-54 were evaluated. The solder joints, themselves, received the nomenclature of "3-1" and "3-2" for those from the SA229-**3** resistor and "54-1" and "54-2" for solder joints from the SA1229-**54** resistor. The solder joints were metalographically cross-sectioned. In a similar analysis methodology as was used with the interconnect circuit board solder joints, the intermetallic compound layer thickness was measured along the barrel wall (position "E") and the top-side fillet pad (position "F") via 1000x micrographs taken at the respective solder/Cu interfaces. The Pb-rich phase particle-size distributions were evaluated from 500x micrographs taken at each of a bottom-side and top-side fillet (positions "G" and "H," respectively).

Lastly, as suggested by the geometry of the leads observed in the joint cross sections, the solder joints were most likely made by soldering operations performed at the top side of the circuit board.



(a) (b)

Figure 11. Circuit board extracted from segment 1440099-4 of the radar stack: (a) top-side and (b) bottom-side. The solder joints from the two resistors designated SA1229-3 and SA1229-54 (top side) were evaluated.

3. Results and Discussion

3.1 Baseline Data Analysis

3.1.1 Intermetallic Compound Layer Thickness

Table 2 shows the intermetallic compound layer thickness data from the as-fabricated circuit board. In every case we observed that the layer was comprised entirely of the Cu_6Sn_5 intermetallic compound stoichiometry; there was no indication of the formation of the Cu_3Sn composition. From a qualitative perspective, the thicknesses are considered to be very small—being in the range of 0.3 to 1.0 μm that is typically observed in newly formed solder joints. We first analyzed the data in Table 2 to determine whether significant differences rested in the intermetallic compound layer thicknesses that were measured at the pad versus those measured at the hole walls. A Student's t-test procedure was used to test the hypothesis of whether the mean value of the layer thickness evaluated at the pad was the same or different from that at the hole wall. The correct t-test to be used was dependent upon the equivalence of the variances of the two data sets as was assessed by the F-test. It was assumed that the distributions were normal and that the sample statistics (mean, x, and variance, s^2) represented the distribution statistics (mean, μ, and variance σ^2).

Table 2
Mean Intermetallic Compound Layer Thickness (μm)
one standard deviation in parentheses

Component	Joint #	Pad (A)	Hole Wall (B)
1/4 W resistors	#1	0.77 (0.23)	0.77 (0.20)
(3 joints	#2	0.81 (0.25)	0.66 (0.19)
	#3	0.68 (0.22)	0.69 (0.24)
16 Pin Ceramic DIP	#1	0.68 (0.24)	1.05 (0.31)
(3 joints)	#2	0.74 (0.24)	0.97 (0.30)
	#3	0.79 (0.13)	0.83 (0.18)
CK0 capacitors	#1	0.53 (0.12)	0.63 (0.19)
(5 joints)	#2	0.48 (0.13)	0.64 (0.15)
	#3	0.52 (0.13)	0.69 (0.12)
	#4	0.53 (0.14)	0.95 (0.36)
	#5	1.08 (0.63)	0.85 (0.19)
1/2 W resistors	#1	0.78 (0.21)	0.82 (0.27)
(2 joints)	#2	0.78 (0.28)	0.77 (0.15)
1/4 W resistors	#1	0.74 (0.40)	0.61 (0.19)
(2 joints)	#2	0.59 (0.14)	0.74 (0.17)
TO18 transistors	#1	0.70 (0.15)	0.75 (0.45)
(2 joints)	#2	0.71 (0.16)	0.96 (0.40)

Table 3 shows the number of joint pairs having equivalent layer thicknesses between the two positions. Overall, the data showed that in 14 of 17 joints, or 82%, the intermetallic compound layer thickness measured at the pad was not significantly different from that measured at the hole wall.

Table 3
Equivalence of Intermetallic Compound Layer Thickness Between the Pad (A) and Hole Wall (B) Positions of the Baseline Test Vehicle

Component	Equal Thicknesses/ Total # of Joints	Description of Unequal Joints
1/4 W resistors (3 joints)	3/3	---
16-Pin Ceramic DIP (3 joints)	2/3	B>A
CK0 capacitors (5 joints)	3/5	B>A B>A
1/2 W resistors (2 joints)	2/2	---
1/4 W resistors (2 joints)	2/2	---
TO18 transistors (2 joints)	2/2	---

Also described in the table is an indication of which layer was thicker relative to the other, when the thicknesses between the two positions were significantly different. In those instances in which such a difference was noted, it was the case that the hole wall thickness was greater than the pad thickness. Unfortunately, the source of this observation cannot be conclusively based upon a difference in metallurgical phenomena between the two locations. The metallographic cross section is taken parallel, and as close as possible, to the hole axis. However, any slight deviation off of that axis will result in an artificial enlargement of the layer thickness in the plane of the micrograph as is illustrated in Figure 12. Since the pad data would not be subjected to this artifact, those thicknesses were designated to represent the intermetallic compound layer formation for the particular hole, joint, etc. and were used solely in subsequent analyses.

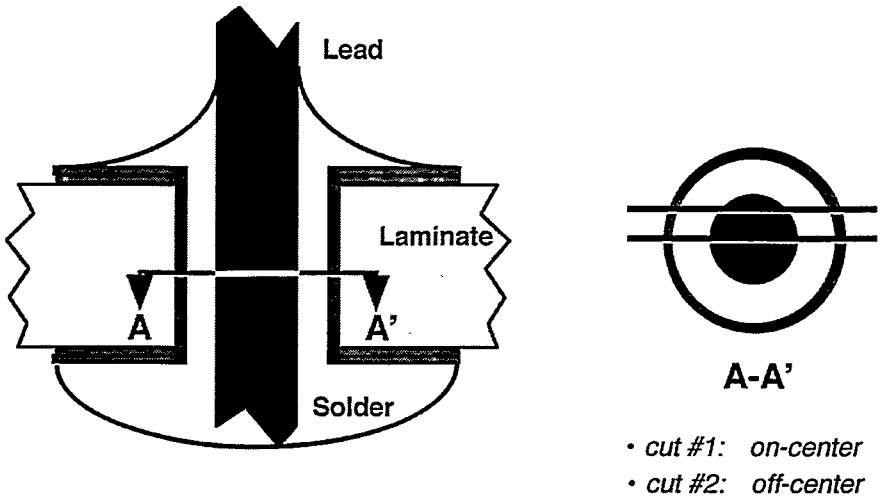


Figure 12. Schematic diagram of the effect of metallographic cross section position on the apparent thickness of the intermetallic compound layer taken at the hole wall (position B).

In our next analysis we examined whether there were significant differences in the intermetallic compound layer thicknesses (pad location, A) among joints from the same components. We performed a pair-wise analysis on the data taken from each component category to test the hypothesis of equivalent means. The slightly more involved procedure was used to determine the pair-wise equivalence of the means. This approach used the mean and variance of the individual data sets, rather than a calculation using all of the individual thickness measurements, to establish the equivalence of variances (F-test) and then, the equivalence of means (t-test). The hypothesis H_o of equivalent variances was determined for a 95% confidence interval (α=0.05). The f parameter was determined from the following equation:

$$f = s_1^2 / s_2^2 \quad , \tag{3}$$

where s_1^2 is the variance of the first data set, and s_2^2 is the variance of the second data set. The f parameter is always less than one so that $s_1^2 < s_2^2$. Then, the value of f is compared to the two-tail, 95% confidence intervals of the F-distribution determined for $\nu_1=n_1-1$ and $\nu_2=n_2-1$ degrees of freedom, where n_1 and n_2 are the populations of the two test groups:

$$F(\nu_1, \nu_2, \alpha/2) < f < F(\nu_1, \nu_2, 1-\alpha/2) \quad H_o: \sigma_1^2 = \sigma_2^2 \quad . \tag{4}$$

The hypothesis of equivalent valences is rejected under the following conditions:

$$f < F(\nu_1, \nu_2, \alpha/2) \quad . \tag{5a}$$

$$f > F(\nu_1, \nu_2, 1-\alpha/2) \quad . \tag{5b}$$

Once the equivalence of the variances had been tested, one of two paths could be taken to ascertain the equivalence of the distribution means, μ_1 and μ_2. In the event that the variances tested equivalent, then the 95% confidence interval for testing the means was established by the following criterion:

$$\left\{(x_1-x_2) - [s_p\,(t_{(\nu,\,1-\alpha/2)})(1/n_1 + 1/n_2)^2]\right\} < \mu_1 - \mu_2 < \tag{6}$$

$$\left\{(x_1-x_2) + [s_p\,(t_{(\nu,\,1-\alpha/2)})(1/n_1 + 1/n_2)^2]\right\} \quad .$$

The parameter, s_p or "pooled standard deviation" is calculated from the following equation:

$$s_p = [(n_1-1)s_1^2 + (n_2-1)s_2^2] / (n_1 + n_2 - 2) \quad . \tag{7}$$

The degrees of freedom parameter, ν, in Equation 6 are computed from the expression:

$$\nu = n_1 + n_2 - 2.$$

Referring to Equation 6, should zero (0) lie between the two limits, then the hypothesis tests correct; that is, $\mu_1 - \mu_2 = 0$. Therefore, the distribution means and the sample means are equivalent.

The second circumstance occurs when the variances are not equivalent. A similar format is used to determine the equivalence of the means; however, the limits are determined from different expressions:

$$\left\{(x_1-x_2) - (t_{(f,\,1-\alpha/2)})(\,s_1^2/n_1 + s_2^2/n_2)^{1/2}\right\} < \mu_1 - \mu_2 < \tag{8}$$

$$\left\{(x_1-x_2) + (t_{(f,\,1-\alpha/2)})(\,s_1^2/n_1 + s_2^2/n_2)^{1/2}]\right\} \quad .$$

The parameter, f, is calculated from the following equation:

$$f = [s_1^2/n_1 + s_2^2/n_2]^2 \,/\, [(s_1^2/n_1)^2 \,/\, (n_1-1) \;+\; (s_2^2/n_2)^2 \,/\, (n_2-1)] \tag{9}$$

Table 4 shows a determination of the frequency of equivalence in pair-wise comparisons between each of the joints per component category. The table also lists the mean thicknesses and standard deviations for the combined data. The results illustrate that only the CK0 solder joints exhibited some instances of non-equivalent thicknesses among the evaluated solder joints. Otherwise, the same layer thickness was observed statistically per the given component configuration in 15 of the 19 pair-wise comparisons, or approximately 79%. This information establishes a consistency of layer thickness between equivalent joints, lending confidence to the fact that a sufficient number of joints were included in the analyses.

In the next step of the layer thickness assessment, a similar evaluation was performed that compared the mean thicknesses between all of the different component categories. The same pair-wise comparison procedure as described above was once again used. It was determined that equivalent mean thicknesses existed in *all* 15 possible pair-wise comparisons. The overall mean intermetallic compound layer thickness (and one standard deviation) was computed as (carrying an extra significant figure):

$$x_o = 0.714 \pm 0.269\ \mu m \tag{10}$$

Table 4
Equivalence of Intermetallic Compound Layer Thickness (μm) via Pair-wise Comparison Between Joints Per Component Type and Combined, Mean Layer Thickesses on the Baseline Test Vehicle
one standard deviation in parentheses

Component	Equal Thicknesses/ Total # of Joints	Mean Intermetallic Compound Layer Thick.
1/4 W resistors (3 joints)	3/3	0.76 (0.24)
16-Pin Ceramic DIP (3 joints)	3/3	0.72 (0.23)
CK0 capacitors (5 joints)	6/10	0.63 (0.38)
1/2 W resistors (2 joints)	1/1	0.78 (0.25)
1/4 W resistors (2 joints)	1/1	0.67 (0.32)
TO18 transistros (2 joints)	1/1	0.71 (0.16)

This value will serve as the intermetallic compound thickness value for as-fabricated solder joints made by the hand assembly of circuit boards. Solder joint aging will be based upon the above value of x_o as the initial condition.

Once an initial condition (x_o) had been determined, it was necessary to obtain the appropriate kinetics equation that would predict the rate of intermetallic compound layer growth under specified time and temperature conditions. Figure 13 shows an intermetallic compound layer thickness in 63Sn-37Pb/Cu that couples as a function of thermal aging time and temperatures of 70°C and 100°C. The data were fit to Equation 2 in order to compute the values of the pre-exponential term, A; time exponent, n; and apparent activation energy, ΔH. The complete intermetallic compound layer growth kinetics equation, including the introduction of x_o as designated by Equation 10, is given as:

$$x = 0.714 \times 10^{-6} + 3.265 \times 10^{-3}\, t^{0.58} \exp(-52200/RT) \quad . \qquad (11)$$

The units of the variables and parameters are:

1. x and 0.714×10^{-6} (m);
2. 3.265×10^{-3}, ($m\text{-}s^{1/n}$);
3. t, (s);
4. 52200, (J/mol);
5. R; (8.314 J/mol-°K), and
6. T, (°K = °C + 273).

The 95% confidence intervals on the values of n and ΔH were ±0.07 and ±8500 J/mol, respectively.

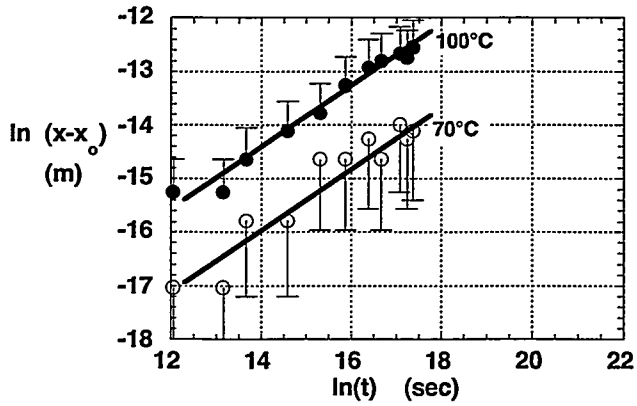


Figure 13. Graph of intermetallic compound layer thickness from 63Sn-37Pb/Cu couples aged at temperatures of 70°C and 100°C and time periods of up to 400 days.

3.1.2 *Pb-Rich Phase Particle-Size Distribution*

Figure 14 shows the histograms representing the Pb-rich phase particle-size distribution as measured in the top-side fillet (D-1) of a 1/4 W resistor solder joint (cut #1). The number of particles counted in each bin is also noted in italic print. The statistical parameters are:

(a) the mean particle size, 5.40×10^{-6} mm^2;
(b) the standard deviation, 1.47×10^{-5} mm^2;
(c) the maximum particle size, 2.10×10^{-4} mm^2; and
(d) total number of particles, 3007.

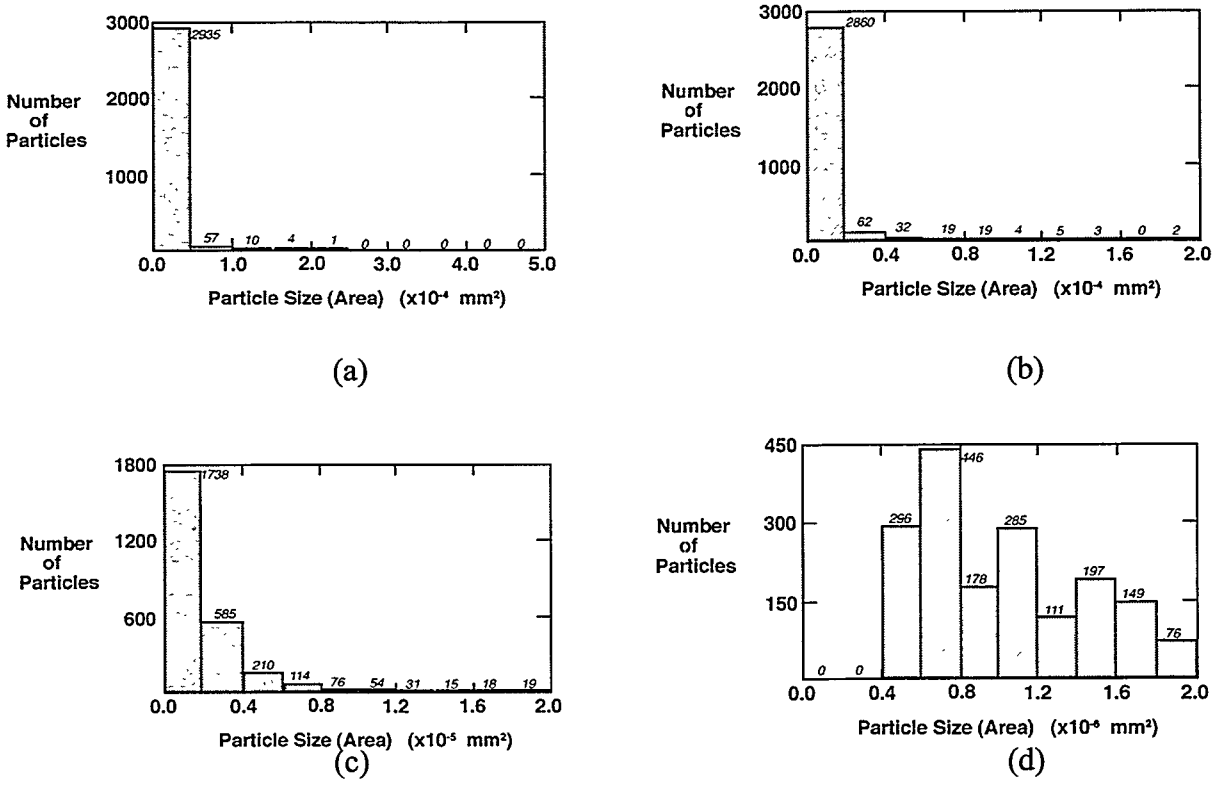


Figure 14. Histograms showing the distribution of Pb-rich phase size particles in one top-side fillet (D-1 position) of a 1/4W resistor solder joint from the (as-fabricated) baseline circuit boards. The particle size ranges per each histogram are: (a) 0-5×10^{-4} mm^2; (b) 0-2×10^{-4} mm^2; (c) 0-2×10^{-5} mm^2; and (d) 0-2×10^{-6} mm^2.

It is clear from the graphs in Figure 14 that the particle-size distribution is approximately lognormal. Given the types of statistical analyses performed on the data in this study, it was

assumed that the distribution was normal and represented by the mean and $\pm$ one standard deviation in any subsequent calculations of statistical significance testing.

The Pb-rich phase particle-size distribution data are listed in Table 5. Overall, the mean particle sizes ranged over nearly one order of magnitude, from a minimum of 1.9×10^{-6} mm^2 to a maximum 14×10^{-6} mm^2. Assuming that the particles were spherical in shape, these area measurements would correspond to particle diameters of 1.6 μm to 11 μm, respectively. It is known that as the number of measurements (i.e., data points) in the analysis decreases, the standard deviation will begin to increase. The increased data scatter will prevent the identification of statistically significant trends. Therefore, an ancillary study was performed to identify the behavior of the standard deviation as a function of the number of particles used in the count.

Table 5
Mean Pb-rich Phase-Particle Size (x 10^{-6} mm^2)
Fillet Locations #1or #2 in the Joint Cross Section-Baseline Test Vehicle
one standard deviation in parentheses

Component	Hole Interior	Fillet Location			
		Top		Bottom	
		#1	#2	#1	#2
1/4 W resistors (3 joints)	4.5 (11) 3.6 (8.8) 5.1 (20)	5.4 (15) 4.5 (15) 8.1 (50)	14 (150) 5.6 (23) 13 (150)	3.7 (11) 3.7 (9.5) 7.1 (85)	3.5 (8.9) 8.6 (99) 11 (130)
16-Pin Ceramic DIP (3 joints)	3.2 (6.0) 2.9 (5.3) 2.3 (4.0)	2.8 (4.4) 2.6 (5.3) 2.9 (4.7)	3.2 (4.6) 4.0 (6.4) 3.0 (5.5)	3.7 (8.2) 3.6 (7.0) 2.9 (5.3)	3.0 (5.6) 3.3 (6.1) 3.1 (5.6)
CK0 capacitors (5 joints)	2.9 (5.5) 5.1 (23) 3.2 (4.9) 2.9 (5.0) 2.5 (4.3)	3.1 (6.5) 5.6 (18) 2.5 (3.5) 3.0 (6.3) 3.7 (8.0)	3.7 (6.8) 4.1 (13) 2.7 (5.2) 3.1 (6.3) 2.0 (3.7)	---- ---- ---- ---- ----	---- ---- ---- ---- ----
1/2 W resistors (1 joint)	4.3 (13)	7.1 (35)	5.1 (17)	3.9 (7.9)	2.8 (6.1)
1/4 W resistors (2 joints)	3.1 (8.0) 4.2 (12)	4.9 (16) 5.3 (19)	3.6 (11) 4.8 (14)	3.1 (7.9) 3.3 (10)	2.5 (6.2) 3.0 (7.2)
TO18 transistors (2 joints)	2.6 (4.9) 1.9 (2.3)	4.1 (8.8) 2.3 (3.2)	3.6 (7.5) 2.5 (3.6)	---- ----	---- ----

Figure 15 is a plot of the standard deviation (S.D.) from each of the component types as a function of the number of Pb-rich phase particles evaluated in those respective sets. The particle-size data from all solder joints and solder-joint locations (fillets, top and bottom as well as the hole location) were used to compile the plot. The results in Figure 15 indicate that the standard deviation reached a minimum and remained there for particle counts in excess of approximately 3000.

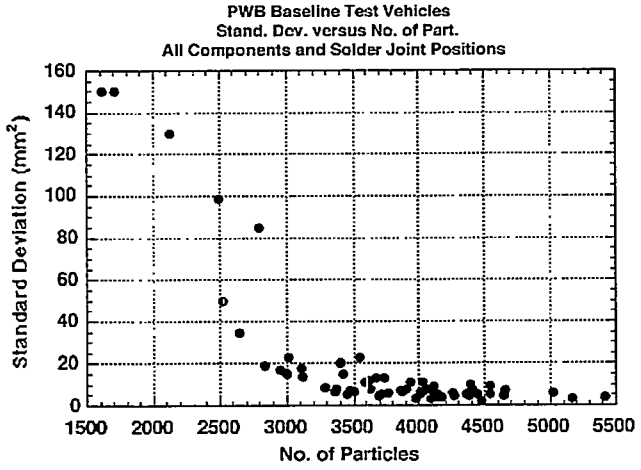


Figure 15. Plot of the standard deviation (S.D.) values as a function of the number of Pb-rich phase particles evaluated in a data set for *all* components (1/4 W resistors, CK0 capacitors, etc.), solder joints, and solder joint locations (fillets, top and bottom as well as the hole location) on the baseline test vehicle.

The analysis was next turned to observations of the individual solder joints. An investigation was performed to identify any statistically significant differences between the mean, Pb-rich phase particle sizes under the following criteria: (1) top-side fillet v. bottom-side fillet; (2) top-side or bottom-side fillet v. hole interior. The particle-size data, per solder joint and component category, were pair-wise analyzed to test the equivalence of their means. The statistical tests for evaluating the differences of mean particle sizes were based upon Equations 3 through 9. The data from the two "quadrants" representing the top-side of the joint, D1 and D2, were combined to represent the "top-side fillet"; likewise, the data representing the two quadrants, D3 and D4, of the bottom fillets of the joint were combined as the "bottom-side

fillet." When combined, the data from the two quadrants, as well as the individual data set of Pb-rich phase sizes from the hole interior, resulted in particle counts that surpassed the "3000 benchmark" noted above. The properties' data are summarized in Table 6.

Table 6
Mean Pb-Rich Phase-Particle Size (x 10^{-6} mm^2)
Both Fillet Quadrants per Top or Bottom Side are Combined-Baseline Test Vehicle
one standard deviation in parentheses

Component	Hole Interior	Fillet Location	
		Top	Bottom
1/4 W resistors (3 joints)	4.5 (11) 3.6 (8.8) 5.1 (20)	9.8 (90) 5.1 (19) 11 (100)	3.6 (9.8) 6.2 (112) 8.6 (106)
16-Pin Ceramic DIP (3 joints)	3.2 (6.0) 2.9 (5.3) 2.3 (4.0)	3.0 (4.5) 3.3 (5.8) 2.9 (5.2)	3.4 (6.9) 3.4 (5.5) 3.0 (5.5)
CK0 capacitors (5 joints)	2.9 (5.5) 5.1 (23) 3.2 (4.9) 2.9 (5.0) 2.5 (4.3)	3.4 (6.6) 4.8 (16) 2.6 (4.4) 3.0 (6.3) 2.9 (5.7)	--- --- --- --- ---
1/2 W resistors (1 joint)	4.3 (13)	6.1 (27)	3.4 (7.0)
1/4 W resistors (2 joints)	3.1 (8.0) 4.2 (12)	4.3 (13) 5.1 (16)	2.8 (7.0) 3.1 (8.7)
TO18 transistors (2 joints)	2.6 (4.9) 1.9 (2.3)	3.8 (8.2) 2.4 (3.4)	--- ---

A statistical analysis was performed on the data represented in Table 6. This evaluation began by determining whether significant differences existed between the mean Pb-rich phase particle sizes from among the various locations in the joints; that is, whether the Pb-rich phase size differed between the top-side fillets, the bottom-side fillets, and the solder inside of the hole barrel. The frequency by which that equivalence was observed versus the total number of trials appears in Table 7. Those data indicate that the top-side and bottom-side fillets were observed to have similar mean particle sizes in about one-half of the cases. The mean Pb-rich phase

particle size within the hole was generally not equal to that of the fillets, most often being the smaller of the two locations.

Table 7
Mean Pb-rich Phase-Particle Size (x 10^{-6} mm^2)
Equivalencies between Top Fillet, Bottom Fillet, and Hole Interior-Baseline Test Vehicle

Component	Joint	Comparison	
		Location	Equivalence
1/4 w resistors	3 joints	Top v. Hole Hole v. Bottom Top v. Bottom	0/3 1/3 2/3
16-Pin Ceramic DIP	3 joints	Top v. Hole Hole v. Bottom Top v. Bottom	0/3 1/3 2/3
CK0 capacitors	5 joints	Top v. Hole	2/5
1/2 W resistors	1 joint	Top v. Hole Hole v. Bottom Top v. Bottom	1/1 0/1 1/1
1/4 W resistors	2 joints	Top v. Hole Hole v. Bottom Top v. Bottom	0/2 0/2 0/2
TO18 transistors	2 joints	Top v. Hole	0/2

The difference of Pb-rich phase size between the fillets and hole interior was most pronounced with the first set of 1/4W resistor joints. The magnitude of the difference diminished with the DIP and CK0 package solder joints. Also, the Pb-rich phase size of the 1/4W resistor (first group) solder joints was generally greater than corresponding values for the DIP and CK0 components (Table 6).

A further evaluation of the results in Table 7 suggested that, as baseline data, the Pb-rich phase-size distribution parameters should be categorized according to component type and solder-joint location. The solder-joint location is top (component-side) fillet, hole interior, or bottom fillet. The data were so combined and are listed in Table 8.

In the analysis of the Pb-rich phase-size distribution, the total quantity of Pb-rich phase was measured from each image. This value was then compared to the nominal composition

expected from eutectic 63Sn-37Pb or near-eutectic 60Sn-40Pb solders. The image analysis procedure combines the particle footprint areas to compute an area percent of the Pb-rich phase.

Table 8
Mean Pb-rich Phase-Particle Size (x 10^{-6} mm^2)
by Solder Joint Location-Baseline Test Vehicle
one standard deviation in parentheses

Component	Hole Interior	Top Fillet	Bottom Fillet
1/4 W resistors (3 joints)	4.4 (1.4)	8.5 (73)	6.1 (64)
16-Pin Ceramic DIP (3 joints)	2.8 (2.3)	3.1 (5.2)	3.3 (6.0)
CK0 capacitors (5 joints)	3.3 (11)	3.3 (8.3)	-----
1/2 W resistors (1 joint)	4.3 (13)	6.1 (27)	3.4 (7.0)
1/4 W resistors (2 joints)	3.7 (8.0)	4.7 (12)	3.0 (7.9)
TO18 transistors (2 joints)	2.2 (1.6)	3.1 (6.1)	-----

In order to convert the area percent to a weight percent that is used to identify solder composition, the following procedure was used. It was assumed that *volume percent* is equal to the area percent [5]. This assumption is based upon the assumptions that the particles are randomly distributed within the matrix and that their shapes do not have a preferred orientation in any one direction. The conversion of the volume percent data to mass or weight percent is performed as follows: The volume percent of Pb (vol.%$|_{Pb}$) is converted into a volume of Pb, $V|_{Pb}$, by multiplying the volume percent by 100.

$$\text{Area \% Pb} = \text{vol.\%}|_{Pb} \Rightarrow V|_{Pb} = vol.\%|_{Pb} \, x \, 100 \quad . \tag{12}$$

Similarly, the volume of Sn, $V|_{Sn}$, is also computed. The mass of Pb, $m|_{Pb}$, and the mass of Sn, $m|_{Sn}$ are computed from these volumes by multiplying each by their respective densities, ρ_{Pb} and ρ_{Sn}.

$$m|_{Pb} = V|_{Pb}\, \rho_{Pb} \quad . \tag{13a}$$

$$m|_{Sn} = V|_{Sn}\, \rho_{Sn} \quad . \tag{13b}$$

The mass or weight percent of the Pb-rich phase is then computed from the following expression:

$$wt.\%|_{Pb} = m|_{Pb} / (m|_{Pb} + m|_{Sn}) = V|_{Pb}\, \rho_{Pb} / (V|_{Pb}\, \rho_{Pb} + V|_{Sn}\, \rho_{Sn}) \quad . \tag{14}$$

The weight percent and corresponding volume (area) percent correlations for the two commonly used Sn-Pb solders, along with that of the 50Sn-50Pb alloy, are:

Wt.%		**Vol.%**
63Sn-37Pb	**(eutectic)**	**72.6Sn-27.4Pb**
60Sn-40Pb	⇒	**70.0Sn-30.0Pb**
50Sn-50Pb		**60.9Sn-39.1Pb**

It is recognized from the Sn-Pb phase diagram that there is a finite solubility of Sn in the Pb-rich phase. Under the circumstances of rapid solidification, the Pb-rich phase will become supersaturated with Sn as the temperature drops. As a result, some Sn precipitates within the Pb-rich particles, forming small, white islands (Figure 16). The quantitative image analysis routine will detect those regions and identify them as Sn-rich phase. However, the Sn atoms that remain in solution in the Pb-rich phase will not be detected. The result of the undetected Sn is that the measured quantity of Pb-rich phase will be shifted to a higher value than is actually the

case. Unfortunately, the amount of Sn dissolved in the Pb-rich phase depends upon the cooling rate at the time of solder solidification, causing the amount of Sn in the Pb-rich phase to be quite variable. Therefore, it was assumed that the range of Sn contents in the Pb-rich phase will be *1 wt.% < Sn < 5 wt.%.* A value of *3 wt.%* was used to represent this range. The weight *fraction* of Sn in the Pb-rich phase is x. Thus, the actual or "corrected" value of the weight percent of Pb is given as:

$$\text{wt.\%Pb}\big|_{\text{corrected}} = (1\text{-x})\ \text{wt.\%Pb}\big|_{\text{measured}} \quad . \tag{15}$$

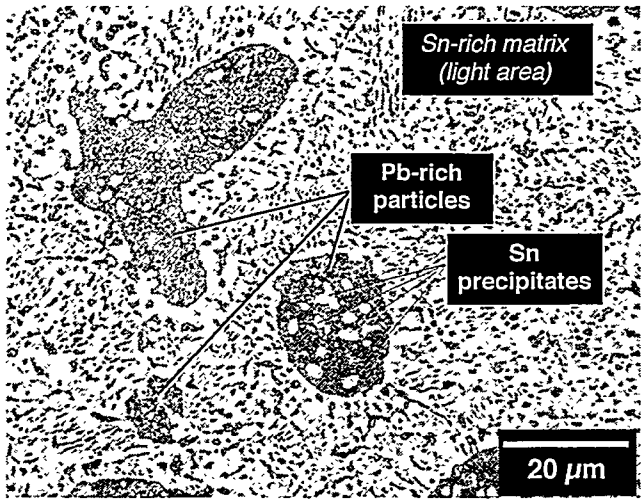


Figure 16. Optical micrograph of the Pb-rich phase in 62.5Sn-36.1Pb-1.4Ag alloy illustrating the precipitation of dissolved Sn as the light particles within the Pb-rich particles.

Table 9 shows the area percents and computed weight percents of total Pb-rich phase measured in the microstructures of the various baseline solder joints. The weight percents of Pb have been corrected for an assumed Sn content of 3 wt.%. The data are presented from measurements performed in the hole interior as well as in the fillets (top and bottom already combined). To within statistical error, there is no significant difference in the quantity of Pb-rich

phase between the fillet and hole locations; therefore, the two data sets were combined to form the last column.

Table 9
Area Percent (%) of Pb-Rich Phase Experimental Measurements and Computed Weight Percent (%)-3 wt.% Reduction for Dissolved Sn Content-Baseline Test Vehicle
one standard deviation in parentheses

Component	Hole Interior		Top and Bottom Fillet		Combined	
	area %	wt. %	area %	wt. %	area %	wt. %
1/4 W resistors (3 joints)	39 (3)	(47 (3)	45 (8)	53 (8)	44 (7)	52 (7)
16-Pin Ceramic DIP (3 joints)	28 (4)	35 (4)	31 (3)	38 (3)	30 (3)	37 (3)
CK0 capacitors (5 joints)	31 (8)	38 (8)	32 (5)	39 (5)	31 (6)	38 (6)
1/2 W resistors (1 joint)	38 (--)	46 (--)	37 (7)	45 (7)	37 (6)	45 (6)
1/4 W resistors (2 joints)	34 (4)	42 (4)	35 (2)	43 (2)	35 (2)	43 (2)
TO18 transistors (2 joints)	25 (6)	30 (6)	28 (5)	35 (5)	27 (5)	34 (5)

It is observed that the Pb-rich phase contents of the 1/4 W and 1/2 W wire wound resistors were significantly higher than a nominal 37 wt.% or 40 wt.% expected from the 63Sn-37Pb and 60Sn-40Pb solders, respectively. The 16-pin ceramic DIP, CK0 capacitor, and TO18 transistor component types had (corrected) Pb-rich phase contents that were commensurate with these solders. We hypothesized that the higher than expected Pb contents of the wire-wound resistor solder joints originated from the use of a high Pb coating on the component leads by the manufacturer. Although the leads were hot solder dipped at AS/FM&T prior to soldering the device onto the printed circuit board, some of the higher Pb coating may have been retained. The additional Pb in the lead coatings "contaminated" the solder-joint microstructure after fabrication, thus raising the latter's apparent Pb content.

The data in Table 9 indicate that the Pb-rich phase particle-size distributions may have been skewed for the 1/4 W and 1/2 W wire-wound resistor solder joints. A review of the data in Table 8 indicates that the higher Pb content of these joints also had an effect on the Pb-rich

phase-particle sizes. It is observed that the 1/4 W and 1/2 W resistors have *greater*, mean Pb-rich particle sizes than do the other components. In fact, the highest Pb content was demonstrated by the solder joints from the first group of 1/4 W resistors (Table 9), and was accompanied by the largest mean Pb-rich phase-particle size (Table 8). However, it is equally important to note that the different Pb contents among the joints did *not* significantly impact the measured intermetallic compound layer thicknesses as listed in Table 4.

A Pb-rich phase, "as-fabricated" solder joint baseline for use of the 63Sn-37Pb or 60Sn-40Pb solders was determined by the measurements taken from solder joints belonging to the ceramic DIP, CK0 capacitor, and TO18 transistor packages. Based on the observation that a minimal variation exists in the particle-size statistics across the respective joints (i.e., between fillet locations as well as the hole interior), the following values were used to establish the "as-fabricated" value: (1) ceramic DIP joint fillets, top and bottom; (2) CK0 capacitors, top fillets; and (3) TO18 transistors, top fillets. A weighted or "pooled" variance was computed to represent a standard-deviation parameter. The resulting baseline Pb-rich phase, mean-particle size was determined to be:

$$x_o = 3.2 \pm 6.5 \times 10^{-6}\ mm^2 \quad .$$

The value of x_0, 3.2×10^{-6} mm^2 was combined with the kinetics parameters determined by the aging experiments performed on the Sn-Pb/Cu couples, using temperatures of 70°C and 100°C. Figure 17 show the Pb-rich phase-particle size data. The kinetics equation for the particle area (mm^2) is given below:

$$x = 3.2 \times 10^{-6} + 1.47 \times 10^{-3}\, t^{0.32} \exp(-31000/RT) \quad . \qquad (16)$$

The units of the variable and parameters are:

1. x and x_o (mm^2);
2. 1.47 x 10^{-3}, (mm^2-$s^{1/n}$);
3. t, (s); (4) 31000, (J/mol);
4. R; (8.314 J/mol-°K), and (
5. T, (°K = °C + 273).

The 95% confidence intervals on the values of n and ΔH were ±0.09 and ±11000 J/mol, respectively.

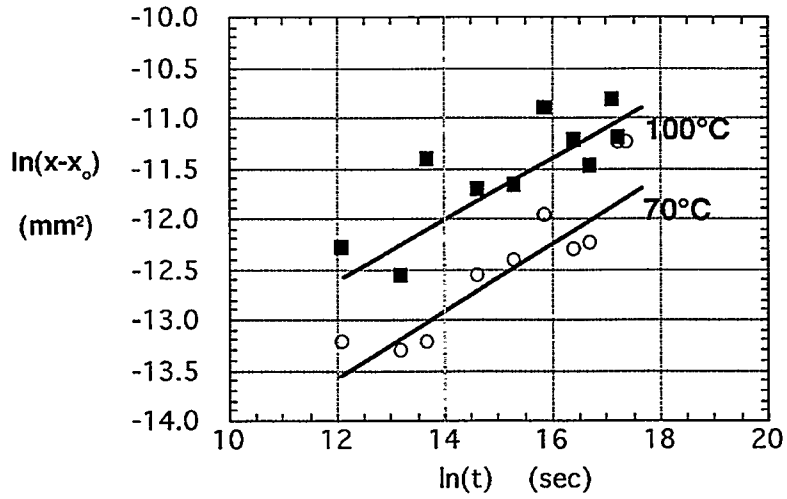


Figure 17. Graph of the mean Pb-rich hase-particle size from 63Sn-37Pb aged at temperatures of 70°C and 100°C and time periods of up to 400 days.

As noted above, the Pb-rich phase size determined from the selected components did not appear to vary significantly from among the top and bottom fillet locations as well as the hole location. However, such may not always be the case, depending on the particular package that is being soldering into place and the soldered operation, itself. Differences in package type, lead diameter, lead material, etc., can cause the solder to have different cooling rates at various locations within the joint structure. Nevertheless, the present study indicated that the ideal situation prevailed, in which the same Pb-rich phase-particle size was observed throughout the solder-joint structure. Therefore, any significant, non-homogeneity that may be observed in the Pb-rich phase mean particle size between different locations in a subject solder joint would be taken into account when determining the cumulative aging of the solder joint.

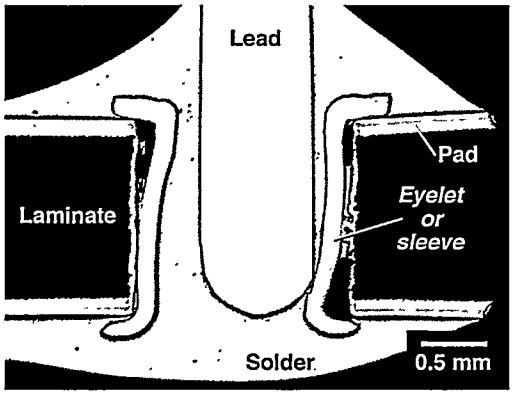
3.2 N57 Analysis

3.2.1 Solder Joint Qualitative (Defect) Analysis—Interconnect Circuit Board

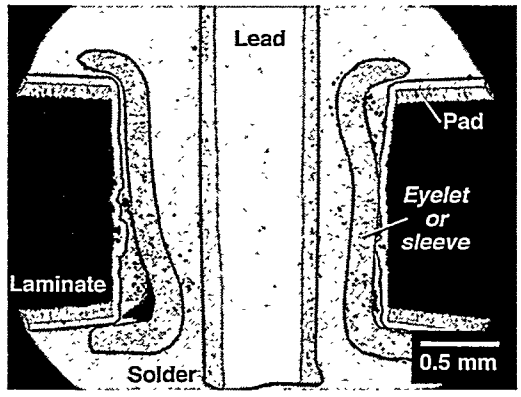
Prior to a quantitative analyses of the intermetallic compound layer thickness and Pb-rich phase particle distribution, a qualitative assessment was made of the interconnect circuit board solder joints. Recall that the circuit-board holes were constructed with the sleeve or eyelet structure (Figure 8). It was observed that the workmanship of the solder joints varied somewhat, even between solder joints on the same circuit board. Figure 18 illustrates representative micrographs of the types of defects observed in the joints. Those defects included:

(a) a solder joint (SA1126 connector) with fully formed fillets showing the typical concave geometry;
(b) a solder joint exhibiting full fillets, but having a convex or bulbous appearance that suggests an excess of solder was used to make it;
(c) a solder joint with a poorly formed fillet on the top-side of the lead; and
(d) solder joint with incomplete hole filling.

Some void formation was also observed in the joints. Generally, the voids were caused by entrapped air or flux volatiles; however, the morphology of a few voids did indicate a wettability problem with the eyelet wall surface. The voids did not appear to instigate further damage to the solder joint, and the signal transmission capability was not jeopardized with these defects.



(a)



(b)

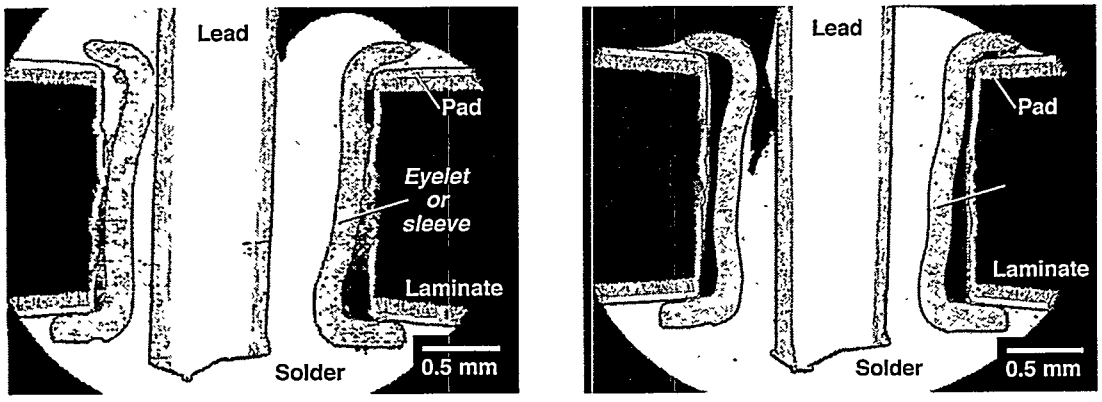


Figure 18. Micrographs representing the qualitative aspects of interconnect circuit board solder joints: (a) a solder joint (SA1126 connector) with fully formed fillets showing the typical concave geometry; (b) a solder joint exhibiting full fillets, but having a convex or bulbous appearance that suggests an excess of solder was used to make the joints; (c) a solder joint with a poorly formed fillet to one side of the lead; and (d) a solder joint with incomplete hole filling.

Past experience with the eyelet-hole configurations from dismantled hardware included observations of cracking in such solder joints [4]. Similar damage was also observed on the interconnect circuit board solder joints reviewed in the present study. Figure 19a presents an example of a solder joint showing cracks; higher magnification views are presented in Figs. 19b and 19c. The cracks generally remained in the fillet formed between the eyelet rim and the circuit-board land. The propensity for cracking was determined by counting the number of cracked solder fillet "quadrants" as examined from the photomicrographs. There are four quadrants viewed per picture, two for the top fillet and two for the bottom fillet. Seventeen solder joints were examined from segments #1 and #2, resulting in an assessment of 34 top-side quadrants and 34 bottom-side quadrants. It was determined that 35% of the top-side quadrants exhibited cracks, while 0% of the bottom-side quadrants showed crack formation. Additional examinations were made to segments #3, #4, and #5. This examination included nine solder joints, or 18 quadrants, on each of the top and bottom sides of the joints. The assessment revealed that 50% of top-side quadrants had experienced cracking, while 17% of the bottom-side quadrants showed the crack defect.

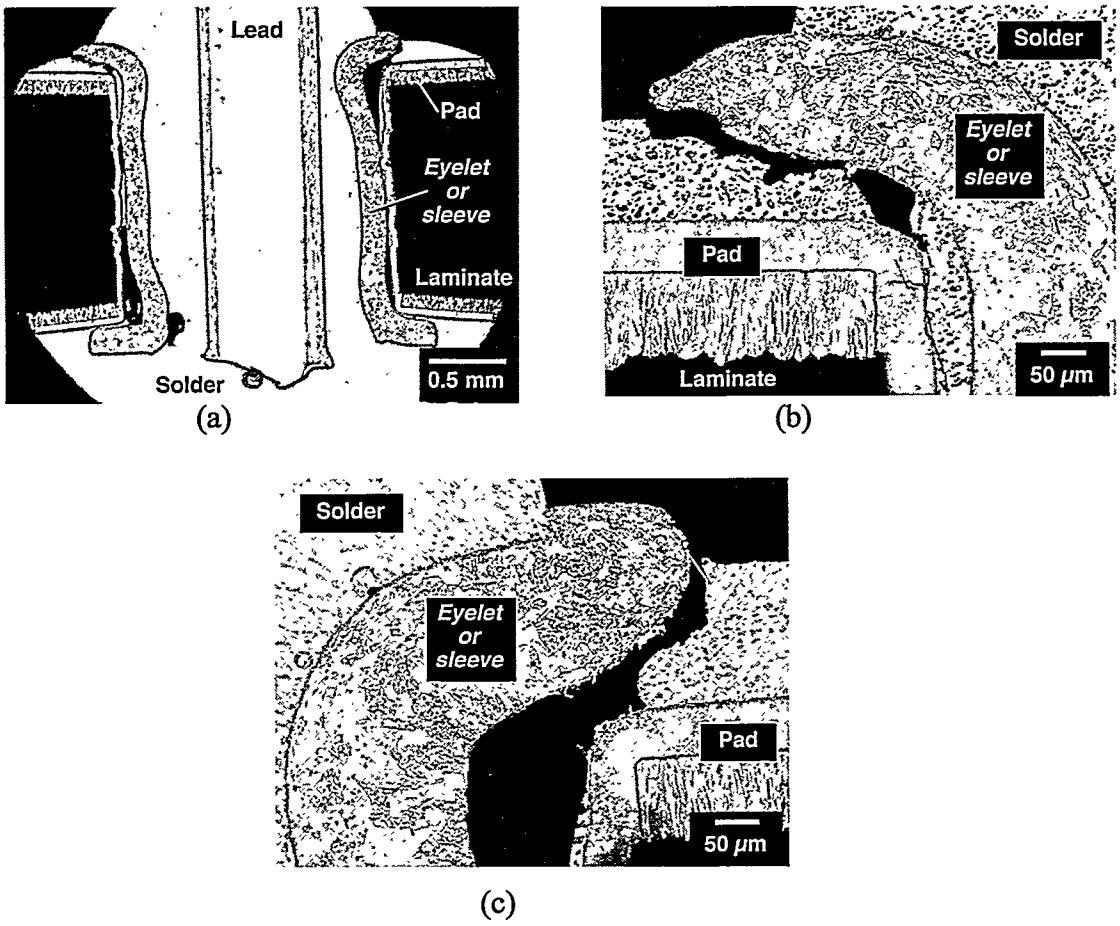


Figure 19. Optical micrographs show cracking in the fillet formed between the Cu eyelet and the circuit board bonding pad. (a) A low magnification view of the joint is shown; the cracks appear on the om-side filletts; (b) and (c) These are high magnification views of the cracks.

The source of the cracking defect was believed to be stresses/strains generated between the Cu sleeve and the printed circuit board laminate caused by a mutual thermal expansion mismatch as the product underwent temperature variations. A similar phenomenon was observed in the case of PIN diodes that are located in holes of circuit boards [6]. It was important to determine whether the cracking defect was a consequence of the relatively small, but more frequent temperature variations (ΔT) experienced by the component while in the stockpile. Under those circumstances, the defect would be considered as a consequence of *stockpile aging*. On the other hand, the cracking could have been caused by temperature excursions experienced during subsequent manufacturing processes. Such temperature variations occur over a relatively

few number of times, but they typically entail very large ΔT's. In this case, the cracks would be more suitably defined as manufacturing or "infant mortality" defects.

The computation was performed in the following manner. It was first assumed that fatigue damage to the solder was a consequence of the global thermal expansion mismatch between the Cu sleeve and printed circuit-board laminate, along a direction parallel to the axis of the hole. Local thermal expansion mismatches between the solder, printed circuit-board laminate, and Cu were neglected. Figure 20 shows a schematic diagram of the eyelet solder joint. We also assumed that the joint was formed by a 50 μm thick volume of solder. The remaining solder that completed the fillet was assumed to be rigidly attached to the underlying printed circuit-board laminate. Shear deformation was introduced into the solder joint "volume" by the relative movement between the eyelet edge and the circuit board over the nominal distance of the board thickness (1.98 mm). It was also assumed that all of the deformation took place at either the top-side fillet or the bottom-side fillet; that is, the damage to the solder was not partitioned between both the top- and bottom-side fillets.

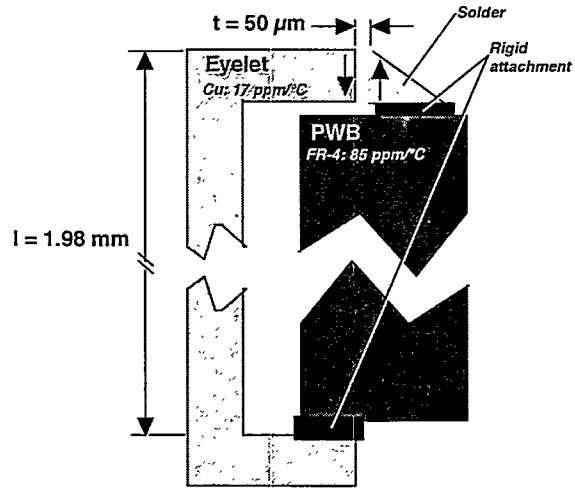


Figure 20. Schematic of the eyelet solder joint as used to compute the latter's fatigue life.

The Cu eyelet and the "z-axis" dimension of the circuit board have vastly different thermal expansion coefficients, α. The eyelet was made of Cu and considered to have a thermal expansion coefficient of 17 x 10^{-6} /°C [7]. The circuit board was made of epoxy resin plus glass

fiber composite [8]. A tabulated value of the z-axis expansion of the epoxy-glass laminate is 85 x 10^{-6} /°C [9]. Over the nominal distance, l, between the top- and bottom-side fillets (1.98 mm), the expansion, Δl_{Cu}, of the eyelet (Cu) and that of the printed circuit board (PWB), Δl_{PWB}, due to a temperature change, ΔT, are given by the products:

$$\Delta l_{Cu} = l \, \alpha_{Cu} \, \Delta T \quad . \tag{17a}$$

$$\Delta l_{PWB} = l \, \alpha_{PWB} \, \Delta T \quad . \tag{17b}$$

The difference, Δx, between the values of Δl_{Cu} and Δl_{PWB} accounts for the strain in the solder and is computed as:

$$\Delta x = \Delta l_{Cu} - \Delta l_{PWB} \quad . \tag{18}$$

The shear strain introduced into the solder, γ_T, where "T" indicates that "total" strain is given by:

$$\gamma_T = \Delta x / t \quad , \tag{19}$$

where t is the thickness of the joint that was assumed to be 50 μm. The fatigue damage in the solder joint is determined by the magnitude of the irreversible plastic shear strain component, γ_p, which is one component of the total shear strain, γ_T; the other component is the elastic or recoverable strain, γ_e. Thus, the total shear strain can be written as:

$$\gamma_T = \gamma_p + \gamma_e \quad . \tag{20}$$

Therefore, an accurate prediction of the fatigue life of the solder requires that the plastic shear-strain component be isolated from the total shear strain. This is done by computing the

elastic shear-strain component and subtracting that value from the total shear strain. The elastic shear strain is computed from the expression below:

$$\gamma_e = \tau_y / G \quad , \tag{21}$$

where τ_y is the (shear) yield stress of the solder and G is the shear modulus of the solder. The yield stress in shear was determined from the tensile yield stress, σ_o, and the Von Mises criterion [10]:

$$\tau_y = \sigma_o / \sqrt{3} \quad . \tag{22}$$

The tensile yield stress of the solder (or for that matter, the yield stress of any material) is strongly dependent upon the temperature. However, for the sake of this computation, the room temperature value will be assumed to represent the entire stockpile temperature range. That tensile yield stress is 2340 psi [11]. The computed value of τ_y is 1300 psi. The shear modulus, G, was computed from the elastic modulus, E, and Poisson's ratio, ν, by way of the following expression [12]:

$$G = E / [2 (1 + \nu)] \quad . \tag{23}$$

As was the case with the yield stress, the elastic parameters of E and ν are also dependent upon temperature. Therefore, average values were selected as being those measured at room temperature, 5.14×10^6 psi [13] and 0.4, respectively [14]. The resulting value of G was computed to be 1.84×10^6 psi. The elastic strain computed from Equation 14 is 7.1×10^{-4}. Thus, the plastic shear strain, γ_p, is determined by the equation:

$$\gamma_p = \gamma_T - 7.1 \times 10^{-4} \quad . \tag{24}$$

Plastic strain accumulates in the solder joint with each thermal cycle. Isothermal fatigue experiments performed by H. Solomon indicated similar fatigue behavior over the temperature range of –55°C to 135°C [15]. As a consequence, it was inferred that non-isothermal (or thermomechanical) fatigue damage to the solder per cycle, γ_p, and the number of cycles-to-failure, N_f, could be quantitatively expressed by a single equation:

$$(\gamma_p)\, N_f^{\alpha} = \theta \tag{25}$$

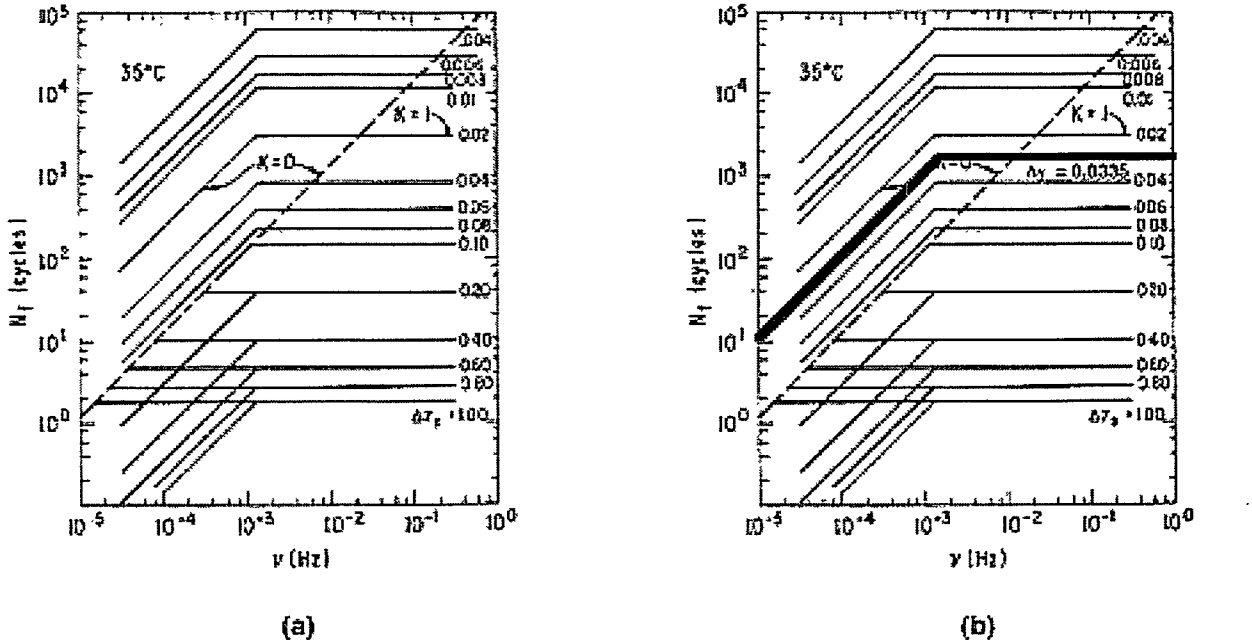
where the constants α and θ were experimentally determined in the cited study [15]. The criterion used to determine those values was the experimental observation of a 50% drop in the load bearing capacity of the solder during testing at a frequency of 0.3 Hz. It was experimentally observed in the cited work that a 50% load drop corresponded to a considerable amount of solder deformation and fatigue crack growth in the tested solder joints. The full equation is given as:

$$(\gamma_p)\, N_f^{0.51} = 1.14 \qquad \textit{(50\% load drop)} \quad . \tag{26}$$

Because this equation was observed to be valid over isothermal fatigue test temperatures of –50°C to 125°C, it is assumed to represent non-isothermal, thermal mechanical fatigue over a similar temperature regime.

Equation 26 was determined from fatigue tests performed at a frequency of 0.3 Hz. It has been observed that the frequency of testing has a significant impact on the cycles-to-failure for a given γ_p. Slower frequencies tend to increase the extent of fatigue damage and thus, reduce the number of cycles to failure of the joint. This dependence is shown graphically in Figure 21 [15]. At frequencies of less than approximately 10^{-3} Hz, there is a substantial drop in the fatigue life as the cycle frequency decreases further. The lower frequency regime would include the typical environmental test cycle having limits of –55°C and 125°C, temperature ramps of 6°C/min and

15 min hold times, which has a computed frequency of 1.85 x 10^{-4} Hz. A daily cycle of night-day temperature extremes that occurs over 24 hours has a frequency of 1.15 x 10^{-5} Hz.



(a) (b)

Figure 21. (a) Graph of the effect of cycle frequency on the number of cycles to failure for fatigue strain γ. (b) Graphical interpretation of the number of cycles to failure, given a one day cycle (1.2x10^{-5} Hz) and a plastic strain of 0.0335.

The above analysis tools were used to determine whether the cracking observed in the solder joints would be a consequence of long-term aging processes, or reflected an infant mortality phenomenon that occurred during subsequent manufacturing process or shortly after delivery of the components.

Case I: Daily temperature cycles, 15°C – 30°C: This computation is based upon temperature variations that would hypothetically occur in a storage environment. It was presumed that, based upon observations of the solder joints, damage only occurred at the top of the joint. Also, the thermal expansion mismatch played along the entire thickness of the hole (1.98 mm). Equations 17a and 17b were solved:

$$\Delta l_{Cu} = 2.55 \times 10^{-4} \text{ mm} \quad .$$

$$\Delta l_{PWB} = 2.00 \times 10^{-3} \text{ mm} \quad .$$

The difference in the displacements, $\Delta x = \Delta l_{PWB} - \Delta l_{Cu}$, was computed to be:

$$\Delta x = 1.75 \times 10^{-3} \text{ mm} \quad .$$

For a gap of thickness, t = 0.051 mm, the total shear strain in the solder was:

$$\gamma_T = \Delta x / t = 0.0342 \quad .$$

The plastic shear strain component was:

$$\gamma_p = \gamma_T - 7.1 \times 10^{-4} \quad .$$

$$\gamma_p = 0.0335 \quad .$$

It is interesting to note that nearly all of the total shear-strain component is plastic shear strain; the elastic component make up only a small percentage (2%) of the total strain. In the event that the frequency effect is ignored, then the value of N_f is calculated from Equation 26 to be:

$$N_f = 1008 \text{ cycles} \qquad (50\% \text{ load drop})$$

Using the graph in Figure 21a, the number of cycles is determined from a maximum frequency of one day ($\nu = 1.2 \times 10^{-5}$ Hz); the graphical interpretation is shown in Figure 21b. The number of cycles is:

$$N_{f,\nu} \sim 10 \text{ cycles} \quad .$$

Given the uncertainty in the frequency compensated correction, let it be assumed that the two values, N_f and $N_{f,\nu}$, provide suitable limits that define a cycles-to-failure range: $10 < N < 1008$

for this temperature cycle. This range would predict a maximum time to solder joint failure (1008 cycles) of 2.76 years and a median failure time of 1.39 years (509 cycles). Both instances would still be considered as infant mortality losses rather than aging-related failures, since the actual lifetime was 35 years. Moreover, the failures will have already occurred in units designated for further service in the stockpile; no further failures would be expected during lifetime extension.

Case II: Soldering cycle, 183 °C - 25 °C: The parameters are similarly calculated as was done above:

$$\Delta l_{Cu} = 5.30 \times 10^{-3} \text{ mm} \quad .$$
$$\Delta l_{PWB} = 2.10 \times 10^{-2} \text{ mm} \quad .$$

The difference is the displacements, $\Delta x = \Delta l_{PWB} - \Delta l_{Cu}$, is:

$$\Delta x = 1.56 \times 10^{-2} \text{ mm} \quad .$$

For a gap of thickness, t = 0.051 mm, the total shear strain in the solder is:

$$\gamma_T = \Delta x / t = 0.307 \quad .$$

The plastic shear-strain component is:

$$\gamma_p = \gamma_T - 7.1 \times 10^{-4} \quad .$$

$$\gamma_p = 0.306 \quad .$$

The cycles-to-failure are listed below. The frequency compensation, which was based on a heating/cooling cycle of 30 s, did not appreciably alter the already low-fatigue life.

$N_f = 13$ cycles (50% load drop)

$N_{f,\nu} \sim 13$ cycles ($\nu = 0.033$ Hz)

Although the solder joint would not have been exposed to 13 such reflow cycles, the results indicate that a significant degree of damage would have already occurred to the solder in the joint simply from the cool-down step of a single soldering process or the heating/cooling cycle of an additional soldering (rework) process. This calculation further substantiates the scenario that the cracking observed in the eyelet solder joints was an infant mortality failure that occurred either at the time of manufacture, during next assembly operations (including any qualification testing), or shortly after initial introduction into the stockpile. No further cracking would be expected in this solder-joint design during lifetime extension in the stockpile.

Loss of electrical functionality would not have occurred as a result of cracking in the solder fillet formed between the eyelet and the circuit board bond pad. As can be seen in Figure 19, the hole walls were electroplated with Cu, thus allowing them to provide a redundant conduction path between the top and bottom pads/traces of the printed circuit board. Careful observation of the Cu plating on the hole walls did not reveal defects that would significantly deteriorate that signal transmission capability.

A qualitative survey was also performed on the SA1126 connector solder joints that were made to the junction board. The contact pins were made of low-expansion, Fe-based alloy; they appeared to have a Ni-plated layer as per the product specification [16]. Figure 22 shows an optical micrograph of one such joint. Generally, the joints showed excellent fillet formation on both sides of the circuit board. Wettability of all surfaces was excellent; voids were not observed; and, there were no significant workmanship defects. As anticipated by the ample supply of solder covering the eyelet on both top and bottom surfaces, the fillet cracking was *not* observed in any of the sectioned joints. However, a second form of damage was noted—a lifting of the Cu bonding pad from the underlying circuit board laminate. High-magnification optical micrographs are shown in Figure 23 that provide views of the pad/laminate interface per each of the four fillet quadrants from the solder joint in Figure 22. The micrographs illustrate the varying degrees of cracking and/or separation between the pad and the laminate. It is noted that the actual failure path was in the epoxy component of the laminate composite near the interface with the Cu pad.

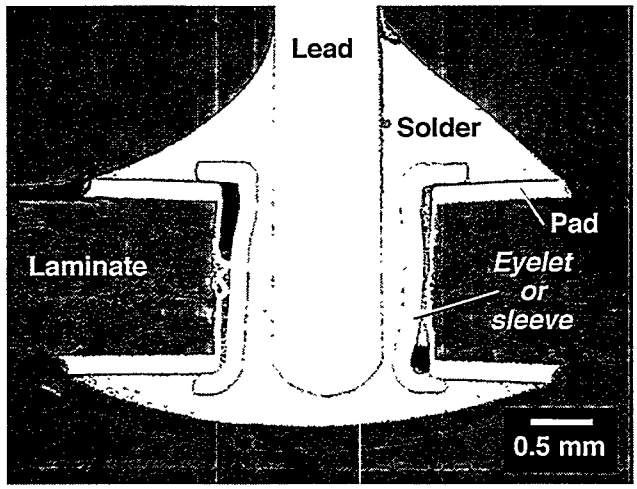


Figure 22. Solder joint illustrating the microstructure of those used to attach the SA1126 connector to the junction board.

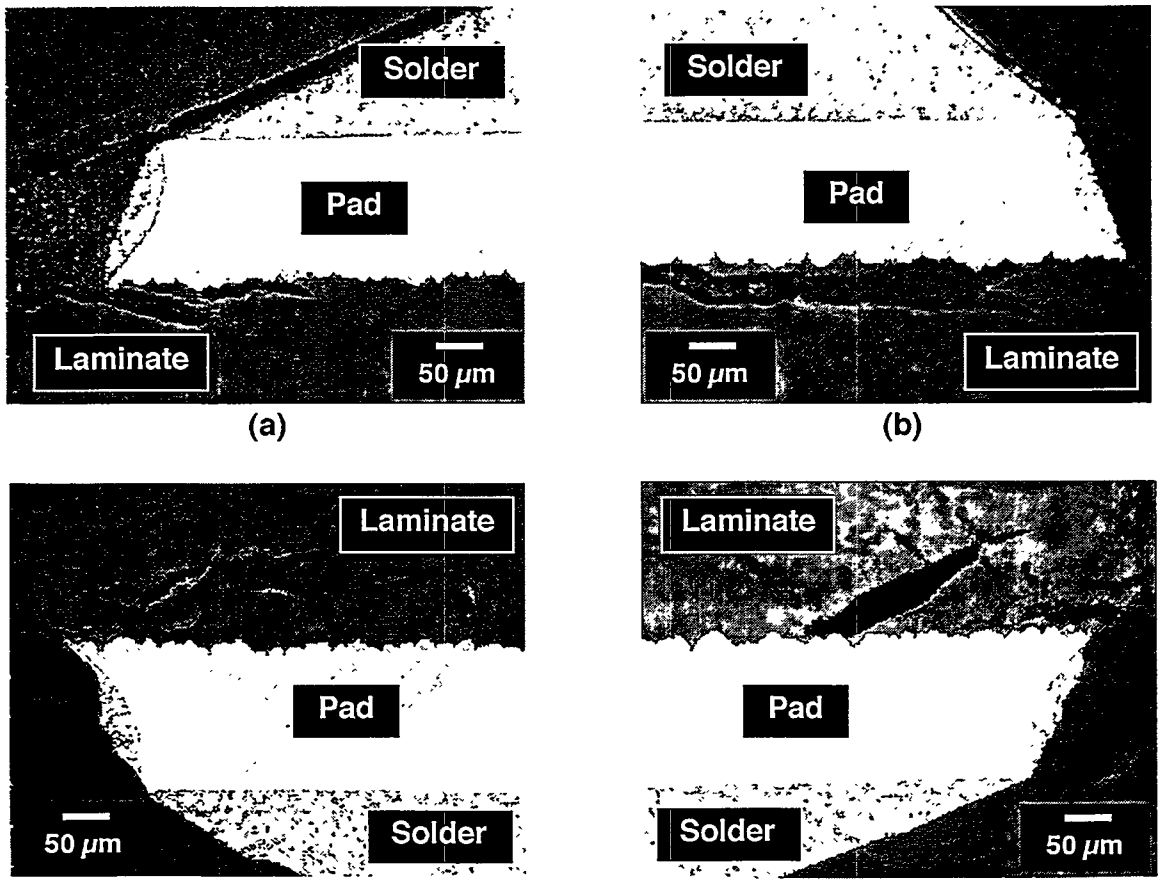


Figure 23. High magnification optical micrographs of the Cu bonding pad/laminate interface of the soldering joint in Figure 22. Each micrograph shows varying degrees of cracking and/or separation near the interface between the pad and the laminate.

A semiquantitative analysis was performed to determine the extent of the pad/laminate failure. Besides noting the occurrence of a crack, the lengths of cracks were also evaluated. Six solder joints were examined. A crack length was assigned to each of the four quadrants of a joint (two on the top side and two on the bottom side) as viewed from the optical micrographs. Cracks were found in 12 of 24 quadrant views, or 50%. Fifty-eight percent of the top-side quadrants exhibited Cu pad/laminate separation, while only 33% of the bottom-side quadrants exhibited the defect. The crack lengths ranged from about 10% to 50% of the radial distance, starting at the outer edge of the pad and progressing to the center edge at the lip of the hole. We did not observe a *complete* separation between the pad layer and the laminate in any of the cases.

Several potential sources of the pad/laminate-interface damage were identified. The most predominant cause of pad/laminate damage is its overheating during a hand-soldering operation. However, overheating causes the heat-sensitive epoxy to melt rather than form sharp cracks. The Cu pad then separates from the laminate. The source of the observed damage was more likely a mechanical overload applied to the joint. Such a condition would result in sharp cracks that propagate through both the epoxy and network of glass fibers as can be noted in Figure 23. Mechanical stresses on the joints would arise from insertion and removal activities of the mating cable assembly. Finally, thermomechanical fatigue was not a likely cause of this failure mode because under such stress/temperature environments, the failure remains in the solder of through-hole joints; pad lifting is not generally observed in this circumstance.

3.2.2 *Intermetallic Compound Layer Growth—Interconnect (Junction) Circuit Board Solder Joints*

The intermetallic compound layer thickness was measured for leaded component solder joints on the interconnect circuit board (1433983-6, BBN-2912-H4) as well as solder joints that attached the SA1126 connector to that board. The leaded component solder joints will be examined at this time. As noted earlier, three segments were cut away from the junction board and had the following respective number of solder joints cross-sectioned for evaluation: #3, 3 joints; #4, 4 joints; and #5, 2 joints. Table 10 is a summary of the intermetallic compound layer

thickness values for each of the leaded components, through-hole joints on the interconnect board, taken at the pad (F) and interior hole (E) locations. Only the Cu_6Sn_5 stoichiometry was observed to have formed at the interface.

Table 10
Intermetallic Compound Layer Thickness (μm)
Locations: Hole (E) and Pad (F)-N57 Junction (Interconnect) Circuit Board
one standard deviation in parentheses

Segment	Solder Joint	Hole (E)	Pad (F)
#3	#1	1.14 (1.02)	1.27 (0.48)
(3 joints	#2	0.86 (0.42)	1.26 (0.73)
	#3	1.23 (0.64)	1.14 (0.64)
#4	#1	0.86 (0.43)	0.88 (0.38)
(4 joints)	#2	0.84 (0.74)	0.58 (0.49(
	#3	1.30 (0.80)	0.50 (0.16)
	#4	0.64 (0.42)	0.59 (0.23)
#5	#1	0.74 (0.26)	0.58 (0.31)
(2 joints)	#2	0.82 (0.34)	1.03 (0.34)

A statistical analysis (t-test) was performed to determine the equivalence of the mean thickness values between the hole-interior location (E) and the pad location (F) of the joints. In eight of the nine joints that were examined, the two intermetallic compound layer thickness values were statistically equal. This observation allows the following conclusion to be drawn. The intermetallic compound layer was *not* thicker at the hole wall than it was at the pad surface (F). The hole walls either had an equivalent or reduced thickness of the intermetallic compound layer depending upon the degree to which the section was off of the center-axis of the hole (Figure 12). Further reference to the intermetallic compound layer thickness of the solder joints will be made to that value determined on the pad (F).

There was no particularly unique trends in layer thickness from among the three sections of circuit board that were evaluated (i.e., #3, #4, and #5). Therefore, the intermetallic compound layer thicknesses from each of the three segments of circuit board were combined. The following computed value represents leaded joints on the interconnect circuit board:

$$x = 0.87 \pm 0.53\ mm\ .$$

This layer thickness value shows that some growth had occurred in the joint, when compared with the baseline value equal to 0.714 $\pm$ 0.269 μm. It was assumed that the part had been in the stockpile for 35 years (1.104×10^9 s). The values of the intermetallic compound layer thickness, x, the initial thickness, x_o, and time, t, were applied to Equation 11, reproduced as Equation 27 below, in order to calculate the cumulative aging temperature that the solder joints experienced while in storage:

$$x = 0.714 \times 10^{-6} + 3.265 \times 10^{-3} t^{0.58} \exp(-52200/RT) \quad (27)$$

That cumulative temperature value was computed to be: *12°C (54°F)*. This temperature is certainly representative of the anticipated environments that this unit would have experienced in laboratory or plant storage and confirms that minimal aging had occurred to the joints.

3.2.3 *Intermetallic Compound Layer Growth—SA1126 Connector/Interconnect Circuit Board Solder Joints*

The intermetallic compound layer thickness was also measured on the solder joints made to the pins of the SA1126 connector. The measurements were performed at two pad (F) locations—one on the top side and the other on the bottom side. There was no significant differences between the values measured at the two sites. Therefore, the values from the two locations were combined for each of the six solder joints. Those values and $\pm$ one standard deviation, were:

(a) 0.75$\pm$0.49 μm,
(b) 0.89$\pm$0.31 μm,
(c) 0.88$\pm$0.42 μm,
(d) 0.95$\pm$0.36 μm,
(e) 0.96$\pm$0.57 μm, and
(f) 0.71$\pm$0.27 μm.

An overall average thickness was determined from these values; a weighted standard deviation was also computed from the measurement values. The layer thickness that represented the SA1126 connector solder joints was:

$$x = 0.86 \pm 0.28\ \mu m \ .$$

This value is very similar to that computed for the leaded-solder joints on the interconnect circuit board, albeit the data scatter was somewhat lower in the case of the SA1126 joints. The mean thickness represents an effective, cumulative aging temperature of *12°C (54°F)* and further confirms that minimal thermal aging had occurred to the joints.

3.2.4 Pb-Rich Phase Particle-size distribution—InterconnectCircuit Board Solder Joints

The Pb-rich phase particle-size distribution was determined for both the leaded solder joints made to the interconnect circuit board as well as the SA1126 connector joints made to the same circuit board. The leaded interconnects will be examined in this section. As noted above, a single measurement was performed on one of the two solder fillet quadrants viewed at the bottom side of the joint; the site was designated "G." Table 11 lists the values of the mean particle size (area), the standard deviation, the number of particles used in the analysis, and the area percent that is the Pb-rich phase. An overall, mean area percent of Pb-rich phase was computed to be 28.7±2.9%. This area percent corresponds to a weight percent value of 39% that, when corrected for the 3% Sn in solid solution, gives a value of 36%, confirming that the 63Sn-37Pb or 60Sn-40Pb solders had been used in the assembly operation.

Table 11
Pb-Rich Phase Particle-size distribution Parameters
Location: Bottom-Side Fillet(G)—N57 Junction (Interconnect) Circuit Board

Segment	Solder Joint	Mean Size (mm^2)	St. Dev. (mm^2)	No. of Particles	Area %
#3	#1	2.50×10^{-6}	4.64×10^{-6}	1058	25.4
(3 joints)	#2	2.68×10^{-6}	$5.71 \times 10^{-}$	1119	28.8
	#3	4.59×10^{-6}	8.91×10^{-6}	704	31.0
#4	#1	3.50×10^{-6}	7.81×10^{-6}	871	29.2
(4 joints)	#2	3.19×10^{-6}	5.73×10^{-6}	983	30.1
	#3	4.04×10^{-6}	9.14×10	843	32.7
	#4	$4.60 \times 10^{-}$	9.19×10^{-6}	673	29.7
#5	#1	6.46×10^{-6}	11.7×10^{-6}	393	24.4
(2 joints)	#2	2.36×10^{-6}	5.18×10^{-6}	1177	26.7

Using the Student's t-test, pair-wise comparisons were made of the equality of the mean particle size between joints within each of the three segments. In the first group of solder joints (segment #3), the three pairings produced only one instance of equality (1/3); the second group (segment #4) resulted in three of six pairings (3/6) having equality; the third group (segment #5) did not show an equality in the only possible pairing. Therefore, of a total of 10 pairings, equality was observed in four of those ten, or 40% of the cases. This evaluation establishes the degree of joint-to-joint variability in mean Pb-rich phase size that can be encountered among solder joints.

In the next analysis, the Pb-rich phase-size measurements from all of solder joints were combined per each segment. The statistical data are recorded in Table 12. Subsequent t-test evaluations determined that only one of the three pairings (#3 versus #4) was shown to have equal mean particle sizes. Under the premise that all of the circuit-board segments were equally representative of the junction board as a whole, the three data sets in Table 12 were combined; the resulting statistical data are listed in Table 13. The mean Pb-rich phase-particle size was calculated to be:

$$x = 3.83 \pm 11 \times 10^{-6}\ mm^2 \quad .$$

Table 12
Pb-Rich Phase Particle-size distribution Parameters
Summary per Segment—N57 Junction (Interconnect) Circuit Board

Segment	Solder Joint	Mean Size (mm^2)	St. Dev. (mm^2)	No. of Particles	Area %
#3	3 solder joints	3.26×10^{-6}	15.0×10^{-6}	2881	28.4
#4	4 solder joints	3.83×10^{-6}	$7.94 \times 10^{-}$	3370	30.4
#5	2 solder joints	4.41×10^{-6}	7.37×10^{-6}	1570	25.6

Table 13
Pb-Rich Phase Particle-size distribution Parameters
Summary per Combined Data—N57 Junction (Interconnect) Circuit Board

Segment	Solder Joint	Mean Size (mm^2)	St. Dev. (mm^2)	No. of Particles	Area %
All	9 solder joints	3.83×10^{-6}	11.0×10^{-6}	7821	28.1

The through-hole solder joints on the interconnect board did not exactly resemble the configurations of the devices listed as the baseline data in Table 8. Nevertheless, it was assumed that the later results would provide an adequate value of x_o for use in Equation 16. The mean Pb-rich phase-size values were combined from the following devices: the 16-pin CDIP, CK05, and the TO18 solder joints. The mean Pb-rich phase-particle size, which was computed from the fillet data of those components, was 3.2×10^{-6} mm^2. This baseline value, along with the overall mean Pb-rich phase-particle size of 3.83×10^{-6} mm^2 were introduced into Equation 16, assuming that the part had been in the stockpile for 35 years (1.104×10^9 s). Equation 16 is reproduced below as Equation 28:

$$x = 3.2 \times 10^{-6} + 1.47 \times 10^{-3} t^{0.32} \exp(-31000/RT) \quad (28)$$

The cumulative aging temperature was *-14°C (6°F).* Since the radar was not stored under sustained subfreezing temperatures, the Pb-rich phase size (and cumulative temperature) indicates that no significant aging had taken place under the laboratory environment.

The cumulative aging temperature calculated from the intermetallic compound layer thickness "metric," 12°C (54°F), and that computed from the Pb-rich phase-particle size, -14°C (6°F) indicates that a minimal extent of aging had taken place. Also, these cumulative temperatures were well below those of expected laboratory environments in which this unit was held. This result is likely a consequence of a small, albeit finite, difference between the *actual* baseline value of the respective metrics, which were not documented 35 years ago, but determined from the present-day baseline values described above (x_o). This difference will have a greater impact on the predicted aging condition when a very limited degree of aging results in

relatively small changes to the intermetallic compound layer thickness and/or Pb-rich phase-particle size.

3.2.5 *Pb-Rich Phase-Particle-Size Distribution—SA1126 Connector/Interconnect Circuit Board Solder Joints*

The Pb-rich phase-particle size of the SA1126 connector solder joints made to the interconnect board was evaluated. Six solder joints were analyzed. The Pb-rich phase particle distribution was determined in each of the four quadrant views of the solder joint fillets. The two sections of the top-side fillet were labeled A and B, and the two bottom-side fillet quadrants, were labeled C and D. This delineation of the solder-joint locations was made in order to determine, through the combined F-test (equivalence of variances) and Student's t-test (equivalence of means), whether there were significant variations in the Pb-rich particle sizes between the top and bottom sides of the joint. (Recall that this analysis could not be performed on the leaded, interconnect board solder joints because particle-size data were taken from only one location—the bottom-side fillet.)

First, the pair-wise comparison technique was used to check the equivalence of the mean Pb-rich phase-particle size from the two quadrants of the *same* side (top or bottom) of the joint. Interestingly enough, equivalence between sites A and B occurred only 60% of the time, while on the bottom side, the two fillet locations C and D had equal mean particle sizes in 80% of the pair-wise comparisons. It was assumed that the solder joints were made by soldering from the bottom (non-component) side of the printed circuit board as the top side would be made inaccessible by the connector structure. Reduced thermal gradients would have been expected in the bottom-side fillets that form last, thus allowing for a more uniform cooling rate and subsequent microstructure there. In the event that this difference in particle-size distribution is retained through the lifetime of the joint, then a possible technique may be developed whereby the location of the soldering operation can be identified from the statistical uniformity of the Pb-rich phase-particle size in the respective fillet locations.

A clear difference in the mean particle size was observed when the top-side solder joint microstructure was compared to that on the bottom side of the joint. In 16 out of 20 pair-wise comparisons (four per joint: A vs. C, A vs. D, B vs. C, and B vs. D for a total of five solder joints), unequal mean particle-size data were observed. Furthermore, of those 16 instances of inequality, 15 were the result of the bottom-side fillets having a larger particle size than did the top side. This latter observation indicates that the fillets formed in the solder joint at the location at which the soldering operation was performed had a slower cooling rate than did the top-side fillets away from the soldering iron. The data per individual quadrants from the two top-side fillet views were combined together as were the data from the two bottom-side fillet quadrants. The mean and ("pooled" or weighted) standard deviation of the Pb-rich phase particle-size distributions were:

Top fillets: Mean, 12.8×10^{-6} mm^2
Standard deviation, 27.6×10^{-6} mm^2.

Bottom fillets: Mean, 21.0×10^{-6} mm^2
Standard deviation, 42.9×10^{-6} mm^2.

The area percent of Pb-rich phase present in the examined microstructure was similarly analyzed. There did not appear to be any distinguishing trends in this parameter between the top-side fillets and the bottom-side fillets. Therefore, the data were combined from the top and bottom fillets per each of the five solder joints; those area percent values were: (1) 29.3, (2) 25.8, (3) 30.5, (4) 29.5, and (5) 31.3. It can be observed that the percents were very consistent among the joints. Thus, these values are combined to form an overall mean for the SA1126 connector solder joints of 29.3 area %. The corresponding weight percent value is 39.2 wt.%. Correcting for the assumed 3 wt.% Sn content in the Pb-rich phase results in a value of approximately 36 wt.%, implying the use of the eutectic 63Sn-37Pb solder to manufacture the joints.

The baseline, Pb-rich phase size of 3.2×10^{-6} mm^2 was used to perform the cumulative aging temperature computation for both the top-side and bottom-side fillets, separately. The cumulative temperatures (assuming a 35-year storage lifetime) were 46°C (115°F) for the top-

side fillets and 64°C (147°F) for the bottom-side fillets. These temperatures exceed conditions expected in laboratory or plant storage and are in disagreement with that predicted by the intermetallic compound layer measurements (12°C). The high, cumulative-aging temperatures computed from the Pb-rich phase sizes can be the result of one or both of two possible scenarios:

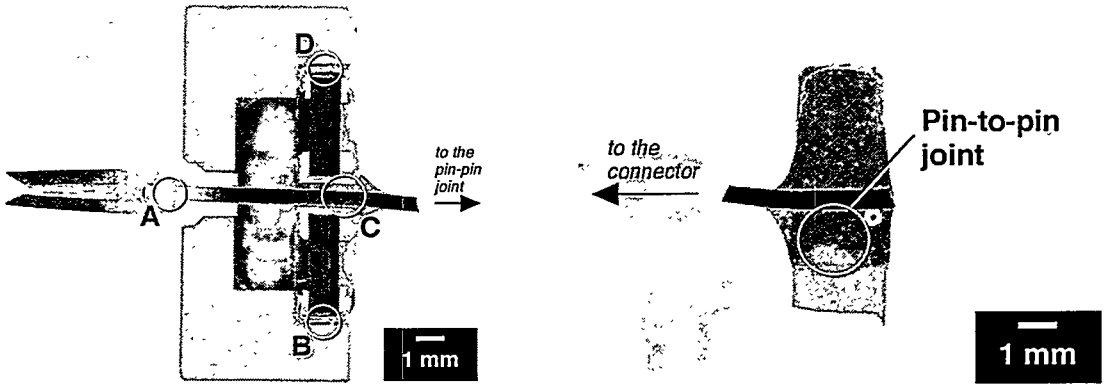
1. The relatively large, mean Pb-rich phase-particle size was a consequence of the soldering process required to make the connector-solder joints, which differed from the procedure used to make traditional leaded joints. The consequence was a coarser, initial Pb-rich phase size due to a very slow cooling rate upon withdrawal of the iron.
2. Thermal expansion induced, residual stresses/strains developed in the solder joints that accelerated coarsening of the Pb-rich phase coarsening at a rate that exceeded that arising simply from isothermal aging. The strain-induced coarsening scenario provides an indication that thermal mechanical fatigue (TMF) processes were active in the solder joints.

Each of the two individual cases will be addressed. Scenario (1) would appear to be least likely, primarily because the bottom-side fillets had a larger Pb-rich phase size than did those on the top side. A greater degree of TMF would have been expected in the top-side fillets because of the proximity of the connector shell structure. The more probable scenario is (2). The connector structure would act as a heat sink during the soldering operation. Therefore, the top-side fillets would have cooled more rapidly than did those on the bottom side, which were last to be contacted by the soldering iron tip, resulting in the former having a smaller Pb-rich phase size than would the latter. This hypothesis indicates the need for a separate, Pb-rich phase distribution data set for non-typical solder joints such as those made to connectors or other, larger structures.

3.2.6 Terminal/Pole Connector-Qualitative (Defect) Analysis

A largely qualitative evaluation was performed on the terminal/pole connector (1433806-3, BBN-2479-E4) solder joints. Shown in Figure 24 are two optical photographs of macro-cross sections of the two structures comprising the connector. Four solder-joint locations—A, B, C,

and D—have been labeled in the photograph; however, views B and D are one-and-the-same joint at diametrically opposed positions. The second structure (Figure 24b) includes a solder joint that is made between the contact lead emanating from solder joint C in Figure 24a and a second pin; this joint is referred to as the pin-to-pin connection. Low magnification, optical micrographs of each of the solder joints are shown in Figure 25. The solder joints are discussed individually, using optical micrographs or extending the investigation by scanning electron microscopy (SEM) and energy dispersive x-ray (compositional) analyses (EDXA).



(a) (b)

Figure 24. Optical micrograph of the cross section of the terminal-pole connector. The primary structure is shown in (a). There are four solder joints (A, B, C, D) in the structure; joints B and D are of, in fact, one and the same joint. The lead seen to extend from joint C connects to a second pin structure shown in (b) which changes the direction of signal transmission within the housing. This latter joint is referred to as the pin-to-pin connection.

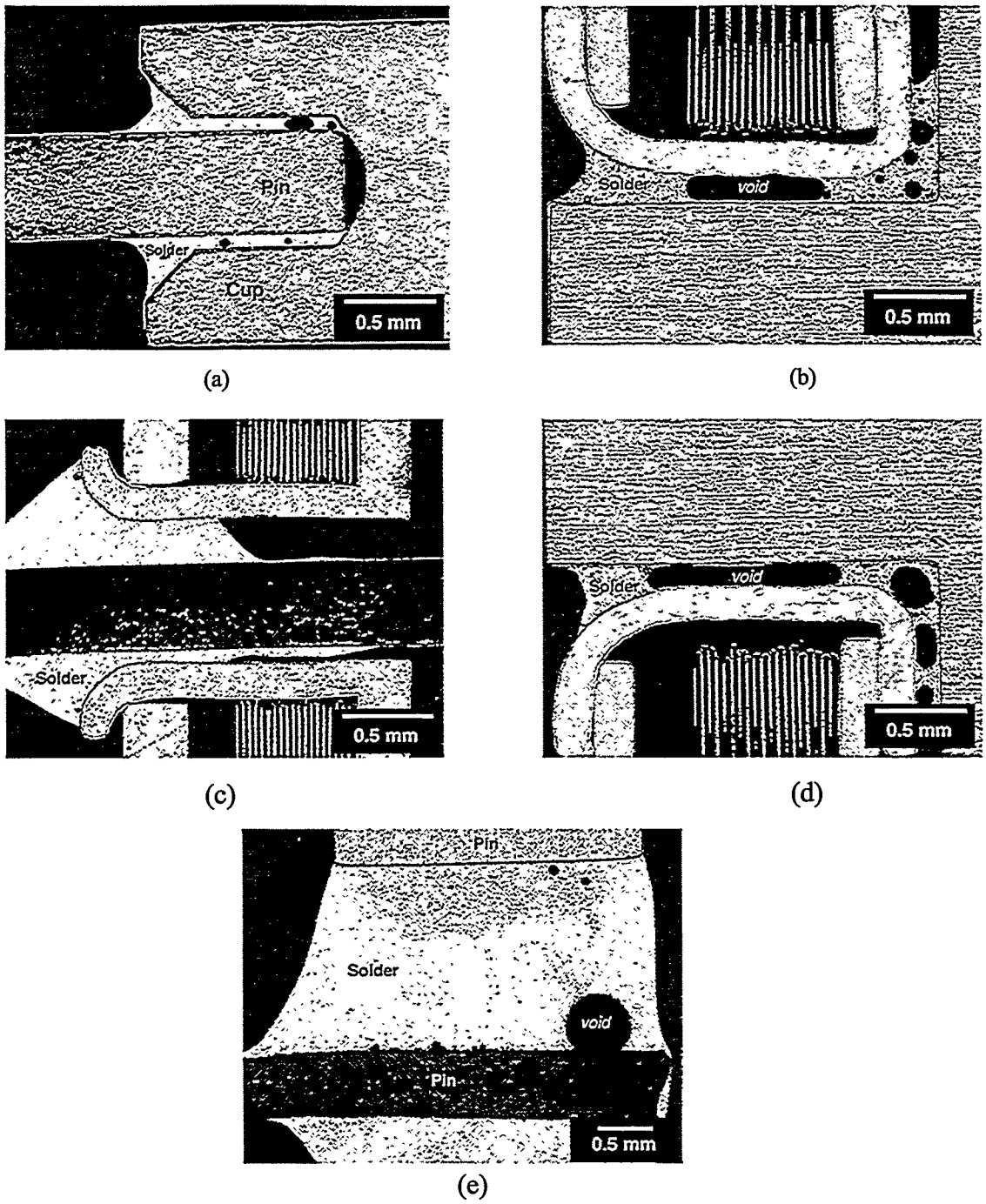


Figure 25. Low magnification, optical micrographs of the solder joints in the primary structure of the terminal-pole connector with reference to Figure 24: (a) solder joint A; (b) solder joint B; (c) solder joint C; (d) solder joint D, which is a continuation of B; and (e) pin-to-pin connection.

Solder joint A. High magnification, optical micrographs of the two sides of the solder joint are shown in Figure 26. Energy dispersive x-ray analysis revealed both the pin and the cup

structures to be made of Cu. Energy dispersive x-ray analysis also indicated that the "solder" material to actually be a higher temperature, braze alloy composed of Ag, Cu, and some Zn.

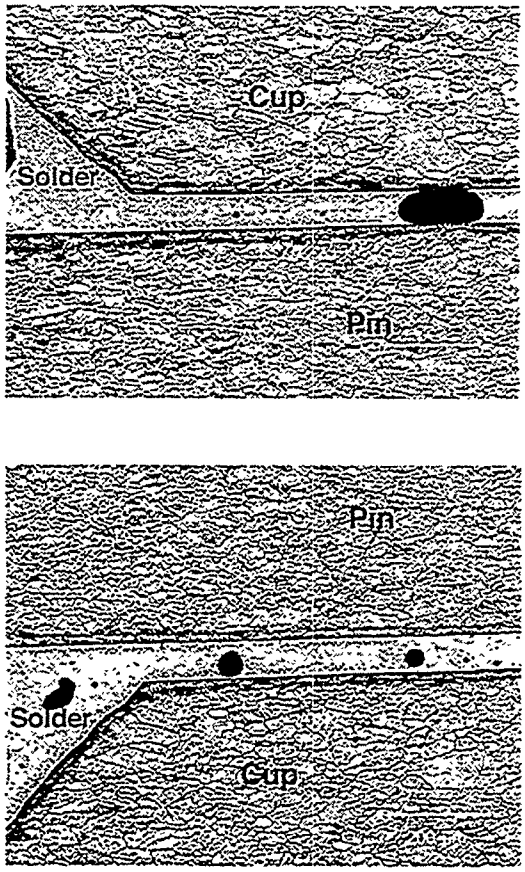


Figure 26. High magnification micrographs of two profiles of solder joint A.

Solder Joints B and D. Figures 25b and 25d show solder joints B and D, respectively; there was considerable void formation in the gaps. A closer examination of the morphology of the voids in joint B is provided by Figures 27a and 27b. Those micrographs indicated the source of the voids as being volatilization of the flux constituents and/or the entrapment of air during the soldering process. Poor surface solderability did not appear to have caused the voids. A similar conclusion was drawn for solder joint D. Energy dispersive x-ray analysis indicated that base metal structures comprising the joint were made of brass (Cu-Zn) alloy. The inner-ring structure (Figure 25b or 25d) had an Ag solderable finish that had not been completely consumed by the Sn-Pb solder. A higher magnification view of the solder in the gap of joint B is shown in Figure

28. A considerable quantity of needle-like structures was noted in this micrograph as well as in that of joint D; these structures were similar to the $AuSn_4$ needles that form when molten solder, which is contaminated with Au, has solidified. The EDXA analysis confirmed that needles were comprised of Au and Sn. The source of the Au was the electroplated protective finish applied to the brass outer housing structure. These needle structures signal a potential for Au embrittlement of the Sn-Pb solder in the joint. However, in spite of the large number of $AuSn_4$ needles, there were no indications of cracking or other forms of degradation in the solder joints.

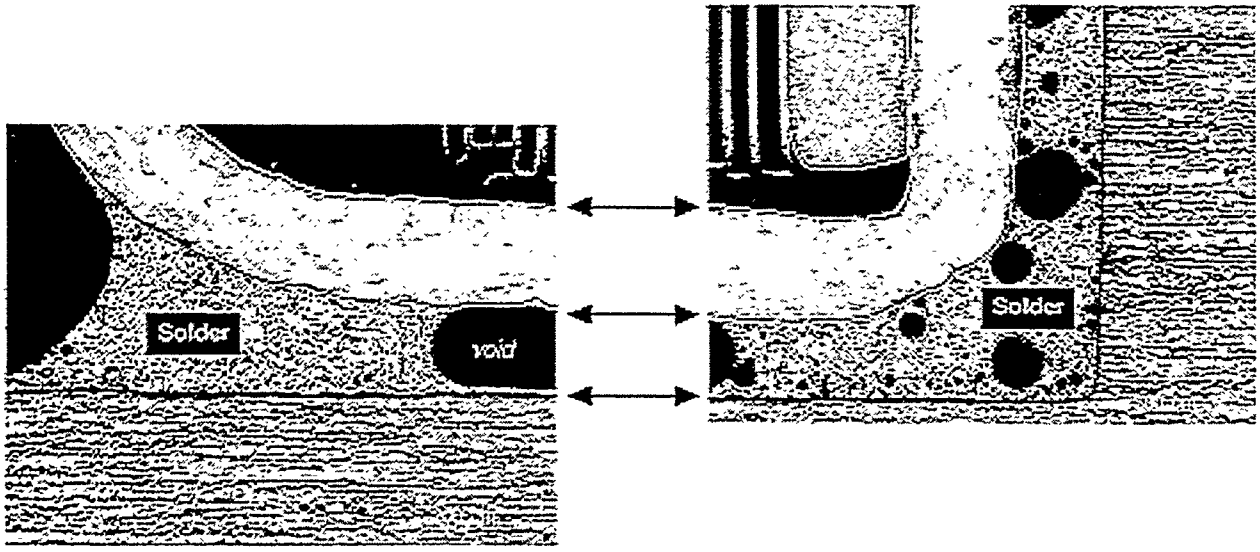


Figure 27. High magnification optical micrographs showing solder joint B. Considerable void formation is observed in the solder forming the gap.

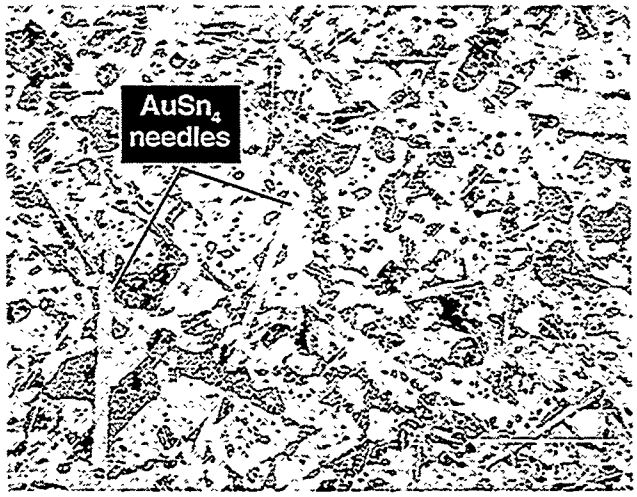


Figure 28. Optical micrograph of the microstructure of the Sn-Pb solder used to make the solder joint B. The presence of $AuSn_4$ needles is evident.

Solder joint C. Optical micrographs of the solder joint appear in Figure 29. Energy dispersive x-ray analysis reaffirmed that the pin material is strictly Cu and that the sleeve to which the lead is attached is brass (Cu-Zn) with an Ag electroplated coating on its surface. The coating had not been fully dissolved by the molten solder. The analysis failed to identify the presence of Ag in the Sn-Pb solder microstructure. The solder joint showed no signs of degradation.

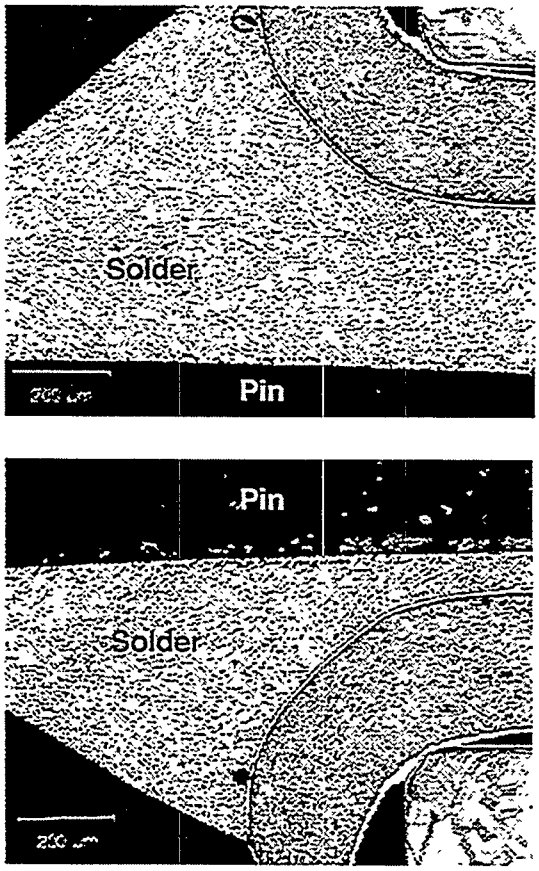


Figure 29. Optical micrographs of the solder joint C.

Solder joint E. The pin (Cu) lead-to-pin solder joint (Figure 25e) was examined. The solder used to make the joint was Sn-Pb. The larger pin to which the lead was soldered was Au plated. There was evidence of $AuSn_4$ precipitates in the solder microstructure along both solder/substrate interfaces (i.e., the interfaces of the smaller pin and the larger pin). Although the presence of Au appeared to be relatively significant, there was no indication of crack formation in the solder.

3.2.7 *Solder Joint Quantitative Analysis—Pb-Rich Phase-Particle-Size Distribution—Terminal/Pole Connector*

The Pb-rich phase particle-size distribution was analyzed for solder joint C. Figure 29 depicts two 500x micrographs taken of either side of the solder joint. The area (volume) percent of Pb-rich phase component in the solder was computed; that value was 32.98 area %. This value converted to 43 wt.%. Allowing for a Sn content of 3 wt.% in the Pb-rich particles, the corrected Pb-rich phase content was 40 wt.%. The mean Pb-rich phase-particle size was determined to be 1.58×10^{-5} mm^2. Placing this value for x in Equation 28 and assuming, once again, a 35 year storage life, the apparent isothermal storage temperature is calculated to have been 53°C (128°F). This cumulative temperature is too high to represent stockpile storage conditions. This discrepancy may indicate that one or a combination of both of the following scenarios took place:

1. The radar unit was subjected to a number of power-up, functional test cycles that raised the connector temperature as electrical signals were transmitted. Confirming documentation did not exist about temperature excursion experienced by this hardware as a result of electrical testing.
2. The soldering process resulted in the joint having a cooling rate that was significantly slower than that of the leaded solder joints (Table 8) used to develop the initial Pb-rich phase-particle size, x_o, of 3.2×10^{-6} mm^2. The slower cooling rate would have resulted in a larger starting mean Pb-rich phase-particle size.

This latter hypothesis is most likely, given the unusual geometry of the joint. Although this scenario would cause Equation 28 to be invalid for this case, the relatively large particle size 1.58×10^{-5} mm^2 indicates that nominal aging of the solder had taken place.

3.2.8 *Summary*

The N57 solder joints from the interconnect board (including those that attached the SA1126 connector to the printed circuit board) as well as the "structural" solder joints used in the construction of the terminal-pole connector did not appear to exhibit significant aging-related

damage. The cracking that was observed in the leaded joints of the interconnect board would not jeopardize their electrical functionality because the Cu-plated hole walls provided a redundant electrical signal path between the top and bottom surfaces of the circuit boards. The cracks were considered as infant mortality events; no further cracking would be expected in units targeted for additional stockpile lifetimes. The engage/disengage function performed on the SA1126 connector attached to the interconnect circuit board may have resulted in cracks observed in the laminate, underneath the Cu bonding pads of the connector pin solder joints. The severity of the damage was not sufficient enough to cause an interruption in the signal functionality of the pad or Cu trace(s) attached to it.

A synopsis is discussed of the quantitative data from the N57 unit analyses. First, it may be expected that the intermetallic compound layer thickness provides the most consistent metric for describing the cumulative temperature exposure experienced by the solder joint. The thickness of the initial intermetallic compound layer that forms during the soldering process (molten Sn-Pb alloy) is least sensitive to the range of soldering conditions (time and temperature) that are likely to occur at manufacturing. Also, a prior study indicated that in the Sn-Pb/Cu system, the solid-state growth of the intermetallic compound layer is not strongly sensitive to residual stresses formed in the joint [17].

However, the Pb-rich phase-size distribution is sensitive to both manufacturing processes and aging conditions. The cooling rate of the solder following joint formation will strongly impact the initial particle size; the faster the cooling rate, the smaller the particle size. The present baseline data were developed for traditional solder joints made between leaded devices and plated though-hole circuit boards. Second, particle size is sensitive to aging conditions, including the contributory factors of temperature history *and* stress/deformation that might occur during thermal mechanical fatigue (TMF) deformation. Interestingly enough, subtracting out from the overall coarsening behavior, that contribution to Pb-rich phase coarsening caused solely by elevated temperature exposure results in that contribution made by the stress/strain effects.

The leaded-solder joints made to the interconnect (junction) circuit board showed a very thin intermetallic compound layer of 0.87 μm. This value results in the calculation of a cumulative aging temperature of 12°C (54°F). This temperature parameter is lower than would be experienced in a storage environment; rather, an impact was had by small data variations (e.g., the *actual* value of x_o) that, in turn, became significant under the very limited layer growth. Nevertheless, the calculation confirms that minimal thermal aging had taken place in the joints. The leaded joints had a Pb-rich phase-size distribution that indicated a cumulative aging temperature of -14°C (6°F), again—a very low value. Similarly, this calculation qualitatively concurs with the intermetallic compound layer thickness data, that there was a minimal degree of aging in those solder joints.

The SA1126 connector pin solder joints made to the interconnect circuit board showed a similarly low, intermetallic compound layer thickness of 0.86 μm. However, the Pb-rich phase size distribution for these solder joints indicated much higher effective aging temperatures of 46°C (115°F) for the top (connector) side of the joints and 64°C (147°F) for the bottom-side fillets. Since known storage conditions and the intermetallic compound layer thickness measurements did not substantiate these unusually high-temperature conditions, it was determined that the initial Pb-rich phase was large because of the soldering process or that significant coarsening had taken place because of TMF that resulted from thermal expansion mismatch strains in the joint. The first premise of large, initial particle sizes as compared to the baseline values appeared most likely to have occurred—given the structure of the connector and soldering process. These results express the need to have separate sets of baseline data for solder joints made to "unusual" structures such as connectors.

The above discrepancy in aging computations caused by use of the non-applicable baseline data may have been indicated by the analysis of the solder joints in the terminal/pole connector, as well. In this case, the Pb-rich phase size distribution indicated a cumulative, effective aging temperature of 53°C (128°F). Again, this connector structure is vastly different

from that of the traditional leaded through-hole solder joints (Table 8) used to establish the baseline value, x_o.

3.3. B61 (0) Analysis

The analyses of a fielded B61-0 tube-type radar (MC1828) used the protocols established in the N57 unit investigation. However, some specifics of those studies were altered slightly. For example, the terminal-pole connector solder joints were given only a qualitative examination. Also, the solder joints of the SA1126 connector attached to the B61 interconnect circuit board were not examined. Conversely, a circuit board was retrieved from within one of the segments of the radar, and the solder joints from two components on that board were qualitatively and quantitatively evaluated. Regarding format, the analyses of intermetallic layer growth and Pb-rich phase-size coarsening have been grouped together by component rather than by the individual metrics in the following discussion.

3.3.1 Solder Joint Qualitative (Defect) Analysis—Interconnect Circuit Board

The interconnect (or junction) printed circuit board (1433983-6) was separated from between the two halves of the radar assembly. Three segments were cut from the printed circuit board. Five solder joints were analyzed from the first segment designated #1and three solder joints from each of the other two segments labeled #2 and #3. Figure 30 is a schematic diagram of the locations of the intermetallic compound layer thickness measurements. Location E is at the hole wall and location F is at the bottom-side pad. The Pb-rich phase particle-size distribution was measured at *two* locations; those locations were G in the bottom-side fillet (the same as with the N57 unit) and H in the top-side fillet. The additional data were taken in order to ascertain whether the differences existed in the Pb-rich phase-particle sizes between the two sites for actual hardware. Recall that differences in the particle sizes were noted between the top-side and bottom-side fillets of the baseline data.

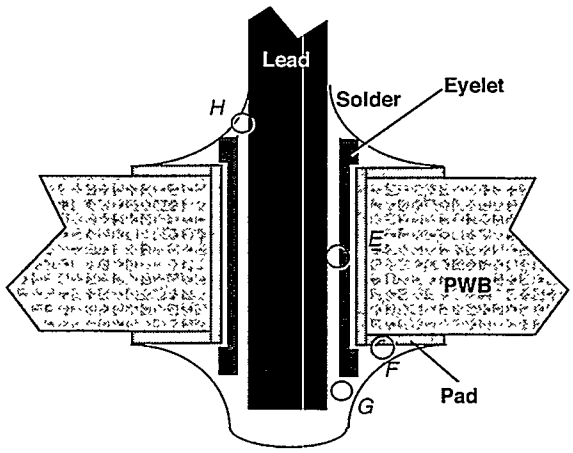


Figure 30. Schematic diagram of the through-hole solder joint on the B61, interconnect (junction) circuit board, indicating the locations of the intermetallic compound layer thicknesses (E, hole wall and F, the bottom surface bonding pad) and Pb-rich phase particle-size distribution (G, bottom-side fillet and H, the top-side fillet).

As was the case with the N57 interconnect circuit board, the B61 solder joints used the same eyelet through-hole geometry. The leads on the B61 hardware were solid Cu, having a nominal diameter of approximately 0.035 in. It was observed that a number of solder joints suffered from incomplete hole fill at the top side (component side) of the joint. These defects are illustrated by the representative, optical micrographs shown in Figure 31. For comparison, a satisfactory, top-side fillet geometry can be observed in Figure 7 for a similar solder joint from the N57 unit. The solder fillet forms an angle of less than 90° against the lead's vertical surface. Figure 31a shows the case in which solder flows through the hole was complete; however, it was insufficient to complete the top-side fillets. The solder is at 90° to the lead. Figure 31b shows the case of incomplete hole filling and, accordingly, the absence of fillets at the joint on the top side of the circuit board. In this case, the angle between the fillet and the lead is greater than 90°.

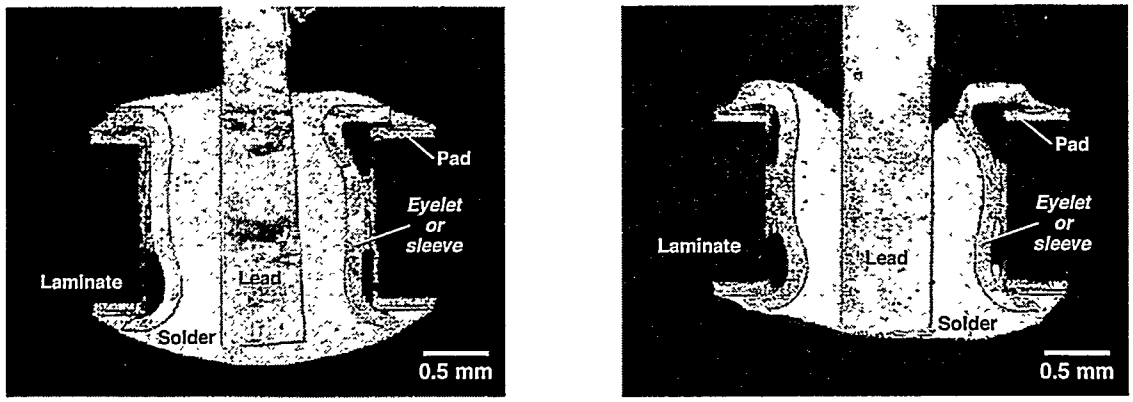


Figure 31. Optical micrographs of the solder fillet defects observed in the B61, interconnect circuit board solder joints: (a) no fillets on the top side but complete hole fill, and (b) no fillets on the top side and incomplete hole fill .

A quantitative assessment was made of the solder joint defects on the interconnect circuit board by identifying one of three defect categories for each joint:

1. full fillet (<90°),
2. filled hole, but absent fillets (90°), and
3. incompletely filled hole (>90°).

Full fillets were observed in only one of the eleven joints (9%); the case of the filled hole, but absent fillets was observed in three of eleven joints (27%); and, the condition of an incompletely filled hole and no top-side fillet was recorded in seven of eleven joints (64%). Therefore, 91% of the solder joints would be considered defective according to present-day soldering standards. By comparison, although the N57 solder joints showed similar defects on the top sides of the joints as did the B61 hardware, they appear to have occurred to a much lesser degree in the former case.

Void formation was an isolated occurrence in the B61 interconnect solder joints, much as was the case with the corresponding N57 hardware. As in the latter case, the morphology of the

voids indicated that their source was entrapped flux volatiles or air rather than a wettability problem associated with any of the Cu surfaces.

Because of the use of the eyelet solder joint design, a quantitative assessment was made of the prevalence of cracking in the fillets formed between the eyelet and the pad. This analysis was slightly more detailed than was the similar exercise performed on the interconnect circuit board solder joints in the N57 unit. The evaluation was performed on the two views or "quadrants" of the top-side fillet of the joint and on the two quadrants of the bottom-side fillet. Although the two views of each fillet cross sections do, in fact, represent the same fillet, the data were expressed *per quadrant* and not combined to represent the overall top or bottom fillet. The condition of each fillet section received one of four possible ratings:

1. large degree of microstructural deformation or "damage," but no crack formation;
2. partial crack propagation;
3. complete fracture of the fillet; and
4. no cracking or damage to the solder.

Table 14 summarizes the results. In the case of the bottom fillets, degradation was observed in 27% of the cases, appearing as microstructural deformation in 25% of the cross sections and partial cracks in 2% of the quadrants. Thirty-nine percent of the top-side fillets were observed to have degradation with 9% exhibiting microstructural deformation and partial fractures in 30% of the top side quadrants. Complete cracks were not recorded for either the top-side or bottom-side fillets.

Table 14
Eyelet Solder Fillet Deformation and Cracking
Percentage of Top and Bottom Fillets (All Joints Combined)
B61 Junction (Interconnect) Circuit Board

Degree of Damage	Top-Side Fillet	Bottom-Side Fillet
Damage present	9%	25%
Partially fractured	30%	2%
Fully fractured	0%	0%

The presence and severity of the defects associated with the eyelets were directly related to the quantity of solder observed in the joint. The top-side fillets were prone to degradation more than the bottom-side fillets (Table 14) because of an absence of solder indicated by a prevalence of poorly formed fillets and unfilled holes. There was ample solder on the bottom side of the joints. In the event of more severe cracking, signal transmission between the two surfaces of the circuit board would not be interrupted. The hole walls had been plated with Cu, thus providing a redundant signal path between the top and bottom surface features of the circuit board.

A comparison was made of these results with those from the N57 unit. In order to make the comparison valid, the B61 results for partial and full cracking were combined; those joints exhibiting only deformation were now considered as "non-defective" for this exercise. The occurrence of cracking in each case was: (N57), 50% top and 17% bottom; and (B61), 30% top and 2% bottom. There was a significantly lower degree of eyelet fillet cracking in both the top and bottom fillets of the fielded B61 interconnect circuit board than was observed in the N57 assembly. Intuitively, this observation appears contradictory because the fielded B61 unit was exposed to harsher conditions (albeit, not severely so) than the N57 nose cone. The source of the reduced frequency of cracking in the B61 joints was a compound effect resulting from the larger number of workmanship defects in the top fillets. Explicitly, the defects resulted in an absence of solder in the top fillets; in effect, there was little or no solder in which cracks could form. Indirectly, the lack of solder (fillets) reduced the constraint imposed on the joint structure during temperature cycling. In particular, the magnitude of residual stresses imposed on the bottom fillets would have decreased. As a result, we observed the extent of cracking there would also have become more limited in scope.

3.3.2 Intermetallic Compound Layer Growth—Interconnect Circuit Board

Table 15 lists the intermetallic compound layer thickness values for both hole (E) and pad (F) locations. Only the Cu_6Sn_5 layer stoichiometry was observed at the interface. The equality

of the intermetallic compound layer thickness between the hole and pad sites was tested by the combination of the F-test for the equivalence of variance and the Student's t-test for the equivalence of the mean thicknesses. Of the eleven solder joints, nine joints (or 82%) exhibited statistically similar mean, intermetallic compound layer thicknesses at both the hole and pad locations. In two of eleven cases (12%) in which the two values were not equal, the layer thickness at the pad was greater than that at the hole wall. As noted in the N57 discussions, the hole wall having a thinner layer would be conclusive since this trend would not be an artifact of the section position relative to the hole axis. The intermetallic compound layer thickness used to represent these solder joints was that at the pad location (F).

Table 15
Intermetallic Compound Layer Thickness (μm)
Locations: Hole (E) and Pad (F)—B61 Junction (Interconnect) Circuit Board
one standard deviation in parentheses

Segment	Solder Joint	Hole (E)	Pad (F)
#1	#1	1.93 (0.27)	1.87 (0.25)
(5 joints)	#2	1.68 (0.28)	1.54 (0.35)
	#3	1.78 (0.25)	1.55 (0.28)
	#4	1.44 (0.26)	1.78 (0.26)
	#5	1.62 (0.11)	1.59 (0.29)
#2	#1	1.68 (0.27)	1.52 (0.28)
(3 joints)	#2	1.64 (0.21)	1.68 (0.17)
	#3	1.33 (0.31)	1.86 (0.25)
#3	#1	1.59 (0.25)	1.81 (0.26)
(3 joints)	#2	1.59 (0.26)	1.52 (0.19)
	#3	1.60 (0.33)	1.70 (0.25)

There was no indication that the solder joints present within each of the three sections (#1, #2, and #3) were made differently from each other. In fact, an equality-of-mean thickness analysis was performed on each possible pairs of solder joints formed within each of the three segments. All three segments exhibited the same behavior—66% of the pair-wise combinations

had equal mean thickness. Moreover, calculated mean values representing each of the three segments were not significantly different from one-another. Therefore, the data from the eleven joints (at F location) were combined into a single value to represent the B61-0 interconnect circuit board; that value was:

$$x = 1.67 \pm 0.29\ \mu m \quad .$$

Clearly, growth of the layer had occurred in the B61 joints when the above value was compared against the baseline value of 0.714 ± 0.269 μm. It was assumed that the part had been in the stockpile for 35 years (1.104×10^9 s). The value of the intermetallic compound layer thickness, x, the initial thickness, x_o, and time, t, were applied to Equation 27 in order to calculate a cumulative aging temperature. Again, the cumulative temperature includes the effects of next-assembly manufacturing steps, power-up/E-tests, and lastly, stockpile storage. That temperature value was *38°C (100°F).* This value is slightly higher than may be expected from stockpile environments. Therefore, the effects of next-assembly processes and subsequent testing are reflected in the intermetallic compound layer thickness. Regardless of the source of the additional layer growth, the resulting thicknesses were not excessive enough to jeopardize the integrity of the solder joint functionality.

Table 16 shows an interesting comparison of the intermetallic compound layer thickness data between the N57 unit, which remained in the laboratory for most of its lifetime, and the B61 hardware, which had been in the field. A greater degree of aging had taken place to the solder joints contained in the junction board of the fielded B61 unit as compared to the "laboratory" N57 solder joints. If it is assumed that both radar assemblies were similarly fabricated, then the differences reflect upon variations in testing environments as well as laboratory versus stockpile storage conditions. Clearly, the intermetallic compound layer data indicate that WR hardware undergoes a greater degree of overall aging than does similar equipment that remains in a laboratory environment.

Table 16
Intermetallic Compound Layer Thickness (Pad Location, F)
N57 Compared to the B61(0)
Junction (Interconnect) Circuit Board Data
one standard deviation in parentheses

Property	N57	B61(0)
Number of joint analyzed	9	11
Intermetallic compound layer thickness (μm)	0.87 (0.53)	1.67 (0.29)
Cumulative lifetime temperature *(assumed lifetime: 35 years)*	12°C, 54°F	38°C, 100°F

An additional point in Table 16 is that the data scatter is significantly less for the thickness measurements from the B61 unit. As a percentage error, the data scatter from the B61 and comparable N57 studies were 17% and 61%, respectively. Given similar sample sizes and the same measurement/analysis techniques, this difference in thickness scatter is statistically significant. The source of the different data scatter values rests with the aging process and resulting intermetallic compound layer morphology. In the as-fabricated condition, the intermetallic compound layer has an uneven, nodular appearance that is represented by small hillocks in two-dimensional images [17,18]. The initial stages of solid-state layer growth include the filling-in of the regions between the hillocks, allowing the layer to have a more uniform thickness along its length. As a result, the statistical variation (standard deviation) of the thickness measurements is reduced with additional aging. This hypothesis explains the differences in scatter between the B61 and N57, interconnect circuit board data.

3.3.3 *Pb-Rich Phase Particle-size distribution Analyses—Interconnect Circuit Board*

The Pb-rich phase size was measured at the top and bottom fillet locations in each of the solder joints. Those values are listed in Table 17. The first step was to examine the area

(volume) percent of Pb found in the joints. The data from both the top and bottom fillets were combined for this computation. The area (volume) percent was determined to be 32.2±3.2%. The data scatter is similar to that observed in the N57 joints as well as that found in the baseline measurements. The corresponding weight percent of Pb is 43%. This value is corrected for an assumed quantity of 3 wt.% of Sn remaining in solid solution in the Pb-rich phase. *The corrected Pb content is 40 wt.% Pb.* A 40 wt.% value would correspond to the use of the 60Sn-40Pb solder to make the joints.

Table 17
Pb-Rich Phase Particle-Size Distribution Parameters
Locations: Bottom-Side Fillet (G); Top-Side Fillet (H)
B61 Junction (Interconnect) Circuit Board

Segment	Solder Joint	Mean Size (mm^2)	St. Dev. (mm^2)	No. of Particles	Area %
#1	#1 (bottom)	12.8×10^{-6}	26.0×10^{-6}	908	28.3
(5 joints)	#1 (top)	15.6×10^{-6}	34.7×10^{-6}	759	28.6
	#2 (bottom)	13.3×10^{-6}	33.3×10^{-6}	946	30.7
	#2 (top)	14.0×10^{-6}	40.1×10^{-6}	826	28.3
	#3 (bottom)	18.9×10^{-6}	46.9×10^{-6}	632	28.9
	#3 (top)	21.7×10^{-6}	72.1×10^{-6}	595	31.2
	#4 (bottom)	17.6×10^{-6}	45.5×10^{-6}	722	31.2
	#4 (top)	17.4×10^{-6}	51.1×10^{-6}	776	33.2
	#5 (bottom)	13.7×10^{-6}	35.1×10^{-6}	1056	35.5
	#5 (top)	17.3×10^{-6}	74.6×10^{-6}	872	37.0
#2	#1 (bottom)	19.4×10^{-6}	33.8×10^{-6}	611	28.8
(3 joints)	#1 (top)	13.1×10^{-6}	65.1×10^{-6}	1169	37.3
	#2 (bottom)	21.9×10^{-6}	51.7×10^{-6}	625	33.3
	#2 (top)	18.1×10^{-6}	32.0×10^{-6}	626	27.9
	#3 (bottom)	17.0×10^{-6}	63.4×10^{-6}	754	30.5
	#3 (top)	24.7×10^{-6}	101×10^{-6}	605	36.4
#2	#1 (bottom)	13.8×10^{-6}	30.0×10^{-6}	974	32.7
(3 joints)	#1 (top)	19.9×10^{-6}	67.4×10^{-6}	604	29.2
	#2 (bottom)	21.8×10^{-6}	53.1×10^{-6}	614	32.5
	#2 (top)	16.4×10^{-6}	72.3×10^{-6}	915	36.4
	#3 (bottom)	18.3×10^{-6}	70.4×10^{-6}	827	36.8
	#3 (top)	20.8×10^{-6}	134×10^{-6}	666	33.7

The next analysis on the Pb-rich phase size was to perform a pair-wise comparison testing the equivalence of the mean particle size between the top side (H location) and bottom

side (G location) fillets. Of the eleven solder joints used in this evaluation, the mean Pb-rich phase size was statistically equal between the two locations (Student's t-test) in nine of the eleven cases, or 82%. In those two instances in which the two values did not test equal, one case had the bottom fillet (G) with the larger particle size and the other had the top fillet (H) with the greater mean particle size; therefore, no trend was observed in the cases of the inequalities.

Next, the bottom-side fillet, Pb-rich phase-particle size values from among all of the joints per segment were combined in each segment as were similar top-side fillet data. Two pair-wise analyses were then performed on these condensed values:

1. The equality of the top and bottom fillet particle sizes in each of the three segments were tested (segment #1, G versus H; segment # 2, G versus H; and segment #3, G versus H). In all three cases, the top and bottom means were equivalent.
2. The bottom side measurements were compared between the different segments (e.g., G value of segment #1 versus the G value of segment #2, etc.) as were the top fillet data cross-compared (e.g., H value of segment #1 versus the H value of segment #2, etc.).

In the former case, two of the three combinations were equivalent, while in the latter case all three means were equal. These analyses confirmed that there was no distinction between the solder joints of the three segments of the interconnect board. Therefore, like data were combined from *all* of the solder joints. The mean particle sizes and weighted or "pooled" variance are listed below:

Bottom fillets: Mean, 17.7×10^{-6} mm^2
Standard deviation, 66.8×10^{-6} mm^2.

Top fillets: Mean, 18.3×10^{-6} mm^2
Standard deviation, 65.4×10^{-6} mm^2.

There was no significant difference of mean particle size between the top and bottom fillets of the solder joints. Table 18 provides a complete summarization of the Pb-rich particle size statistics. The difference in area percent of Pb for the top-side fillet versus the fillet on the bottom of the joint was not statistically significant; the corresponding weight percent Pb values (subtracting the 3% correction) were bottom, 39% and top, 40%.

Table 18
Pb-Rich Phase Particle-Size Distribution Parameters
Summary Of Combined Data (All Segments)-
B61 Junction (Interconnect) Circuit Board

Fillet Location	Number Of Joints	Mean Size (mm^2)	St. Dev. (mm^2)	No. of Particles	Area %
Bottom fillets	11 solder joints	17.7×10^{-6}	66.8×10^{-6}	8669	31.9
Top fillets	11 solder joints	$18.3 \times 10^{-}$	65.4×10^{-6}	8413	32.9

The cumulative aging temperature was computed from the Pb-rich phase sizes of the B61 interconnect circuit board solder joints using Equation 28. Again, a 35-year lifetime was assumed for the hardware age. The computed aging temperatures for the bottom- and top-side fillets were: *bottom, 57°C (135°F) and top, 59°C (138°F).* These values are relatively high, not only from the standpoint of stockpile storage environments, but also when compared to the 38°C (100°F) temperature based upon the intermetallic compound layer thickness. The Pb-rich phase particle metric shows that the solder microstructure had received additional aging besides that caused by the temperature conditions. A likely source of the supplemental temperature would be strain-enhanced coarsening of the Pb-rich particles under the residual stresses created in the joint. The relatively high-aging temperature condition indicated by the intermetallic compound layer thickness (38°C) would suggest that the solder joints experienced high-temperature excursions (e.g., next assembly, E-testing, etc.). Those elevated temperature events could have generated considerable thermal expansion mismatch stresses, the corresponding strains would have accelerated the coarsening rate of the Pb-rich phase particles.

3.3.4 *Intermetallic Compound Layer Growth—Segment 1440099-4 (Internal) Circuit Board*

A circuit board was extracted from within the fourth segment (1440099-4) of the radar assembly. The solder joints from two resistors, SA1229-3 and SA1229-54, were evaluated. The solder joints from the SA1229-**3** resistor were designated "3-1" and "3-2" while those from the SA229-**54** resistor were designated "54-1" and "54-2." The resistor leads were soldered to plated-through holes in the 0.030-in. thick circuit board; there was no eyelet construction used in these joints as illustrated by the micrograph in Figure 32. The intermetallic compound layer measurements were taken from two locations in the joints—the hole wall (E) and the pad interface (F).

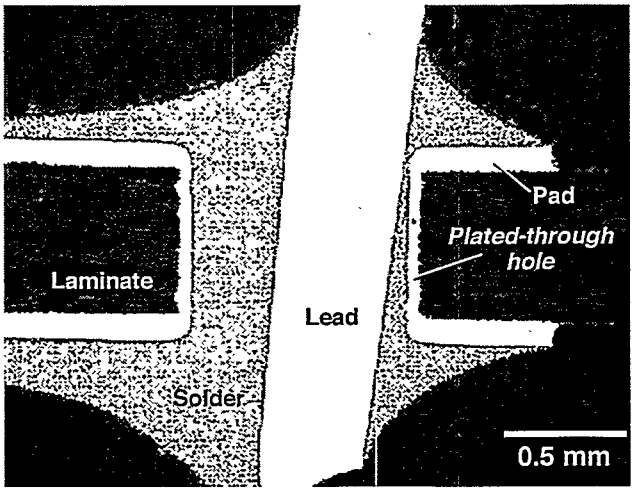


Figure 32. Optical micrograph of the SA1223-3 resistor, "3-2" solder joint on the internal circuit board.

An interesting observation was made of the intermetallic compound layer that formed in these joints when compared to that from solder joints in the interconnect circuit board. That difference was the appearance of the Cu_3Sn sublayer along with the traditionally observed, Cu_6Sn_5 sublayer. This finding is shown by the micrograph in Figure 33 of the intermetallic compound layer at the solder/Cu interface of the hole wall. The view is rotated 90°. The two sublayers were also observed at the solder/Cu interface of the pad. Table 19 lists the mean and standard deviation statistics for the intermetallic compound layer thicknesses of each joint, including measurements of the individual sublayers along with the total layer thickness. The

unexpected nature of the occurrence of a Cu_3Sn sublayer is based on previous studies that indicated that this stoichiometry did not appear under solid-state aging conditions until a significant thickening of the Cu_6Sn_5 layer to values in excess of 5-6 μm had already occurred [19, 20]. In terms of aging parameters, measurable Cu_3Sn thicknesses were not realized in Sn-Pb/Cu couples until the aging temperature exceeded 135°C and for time periods in excess of 135 days; in fact, the study in Reference 20 determined that the Cu_3Sn layer was not observed for lesser aging temperatures, even after time periods of as long as 400 days. Moreover, the B61 solder joints had an ample solder field to preclude the preferred formation of the Cu_3Sn sublayer in the absence of an adequate Sn supply. The ratio of the thickness of the Cu_3Sn layer to the total layer thickness was computed for the pad (location F) of each resistor. The averages of those values were (1) SA1229-3, 0.26 and (2) SA1229-54, 0.27. These values were similar to those expected of the Sn-Pb alloy on Cu [20].

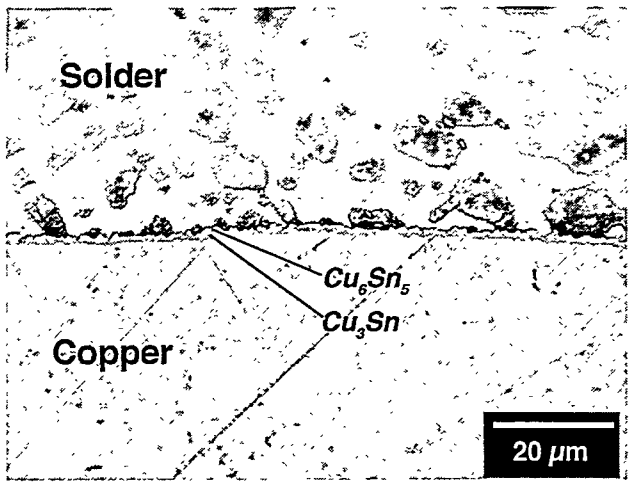


Figure 33. Optical micrograph of the solder/hole wall interface (location E) of the solder joint SA1229-3, #2 showing the intermetallic compound layer composed of both the dark Cu_3Sn sublayer next to the Cu conductor and lighter Cu_6Sn_5 sublayer adjacent to the solder field.

A likely scenario behind the appearance of the Cu_3Sn sublayer was that the circuit board had been subjected to solid-state aging between the Cu and Sn-Pb coating prior to it being soldered with components. The pre-assembly aging resulted in the growth of the Cu_3Sn sublayer, along with the Cu_6Sn_5 sublayer. A limited Sn supply resulting from the thin Sn-Pb

coating would have favored the formation of the Cu_3Sn sublayer. There remained some solder coating to ensure adequate solderability of the conductive traces. When the soldering assembly of the leaded components was performed, the soldering process removed the Cu_6Sn_5 sublayer but was sufficiently fast that it did not dissolve away the underlying Cu_3Sn sublayer. As a result, the latter sublayer was present in the solder joints.

All further analyses have been performed on the total layer thickness values (Table 19). The equality of the intermetallic compound layer thickness at hole (E) and pad (F) locations was tested using the appropriate Student's t test. The SA1229-3 resistor joints both indicated equality of the mean thickness between the two locations, while both joints of the SA1229-24 resistor showed unequal thicknesses between the hole and pad locations. In the latter case, the layer thicknesses were greater at the Sn-Pb/Cu interface on the hole wall as compared to the same interface on the pad. This difference may have been caused by a non-axial, metallographic section and, therefore, was deemed an experimental artifact. As in previous protocols, the pad location (F) thicknesses were used in further quantitative analyses.

Table 19
Intermetallic Compound Layer Thickness (μm)
Locations: Hole (E) and Pad (F)-
B61, Internal Circuit Board (SA1229 resistors)
one standard deviation in parenthesis

	Hole (E) (μm)			Pad (F) (μm)		
Solder Joint	Cu_3Sn	$CuSn_5$	Total	Cu_3Sn	$CuSn_5$	Total
3-1	0.55 (0.15)	0.74 (0.23)	1.29 (0.27)	0.29 (0.14)	0.83 (0.27)	1.12 (0.20)
3-2	0.75 (0.26)	0.55 (0.33)	1.30 (0.46)	0.28 (0.13)	0.76 (0.29)	1.04 (0.26)
54-1	0.70 (0.16)	0.99 (0.33)	1.68 (0.30)	0.59 (0.11)	0.52 (0.23)	1.11 (0.21)
54-2	1.04 (0.21)	0.88 (0.33)	1.92 (0.29)	0.00 (0.00)	1.03 (0.32)	1.03 (0.32)

A comparison was made of the mean thickness values between the two solder joints (-1 and -2) per each of the resistors. In the case of either resistor, the intermetallic compound layer thicknesses were statically equal for both joints.

The intermetallic compound layer thickness data (F) from the two joints per resistor were combined. The resulting values were (1) SA1229-3, 1.08±0.23 μm and (2) SA1229-54, 1.07±0.28 μm. The Student's t test was used to assess the equality of the two mean thickness values; the result was that the two mean values were not statistically different. Therefore, the two data sets derived from the two resistors were combined into a single value to represent the intermetallic compound layer thickness of the internal circuit board solder joint; that value along with as-pooled standard deviation was:

$$x = 1.08 \pm 0.26\ \mu m \quad .$$

This mean thickness is slightly less than that calculated for the interconnect circuit board solder joints (1.67±0.29 μm). The corresponding aging temperature of the internal circuit board solder joints was calculated to be *24°C (75°F)*, indicating a reduced temperature exposure during the lifetime of the internal circuit board. This trend is not at all unexpected, given that the circuit board is potted and that it is located deep within the segment #4 housing. The amplitude of temperature excursions would be significantly curtailed in that enclosed environment when compared to conditions experienced by the more exposed interconnect solder board.

3.3.5 Pb-Rich Phase Particle-Size Distribution Analysis—Segment 1440099-4 (Internal) Circuit Board

Table 20 lists the Pb-rich phase particle-size distribution measurements at locations in both the bottom (G) and top (H) fillets of the solder joints. The Pb-rich phase area percent values for each of the two resistors were analyzed for the equivalent weight percent. The data from the two fillets of both joints were combined. The mean area percent for the SA1229-3 resistor solder joints was 30.2%; the mean area for the SA1229-54 was 31.9%. The corresponding weight percent values, which were compensated for an assumed 3 wt.% content of Sn in solid solution in the Pb particles, were 37% and 39%, respectively. These values corroborate earlier measurements on the interconnect board solder joints and indicate a composition corresponding to the use of 63Sn-37Pb or 60Sn-40Pb solder.

Table 20
Pb-Rich Phase Particle-Size Distribution Parameters
Locations: Bottom-side Fillet (G); Top-Side Fillet (H)
B61 Internal Circuit Board (SA1229 resistors)

Resistor	Solder Joint	Mean Size (mm^2)	St. Dev. (mm^2)	No. of Particles	Area %
SA1229-3	#1 (bottom)	15.9×10^{-6}	31.2×10^{-6}	828	32.1
(2 joints	#1 (top)	18.8×10^{-6}	34.6×10^{-6}	656	30.0
	#2 (bottom)	16.7×10^{-6}	35.9×10^{-6}	753	30.6
	#2 (top)	21.4×10^{-6}	46.0×10^{-6}	537	28.0
SA1229-54	#1 (bottom)	20.9×10^{-6}	40.4×10^{-6}	595	30.5
(2 joints)	#1 (top)	21.4×10^{-6}	41.2×10^{-6}	596	31.0
	#2 (bottom)	13.7×10^{-6}	24.5×10^{-6}	958	32.1
	#2 (top)	21.1×10^{-6}	$55.9 \times 10^{-}$	660	34.0

A review of the data in Table 20 indicated that the bottom fillets appeared to have a smaller mean particle size and a greater number of particles in the evaluation area than did the top fillets. A pair-wise comparison was made of the Pb-rich phase particle mean size values measured at the bottom-side fillet versus the top-side fillets of each joint. In fact, the Student's t-test indicated that mean Pb-rich phase-particle sizes were actually equivalent between the bottom and top-fillet locations for all joints. Hypothetically, a smaller particle size on the bottom-side fillets implies a faster cooling rate than was experienced by the top-side fillet. This difference, if it were significant, would provide corroborative evidence that the joints were made at the top (or component) side of the circuit board.

The particle-size data from each of the solder joints were combined with each of the resistors. Those results are reported in Table 21. When pair-wise (Student's) t-tests were performed to test the equivalence of particle size means between solder joints of the two resistors, the means were, in fact, the same in all cases. Therefore, the data from the two resistors were combined to result in a value that represented the Pb-rich phase particle distribution for solder joints on the internal circuit board; these mean values are listed in Table 22

along with the standard deviations, particle counts, and area percent data. Again, the top-side and bottom-side distinction is maintained, although, the values are not statistically different.

Bottom fillets: Mean, 16.8×10^{-6} mm^2
Standard deviation, 32.5×10^{-6} mm^2.

Top fillets: Mean, 20.7×10^{-6} mm^2
Standard deviation, 45.2×10^{-6} mm^2.

Table 21
Pb-Rich Phase Particle-size Distribution Parameters
Locations: Bottom-Side Fillet (G); Top-side Fillet (H)
B61 Internal Circuit Board (SA1229 resistors)
Summary per Resistor Type

Resistor	Location	Mean Size (mm^2)	St. Dev. (mm^2)	No. of Particles	Area %
SA1229-3	Bottom	16.3×10^{-6}	33.5×10^{-6}	1581	31.4
(2 joints)	Top	20.1×10^{-6}	40.1×10^{-6}	1193	29.0
SA1229-54	Bottom	17.3×10^{-6}	31.6×10^{-6}	1553	31.3
(2 joints)	Top	21.3×10^{-6}	49.5×10^{-6}	1256	32.5

Table 22
Pb-Rich Phase Particle-Size Distribution Parameters
Summary per Combined Data (Both Resistors)
B61 Internal Circuit Board

Fillet Location	Number of Joints	Mean Size (mm^2)	St. Dev. (mm^2)	No. of Particles	Area %
Bottom fillets	4 solder joints	16.8×10^{-6}	32.5×10^{-6}	3134	31.4
Top fillets	4 solder joints	20.7×10^{-6}	45.2×10^{-6}	2449	30.7

The cumulative aging temperatures were calculated for the bottom and top fillet data. Those values were: *bottom, 56°C (132°F)* and *top, 63°C (145°F).* These temperatures are considerably greater that the value of 24°C (75°F) that was determined from the intermetallic

compound layer thickness data. Similar particle sizes were observed in the interconnect circuit board solder joints, as well. In both that case and the internal circuit board case here, the cumulative aging temperatures calculated from the Pb-rich phase size distributions were considerably greater than those temperatures predicted from the intermetallic compound layer growth. The additional aging indicated by the Pb-rich phase size is most likely the result of accelerated coarsening of the Pb-rich phase particles caused by mechanical loading of the joint. Temperature cycling can impose stresses and, consequently, deformation on the solder because of thermal expansion mismatch between the various materials in the joint (solder, lead material, and printed circuit board laminate). In addition, the potting material on the internal circuit board and sealant rubber on the interconnect circuit board would have potentially impacted those thermal expansion mismatch loads, as well.

3.3.6 Terminal/Pole Connector—Qualitative (Defect) Analysis

As in the case of the N57 unit, the terminal/pole connector (1440097-3, BBN4797) solder joints from the fielded B61 hardware were also examined. The configuration of the connector is the same as was shown in Figures 24 and 25 from the N57 unit. The analysis was limited to a qualitative survey of the various solder joints. Generally, the appearance of the joints in the primary connector structure was similar to those observed in the N57 unit (Figure 24a and Figures 25a-d). However, the pin-to-pin solder joint in the B61 radar exhibited cracking, unlike the similar joints from the N57 unit that is shown in Figure 24b and at a higher magnification in Figure 25e. There are two such solder joints in the B61 radar assembly—both exhibited cracking. This defect from the "right-hand" connection is shown in a low-magnification photograph in Figure 34a; the "left-hand" connection is presented in Figure 34b. It is observed that the fracture in Figure 34b occurred at the toe of the fillet, which in Figure 34a has formed well lower down the profile of the fillet, and was largely a surface crack of minimum depth. Using optical microscopy, a higher magnification cross-section view of the failure in Figure 34b is shown in Figure 34c.

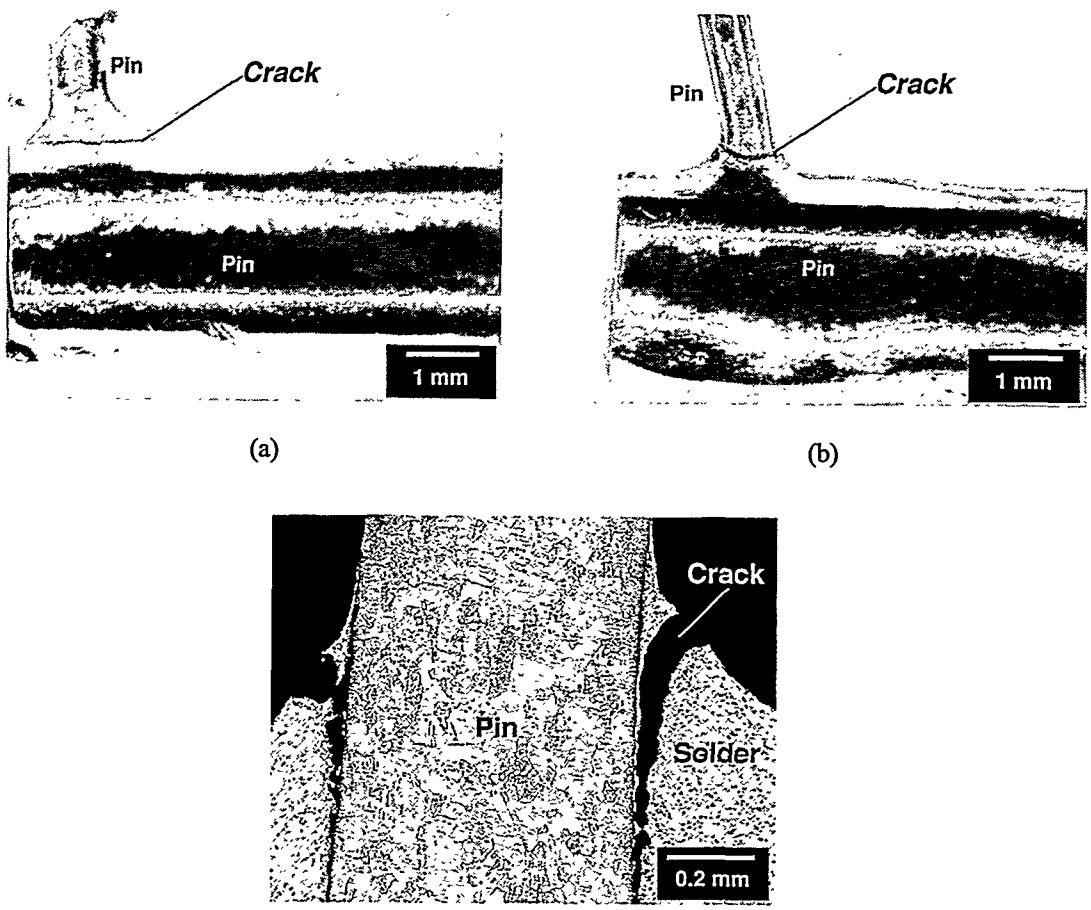


Figure 34. (a) Low magnification photograph of the "right-hand," pin-to-pin solder joint in the terminal/pole connector of the B61 radar, showing the crack that had formed in the solder joint. (b) The "left-hand" connector joint is shown in this photograph. (c) Optical micrograph shown a cross-section of the cracked area of the "left-hand" joint.

The source of the cracking remains ambiguous. There are two likely scenarios:

1. The cracks were caused by excessive mechanical loads, which may have occurred during assembly/disassembly activities and/or rework steps; or.

2. The source was thermal mechanical fatigue (aging) arising from temperature fluctuations encountered during next-assembly operations or while the radar was in the stockpile.

Closer examination of the cross-sections of *both* solder joints (left and right) showed some evidence of Pb-rich phase coarsening preferentially around the cracked area—an observation that would favor some degree of cyclic damage in the solder. While a portion of that fatigue strain would arise from the local thermal expansion mismatch between the Cu-based pin material and the solder, global mismatches cannot be ruled out, considering the various materials comprising the other structures to which the pin is connected and the relatively large distances covered by the parts. The failure paths occurred near the interface formed between the solder and the intermetallic compound layer that adjoined the Cu. Because this failure morphology can also be attributed to a mechanical overload, it is not possible to state with absolute certainty that stockpile aging was the source of cracks in the terminal/pole connector, pin-to-pin solder joints. Nevertheless, a comparison of the cumulative-aging temperatures calculated from the intermetallic compound layer thickness measurements against those determined from the Pb-rich phase-size distributions indicated that the B61-0 solder joints were exposed to thermally driven-aging processes, including the possibility of thermal mechanical fatigue, that accelerated the coarsening rate of the Pb-rich phase particles.

4. Summary Analysis

It is important to summarize and compare the data presented in this study in order to identify any generalized trends of solder joint aging, or to find any specific behaviors in the B61 tube-type radar electronics. The following summations have been categorized according to the three test vehicles used in this study:

1. the baseline test vehicle,
2. N57 tube-type radar circuit boards, and
3. the field-returned, B61(0) radar unit circuit boards.

Suitable comparisons between test vehicles will be made to effectively illustrate one or more particular points. The aging data have been summarized in Table 23 to assist in the analyses. All cumulative, isothermal aging temperature computations were based on an assumed lifetime of 35 years.

Table 23
Aging Data Summary

System Hardware	IMC Thickness μm (st. dev.)	Aging Temp. IMC °C(°F)	Pb-rich Phase Size x 10^{-6} mm^2 (st. dev.)	Aging Temp. Pb-rich Phase °C (°F)
Base	0.71 (0.27)	*****	3.2 (6.5) *bottom and top*	*****
N57 Interconnect Bd. Leaded Joints	0.87 (0.53)	12 (54)	3.8 (11) *bottom*	-14 (6)
N57 SA1126 Connector	0.86 (0.28)	12 (54)	21 (43) *bottom* 13 (23) top	64 (147) 46 (115)
N57 Terminal/pole Connector	*****	*****	16	53 (128)
B61 Interconnect Bd. Leaded Joints	1.67 (0.29(	38 (100)	18 (69) *bottom* 18 (65) *top*	57 (135) 59 (138)
B61 Internal Bd.	1.08 (0.26)	24 (75)	17 (33) *bottom* 21 (45) *top*	56 (132) 63 (145)

Baseline test vehicle data. The baseline, through-hole test vehicle established the "as-fabricated," mean intermetallic compound layer thickness at *0.71 μm*, and the mean Pb-rich phase size at *3.2 x 10^{-6} mm^2* for joints made with 63Sn-37Pb solder (or 60Sn-40Pb solder). The Pb-rich particle-size parameter was based on measurements taken of the ceramic DIP, CK0 capacitor, and TO18 transistor solder joints that were confirmed to have had a Pb content commensurate with the use of the 63Sn-37Pb solder. The baseline, Pb-rich phase particle metric was adapted to represent the baseline value for *all* locations within a joint structure (bottom fillet, top fillet, and hole).

The wire-wound resistor-solder joints had higher Pb-contents than would be expected of joints made with 63Sn-37Pb solder. The combined, mean Pb-rich phase-particle sizes for the wire-wound resistor solder joints reflected the greater Pb content, being 4.2×10^{-6} mm^2 for the bottom fillets, 4.1×10^{-6} mm^2 for the hole interior, and 5.4×10^{-6} mm^2 for the top fillet. However, intermetallic compound layer thicknesses were not significantly different from those measured with the other components and were thus included in the baseline metric.

N57 tube-type radar. The intermetallic compound layer thickness of the leaded (discrete component) solder joints on the interconnect (junction) circuit board was measured to be 0.87 ± 0.53 μm. The mean Pb-rich phase-particle size, which was determined at the bottom-side fillet (i.e., the non-component side of the printed circuit board) of the through-hole joint, was $3.8 \pm 11 \times 10^{-6}$ mm^2. The Pb-rich phase area percent measurements confirmed that the joint contained eutectic or near-eutectic solder. The corresponding cumulative aging temperatures calculated from the intermetallic compound layer thickness and mean Pb-rich phase size were 12°C (54°F) and -14°C (6°F), respectively. Qualitatively, these temperature values indicate that the solder joints exhibited very little aging throughout an assumed lifetime of 35 years. These temperatures are not commensurate with the laboratory-like environment to which this part was exposed throughout most of its lifetime. Thus, they illustrate the error that can develop when aging effects are small as compared to the baseline value itself, which may have deviated slightly from the actual value of the hardware.

Cracking of the solder fillets that formed between the eyelet and the Cu pad was observed in 50% of the top-side fillet "quadrants" and only 17% of the bottom-side quadrants as compiled from the cross-sectioned, leaded interconnect board solder joints. Two thermal-fatigue analyses were performed on the solder joint, based on the assertion that thermal expansion mismatch between the lead material and the circuit board laminate (z) was the source of the deformation in the solder material. Those analyses indicated that the soldering process contributed significantly to fatigue damage, as would have daily temperature variations over the course of 1-2 years of stockpile lifetime; the latter circumstance would be considered as an infant mortality loss rather

than a long-term aging-related failure. Moreover, no further failures would be expected during lifetime extension. The fact that the circuit board holes were also electroplated with Cu along the walls provided a redundant path over which the signal might reach the lead and/or conductor features on the opposite side of the circuit board.

The same microstructural analyses were performed on the SA1126 connector solder joints made to the interconnect board of the N57 unit. The intermetallic compound layer thickness was recorded to be $0.86 \pm 0.28\ \mu m$. The Pb-rich phase particle distributions were determined at both the top and bottom side solder fillets; those values were $21 \pm 43 \times 10^{-6}\ mm^2$ *(bottom)* and $13 \pm 23 \times 10^{-6}\ mm^2$ *(top)*. The total area percent Pb in the solder joint fillets corresponded to concentrations within the range of eutectic or near-eutectic Sn-Pb solder use. The effective, isothermal aging temperatures were:

1. intermetallic compound layer thickness, 12°C (54°F);
2. Pb-rich phase-particle size (bottom), 64°C (147°F); and
3. Pb-rich phase-particle size (top), 46°C (115°C).

The intermetallic compound layer "temperature" corroborated that which was computed for the leaded solder joints on this circuit board. The higher aging temperatures recorded from the Pb-rich phase size suggested that the fabrication process and, in particular, the cooling rate of the joints, was significantly different from that of the typical leaded joints that made up the baseline data. Therefore, the baseline measurements of Pb-rich phase-particle size as described earlier would not be applicable to connector joints.

Cracking of the solder fillet that formed between the eyelet and Cu pad was not observed in the connector pins solder joints. However, damage at the interface between the Cu pad (or land) and the underlying laminate was observed in 58% of the top "quadrants" and 33% of the bottom "quadrants." The cracks, which had lengths of 10% to 50% of the distance under the Cu/laminate bond, started at the outer edge and ran toward the hole. The defect was not of a magnitude that would jeopardize the functionality of the joint.

The terminal/pole connector solder joints were examined. The joints made to Au-plated surfaces showed a high concentration of Au in the solder, indicating that the Au had not been removed from those prior to the soldering step. However, cracking of the solder joints was not observed. A quantitative analysis was performed to determine the Pb-rich phase particle-size distribution in one of the Sn-Pb solder joints. A mean particle size of 15.8×10^{-6} mm^2 was measured. Although the corresponding cumulative aging temperature of 53°C (128°F) would suggest a rather extreme thermal environment, it was surmised that the baseline data would not be applicable for the geometry of the terminal/pole solder joint.

B61 tube-type radar. The Pb-rich phase area percent measurements confirmed that the joints contained eutectic or near-eutectic solder. The intermetallic compound layer thickness of the leaded (discrete component) solder joints on the interconnect (junction) circuit board was measured to be 1.67 ± 0.29 μm. The mean Pb-rich phase-particle sizes, which were measured at both bottom-side and top-side fillets of the through-hole joint, were not significantly different at $18 \pm 67 \times 10^{-6}$ mm^2 and $18 \pm 65 \times 10^{-6}$ mm^2, respectively. The cumulative aging temperature calculated from the intermetallic compound layer thickness was 38°C (100°F). The Pb-rich phase-particle size measurements yielded similar temperatures of 57°C (135°F) for the bottom-side fillet and 59°C (138°F) for the top-side fillets. The intermetallic compound layer thicknesses clearly indicated that a modest degree of thermal aging had taken place in the solder joints. However, coarsening of the Pb-rich phase particle indicated that additional aging had occurred in the solder, likely the result of residual stresses imposed on the solder by the thermal expansion mismatch between the lead and laminate materials. The additional aging of the solder microstructure would represent a loss of thermal fatigue life for those interconnects.

As was the case with the N57 interconnect circuit board solder joints, the interconnect circuit board solder joints in the B61 unit used the through-hole configuration that contained an eyelet. Cracks passing completely through the fillet were not observed; partial cracks were recorded in 30% of the top-side fillet quadrants and 2% of the bottom-side fillet quadrants. These values represent a reduced extent of damage than was observed in similar joints on the N57

unit (with cracks on 50% of the top-side fillet quadrants and 17% of the bottom-side fillet quadrants). However, the B61 data must also be qualified by the fact that a full 91% of the solder joints in the B61 junction board also contained assembly defects that included partial hole fill or incomplete formation of the top-side fillets. These defects were surmised to reduce the frequency of eyelet cracking.

Solder joints contained in the internal circuit board from segment #4 of the B61 radar assembly showed degrees of aging, as determined from the intermetallic compound layer thickness and Pb-rich phase-particle sizes, that were generally on par with those observed with the interconnect circuit board. The intermetallic compound layer thickness of the leaded (discrete component) solder joints on the interconnect (junction) circuit board was measured to be $1.08 \pm 0.26\ \mu m$. The mean Pb-rich phase-particle size, which was measured at both the bottom-side and top-side fillets of the through-hole joint, were $17 \pm 33 \times 10^{-6}\ mm^2$ and $21 \pm 45 \times 10^{-6}\ mm^2$, respectively. The Pb-rich phase area percent measurements confirmed that the joint contained eutectic or near-eutectic solder. The corresponding cumulative aging temperature calculated from the intermetallic compound layer thickness was 24°C (75°F). This value is slightly lower than that computed from the intermetallic compound layer thicknesses of the interconnect circuit board solder joints (38°C, 100°F) and suggests slightly reduced temperature excursions as a result of the enclosed and potted environment. The cumulative aging temperatures determined by the mean Pb-rich phase sizes of bottom-side and top-side fillets, 56°C (132°F) and 63°C (145°F), respectively, nearly equaled values determined from the interconnect board. This similarity confirmed that, in both cases, accelerated coarsening of the Pb-rich phase had occurred. The effects of the covering or potting material on solder joint stresses cannot be ruled out.

Some cracking was observed in the terminal/pole connector, pin-to-pin solder joints. Nevertheless, the joints remained functional; all other joints within that assembly were defect free.

The above analyses of the B61-0 tube-type radar-solder joints indicated two important points.

1. The microstructural metric of intermetallic compound layer growth confirmed that overall, stockpile aging of solder joints caused by nominal environmental temperatures was limited. However, the Pb-rich phase-particle size metric clearly indicated that supplemental aging mechanisms arising from stress/strain effects had taken place in the solder joints.
2. The extent of further aging arising from an additional 20 years of stockpile life was approximated. For the metric of the intermetallic compound layer growth, a worst-case isothermal aging temperature of 38°C (100°F) was used. The resulting layer thickness would be 1.99 μm. If it is assumed that the layer growth is entirely a result of the formation of the Cu_6Sn_5 stoichiometry, then the corresponding loss of Cu was be 0.71 μm [22].

The *minimum* Cu feature thickness of all of the analyzed solder joints in the B61 radar was measured at the hole walls of solder joints from the internal circuit board—that value was 62 μm. Therefore, it is not likely that intermetallic compound layer growth will consume an appreciable amount of the Cu feature so as to jeopardize the integrity of the solder joints.

The impact had by an additional 20 years of stockpile life on the Pb-rich phase-particle size is also examined. However, the previous calculation of cumulative temperatures (listed Table 23) can only indicate that, in fact, accelerated coarsening of the Pb-rich phase particles had taken place. That conclusion is drawn simply through a comparison with the same calculation based on the intermetallic compound layer thickness data. It *cannot* be assumed that additional coarsening of the Pb-rich phase will be predicted by the same Equation 28, using an aging temperature of approximately 59°C. Certainly, the isothermal coarsening component of the overall coarsening effect for the additional 20 years can be computed, based upon the cumulative aging temperature of 38°C (100°F) indicated by the intermetallic compound layer growth (Table 23). The increase

would be 0.3×10^{-6} mm^2 above the 18×10^{-6} mm^2 value currently observed. However, the kinetics of the "stress-assisted" coarsening component of the Pb-rich particles are not known at this time. (The stress state of the solder in the joints is not immediately known but could be readily determined by finite element analysis.) Therefore, the extent of accelerated coarsening that may be predicted from temperature cycles and the configuration of the solder joint cannot, as yet, be determined.

An important point to be determined is whether the B61-0 radar solder joints having this Pb-rich phase size are, or will become, more susceptible to thermal mechanical fatigue deformation and/or fatigue cracking under the *anticipated* 20 additional years of stockpile environment. Moreover, the impact on solder joint functionality and by the additional fatigue damage must be ascertained. Although at present, exceptional progress has been made in both modeling and experimental validation efforts on solder interconnect reliability, the point has not been reached in either aspect that would enable a conclusive answer to be drawn. Ancillary studies on connector solder joint configurations have shown that cracking began when the fillet, Pb-rich phase size in the joints reached 15-18 x 10^{-6} mm^2 after being exposed to continuous, accelerated testing conditions (-55°C, 100°C, 6°C/min, 15 min hold times, 1000 cycles) [21]. The applicability of this result to the B61-0 solder joints has not been confirmed. Therefore, although the current state of solder joint fatigue research cannot determine conclusively that simply having a mean Pb-rich phase-particle size in the range of 15-18 x 10^{-6} mm^2 implies that fatigue cracking is imminent, this scenario cannot be dismissed outright until ongoing studies have been completed.

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