7-20-95

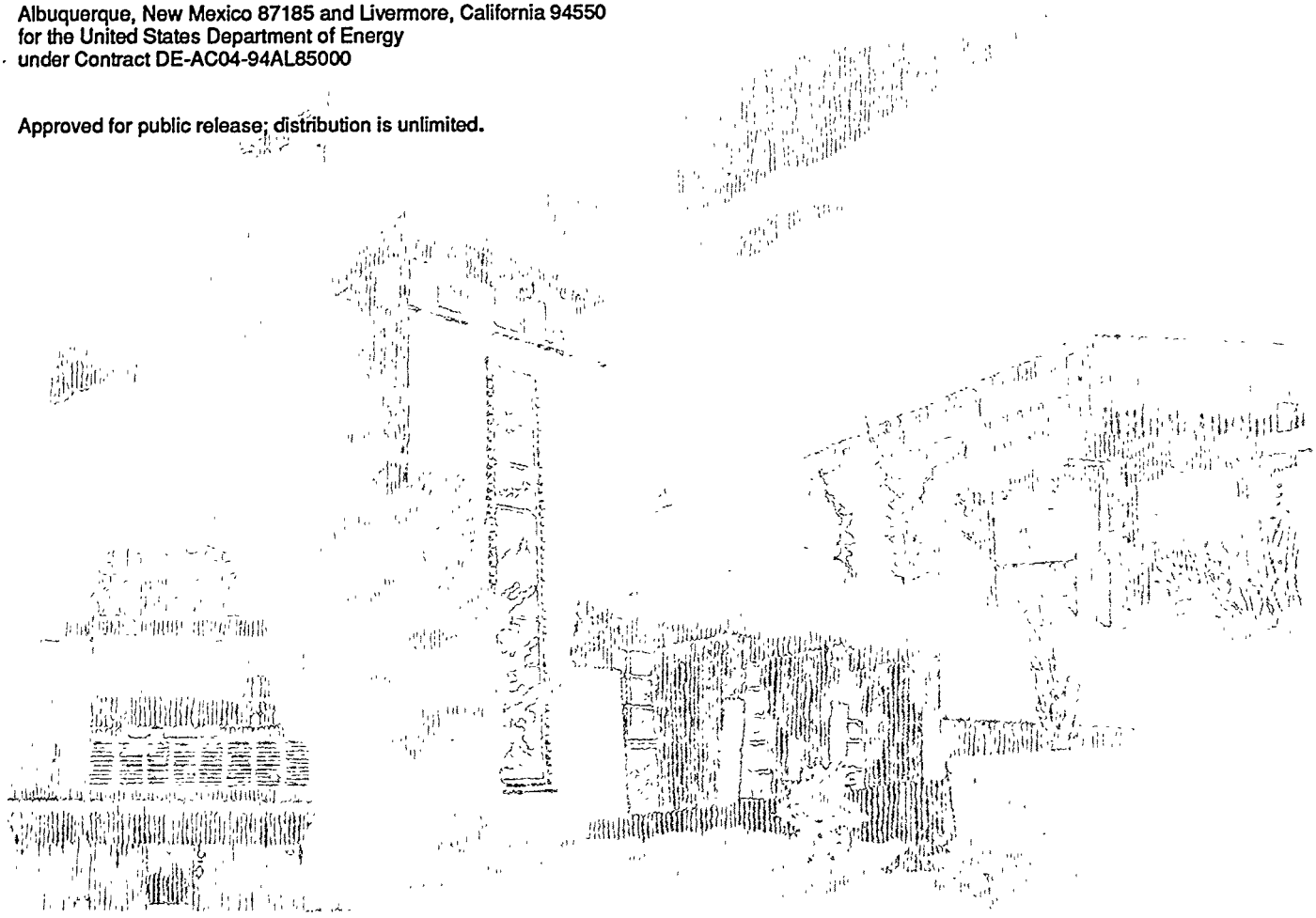
SANDIA REPORT

SAND95–0861 • UC–706
Unlimited Release
Printed May 1995

Smart Substrates: Making Multi-Chip Modules Smarter

Thomas F. Wunsch and R. Keith Treece

Prepared by
Sandia National Laboratories
Albuquerque, New Mexico 87185 and Livermore, California 94550
for the United States Department of Energy
under Contract DE-AC04-94AL85000



SF2900Q(8-81)

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Distribution Category
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Smart Substrates: Making Multi-Chip Modules Smarter

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Abstract

A novel multi-chip module (MCM) design and manufacturing methodology which utilizes active CMOS circuits in what is normally a passive substrate realizes the 'smart substrate' for use in highly testable, high reliability MCMs. The active devices are used to test the bare substrate, diagnose assembly errors or integrated circuit (IC) failures that require rework, and improve the testability of the final MCM assembly. A static random access memory (SRAM) MCM has been designed and fabricated in Snadia's Microelectronics Development Laboratory in order to demonstrate the technical feasibility of this concept and to examine design and manufacturing issues which will ultimately determine the economic viability of this approach. The smart substrate memory MCM represents a first in MCM packaging. At the time the first modules were fabricated, no other company or MCM vendor had incorporated active devices in the substrate to improve manufacturability and testability, and thereby improve MCM reliability and reduce cost.

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Acknowledgements

The authors thank Paul Dressendorfer, manager of the Multi-Chip Module Department, for very helpful discussions regarding both technical and managerial aspects of this project. We would also like to thank Harold Stewart, Tom Hill and the rest of the Sandia Microelectronics Development Laboratory staff for their efforts in successful fabrication of the first Smart Substrate Multi-Chip Module, Nao Moore of the Packaging Assembly Laboratory for her patience in assembling the prototype modules, Scott Bieber for his proficiency in module layout and Arturo Gonzalez of the University of Texas at El Paso for his assistance in writing and executing the boundary scan test routines.

Nomenclature

ANSI American National Standards Institute

BSDL Boundary Scan Description Language

BIST Built-in Self Test

CTE Coefficient of Thermal Expansion

CMOS Complimentary Metal Oxide Semiconductor

COB Chip on Board

DC Direct Current

DFT Design for Testability

DSP Digital Signal Processor

ESD Electro-Static Discharge

GPIB General Purpose Interface Bus

HTCC High Temperature Cofired Ceramic

IC Integrated Circuit

IEEE Institute of Electrical and Electronic Engineers

I/O Input/Output

LFSR Linear Feedback Shift Register

LTCC Low Temperature Cofired Ceramic

MCM Multichip Module

PCB Printed Circuit Board

PGA Pin Grid Array

SRAM Static Random Access Memory

TAP Test Access Port

Smart Substrates: Making Multi-chip Modules Smarter

1 Introduction

The trend to Multi-chip Modules (MCM) is producing higher density and improved performance over the hermetic single chip package approach. However, dense packing of bare integrated circuits (IC) on substrates having passive interconnection only substrates also raises a host of challenges: pretesting the bare chips, diagnostic testing of the assembled substrate, substantial distribution of high quality DC power to the chips, signal noise, impedance matching, and dissipation of generated heat. Each of these problems can lead to a failure in operation of the MCM system. As a result, extremely difficult testing requirements are placed on the MCM system. Rather than trying to meet all these testing difficulties by the expensive customization of each IC (by adding built in test features), an approach is proposed using standard commercial ICs assembled on a smart interconnection substrate. These interfaces are "smart" in that they use active CMOS devices fabricated in the MCM silicon substrate to solve many of these system test challenges.

2 Multi-Chip Module Technology: The Need for Cost Effective Test Solutions

2.1 Multi-Chip Module Technologies

An MCM is a structure consisting of two or more ICs (typically bare chips) interconnected on a common supporting substrate (Figure 1). The substrate conductors are usually formed in multiple layer structures that are separated by dielectric material. Vias vertically connect the various layers. MCMs usually permit wiring densities covering up to 90% of the substrate, whereas only 10% coverage is typical on conventional printed circuit boards (PCBs).

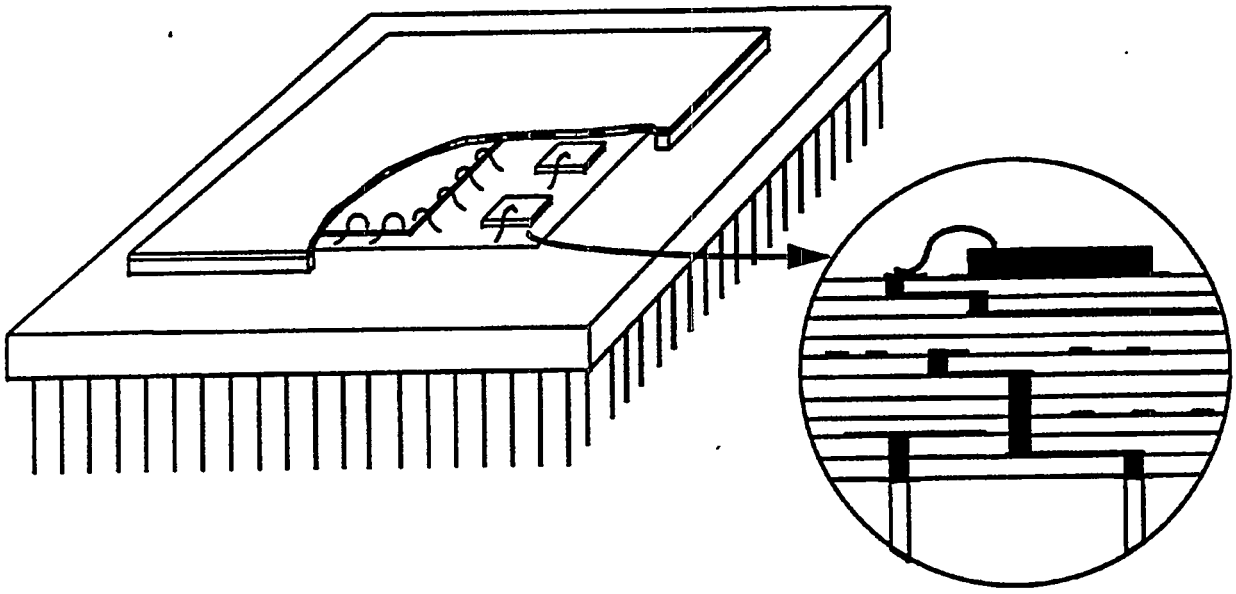

Figure 1: Schematic drawing of an MCM structure.

MCMs have been around for a long time, though not in the same form as seen today. Microelectronic devices with more than one active device or chip existed earlier as a hybrid microcircuit. Hybrids are defined as circuits that include at least two components–one of which is an active semiconductor device–manufactured by a combination of technologies and joined on a common substrate. MCMs grew out of the hybrid market, and while both are variations of the same species, certain characteristics distinguish true hybrids from true MCMs:

- Hybrids were originally thick film based, while MCMs tend to have a thin film structure. This difference has diminished over the years as hybrid technology has adopted more thin film procedures. Some MCM manufacturers use thick film or a combination of thick and thin film technologies.

- Hybrids typically contain a few active devices surrounded by a number of discrete

passive devices, e.g., resistors and capacitors. MCMs, on the other hand, typically contain more active devices, including microprocessors, memory, and logic devices. Some MCMs have been built with 50 to 100 ICs.

2.1.1 MCM Substrate Technologies

MCMs are most commonly classified by their substrate technology:

MCM-L (laminate): These modules use advanced printed wiring board technologies, copper conductors, and laminate based dielectrics.

MCM-C (ceramic): Circuitry for these MCMs is formed using thick film (screen printing) technologies on cofired ceramic substrates. (Cofired means that all circuit layers are sintered in an oven concurrently.)

MCM-D (deposited): Interconnections are formed by the thin film deposition of metals on deposited dielectrics of polymer or inorganic compounds. Silicon is a common substrate material used for MCM-D. One variation is the use of aluminum conductors and SiO_2 as the inorganic dielectric media. Very fine feature sizes are possible and conventional IC fabrication equipment can be used.

MCM-L MCM-L is basically an extension of chip-on-board (COB) assemblies where bare or micro-packaged chips are wire bonded or soldered to conventional PCBs. MCM-Ls most often contain relatively few semiconductor devices.

A majority of MCM-Ls have between six and eight layers. Frequently there are two to four signal layers, the remainder being power, ground, and pad layers. Typically, line widths and spaces are 3 to 5 mils and hole diameters are 8 to 12 mils. Surface pad pitch can be as low as 0.010 to 0.008 in. Bond pads are usually finished in gold to accommodate wire bonding, which is the most commonly used chip connection.

An obvious advantage of MCM-Ls is cost. Switching to MCM-Ls results in at least a 5X cost reduction over MCM-D and a 2X reduction over MCM-C. Other advantages include the availability of well known manufacturing processes using proven materials with repeatable characteristics and the ability to batch produce, to provide copper conductors of varied thickness and cross section over a controlled dielectric thickness, and to have assemblies with components on both sides of the substrate.

MCM-Ls are beginning to find wide use in the computer and workstation industry today. They are used in test equipment, measurement instruments, advanced memory cards, optical displays, mobile telephones, calculators, and hand-held video games.

MCM-C Ceramic based MCMs have been used in the electronics industry for over 20 years. MCM-Cs are hybrid circuits with bare chips mounted on substrates and interconnected using screen printed conductor materials. The technology is an extension of thick film hybrid and cofired ceramic single chip package technologies. Early MCM-Cs employed cofired alumina ceramics with refractory metallization. MCM-C structures now use either thick film

multilayer, high temperature cofired ceramic (HTCC) or low temperature cofired ceramic (LTCC) technologies with copper metalization.

MCM-C substrates are increasingly being used in mainframe computer applications, implantable medical electronics, and various defense applications. An LTCC MCM is illustrated in Figure 2.

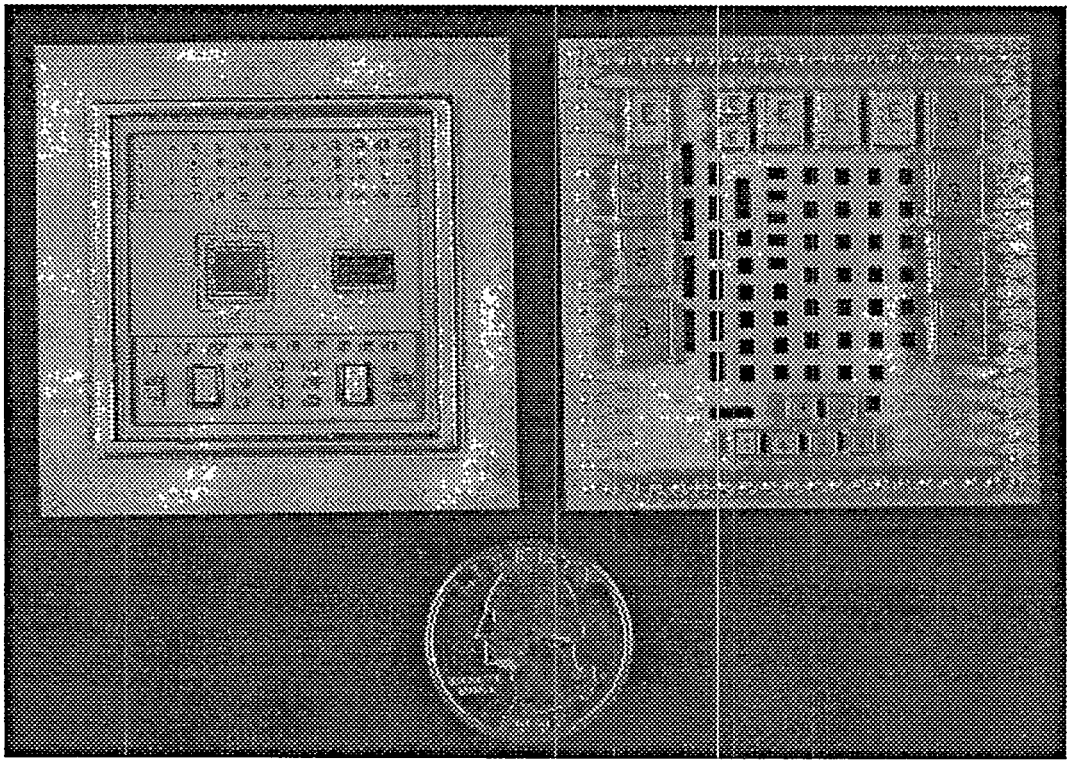

Figure 2: An MCM fabricated with LTCC substrate technology.

MCM-D MCM-D utilizes IC technology to produce high density thin film interconnections. In MCM-Ds, thin film metal signal conductors are sandwiched between unreinforced dielectric insulation on a silicon, ceramic, metal, or PCB laminate support. A typical implementation of MCM-D is illustrated in Figure 3.

The "D" in MCM-D refers to the deposited dielectric used to fabricate the MCM substrate. Polymers are the most commonly used dielectrics, although other materials such as plasma deposited SiO_2 are also used. Polymers are deposited from an appropriate solvent by spin or spray coating. They should have a low dielectric constant, good adhesion to the support and the metallization, low water absorption, good planarization characteristics, and compatible thermal properties and mechanical properties.

MCM-Ds are manufactured using IC techniques, such as photolithography, sputtering, and wet and dry etching to create the interconnect. This technology offers the highest interconnect density of the MCM categories. MCM-D fabrication allows the creation of 10 to 20 μm vias, i.e., vias significantly smaller than those that can be manufactured by other means such as drilling and punching.

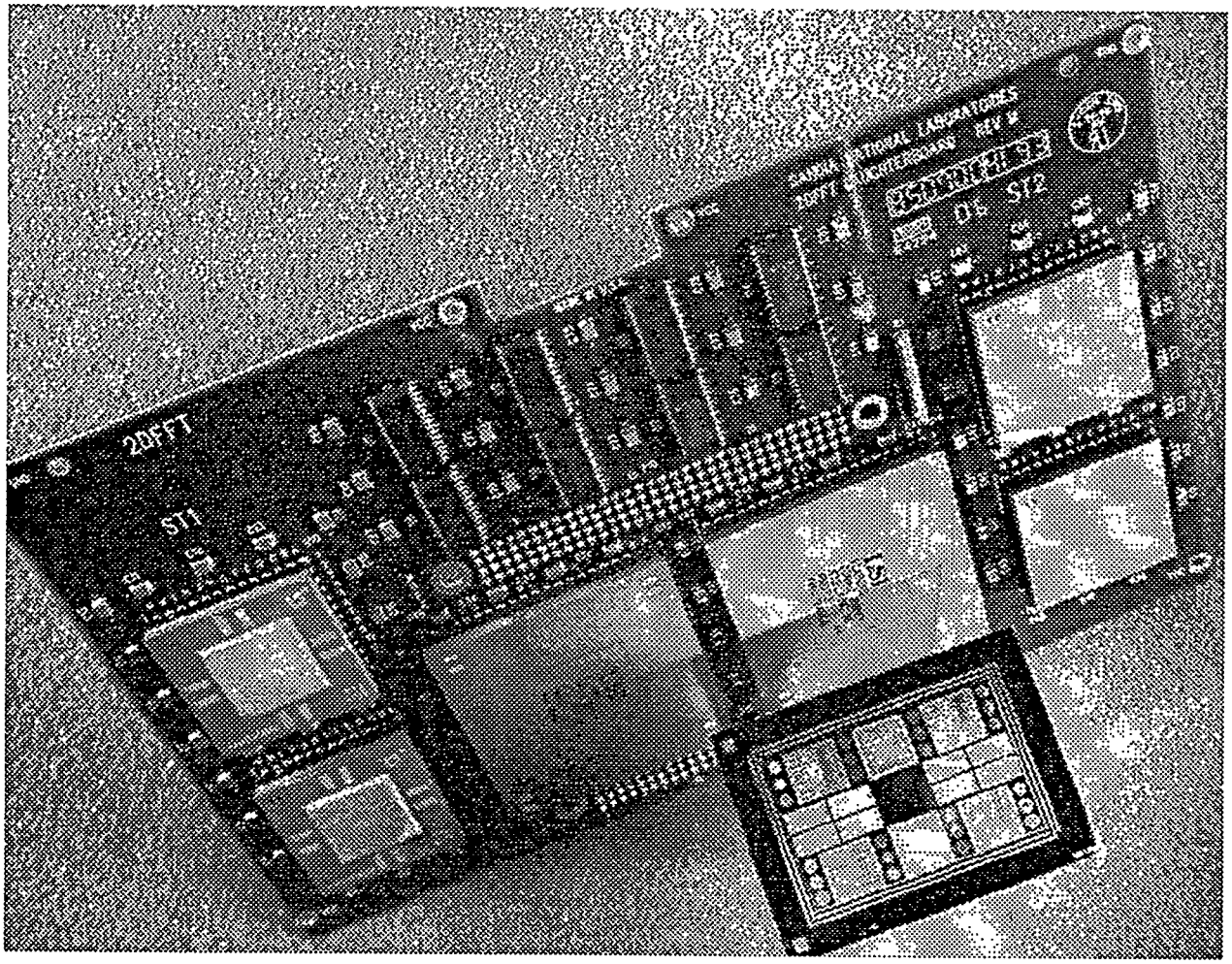

Figure 3: An MCM fabricated with MCM-D technology and its much larger PCB counterpart.

Conductors are deposited by sputtering, evaporation, or electroplating techniques and are patterned by common photolithography and etching techniques. Polyimide film patterning is accomplished with wet or dry etching, or by laser ablation.

MCM-D provides shorter signal paths and produces lower capacitive loading and reduced circuit noise. The lower dielectric constant of the MCM-D polymer insulation layers and the shorter signal path lengths result in faster clock rates for a given system.

MCM-D technology may also employ a conventional silicon wafer substrate, aluminum as the conductor, and silicon dioxide as the inorganic dielectric medium. Vacuum deposition is used to deposit the SiO_2 dielectric layer. Wafer spinners and mask aligners are used to apply and pattern the photoresist. Very fine feature sizes are possible due to the extremely smooth, flat silicon wafer surface.

High signal interconnection density and an excellent CTE match to the silicon die are some of the advantages of MCM-D. For high frequency applications, the higher resistivity of aluminum over copper and the higher dielectric constant and normally thinner layers of SiO_2 over polyimide are disadvantageous. Currently, MCM-D has the greatest extendibility to future very high performance systems, but current pricing is impeding high volume production.

2.2 Multi-Chip Module Test Techniques

2.2.1 Boundary Scan Testing

Boundary scan is a built-in technique for testing an assembled printed-circuit board or MCM – specifically, the digital ICs and their interconnections. Its key feature is the insertion in every IC of small logic circuits, called boundary-scan cells, between each pin and the chip circuitry to which that pin normally is directly connected (Figure 4). In addition to their connections to the chip pins and the working logic, the boundary-scan cells have other terminals through which they can be connected to each other in series, forming a shift-register path around the periphery of the IC.

During normal operation, data is passed between pins and logic as if the boundary scan cells were not there. When put into the test mode, however, they can be directed by a test program to pass data along the shift-register path, which need not be confined to a single chip, but can encompass the entire board or MCM. Once data has been loaded into the cells, it can be used instead of the normal data flowing to or from the pins, so that either the internal logic or the external chip-to-chip connections can be tested. Boundary scan thus can put desired test sequences wherever they are needed. It also makes it easy to distinguish testing the chips themselves from testing the connections between chips.

The ANSI/IEEE Std 1149.1 IEEE Standard Test Access Port and Boundary-Scan Architecture defines a method of communicating test instructions and data from an external test processor to the various ICs on a board or MCM .

Four or five extra pins are required on an IC that complies with the ANSI/IEEE standard. These pins constitute the test access port, or TAP. The TAP is analogous to a diagnostic

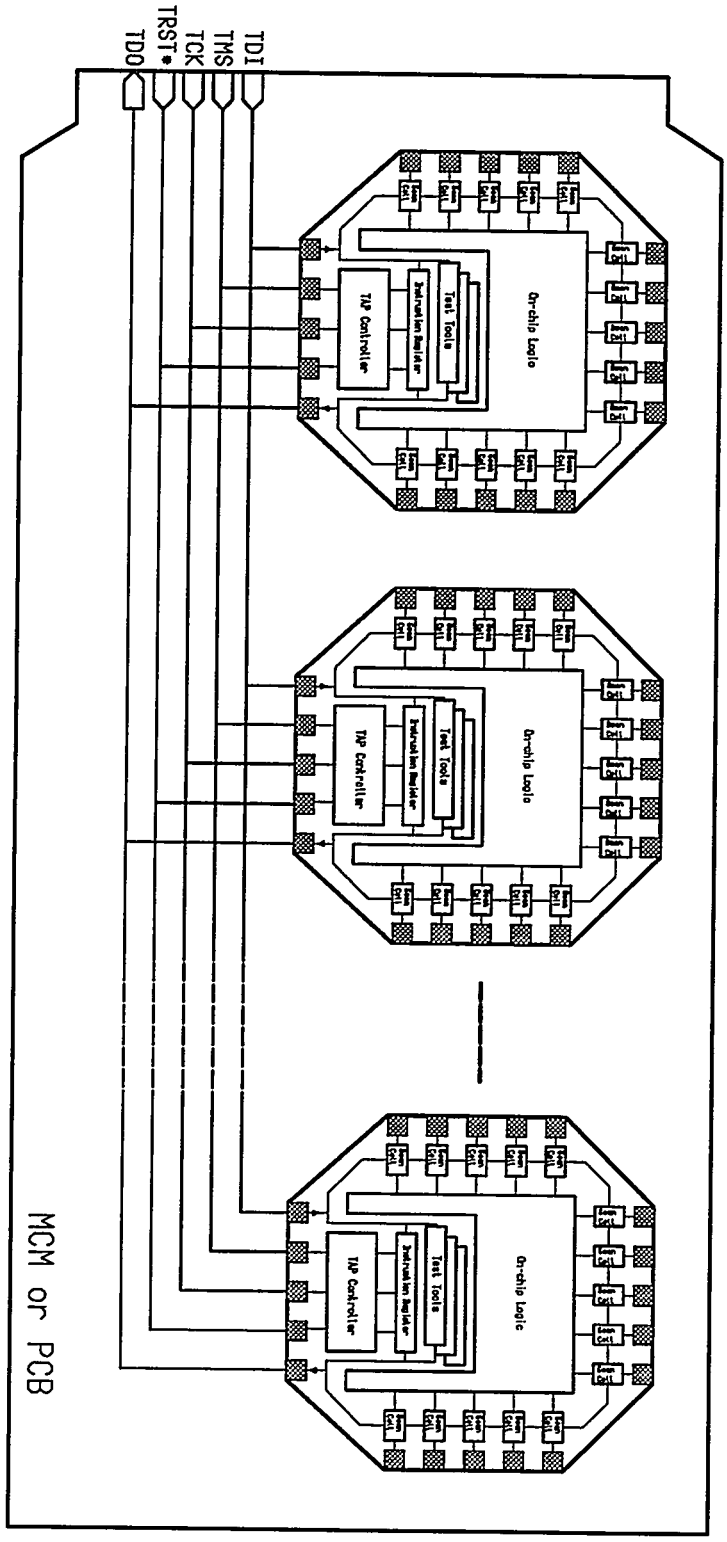

Figure 4: Diagram of a boundary scan daisy chain.

socket: it allows an external test processor to control and communicate with the test features built into the product.

Of the TAP pins, two (test data in, TDI; and test data out, TDO) provide for the serial input and output of data, while the others control the movement and use of data in accordance with a defined protocol. The protocol is interpreted by a small finite-state machine (the TAP controller) that generates internal control signals required to operate the test tools built into each IC. These control signals – Update, Mode, and Shift/Load – determine the operation of the serial shift-register formed by the boundary scan cells.

The TAPs of individual ICs on a loaded board or MCM can be configured to provide a single "daisy-chain" serial data path that snakes its way around the board from one IC to another. Building that single serial path is simple: the TDO of one chip is connected to the TDI of the next chip in the chain. Note that, in the example of Figure 4, the external control signals are not daisy-chained but are broadcast in parallel to all boundary scan ICs. Those control signals are the Test Clock (TCK), Test Mode Select input (TMS), and, optionally, Test Reset input (TRST).

Four principal types of tests can be performed with the boundary scan register. They are: interconnect tests, using the EXTEST (external test) instruction; chip tests, using the INTEST and RUNBIST instructions; sampling, using the SAMPLE instruction; and user defined tests which are custom developed to perform design specific testing functions.

2.2.2 Built-in Self Test (BIST)

BIST is the capability that allows a circuit to test itself. The circuit could be a chip, an MCM, a board, or a system. Various levels of chip level BIST have been used during the past decade. The BIST schemes that are needed for the MCM technology are ones that provide very high fault coverage. The incorporation of BIST and boundary scan in an MCM greatly simplifies the task of obtaining very high fault coverage. In addition, the BIST operation allows system performance testing at operational speeds.

BIST schemes, in general, need hardware facilities for test pattern generation, as well as hardware facilities for output data evaluation. Typically, BIST schemes detect single stuck-at faults in the functional circuitry. Most schemes can detect some other types of faults as well. The ideal BIST scheme would be a generic one that would be applicable to any block in the MCM. However, such a scheme may not be realizable, due to the fact that digital chips consist of blocks of different types of structures, device densities, and fault models associated with each. Hence, specific BIST schemes are needed to test each type of block in order to achieve very high fault coverage.

With BIST and boundary scan incorporated into the chips, most of the testability facilities are ready for the module level tests. In fact, all the BIST and boundary scan capabilities are directly accessible from the MCM boundaries through the four boundary scan lines (TDI, TDO, TMS, and TCK). Even though some commercial chips, such as AT&T's DSP family, Intel's 80486, and Motorola's 68070 microprocessors, offer boundary scan in their products,

the problem of having off the shelf chips without boundary scan will be faced in many MCM products.

2.3 Test Cost Analysis and Selection Metrics

Many test solutions produce unique advantages and disadvantages. As an example, Table x illustrates various solutions that might be available throughout the complete process of producing a fully functional, fault-free, and reliable MCM.

To properly weigh the benefits of the approaches, or combinations of solutions, it is necessary to compare them against a common set of metrics. Two primary quantitative metrics serve as the basis of comparison:

- impact on the cost of the MCM
- impact on the quality of the MCM measured by the defect level (in parts per million) in the produced MCMs.

The selection of cost as one of the comparison metrics reflects the important role that test plays in determining the final cost of an MCM. It also emphasizes the importance of finding cost effective test solutions and not just test solutions at any cost.

The second performance metric serves as a balance against recommending cheap solutions with inferior quality. The defect level (or equivalently, the outgoing yield) of the produced MCM can be used as a measure of quality. Since all alternative test methods should not change the product functionality (DFT methods may result in slight performance degradation), cost and quality become the two prime characteristics for evaluating any product.

2.3.1 Evaluation Criteria for Test Method Selection

In addition to cost and quality, we can use several other criteria to evaluate test strategies. Examples of these criteria are

- Impact of a test strategy on time to market. Although variations in design, manufacturing, test and repair times are ultimately accounted for in the cost, test strategies that result in excessively long times to market must be avoided.
- Adverse impact of a test method on the reliability of the product. For example, certain test methods may cause damage to the IC pads or they may cause thermal overstress. Another example is MCM test strategies that rely on having a high number of rework cycles. The reliability of the product resulting from the rework cycles might be significantly reduced, and should be avoided if possible.
- Usefulness of a method at higher levels of system integration and for field test, diagnosis, and maintenance.
- Impact of a test method on manufacturability. This covers issues such as: How easy is it to adapt this method into existing manufacturing processes? How big must an infrastructure

be to support the new method? How expensive is the equipment required to support this test method?

• Electrical performance degradation caused by a test method. Most DFT methods introduce slight delays into the design. However, proper design of DFT features minimizes effects on the critical paths and reduces the overall DFT performance impact.

2.3.2 Analysis of Available Test Methods

Test techniques developed for the Printed Circuit Board (PCB) arena, such as the use of mechanical probing for in-circuit testing, are not practical for the high pin count, densely packed circuitry of MCMs. Thorough testing is only possible by viewing the MCM as a unique integrated system. This system, from the testing perspective, more closely resembles a large Integrated Circuit than a PCB. Application of IC test techniques, however, can be applied only within the restrictions allowed by the MCM architecture. For example, the IEEE 1149.1 standard boundary scan architecture, which can be designed into an IC to aid in testability, can be designed into an MCM with the limiting restriction that 1149.1 compliant die be available for the die functions required.

Acceptance of the IEEE 1149.1 boundary scan architecture has led to an increasing number of commercially available scan testable die. However, the production of scan testable die is notably absent in several areas, especially for "commodity" type die such as SRAMs. The fact that profit margins are especially low on memory and other commodity die will likely preclude the introduction of scan (and the associated area and pin count overhead) on these die. *The smart-substrate solution alleviates the restrictions of non-scan die by placing the scan circuitry on the substrate in close proximity to the die. The circuitry can be designed to fully test non-scan die within an MCM while accommodating and exploiting the existing scan features of 1149.1 compliant die.*

Traditional IC test strategies rely on the use of expensive high pin-count testers. The use of multi-million dollar IC test equipment for MCM testing may not be economically feasable, particularly for small production runs where the test equipment cost is not supported through economies of scale. *The use of boundary scan circuitry and built in self test removes the restrictions of high cost large pin count IC test equipment since the MCM system is testable through a four or five pin test access port on an inexpensive PC-based test system.*

The application of IC testers in an MCM test strategy is further limited by the fact that the typical MCM will contain a much smaller I/O pin to gate count ratio than the typical IC. The problem for the MCM manufacturer is not simply to determine if the component is good or bad, but to identify faulty die which may then be replaced. The component parts of the MCM system – package, substrate, and die – are usually too expensive to allow the MCM to be discarded to the "bone pile" as is done with ICs. The MCM system must allow diagnosis of faulty components across the natural physical partitions, namely package wire bond connections, substrate, die, and die wire bond or solder bump connections. These points of interconnection are uniquely accessible to test circuitry placed in the MCM substrate. *Module rework and repair costs are significantly reduced for the smart-substrate*

system through the use of diagnostic software and the self-diagnostic features available in the smart substrate boundary scan and BIST circuitry.

3 Smart Substrate Multi-Chip Module Systems

3.1 Smart Substrates Defined

The concept of a smart substrate can be developed by viewing the entire MCM from a system perspective. In order to provide the highest level of integration, each component of the system must be exploited to maximum functional benefit. In the case of a standard MCM-D system, the substrate performs a mechanical function only, providing a platform for supporting electrical interconnect and bond pads as well as providing certain desirable thermal functions. In the smart substrate system, the substrate silicon is exploited to provide electrical test functions that otherwise would not be available in the module design. It is possible to add other electrical functions to the substrate as well, such as driver circuits for signals going off substrate and input ESD protection.

Figure 5 illustrates the main features of the smart substrate system. The system is designed on a large area silicon substrate with active CMOS devices (and possibly bipolar and passive devices) embedded in the substrate material. The performance characteristics of the devices in the substrate are not necessarily critical to obtaining an overall benefit to the system. For example, slower speed glue logic and serial scan test devices may be built into the substrate while performance critical system components are fabricated separately on high volume, high performance IC fabrication lines and are assembled into the system in die form. The interconnect is optimized to provide high speed communication between these high performance devices and may perform secondarily the function of interconnection between the circuits incorporated in the substrate.

The concept of a system with lower performance devices on the substrate allows a more conservative manufacturing approach to the electrical design of the substrate. Conservative design rules and design redundancy and robustness are critical to obtaining an acceptable yield from the large area substrates. By not using the silicon substrate area to state of the art performance and density, it is possible to obtain substrate yields close to the yields of passive interconnect-only substrates. Another advantage of this approach is that it makes economic sense to build substrates in the proven baselined technologies that are not on the forefront of performance and density because these facilities are less expensive than fabrication lines using state-of-the-art equipment and manufacturing techniques.

3.2 Smart Substrate Manufacturing Technology

Development of a smart substrate manufacturing technology requires close attention to lay-out and design procedures in order to maximize the yield of the substrates. In a previous section it has been noted that the current cost factors of MCM-D are preventing this technology from achieving volume production status. In the smart substrate technology this holds true to a larger degree due to the increased cost of designing and fabricating the substrates. It is important, however, to distinguish between commercial high volume, commodity items where the ICs and the entire MCM are inexpensive, and lower volume, high reliability MCMs with expensive ICs. For inexpensive commodity MCMs, cost is the strongest driver and the

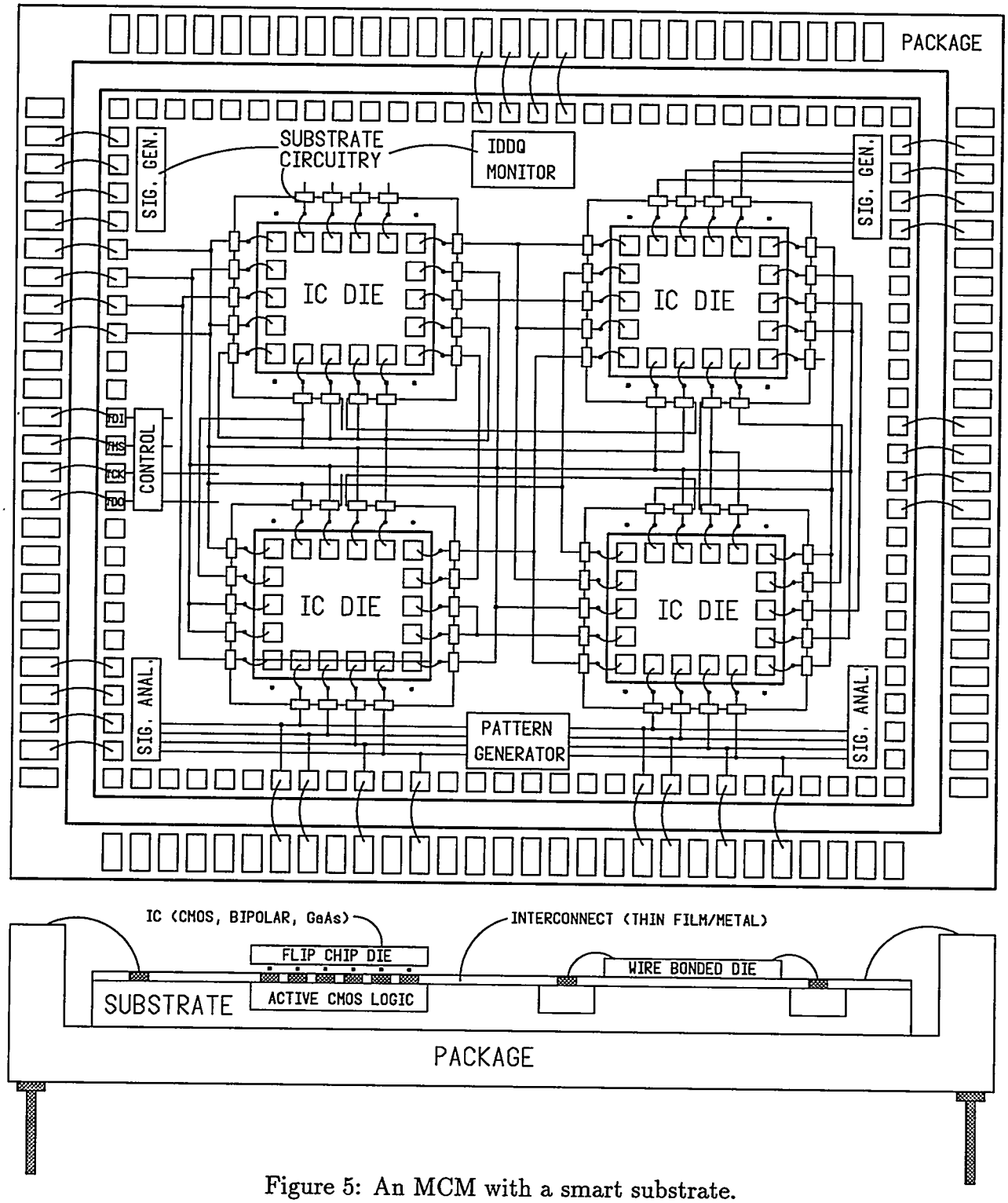

Figure 5: An MCM with a smart substrate.

current trend is to use MCM-L. For high reliability applications, such as weapon or satellite MCMs, MCM-D and smart substrates may be the most appropriate technology.

A key element to the successful implementation of a smart substrate MCM is the degree to which value may be added to the MCM through the added substrate circuitry. The overall cost must be reduced or comparable to an analogous interconnect only design. In an apparent contradiction to this premise, the increased complexity of the smart substrate coupled with its large size makes the substrate more susceptible to low manufacturing yield than its interconnect only counterpart. The remainder of this section presents several guidelines which make the substrate yield issue manageable.

3.2.1 Manufacturing Guidelines

Selection of Process Technology The selection of the process technology should be made with more consideration to cost than performance. For example, the smart substrate may be manufactured in an older process technology, perhaps even an underutilized manufacturing line. This results in two benefits the first of which is the reduced cost over using a state of the art process line. The second benefit is that typically these older technologies are better characterized and more robust and the expectation of acceptable manufacturing yield is higher.

Conservative Performance Goals In line with using an older technology, it is necessary to limit the performance goals of the smart substrate technology. High speed functions should occur in the MCM die, with lower speed operations such as scan testing occuring in the substrate circuitry.

Redundancy in Design and Layout Design and layout redundancy adds additional robustness to the substrate. Additional contacts and vias and multiple transistor transmission gates are two examples of simple redundancy which can be added to the layout. Redundant circuit functions may be added as space permits.

Automation of Design Process Standardization of the boundary scan architecture allows a library of cells to be developed which will have a high level of reuse between different smart substrate designs. Once the cell designs are completely verified, an automated placement utility may facilitate the MCM boundary scan and BIST design.

Automation of Test Development The added substrate circuitry reduces the complexity and cost of testing the assembled MCM by allowing increased access to the internal circuit nodes of the MCM. In addition, test vectors developed for the individual IC die may be serialized and scanned directly to that die on the MCM, thereby reducing test vector development time and aiding in the assembled MCM debugging process. Additional benefits are gained through the use of a standard boundary scan architecture and through development of Boundary Scan Description Language (BSDL) definitions for the test architecture. For

example, interconnect testing may be developed automatically through the use of specialized software.

The circuitry in the substrate, if limited to test functions and perhaps some glue logic, will rely on a small active area relative to the overall substrate size. This will allow the design rules of a technology to be relaxed to the point that very high yields are achievable. Thus, the trade off between a smart substrate and an interconnect only substrate will not be limited by the yield issue. The defining issue will be the relationship between the added substrate cost, the reduced cost of testing the MCM, and the value added to the MCM as a result of higher reliability, testability, and better diagnosis of die failures for more efficient rework.

4 Smart Substrate SRAM MCM Design

4.1 Design Features of the SRAM Module

We designed and fabricated a prototype smart substrate MCM to demonstrate the technical feasibility of the smart substrate methodology and to evaluate circuit and manufacturing techniques which will be required to develop smart substrate MCMs. The prototype is a 4Mb SRAM module. The module consists of 16 Micron MTC5286 32Kx8 SRAM memory die, 2 Sandia SA3294 3x8 decoder die, and 3 Sandia SA3295 8 bit latch die. The decoder die act to decode the high order address lines enabling the chip select lines of the 16 memory die. The latch die act to latch the incoming address lines through a single address strobe signal.

Several factors led to the choice of a memory module as the prototype demonstration vehicle. First, we were familiar with the Micron die through recent project work with the 2DFFT MCM and the repatterned die work at Sandia. The Micron die were readily available in varying levels of quality including availability as KGD. The Sandia die were also available through previous project work and a significant experience base was readily accessible. Secondly, as mentioned previously in this report, memory represents an important area in electronic design where die with boundary scan and other DFT features are not readily available.

Figure 6 is a block diagram illustrating the function of the module. Nineteen address lines act to decode the 512K 8 bit memory word locations. The 15 lowest order address bits are decoded by each of the memory die, while the 4 highest order address bits are decoded by the 2 SA3294 3x8 decoder die which in turn enable one of the 16 memory die. The SA3295 die latch the incoming address lines when the _ADS (Address strobe) line is asserted. The 8 bit memory words are available on the DATA output bus provided the _OE, and _ME lines are asserted. The _OE line, when not asserted, sets the DATA output bus in a tri-state condition. The _ME line, when not asserted, will also tri-state the DATA output bus and will not allow internal toggling of the latched address signals.

An additional feature of the module design, was that the layout was performed such that the memory word size could be altered with the change of a single via mask layer. Although the smart substrate module was fabricated in only the 512kx8 bit configuration, the design would permit fabrication in 256kx16 bit and 128kx32 bit configurations with this single via mask change.

The DFT features incorporated in the smart substrate include a full boundary scan path for each die in the module, a LFSR based BIST algorithm and custom boundary scan cell designs which allow for short circuit and open circuit testing of the unpopulated substrate utilizing a unique current monitoring approach.

The silicon substrate is shown if Figure 7. The substrate measures aprroximately 2.0" x 1.4". The assembled and packaged module is show in Figure 8. The module, in its PGA package, has a footprint of only 2.5" x 1.8".

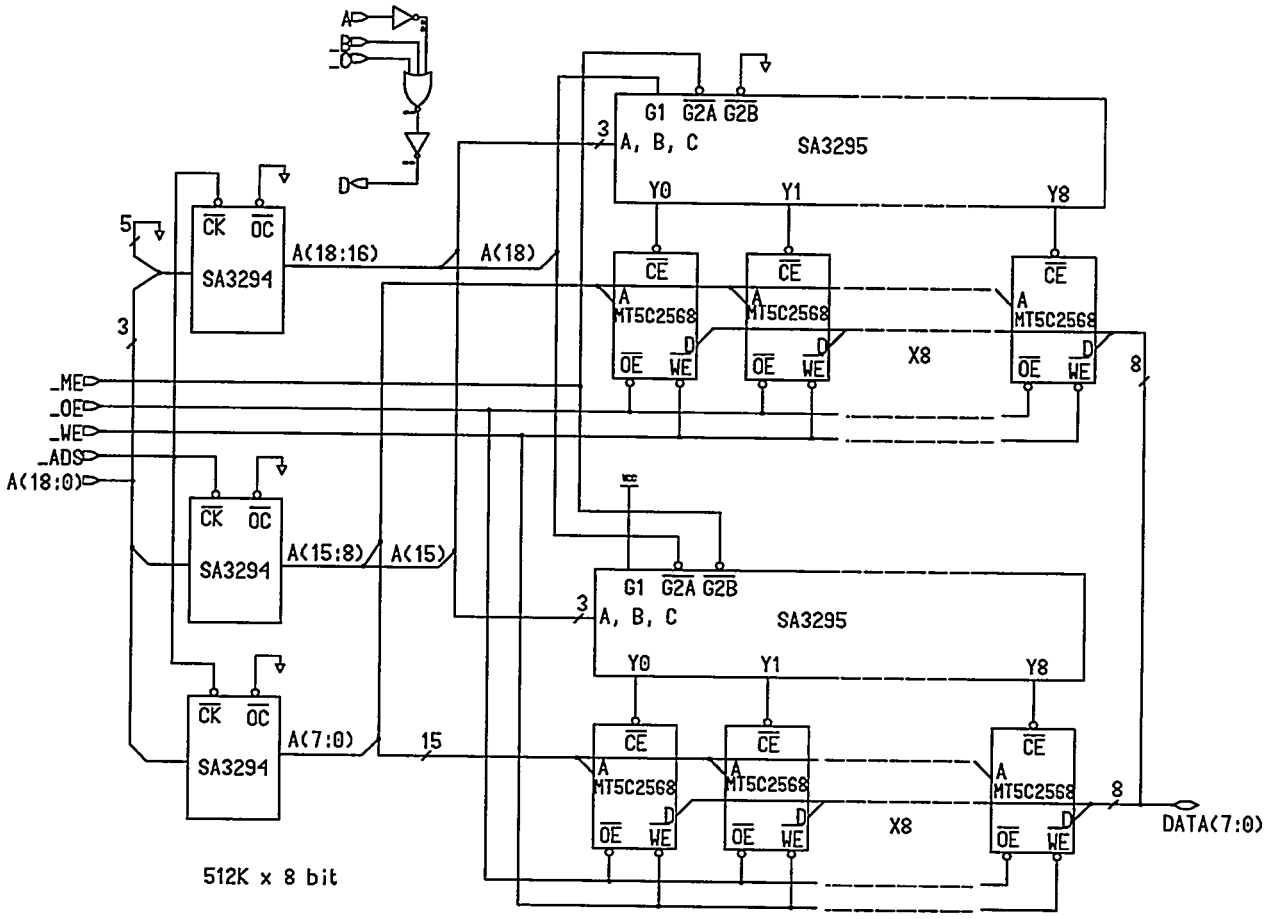

Figure 6: Block diagram of the SRAM smart substrate memory function.

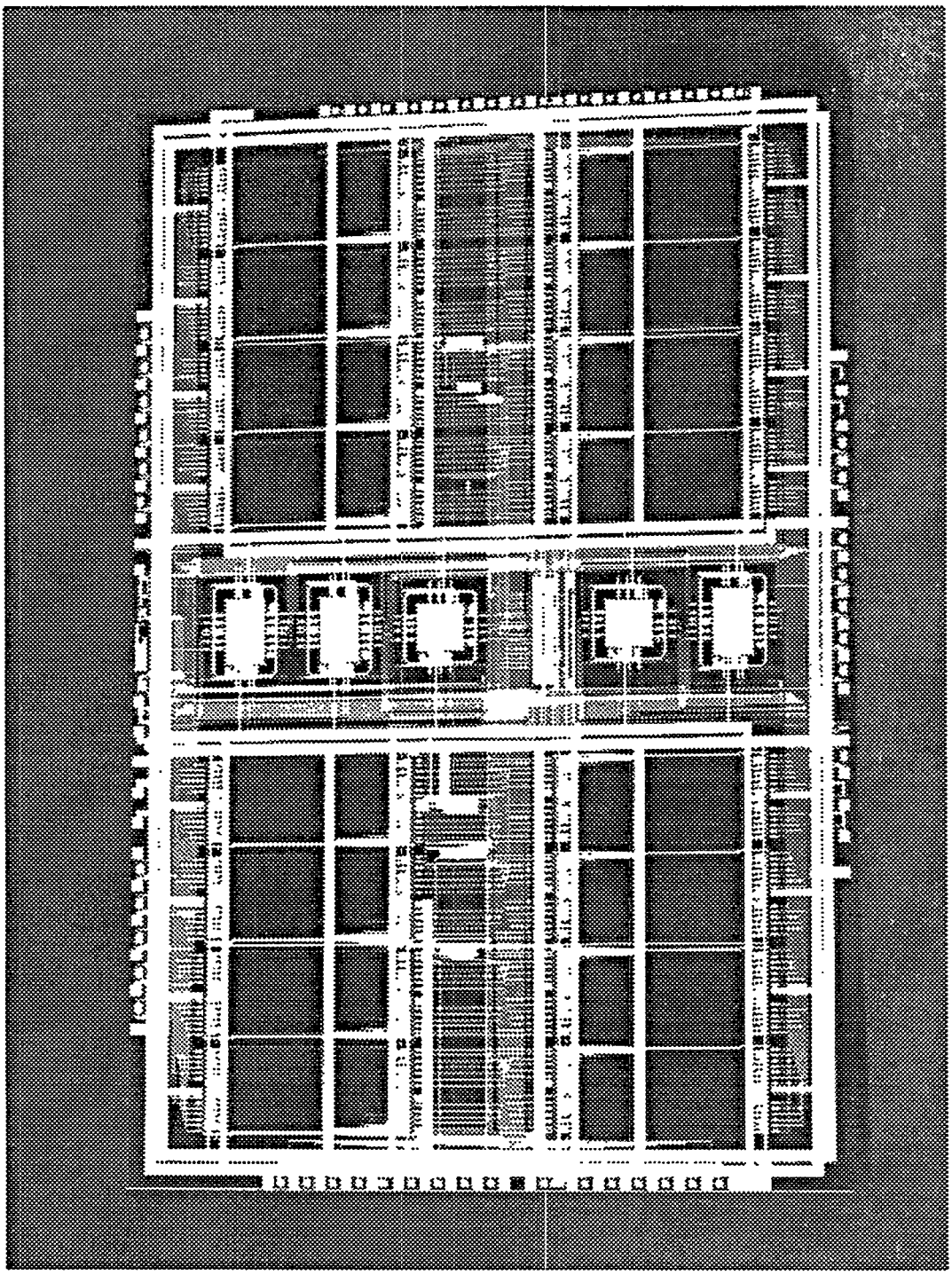

Figure 7: Photograph of the unpopulated smart substrate.

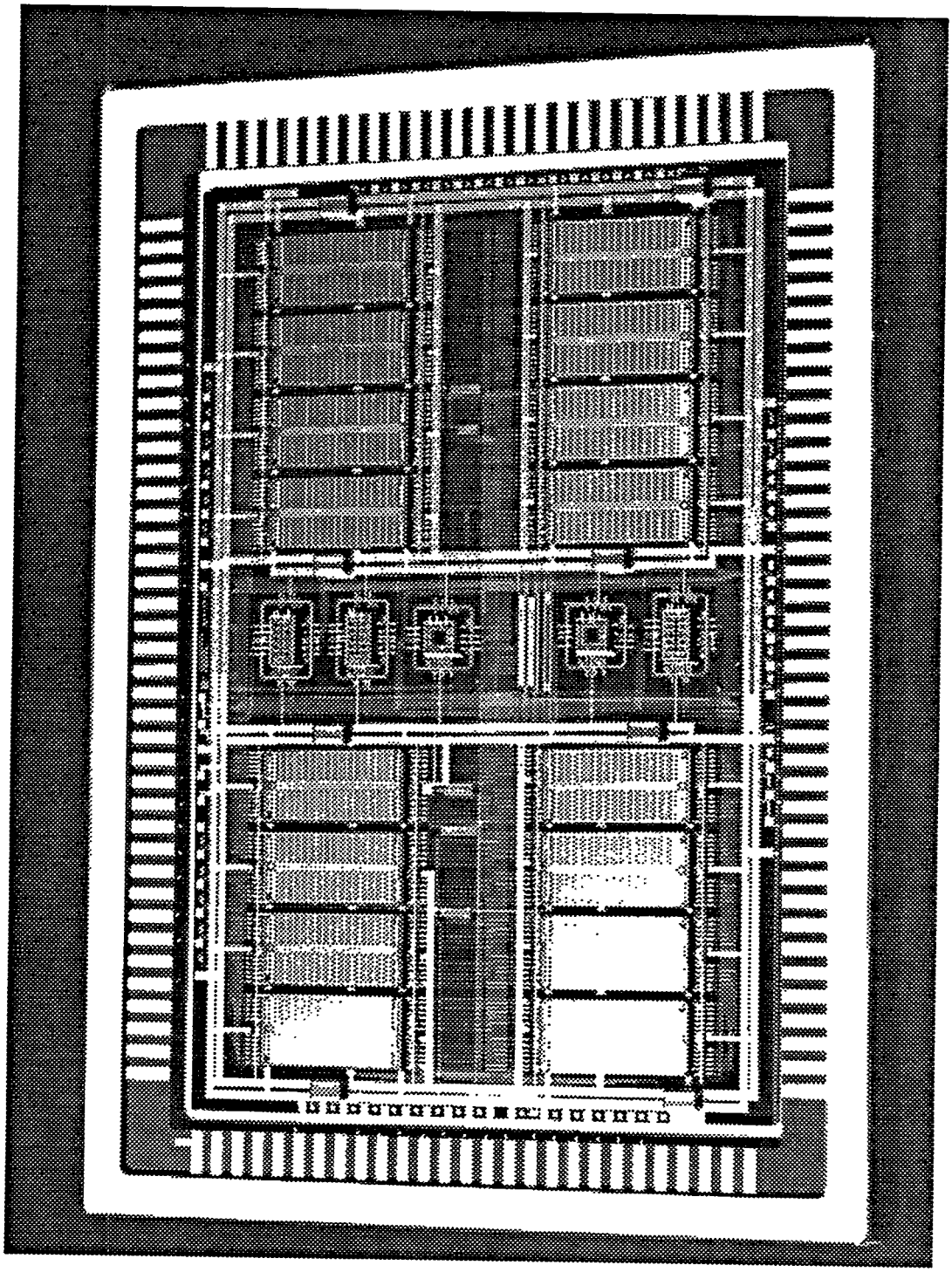

Figure 8: Photograph of the assembled and packaged smart substrate MCM.

4.2 Design for Test Features of the Smart Substrate Module

4.2.1 Boundary Scan Design

The architecture for the boundary scan test features is illustrated in Figure 9. The serial scan path exists between the test data input pin (TDI) and the test data output pin (TDO). The main serial boundary scan test register is comprised of the individual boundary test registers associated with each of the die in the module. Thus, this register is comprised of 21 uniquely addressable test registers. Test register selection is accomplished through the operation of the TAP controller and the decoded instruction scanned into the instruction register. The bypass register is a single bit bypass stage required by the IEEE 1149.1 standard.

The operational sequence of a boundary scan test is fully controlled through access to the four test pins (TDI, TDO, TMS, and TCK). This simple interface is the strength of the serial scan test approach. A minimal overhead, in terms of package pin count, is required to implement this test strategy. The simple test interface requires a minimal amount of test fixturing and is easily controlled through a relatively inexpensive personal computer (PC) based test system.

As an illustration of the data flow of the serial test sequence, consider the application of a test vector. The first operation to be performed is to load the instruction which allows the serial test vector to be scanned into the boundary scan register. This instruction is the SAMPLE/PRELOAD instruction. The TAP controller, through application of a sequence of defined bit patterns at the TMS input, is placed in a state which selects that the instruction register be placed in the serial path between TDI and TDO. The instruction bit pattern or opcode, in this case '0001' is applied at TDI. Four cycles of the test clock, TCK, will load this instruction opcode into the instruction register. The TAP controller is then placed in a state which along with the decoded instruction selects that the boundary register be placed into the serial path between TDI and TDO. The test vector is now scanned in by applying the vector to TDI and clocking TCK a number of clock cycles equal to the vector length. With the vector now loaded, a new instruction is loaded into the instruction register which will cause the vector to be applied to the MCM system. For example, if the MODULE INTEST instruction is loaded, the vector will be applied to the input pins of the MCM with output pin data being captured into the boundary scan register. The captured data, which constitutes the results of applying the test vector to the MCM, can now be scanned out through TDO for examination by the test system.

The TAP Controller. The TAP controller is a 16-state finite state machine that operates according to the state diagram shown in Figure 10. Note that in the states whose names end in "-DR" the test data registers operate, while in those whose names end in "-IR" the instruction register operates. A move along a state transition arc occurs on every rising edge of TCK. The '0's and '1's shown adjacent to the state transition arcs show the value that must be present on TMS at the time of the next rising edge of TCK for the particular transition to occur.

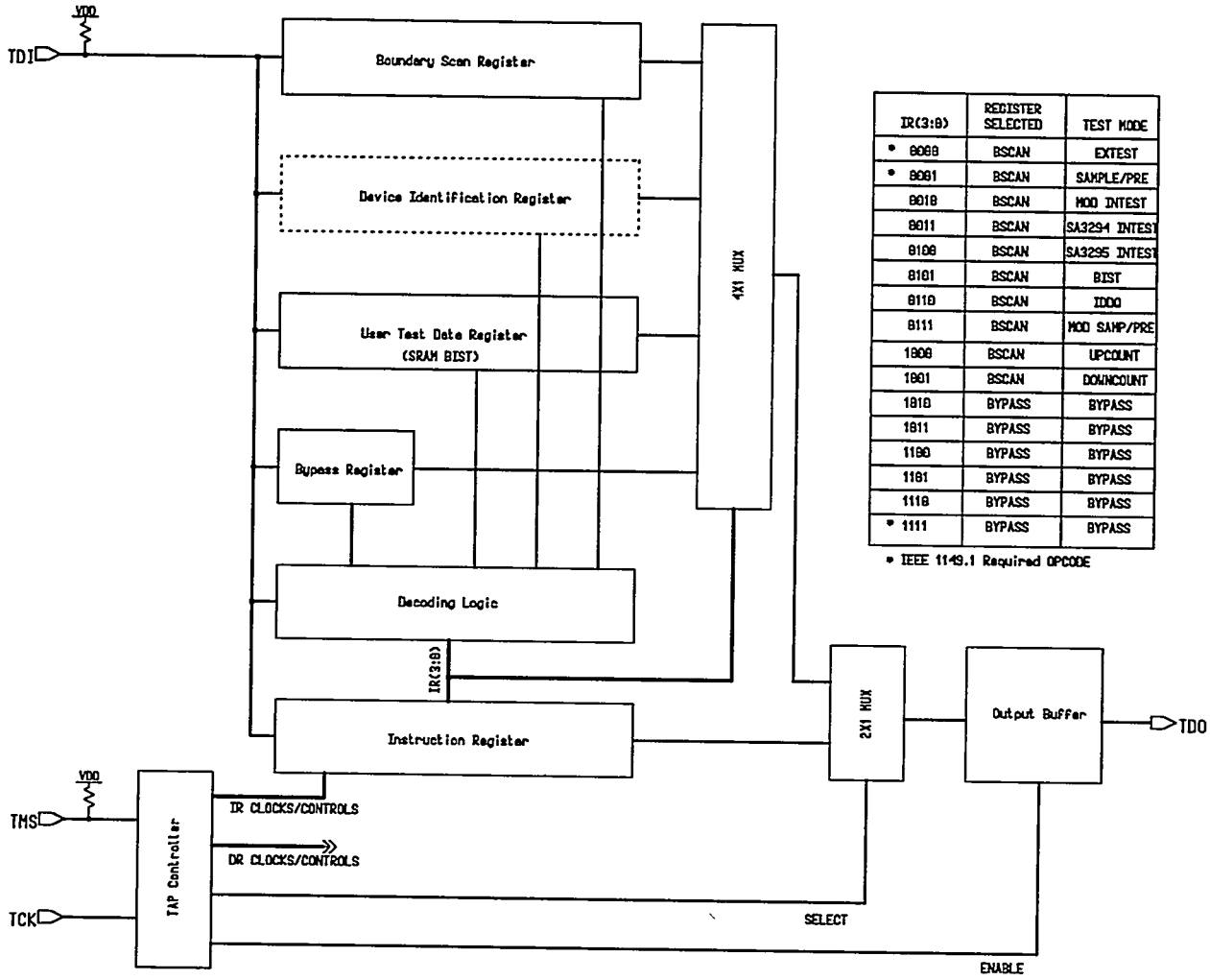

Figure 9: Boundary scan architecture for the smart substrate.

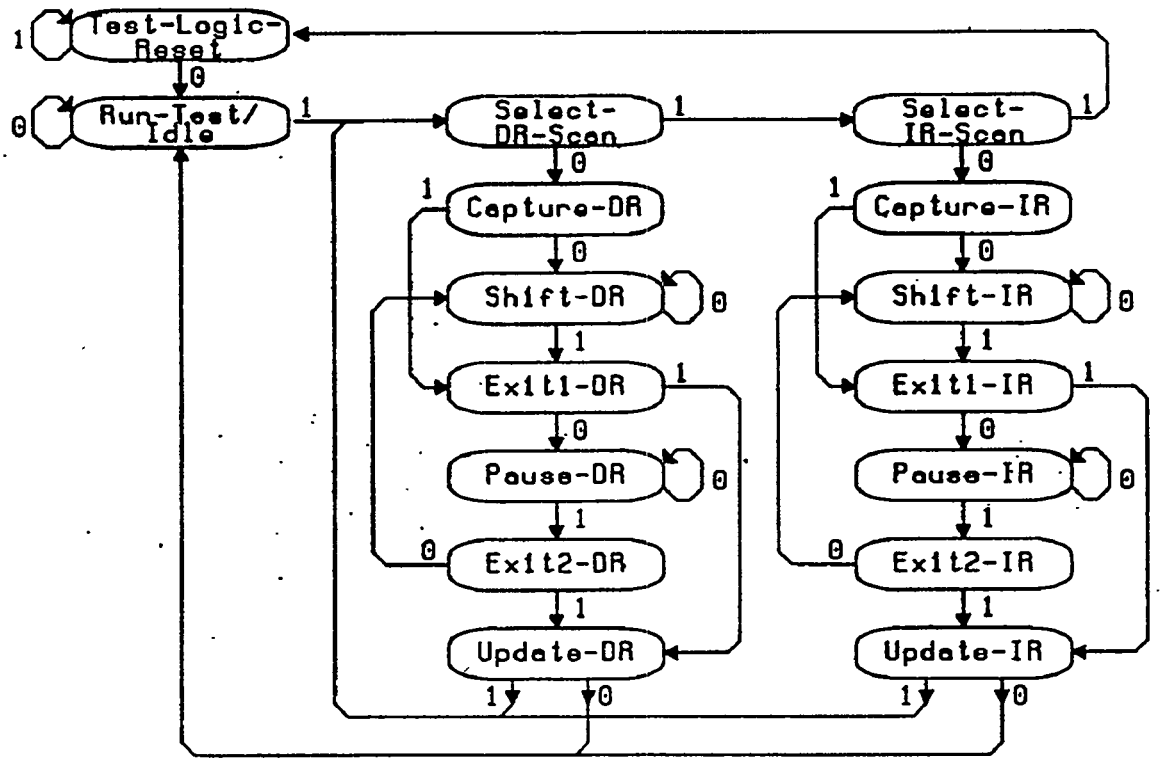

Figure 10: State diagram of the TAP controller state machine.

Eight of the 16 controller states determine operation of the test logic, allowing the following test functions to be performed:

Test-Logic-Reset: In this controller state, all test logic is reset. When the test logic is reset, it is effectively disconnected from the MCM system logic, allowing normal operation of the MCM to occur without interference. Regardless of the starting state of the TAP controller, the Test-Logic-Reset controller state is reached by holding TMS input at '1' and applying five rising edges at TCK. An additional signal line, _TRST is provided that can be used to force the controller asynchronously into this state at any point during circuit operation.

Run-Test/Idle: The operation of the test logic in this controller state depends on the instruction held in the instruction register. When the instruction is, for example, the BIST instruction, then the BIST will be run when the controller is in this state. As another example, during static current testing, the controller may be placed in this state to idle while a current measurement is being performed.

Capture-DR: Each instruction must identify one or more test data registers that are enabled to operate in test mode when the instruction is selected. In this controller state, data are loaded from the parallel inputs of these selected test data registers into their shift-register paths on the rising edge of TCK.

Shift-DR: Shifting allow new test data to be shifted into the data registers or allows previously captured data to be shifted out for examination. In the Shift-DR state, the TDO output is active.

Update-DR: This controller state marks the completion of the shifting process. New test data is transferred to the parallel outputs of the boundary scan register on the falling edge of TCK in this controller state.

Capture-IR, Shift-IR, and Update-IR: These controller states are analogous to Capture-DR, Shift-DR, and Update-DR respectively, but cause operation of the instruction register. By entering these states, a new instruction can be entered and applied to the test data registers. The new instruction becomes valid on the falling edge of TCK in the Update-IR controller state.

The Instruction Register The instruction register provides one of the alternate serial paths between TDI and TDO. It operates when the instruction scanning portion of the controller state diagram is entered.

The instruction register allows test instructions to be entered into each component along the scan path. The instruction register for the smart substrate is 25 bits long. The four lowest ordered bits decode to boundary scan operational instructions. The 21 highest ordered bits are used to set bypass registers for each of the 21 die on the MCM. In this fashion, any or all die scan test registers may be bypassed to produce a shorter data scan path. This is extremely useful when testing individual die on the MCM.

The test instructions available in the smart substrate are shown in Figure 9 and are detailed below.

EXTEST: This instruction drives the data in the boundary scan register onto the system output pins while simultaneously capturing the signals present at any input pins. This function serves two purposes–first, it may be used to verify the continuity between an output pin and any inputs to which it may be attached and secondly, it may be used to apply stimulus to logic that may exist between boundary scan cells.

SAMPLE/PRELOAD: This instruction is used to preload data into the boundary scan register and to sample the states of die pins during operation.

MODULE INTEST: This instruction applies the data in the boundary scan register onto the system input pins while simultaneously capturing the signals present on the system output pins. It may be used for low frequency functional testing.

SA3294 INTEST: This instruction applies the data in the boundary scan register onto the SA3294 input pins while simultaneously capturing the signals present on the SA3294 output pins. It may be used for low frequency functional testing.

SA3295 INTEST: This instruction applies the data in the boundary scan register onto the SA3295 input pins while simultaneously capturing the signals present on the SA3295 output pins. It may be used for low frequency functional testing.

BIST: This instruction allows execution of the BIST circuitry. This circuitry is described in more detail in a later section.

IDDQ: This instruction allows a unique current test to be performed which will verify MCM interconnect integrity. This test is also described in further detail in a later section.

MODULE SAMPLE/PRELOAD: Same as SAMPLE/PRELOAD, except loads data into the data register of the module periphery only. All internal scan registers of the MCM are bypassed.

UPCOUNT: Upcounts the data pattern being applied to the input address lines.

DOWNCOUNT: Downcounts the data pattern being applied to the input address lines.

BYPASS: Produces a single bit bypass of all test scan registers.

The Bypass Register The bypass register is, in effect, a null tool that can be selected when no other test operation is required in a given MCM. Selecting the bypass register with the BYPASS instruction allows the normal operation of the MCM to continue without interference. It speeds the flow of test data through the MCM by reducing to one clock cycle the number of clock transitions required to move data from the serial input to the serial output.

The BYPASS instruction is particularly useful when a few complex MCMs and ICs are to be tested on a board containing many other MCMs or ICs that comply with the IEEE 1149.1 standard. In that case, the BYPASS instruction can be scanned into all components other than those that will undergo test, while the target ICs receive the instructions appropriate to initiating the required tests.

4.2.2 Built-in Self Test

The built-in self test (BIST) function of the smart substrate circuitry is designed to fully test the operation of the SRAM module. The design of the BIST function centers around a finite state machine controller and a full length linear feedback shift register (LFSR). The state machine controls the operation of the LFSR including initialization. The LFSR is a 19 bit register with feedback taps applied to provide a 19 bit pseudo random pattern to the address lines of the MCM. The lowest ordered 8 bits of the LFSR are also applied to the data inputs of the memory. In this manner, each address of the memory is written in a pseudo random order with a pseudo random bit pattern applied to the data inputs. The sequence is repeated as a read operation on the memory with the 8 bit data pattern now being used as input to a comparator circuit to determine if the pattern read from memory is identical to the pattern which was initially written. Discrepancies in the comparison cause a fail bit flag to be set and loaded into the instruction register and the address and data inputs to the failed memory are latched into the boundary scan register of the failing memory. The sequence is repeated with complementary data on the memory data inputs to insure that each memory location is written with a '1' and a '0'.

Following completion of the test, inspection of the instruction register bits gives an indication of any failing memory die. The computer controlled test system analysis of the instruction register will then automatically scan out the boundary registers of any failing die to provide more complete diagnostics of the problem. Further diagnostic information may be gathered utilizing the INTEST, UPCOUNT, or DOWNCOUNT functions of the boundary scan circuitry to isolate the fault to the decoder, latch, or memory die.

4.2.3 Static Current Interconnect Test

A unique boundary scan cell design allows for testing of the module interconnect before MCM assembly. This feature is important to the overall test strategy because it allows for a known good substrate to be used in the assembly process.

Traditional interconnect testing using boundary scan circuitry involves applying bit patterns using the EXTEST command to nets that are to undergo examination. For example, one may apply a '1' to a net through an IC output boundary scan cell and a '0' to all other nets. Under correct operation, the '1' is propagated to the various inputs that the net fans out to. This '1' is then captured and scanned out for examination. A faulty net may be stuck-at '0' if it is shorted to another net and examination of the scanned out pattern will reveal this discrepancy. On the other hand, if the net is open, the '1' will not be propagated and testing of the net with both '1' and '0' patterns will likely reveal this problem. The problem with this approach to the interconnect testing problem is that interconnect shorts and opens are most likely to be resistive in nature. If the resistivity of the short is large or the resistivity of the open is small, the faulty nets may not be stuck-at the opposite state and the defect may not be revealed.

What is needed is a test which will be sensitive to the resistive faults. Consider the example shown in Figure 12. If the resistor shown represents a resistive open along the

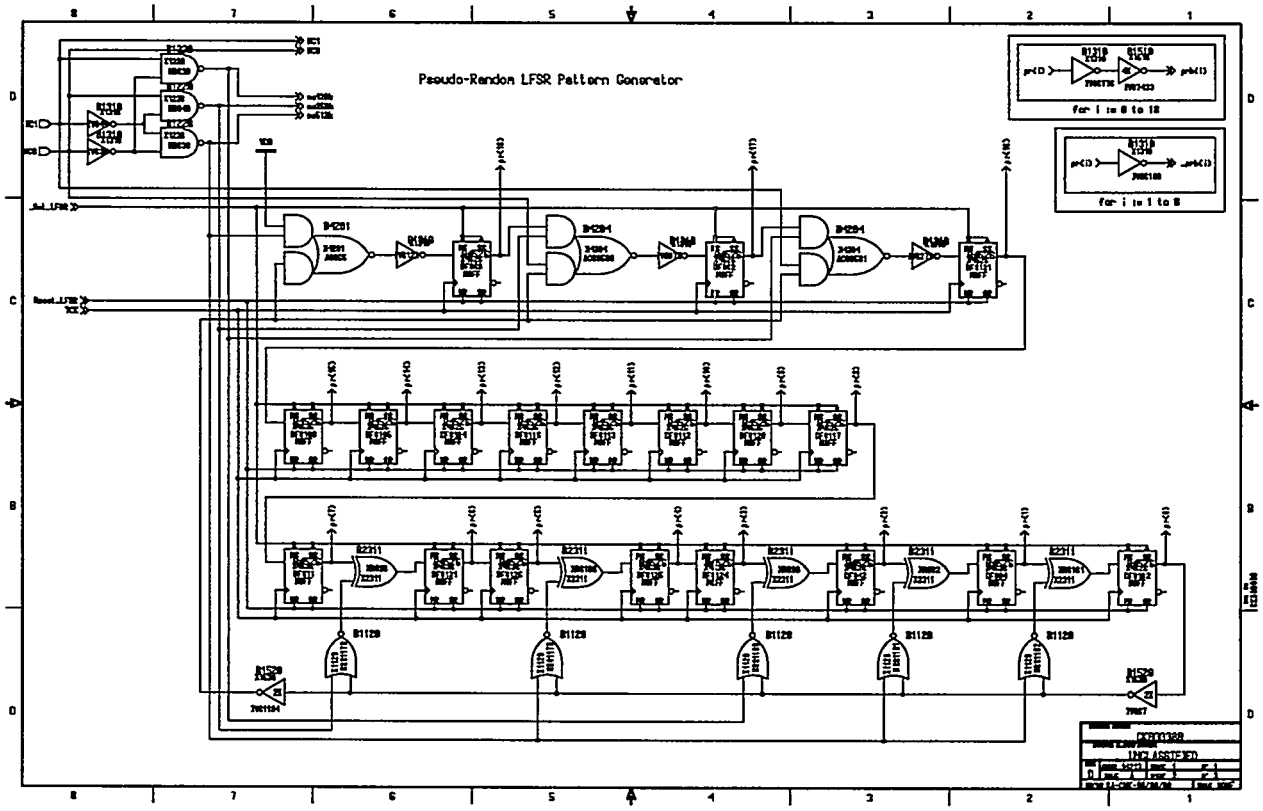

Figure 11: Schematic of BIST LFSR.

path between nets A and B, we may test this net by applying a '1' to net A, a '0' to net B and tristate the outputs of all other boundary scan cells attached to other nets. For a connection between net A and net B, we would expect a current flow proportional to the potential difference between a logic '1' and a logic '0' say 5 volts. If the resistivity of the net is small, this current flow will exceed by several orders of magnitude the normal static current consumption of the fully static CMOS test circuitry. This current will be limited by the resistivity of the output drive switches in the boundary scan cell. If we limit this current to a reasonable value, say 5 mA, through proper sizing of the output pass transistors, a reduction below a preset current value, say 1 mA, would indicate a resistive open along this net.

Now consider the opposite case, that the resistor in Figure 12 represents a short between net A-C and net B. Applying a '0' to net A and a '1' to net B will result in a high static current flow if the short exists. Again, this current flow will be orders of magnitude above the static current draw of the substrate and is easily detected by monitoring the quiescent current draw of the substrate power supply.

4.3 Smart Substrate Test Strategy

The testing of the smart substrate encompasses a four part strategy. First, the substrate is tested following fabrication but prior to assembly. Second, the module may be tested during assembly. Third, the assembled and packaged module is tested. Finally, the module contains certain system level test features which may be utilized upon insertion in the next higher level of assembly or even in field diagnostic evaluation.

4.3.1 Unpopulated Substrate Testing

The main objectives of testing the unpopulated substrate are to verify the functionality of the substrate test circuitry and to verify the integrity of the module interconnect.

The functionality of the substrate test circuitry may be verified to a large extent by executing various shifting operations through the scan circuitry. Various patterns including all '0's, all '1's, and alternating sequences of '0's and '1's provide a reasonably thorough test of the scan path, the instruction register, and the TAP controller.

The interconnect is tested utilizing the static current testing techniques described in Section 4.2.3. Each module trace is tested alone for open circuits, and against every other trace, VDD, and GND for short circuits. The test vector patterns were generated fairly simply by a PC based program and the resulting bit patterns applied to the substrate utilizing the Texas Instruments ASSET diagnostic system. The static current flow was monitored through an inline .1Ω resistor and a Hewlett Packard GPIB controlled digital multi-meter.

A special fixture was designed to allow bare testing of the unpopulated substrate. This fixture is shown in Figure 13. The fixture contains two sockets – one, a PGA socket, is for testing the packaged module, the other, a z-axis elastomer compression socket, may be

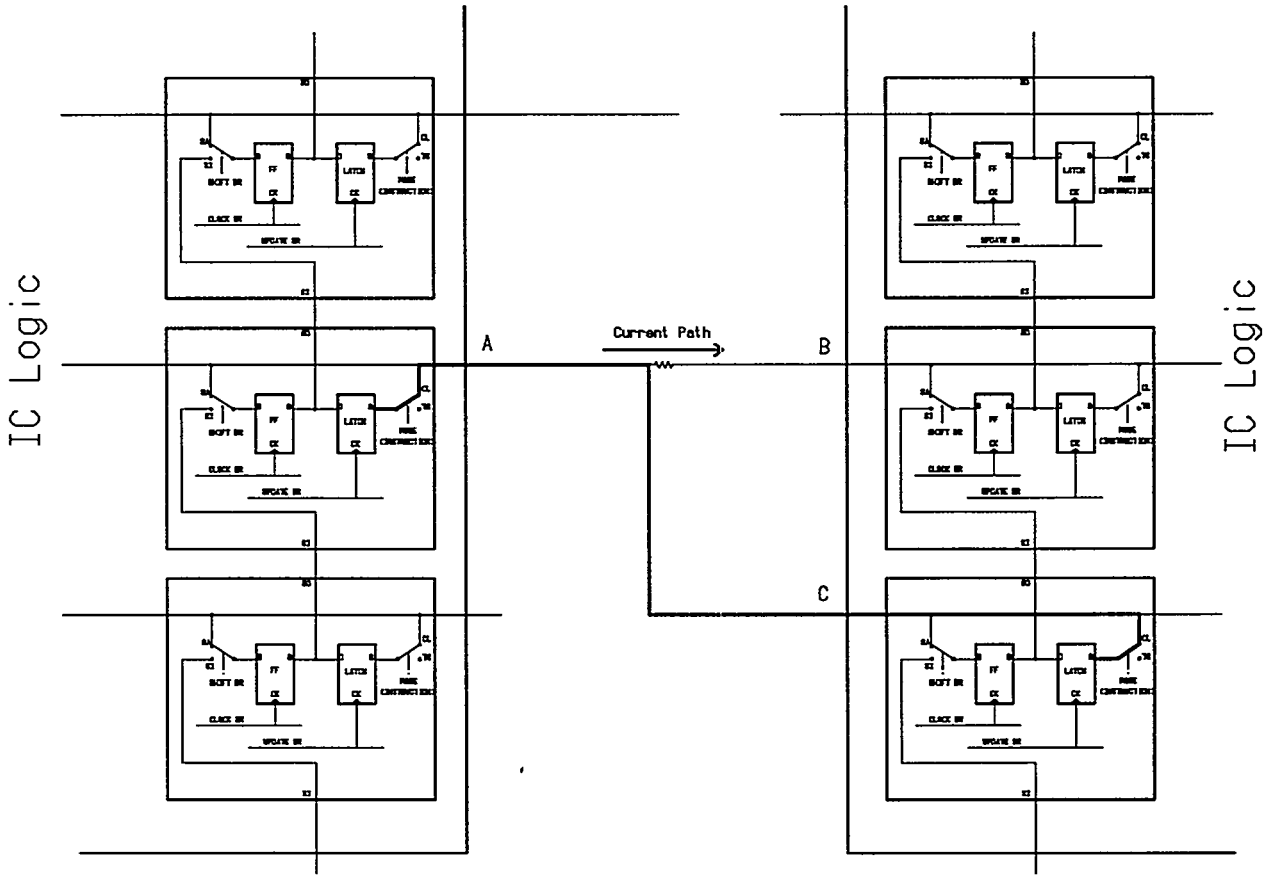

Figure 12: Illustration of static current testing technique.

used for testing the bare substrate. The compression socket contains a machined template which aligns the substrate to a set of solder bumped pads on the fixture board. Between the bumped pads and the substrate, a z-axis elastomer is placed. The elastomer acts as an insulator unless compressed. Compression occurs along the solder bump pads when the substrate is clamped into the fixture providing continuity between the substrate pads and the test fixture pads.

The photograph shows sockets for connection to the TI ASSET system, connection to an external TCK source, jumpers and test points for I_{ddq} testing and for I_{ddq} bypass.

4.3.2 Test During Module Assembly

A substantial amount of testing may occur during assembly if desired. Utilizing the INTEST operations of the boundary scan circuitry, each individual die may be tested for functionality and wire-bond continuity. EXTEST operations may also be used to verify wire-bond continuity.

The partially assembled testing capabilities prove to be extremely valuable for modules with large numbers of components.

4.3.3 Assembled Module Substrate Testing

The assembled module testing relies heavily on the BIST features in the MCM substrate. The BIST and boundary scan features in the substrate make this thorough test very simple to execute. All that is required is that the BIST instruction be loaded in the instruction register of the boundary scan logic, the TAP controller be placed in the Run/Test-Idle state through application of the appropriate bit sequence to TMS, and application of the correct number of clock cycles to TCK for the test to complete execution.

The test fully exercises the latch and decode die and each memory location of each memory die. The BIST logic writes bit patterns to each memory location and then reads these same memory locations to compare with the written pattern. If the pattern written to the memory and that read from the memory do not compare bitwise, a flag is set in a portion of the instruction register which identifies the memory die being tested. Upon completion of the test, the instruction register will contain a bit pattern identifying all faulty memory die locations. This pattern can be scanned out by the test system for examination. If a faulty die location is indicated, further diagnostic information may be obtained by scanning out the boundary scan register. During BIST operation, the boundary scan register is set up to latch the state of the memory any time a bitwise data comparison fails. Thus, this register will contain the address and data information being read at the time a failure occurs. This data may be used along with the INTEST, UPCOUNT, and DOWNCOUNT to further test the decode logic at this address. This diagnosis will further eliminate the possibility of a faulty decoder die aliasing a memory die failure. The BIST test frequency may be increased to operational frequency until a failure occurs. In this manner, the operational frequency of the module may be determined.

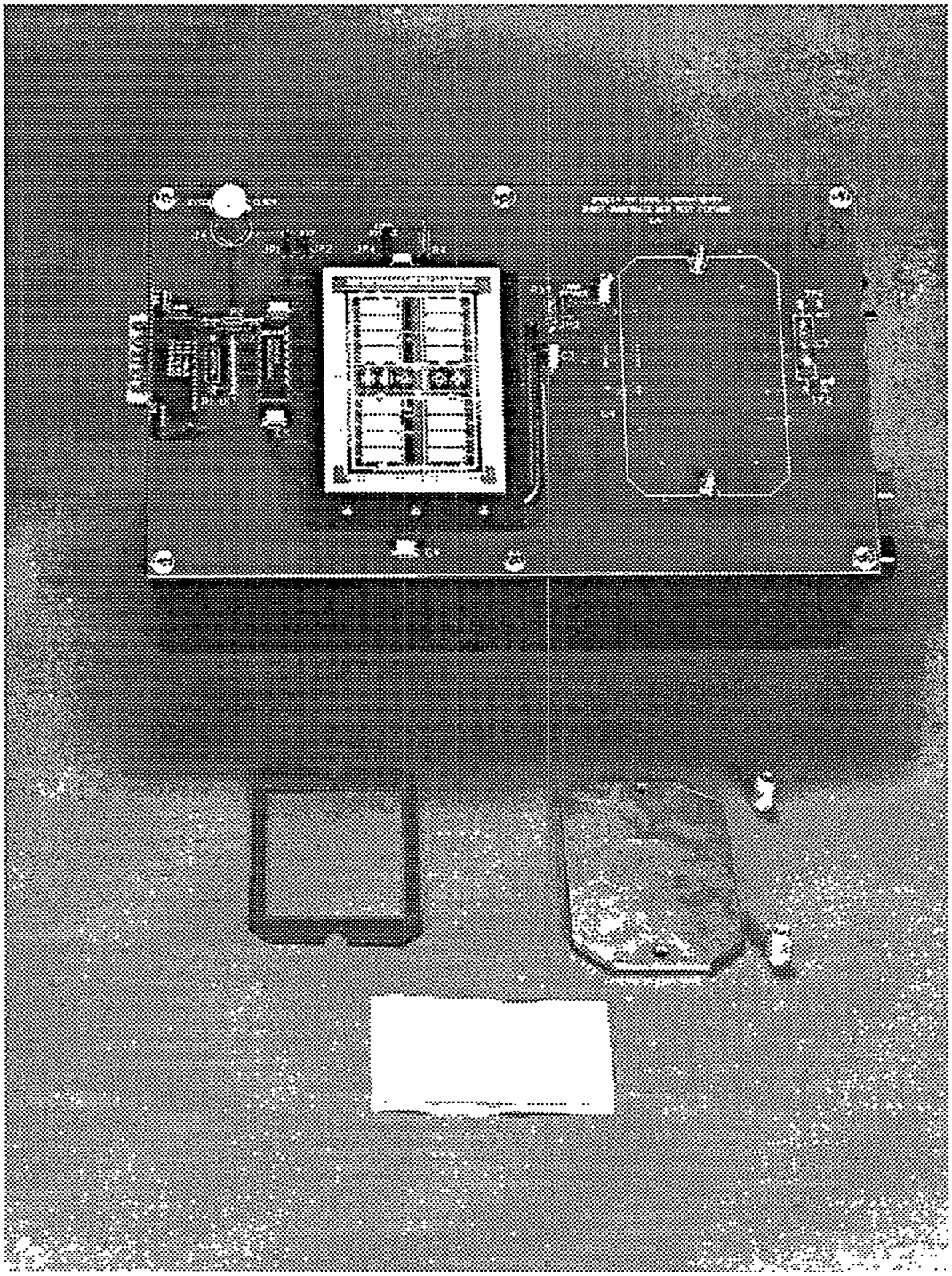

Figure 13: Photograph of the smart substrate test fixture. The bare substrate portion of the fixture is disassembled to show the substrate template, compression plate, compression nuts, elastomeric sheet, and the smart substrate.

4.3.4 System Level Test Features

As with boards, assembled MCM systems can accept a structured based test based on boundary scan. Here, the pre-existing test data for the various MCMs is brought together and supplemented with tests for new system level features, such as module to module connections.

This reuse of test data is extremely cost efficient to the system developer. Test development for loaded boards involves assembly of this pre-existing data and test pattern generation targeted at the new circuitry introduced when the board is assembled–the module to module interconnections and the circuitry which does not conform to the IEEE 1149.1 standard.

Test equipment for testing individual MCMs can be expected to undergo significant changes. In the long term, widespread use of boundary scan and BIST allow powerful and expensive automatic test equipment to be replaced by much simpler, lower cost test systems. A principle advantage of built in system testing is that most connections between system components can be exercised at low speeds–say, a few megahertz–reducing the amount of expensive, high performance test circuitry require in automatic test equipment.

The advent of boundary scan coupled with the smart substrate approach provides powerful testing capabilities. Field technicians can be equiped with testers of similar fault finding capability as those used in the manufacturing environment. The value of such highly portable tools in field service could be enormous.

4.4 Results of Prototype Smart Substrate MCM Testing

The results of the prototype testing are presented in Table 1. A total of 13 wafers with 4 substrates per wafer were fabricated. Of the 13 wafers, 3 did not undergo testing – one wafer was not delivered from fab due to damage, one wafer was immediately sawed and substrates assembled for visual display purposes only, and one wafer was left intact without undergoing testing.

Of the wafers tested, 29 substrates passed the initial instruction register verification, scan path verification and interconnect testing. A total of 11 substrates failed one or all of these tests and did not undergo further testing.

A total of 21 of the good substrates were selected for full assembley. Each of these 21 modules successfully passed the BIST testing. Eight substrates were left unassembled for further development of the bare substrate fixturing and test software.

Substrate yield was approximately 72% for the substrates selected for testing. These results are consistent with expectations for the process line taking into consideration this was a first attempt at developing a smart substrate technology. The results of testing are promising and additional development is warranted to achieve higher yields through process development, failure analysis, and closer examination of the robustness of the design.

S/N	IR Verify	Scan Path ATP	Inteconnect Test	BIST	Comments
W1-1	Pass	Pass	Pass	Pass	
W1-2	Pass	Pass	Pass	Pass	
W1-3	Pass	Pass	Pass	Pass	
W1-4	Pass	Pass	Pass	Pass	
W2-1	Pass	Pass	Pass	Pass	
W2-2	Pass	Pass	Pass	Pass	
W2-3	Pass	Pass	Pass	Pass	
W2-4	Fail	Fail	N/A	N/A	Not Assembled, high current
W3-1	N/A	N/A	N/A	N/A	Incorrect pin out
W3-2	N/A	N/A	N/A	N/A	Incorrect pin out
W3-3	N/A	N/A	N/A	N/A	Assembled w/o testing (demo)
W3-4	N/A	N/A	N/A	N/A	Assembled w/o testing (demo)
W4-1	Pass	Pass	N/A	N/A	Not Assembled
W4-2	Pass	Pass	N/A	N/A	Not Assembled
W4-3	Pass	Pass	N/A	N/A	Not Assembled
W4-4	Pass	Pass	N/A	N/A	Not Assembled
W5-1	Pass	Pass	Pass	Pass	
W5-2	Fail	Pass	N/A	N/A	Not Assembled
W5-3	Pass	Pass	Pass	Pass	
W5-4	Fail	Fail	N/A	N/A	Not Assembled, high current
W6-1	N/A	N/A	N/A	N/A	Wafer damaged in fab
W6-2	N/A	N/A	N/A	N/A	Wafer damaged in fab
W6-3	N/A	N/A	N/A	N/A	Wafer damaged in fab
W6-4	N/A	N/A	N/A	N/A	Wafer damaged in fab
W7-1	Pass	Pass	N/A	N/A	Not Assembled
W7-2	Pass	Pass	N/A	N/A	Not Assembled
W7-3	Pass	Pass	N/A	N/A	Not Assembled
W7-4	Fail	Fail	N/A	N/A	Not Assembled, high current
W8-1	Pass	Pass	N/A	N/A	Not Assembled
W8-2	Fail	Fail	N/A	N/A	Not Assembled, high current
W8-3	Fail	Fail	N/A	N/A	Not Assembled, high current
W8-4	Fail	Pass	N/A	N/A	Not Assembled
W9-1	Pass	Pass	Pass	Pass	
W9-2	Pass	Pass	Pass	Pass	
W9-3	Pass	Pass	Pass	Pass	
W9-4	Pass	Pass	Pass	Pass	
W10-1	Pass	Pass	Pass	Pass	
W10-2	Fail	Pass	N/A	N/A	Not Assembled
W10-3	Fail	Pass	N/A	N/A	Not Assembled
W10-4	Pass	Pass	Pass	Pass	

S/N	IR Verify	Scan Path ATP	Inteconnect Test	BIST	Comments
W11-1	Pass	Pass	Pass	Pass	
W11-2	Pass	Pass	Pass	Pass	
W11-3	Pass	Pass	Pass	Pass	
W11-4	Pass	Pass	Pass	Pass	
W12-1	Pass	Pass	Pass	Pass	
W12-2	Pass	Pass	Pass	Pass	
W12-3	Pass	Fail	N/A	N/A	Not Assembled
W12-4	Fail	Pass	N/A	N/A	Not Assembled
W13-1	N/A	N/A	N/A	N/A	Wafer not sawed
W13-2	N/A	N/A	N/A	N/A	Wafer not sawed
W13-3	N/A	N/A	N/A	N/A	Wafer not sawed
W13-4	N/A	N/A	N/A	N/A	Wafer not sawed

5 The MCM Market: Possibilities for Smart Substrate Systems

There are two distinct environments for which MCMs are manufactured– the merchant markets and the captive markets. Merchant MCM manufacturers sell products to equipment manufacturers in a variety of application areas. The supplier may specialize in one type of MCM–for example, MCMs for the telecommunication segment. Captive vendors are those who manufacture exclusively for a single customer and are, more often than not, subsidiaries of some major corporation. Currently, captive suppliers dominate the MCM market, supplying mainly to the mainframe and super-computer industries.

In 1990, the MCM-C sector saw a nearly equal market share for both captive and merchant markets, while the MCM-D sector was mildly captive and the MCM-L sector was strongly captive. The MCM market was 79% captive and 21% merchant, whereas in the year 2000, the captive portion is projected to shrink to 53%.

The MCM market has been projected to grow at a compound annual growth rate of 60%. MCM-Ls held the largest market share in 1992 with 68%. However, this share is projected to be eroded by the MCM-D sector, which is projected to have a 40% share of a $20 billion market in the year 2000.

The development of the MCM-D market would indicate that there is clearly a role for active substrate MCMs. The current cost structure for high volume consumer electronics favors MCM-L and it is expected that this will continue throughout the next decade. MCM-Ds will provide an important strategy for increased electronic integration and system performance in high-reliability and low volume high performance applications. The testability advantages of the smart substrate solution would provide a unique capability not available in other MCM technologies. For example, consider an electronic system in a satellite. The system could incorporate BIST monitoring of the system health with defect sensing and fault tolerant operations built into the system substrate. Such a system could correct for single-event-upset (SEU) errors as part of the normal system operation and would allow for memory address blocks to be partitioned out of the system as they become unreliable. The value added through the smart substrate circuitry could prove to be an enormous benefit while representing a fraction of the total system cost. Similar benefits exist when analyzing weapons systems, nuclear reactor instrumentation, medical systems and other high reliability applications.

6 Conclusion

This paper has outlined the successful development and testing of a fully functional smart substrate MCM. Results have confirmed the acceptability of this technology as an alternative approach to many difficult test issues affecting the acceptance of MCMs as a mainstream alternative to PWB assemblies. The test data, though taken on the first prototype of its kind, shows yield to be within an acceptable range for this type of system. Improvement of the manufacturing yield and reduction in smart substrate system design time and cost appears to be achievable with continued experience and modest development efforts. Continuing development should focus on further yield improvements, diagnostic performance evaluation and reduction in design cycle time.

Improvement in the design cycle time is possible with the addition of automated BIST and boundary scan design tools being developed both by industry and university research programs. Such systems will have the effect of lowering the time from concept to hardware and as a result, reduction in cost of smart substrate systems.

The continued development of diagnostic software, both by Sandia and industry, will provide data to confirm the diagnostic capabilities of smart substrate systems that have been verified by simulation and to a more limited extent by testing of the prototype system. As more complex MCM systems are developed, the diagnostic capabilities of substrate test circuitry have the potential to reduce the MCM repair cycle time and cost. Reductions in rework cycles have also been shown to improve MCM reliability by reducing the handling and repair of the MCM circuitry.

Manufacturing yield, while acceptable, will be key to industry acceptance of smart substrate systems. Additional development of scan and BIST cell libraries will make substrate circuitry less susceptible to defects. Knowledge gained in this study will also prove to be invaluable to further process development in future designs.

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Appendix A: Sandia National Laboratories Smart Substrate Program

1991 Active test substrate conceptualized.

"Smart Substrate" coined to describe active test substrate.

1992 Project defined and submitted as a Laboratory Directed Research& Development (LDRD) program.

LDRD funding approved.

SRAM MCM definition and design completed.

First smart substrate lot start.

1993 First functional smart substrate (3/94).

Functional assembled smart substrate MCM (4/94).

Diagnostic software development (TI ASSET system)

Appendix B

Publications and Presentations:

T. F. Wunsch, R. K. Treece, "Smart Substrates: Making Multi-Chip Modules Smarter," ISHM Advanced Technology Workshop on Multi-Chip Module Test, (1994)

Invention Disclosures: N/A

Patents: N/A

Copyrights: N/A

Employee recruitment and student involvment:

Mike Wick, UNM student from 10/93 - 7/94
Arturo Gonzalez, UTEP student from 6/94 - 8/94

Follow on work:

Development of follow on work is in progress.

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