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AN EVALUATION OF PROTOTYPE SURFACE MOUNT CIRCUIT BOARDS ASSEMBLED WITH THREE NON-LEAD BEARING SOLDERS

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ABSTRACT

Prototype circuit board test vehicles were assembled with three candidate lead-free solders: 96.5Sn-3.5Ag (wt%), 58Bi-42Sn, and 91.84Sn-3.33Ag-4.83Bi., using a forced-convection/infrared furnace and RMA flux based pastes. Wettability of circuit board features and packages was best with Sn-Ag-Bi alloy followed in order by Bi-Sn and Sn-Ag solders. The Sn-Ag-Bi solder had a greater propensity for void formation in the joints. The reliability assessment was based upon solder joint microstructure and the shear strength of selected leadless packages. Solder joint damage was of a greater extent after thermal shock exposures rather than thermal cycling. The Sn-Ag-Bi alloy on the largest package appeared most susceptible to thermal shock. Test vehicle performance clearly demonstrated that, with the non-lead solders, local thermal expansion mismatch can be as detrimental to joint integrity as the traditional global mismatch damage.

INTRODUCTION

The technology drivers for the electronics industry continue to be: (1) device and system miniaturization, (2) increased functionality with greater reliability, and (3) low cost manufacturing processes. Clearly, current assembly technology based upon the lead-bearing solders has met these objectives. In fact, it is foreseen that tin-lead solders will continue to satisfy these goals in *a majority* of the next generation of devices, sub-systems, as well as final assemblies. However, it is becoming increasingly obvious that as product and assembly technologies forge ahead, the properties of the traditional lead-bearing solders may not be able to fully support the miniaturization, reliability, and cost objectives of new advanced packaging concepts. In addition, a further requirement that, both manufacturing processes as well as final products be compatible with the environment, may limit the availability and/or cost-effective use of lead-bearing solders. Therefore, alternative solders will have to be developed that meet both the technological demands of the electronics industry as well as the environmental objectives of the community at-large.

In light of the forecasts outlined above, numerous efforts have been underway to develop new solder alloys that will replace the lead-bearing materials[1,2,3]. A large extent of this work has targeted alternatives to the eutectic 63Sn-37Pb (wt%) and near-eutectic 60Sn-40Pb solders; however, alloy development to replace the lead-based, high melting temperature solders such as used in C4 technology, will surely follow[4]. Laboratory test methodologies have been developed which measure solder alloy properties as well as describe the interactions between solder and substrate materials. These procedures include melting temperature determination (Differential Scanning Calorimetry, or DSC), wettability measurements (meniscometer/wetting balance, parallel plate capillary flow, and sessile drop techniques), and mechanical strength tests (ring-in-plug and fracture toughness)[5,6,7]. Such studies are invaluable for documenting alloy "credentials" and subsequently, to select the most promising candidates.

However, laboratory evaluations provide only a preliminary assessment of the performance of the candidate replacement solders. An understanding of the solder joint manufacturability and reliability rests upon the alloys' performance in the assembly and testing of circuit board test vehicles. While the ultimate trial of any new solder is its time-tested performance in the service life of actual products, test vehicle prototypes provide a cost effective means of predicting product manufacturability and service mortality through the use of assembly feasibility trials and accelerated reliability tests.

Manufacturing feasibility and reliability assessments are based upon quantitative analyses of the prototype units[8,9,10]. In the case of manufacturing produceability, test vehicle defects must be identified, given a quantitative figure-of-merit, and then counted for each of the units. Besides determining the relative number of defects between several solders or processes for a given solder, the significance of the *absolute* defect rate, projected towards the produceability of a specific product, must also be determined. Typically, evaluations with prototypes assembled with 63Sn-37Pb solder provide the baseline data.

Reliability test data are determined from one or more environmental stressing procedures[11,12,13]. Because the overwhelming number of surface mount failures are caused by thermal fatigue of the joints, thermal cycling provides a

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means of accelerated testing to predict long-term solder joint integrity. Quantitative measurements of solder joint fatigue damage include (1) electrical continuity, (2) microstructural characteristics, and (3) mechanical strength. Prior to the acquisition of numerical statistics, failure criteria must be established for each of these test domains. Lastly, recommendations for a particular alloy must be made, based upon either the absolute magnitude of the quantitative results (e.g., a strength value or crack length), or be determined through relative comparison with baseline results such as those provided by the 63Sn-37Pb solder.

A collaborative program between AT&T/Engineering Research Center, Princeton, NJ and Sandia National Laboratories, Albuquerque, NM has produced an extensive data resource on the manufacturability and reliability of several lead-free solders on circuit board test vehicles[14,15,16]. Those results included tests with such alloys as 96.5Sn-3.5Ag, 58Bi-42Sn, 52In-48Sn, 95Sn-5Sb on 50 mil pitch printed circuit boards as well as assembly trials with several lead-free solders in no-clean paste formulations using test vehicles with fine pitch package technology[8]. In the work by Vianco, et al..[11], the wetting properties of the 96.5Sn-3.5Ag and 58Bi-42Sn solders were shown to be slightly poorer than that of the 63Sn-37Pb solder control group; however, the results were deemed quite acceptable, given the limited degree of both process definition as well as flux development. The limited reliability of the two solders resulted in no unexpected results; the Sn-Ag joints maintained excellent integrity through 5000 thermal cycles (0°C to 100°C, 30 min cycle times) as determined by electrical monitoring, microstructural analysis. The Bi-Sn solder exhibited slightly greater microstructural damage as exemplified by optical microscopy and confirmed by mechanical strength measurements; however, no loss of electrical integrity was detected.

The present study examined the implementation of the Sn-Ag and Bi-Sn solders into an alternative, all surface mount circuit board assembly. Aside from a larger variation of devices to be soldered and different laminate as compared with the experiments noted above[11], this test vehicle provided necessary manufacturing and reliability data prior to the follow-up build of fully functional units. Manufacturability defect analysis was performed on the as-fabricated test vehicles. Selected units were exposed to thermal cycling or thermal shock environments as part of the reliability assessment. Solder joints from the as-fabricated as well as thermally stressed units were evaluated for microstructural damage and strength.

In addition to the Sn-Ag and Bi-Sn alloys, a third solder was evaluated. This alloy was developed at Sandia National Laboratories and had the composition: 91.84Sn-3.33Ag-4.83Bi (and abbreviated as Sn-Ag-Bi)[1]. Differential thermal analysis (DSC) determined the onset temperature to be 212°C at a scanning rate of 10°C/min. Separate solidus and liquidus transitions could not be identified in the data traces. The solder microstructure (Fig. 1) was comprised of a Sn matrix containing Ag_3Sn intermetallic particulates which represent the other terminal phase of the Sn-Ag binary alloy. Bismuth (the very bright phase in Fig. 1) remained in the microstructure as a free element, both in solid solution within the Sn matrix (as predicted by the binary Bi-Sn phase diagram) as well as larger precipitates which decorated the Ag_3Sn particles.

Figure 1: Microstructure of the Sn-Ag-Bi solder (SEM).

The Sn-Ag-Bi solder exhibited excellent wettability on copper and exceptional strength. Laboratory meniscometer/wetting balance tests measured a contact angle of 33±4° as compared with 17±4° for the 60Sn-40Pb alloy and 36±3°for the Sn-Ag solder at 260°C. All solders were evaluated with an RMA flux. The solder exhibited excellent capillary flow as determined by the parallel plate, capillary flow wettability test. These data are shown in Fig. 2 for tests performed at several temperatures. The results

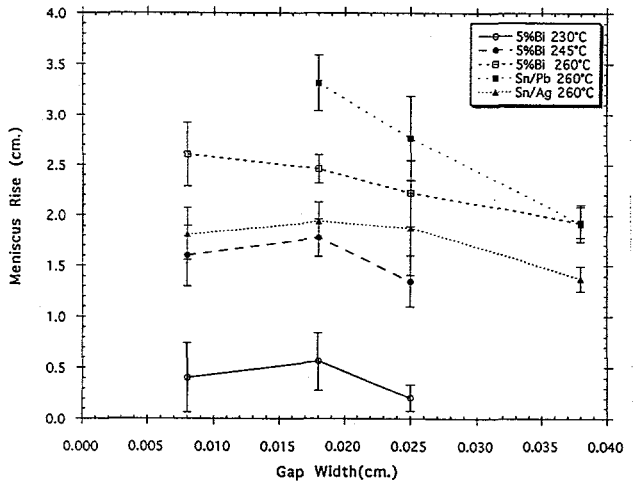
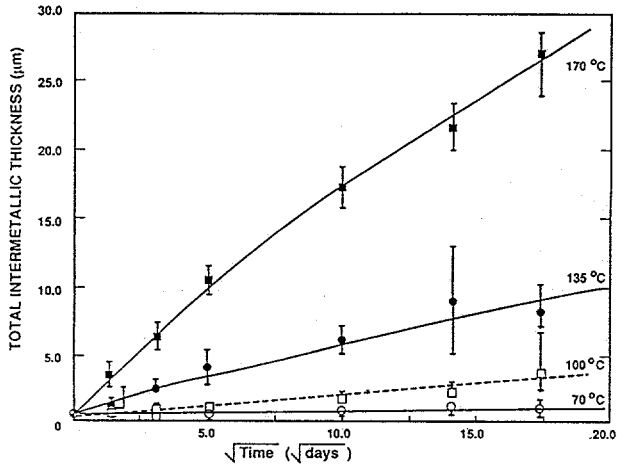
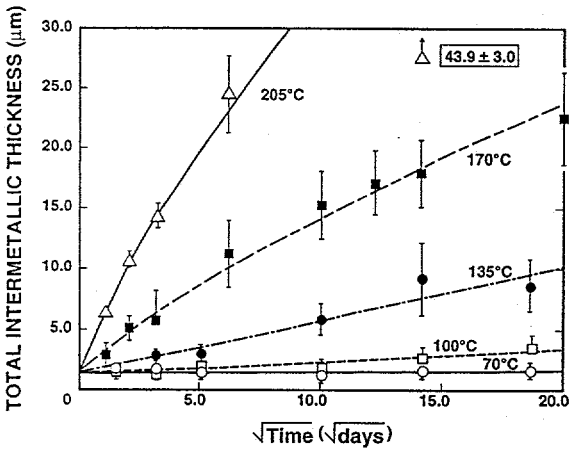


Figure 2: Parallel plate capillary flow solderability test data for the Sn-Ag-Bi solder (designated "5%Bi") as a function of gap size for tests performed at 230°C, 245°C, and 260°C. Sn-Ag and Sn-Pb solder test data have been included for comparison.

for Sn-Pb and Sn-Ag solders have been included for comparison. Ring-in-plug tests on the Sn-Ag-Bi demonstrated a shear strength for the Sn-Ag-Bi solder of 81±11MPa. This value is significantly higher than the strengths of the Sn-Ag and Sn-Pb solders: 55±1 MPa and 42±2 MPa, respectively. Long-term aging of the Sn-Ag-Bi solder on Cu for periods of up to 400 days and at temperatures of between 70°C and 170°C demonstrated growth kinetics very similar to those of the Sn-Ag solder (Fig. 3).



(a)



(b)

Figure 3: Total intermetallic compound layer thickness between copper and (a) Sn-Ag-Bi or (b) Sn-Ag solders following thermal aging in air.

EXPERIMENTAL

Solder Materials.

The solder compositions (expressed as wt%) that were used in this study included the commercially available alloys: 96.5Sn-3.5Ag (T_s=T_l=138°C where T_s and T_l are the solidus and liquidus temperatures, respectively) and 58Bi-42Sn (T_s=T_l=138°C). In both cases, the solder pastes were formulated with a rosin-based, mildly activated (RMA) flux, metal content of 89-91%, and a particle size of 40-50 microns. The 91.84Sn-3.33Ag-4.83Bi solder was initially formed as an ingot and subsequently blown into a powder 30-70 microns particle diameter. The powder was mixed with an RMA-based flux vehicle to a metals content of 90.5%.

Test Vehicle.

The test vehicle used in this study is shown in Fig. 4. It had top side and bottom side surface mount components with no vias. The circuit board measured 2.41 x 1.50 cm and was 0.178 cm thick. The laminate was polyimide-quartz with "1 oz." copper features. A dry solder mask covered the appropriate areas of the board surface. The copper features of the test specimens were coated with either an immersion tin layer or with an organic solderability preservative (OSP); both protective finishes were applied from commercially available products. The circuit boards were baked at 120°C for 4 hours prior to assembly. Signal passage between the top and bottom surfaces as well as to the rest of the system was provided by edge clips. The edge clips were attached with 63Sn-37Pb solder and were separated from the device pads by solder mask so at to prevent mixing of the Sn-Pb and non-lead bearing solders.

(a) (b)

0.50 cm

Figure 4: The (a) top and (b) bottom surfaces of the test vehicle.

As is observed in Fig. 4, the *top* side of the test vehicle was populated with five devices: a large "1825" chip capacitor (designated C6); two small "0805" chip capacitors (C1 and C2); a beam-leaded small outline transistor (SOT, designation Q1); and a resonator package (SM-1). The *bottom* side contained a single "1210" capacitor (C5) and a 16 I/O small outline integrated circuit (SOIC, designation U1). The SOIC lead configuration was gull-wing. The chip capacitors were supplied with 100Sn plated finishes over Ni or Cu barrier layers. The SOT and SOIC leads were manufactured of a low expansion alloy that had been electroplated with a solderable finish of Ni followed by a protective Au layer. The Au coating was removed from these two devices by hot-solder dipping each lead (or row of leads) in a 100%Sn bath (270°C) using an RMA flux.

The immersion step was performed three times[17]. The finish on the SM-1 was a Au/Au-W metallization. The Au was not replaced with a 100Sn finish in order to prevent an inordinate amount of Sn from being encompassed into the solder.

Assembly Procedures.
The test vehicles were assembled via a double reflow process in order to populate both sides of the board. The bottom side was assembled first, followed by the top side which included the attachment of the edge clips. For each side, the paste was dispensed using a 127 micron thick stencil, and the parts automatically placed in the proper locations. Reflow was performed in a four-zone, convective/infrared furnace (60% convective/40% infrared) under a nitrogen atmosphere. The thermal profiles were based upon a preheat of 1.5 to 2 min. at approximately 175°C followed by the spike of 45 to 60 sec time duration above reflow with a peak temperature 20 to 30°C above the melting point. All units were cleaned of flux residues following each of the reflow cycles. Cleanliness evaluations for ionic residues were performed on all of the units; each passed under the designated criterion. *Rework of the units was not permitted.*

Manufacturability Assessment.
A visual assessment of the solder joints was initially performed by the operators to determine whether *generally* acceptable joints were being formed. Such was the case with each of the solders.

A more extensive defect analysis was based upon a set of Figures of Merit (FOM) which quantified the visual attributes of the joints. The following guidelines and FOMs were used for the quantitative assessment:

Chip capacitors and SM-1: Pad wettability was determined on a scale of 0 (good) to 4 (poor). Chip termination wettability was documented as the number of non-wetted terminations: 0 (good), 1, or 2 (poor). Dewetting was determined as a count of the number of terminations (excluded the SM-1 unit) and the number of pads showing the phenomenon. Externally observed voids were evaluated simply as the number of them occurring in any and all joints. Part misregistration was categorized as either: (1) "lateral", i.e., parallel to the short axis; (2) "longitudinal", parallel to the long axis; or (3) rotational. The extent of each displacement was judged in severity as 0 (none), 1 (slight), 2 (moderate), and 3 (severe). Lastly, solder balls (under the packages) were ranked on a scale of 1 (poor) to 5 (none).

SOT and SOIC: Pad wettability was 0 (good) to 6 (poor) for the SOT and 0 (good) to 16 (poor) for the SOIC. Lead wettability was counted as simply the number of non-wetted leads: 0 to 3 for the SOT and 0 to 16 for the SOIC. Dewetting, external voids, misregistration, and solder balls were evaluated in the same manner as for chip capacitors and the SM-1.

Pads: Two sets of (unoccupied) bonding pads were evaluated for wetting and dewetting on a scale of 0 (no defect), 1 (one pad defective), and 2 (both pads defective).

The following procedure was developed to compile the quantitative data in order to arrive at a generalized or average figure-of-merit, <FOM>, for the test vehicles of a particular solder alloy. The value of <FOM> was calculated as an arithmetic average:

$$\langle FOM \rangle = \Sigma FOM / \Sigma(\text{Test Vehicles}) \qquad (1)$$

where ΣFOM is the total of all of the FOM 's added together from the particular board group and Σ(Test Vehicles) is the total number of circuit boards used in the evaluation. Scatter in the data was represented as $\pm$ one standard deviation.

Reliability Analysis.
The reliability analysis of the solder joints can be separated into two parts: (1) environmental stressing and (2) solder joint integrity evaluation. Environmental stressing was based upon the provision of solder joints in the as-fabricated condition, those exposed to thermal cycling ("slow" temperature ramps), and units subjected to thermal shock ("fast" temperature ramps) exposure. The thermal cycling conditions were: -55°C and 115°C for the lower and upper limits, respectively; 6°C/min ramps; 30 min holds at the limits; and 300 total cycles with visual observations performed after 150 cycles. The thermal shock test parameters were: -55°C and 100°C limits; liquid-to-liquid transfer; 15 min dwell at the temperature limits; and 400 total cycles. A total of 13 units were examined in the as-fabricated condition (all with the immersion tin finish); 16 units were assessed after thermal cycling (13 with immersion tin and 3 with the OSP); and 13 units were evaluated after thermal shock exposure (all with the immersion tin finish).

The evaluation of prototypes in the as-fabricated condition as well as those following thermal cycling or thermal shock exposures was comprised of: (1) an assessment of the solder joint microstructure through metallographic cross sections and (2) mechanical shear tests on the chip resistors and SM-1 resonator package. For metallographic analysis, three circuit boards were evaluated so that three solder joints could be examined per device type. Longitudinal cross sections were made through the chip capacitors and SM-1 so that both joints were included. Single joints were viewed of the SOT. In the case of the SOIC package, three cuts were made across the package frame which included two solder joints each, for a total of six joints. A quantitative evaluation scheme was derived which assessed each solder joint for the following attributes: (1) internal voids, (2) fillet integrity (e.g., cracks, plastic deformation, etc.), and (3) device I/O wettability and package condition (primarily cracked capacitors). Of the three attributes, the propensity for internal voids actually reflected upon manufacturing processes since such defects were not expected to be formed by thermal cycling conditions. However, it is

included here for documentation. Each of the attributes was evaluated on a figure-of-merit defined by a scale of 0 (numerous defects) to 5 (no defects). The data was compiled for each device, per each solder, and computed according to equation (1). The mean value and ± one standard deviation represented each data set.

The mechanical (simple) shear tests were performed on a jig shown in Fig. 5. The fixture was placed into a testing machine which monitored load and displacement. Tests were performed at a displacement rate of 10 mm/min. Seven test vehicles per solder were reserved for mechanical strength measurements so that test data from seven parts comprised a mean strength and a scatter (±one standard deviation).

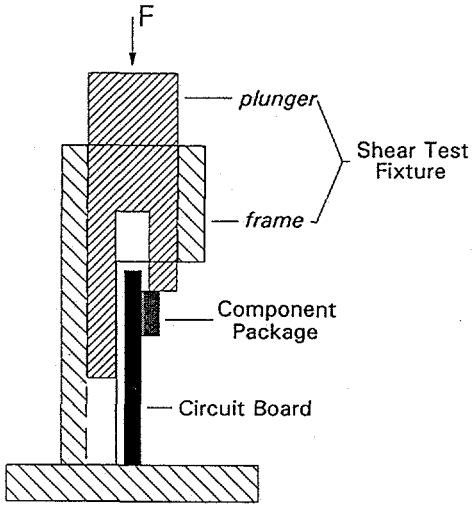


Figure 5: Jig used to shear test the chip capacitors and SM-1 component package from the circuit board.

RESULTS AND DISCUSSION

Manufacturing Feasibility Defect Analysis

The defect analysis will be examined with respect to the properties of: (1) wettability, (2) dewetting, (3) external voids, (4) misregistration, and (5) solder balls. Based upon prototype studies with lead-free solders, wettability is a critical area of analysis and will therefore receive extensive attention. Shown in Fig. 6 are the FOMs for the chip capacitors, C1, C2, C6, and C5 along with that of the SM-1. The FOM ranges from 0 (good) to 4 (poor). The large scatter was attributed more so to the limited number of test boards than properties for the respective devices. Overall, the data show that the worst wettability occurred with the 96.5Sn-3.5Ag solder; the best wetting was observed with the Sn-Ag-Bi solder. It can also be noted that the extent of nonwetting demonstrated a general dependence on the particular device with non-wetting being greatest with the C6, followed by the SM-1 components, and so on. Both C6 and SM-1 were the larger non-leaded device packages as well as being located at the board edges (C5 was the third largest followed by C1 and C2 as the smallest packages). Therefore, reduced heat input due largely to device size was a likely cause of the wettability trends as a function of

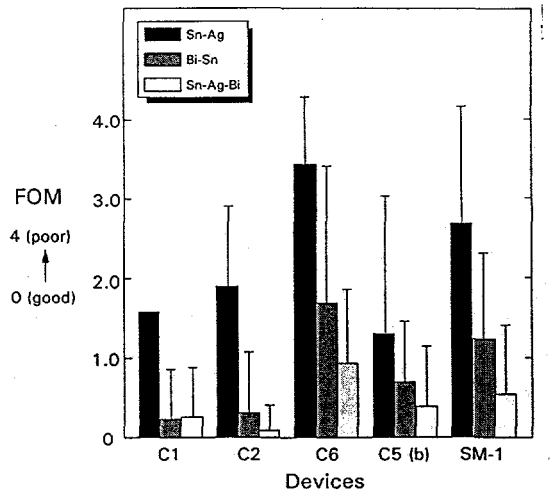


Figure 6: Circuit board pad wettability for the devices C1, C2, C6, C5, and SM-1 with the immersion tin finish. C1, C2, C6, and SM-1 were on the top surface and C5 was on the bottom surface.

component. The same solder alloy dependence by wettability was also observed for the leaded devices, Q1 and U1, as well as the vacant pads (Fig. 7). Measurable dewetting of the circuit board pad surfaces was observed only on the U1 pads with an FOM of 4.2±0.6 as compared with a value of 16 being the worst case.

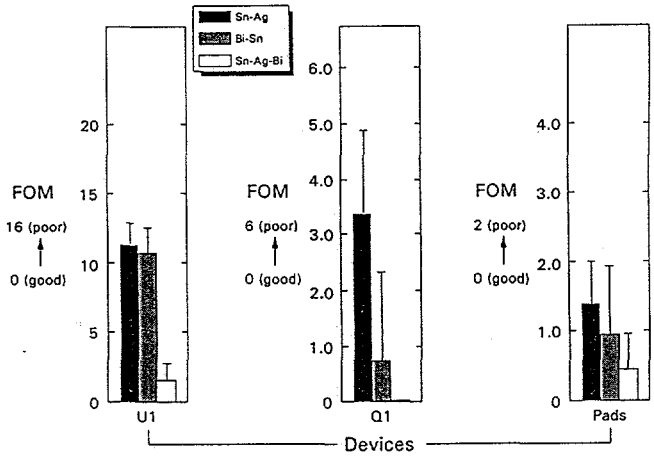


Figure 7: Circuit board pad wettability for the devices U1, Q1, and vacant pads with the immersion tin finish.

Circuit board pad wetting was considerably deteriorated with the OSP finish. In general, the same trend of wettability as a function of solder alloy was observed in the order of most-to-least defects: Sn-Ag, Bi-Sn, and Sn-Ag-Bi.

Wetting of the package termination or leads was excellent in all cases. Dewetting was absent, as well. Void formation was observed largely on the C1 and C2 capacitors as well as the gull wing joints of U1; however, the magnitude was not appreciable and did not exhibit a

significant solder alloy dependence. This latter observation suggests that void formation may have been a property of the Sn surface finish (e.g., the volatilization of entrapped organic compounds or water vapor during the reflow process).

Device misregistration reflects the capacity for the solder to align devices which are not properly centered on the pads during the placement process. Shown in Fig. 8a is the bar diagram of the FOMs for each of the three displacement "vectors" (longitudinal and lateral cases as per the insert in the upper right-hand corner) for the C1 and C2 chip capacitor measurements. In general, for each classification of misregistration (longitudinal, lateral, or rotational), the overall magnitude was very slight. Longitudinal displacements and chip rotation were the most and least observed defects, respectively. However, lateral displacements gained prevalence on the C2 capacitor. a higher propensity for misregistration was observed with the Bi-Sn solder. This observation reflects the lower surface tension of the Bi-Sn solder (310 dynes/cm) as compared to values of the other alloys (490 dynes/cm and 418 dyne/cm for the Sn-Ag and Sn-Ag-Bi solders, respectively)[6]. The surface tension provides a mechanical force which centers the package between the pads in order to minimize system free energy; the higher the surface tension, greater is the alignment force. The C5 and C6 capacitors showed similar trends; again, most of the orientation defects were associated with the Bi-Sn solder (Fig. 8b).

The misregistration of the Q1 (SOT) and SM-1 packages produced a different situation because the wettable area of each package was non-symmetrical. Shown in Fig. 8c are the FOMs for each of the misregistrations from the Q1 and SM-1 packages. The pictorial inserts describe the bonding format of the two packages. In the case of the SOT, the solder surface tension of the joint of the non-paired lead would cause a persistent longitudinal shift to exist which was observed. The shift would expectedly increase for solders with higher surface tension which was borne out by observing that the least shift occurred with the Bi-Sn solder. The effect, however, was not sufficiently strong enough to distinguish between the Sn-Ag and Sn-Ag-Bi solders. Lateral misregistration was small; however, the amount of rotated parts was high, indicating a placement problem.

Longitudinal shifts were expected, and observed, for the SM-1 package since the bond (or wettability) area is larger on one end than the other (insert in Fig. 8c). Solder surface tension would tend to pull the package toward the end with the larger bond area. Again, the longitudinal shift was weakest for the Bi-Sn solder due to its lower surface tension. The high lateral shift was caused by the package literally "rolling" off of the solder bumps comprising the joints; this phenomenon would have no consistent solder composition dependence; this point was verified by the data in Fig. 8c.

Finally, the propensity for solder ball formation was examined. The only solder balls remaining were those

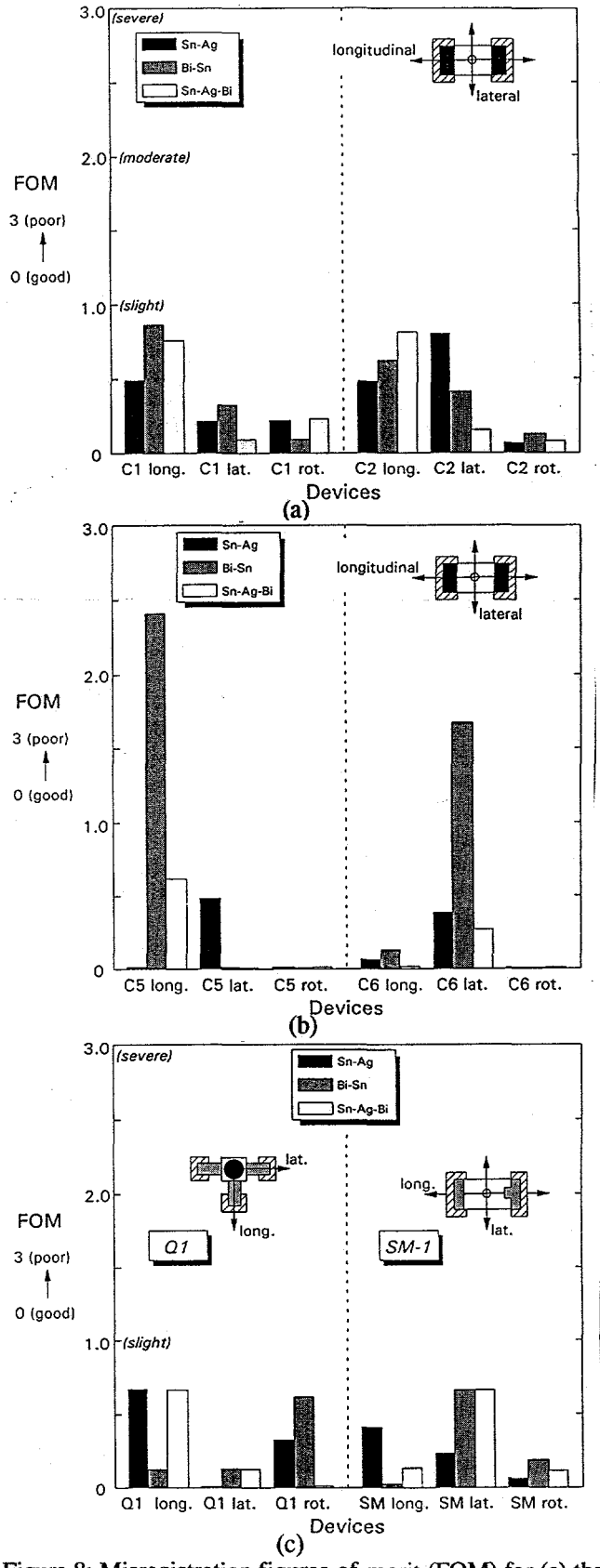


Figure 8: Misregistration figures-of-merit (FOM) for (a) the C1 and C2 chip capacitors, (b) C5 and C6 chip capacitors, and (c) the Q1 and SM-1 packages.

located under the package which could not be loosened when each of the test vehicles was cleaned after assembly. The magnitude of solder balls was very limited in all cases. Solder balls were not observed at all for the U1 package, due to the high package-to-laminate clearance. Generally, solder balls were more prevalent with the Bi-Sn solder per a given package. Readily oxidized Bi-Sn particles and a lower process temperature profile that may not have completely removed paste volatiles, were the two likely causes for preferred solder ball formation with this solder.

In summary, the manufacturing feasibility analysis determined that there were no catastrophic assembly problems from the test vehicles fabricated with the Bi-Sn, Sn-Ag, and Sn-Ag-Bi lead-free solders. It is believed that the defects which were noted in the analysis, could likely be eliminated with normal process development such as: (1) paste reformulation; (2) print and placing procedures; and (3) further furnace profile optimization. Overall, the quantitative analysis indicates that the best performance was realized with the Sn-Ag-Bi solder, followed by the Bi-Sn alloy, and lastly, the Sn-Ag eutectic solder. This determination is heavily weighted with respect to the wettability results which are very sensitive to the solder composition, and most critical to the successful assembly application.

Reliability Analysis - Solder Joint Microstructure.
As-fabricated test vehicles.
The first analysis derived from optical microscopy of the solder joint cross sections was the extent of void formation. As noted earlier, this attribute was more reflective of the manufacturing process rather than thermal fatigue as void formation and/or expansion were not expected to be a consequence of thermal fatigue. Shown in Fig. 9 are the

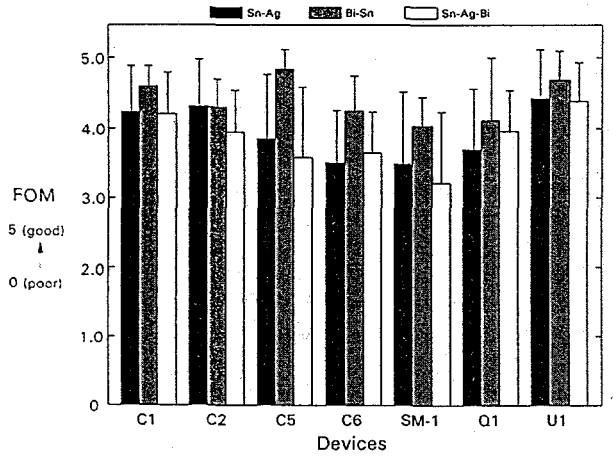


Figure 9: Solder fillet voiding FOM for each of the devices and solders. Data from each of the as-fabricated units as well as those exposed to thermal shock or thermal cycle exposure were combined in the analysis.

FOM data for voids from the combined as-fabricated, thermal shock, and thermal cycled test vehicles. It was noted that, for the leadless devices (i.e., C1, C2, C5, C6, and SM-1), the propensity for void formation increased as the package size increased. Larger packages have a greater thermal lag in the heating cycle. Therefore, their maximum temperature as well as the time at peak temperature becomes more limited so that paste volatiles have less opportunity to exit the joint. A larger physical size of the package also limits the escape paths available to the gaseous volatiles, thereby entrapping them in the joint. Void formation was reduced for the leaded packages because of the smaller I/O dimensions as well as the likelihood of their improved heating since the package is removed from the joint area by a lead, the material of which has relatively poor thermal conductivity.

In all cases, the Bi-Sn solder exhibited less void formation than the other solders for all of the devices. The opposite trend would have been expected since the reduced temperatures of the heating profile would have hampered the removal of paste volatiles. However, this behavior may demonstrate, rather, the effect of the lower surface tension of the Bi-Sn solder as compared with the other alloys (see the previous section for values). The lower surface tension would facilitate the release of gas bubbles during solder reflow. The behaviors were not significantly different between the Sn-Ag and Sn-Ag-Bi alloys.

Both damage to the devices and solder wettability of terminations and leads (viewed in cross section) were also included in the analysis. A primary damage concern was cracking of the ceramic chip capacitors as well as the ceramic bodies of the U1 SOIC, Q1 SOT, and the SM-1 specialized package under the relatively high processing temperatures of the Sn-Ag and Sn-Ag-Bi solders. In all cases, no significant damage was recorded. The wettability analysis, like the void assessment above, reflects more on the manufacturing process than on thermal cycling effects. Wetting defects were very few; those that were observed primarily with Sn-Ag solder on the C5 capacitor and the SM-1 package. However, the incidents were isolated and so did not represent a persistent problem with these particular packages. These results confirmed the low magnification visual assessment of the solder joints described earlier in the manufacturability assessment.

The attribute of primary interest in the reliability assessment was the *fillet integrity* of each of the devices. The effects of solder fillet damage would include plastic deformation such as grain boundary or phase boundary sliding as well as the formation of cracks. Shown in Fig. 10 is the bar chart of the fillet integrity FOM for units in the as-fabricated condition. The solder joints of the all of the leadless packages, i.e., all of the chip capacitors as well as the SM-1 device, were flawless. However, the Q1 SOT and U1 SOIC packages with leaded I/Os exhibited a limited amount of damage to the solder fillets, most noticeably with the Bi-Sn and Sn-Ag-Bi solders. Because the lead and laminate materials had well matched thermal expansion coefficients, thermal strains due to global thermal expansion mismatch were expected to be minimal. Moreover, the SOT and SOIC packages were leaded which

would further reduce the extend of mismatch strain as displacements are relieved by the compliance of the leads.

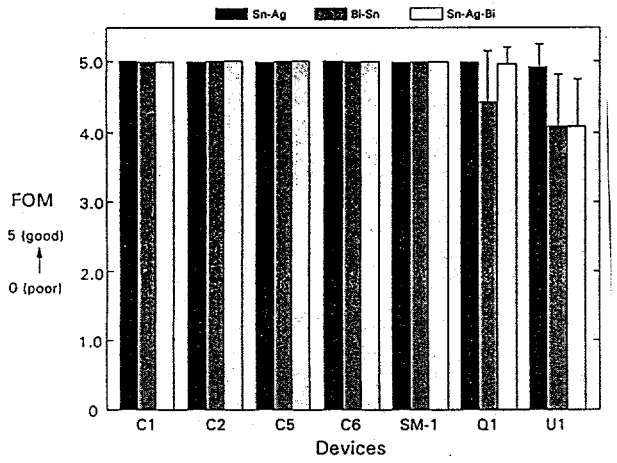


Figure 10: Fillet integrity FOM chart for solder joints in the as-fabricated condition.

Rather, it appears that *local* expansion mismatch between the lead material or circuit board laminate and the solder alloys was the primary damage mechanism in these test vehicles. The leads were fabricated of low thermal expansions ferrous alloys. The relatively high thermal expansion coefficient of the solders, particularly the Sn-Ag-Bi solder owing to the high Sn content, would result in a significant strain to the solder material.

Solder joint deformation was in the form of grain and/or phase boundary sliding as was observed for the Bi-Sn and Sn-Ag solders in previous experiments[11]. The extent of damage was somewhat greater with the gull wing leads of the SOIC than appeared on the beam leads of the SOT. Although the linear dimension of both leads was nearly equivalent, the gap formed between the lead and the copper pad of the circuit board was considerably smaller for the SOIC due to the weight of the package. Since the strain introduced into the solder is proportional to the reciprocal gap distance, the damage would be greater under the SOIC gull wing leads than the SOT beam leads.

Thermal shocked test vehicles.
The fillet integrity FOMs compiled from units exposed to 400 thermal shock cycles are shown in Fig. 11. All of these solders exhibited some degree of deterioration. This loss is more clearly illustrated in Fig. 12 which shows the change in FOM between the as-fabricated units and those subjected to 400 thermal shock cycles. The Sn-Ag solder had the best overall performance, with fillet damage limited to the SM-1, Q1, and U1 solder joints. Grain boundary sliding and some minor crack formation, particularly at the grain boundary triple points, characterized the microstructural damage. The increased damage to the SM-1 solder joints may indicate a small contribution by global thermal

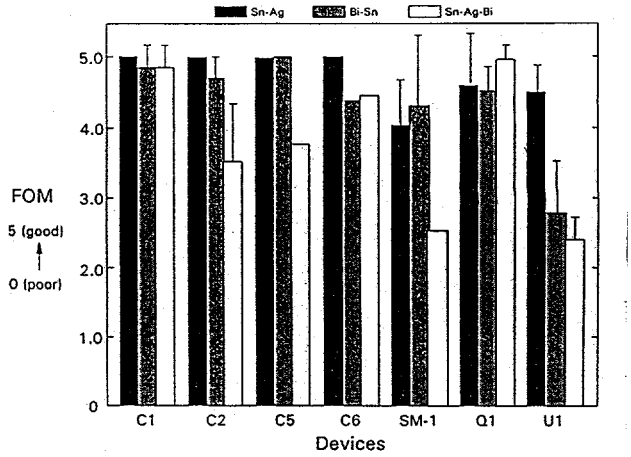


Figure 11: Fillet integrity FOM chart for solder joints after 400 thermal shock cycle exposure.

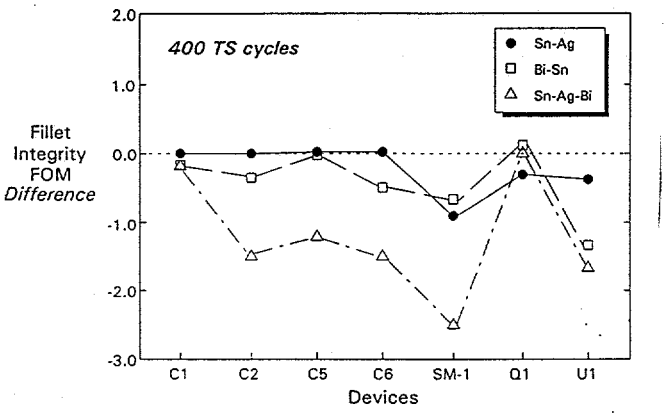


Figure 12: Fillet integrity FOM *difference* between the as-fabricated units and those subjected to 400 thermal shock (TS) cycles.

expansion mismatch. Local mismatch strains were believed to predominate the Q1 and U1 solder joints.

Solder joint integrity was deteriorated slightly more so with the Bi-Sn solder; the change was particularly large for the SM-1 and the SOIC (U1) packages. Although global mismatch effects were present as exemplified by the increasing magnitude of the FOM difference with increased size of the leadless devices (Fig. 12), the local thermal expansion mismatch between the solder and the package and/or substrate were once again dominant as noted by damage in the leaded device joints. However, the differing behaviors between the Q1 and U1 devices accentuate the role that solder joint gap had on microstructural damage generation; the Q1 joints incurred no additional damage by the thermal shock exposure.

The results in Figs. 11 and 12 indicate that the Sn-Ag-Bi solder exhibited the greatest degree of solder joint damage. Generally, the extent of deterioration increased with package size for the leadless devices, confirming that global mismatch had a noticeable effect on the solder integrity. An interesting observation from the data in Fig. 12 is that a greater degree of damage took place in the C2 joints than the C1 fillets, despite the chip capacitors having exactly the same dimension. Review of the manufacturability analysis, including wettability (Fig. 6), misregistration (Fig. 8) and void formation (Fig. 9) did not indicate that the C2 units were initially more defect prone than the C1 units. This behavior suggests that the position of the device on the circuit board, with respect to both location on the laminate as well as proximity to other packages, can impact solder joint reliability. This is particularly the case with thermal shock conditions in which non-equilibrium temperature gradients may be established across the test vehicle circuit board.

As was the case of the Bi-Sn solder, the Sn-Ag-Bi alloy exhibited severe degradation of the U1 joints. However, no additional damage to the Q1 joints after thermal shock exposure was observed.

Microstructural damage to the Sn-Ag-Bi solder joints was largely grain boundary sliding (Fig. 13). However, the

Figure 13: Micrograph of a Sn-Ag-Bi U1 solder joint following 400 thermal shock exposure (SEM).

damage was particularly severe in the SM-1 solder joints, resulting in cracks near the solder/SM-1 package interface (Fig. 14). As can be seen in the scanning electron micrograph (SEM) micrograph, voids in the joints (which were extensive in these joints as noted in Fig. 9) appeared to influence crack propagation.

In summary, the data in Figs. 11 and 12 indicate that thermal shock exposure over the range of -55°C to 100°C caused microstructural damage to the joints with general severity in increasing order shown by the Sn-Ag, Bi-Sn, and

Figure 14: SEM micrograph of crack formation in a Sn-Ag-Bi SM-1 solder joint following 400 thermal shock cycles exposure.

Sn-Ag-Bi solders. Damage to the leadless package solder joints reflected a growing influence by global thermal expansion mismatch; however, local affects were still important as exemplified the U1 joint conditions. The damage mechanism remained grain and/or phase boundary sliding which in severe cases, culminated in the formation of cracks at boundary triple points. Microstructural coarsening or shear band formation, which are the damage characteristics of the traditional Sn-Pb solders, were not observed.

Thermal cycled test vehicles.

Exposure of the solder joints to thermal cycling environments (i.e., slower temperature ramp rates) impacted the solder microstructure. The fillet integrity FOM difference diagram for samples exposed to 300 thermal cycles is shown in Fig. 15. These results were compared

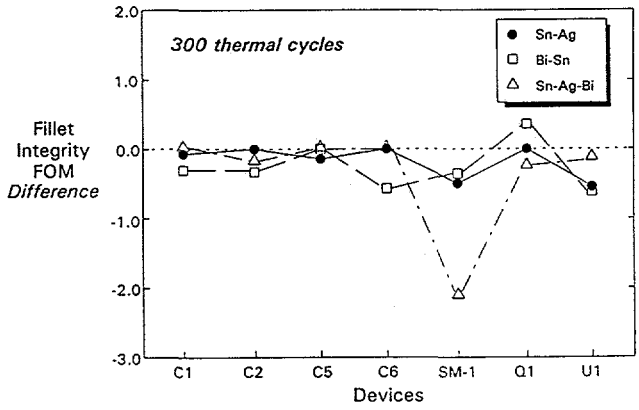


Figure 15: Fillet integrity FOM *difference* diagram for solder joints after exposure to 300 thermal cycles.

with those in Fig. 12 from the thermally shocked units. The Sn-Ag and Sn-Ag-Bi solders exhibited negligible change to the fillets of the chip capacitors. Slightly more degradation was observed with the Bi-Sn alloy; the trend showed a negligible dependence upon the package size. Deformation was in the form of phase boundary sliding, located in the gap between the pad and package. The solder fillet was not disturbed (Fig. 16). The Bi-Sn and Sn-Ag-Bi solders

(a)

(b)

Figure 16: (a) C6 chip capacitor solder joint following 300 thermal cycles showing phase boundary sliding in the gap region only (optical). (b) High magnification image of the fillet region showing an absence of phase boundary sliding (SEM).

exhibited considerably less deterioration after thermal cycling than was observed following thermal shock testing for the same components. Only the Sn-Ag-Bi solder had a significant decline of SM-1 solder joint integrity; the changes were only very slight for the Sn-Ag and Bi-Sn solders. As in the case of thermal shock exposure, the Q1 solder joints exhibited no additional degradation after thermal cycling. Lastly, the U1 solder joint deformation observed with the Sn-Ag-Bi and Bi-Sn alloys on the U1 device after thermal shock (grain boundary and phase boundary sliding for the Sn-Ag-Bi and Bi-Sn solders, respectively) was significantly less in the thermal cycling case than following the thermal shock exposure. The deformation mechanism remained unchanged. The Sn-Ag, U1 solder joint exhibited the same degree of deterioration between the two aging treatments.

A closer inspection was performed of phase boundary sliding in the U1 solder joints fabricated with the Bi-Sn alloy. This analysis indicated that, in addition to boundary sliding being found only in the gap region, its magnitude was directly dependent upon the gap thickness. This point is illustrated by the SEM micrographs in Fig. 17. The larger gap in Fig. 17a exhibited no phase boundary sliding while in the smaller gap in Fig. 17b, phase boundary sliding was quite prevalent.

Combined thermal shock/thermal cycling evaluation.
A comparison of the thermal shock and thermal cycling data resulted in the following general observations: (1) Thermal shock was more degrading to the solder joints than thermal cycling. (2) Thermal shock damage was greatest for joints with the Sn-Ag-Bi solder and least for those with the Sn-Ag solder. On the other hand, all three solders exhibited similar degrees of microstructural change after thermal cycling with the exception of the SM-1 package. (3) The dependence of deformation on package size for the leadless components was significant only in the thermal shock case. (4) On a component-by-component basis, solder degradation was generally greatest with the SM-1 package joints, followed by the leaded U1 SOIC and SOT joints, and least for the chip capacitors.

The description (with a goal of "prediction") of the impact which thermal stressing has on the microstructure of the lead-free solder joints (Figs. 11, 12, and 15) must include the following points: (1)manufacturing defects in the joints; (2) the mechanical and physical metallurgy of the solder; (3) the solder joint configuration, including joint geometry as well as the properties of the lead or termination and substrate materials; and (4) the thermal environment conditions. An analysis of the data with respect to the above points was made with the objective of developing some general trends.

It was noted in the previous section that each solder exhibited acceptable manufacturability based upon the defect analysis. The trends and behaviors of the solder joints observed following thermal shock and/or thermal cycling exposures (Figs. 1, 12, and 15) did not corroborate with the differences recorded in the defect analyses (between solder or components). For example, although the

(a)

(b)

Figure 17: Bi-Sn solder joint gaps on a U1 lead after 300 thermal cycles: (a) large gap and (b) small gap (SEM).

Sn-Ag-Bi solder exhibited the greatest amount of fillet deformation of the three solders following thermal stressing, it exhibited a best overall wettability as well as comparable registration and voiding performance. A very weak link may exist between the manufacturability data and the thermal stressing results of the SM-1 joints, specifically, void formation versus fillet damage. *In the earlier assessment, the assembly processes produced acceptable, consistent solder joints such that defects did not significantly affect the reliability analysis.*

When considering the extent of thermal fatigue in a solder joint, the mechanical properties of the solder (strength, creep resistance, etc.) as well as the thermal expansions coefficients of the solder and substrate materials are important parameters. Pertinent properties of the solder, device package, and circuit board materials are listed in Table 1. The substrate materials (i.e., leadless packages, lead materials, and laminate) were expected to minimize global thermal expansion mismatch strains during thermal cycling. The lead-free solders are considerably stronger than their 63Sn-37Pb counterpart. The thermal expansion coefficients of the Sn-Ag and Sn-Ag-Bi alloys were assumed to be close to that of 100Sn since exact values were not available. The Bi-Sn solder has a lower thermal expansion coefficient than the other lead-free alloys; however, it is still considerably higher than those of the substrate materials.

Material	Shear Strength[1] (MPa)	Thermal Expansion Coefficient (ppm °C^{-1})
Alumina	*****	6 [2]
Polyimide Quartz	*****	6 - 8 [3]
Kovar™	*****	6.5 [4]
96.5Sn-3.5Ag	55 [5]	23 [6]
58Bi-42Sn	63 [5]	14 [7]
Sn-Ag-Bi	81 [5]	23 [6]

(1) Ring-in-plug test; 10 mm/min; 63Sn-37Pb = 42 MPa
(2) R. Klein-Wassink, SOLDING IN ELECTRONICS, (1989), p.373.
(3) R. Prasad, SURF. MOUNT TECH., (1989), p. 125.
(4) LOW THERMAL EXPAN. ALLOYS & COMPOSITES, ed. J. Stephens et al, (1994), p. 9.
(5) P. Vianco, unpublished data.
(6) estimated from values for 100Sn.
(7) Inter. Tin Res. Inst., Pub. 656, p. 60.
Kovar is a registered trademark of Carpenter Technologies

Table 1: Physical and mechanical properties of pertinent test vehicle materials.

Generally, the thermal cycling data demonstrated that, save for the SM-1, Sn-Ag-Bi solder joints, the three solders exhibited a good thermal fatigue resistance. Thermal shock cycles caused greater damage to the solder joint microstructure, the effect being least for the Sn-Ag solder, moderate for the Bi-Sn alloy, and greatest for the Sn-Ag-Bi solder. The strengths and ductility of the solders would increase and decrease, respectively, in the same order *These results suggest that the stronger (less ductile) high temperature solders were more susceptible to microstructural damage under thermal shock environments (high temperature ramp rates) rather than to thermal cycling tests (slow temperature ramps).*

Mechanistically, the global thermal expansion mismatch predicted between the ceramic devices and the circuit board, was minimized, particularly by the selection of a polyimide laminate (Table 1). The role which the local thermal expansion mismatch has on the solder joint integrity was initially illustrated by the decrease in the as-fabricated U1 joint fillet integrity (Fig. 10) The Sn-Ag-Bi alloy, and to a lesser extent, the Bi-Sn alloy, demonstrated some damage, probably due to the solder solidification process which approximated one-half of a thermal shock cycle. The sensitivity of these solders to local mismatch strains was further accentuated by the thermal shock data

for the U1 solder joints (Fig. 11 and 12). Thermal shock caused a noticeable sensitivity to the even the minimal global thermal expansion differences. In all cases, damage was dependent upon the joint gap geometry, increasing as the gap became smaller. *The high temperature solders are particularly sensitive to local thermal expansion mismatches of materials used in the solder joint under thermal shock environments. This sensitivity extends to global thermal expansion differences, even under the best match system as in the current study.*

It was noted that the SM-1 package incurred the most extensive degree of damage. The thermal shock data indicated that this behavior stemmed from an overall trend of global expansion mismatch effects as evidenced by the other leadless devices. However, such a trend was not present with the other packages following thermal cycling, indicating a joint integrity degradation mechanism that may be unique to the SM-1 package. The propensity for void formation in these joints (Fig. 9) may have enhanced the damage mechanism. However, voids could not always be associated with overall solder damage. Mechanical test data in the following section may further illuminate a possible source.

Reliability Analysis - Mechanical Strength

Shown in Fig. 18 are the maximum shear loads from the C1 and C2 chip capacitors (Fig. 18a) as well as the C6 capacitors and the SM-1 packages (Fig. 18b) for units in the as-fabricated condition and those following thermal shock (TS) or thermal cycling (TC) exposures. In the as-fabricated condition, the joint strengths of both the C1 and C2 capacitors were quite similar between the three solders. This observation suggests that the significantly different ring-in-plug strengths in Table 1 may not exactly be reflect in the (device) solder joint test configuration, particularly when the failure path is not within the solder (e.g., catastrophic failure of the ceramic body or fracture between the ceramic and the thick film termination metallization)[18]. After thermal shock exposure, the C1 capacitors exhibited a strength increase with the Sn-Ag-Bi solder and slight decreases with the other two alloys. Similar trends were noted for the (C1) solder joints exposed to 300 thermal cycles. The fillet integrity FOMs remained unchanged after thermal shock or thermal cycle exposures (Fig. 12 and Fig. 15, respectively), indicating that this parameter was not sufficiently sensitive so as to reflect the microstructural changes responsible for the strength variations.

The trends recorded for the C2 capacitor were mixed after thermal shock or thermal cycle testing. In the case of both Bi-Sn and Sn-Ag-Bi alloys, the strengths decreased after thermal shock testing, and increased as a result of thermal cycling. The strength increase of the Sn-Ag-Bi solder following thermal cycling was substantial; that of the Bi-Sn solder was less dramatic. The Sn-Ag solder joint strength was unchanged after thermal shock testing and experienced a slight decline following thermal cycling. The strength losses by the Bi-Sn and Sn-Ag-Bi solders after thermal

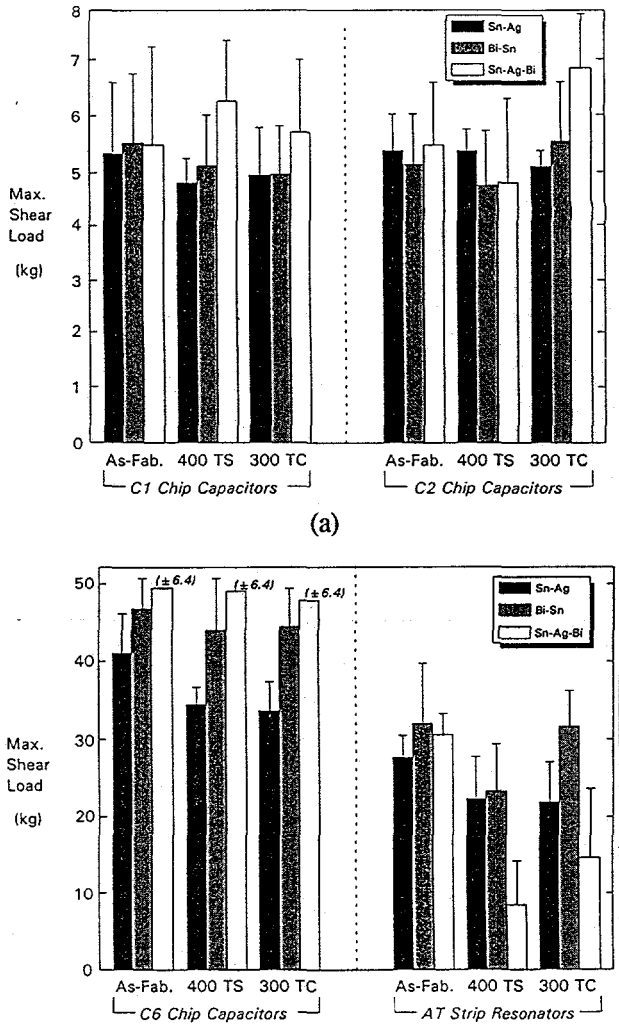


Figure 18: Maximum shear loads for (a) the C1 and C2 capacitors and (b) C6 capacitors and SM-1 packages in the as-fabricated condition, post-400 thermal shock (TS) cycles and post-300 thermal cycles (TC).

shock exposure were accompanied by drops in the corresponding FOMs that indicated significant grain and phase boundary sliding. As in the case of the C1 capacitors, the strength increases of the Bi-Sn and Sn-Ag-Bi solders and small decrease by the Sn-Ag solder were not accompanied by a change to the microstructure significant enough to be recorded by the FOM analysis.

The data in Fig. 18a indicates that the C1 and C2 capacitors had different behaviors, in spite of them being identical devices. This apparent discrepancy may reflect the different locations of the two devices on the circuit board. In general, slight strength decreases are expected from elevated temperature exposure as the microstructure relaxes from the non-equilibrium configuration generated by the solidification process. The increase in strength which appeared to have characterized a large part of the Sn-Ag-Bi solder data may reflect a hardening effect unique to the

solder, probably due to the precipitation of Bi "colonies" within the Sn matrix.

The larger C6 capacitor joints exhibited a greater strength differential between the solders in the as-fabricated condition (Fig. 18b). The strength values reflected the relative ring-in-plug strengths. This distinction was retained in the thermal shock and thermal cycling data, as well. The Sn-Ag showed a strength decrease following each of the thermal aging treatments. A similar trend was noted for the Bi-Sn solder. The C6 solder joints fabricated with the Sn-Ag-Bi alloy exhibited strength values that remained essentially unchanged.

A comparison the of strength data with the FOMs does not result in a significant correlation. For example, the FOM analysis did not reveal a noticeable change to the microstructure which would account for the strength decrease noted in Fig. 18b. The Bi-Sn solder and particularly, the Sn-Ag-Bi alloy showed significant microstructural degradation after thermal shock testing which were not accompanied by similar strength behaviors. Clearly, this analysis indicates that the microstructural damage represented by the magnitude of the FOM change was not sufficient to be reflected in the strength behavior of the C6 capacitor.

An examination of the SM-1 solder joint data is now made. The SM-1 solder joints made of the Sn-Ag alloy showed the same decrease following thermal shock or thermal cycle stressing. The Bi-Sn solder exhibited strength decreases after each of the treatments; however, the decline following thermal shock exposure was largest. The most significant impact of thermal aging treatments was on the Sn-Ag-Bi solder. Considerable strength loss was recorded after either thermal shock or thermal cycle testing; the decrease was greatest after the former.

The FOM analysis reflected the strength deterioration of the three solders after thermal shock exposure, particularly in the magnitude of changes accompanying the Sn-Ag-Bi alloys versus the other two solders. The lower strength of the Sn-Ag-Bi joints after thermal cycling was corroborated by the microstructural damage observed through FOM analysis. The Sn-Ag solder had the same strength and FOM after thermal cycling as that observed after thermal shock exposure. The FOM data from the Bi-Sn solder was not sufficiently sensitive to illustrate the reduced strength change after thermal cycling.

The comparison of the fillet integrity FOM analysis and the strength data for all of the devices confirms the earlier assessment that the mechanical strength was a far more sensitive indicator of microstructural changes to the solder joint system than was a quantitative FOM of solder fillet integrity (deformation). This observation suggests that observed microstructural changes comprising the FOM did not represent the entire range of defects incurred by thermal cycling. The joint mechanical strength was more sensitive to these latent defects. It appeared that changes to the FOM in excess of approximately 1.5 units was required to observe a correlation with the strength measurement.

It was clear from the thermal cycling data (Figs. 15 and 18) and the thermal shock results (Figs. 11, 12, and 18) that the Sn-Ag-Bi solder joint performance for the SM-1 package was particularly deteriorated by the thermal stressing environments. Several contributory factors were considered. First of all, the Sn-Ag-Bi solder had very low ductility due to its high strength. Low ductility, and the fact that the SM-1 package presented the greatest potential for thermal fatigue damage from global thermal expansion mismatch strains, increased the likelihood of poor joint integrity. Secondly, the FOM data recorded from the solder joint cross sections demonstrated that the SM-1 joints were susceptible to void formation. Voids, which were most prevalent with the Sn-Ag-Bi solder, can accelerate fatigue damage due to notch effects.

A third scenario was based upon the Au termination finish of the SM-1 package. Because the package was not hot solder dipped prior to assembly, the retained Au raised the potential for embrittlement of the solder. Because Au embrittlement studies have not been performed specifically on the Sn-Ag-Bi alloy, a hypothesis will have to be inferred from other work. Studies by Jacobson and Humpston indicated that Au contamination of the 96.5Sn-3.5Ag solder causes a loss in ductility when Au concentrations exceed 10wt%[18]. The embrittlement mechanism is the precipitation of $AuSn_4$ platelets. In the case of the 58Bi-42Sn alloy, the formation of such platelets and subsequent ductility drop, occurred at only 0.8 wt% Au.

Some preliminary calculations were made to determine the Au concentration of SM-1 joints on the current test vehicles. Assuming a nominal solder joint having a 76 micron gap and a Au thickness of 2.2 microns along with uniform distribution of Au in the immediate solder layer, the Au contents of the Sn-Ag and Bi-Sn solders were calculated to be 6.6wt% and 5.6wt%, respectively. The Au concentration in the Sn-Ag-Bi solder is well below the embrittlement level for the Sn-Ag alloy; however, it exceeds the minimum of the Bi-Sn solder by a considerable amount. If the presence of Au in the solder joints is truly responsible for the strength loss by the Sn-Ag-Bi solder observed in Fig. 18, then the data suggest that a particularly strong interaction took place between the Sn-Ag-Bi solder and the Au which significantly deteriorated the solder joint strength. Of course, solder embrittlement arising from such an interaction could only be further enhanced by the already low ductility of the high strength Sn-Ag-Bi solder.

In spite of the data scatter recorded with the mechanical strength data, some additional, general trends can be developed from the strength data in Fig. 18: In three of the four devices, the Bi-Sn solder demonstrated a lower strength after the thermal shock treatment as compared with thermal cycling. This trend likely illustrates the lower ductility that is characteristic of the Bi-Sn binary alloy. Limited ductility would be particularly detrimental to joint

integrity when it is subjected to the higher strain rates of a thermal shock exposure as compared to the slower temperature ramps in thermal cycling tests. This trend was less frequent for the Sn-Ag-Bi solder, being observed only on the C2 chip capacitor and the SM-1 package. However, the magnitude of the variation was much greater with the Sn-Ag-Bi alloy. The Sn-Ag solder exhibited a general strength loss indicative of thermal fatigue damage or structural relaxation caused by the elevated temperature exposure.

Finally, the solder joint integrity of all device/solder combinations, with the exception of the SM-1/Sn-Ag-Bi system, remained more than adequate to provide proper mechanical attachment and electrical conductivity between the components and the circuit board.

CONCLUSIONS

1. Prototype circuit board test vehicles were assembled with three candidate lead-free solders: 96.5Sn-3.5Ag, 58Bi-42Sn, and 91.84Sn-3.33Ag-4.83Bi. The devices included leadless chip capacitors and a resonator package as well as SOT and SOIC leaded packages. A polyimide-quartz laminate was selected for the substrate material; reflow was performed in a forced-convection/infrared furnace with RMA flux based pastes.

2. Manufacturing feasibility of the prototype units was established, based upon a defect analysis of the solder joints. Wettability of circuit board features and packages was best with Sn-Ag-Bi alloy, followed in order of Bi-Sn and Sn-Ag solders. The Sn-Ag-Bi solder had a greater propensity for void formation in the joints.

3. The reliability assessment was based upon solder joint microstructure and the shear strength of selected leadless packages. The solder joints of these higher strength alloys were damaged to a greater extent by the thermal shock exposures than by thermal cycling. The Sn-Ag-Bi alloy on the larger SM-1 package appeared most sensitive to the thermal shock tests. Moreover, the test vehicles clearly demonstrated that local thermal expansion mismatch can be as detrimental, or more so, to the integrity of joints made with these solders, than the traditionally thought-of global mismatch damage.

ACKNOWLEDGMENTS

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figure captions

Figure 1: Microstructure of the Sn-Ag-Bi solder (SEM).

Figure 2: Parallel plate capillary flow solderability test data for the Sn-Ag-Bi solder (designated "5%Bi") as a function of gap size for tests performed at 230°C, 245°C, and 260°C. Sn-Ag and Sn-Pb solder test data have been included for comparison.

Figure 3: Total intermetallic compound layer thickness between copper and (a) Sn-Ag-Bi or (b) Sn-Ag solders following thermal aging in air.

Figure 4: The (a) top and (b) bottom surfaces of the test vehicle.

Figure 5: Jig used to shear test the chip capacitors and SM-1 component package from the circuit board.

Figure 6: Circuit board pad wettability for the devices C1, C2, C6, C5, and SM-1 with the immersion tin finish. C1, C2, C6, and SM-1 were on the top surface and C5 was on the bottom surface.

Figure 7: Circuit board pad wettability for the devices Q1, U1, and vacant pads with the immersion tin finish.

Figure 8: Misregistration figures-of-merit (FOM) for (a) the C1 and C2 chip capacitors, (b) C5 and C6 chip capacitors, and (c) the Q1 and SM-1 packages.

Figure 9: Solder fillet voiding FOM for each of the devices and solders. Data from each of the as-fabricated units as well as those exposed to thermal shock or thermal cycle exposure were combined in the analysis.

Figure 10: Fillet integrity FOM chart for solder joints in the as-fabricated condition.

Figure 11: Fillet integrity FOM chart for solder joints after 400 thermal shock cycle exposure.

Figure 12: Fillet integrity FOM *difference* between the as-fabricated units and those subjected to 400 thermal shock (TS) cycles.

Figure 13: Micrograph of a Sn-Ag-Bi U1 solder joint following 400 thermal shock exposure (SEM).

Figure 14: SEM micrograph of crack formation in a Sn-Ag-Bi SM-1 solder joint following 400 thermal shock cycles exposure.

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Table 1: Physical and mechanical properties of pertinent test vehicle materials.

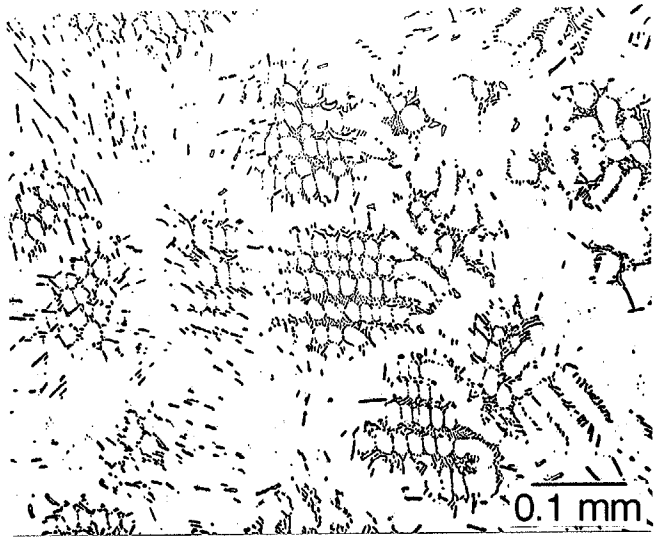
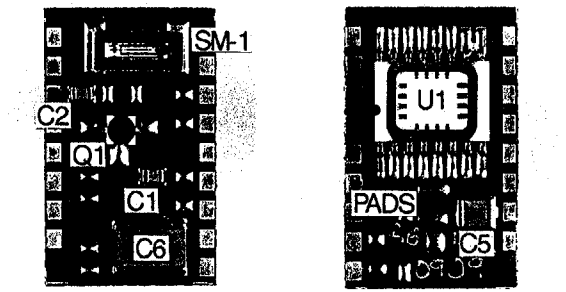


FIG. 1
P. Vianco



(a) (b)

Fig. 4
P. Vranco.

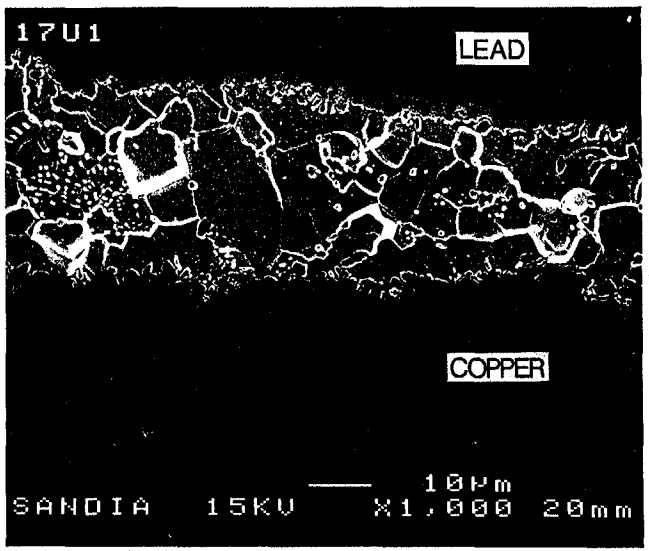


Fig. 13
P. Vlcinco

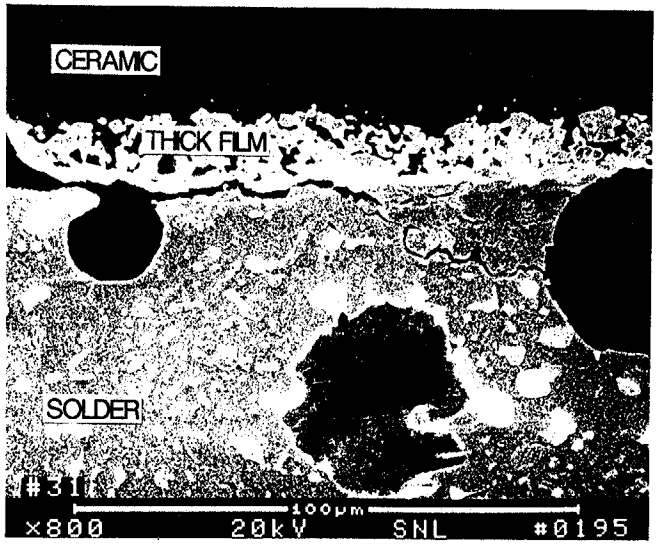
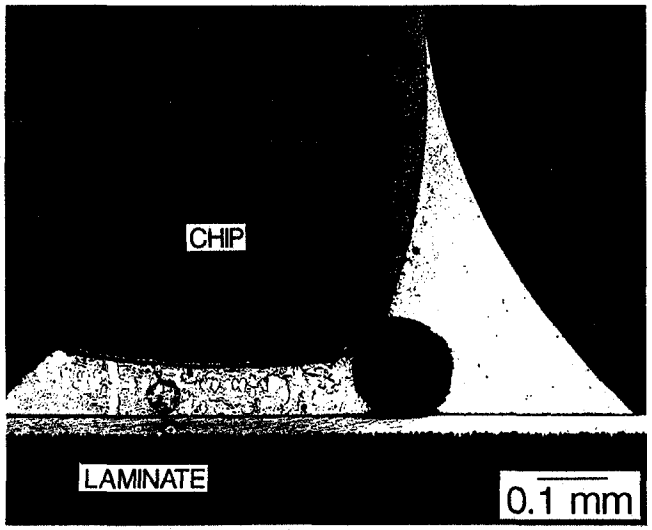
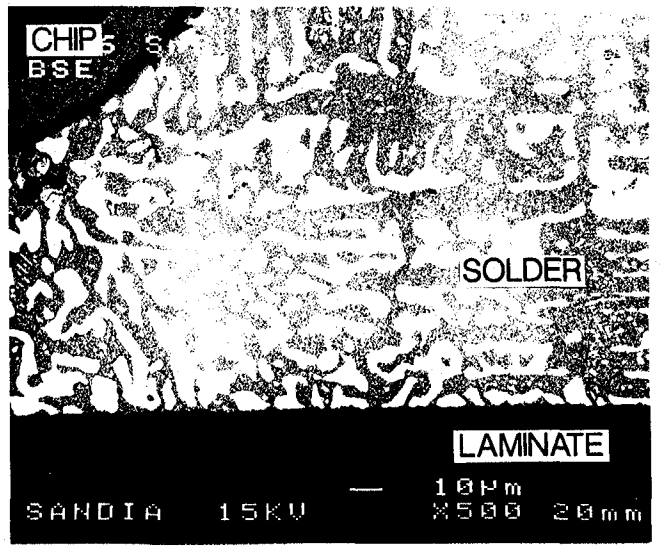


Fig. 14
P. Vianco

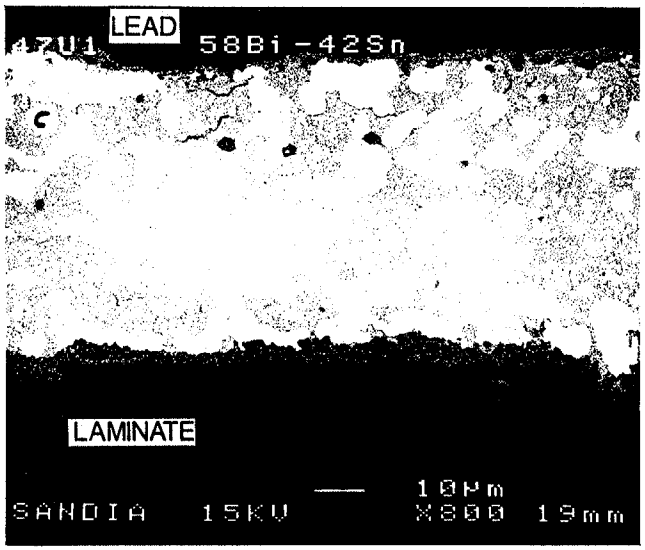


(a)

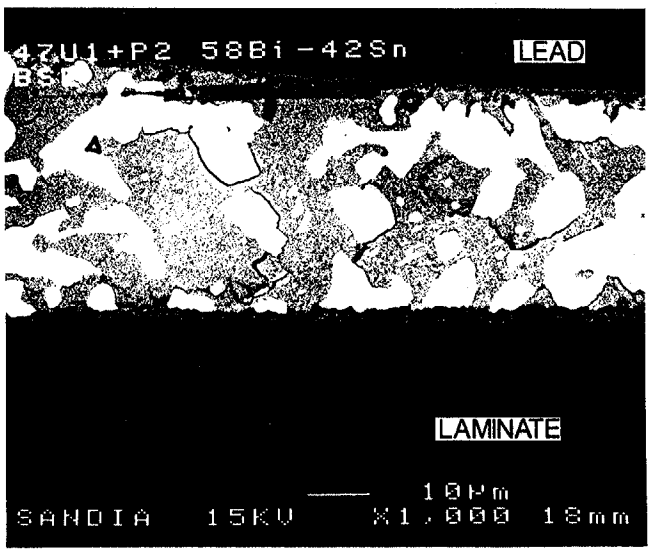


(b)

FIG. 16
P. Vianco



(a)



(b)

Fig. 17
R Vlaico