Die Backside FIB Preparation for Identification and Characterization of Metal Voids

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Abstract

Both the increased complexity of integrated circuits, resulting in six or more levels of integration, and the increasing use of flip-chip packaging have driven the development of integrated circuit (IC) failure analysis tools that can be applied to the backside of the chip. Among these new approaches are focused ion beam (FIB) tools and processes for performing chip edits/repairs from the die backside. This paper describes the use of backside FIB for a failure analysis application rather than for chip repair. Specifically, we used FIB technology to prepare an IC for inspection of voided metal interconnects ("lines") and vias. Conventional FIB milling was combined with a super-enhanced gas assisted milling process that uses XeF_2 for rapid removal of large volumes of bulk silicon. This combined approach allowed removal of the TiW underlayer from a large number of M1 lines simultaneously, enabling rapid localization and plan view imaging of voids in lines and vias with backscattered electron (BSE) imaging in a scanning electron microscope (SEM). Sequential cross sections of individual voided vias enabled us to develop a 3-d reconstruction of these voids. This information clarified how the voids were formed, helping us identify the IC process steps that needed to be changed.

Introduction

Performing FIB circuit modification from the backside of a chip has become routine for flip-chip packaged ICs, where backside access to the chip is required if electrical operation of the IC is to be preserved in the original package [1-4]. Backside FIB modification is also being considered for making repairs at lower-lying nodes (e.g., M1) in multi-layer non-flip-chip ICs that would otherwise require elaborate circuit modification from the front side. Beyond this, backside FIB sample preparation techniques offer a powerful new capability which failure analysts are just beginning to exploit. This paper describes one such failure analysis application: the use of backside FIB milling combined with conventional FIB milling, imaging, and cross-sectioning to enable the investigation of voiding and etch defects in a 2-level metal (aluminum) CMOS technology.

The goal of our study was to identify and image voiding at the M1 level and in the M1 to M2 vias without performing any deprocessing steps that would introduce additional voiding or alter existing voids. Backscattered electron (BSE) imaging performed at the highest primary beam energies (say, 30-40kV) of most scanning electron microscopes (SEMs) can often be used to characterize voiding from the front side of the chip [5], but with limited resolution and only in the uppermost interconnect layers. The resolution of BSE void images suffers even for the top level metal due to the thickness and, for unplanarized technologies, the roughness of the passivation layer covering it. Obtaining crisp images of voids in vias or deeper levels of metal from the front side is problematic because of the thickness of overlying materials and the nonplanar topography in some IC technologies. In our case, the M1 to M2 vias were formed from aluminum as part of the M2 deposition, resulting in a highly nonplanar topography that produced marked shadowing in the SEM images of the vias. More important, however, the presence of a TiW layer at the bottom of M1 prevented imaging of the voids in M1 and in the vias. The strong backscattered signal from the TiW overwhelms the signal from the aluminum interconnect, obscuring any evidence of voiding. While FIB cross-sections through vias or buried metal layers can be used to image voids, only one location or via at a time can be studied, and this technique obviously cannot be used to locate the voids in the first place. Thus, it was necessary to remove the TiW underlayer in order to successfully perform BSE imaging of the voids in M1 and in the M1 to M2 vias. The backside FIB technique described in this paper exposes long lengths of interconnects and

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many vias at one time, allowing voids to be located as well as imaged.

Experimental Approach

In order to remove the TiW underlayer, we first needed to expose the M1 lines from the backside of the chip. A Micrion 9800 FIB system, designed for performing chip repair from the back side, was used for this purpose. This FIB system uses super-enhanced gas assisted milling for quick, uniform removal of the silicon substrate and also has an integrated high resolution infrared (IR) microscope to identify the areas of interest from the backside of the chip.

Super-enhanced gas assisted milling of Si uses the same etchant gas, XeF_2, that is commonly used for the selective removal of SiO_2 and W during "normal" gas assisted milling in a FIB. An important difference between the two processes is the degree of enhancement, which is defined as the increase in material removal during gas assisted milling compared with FIB milling without gas. In the latter case, material removal is accomplished solely by ion sputtering, whereas in the former case a chemical reaction increases the amount of material removed per unit ion dose. The typical enhancement for "normal" gas assisted milling is a factor of 10 – 20. In contrast, super-enhanced gas assisted milling removes Si with an enhancement of ~1000x. This super-enhancement leads to very fast processing times; for the samples used in this study, the silicon (100 – 150 μm thick) was completely removed from areas up to 350 μm x 350 μm in size in less than 30 minutes.

Super-enhancement of Si removal is achieved through the use of a high current density (20 A/cm^2) FIB column combined with a special gas delivery nozzle for XeF_2. As shown in Fig. 1, the ion beam passes through the center of a round nozzle; this nozzle delivers a high XeF_2 flux uniformly to the area scanned by the beam, eliminating the directionality effects that are problematic in performing XeF_2 backside gas assisted milling with the single needle-shaped gas delivery nozzles that are standard for most FIB systems [1]. This special gas delivery approach both super-enhances the milling process and provides a very smooth milled surface. The nozzle is positioned a few hundred microns above the sample. The system base pressure (1 x 10^{-7} torr range without gas flow) is monitored as the XeF_2 gas is introduced and reaches a maximum of ~2 x 10^{-5} torr. The beam current required for a high rate of silicon removal is about 20nA in a spot approximately 0.5 μm in diameter.
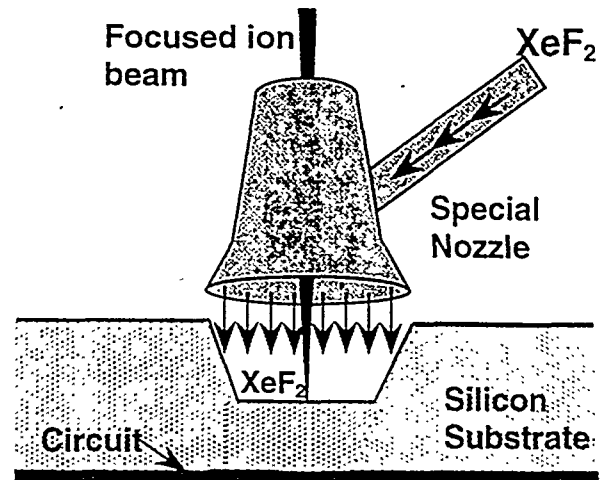

Fig. 1. Special nozzle used for super-enhanced gas assisted milling for backside sample preparation

The high resolution IR microscope integrated into this FIB system detects wavelengths from approximately 0.9 to 1.9 μm. IR imaging was used to locate features of interest from the chip backside, and then localized milling was used to rapidly and completely remove the silicon substrate over the area of interest. The FIB system's laser interferometer stage enables reliable alignment and registration between the FIB image and the IR microscope image.

The samples used in the study were individual dice which were first pre-thinned to 100 - 150 μm by mechanical polishing. Pre-polishing the sample quickly removes relatively large amounts of silicon and also facilitates infrared (IR) imaging of the circuitry 100 - 150 μm beneath the surface by reducing the amount of reflection and diffraction at the back surface. Backside FIB preparation was used in preference to global thinning of the backside of the samples with parallel polishing for several reasons. First, our objective was to expose a number of lines and vias simultaneously with as little thickness variation as possible. Backside thinning accomplished with the polishing wheels used in most FA labs generally cannot achieve the required flatness; the typical thickness variation is a few micrometers over the width of the die. In contrast, the super-enhanced gas assisted milling process permits the complete removal of the Si substrate, exposing the flat back surface of the field and gate oxides. Perhaps more important, globally thinned dice are extremely difficult to handle. Local thinning accomplished with FIB leaves the bulk of the die thick enough (~ 150 μm) to handle with relative ease. Another advantage of the backside FIB tool for this application is that the IR imaging capability permitted easy identification of the locations of interest for local thinning.

After loading the sample in the FIB system, the area of interest in the circuit is located with the IR microscope. For optimum image collection, the optical beam needs to be at 90 degrees to the sample surface. However, this is also the required angle of incidence for the ion beam, and thus the system was designed with the IR microscope off-axis from the ion beam. The position of the sample is translated back and forth between the FIB and IR microscope with a high degree of accuracy (0.25 μm) by using the system's laser interferometer stage. Once registration between the FIB and optical images is established, the area(s) to be milled are defined in the IR mode. The system is then returned to FIB mode, the milling parameters are established, and controlled removal of the bulk silicon begins.

Results

The optical microscope identified areas of interest, which have a high density of M1 lines and M1 to M2 vias. A backside IR image of one such area is shown in Fig. 2. Backside IR images of the same area are shown in Fig. 3 after the removal of about half of the Si (70 μm remains) and in Fig. 4 following complete removal of the silicon substrate.
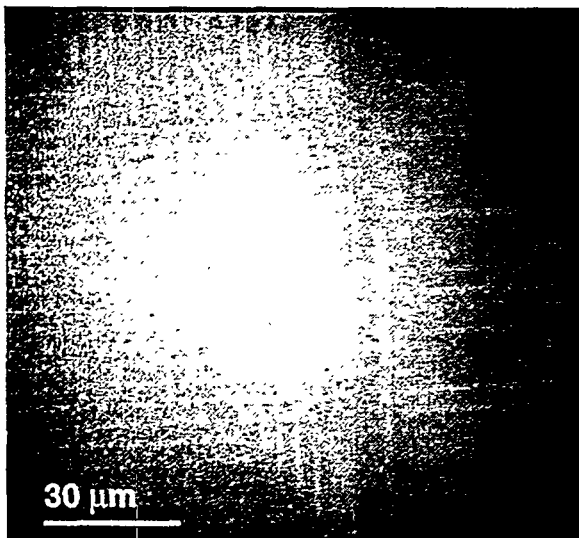

Fig. 2. A portion of the IC imaged through the backside of the chip. The Si substrate is approximately 150 μm thick.

Typical rates of removal have been calibrated for specific milling conditions (e.g., beam current density, XeF_2 pressure, etc.) and, using the calibrated values, the ion dose necessary for complete removal of the Si was estimated. The actual dose required to completely remove the Si varied with the remaining Si thickness, and was approximately $0.25 - 0.3$ $nC/\mu m^2$ for samples with $75 - 100$ μm remaining silicon. This is consistent

with the expected acceleration of about 1000x for super-enhanced FIB/XeF_2. During FIB processing, a visual endpoint frame was used to determine when the Si had been completely removed from the backside of the sample. The endpoint frame was monitored until the entire area was completely clear of Si, and then the FIB/XeF_2 milling was stopped. Because the acceleration of Si removal by FIB/XeF_2 is about 100x greater than the removal of SiO_2, very little loss of planarity of the surface is introduced by the fact that the milled area has sloped edges that clear last during milling.
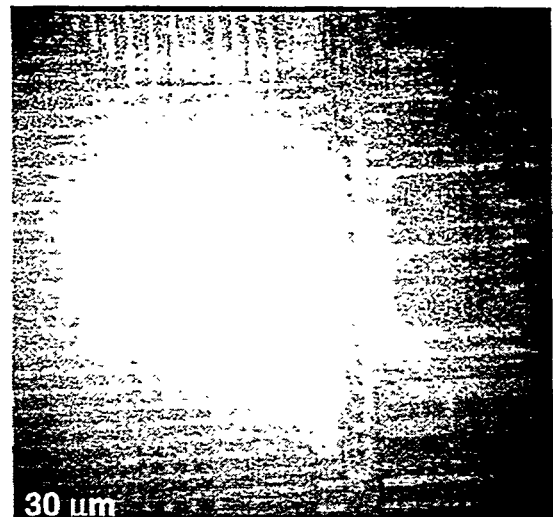

Fig. 3. IR image through the chip backside following partial removal of the Si substrate. The remaining Si is approximately 70 μm thick.
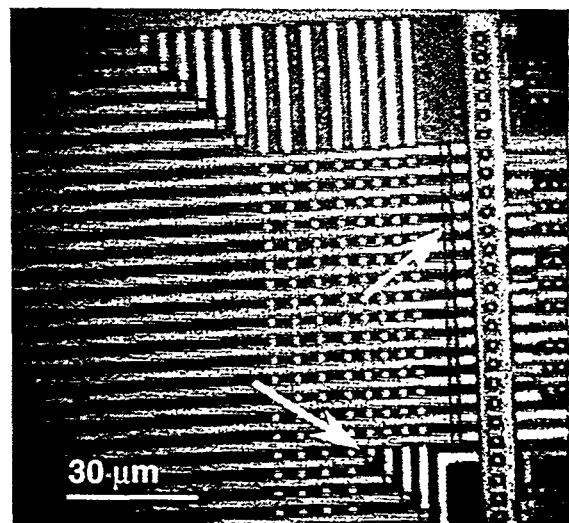

Fig. 4. IR image of the chip backside following complete removal of the Si substrate. The M1 lines are horizontal and M2 lines are vertical. Representative M1 to M2 vias are indicated by arrows.
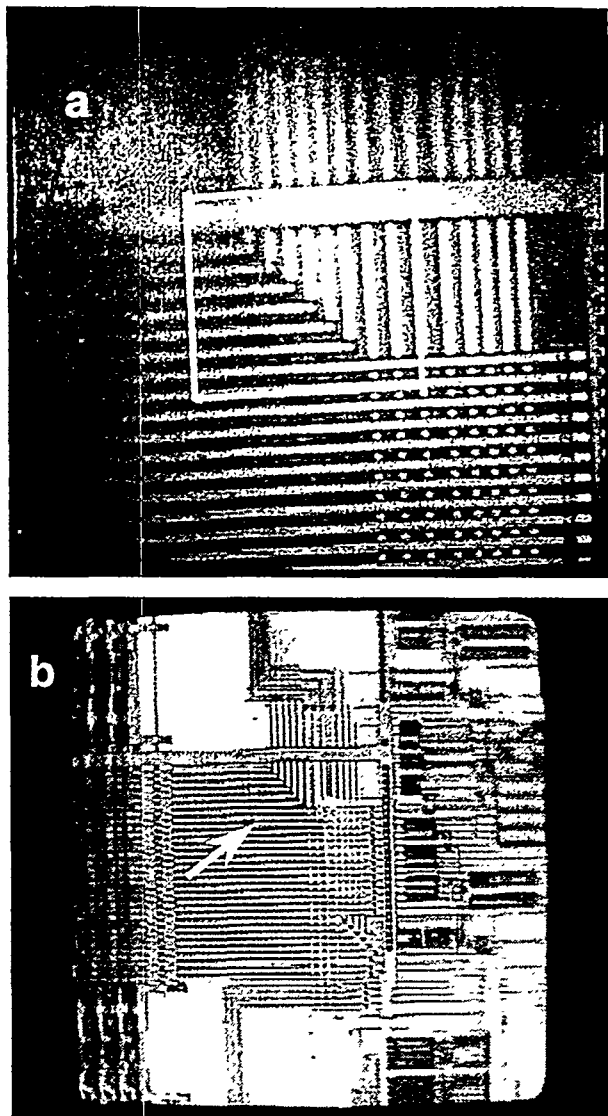
Fig. 5 a. IR image of an area to be marked, with the mill box area defined. b. optical micrograph of backside-thinned sample. The area of interest has been marked (arrow) by straight sputter milling.

After super-enhanced FIB/XeF$_2$ milling had removed the Si substrate, additional FIB milling was performed in a conventional FIB system. The change of FIB systems was for logistics reasons only; conventional FIB milling can also be performed in the flip-chip FIB. In fact, before removing the samples from the flip-chip FIB system, straight sputter milling was used to mark the areas of interest so that they could be easily located in our conventional FIB system which lacks an IR imaging capability. Shallow trenches (about 0.125 μm deep) were milled to mark these areas. Fig. 5a is a backside IR image showing the definition of the mill box. Fig. 5b is an optical micrograph showing the entire thinned area (350 μm x 350 μm) as well as the marked region, indicated by an arrow. Optical images such as Fig. 5b. are used to assist with navigation on the samples in the conventional FIB system.

Figure 6 shows a "cartoon" cross section of the samples used for this study. The cross section shows the presence of polysilicon "pedestals" beneath the M1 to M2 vias. In many flip-chip FIB applications, "normal" XeF$_2$ gas assisted milling would be used to accelerate the removal of the SiO$_2$-based inter-level dielectric (ILD) while performing FIB-milling to reach a node of interest in a circuit repair application [5,6]. However, our objective was to keep the sample surface as flat as possible so that the M1 lines would be exposed uniformly without overetching or undercutting. Because the selectivity of XeF$_2$ is higher for polysilicon than for SiO$_2$, the polysilicon pedestals (0.5 μm thick) would be removed much more quickly than the surrounding ILD if "normal" FIB/XeF$_2$ were used, leading to the formation of depressions in the sample surface. During subsequent milling, the backside of M1 would not be exposed uniformly, but instead the backside of the vias would be reached first, and the metal would be undercut in those regions by the time the rest of the M1 backside was exposed. On the other hand, the via regions actually sit slightly further away from the backside of the sample than the surrounding M1, as shown in Fig. 6. With straight sputter milling, the backside of M1 in via regions will be exposed last, but the deviation in surface flatness will be less than if the FIB/XeF$_2$ approach is used. For these reasons, straight-sputter milling was used to remove the layers once the Si substrate had been removed even though this is a much slower process than "normal" XeF$_2$-assisted milling.

Conventional FIB milling was performed in a Micrion 9000 (25 nm/30 keV column) to remove the ILD and expose M1 from the backside. The approximate milling dose required for material removal was calculated from the known layer thicknesses. A visual endpoint frame was continuously monitored, and the milling dose adjusted as needed. An ion dose of ~ 4.75 nC/μm^2 was used to remove the ILD and polysilicon pedestals, exposing the backside of M1. As the M1 layer was approached, the milling process was interrupted frequently (every 0.1 μm or so). Once the M1 lines were exposed, milling was performed in increments of 0.025 – 0.05 μm until the TiW was removed. Between mills, a high resolution secondary electron mode FIB (SEFIB) image was acquired to monitor removal of the TiW more closely. Figure 7 is one such image showing the early stages of TiW layer removal. The etch rate of the TiW appears to vary with grain orientation, leading to roughening of the layer as it is removed and thus to a "speckled" appearance. The TiW at the ends of the lines has not yet been appreciably etched, and thus exhibits more uniform contrast than the lines themselves.
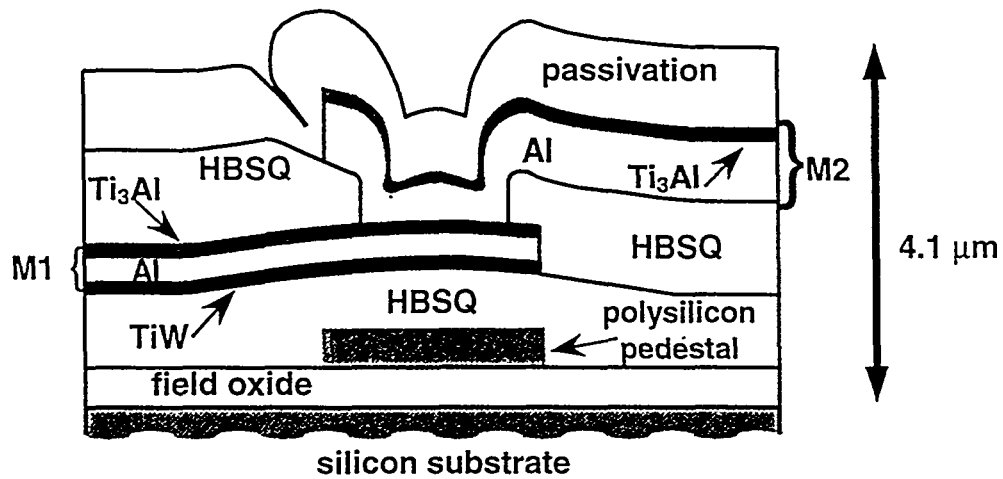
Fig. 6 Cartoon cross section of M1 to M2 via in material used for this study. The M1 and M2 lines are parallel to each other, and run left to right in this field of view.
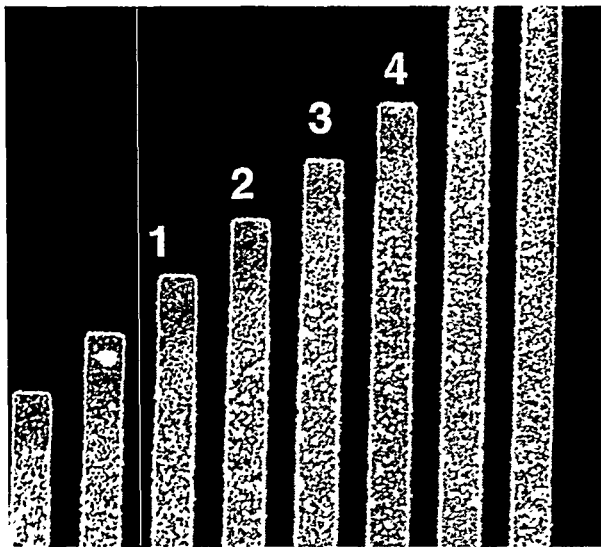

Fig. 7. Secondary electron mode image showing the backside of several of M1 lines. A moderate amount of the TiW underlayer remains (areas of dark contrast along the lines and at the ends).

The die was removed from the FIB and examined in the field emission SEM (FESEM) at several stages during removal of the TiW layer. Fig. 8 shows 3 keV FESEM images of these lines with increasing amounts of TiW removal. The TiW layer has bright contrast in the FESEM images compared with darker contrast in the SEFIB image (Fig 7). Voids are visible at the ends of several of the M1 lines, which correspond to the location of M1 to M2 vias. It should be noted that the large, circular holes in M1 are not voids, but are pitting that likely resulted from residual polishing debris that remained on the surface during backside milling.
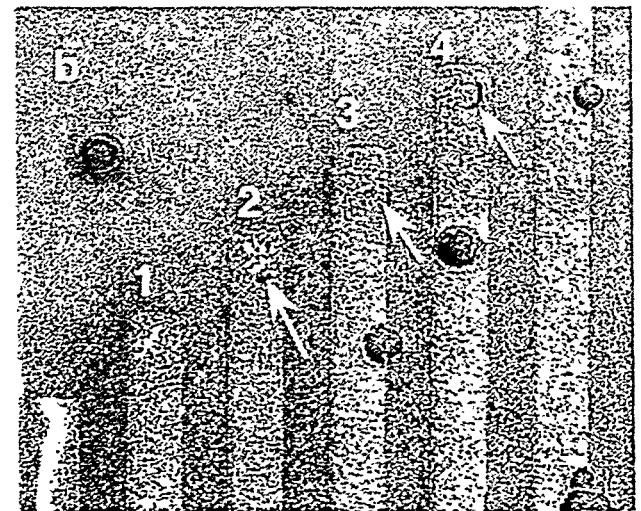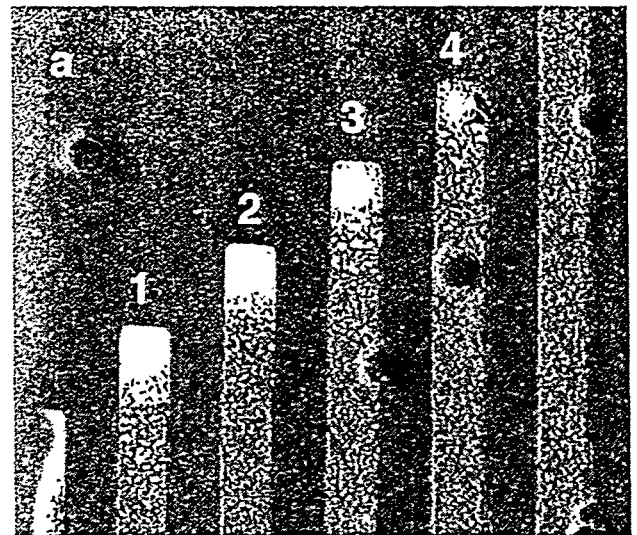

Fig. 8 3 keV FESEM images of several M1 lines. In (a) the via regions are mostly covered by TiW (bright contrast). In (b), the TiW has been removed almost completely and voiding is visible (arrows).
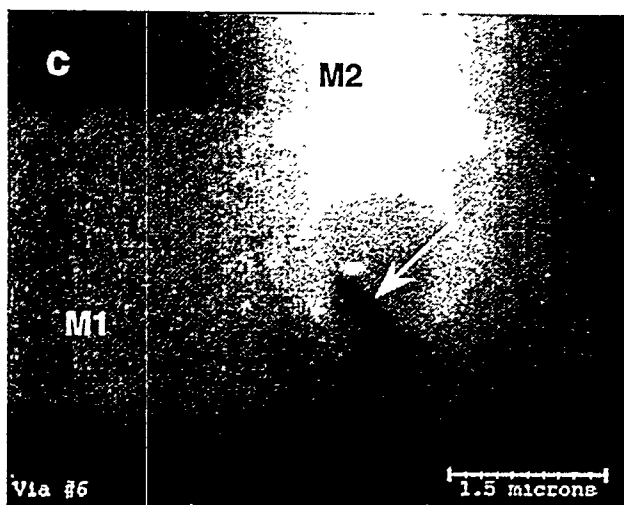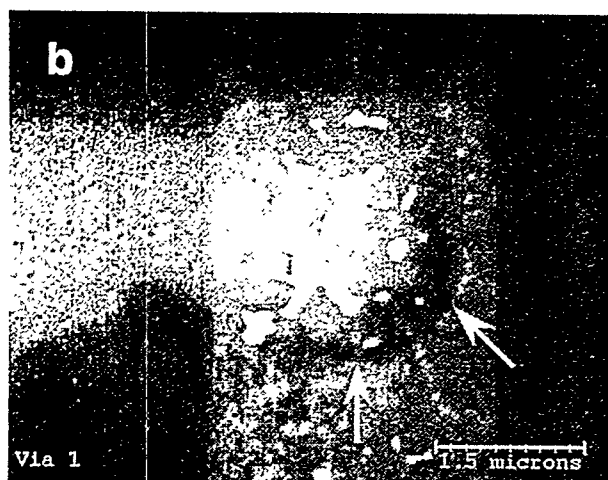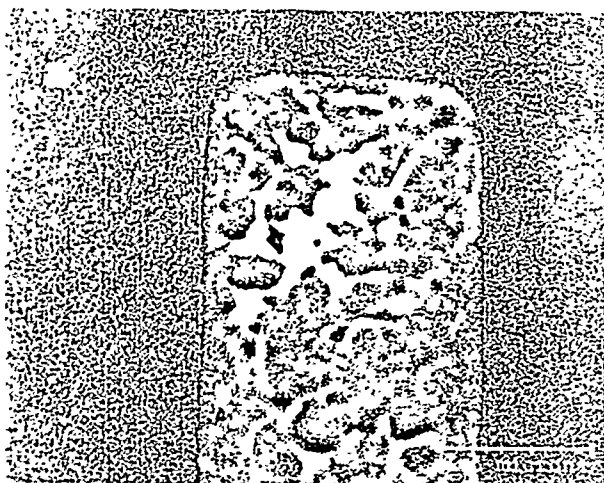
images show a higher magnification view of the M1 via labeled "1" in Fig. 8. Fig. 9a is an FESEM image taken at 3 keV, which shows the surface structure of the line; no voiding is visible. Fig. 9b is a 30 keV BSE image of the same location, clearly showing the presence of subsurface voiding. The subsurface void in Fig. 9b has the same crescent shape as the void that intersects the sample surface in the M1 line labeled "4" in Fig 8. The crescent-shaped morphology suggests that these voids lie along the perimeter of the circular via; the images of voids in Vias 1 and 4 (Figs. 8 and 9) together suggest that the voiding may occur in both M1 and the via. Fig. 9c is an image of a void that extends into the via; this void is thought to be a stress void.

In addition to revealing voids in vias, BSE imaging also permits viewing voids in M1 and M2. Figure 10a shows both a number of voids along the edges of the M2 lines and that no appreciable voiding is observed in M1 in this field of view. Figure 10b is the identical field of view, imaged from the front side of the die. The mirror image of the BSE front side image is shown here so that the field of view exactly matches that from the back side. Voiding in the vias and M2 lines is much more visible in the backside images (Fig. 10a).

Fig. 9. Increased magnification FESEM images of Via 1. (a) shows a 3 keV image of the via area, with no voiding apparent. (b) is a 30 keV BSE image showing subsurface voiding (indicated by arrows). (c) is a stress void in the via.

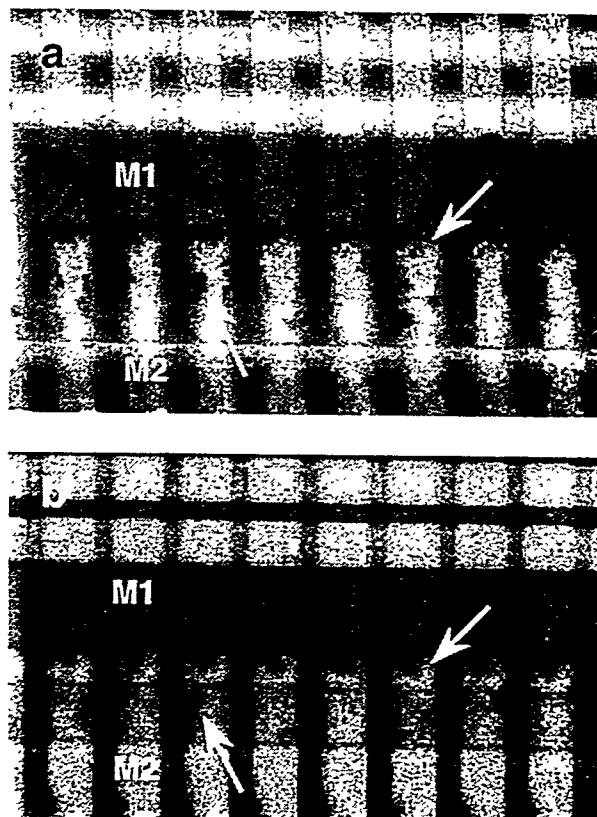The images shown in Figure 9 make clear that the voids in Fig. 8 are *not* an artifact of FIB milling. These

Fig. 10. 30 keV BSE images showing voiding in the vias and at the edges of the M2 lines. (a) is a BSE image from the backside of the die and (b) shows the same field of view from the frontside. The arrows indicate the same via and edge voids in each image.
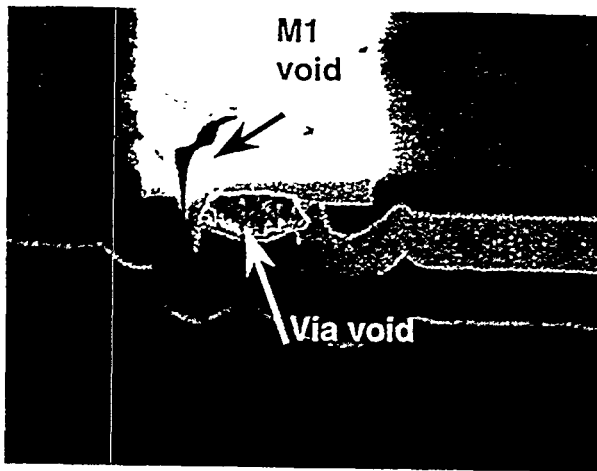
Fig. 11. Cross section through via 4 showing voiding in both M1 and M2.

We performed a series of FIB cross sections through several of the vias that exhibited crescent-shaped voids in M1. The following images of the cross sections are all secondary electron mode FIB images. Fig. 11 is a cross section through Via 4 (Fig. 8). This image shows voiding in both M1 (top surface) and M2 (on the face of the cross section), suggesting a possible connection between the two voids. Figs. 12 a – e are a series of images showing the sequential cross sectioning of another via associated with a crescent-shaped void in M1.
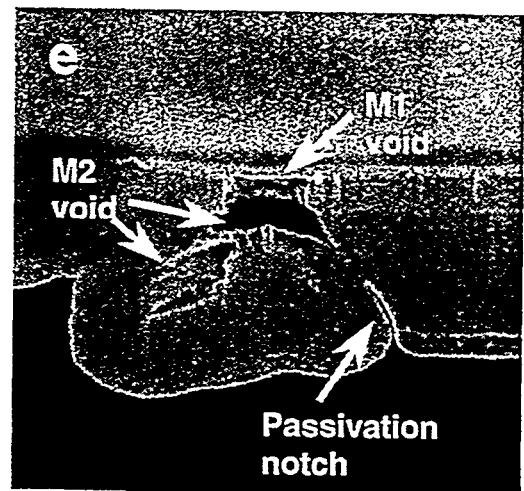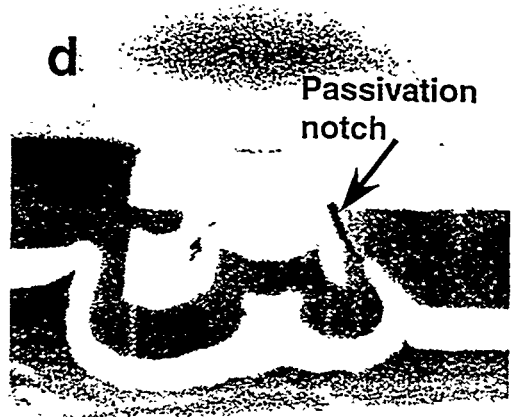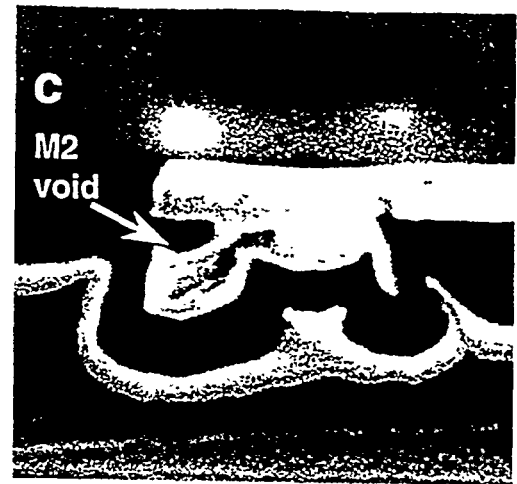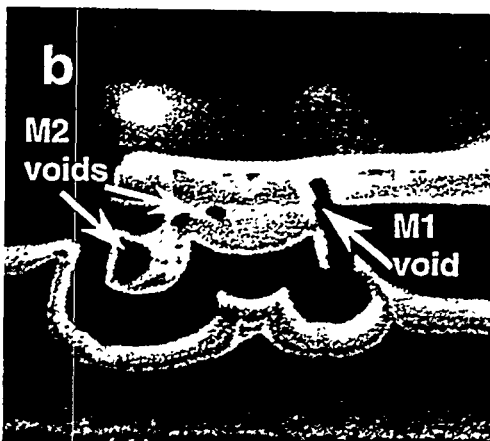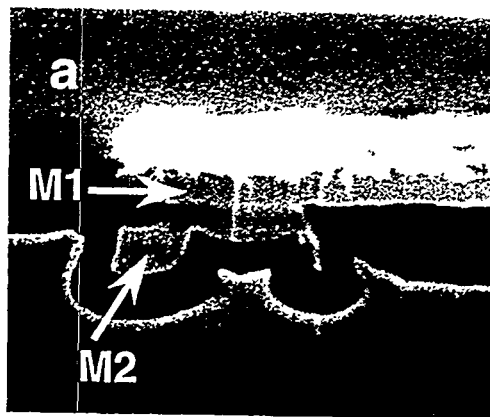

Fig 12. This series of 5 FIB images shows a series of cross sections through a voided via. (a) First cut, showing no voiding. (b) Second cut, showing voiding both in M1 and M2. (c) Third cut showing extensive M2 voiding. (d) Third cut, with image contrast adjusted to show that the M1 void is connected to the passivation surface. (e) Final cut, showing that voids in M1 and M2 are physically continuous. All are secondary electron mode FIB images; Figs. a – d were imaged with the 30 keV, 25 nm ion column, and Fig. e was imaged with a 50 keV, 5 nm column.

The cuts in Fig. 12 are made in a plane parallel to that of the cartoon cross section in Fig. 6. Fig. 12a was the first cut into the via, with no voiding apparent. Fig. 12b is the second cut, showing some voiding (dark areas) in M2 as well as a notch-shaped void in M1. The M1 void, in plan view, is what we refer to as a crescent-shaped void shown in Figs. 8 and 9. The third cut is shown in both Figs. 12c and d. Fig. 12c is a high contrast, low brightness image showing extensive M2 voiding. In Fig. 12d, the brightness was increased to show that the notch void in M1 is connected to the passivation surface via a notch in the passivation caused by a "breadloafing" processing defect. The final cut, shown in Fig. 12e, indicates that the voids in M2 and M1 are physically connected. This suggests that the void may have nucleated in one metal level and subsequently grew to include both metal levels.
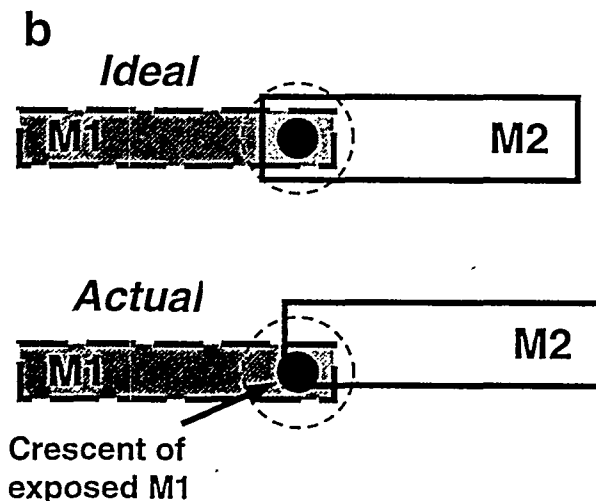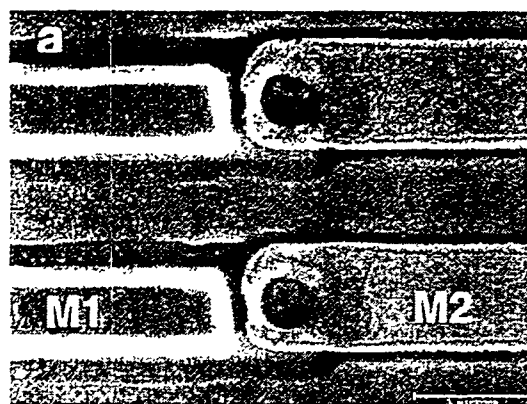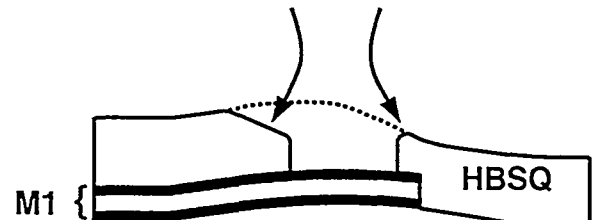
In addition to the voiding shown in Figs. 8 - 12, we observed significant misalignment between M1 and M2 in this material. Fig. 13 shows the misalignment of M2 relative to M1 in both an FESEM image (Fig. 13a) and in a cartoon representation (Fig 13b). In this field of view, M2 is displaced to the right and upward relative to its intended location.

Fig. 13 FESEM image of M1 to M2 vias. (a) 5 keV FESEM image showning the misalignment between M1 and M2. M1 is covered with a bias-sputtered quartz interlevel dielectric. The M2 lines are not passivated. (b) Cartoon depicting the intended and actual alignment of M1 and M2. M2 is displaced upward and to the right relative to where it should be.
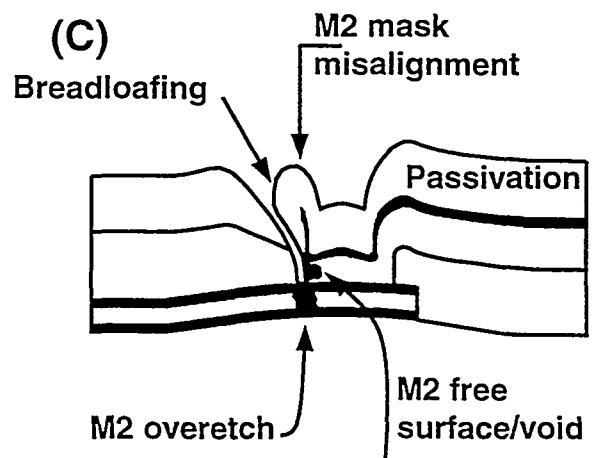

Fig. 14. Illustration of processing defects leading to M1 and M2 voiding. (a) shows the shallow taper of the M1 to M2 via hole etch. (b) shows the intended M2 patterning. (c) shows the effects of M2 misalignment, overetching of M2, and passivation breadloafing on the structure of this via.

Discussion

Combining the 3-dimensional understanding of the void morphology derived from the information in Figs. 5 – 12 with the known M2 misalignment (Fig. 13) led to the following understanding of the voiding process in this technology. Fig. 14 illustrates the backend process steps, showing how the M2 misalignment leads to the observed voiding. Fig. 14a shows the shallow taper of the via hole etched through the high bias-sputtered quartz (HBSQ) interlevel dielectric. Fig. 14b shows the blanket M2 film deposited and also indicates where the end of the M2 interconnect is intended to be. Referring to the previous figure, Fig. 13b showed a top view of the misalignment of M2 to the via hole and to M1 after M2 patterning and etching. Fig. 14c shows that misalignment causes the M2 edge (and, one can imagine, the side of the M2 line) to coincide with the via hole. When M2 was overetched in this instance, the etch cleared the M2 out of the via in a crescent shape and proceeded to attack M1 as well. Because of the shallow taper of the via hole, the severe topography of the M2 sidewall, and the deposition characteristics of the passivation, the passivation layer does not completely seal the M2, leaving exposed free surfaces which can act as sources of vacancies for the formation of stress voids in M1 and the M2 vias. The fairly "clean" crescent-shaped voids in Fig. 8b are caused by the M2 etch. The irregularly-shaped voids in M2 in Figs 11 and 12 were determined by other analytical work (not reported here) to be stress voids. Thus, the M2 misalignment and concomitant etch defect create the nucleation point for the larger stress void network that forms in M2. The voids noted at the edges of M2 (Fig. 10) are also stress voids that nucleated from metal sidewall etch defects.

Conclusions

Conventional BSE SEM imaging of the front side of an IC can detect voids in the top metal layer with somewhat limited spatial resolution. Severe topography, materials, and the depth of the layer of interest can prevent the clear detection and characterization of voids in vias and buried metal layers. We have demonstrated that backside thinning in a FIB system can be combined with conventional FIB milling to enable the inspection of voiding at lower lying metallization layers. In particular, we used backside thinning to remove the TiW underlayer from M1 that prevented successful front-side detection of voids with BSE imaging in a SEM. This sample preparation approach allowed us to view the voiding in many vias at once and was crucial in developing an accurate model of how voiding occurred in the vias on this material. BSE imaging from the backside yielded sharper images of voids than is possible from the front side because the amount of material between the void and the surface is reduced and because the backside preparation eliminates surface roughness. Backside FIB techniques can be used to expose large areas on a chip; in this study, we used backside FIB processes to remove the silicon substrate from areas up to 350 μm x 350 μm in size. This planar approach permits inspection of a large number of lines and vias relatively quickly and is therefore much more time-effective than performing cross-sections on a number of individual vias.

Acknowledgments

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