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Focused Ion Beam Induced Effects on MOS Transistor Parameters

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Abstract

We report on recent studies of the effects of 50 keV focused ion beam (FIB) exposure on MOS transistors. We demonstrate that the changes in value of transistor parameters (such as threshold voltage, V_t) are essentially the same for exposure to a Ga^+ ion beam at 30 and 50 keV under the same exposure conditions. We characterize the effects of FIB exposure on test transistors fabricated in both 0.5 μm and 0.225 μm technologies from two different vendors. We report on the effectiveness of overlying metal layers in screening MOS transistors from FIB-induced damage and examine the importance of ion dose rate and the physical dimensions of the exposed area.

Introduction

Focused ion beam (FIB) technology has become increasingly important for performing circuit modifications in support of the design verification phase of IC manufacturing. The successful use of FIB technology for these applications significantly reduces the development costs and time-to-market of new products. Because of the importance of these tools in both design verification and failure analysis applications there has been growing interest in understanding the possible side effects of FIB exposure on ICs.

Two recent studies have systematically investigated the effects of FIB exposure at the transistor level to understand the basic phenomena and likely damage mechanisms [1,2]. Both Campbell et al. (1997) [1] and Benbrik et al. (1998) [2] investigated the effects of 30 keV Ga^+ exposure on MOS transistors for submicron and older technologies. Both studies showed that transistor parameters, such as threshold voltage (V_t) and transconductance (g_m), change in response to FIB exposure. Both studies also found that the magnitude of transistor parameter changes increases with higher ion dose and smaller gate areas for a given technology.

Campbell et al. showed that FIB-induced changes in transistor parameters were bake-recoverable and that they could be prevented by the use of electron flood charge neutralization [1]. Also, they found that the observed changes in transfer characteristics were consistent with the development of oxide- and interface-trapped charge as a result of FIB exposure. These defects were likely caused by sample charging, but the possibility of ionizing radiation-induced defects was not ruled out.

Benbrik et al. studied the effects of FIB exposure on CMOS inverters, diodes, and bipolar devices in addition to MOS transistors [2]. They found that MOS technologies are less sensitive to FIB-induced degradation than bipolar technologies, and concluded that input protection structures play an important role in protecting MOS ICs. They also suggested that overlying metal signal and power lines may protect active regions. These authors related the transistor-level damage to sample charging during FIB exposure.

Ion columns with reduced spot size (~5 nm) and increased operating voltage (50 keV) are now commercially available. A primary purpose of this study is to examine the effects of FIB exposure at 50 keV and compare them with the results of exposure at 30 keV. In addition, we describe several other experiments aimed at obtaining a better understanding of the degradation mechanisms involved. One set of experiments examines the dose rate dependence of FIB-induced damage and another evaluates the effectiveness of overlying metallization layers in screening MOS transistors during FIB exposure.

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Experimental Approach

MOS transistors fabricated from different technologies were used as the test vehicles for evaluating the effects of FIB exposure. The transistors were characterized electrically by measuring the transfer characteristic (drain current, I_d, vs. gate voltage, V_g) both prior to and following FIB exposure. The changes in transistor parameters, such as threshold voltage, V_t, and/or transconductance, g_m, were used to monitor the effect of FIB exposure on the MOS transistors. In general, a different transistor was used for each data point.

The technologies studied in this work included two 0.5 µm CMOS technologies from an R&D class wafer fab and an industrial 0.225 µm CMOS technology. The details of these technologies and the transistor geometries used in these experiments are shown in Table 1. The dimensions "0.5 µm" and "0.225 µm" are the minimum as-drawn feature sizes and will be used generically to refer to these technologies. However, the actual sizes of the transistors used in a given experiment may vary.

Both *n*- and *p*-channel transistors of several geometries were exposed to the FIB with ion doses ranging from ~10^{-4} nC/µm^2 to ~10^{-2} nC/µm^2. Ion exposures in this range are representative of the ion doses that result from image acquisition during navigation to an area of interest.. As a general rule of thumb, a dose of 4 nC/µm^2 removes approximately one micrometer of typical IC materials such as Al, Si, and SiO_2.

Two different FIB systems were used for the ion exposure experiments. A Micrion 9000 FIB system with 25 nm minimum spot size was used for FIB exposure at 30 keV. The 50 keV exposures were performed in a Micrion 9500 system with 5 nm minimum spot size. Exposure of the MOS transistors was performed with the electron floodgun both active and disabled. The floodgun directs a low energy (~ 80 eV) spray of electrons at the sample surface to counter the charging effects of Ga^+ ions. Except where indicated, all experiments were performed at the wafer level with the substrate grounded through the sample stage.

Blind navigation was used as far as possible to position the transistor of interest under the ion beam without delivering an imaging dose to other areas on the test chip. Navigation to the transistor of interest was accomplished by moving a known distance from a reference point on the die. Navigation between dice was accomplished by using the FIB system's wafer map function. The ion dose was delivered to the sample surface above the test transistor. As shown in Fig. 1, the exposed area was somewhat larger than the transistor itself. Figure 1 is an optical photomicrograph of one of the 0.5 µm technology transistors with a 70 µm x 70 µm FIB-exposed area indicated by the box. A square or rectangular region ranging from 40 µm x 40 µm to 100 µm x 100 µm in size (depending on the experiment) was used for the FIB exposures.

The desired dose per unit area was achieved either by using the FIB system's milling function or by "grabbing" one or more single-frame images of the area of interest. The milling parameters (pixel spacing and pixel dwell time) were adjusted to match those used in grabbing single-frame images. The intent of the experiment is to simulate the exposure that occurs during "grabbing" images in the FIB system while navigating to an area of interest.

Table 1
Summary of Test Transistor Technologies

Technology	Minimum L_{eff}	Metallurgy	t_{ox}	Isolation	Passivation	Transistor Geometry
0.5 µm	0.5 µm	Planarized, 3-level aluminum with W plugs	12 nm	LOCOS	1.2 µm phospho-silicate glass	W = 20 µm L = 0.5, 0.6, 0.75, and 1.0 µm
0.5 µm	0.5 µm	Planarized, 3-level aluminum with W plugs	12 nm	Shallow trench isolation	1.2 µm phospho-silicate glass	W = 20 µm L = 0.5, 0.6, 0.75, and 1.0 µm
0.225 µm	n-channel: 0.12 +/- 0.04 µm p-channel: 0.14 +/- 0.04 µm	Planarized, 6-level copper	3.5 nm	Shallow trench isolation	0.4 µm Si_3N_4 over 0.45 µm SiO_2	W = 9 µm L = 0.225 µm

The ion dose delivered in a single-frame image, D_o, is calculated from the expression $D_o = [(I_b)(t_d)/X_pY_p)]$, where I_b is the beam current in nA, t_d is the time (in seconds) that the ion beam dwells at each pixel, and X_p and Y_p are the pixel spacings in the x- and y-directions. In most experiments, the beam parameters used were t_d = 16 µs, X_p and Y_p = 0.195 µm, and I_b = 660 pA. The pixel spacing corresponds to a 512 x 512 pixel image of an area 100 µm x 100 µm in size, or to a 256 x 256 image of a 50 µm x 50 µm area. Under these beam conditions, each raster scan delivers an ion dose of about 2.7 x 10^{-4} nC/µm^2 and removes less than a monolayer of material from the sample surface.

A set of experiments was conducted to compare the FIB effects resulting from "default" milling parameters and the "image frame grab" parameters. The I_b for these experiments was 1.7 nA. The parameters used for the "image frame grab" mills were X_p and Y_p = 0.39 µm and t_d = 1 µs, and those used for the "default" mills were X_p and Y_p = 0.02 µm, and t_d = 5 µs. With these beam parameters, the dose delivered per raster in the "default" mill is almost 1800 times greater than by the "image frame grab" mill. The total number of rasters delivered at a given dose for the "default" mill is proportionally smaller. The total process time to deliver a given dose is the *same* for the two process types, and therefore the overall dose rate (total dose/time) is the same. However, the *instantaneous dose rate* increases for longer pixel dwell time and smaller pixel spacing, and is therefore considerably higher for the "default" milling condition.

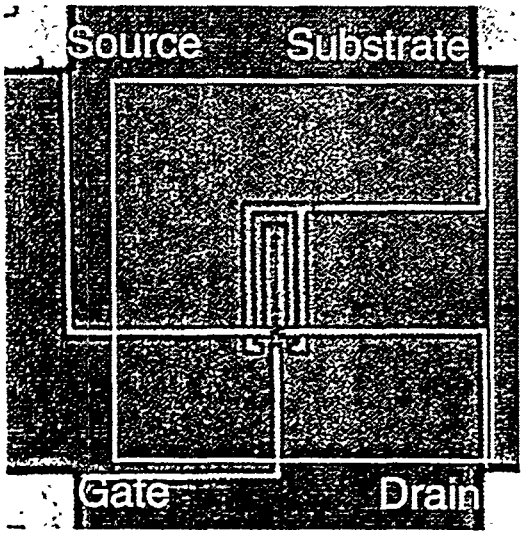

Fig. 1 Optical image showing the FIB-irradiated region (indicated by the white box) around a 20 x 0.6 µm *n*-channel transistor. The bond pads are visible at the corners of the image.

We developed a special test structure to evaluate the effectiveness of an overlying metal structure in shielding a transistor from FIB-induced parameter shifts. The test structure is implemented in the 0.5 µm CMOS technology with LOCOS isolation and consists of unmodified n- and p-channel transistors as well as transistors with a metal pad completely covering the gate and active regions. A photomicrograph of one of the special transistors is shown in Fig. 2. All of the interconnections to these transistors occur at the M1 level. The metal shield is implemented at either M2 or M3 for a given transistor and is connected to the substrate (ground potential in our experiments). The area exposed by the FIB was 60 µm x 60 µm and was centered on the 75 µm x 75 µm shield.

Finally, we used scanning force microscopy (SFM) to investigate the effects of FIB exposure on the sample surface. Both topology and surface potential imaging were used in our study. This work was performed in a modified Digital Instruments Dimension 3000 system.

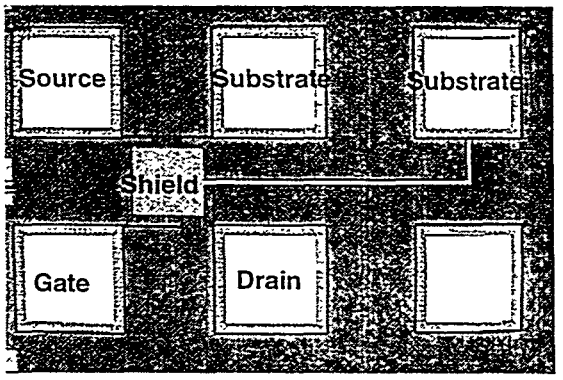

Fig. 2 Optical image showing a test transistor with a shielding pad. The shield is tied to the substrate, which is at ground potential in our experiments.

Experimental Results

Comparison of 30 and 50 keV Exposure

The effects of FIB exposure at 30 and 50 keV were were studied for the 0.5 µm CMOS technology fabricated with LOCOS isolation. The area exposed by the ion beam was 100 µm x 100 µm, completely covering the transistor as well as some of the metal interconnections to the device terminals (see Fig. 1). The ion beam parameters were adjusted so that I_b = 660 pA at the two ion energies. The only difference between the test conditions at 30 and 50 keV was the larger spot size at 30 keV. The other beam parameters were the same for both sets of experiments. The ion doses were 2.7 x 10^{-4}, 5.4 x 10^{-4}, and 2.7 x 10^{-3} nC/µm^2, corresponding to 1, 10, and 20 individual "frame grabs".

Individual I_d vs. V_g curves were collected for each of the transistors. An example of these data is given in Figure 3 for an n-channel, 20 x 0.6 μm transistor which received an ion dose of 5.4 x 10^{-3} nC/μm^2. As before [1], we found a general trend toward larger parameter shifts at smaller transistor geometry; for simplicity, we show results for just one geometry. The results for 20 x 0.6 μm n- and p-channel transistors are shown in Figs. 4 and 5. The changes in V_t (ΔV_t = V_t post-FIB *minus* V_t pre-FIB) as a function of ion dose are fairly comparable for ion beam exposure at 30 and 50 keV. In general, the magnitude of ΔV_t is greater for n-channel than for p-channel transistors in this technology. Our results show that electron flood charge neutralization is highly effective in minimizing transistor parameter shifts at both 30 and 50 keV, consistent with our previous findings for 30 keV ion exposure for this material [1].

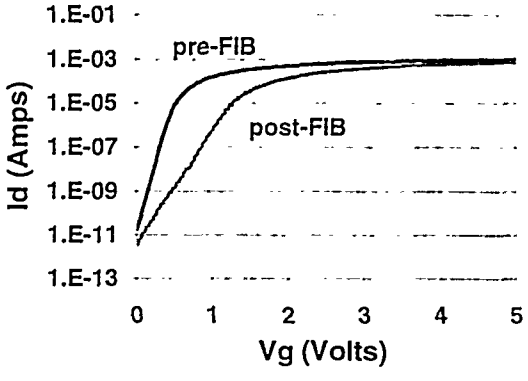

Fig. 3. Pre- and post-FIB Id vs. Vg curves for an n-channel, 20 x 0.6 mm transistor which received an ion dose of 5.4 x 10^{-3} nC/μm^2.

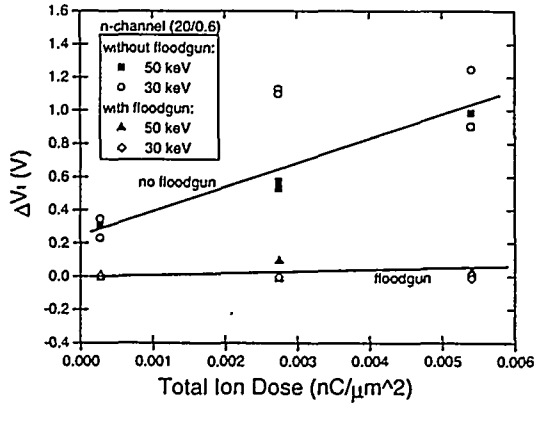

Fig. 4. ΔV_t as a function of ion dose for 20 x 0.6 μm n-channel transistors at 30 and 50 keV FIB exposure, with and without electron flood charge neutralization. The measurement error is ~ 0.003 V.

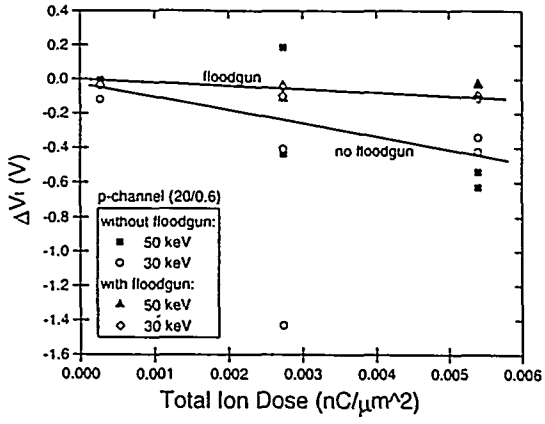

Fig. 5. Changes in V_t as a function of ion dose for 30 and 50 keV FIB exposure of 20 x 0.6 μm p-channel transistors, with and without electron flood charge neutralization. The measurement error is ~ 0.003 V.

We also measured the effects of 50 keV FIB exposure on 20 x 0.6 μm MOS transistors fabricated with shallow trench isolation (STI). The beam conditions were identical to those used for the LOCOS material, and the results were very similar. The 50 keV results for both LOCOS and STI n-channel, 20 x 0.6 μm transistors exposed without electron flood charge neutralization are plotted in Figure 6.

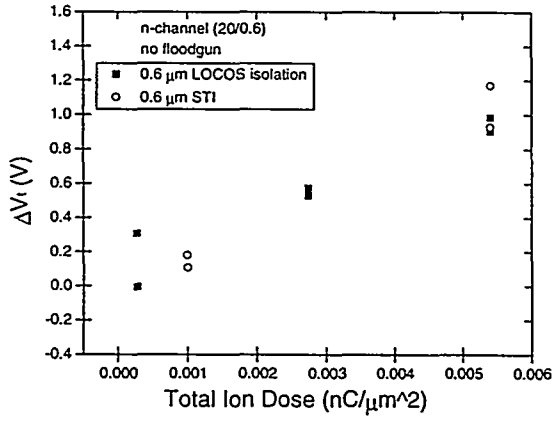

Fig. 6. ΔV_t as a function of ion dose for 20 x 0.6 μm n-channel transistors fabricated with both LOCOS and STI. FIB exposure was performed at 50 keV without charge neutralization. The measurement error is ~ 0.003 V.

Effects of FIB Exposure on 0.225 μm Technology

The effects of 50 keV ion beam exposure on test transistors fabricated in a 0.225 μm CMOS technology were also characterized. The results of exposure of 9 x

0.225 μm n- and p-channel transistors without charge neutralization are given in Figs. 7 and 8. The difference in vertical scale between these figures (mV) and Figs. 4 – 6 (V) should be noted. These results show no increase or decrease in the magnitude of ΔV_t with increasing dose for the 0.225 μm transistors, in contrast to the monotonic increase with dose observed for the 0.5 μm CMOS n- and p-channel transistors. Furthermore, the magnitude of ΔV_t is at least two orders of magnitude smaller than that observed for the 0.5 μm transistors.

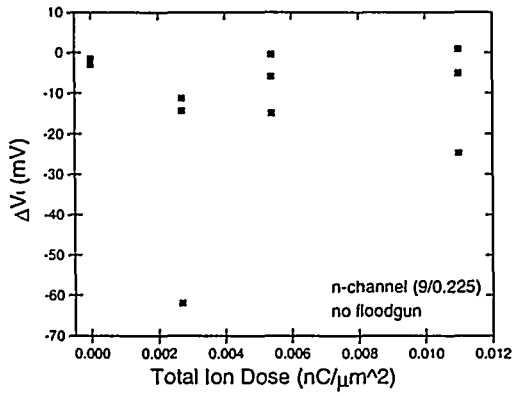

Fig. 7. Shifts in V_t as a function of ion dose for 9 x 0.225 μm n-channel transistors. Ion exposure was at 50 keV without charge neutralization. The measurement error is ~ 3 mV.

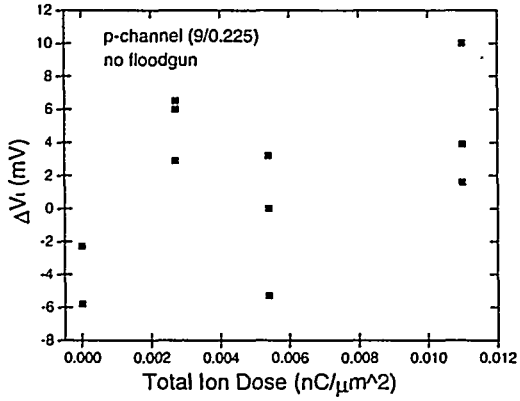

Fig. 8. Shifts in V_t as a function of ion dose for 9 x 0.225 μm p-channel transistors. Ion exposure was at 50 keV without charge neutralization. The measurement error is ~ 3 mV.

We also measured the effects of FIB exposure on another set of 0.225 μm n-channel test transistors that do not have protection diodes but do have a common gate. For exposure with an ion dose of 5.4 x 10^{-3} nC/μm^2 without electron flood charge neutralization, we observed ΔV_t values of approximately –0.12 V for the smallest transistor geometry (0.35 x 0.25 μm), and much smaller values (-0.02 V) for 10 x 10 μm transistors. These ΔV_t results show similar dose-dependence but are still at least an order of magnitude smaller than those observed for the unprotected n-channel 0.5 μm technology transistors (Figs. 4, 6). However, a direct comparison of the results of FIB exposure on these two technologies is not appropriate because of the many differences (e.g., design, processing, oxide thickness, and levels of integration) between them.

Effects of Shielding on Transistor Parameter Shifts

The results of FIB exposures performed on shielded 20 x 0.6 μm n-channel transistors are given in Table 2.

Table 2
Effect of Shielding on n-channel Transistors
Ion Dose = 0.011 nC/μm^2

Transistor Type	Charge Neutralization	ΔV_t (V)
No shield	No	-0.4
M2 shield	No	0.049
M3 shield	No	0.065
No Shield	Yes	0.0
M2 Shield	Yes	-0.003
M3 Shield	Yes	0.006

FIB exposure was performed at 50 keV with a dose of 0.011 nC/μm^2 both with and without electron flood charge neutralization. The data clearly show that the grounded shielding plate significantly reduced the magnitude of the parameter shifts even when charge neutralization was not used. For example, a substantial ΔV_t (about 0.4 V) was observed for n-channel transistors when no shielding pad was present. With an M2 or M3 shielding pad, ΔV_t *is* 0.04 – 0.06 V. The use of electron flood charge neutralization further reduced the magnitude of ΔV_t to 0 – 0.005 V for the n-channel transistors with or without the shielding pads.

Dependence of FIB Effects on Dose Rate

A set of experiments was performed to compare the results of the "image frame grab" and "default" mills described in the Experimental Approach section. Both n- and p-channel, 0.5 μm technology transistors fabricated with the LOCOS process were exposed to an ion dose of 0.02 nC/μm^2 at 30 keV without electron flood charge neutralization. The results of this experiment are given in Table 3. Each table entry is the average of two measurements. The magnitude of ΔV_t

for the n-channel transistors is about 35% larger for the higher instantaneous dose rate ("default" mill), but is about 25% lower for the p-channel transistors. The measured ΔV_t values were comparable at the two dose rates when the floodgun was used. In our previous study [1], ion exposure was performed entirely in the "image frame grab" mode. The dose rate was varied in one experiment by changing the ion beam current. In that case, the variation in transistor parameter shifts with dose rate for the same total dose were small [1].

Table 3
Effect of Instantaneous Ion Dose Rate
Ion Dose = 0.02 nC/μm²

Transistor type	W/L	ΔV_t (V) Default Mill	ΔV_t (V) Image Grab Mill
n-channel	20/0.5	1.35 ± 0.02	0.99 ± 0.002
n-channel	20/0.6	1.38 ± 0.03	1.07 ± 0.02
p-channel	20/0.5	-.48 ± 0.03	-0.68 ± 0.04
p-channel	20/0.6	-.49 ± 0.02	-0.72 ± 0.03

Effect of Exposed Area

The effect of the size of the area exposed to the ion beam on the magnitude of ΔV_t was also examined. In this experiment, the same ion dose (10^{-2} nC/μm²) was delivered to two different sized regions (1600 μm² and 6400 μm²) above the test transistors. In other words, the transistors with 80 μm x 80 μm exposure received 4x the amount of Ga^+ ions as those with the smaller area exposure. Transistors built in the 0.5 μm technology with STI were used for these experiments, which were performed at 50 keV. Table 4 shows that the magnitude of ΔV_t increases with exposed area for transistors of two different gate lengths, and that the effect is more pronounced for the n-channel transistors. The data set in Table 4 is small, and thus additional experiments will be required for corroboration.

Table 4
Effect of Exposed Area on Parameter Shifts
Ion Dose = 0.01 nC/μm²

Transistor type	W/L	ΔV_t (V) 80 μm x 80 μm box	ΔV_t (V) 40μm x 40 μm box
n-channel	20/0.5	0.769	0.259
n-channel	20/0.6	0.598	0.307
p-channel	20/0.5	-0.313	-0.237
p-channel	20/0.6	-0.311	-0.191

Physical Evidence of Damage

Scanning force microscopy was used to examine the passivation surface above several 0.5 μm transistors following FIB exposure at 30 keV. Packaged transistors were used for these experiments but no electrical connections were made to the device terminals. Imaging of the surface topology was performed following FIB exposure to look for evidence of physical degradation, and surface potential imaging was use to look for residual surface charge. The same field of view (40 μm) is used for the results shown in Figures 8 – 10.

Fig. 8 shows both topology and surface potential images of the passivation surface above an n-channel transistor that received a large ion dose of 0.5 nC/μm² with electron flood charge neutralization. These images are featureless, indicating that the passivation surface is smooth and that no residual surface charging is apparent.

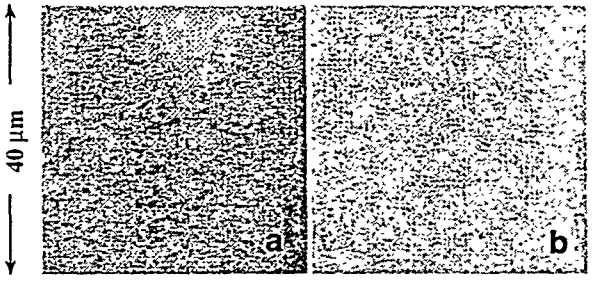

Fig. 8. (a) Topology and (b) surface potential images of a planarized *n*-channel transistor after a high-dose FIB exposure of 0.5 nC/μm² with electron flood charge neutralization.

The results were very different when charge neutralization was not used during milling. The topology image shown in Fig. 9a is of the FIB-exposed area of the passivation. The RMS roughness of this area is 1 – 2 nm, with the exception of a few areas that resemble small "bumps" with a height of 5 – 10 nm. These "bumps" were observed on the sample surface following an ion dose of 0.1 nC/μm² and were not visible with optical or SEM imaging. Fig. 9b shows that the variation in surface potential of this area is very small following the 0.1 nC/μm² dose exposure.

The same n-channel transistor received an additional 0.5 nC/μm² dose, again without charge neutralization. The additional FIB exposure apparently converted some of the "bumps" into "pits", as shown in Fig. 10a. In addition, residual charge was observed after the subsequent higher-dose exposure (Fig. 10b). The solid arrow in Fig. 10b indicates the area of greatest residual charge, which coincides with a "bump" visible in Fig.

10a (also indicated by a solid arrow). Four other areas with less residual charge are indicated by the dashed arrows in Fig. 10b. These areas coincide with "pit" location in Fig. 10b.. The occurrence of a large residual charge at one of the "bump" locations suggests that charge build-up occurs at these locations prior to an electrostatic discharge (ESD)-like event. Subsequent electrical measurements indicated the presence of a gate oxide short defect in this transistor.

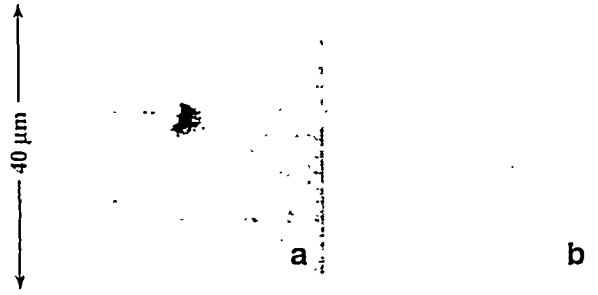

Fig. 9. (a) Topology and (b) surface potential images of a planarized *n*-channel transistor after FIB exposure of 0.1 nC/µm^2 without electron flood charge neutralization.

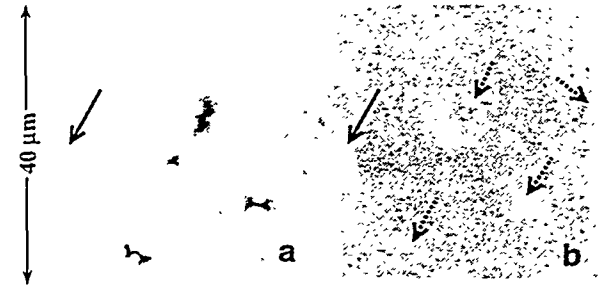

Fig. 10. (a) Topology and (b) surface potential images of the same planarized *n*-channel transistor in Fig. 9 after an additional FIB exposure of 0.5 nC/µm^2 without charge neutralization.

Discussion

We have measured the effects of 50 keV FIB exposure on two similar 0.5 µm CMOS technologies and on a 0.225 µm CMOS technology. The size of the parameter shifts (ΔV_t) obtained for the 0.225 µm technology are very different from those for the 0.5 µm technology, which is to be expected given the many differences between these technologies, including gate dielectric thickness, number of levels of integration (and hence thickness of the stack), protection diodes and common gates electrodes in the 0.225 µm technology transistors, and the materials used.

Our findings show that the amount of transistor degradation at a given ion dose (measured by threshold voltage shift) is comparable for 30 and 50 keV exposures with the same beam parameters for a given transistor technology, as demonstrated for the 0.5 µm technology. We have also shown that the ion dose rate and size of the area exposed have moderate effects on ΔV_t. This indicates that the magnitude of the parameter shifts is related to the amount of sample charging and charge-up rate rather than to the ion energy per se. The main effect of energy observed to date is that the dose level which a transistor can sustain prior to failure (e.g., by a gate oxide short) is reduced somewhat at the higher energy.

It should be noted that FIB exposure on the unshielded 0.5 µm transistors is truly a "worst case" situation. These transistors are completely isolated, without the charge dissipation paths that would be present in a real IC. The 0.225 µm transistors with common gate electrodes and protection diodes are closer to the structures encountered in actual use condition. We have also demonstrated that metal shielding helps reduce the effects of ion beam exposure. A large fraction of the transistors in today's ICs are at least partially shielded by overlying metallization lines and power buses.

We have performed most of the FIB exposures with a single ion beam current. This was done because the emphasis in this study was to compare the effects of FIB exposure at different ion beam energies and on different technologies. Ion beam current was a variable in our earlier study [1].

In practical terms, our findings indicate that it is always best to minimize the amount of FIB exposure of the sample if subsequent electrical operation is to be performed. Whenever possible, it is of benefit to navigate to the area of interest by using one or more of the available methods, including the use of known x-y coordinates of the area of interest and CAD navigation software. The use of measures to reduce sample charging, including electron flood charge neutralization and sample grounding, is always advisable.

Degradation Mechanism

It is known that charge accumulation can adversely affect transistor operation, causing effects ranging from subtle (and sometimes recoverable) parameter shifts to catastrophic (irreversible) damage of pn junctions and gate oxide. Charge accumulation on transistor electrical nodes and construction layers can occur both during fabrication (such as during plasma processes) and after fabrication due to testing, handling, and assembly electrostatic events. Excessive charge

accumulation in the sample (enough to cause the electric field in the gate oxide to exceed a critical threshold) can result in Fowler-Nordheim tunneling of electrons from the silicon such that impact ionization generation of electron-hole pairs becomes significant. **[Jeff- I one or two references here]**. This in turn can result in a large density of oxide- and interface-trapped charge. The I_{ds}-V_{gs} characteristics for the 0.5 μm technologies (see Fig. 3) exhibit a subthreshold stretchout following FIB exposure. Such stretchout is associated with the presence of interface traps. The post-FIB I_{ds}-V_{gs} characteristics for the 0.225 μm technology exhibit essentially no change or small parallel shifts relative to their pre-FIB values. The latter condition is consistent with oxide-trapped charge.

A number of our findings indicate that the primary transistor degradation mechanism is due to the charging effect of the Ga^+ ion beam. The effectiveness of the electron floodgun (used to provide a charge neutral surface) in minimizing parametric shifts strongly supports this hypothesis. Degradation effects are minimized with the incorporation of an overlying metal plate (which serves as a crude Faraday cage). When this plate is grounded during FIB exposure it would cause the electric field between the deposited positive charge on the passivation and the silicon substrate to be significantly altered. As a result, the electric field in the vicinity of the transistor is reduced, and hence, the likelihood for interface trap creation is much less. The diode-protected 0.225 μm technology transistors exhibit small degradations, while the unprotected devices show relatively larger parameter shifts. Clearly, the accumulated charge on the protected gates has an alternate path to the substrate, whereas the unprotected gates will dissipate charge almost exclusively through the gate oxide. Additional support for charging as the primary degradation mechanism is found in the dependence on exposure area (ΔV_t increased as the exposed area increased), independence of ion energy and the occurrence of parameter shifts in a radiation-hardened CMOS technology (the STI 0.5 μm technology).

Perhaps the most compelling evidence for charging-related degradation is the physical evidence of damage to the passivation. Comparison of the SFM topology and surface potential images suggests that localized charge accumulation occurs in the high resistivity passivation prior to an ESD-like event resulting in a dielectric failure. However, ESD-like events can also be non-fatal [3-6]. High electric field transients can produce shifts in V_t and other parameters due to oxide and interface trapped charge. ESD events in packaged ICs have been observed to alter transistor parameters within the IC, beyond the common manifestations of current leakage or shorts in I/O protection circuitry. In several cases, it has been shown that the alteration of transistor behavior is due to charge accumulation on the passivation layer above the affected transistors [7-9]. The accumulation of charge can be localized, especially for high resistivity passivation materials. Alternatively, such local charging might occur if the charge generation rate is high compared to the dissipation or neutralization rate or if the dissipation or neutralization mechanisms act in a nonuniform manner. The localized accumulation of charge on dielectric surfaces ("charge packets") during ESD events has interesting parallels to the features observed in the SFM topology and surface potential images of transistors after FIB exposure.

Our previous experiments on biased capacitors indicated the occurrence of radiation-type damage in the FIB system [1]. We do not discount these earlier findings, but believe that they are a secondary or tertiary effect compared with degradation due to sample charging.

Summary

We have described our recent investigation of the effects of ion energy during FIB exposure on MOS transistors, and have shown that the magnitudes of transistor threshold voltage shifts, ΔV_t, are comparable for FIB exposure with 30 and 50 keV ions. We have shown that, while the effects of FIB exposure increase as transistor size shrinks for a given technology, the observed ΔV_t are much smaller for a commercial 0.225 μm technology than for a 0.5 μm research technology. We have demonstrated that an overlying metallization shield reduces the magnitude of transistor parameter shifts as a result of ion beam exposure, and that both the instantaneous dose rate and area exposed to the ion beam play a role determining the magnitude of the transistor parameter shifts. Electron flood charge neutralization was found to be equally effective at minimizing ΔV_t at 30 and 50 keV. Finally, we have found physical evidence for the occurrence of localized charge buildup and subsequent electrostatic discharge in response to sample charging during FIB irradiation. All of these findings are consistent with sample charging during FIB exposure as the primary degradation mechanism.

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