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UPGRADING THE TFTR TRANSREX POWER SUPPLIES*

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***Abstract*— In order to provide improved and expanded experimental capabilities, the existing Transrex power supplies at PPPL are to be upgraded and modernized. Each of the 39 power supplies consists of two six pulse silicon controlled rectifier sections forming a twelve pulse power supply. The first modification is to split each supply into two independent six pulse supplies by replacing the existing obsolete twelve pulse firing generator with two commercially available six pulse firing generators. The second change replaces the existing control link with a faster system, with greater capacity, which will allow for independent control of all 78 power supply sections. The third change replaces the existing Computer Automated Measurement and Control (CAMAC) based fault detector with an Experimental Physics and Industrial Control System (EPICS) compatible unit, eliminating the obsolete CAMAC modules. Finally the remaining relay logic and interfaces to the "Hardwired Control System" will be replaces with a Programmable Logic Controller (PLC).**

Keywords-power supply; CAMAC; EPICS

I. OBJECTIVES

The Transrex power supplies, which were origionally procured for use on the Tokamak Fusion Test Reactor (TFTR), were designed over thirty years ago. The transformers and other power handling components have proven to be reliable, and with normal maintenance, should provide many more years of service. The auxiliary systems are becoming obsolete and in many cases the parts needed to maintain the units are no longer available. Also mechanical parts, such as printed circuit board edge connectors, wear out with use and are not easily repairable. The current system is in need of better diagnostics, since it can take over an hour to find the cause of a power system fault. To allow for doubling of the available toroidal field (TF) coil current, we need to double the number of parallel branches from four (4) to eight (8). This requires more floor space in the TF wing of the power conversion building to add current limiting inductors. The space for these inductors is currently occupied by the data acquisition and control system racks which will be replaced by the various new systems described in this paper. It is also desired to divide the current twelve pulse power supplies into two six pulse power supplies.

II. THE CURRENT SYSTEM

There are currently thirty nine (39) identical power supply units in use at PPPL. Figure 1 is a photograph of a typical power supply with several of the functional units labeled. The power supply consists of two, independent sections labeled 'A' and 'B' with their separate disconnect switches. Each section is wired as a six pulse phase controlled rectifier power supply with one section driven from the 'delta' secondary and the other driven by the 'wye' secondary of the common transformer. Each section contains six paralleled power modules and two paralleled bypass modules. These modules are independently removable, and can be easily serviced. The firing generator drives these two sections as if they were one twelve pulse power supply. The firing generator is provided one eight bit digital alpha signal, which sets the firing angle for both sections. This signal is provided from CAMAC modules which are driven from the NSTX real time control computer.

The fault detector uses independent sensors on both of the power supply sections, along with a limited number of common signals to provide a set of fast parallel fault signals and a set of slow series fault signals. The fault detection is done totally with analog processing, with gains, offsets and trip levels set with potentiometers. The monitoring and control of the fault detector uses many obsolete CAMAC modules.

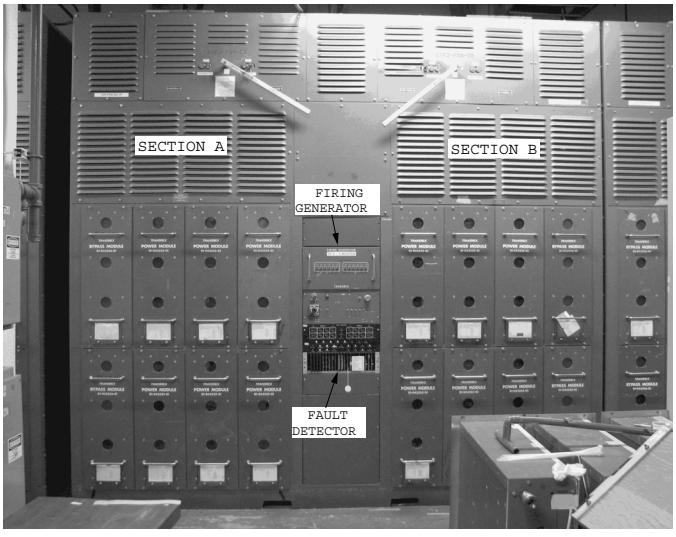

Figure 1. Transrex Power Supply

III. THE PROPOSED UPGRADES

There are three classes of upgrades being proposed, first systems that need no or minimal changes, second systems that need to be replaced immediately and finally systems that can be

upgraded as failures occur. There will also be an added interface to a PLC based fault system.

A. *Retained systems*

The main power components will all be retained. The transformer, primary and secondary current transformers and the primary voltage monitor transformers are all in good condition and will still be needed. The primary voltage phase reference circuit and the secondary current rectifier and filter assemblies will need to be re-packaged but the terminal boards and their related wiring will remain the same. The existing primary voltage monitor relays will be absorbed into the new fault detector.

The power modules and the bypass modules will be retained with no changes. The output voltage divider and the output disconnect switch will also not be changed. The Alternating Current Current Transformers (ACCT) on the input to the power modules will be retained as well as the Direct Current Current Transformers (DCCT) on the outputs of the bypass modules. The DCCTs are a known weak point in the system. It would cost $400.00 each and four to eight hours to replace each of the twelve DCCTs in a rectifier section. The current plan is to improve the analog electronics in the fault detector that operates the DCCTs, and to include the ability to easily replace the existing units with new units if future operation of the power supplies proves that to be necessary.

B. *Replacement Hardware*

The three necessary replacement items are the Firing Generator, the Control Link and the Fault Detector. Of these three only the Control Link and the Fault Detector are needed to remove all of the existing CAMAC hardware. The Firing Generator is only needed for splitting the operation of the two power supply sections. If the Firing Generator is not replaced initially, one of the printed circuit cards in it (the A14 card) will have to be replaced to allow for the new control link. Each of the replacement units will be designed to fit into the same physical location and use the same connectors, signal levels and pin-outs as the existing units. There will be some signals, such as the ones to the CAMAC modules that will not be used in the new system, but in those cases either a dummy connector will be provided or the unused cable can be coiled up and abandoned in place. There will be three new signals between the Firing Generator and the Fault detector, but these can be added on unused pins on the existing connectors. There will also need to be a new fiber optic cable added to the Firing Generator for the new Control Link. Sections IV, V and VI will cover the proposed new hardware.

C. *Hardware to be replaced as needed*

The existing Master Gate Driver (MGD) system and the output voltage monitor will be retained. Each of these systems contains components that are no longer available, but we retain enough spare parts to keep these running. There is an existing fiber optic analog link that with minor re-packaging can be installed in the place of the existing hardware, and the installation of a new fiber optic cable. The primary issue with the MGD is the obsolete fiber optic components. The upgrade path for these will have to be determined in the future.

D. *The fault system interface*

The fault protection system for each power supply will be modified with the addition of an interface to a new central PLC. This new PLC based system is being added to provide for better error reporting and fault tracing. See [1] for a description of the overall protection system.

IV. Power Supply Control Link

The existing power supply control link consists of an interface board which takes control words from the Front Panel Data Port (FPDP) interface on the real time control computer and converts the data to a form usable by the existing H336 and H337 CAMAC modules. The CAMAC modules then send the eight bits of firing angle data and four control bits to the firing generator in each power supply. The existing system is limited in its update rate since multiple CAMAC modules share a common serial link from the interface board. The CAMAC modules are a known point of failure in the existing system, and if the power supply sections are separated the existing stock of CAMAC modules would not cover the new requirements.

The proposed new control link would consist of three parts. First is a module called the FPDP Output Module – Serial (FOMS). This takes the FPDP data from the control computer, decodes the power supply address, and sends the firing angle data and the power supply control bits as a serial data stream to a power supply. Each FOMS will be able to control eight power supplies, with a maximum total of one thousand five hundred thirty six (1,536) total power supplies possible. Each FOMS channel output is provided with a fiber optic connection, which allows for ground isolation between the control system and the power supplies. The output data is Manchester encoded with a 6.25 MHz bit rate and up to 312.5 kHz update rate. The FOMS design will be derived from the existing FPDP Output Module – Analog (FOMA) module, with the analog output circuitry replaced by a shift register and Manchester encoder.

The second component of this upgrade is a fiber optic cable from the central location where the FOMS units are located to each individual power supply. The actual cable to each power supply will contain at least twelve individual fibers which along with the control link will also include the communication link for the fault detector, and spares for future enhancements.

The final component is the FOMS receiver. This will take the optical data stream from the FOMS, decode it to a parallel digital form and then output the firing angle and control bits as both a set of parallel bits and as an analog value. This allows for ease of testing and allows the firing generator to have the option of having either an analog or digital input. The receiver is derived from an existing fiber optic analog link, and will only require minor printed circuit board layout changes.

V. The Firing Generator

The new firing generator has two major operational constraints that it must meet. First, since the power supplies can be operated from the output of a motor – generator set, the firing generator has to be able to operate with an input

frequency that varies from 90 Hz to 50 Hz. This frequency can change at a rate of up to 10 Hz/second. The other constraint is the need to prevent commutation failure during inversion. This requires the firing angle to be limited in real time as a function of the input frequency, the load current, the load inductance and the input voltage. We are following three options for the firing generator, one is to procure a commercially available unit that can track frequency changes and then add a custom inversion limit calculator. Second is to procure a commercial firing generator that includes the inversion limit calculator. Finally the third option is to develop a fully custom unit. The firing angle command value and the computed inversion limit value will be stored by the fault detector for test and diagnostic purposes.

VI. THE FAULT DETECTOR

The new fault detector has three main functions that need to be implemented. First it must replace all of the CAMAC modules that have not been replaced by the control link. Secondly it must interface with both the existing parallel fault system and the new low speed fault system. Finally it must provide for all of the power supply section fault detection as well as interlock and fault checking functions for all common components in the power supply cabinet. Each power supply cabinet will have one fault detector chassis, but internally this will be implemented such that each power supply section will have an independent fault detector unit, with only the communications unit common to both sections. This will allow the fault detector sections to operate in the event of a communications processor failure. Each fault detector section will take as inputs the eighteen ACCT signals from each of the power modules, the twelve DCCT signals from the bypass modules, the output voltage, the total input current, and the power supply permissive signal. The common chassis fault detector will take the two firing angle signals, the inversion limit signals, the primary voltage and any other signals as are needed as inputs.

The analog signals will be received by an input circuit that will protect the fault detector hardware against overvoltage conditions, provide RF filtering and allow for self-test voltages to be applied. The input circuit will be followed by an analog anti-aliasing filter and an analog to digital converter. The digitized signals will go to a field programmable gate array (FPGA) for gain and offset correction, storage of the waveforms in an external memory, and all limit checks and fault calculations that need to be accomplished. Some of the fault checks that will be made in the FPGA are:

- Three phase current in balance into each power module
- DC currents within limits into each bypass module
- Bypass module not conduction when commanded
- Section current 'ON' for excessive time
- Output with lack of permissive

The fault detector will have to supply the excitation current for the existing DCCTs.

The FPGA will maintain a sixty four word list of faults along with a time stamp as to when the fault status changes, this will allow the user to determine what the initiating fault event was. The time stamp will be common to all power supplies to within one microsecond, so that interactions between power supplies can be traced. The waveform memory on each fault detector will be able to store up to 15.4 seconds of all analog waveforms from a trigger point defined by the facility clock system. The self-test voltage input to the analog input stage will allow for an automatic test of the fault detector hardware and firmware. Each of the custom boards in the fault detector will have on-board power supply checking as well as a test that all boards are installed.

The fault detector will have a communications processor which will act as an EPICS server to provide data acquisition and control functions. The processor will also provide a web server which will allow the power supply status to be easily viewed. The common processor will only be used for communications to the three individual FPGAs and will not take part in the protection functions.

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[1] X.Zhao, NSTX Protection and Interlock Systems, 23rd Symposium on Fusion Engineering.

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