

LOW TEMPERATURE FRONT SURFACE PASSIVATION OF INTERDIGITATED BACK CONTACT SILICON HETEROJUNCTION SOLAR CELL

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ABSTRACT

The interdigitated back contact silicon heterojunction (IBC-SHJ) solar cell requires a low temperature front surface passivation/anti-reflection structure. Conventional silicon surface passivation using SiO₂ or a-SiN_x is performed at temperature higher than 400°C, which is not suitable for the IBC-SHJ cell. In this paper, we propose a PECVD a-Si:H/a-SiN_x:H/a-SiC:H stack structure to passivate the front surface of crystalline silicon at low temperature. The optical properties and passivation quality of this structure are characterized and solar cells using this structure are fabricated. With 2 nm a-Si:H layer, the stack structure exhibits stable passivation with effective minority carrier lifetime higher than 2 ms, and compatible with IBC-SHJ solar cell processing. A critical advantage of this structure is that the SiC allows it to be HF resistant, thus it can be deposited as the first step in the process. This protects the a-Si/c-Si interface and maintains a low surface recombination velocity.

INTRODUCTION

The rapid market growth of silicon solar cells is driving the development of devices using thinner Si wafers and higher efficiency technologies, both of which require approaches capable of low surface recombination together with elimination of optical loss in the illuminating side for high open circuit voltages (V_{oc}) and high short circuit currents (J_{sc}). The interdigitated back contact (IBC) silicon solar cell structure proposed by Lammert and Schwartz [1], where the emitter and contact are on the back of the wafer, provides an independent control for optimum optical performance in the illuminating front side and optimum electrical performance with low series resistance on the back side. The IBC silicon heterojunction (IBC-SHJ) solar cells fabricated at IEC have confirmed efficiency of 11.8% under AM1.5 illumination using an a-Si/ITO structure for front surface passivation and anti-reflection coating [2]. However, the structure was not fully optimal and resulted in a low J_{sc} due to extra optical absorption loss in a-Si:H, which means the a-Si:H film should be as thin as possible. The a-Si:H/crystalline silicon (c-Si) structure has demonstrated a low surface recombination, but it is often seen that the passivation quality degrades over time [3], especially for a thin (<20 nm) a-Si:H layer. Additionally, the growth of ITO AR coating, degrades the front surface passivation most likely due to ion damage during sputtering. The PECVD grown a-SiN_x:H requires to be deposited at a wafer temperature over 400°C to ensure high quality

passivation [5-8]. However, the high deposition temperature is not compatible with IBC-SHJ where a-Si:H is used for the emitter and base layers. Additionally, a-SiN_x:H is soluble in HF and makes the fabrication process for the back emitter and base layers more complex.

The purpose of this work is to develop a front surface passivation structure of IBC-SHJ solar cell with the following properties: low and stable front surface recombination velocity (SRV), effective AR coating, HF resistant and minimum optical absorption. In this paper, we propose an a-Si:H/a-SiN_x:H/a-SiC:H stack structure to passivate and AR coat the front surface of c-Si wafer for a IBC-SHJ solar cell structure. All processing steps are performed at low temperature, <300°C, which are compatible with the a-Si:H emitter and base structures. The optical properties of PECVD a-SiN_x:H and a-SiC:H films are characterized along with the surface passivation quality and stability of different a-Si:H layers with and without a-SiN_x:H/a-SiC:H. Solar cells using such structures are fabricated, and device performance is discussed.

OPTICAL PROPERTIES OF a-SiN_x:H/a-SiC:H

The a-SiN_x:H films were grown by RF-PECVD on both 7059 glass and uncleaned n-type float-zone c-Si wafer substrates at 1000 mTorr with gas flow rates of SiH₄=20 sccm, H₂=100 sccm and NH₃=80 sccm. The substrate temperature was either 150°C or 300°C, and the plasma power was varied from 20W to 40W to control the film properties. The a-SiC:H films were deposited at 200°C by DC-PECVD at 1250 mTorr and 123 mA, with gas flow rates of SiH₄=10 sccm, H₂=60 sccm and CH₄=30 sccm. The optical properties of the films were characterized using a VASE32 ellipsometer and the data was analyzed using a Tauc-Lorentz oscillator model. Figures 1 and 2 show the indices of refraction and extinction coefficients respectively of a-SiN_x:H and a-SiC:H films as a function of photon wavelength.

The a-SiN_x:H film deposited at 300°C with plasma power of 40W exhibits a refractive index of 2.0 – 2.2 over a wide wavelength range, which is adequate for use as an anti-reflection (AR) layer on Si wafer. The refractive index of a-SiC:H film is, however, far below 2.0 at incident photon wavelength of higher than 400 nm and hence is not optimized for AR properties. Extinction coefficients of all films reduce to zero above the wavelength of 500 nm. In a-SiC:H film the absorption of short wavelength photons can be further suppressed by widening its bandgap.

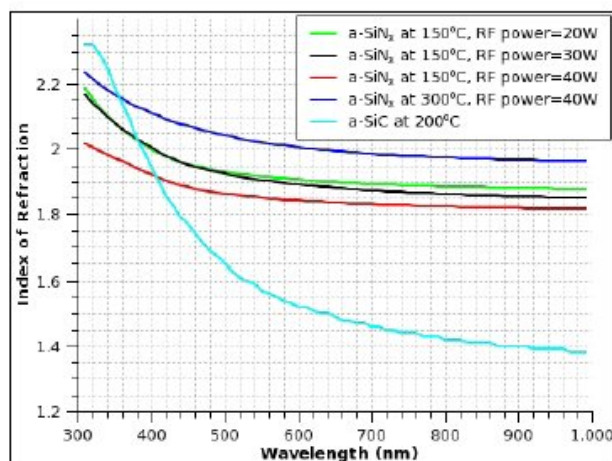


FIG. 1: Index of refraction of PECVD a-Si_x:H and a-SiC:H films.

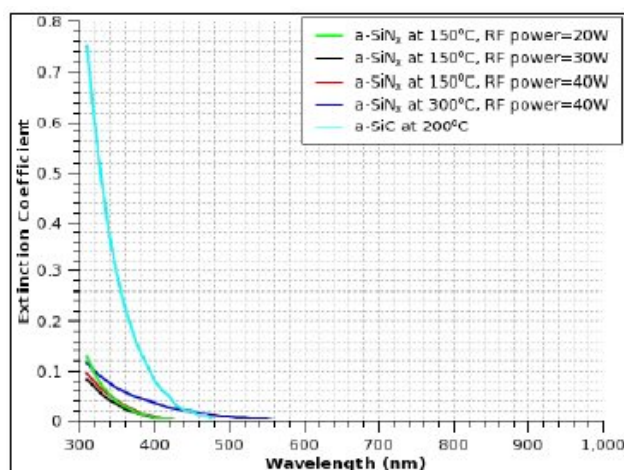


FIG 2: Extinction coefficient of PECVD a-Si_x:H and a-SiC:H films.

To evaluate the optical transmission and reflection of the films, 60 nm a-Si_x:H/20 nm a-SiC:H structures were deposited on glass substrates. Additionally, a-Si:H/ a-Si_x:H/a-SiC:H structures were prepared on polished c-Si wafers.

Figure 3 shows the absorption determined from T and R measurements for the ITO (80 nm) and a-SiN (60 nm)/a-SiC (20 nm) stack. The stack has slightly higher absorption from 350 to about 900 nm, where the free carrier absorption in the ITO begins to increase. Integration of the absorption with the AM1.5 spectra gives 1.0 and 1.5 mJ/cm² losses for the ITO and the stack, respectively.

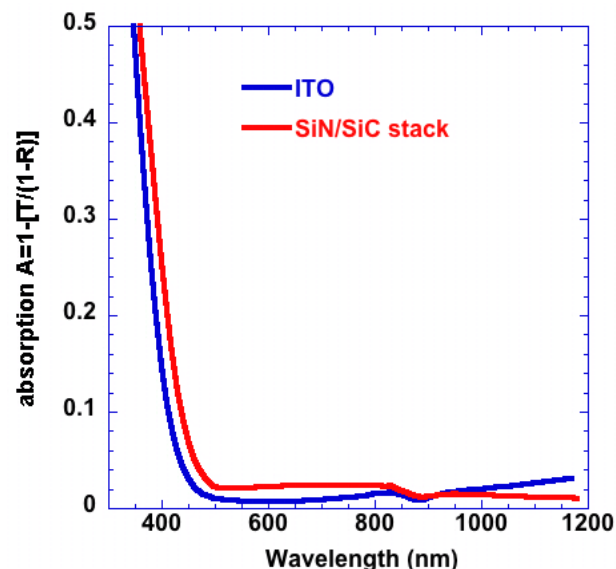


FIG 3: Absorption of the 80 nm thick ITO and a-SiN:H (60 nm)/a-SiC:H (20 nm) stack on glass (no a-Si:H).

SURFACE PASSIVATION USING a-Si:H/a-Si_x:H/a-SiC:H STACK STRUCTURE

To evaluate the surface passivation quality, symmetric test structures (identical structures on both front and back c-Si surfaces) consisting of either a a-Si:H layer or a a-Si:H/a-Si_x:H/a-SiC:H layered structure were deposited on 300 μm n-type Fz silicon wafer with resistivity of 2.5 Ωcm. The wafer was cleaned using a 5 min piranha etch (H₂SO₄/H₂O₂), followed by a 5 min DI water rinsing, a 60 sec dipping in 10% HF solution prior to loading in the deposition system. The intrinsic a-Si:H layers of different thickness were deposited using 123mA DC plasma with gas flow ratio R=H₂/SiH₄ =4 and 1250 mTorr gas pressure at 200°C, followed by a 25 min annealing at 300°C in vacuum. 60 nm thick a-Si_x:H was then deposited at 300°C, followed by 20 nm thick a-SiC:H deposition at 200°C. The wafer was flipped over within the system without breaking vacuum. After depositions, half of the samples were stored in atmospheric environment and the other half in vacuum to test stability of effective minority carrier lifetime over time.

The effective minority carrier lifetime was measured using a Sinton WCT-100 photoconductive decay tester and in all cases determined using a minority carrier density of 10¹⁵ cm⁻³. The measured lifetime is dominated by recombination at c-Si surface due to the high lifetime of Fz wafer. Hence the changes in lifetime are considered to be due to changes in the surface passivation quality.

The changes of measured lifetime of the samples which have only intrinsic a-Si:H layers are shown in Figure 4. An initial lifetime of >1 ms with 5 nm a-Si:H thickness was measured; however, the lifetime decrease by a factor of 4 within 2 days when stored in air. The surface passivation with 20 nm a-Si:H layer remain almost unchanged over two weeks. The lifetime

decay is much slower for the sample stored in vacuum. One of the possible reasons of instability of lifetime is due to the water adsorption on the surface. Therefore, thicker a-Si:H layer results in stable and high lifetime but has a higher optical absorption. The calculated J_{SC} losses with different intrinsic a-Si:H layers thickness are given in Table.I. Thus, there is a trade-off between passivation resulting from a-Si:H and optical absorption in a-Si:H layer.

The lifetimes of the samples with different thickness of a-Si:H layer capped with a-SiN_x:H/a-SiC are higher than those of uncapped samples, especially for the cases 2 nm and 5 nm a-Si:H layers, and are stable over time as shown in Figure 5. A stable effective minority carrier lifetime over 2 ms with 2 nm a-Si:H was achieved using the stack structure. This suggests that a-SiN_x:H/a-SiC stacked capping layer not only greatly improves the a-Si:H/c-Si interface passivation, but also removes any instability of effective lifetime. This structure should also have very low absorption losses, about 1.5 (AR stack)+0.2 (a-Si) =1.7 mA/cm². Additionally, a-SiC:H layer is not soluble in HF and protects the a-SiN_x:H during cell processing.

Table I: J_{SC} Losses with different thickness of intrinsic a-Si layer.

	2 nm a-Si	5 nm a-Si	10 nm a-Si	20 nm a-Si
J_{SC} Loss (mA/cm²)	0.23	0.54	0.98	1.77

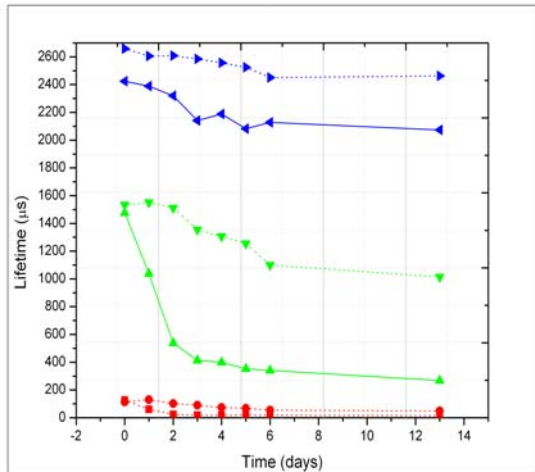


FIG. 4: a-Si:H passivation vs. time. Red solid (dotted): 2 nm intrinsic a-Si:H, stored in air (vacuum). Green solid (dotted): 5 nm intrinsic a-Si:H, stored in air (vacuum). Blue solid (dotted): 20 nm intrinsic a-Si:H, stored in air (vacuum).

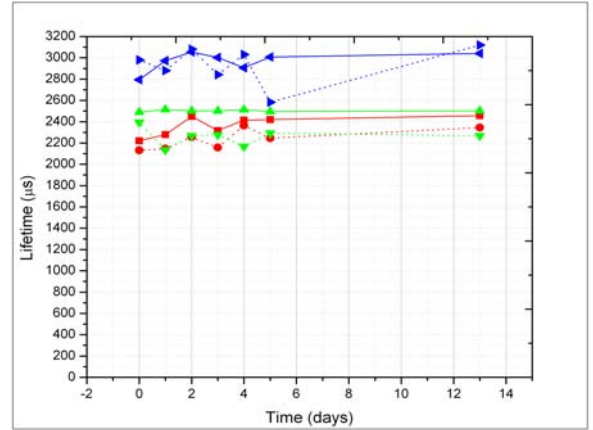


FIG.5: a-Si:H/a-SiN_x:H/a-SiC:H stack structure passivation vs. time. Red solid (dotted): 2 nm intrinsic a-Si:H, stored in air (vacuum). Green solid (dotted): 5 nm intrinsic a-Si:H, stored in air (vacuum). Blue solid (dotted): 20 nm intrinsic a-Si:H, stored in air (vacuum).

SOLAR CELL PERFORMANCE

A schematic of the IBC-SHJ solar cell is shown in Figure 6. The cells are fabricated on 300 μ m n-type Fz silicon wafer with resistivity of 2.5 Ω cm. All a-Si:H layers, intrinsic and doped, were deposited at 200°C. On the back side of the wafer, the emitter and contacts consist of interdigitated p-type and n-type a-Si layers at a thickness of 20 nm. There was no intrinsic a-Si:H passivation layer used on the rear contacts, therefore the back SRV will be high and the V_{OC} low. This was done to simplify the process to allow focus on the front surface. A 200 nm thick aluminum deposited by electron beam evaporation is used as a robust contact for testing. The interdigitated pattern was created by a 2-step photolithography process where p and n regions have lateral dimensions of 1.2 mm and 0.5 mm, respectively. The separation between p and n regions is 50 μ m. To evaluate the front surface passivation of the stacked structure, solar cells were fabricated with either an a-Si:H/ITO or a-Si:H/a-SiN_x:H/a-SiC:H structure. The thickness of the front a-Si:H layer was either 5 or 20 nm.

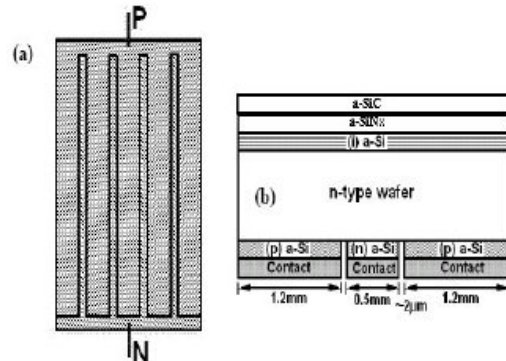


FIG 6: Schematic picture of the IBC-SHJ structure: (a)bottom view.(b)cross section view of structure without i-layer. For clarity, the cell dimension is greatly exaggerated.

Table II shows J_{SC} and integrated IQE for four IBC-SHJ solar cell with different front surface passivation and AR layer structures. A key difference between devices with ITO or the a-Si $_x$ H/a-SiC:H stack is that the ITO was deposited as the last step, after ~12 days, while the a-Si $_x$ H/a-SiC:H stack was deposited first. Thus, the critical front surface was better protected during processing with the a-Si $_x$ H/a-SiC:H stack than with ITO. With an ITO layer as an AR coating applied at the end of cell fabrication, reducing the a-Si thickness from 20 to 5 nm decreases J_{SC} from 24.7 mA/cm² to 1.8 mA/cm². This large drop in J_{SC} is due to a degraded front surface passivation quality over the complete solar cell fabrication period (as shown in Figure 4). The QE of this device showed response only from 800-1200 nm presumably because the front SRV was so high that only carriers generated near the back surface were collected. It also had the lowest V_{OC} , consistent with the high front SRV. However, the a-Si $_x$ H/a-SiC:H stack structure with 5 nm a-Si:H had improved J_{SC} of 27.5 mA/cm², which is consistent with a stable front surface passivation quality and a reduced absorption loss due to thinner a-Si:H.

Table II: Measured J_{SC} and calculated photocurrent from integration of IQE with AM1.5 spectrum. The V_{OC} for the last three devices were in the range 0.55-0.60V while the first one had 0.44V.

Front surface structure	J_{SC} mA/cm ²	IQE mA/cm ²
5nm a-Si/ITO	1.8	n/a
20nm a-Si/ITO	24.7	26.1
5nm a-Si/Stack layer	27.5	30.2
20nm a-Si/Stack layer	24.9	n/a

Figure 7 shows the internal $IQE = QE/(1-R)$ and R for IBC devices with two types of front passivation layers. Despite the slightly higher absorption for the 5 nm a-Si:H/stack structure (Figure 7), this device has significantly higher IQE over the entire wavelength range. Integration of the IQE with the AM1.5 spectra is shown in Table II. The 4 mA/cm² difference is comparable to the difference in J_{SC} (Table II). The increase in IQE with wavelength over most of the range is consistent with the fact that carriers must reach the back of the device to be collected, thus more deeply generated carriers are collected more efficiently. Two additional observations about the J_{SC} and IQE. First, the thicknesses have not been optimized to minimize reflection. Second, LBIC scans for these devices show 30-50% lower collection for carriers generated above the n-strip (base contact) compared to the p-strip (emitter) for devices with unoptimized back surface passivation like these. Given that the ratio of n-to-p strip widths is $(4 \times 0.5)/(5 \times 1.2) = 0.33$, an additional 10-15% of the current will be lost due to this rear contact collection problem. This explains why the IQE does not approach unity in Figure 7. We have shown that this decreased collection over the n-strip is greatly diminished with good back surface passivation, leading to $J_{SC} = 30$ mA/cm² and $V_{OC} = 0.67$ V (9).

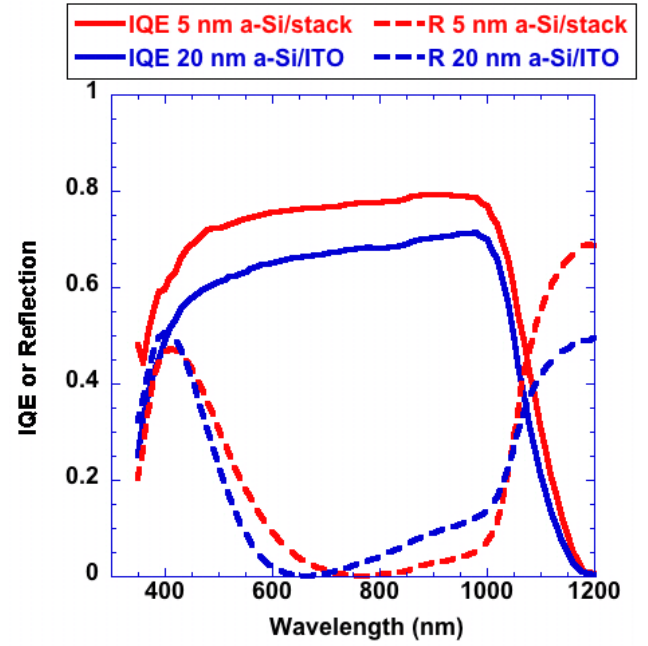


FIG. 7: IQE (0V, 100% bias light) and R for the completed devices.

Summing the front absorption losses due to the a-Si:H (Table I) and the AR coatings (discussed in Figure 3) gives 2.7 mA/cm² for the a-Si:H (20 nm)/ITO and 2.0 mA/cm² for the a-Si:H (5 nm)/a-Si $_x$ H/a-SiC:H stack. Yet there is a 4 mA/cm² difference in the photocurrent calculated from the IQE of Figure 7. Clearly, the stack has additional benefits for the photocurrent. This may be partially explained by Figure 8 which shows the bias light intensity of the QE for the device with a-Si:H (20 nm)/ITO front passivation layer measured with 0, 10, and 100% bias light. Note the significant increase in QE with light intensity especially below 800 nm. This agrees with the carrier density dependent lifetime observed by lifetime measurements reported elsewhere [2] in which we speculated this is due to ion damage of the a-Si:H during ITO sputtering. It suggests that the details of the front surface passivation influence the carrier collection throughout the bulk of the wafer. This effect was not observed in the other PECVD-based front passivation layers. Thus, collection hence J_{SC} for the ITO device is also reduced by the reduction in front surface recombination. This is not a fundamental limitation since Sanyo uses ITO on their high efficiency HIT cells.

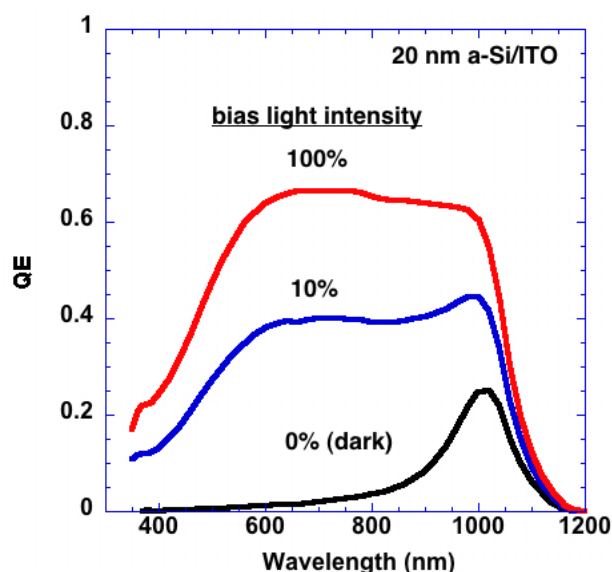


FIG. 8: QE for device with 20 nm/ITO layers measured at 3 bias light intensities.

CONCLUSION

A 20 nm thick a-Si:H with ITO AR layer provides excellent passivation quality but with increased optical absorption loss and lower J_{SC} . In this paper, we propose a more transparent stack structure (a-Si:H/a-SiN_x:H/a-SiC:H) to passivate the front surface of crystalline silicon at low temperature. A critical advantage of this structure is that the a-SiC:H allows it to be HF resistant, thus it can be deposited as the first step in the process. This protects the a-Si:H/c-Si interface and maintains a low SRV. Using an ITO layer deposited at the end of the process requires a much thicker a-Si:H layer with attendant optical losses. With only a 2 nm a-Si:H passivation layer, the stack structure exhibits stable passivation with effective minority carrier lifetime higher than 2 ms, which is compatible to IBC-SHJ solar cell processing. A reduced optical loss with thinner a-Si:H layer in stack structure is evident from higher J_{SC} in IBC-SHJ cell. Passivation of front and back surfaces is critical for a high efficiency IBC-SHJ solar cell.

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