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Outside of Normal Operating Conditions: Using Commercial Hardware in Space Computing Platforms for Ubiquitous Sensing

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Abstract

Over the past decade field-programmable gate arrays (FPGAs) have been useful in speeding up digital signal processing (DSP) algorithms, and FPGA implementations can be orders of magnitude faster than microprocessor implementations. As many national security satellites are DSP-oriented, many organizations have started using commercial FPGAs to process data closer to the sensor. Using commercial technology successfully in this environment has lead to new research into fault tolerance and resilience.

1. Introduction

Ubiquitous sensing is an important aspect of the national security program. More and more, this data collection is handled by satellites designed to monitor global events. The satellite data is currently sent to ground stations for further processing, such as removing sensor artifacts from the data or doing feature extraction, so that policy analysts can make decisions based on this data. Over time the number of sensors and the amount of data these sensors produce has increased. As the *telemetry pipeline* responsible for communicating the data to the ground station is small, this has led to what is often called the *telemetry chokehold*, which limits the amount of data that can be transmitted.

In an attempt to optimize the telemetry, several government and commercial organizations have been researching the use of commercial electronics to provide on-board processing. These organizations have been studying the commercial field-programmable gate arrays (FPGAs) for space-based computational platforms for the past decade [1][2]. As FPGAs implement user circuits in programmable logic and routing in SRAM technology, the speedups for implementing digital signal processing (DSP) algorithms, which are often used in space-based computing, are comparable with building custom hardware. Unfortunately, commercial FPGAs are not radiation-hardened and radiation-induced faults, called single-event upsets (SEUs), can cause the user circuit to output bad data. This research has shown that triple-modular redundancy can be used effectively to mask radiation-induced errors [3].

The first demonstration of this research at Los Alamos National Laboratory was launched on the Cibola Flight Experiment (CFE) satellite in March 2007, which had nine Xilinx Virtex-I field programmable gate arrays (FPGAs) for a software-defined radio application. Since it's launch we have been monitoring CFE's hardware for SEUs. While there have been more than 100 SEUs since launch, the FPGAs have been able to continue processing fault tolerantly.

Conclusions

In conclusion, we have presented a brief introduction to how commercial electronics are being used as part of the national security ubiquitous sensing program in spacecraft. Since these devices were not intended for the harsh radiation environment, their sensitivity to radiation must be measured and fault tolerance techniques must be studied. The first demonstration of this hardware has been working successfully on orbit since March 2007.

Bibliography

[1] E. Fuller, et al, "Radiation test results of the Virtex FPGA and ZBT SRAM for space based recon_gurable computing," in Proceeding of the Military and Aerospace Programmable Logic Devices International Conference(MAPLD), Laurel, MD, September 1999.

[2] M. Caffrey, at al, "A space-based recon_gurable radio," in Proceedings of the 5th Annual International Conference on Military and Aerospace Programmable Logic Devices (MAPLD), September 2002, p. A2.

[3] C. Carmichael, "Triple module redundancy design techniques for Virtex FPGAs," Xilinx Corporation, Tech. Rep., November 1, 2001, XAPP197 (v1.0).

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