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DUAL-SIDE WAFER PROCESSING AND RESONANT TUNNELING TRANSISTOR APPLICATIONS

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We describe dual-side wafer processing and its application to resonant tunneling transistors in a planar configuration. The fabrication technique utilizes a novel flip-chip, wafer thinning process called epoxy-bond and stop-etch (EBASE) process, where the substrate material is removed by selective wet etching and stopped at an etch-stop layer. This EBASE method results in a semiconductor epitaxial layer that is typically less than a micron thick and has a mirror-finish, allowing backside gates to be placed in close proximity to frontside gates. Utilizing this technique, a resonant tunneling transistor – the double electron layer tunneling transistor (DELTT) - can be fabricated in a fully planar configuration, where the tunneling between two selectively-contacted 2DEGs in GaAs or InGaAs quantum wells is modulated by surface Schottky gate. Low temperature electrical characterization yields source-drain I-V curves with a gate-tunable negative differential resistance.

INTRODUCTION

In heterostructure modulation-doped FETs, the conducting region is composed of two-dimensional electron gas (2DEG) layers confined within quantum wells. By stacking the QWs [1] or using a single wide QW [2], multi-channel MODFETs have been exploited mainly to achieve higher current operation. However, although the resonant tunneling process is known to be extremely high-speed (in the THz regime) [3], to date there have been few studies of resonant tunneling between the channels. In particular, the implementation of tunneling transistors based on multi-channel MODFET structures as a novel quantum device has received relatively little attention until recently. [4]

The first resonant tunneling device to be demonstrated was the double-barrier resonant tunneling diode (DBRTD). [5] In the DBRTD, electrons in a three-dimensional (3D) emitter layer can pass into a 3D collector layer only by first resonantly tunneling through the two-dimensional (2D) states in a quantum well (QW) formed by the two barriers between the emitter and collector. The extremely high speed of resonant tunneling was demonstrated by the observation of power oscillations at 712 GHz. [6] However, the main drawback of the DBRTD structure is that it is not practical to add a third terminal so as to create a resonant tunneling transistor: schemes to add a third terminal have all required non-planar geometries in which the stringent lithographic tolerances required render the device impractical. [7] In order to circumvent this difficulty, hybrid devices combining both the DBRTD and either bipolar transistors [8] or

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FETs [9] have been explored as an alternative. We note that many other proposed quantum transistors, including single electron transistors [10] and quantum cellular automata [11], encounter similar difficulties with respect to non-planar geometries and the resulting stringent lithographic tolerances. [11].

Recently, we reported a novel resonant tunneling transistor, the double electron layer tunneling transistor (DELTT), which avoids these problems. In the DELTT two separate independently contacted 2DEG channels are realized from MBE-grown, modulation-doped GaAs/$Al_{0.3}Ga_{0.7}As$ coupled double QW heterostructures. Tunneling between the two 2DEGs is controlled by a surface Schottky gate. [4] The DELTT thus has a planar geometry with very practical requirements for lithographic dimensions (order of microns). The only critical dimensions of the DELTT are in the growth direction and are well within the capabilities of modern epitaxial growth techniques. Because both electron layers of the DELTT are 2D, the positions of the QW subband energy levels, and hence the tunneling current, are easily controlled by biasing a surface gate, yielding the transistor action.

The schematic structure of the DELTT is shown in Fig. 1(a). The DELTT is comprised of diffused Au/Ge/Ni ohmic contacts to the quantum wells, front and back

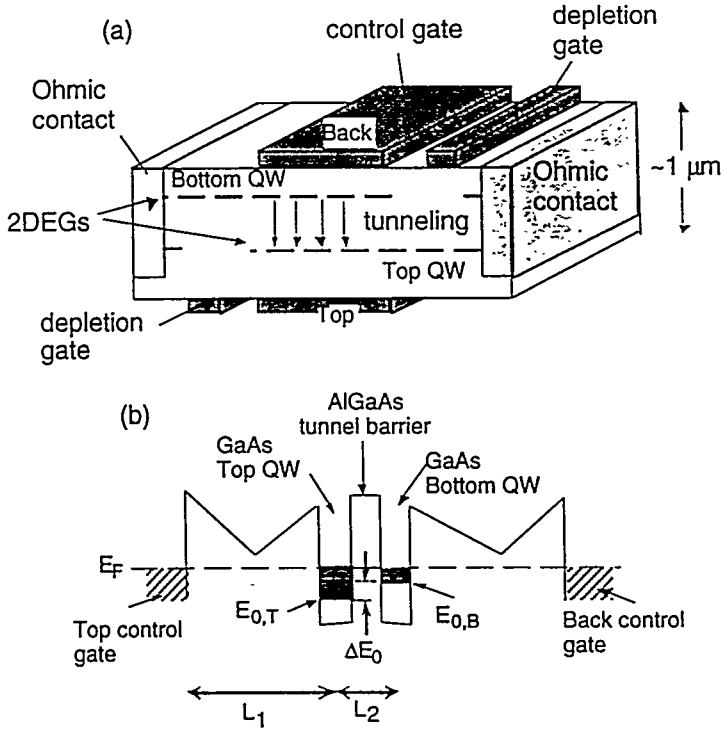

FIG. 1 (a) Schematic diagram of the DELTT device structure, showing the two selectively contacted 2DEGs via a selective gate depletion technique. (b) Typical conduction-band profile with no gate or source-drain bias.

depletion gates which allow for *independent electrical contact to each quantum well*, and a front and/or back control gate for switching the tunneling on and off. Independent contacts to each 2DEG layer are obtained by applying a negative DC bias to the front and back depletion gates, depleting electrons from the QW that one does not wish to contact. By this technique, the source ohmic makes electrical contact to only the top QW and the drain ohmic makes electrical contact to only the bottom QW. The backgating of QWs can be done by either ion-implantation through a patterned SiN mask or by use of the epoxy-bond-and-stop-etch (EBASE) technique [12], to be described below. All of the DELTTs presented in this paper were fabricated by EBASE, which allows mutually aligned lithographic processing on both sides of an epitaxial layer as thin as 0.25 microns, over cm^2 areas. We also report on the extension of the EBASE technique to utilize dual-side electron beam lithography in which sub-0.1 μm dual-side alignment is achieved by use of the same set of metallic alignment marks for both the front and back side electron beam patterning. [13]

FABRICATION

The DELTTs were fabricated from MBE-grown, modulation-doped $GaAs/Al_{0.3}Ga_{0.7}As$ double QW heterostructures with a chemical etch-stop on a sacrificial substrate. Fabrication begins with conventional frontside processing using several levels of optical lithography and standard semiconductor processing. First, device mesas are defined and Au/Ge/Ni contacts are evaporated and annealed 90 seconds at 420 °C. Several front-side Schottky gates composed of 200 Å Ti/2000 Å Au are then deposited by evaporation and lift-off. When electron beam lithography is necessary, the optically-defined Schottky gates lead up to the device mesa and then terminate, and then the actual device gates are defined by electron beam lithography and are aligned to the optically-defined gate leads. The electron beam lithography was performed on a JEOL JBX-5FE thermal field emission system operating at 50 kV. The beam current used was 1 nA with a corresponding beam diameter of approximately 12 nm. The resist used was polymethylmethacrylate (PMMA) at a thickness of 400 nm. The PMMA was developed for one minute in a 1:3 solution of methyl isobutyl ketone and isopropyl alcohol. The gates consist of 10 nm Ti/70 nm Au deposited by electron beam evaporation followed by liftoff in acetone. This completes the frontside processing. Shown in Fig. 2 are the steps used in the EBASE process.

After the front side processing [Fig. 2 (a)] is complete, the sample is ready to be epoxied to the host support substrate as shown in Fig. 2 (b). A low viscosity heat-cured epoxy has been found to be best for bonding the samples. A small amount of epoxy is placed on the front side of the active wafer, and the host substrate is placed smooth-side down on the epoxy. The sample is then baked on a 100 °C hotplate for about 30 minutes to cure the epoxy. Once the epoxy has hardened, the original sacrificial substrate on which the active layers were grown is removed as shown in Fig. 2 (c). Because of the relatively slow etch rate of the selective citric acid etch used later in the process, most of the substrate is first removed by mechanical lapping using a 3 μm Al_2O_3 grit with the

sample attached by wax to a glass puck. When only about 25 μm of the sacrificial substrate remains, the lapping is finished. The sample is then placed in the citric acid selective etch to remove the remaining GaAs sacrificial substrate. Etching stops on a ~3000 Å thick $Al_{0.55}Ga_{0.45}As$ stop etch layer grown at the base of the epitaxial layer structure, leaving a mirror finish.

The design of the stop etch layer is based on the chemical etching selectivity and takes into account the possibility of oxidation of the surface. To get a high selectivity of etch rates between the sacrificial GaAs substrate and the stop etch layer, we use a critic acid selective etch buffered with H_2O_2 in the ratio 6.5:1 (critic: H_2O_2), which etches GaAs much faster than $Al_xGa_{1-x}As$. While this etch solution in general shows a greater selectivity for higher Al content, a pure AlAs stop etch layer leaves a very rough surface after etching, presumably due to oxidation of the finished surface. On the other hand, $Al_{0.3}Ga_{0.7}As$ exhibits a selectivity over GaAs of only 100, which is somewhat low for our purposes. We have found that a 55% - 75 % aluminum content AlGaAs layer has very high selectivity, yet still yields an extremely smooth surface for patterning.

The electrical contacts to the front side gates and ohmics are accessed by via holes etched through the active layers as shown in Fig. 2(d). On the same evaporation step, 200 Å Ti/2000 Å Au is deposited in the via holes, and also in the backside Schottky gate

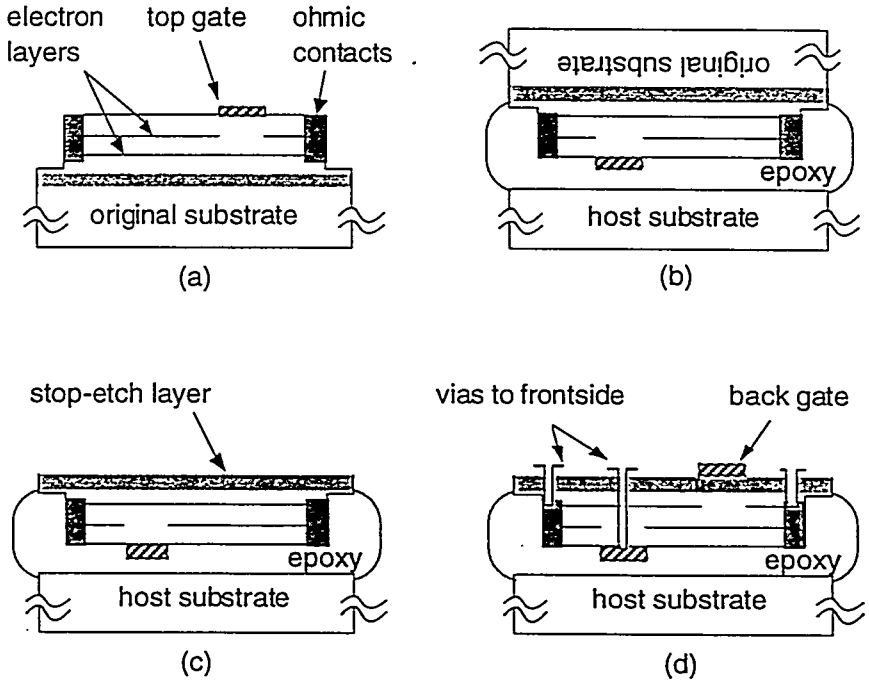

FIG. 2. Sketch of the different steps involved in the epoxy-bond-and-stop-etch (EBASE) technique. (a) Top side processing. (b) Epoxying to new host substrate. (c) Removal of original substrate with a chemical stop-etch. (d) Etching of vias to frontside contact pads and deposition of back gates

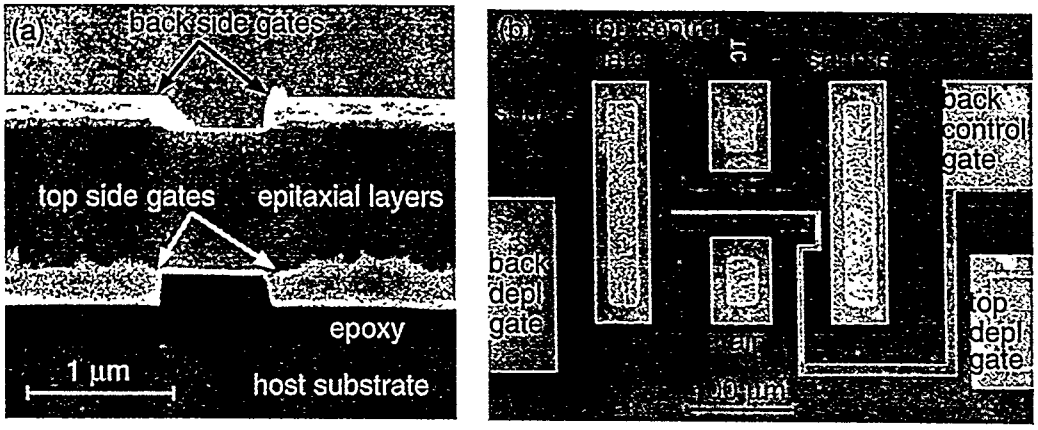

FIG. 3. (a) Scanning electron micrograph side view of an EBASEd test structure. The irregularities in the top gate metal are due to cleaving. (b) Top side view of a DELTT fabricated for microwave probing.

pattern. The front and back gates are placed in close proximity to the quantum wells on opposite sides of the micron-thick epitaxial layer through the use of the EBASE process. If necessary, we can also utilize a second stop etch step to thin the epitaxial layers down to submicron thickness, In this case the first AlGaAs stop-etch layer is itself also removed by a second selective etch which terminates on a 15 nm thick GaAs stop-etch layer. The second selective etch enables attainment of a total epitaxial layer thickness of only 230 nm, as well as increasing the smoothness of the backside surface.

In the case where electron-beam processing is involved, a pair of electron beam alignment marks is defined optically as part of the frontside processing. These alignment marks are easily detected by the 50 kV electron beam from the back surface through the several hundred nanometers of epitaxial material remaining at the end of the EBASE processing, since the electron beam easily penetrates it. Use of the same set of alignment marks allows for sub-tenth-micron alignment between the front and backside patterns. As shown in Fig. 3 (a), precise alignment of the front and back gates is obtained.

Fig. 3(b) shows a SEM image of a DELTT designed for microwave probing in ground-signal-ground configuration. Unlike a HEMT, the DELTT has three additional 2 μm long gate fingers, which act as front and back depletion gates and a backside DC control gate. The top RF gate length L_G is 1 μm, and the width is 100 μm. The source-drain contact spacing is 12 μm. We have also fabricated DELTTs with submicron gate lengths utilizing the dual-side electron beam lithography technique described above, where the source-drain spacing is only a few microns.

DELTT OPERATION.

In the DELTT, electrons undergo 2D-2D interwell tunneling between the two quantum wells in the device. However, to first order the tunneling can occur only when there exist states in both QWs with identical energy and in-plane momentum. [14] This is

Sample	w_{QW} Å	t_b Å	n_t 10^{11} cm^{-2}	n_b 10^{11} cm^{-2}	ΔE_F meV	PVR
G1717	150	125	2.0	1.4	2.1	20:1
G1881	120	125	8.0	2.0	21.3	8:1
EA141	200	70	1.7	2.57	3.0	12:1
EA255	120	100	5.6	6.6	3.5	10:1

TABLE 1. Sample parameters for DELTT devices G1717, G1881, EA141 and EA255. Given are QW widths (w_{QW}), tunnel barrier thickness (t_b), built-in electron densities for the top and bottom QWs (n_t and n_b) and the resulting difference in Fermi energy ($\Delta E_F = |E_{F1} - E_{F2}|$), when no biases are applied. The PVR is the peak-to-valley current ratio obtained from low temperature (~1 K) source-drain I-V measurements.

equivalent to requiring that the top and bottom quantum well subband energies E_{0T} and E_{0B} be precisely aligned. When the subband energies E_{0T}, E_{0B} differ as illustrated schematically in Fig. 1(b), no pairs of states of identical momentum and energy exist and then tunneling does not occur, neglecting inelastic scattering. Tunneling can be switched on by (1) varying the densities of either 2D layer with surface gates, (2) changing the chemical potential difference between the QWs by applying a source-drain bias, or (3) both. The current depends on the difference in the subband energies $\Delta E_0 = E_{0,T} - E_{0,B}$, with the tunneling current exhibiting a strong peak at $\Delta E_0 = 0$. In general, the subbands will coincide and $\Delta E_0 = 0$ when

$$eV_{SD} - C_T V_{TC} \pi\hbar^2/m^* = E_{F1} - E_{F2} = (n_1 - n_2)\pi\hbar^2/m^* \quad (1)$$

where C_T is the capacitance per unit area between the top control gate and the top QW, m^* is the electron effective mass, and n_1 and n_2 are the electron densities in the two QWs. In the above, we have assumed that the in-plane resistances are negligible in comparison to the tunneling resistance.

The experimentally measured devices were processed from modulation-doped GaAs/$Al_{0.3}Ga_{0.7}As$ DQW heterostructures grown by molecular beam epitaxy. (The stop etch layers had higher Al compositions, as discussed previously.) The GaAs QW widths ranged from 120 to 200 Å, and the $Al_{0.3}Ga_{0.7}As$ barriers between them had a thickness ranging from 70 to 125 Å. Details of the samples are provided in Table 1, where the electron densities in the QWs were obtained by Shubnikov-de Haas measurements at 0.3

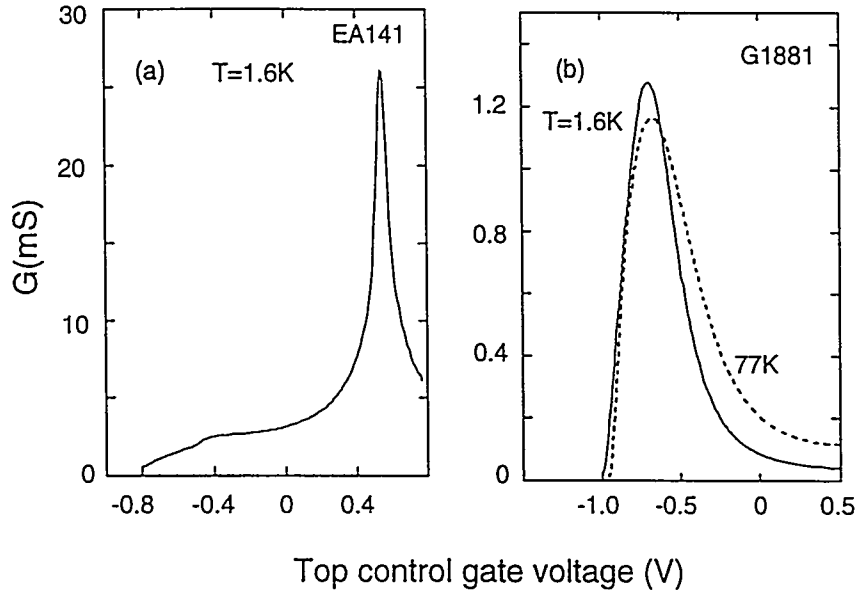

FIG. 4. (a) The small-signal tunnel conductance of (a) DELTT EA141 at 1.6 K, and of (b) DELTT G1881 at 1.6 and 77 K.

K in the dark. We found that devices with a larger built-in Fermi energy difference $\Delta E_F = |E_{F1} - E_{F2}|$ exhibited higher temperature operation.

This is illustrated in Fig. 4, where the small-signal ($V_{SD} \equiv 0$) source-drain conductance G_{SD} vs. top control gate voltage V_{TC} is shown in Fig. 4 (a) for DELTT EA141 and Fig. 4 (b) for DELTT G1881. A strong tunneling resonance appears at 1.6 K, at least 10 times larger than the background conductance. In G1881, a relatively weak temperature dependence of the tunnel-conductance peak is observed, with a peak-to-background ratio of 20:1 at 1.6 K, 10:1 at 77 K and (not shown) 2:1 at 170 K, due to a relatively large built-in Fermi energy difference. By contrast, the peak in EA141 disappeared at ~20 K.

We also fabricated DELTTs from various pseudomorphic InGaAs/AlGaAs heterostructures. These structures, described in Table 2, had either (i) $In_{0.25}Ga_{0.75}As$ notches in the quantum wells, (ii) AlAs cladding layers at the edges of the quantum wells, or (iii) both. The addition of AlAs cladding layers increased the 2D confinement, but simultaneously reduced the electron density difference between the QWs, and hence the Fermi energy difference ΔE_F, resulting in a stronger temperature dependence. By contrast, when InGaAs notches were placed in the center of the QWs it was possible to increase ΔE substantially, resulting in a much weaker temperature dependence. Fig. 5 shows the normalized amplitude of the change in resistance between the resonant peak and the background, as a function of temperature. Structures with the largest ΔE_F exhibited the weakest temperature dependence.

	Sample	ΔE_F(mev)
Baseline	EA382	27.6
AlAs cladding	EA381	22.7
InGaAs notch	EA384	42.1
AlAs & InGaAs	EA385	34.0

TABLE 2. Samples testing use of InGaAs notches and AlAs cladding. ΔE_F is indicated.

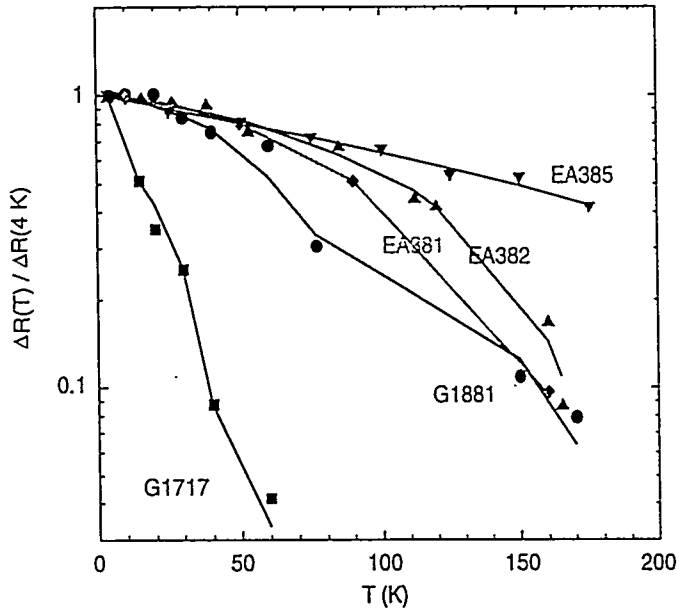

FIG. 5. Plot of tunnel conductance obtained from the pseudomorphic heterostructures .

We now turn to the non-equilibrium case of high source-drain bias. In Fig. 6 we plot the source-drain I-V curves for sample 1881 at 77 K for (a) several topgate voltages, and (b) several backgate voltages. The I-Vs are highly non-linear, with well-defined negative-differential-resistance (NDR) regions. With no control gates biased. the peak-to-valley ratio is ~2:1 with a peak current I_p of ~60 μA and peak voltages of V_p ~ 0.053V. The peak voltage is larger than the difference in the Fermi energies, ~21 meV. This is due to the fact that the in-plane 2DEG channel resistance and/or ohmic resistance is non-negligible in comparison with the tunneling resistance, resulting in an additional source-drain bias needed to bring the two subband energies into alignment.

Most importantly, in Fig. 6 we observe a strong modulation of the NDR region with gate voltage. As can be seen, the topgate and backgate modulate both Vp and Ip in an opposite manner or polarity. This is due to the fact that, at zero source-drain bias, application of a positive topgate bias increases the electron density in the top QW and pushes the subbands further away from the alignment condition, *decreasing* the tunneling current. By contrast, application of a positive backgate bias increases the electron density in the bottom QW and pushes the two subbands closer to the alignment condition, *increasing* the tunneling current. Thus the polarity of the transconductance can be selected depending on which gate – top or back – is biased. As described elsewhere [15], we have constructed circuits with two DELTTs in series, and applied the same input voltage to the topgate of one DELTT and the backgate of the other. This circuit exhibited complementary switching behavior, similar to that of a Si CMOS circuit, except that in the DELTT case the circuit was *unipolar*.

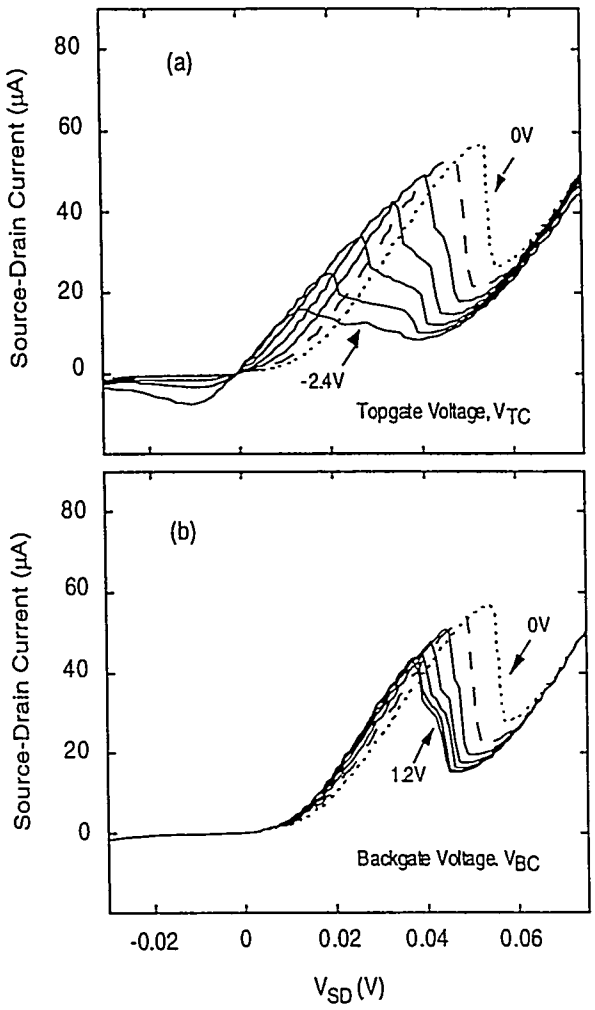

FIG. 6. Source-Drain I-Vs of DELTT G1881 measured at 77 K (a) for several values of top control gate voltage, and (b) for several values of backgate voltage.

SUMMARY

We have described a wafer thinning and flip-chip technique, EBASE, which allows backside gates to be placed in close proximity (less than one micron) to epitaxially grown semiconductor layers of submicron thickness. The backgates can be aligned with submicron accuracy to frontside gates deposited on the same structure. Indeed, due to the extreme thinness of the epitaxial layers, electron-beam defined sub-micron features can be placed on both sides of the structure and mutually aligned using the same alignment mark. Using the EBASE technique, we have fabricated novel planar resonant tunneling

transistors, the double electron tunneling transistor or DELTT, based on gate-controlled 2D-2D tunneling. In these structures the source and drain terminals selectively contact each 2DEG and Schottky gates are used to modulate the 2D – 2D inter-QW tunneling currents. Electrical characterization of fabricated DELTTs showed strong negative differential resistance up to 170 K, with peak-to-valley ratios reaching 20:1 below 1K. Most importantly, both the amplitude and voltage position of the resonant tunneling current peaks are controllable by gate voltage over a wide range.

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