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ENHANCED EDOT X SYSTEM

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ENHANCED EDOTX DYNAMIC RANGE

Executive Summary:
The EdotX data acquisition equipment was originally developed by Los Alamos National Laboratory (LANL) and has been successfully utilized in scientific experiments that support the Department of Energy's NNSA programs. The capability of EdotX would be improved by increasing the instrument's dynamic range to expand the range of signals measurable by the device. The heart of the EdotX system is a two channel analog to digital (A/D) conversion card with two analog to digital converters tightly coupled to a field programmable gate array (FPGA). Signals are continually digitized by the A/D and processed by the FPGA. When the FPGA detects a trigger condition, the data are transferred using direct memory access to the host computer memory, which in turn saves the data to disk. The original design utilizes a single A/D channel for data acquisition.

Our task was to increase the dynamic range of the system by enabling the second A/D channel, allowing the simultaneous acquisition of the original A/D channel and the additional second A/D channel. The input signal would be fed to the original channel and to the second channel with the second channel input being attenuated. When a signal hits the maximum range of the first channel, the data from the second channel, which is attenuated, are then used. Because both A/D's acquire data simultaneously, they may be used as a single expanded dynamic range channel.

Work began on the design and, as small changes were implemented to the FPGA design, it was noted that direct memory access (DMA) issues were appearing. Bad data, no data, or even system crashes occurred after making minimal modifications to the code and enabling the second DMA channel. The board is designed to utilize a separate DMA channel for each A/D and the problems appeared to be tied to the second A/D channel being enabled. The manufacturer of the A/D card was contacted. After working with the manufacturer for several weeks, they believed that a hardware failure had occurred on the board. They requested that the board be returned to them for evaluation and possible repair. The decision that the board was malfunctioning was based on the board not functioning correctly using test programs provided by the manufacturer. The board was returned to the manufacturer who then determined that the test program that they provided did not work. The board was declared operational by the manufacturer and returned. The original issue with DMA errors was not addressed by the manufacturer. Although the manufacturer worked with us at trying to resolve the issues with the DMA, the issues have not been resolved and a functioning two channel design has not been produced. Due to the age of the design, limited production lifetime of the A/D card, and unresolved issues with the DMA, it is not viable to use the second channel on this board to expand the dynamic range of the EdotX system.

System Description

The EdotX system utilizes a specialized card hosted by a computer running Linux Fedora Core 2. The card features two A/D channels, static RAM, FPGA, and PCI bridge. The

FPGA has numerous functions on the board. It provides the control logic and timing to the A/D converters and Static RAM, local bus interface to the PCI bridge, and contains the DMA engine. The DMA engine is provided as a "black box" precompiled unit, for which the user has neither access to implementation details nor the ability to modify the unit. The remaining portion of the FPGA is available for the user to customize. The trigger detection algorithms are implemented in the user section of the FPGA.

Development Phase 1:
Hardware/Software Compatibility
LANL provided the source code and operational binaries for the EdotX FPGA and source code for the Linux programs that comprise the EdotX system. Using this as a starting point, the provided FPGA binary was loaded and all Linux software was compiled and installed. The system was functionally verified to insure proper operation prior to beginning modifications to hardware and software.

Verification of FPGA Build Capability
The FPGA provided on the A/D card is a Xilinx Virtex II. The source code provided by LANL is written in VHDL. To transform the source code into a downloadable binary for the FPGA, a specialized software package is used. Due to the size of the design and the complexity of the original code, a full build of the part takes more than one hour to execute. The original FPGA source code was built into a downloadable binary for the FPGA. The newly built code was then functionally verified to ensure proper operation of the EdotX. At this point the source files and hardware were known to be functional and a valid starting point for adding the second A/D channel.

Development Phase 2:
Code Analysis
The LANL provided FPGA code was analyzed to determine the steps required to enable the second A/D channel. The board design is such that each A/D channel has a separately dedicated DMA channel used to move data from the on board static RAM to the host CPU system memory. The original single channel source code utilized the first DMA channel per board design. From the code analysis, it was determined that the upgrade plan would be performed in two steps. The first step would enable the second DMA channel and modify the Linux software to handle the channel. The second step would enable the second A/D channel.

Implementation
A simple approach to enabling and testing the second DMA channel was used. The FPGA data source for DMA channel two was a simple counter setup to increment on each transfer of data from the A/D card to the host memory. Utilizing a counter ensured that the DMA operation could not under-run. Additionally, it provides incrementing data that is easily verified to ensure that no data loss is occurring. The trigger for DMA operations was left unmodified, so that whenever DMA channel one would transfer data, so would DMA channel two. The Linux programs were modified to handle the extra channel. The FPGA code was built and downloaded. Testing was initiated and problems

were found. DMA channel two was not transferring the data correctly to the host system memory. The modifications to the code were re-examined and no explanation for the DMA errors could be determined.

Resolving the DMA Errors

Having exhausted all ideas on how to resolve the DMA issue, the A/D board manufacturer was contacted about it. They would not discuss any problems that were related to any FPGA code that was not directly from them. They requested that we try the demonstration code provided on the CD that shipped with the card. The demonstration code comprised both a FPGA binary and Linux software. This approach was tried and also demonstrated DMA problems. The manufacturer then suggested that we download both the FPGA binary and the Linux software from their website. The code was downloaded and tested. Problems still occurred. The manufacturer would make a suggested code change and it would be implemented by us. Problems persisted, and suggestions and test results went back and forth with the manufacturer for several weeks. Finally, the manufacturer requested that the board be returned for testing and possible repair because it looked like the board was faulty. The board was returned to the manufacturer who determined that the test software that they provided was faulty and the board was functioning correctly. This did not address the problems that were originally seen after enabling the second DMA channel. The second channel DMA issue remains unresolved.

Path Forward

There are numerous issues that relate to a path forward for the existing EdotX system hardware platform. The DMA for the second channel does not work correctly and attempts to work with the manufacturer to resolve this issue have not been successful. Source code for the malfunctioning DMA engine module is not available and, even if it were, it would be cost prohibitive to attempt a re-write or repair. The Linux drivers provided for the card are for very old versions of Linux. The ability to purchase new/replacement hardware that is compatible with the supported version of Linux will diminish with time. If this hardware platform is relied on then it is possible that the operating system required for the A/D card drivers will not install on the new host platform. Lastly the projected manufacture life of the board is limited. The recommended path forward is to use a different, newer board that has improved long term support. The EdotX units can still operate in their original configuration, albeit without the expanded dynamic range.

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