Mold Heating and Cooling Microprocessor Conversion

Kansas City Division

D. P. Hoffman

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Final Report

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Abstract

Conversion of the microprocessors and software for the Mold Heating and Cooling (MHAC) pump package control systems was initiated to allow required system enhancements and provide data communications capabilities with the Plastics Information and Control System (PICS). The existing microprocessor-based control systems for the pump packages use an Intel 8088-based microprocessor board with a maximum of 64 Kbytes of program memory. The requirements for the system conversion were developed, and hardware has been selected to allow maximum reuse of existing hardware and software while providing the required additional capabilities and capacity. The new hardware will incorporate an Intel 80286-based microprocessor board with an 80287 math coprocessor; the system includes additional memory, I/O, and RS232 communication ports.

Summary

Mold Heating and Cooling (MHAC) controllers are used by the Plastics Molding and Machining Department and the Filled Elastomers Department at AlliedSignal Inc., Kansas City Division (KCD). Conversion of the microprocessor hardware and software for the MHAC pump package controllers was required to provide system enhancements and data communications capabilities with the Process Information and Control System (PICS).

The existing microprocessor-based controllers for the pump packages use an Intel 8088-based microprocessor board with a maximum program memory of 64 Kbytes. The new system hardware has been designed to use an Intel 80286-based microprocessor board and includes additional memory, I/O, and RS232 communications ports.

The conversion constraints for the redesign included the requirement to reuse as much of the existing hardware as possible. To reuse the existing software, basic system interrupt and addressing architectures were required to be maintained. The existing control system hardware uses a Multibus architecture. The hardware selected for the conversion will allow the Multibus chassis, bubble memory board, analog-to-digital converter board, and the digital-to-analog converter board to be reused in the new configuration.

The converted microprocessor control systems will be programmed using newer Intel development system tools including an in-circuit emulator, cross compilers, and cross assemblers which will run on a standard PC as the development platform. Software changes required for the converted hardware were to be minimized by the selection of compatible hardware. The new configuration will also provide sufficient capability for future expansion. The work to interchange the hardware and modify the software is outside the scope of this report.

This report covers the design and development work performed up to the procurement of the conversion computer hardware. The hardware installation and the software upgrades are addressed in the Future Work section.

Discussion

Scope and Purpose

The purpose of this project was to identify and develop the upgrade hardware and software development tools necessary for conversion of the MHAC pump package controllers to achieve a newer, faster control system with more memory, I/O, and communications capacities. The conversion was required to allow system enhancements and to allow the MHAC controllers to communicate with PICS. The scope of this project was to address the hardware design and development requirements for the conversion and to address the requirements for a newer software and hardware development platform for enhancing the software to conform to the new hardware.

Prior Work

Prior work included formulating the design criteria and selecting the hardware for the current Mold Heating and Cooling System; designing, coding, and debugging the software system; and developing of the current microprocessor controller.[1]

Activity

Existing Hardware Description

Figure 1 illustrates the overall architecture of the MHAC pump package controllers showing the major components. The arrows indicate data flow paths and control signal flow paths through the major components.

The MHAC system provides temperature-controlled fluid which circulates through channels in plastic molds to heat and cool the molds and material to a specified recipe. The original control system was designed and developed by Plastic Products Engineering at KCD in the early 1980s using the Multibus computer bus standard, an Intel iSBC 80/24 micro-processor board, and various interface, I/O, and memory components. The existing system is housed in a Multibus chassis inside a 19-inch rack mount control cabinet. The existing control systems were fabricated and assembled by Custom Control of Merriam, KS. Figure 2 shows the layout of the microprocessor control system inside the Intel model 660 Multibus chassis.

Hardware Constraints

The MHAC microprocessor control software and hardware are designed as a real time, interrupt-driven system. The system must perform certain control functions on a fixed schedule of clock interrupts and must respond on demand to other interrupts internal or external to the system. Table 1 shows the interrupts used in the original system.

The upgraded system was constrained to reuse as much of the existing hardware and software as possible while still allowing for the required enhancements.

Hardware requirements of the upgraded system to support the existing functions of the MHAC control system include the following:

1. One serial RS232C communications port for communication with the user's terminal;

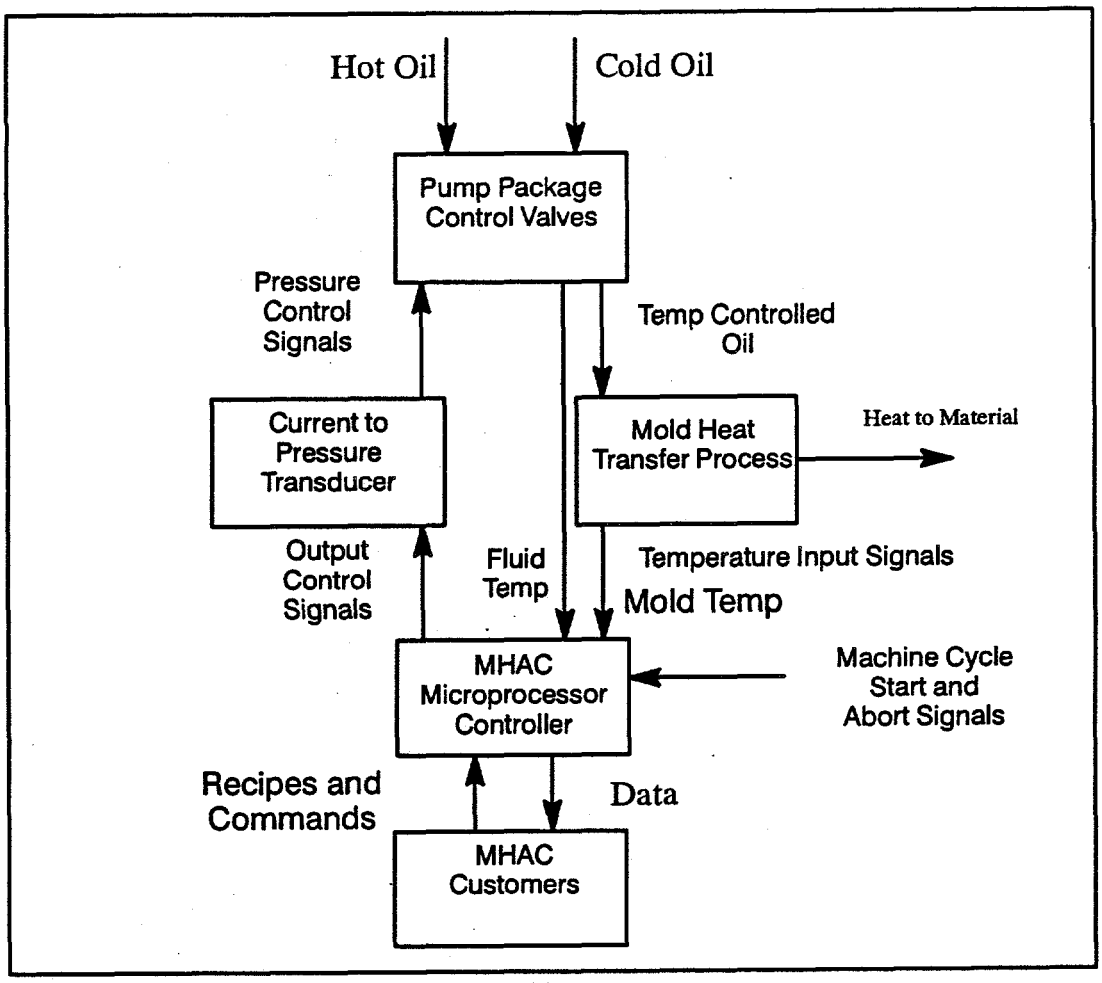

Figure 1. MHAC Pump Package Control Block Diagram

Table 1. Interrupt Structure

Level	Description
0	Emergency Stop
1	Clock
2	Analog-to-Digital Conversion
3	Not Used
4	Scheduler
5	Receive From CRT
6	Collision Handler

2. Two digital I/O lines for input and output of the start and stop signals from the pump package; and

3. An SBX connector for connecting the iSBX 311 Analog-to-Digital Converter.

The following were required to upgrade the system for interface with PICS:

4. An additional serial RS232C communications port to transmit process data and recipe information to PICS and receive commands and recipe information from PICS;

5. Additional program memory capacity to support the additional software

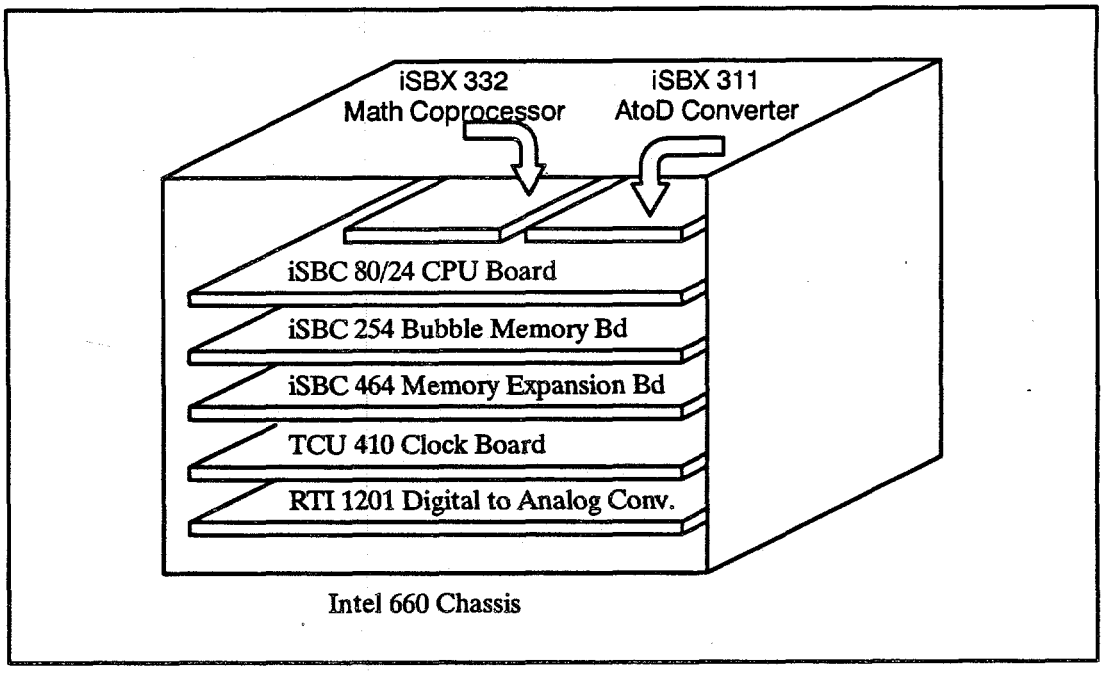

Figure 2. Original MHAC Microprocessor Hardware

required to interface with PICS and support the PICS-related functions;

6. Additional data memory capacity to allow for temporary storage of process data until it is transmitted to PICS; and

7. Increased CPU speed to support the PICS interface functions while not jeopardizing the real-time temperature control response of the system.

Support of planned enhancements to the MHAC software required

8. A third serial communications port for communication with a serial printer to be optionally available for hard-copy output from the MHAC system.

Software Constraints

The software for the upgraded system must, for the most part, reuse the software of the existing system. The cost and time invested in the existing software could not be easily replaced. The existing software is written using the PLM programming language and the ASM80 assembly language. The new system and the new development tools must be compatible with, and allow modification of, the existing code and must allow addition of new code functions and modules.

The existing code is delivered to each MHAC controller on UV erasable programmable read only memory (PROM) chips using a PROM programmer. The development environment of the original software and hardware was a Series II Intel development system. The Series II development system in Plastic Products Engineering has been upgraded at various times until it was equivalent in capability to the slightly newer Series III development systems from Intel. Both of these models of dedicated development systems have been obsolete and unsupported by Intel since the late 1980s. A new development environment was needed for the required software changes and enhancements. The

new development system and tools, however, must be able to use the existing PLM and ASM80 codes and allow the software to be delivered on PROMs.

Hardware Design and Procurement

Based on the hardware and software constraints on the new control system, a new configuration was developed and hardware was procured for the upgrade. Appendix A itemizes the original, reused, and new hardware for the control system conversion.

iSBC 286/10A Single Board Computer

The iSBC 286/10A Single Board Computer was selected to replace the SBC 80/24 single board computer and the iSBX 322 hardware math board. The board is compatible with the existing Intel 660 chassis and Multibus backplane and will support the additional memory required for the upgrade. Figure 3 shows the iSBC 286/10A Single Board Computer. Figure 4 shows the component layout of the iSBC 286/10A Single Board Computer. The iSBC 286/10A includes the following features:

- Multibus and SBX compatible single board computer;
- iAPX 286 CPU with protected mode or real mode, and extended iAPX 86, 88 instruction set;
- Four JEDEC sockets for local memory up to 128 kB for program memory;
- Four JEDEC sockets for dual-port memory up to 256 kB for data memory;
- Two programmable serial I/O interfaces;
- Acceptance of 80287 Numeric Processor;
- Two iSBX bus interface connectors for I/O expansion to support reuse of the iSBX 311 Analog-to-Digital Converter;
- Centronics-compatible parallel I/O printer interface;
- Fifteen levels of vectored interrupt control; and
- A 4.9 MHz or 8.0 MHz (default) system clock speed.

iSBC 517 I/O Expansion Board

The iSBC 517 I/O Expansion Board was selected to support the digital I/O from the SBC 80/24 and to provide the additional serial communications port. Figure 5 shows the functional block diagram for the iSBC 517. The features of the iSBC 517 are listed below:

- Two Intel 8255 Programmable Peripheral Interfaces;
- Forty-eight configurable I/O lines;
- Intel 8251 USART for Asynchronous/Synchronous serial communications; and
- Eight-level maskable interrupt feature.

Memory

To provide the required program memory, the Intel 27256, 256 kB (32 kB x 8) UV erasable PROM was selected. The 27256 will be programmed using the PROM programmer with the MHAC code. The SBC 286/10A with four 27256s will have two times the program capacity of the original 80/24 and the SBC 464 memory expansion board.

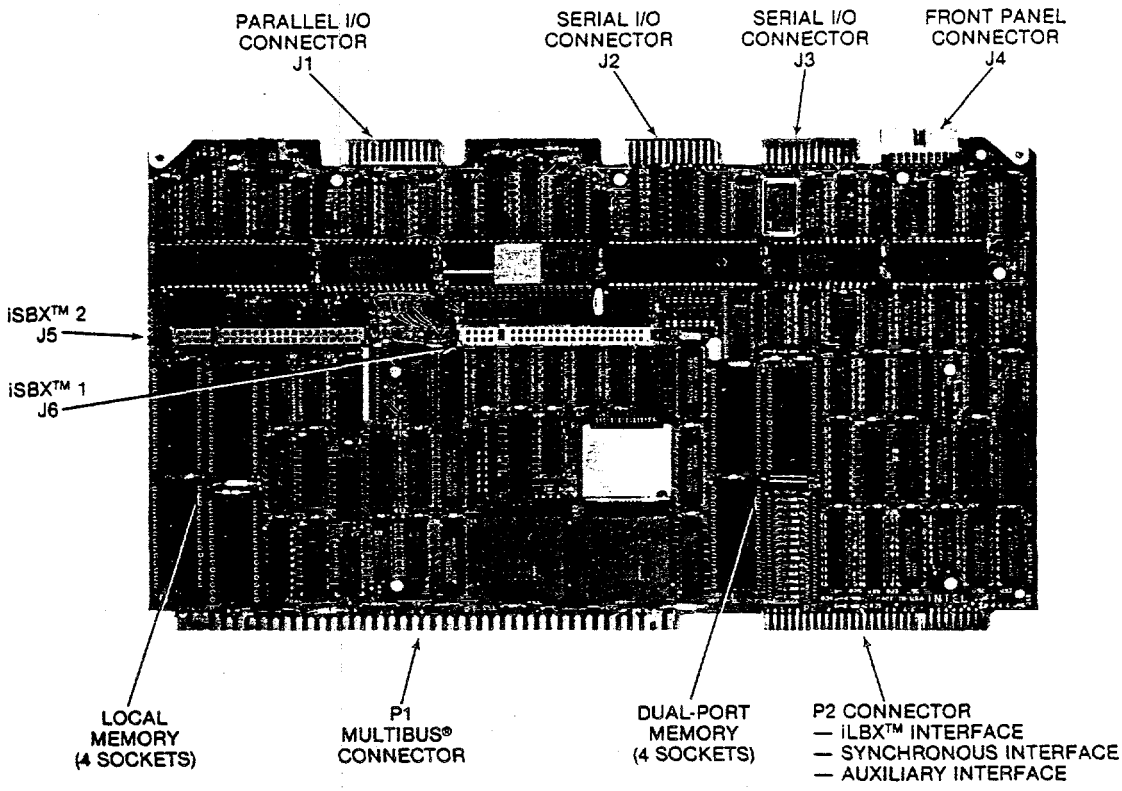

Figure 3. iSBC 286/10A

To provide the required data memory, the Vitelic 32 kB x 8 CMOS Static RAM was selected. A maximum of 256 kB of RAM will be available for data memory in the upgraded system.

Development Environment Upgrade

A PC-based development system was developed and with an Intel I2ICE in-circuit emulator, a PROM programmer, a PLM compiler, an ASM assembler, and support software for development of the required code. The new development system is capable of supporting the existing and new hardware and software as well as software developed for other control systems at KCD. Appendix B details the software and hardware procured for the development system PC.

Accomplishments

This project identified and developed the upgrade hardware and software development tools necessary for conversion of the MHAC pump package controllers to a newer, faster control system with more memory, I/O, and communications capacities. A new configuration was developed and hardware was procured for the upgrade, based on the hardware and software constraints on the new control system.

The iSBC 286/10A Single Board Computer was selected to replace the SBC 80/24 single board computer and the iSBX 322 hardware math board. The iSBC 517 I/O Expansion Board was selected to support the digital I/O from the SBC 80/24 and to provide the additional serial communications port. The Intel 27256 UV Erasable PROM was selected to provide

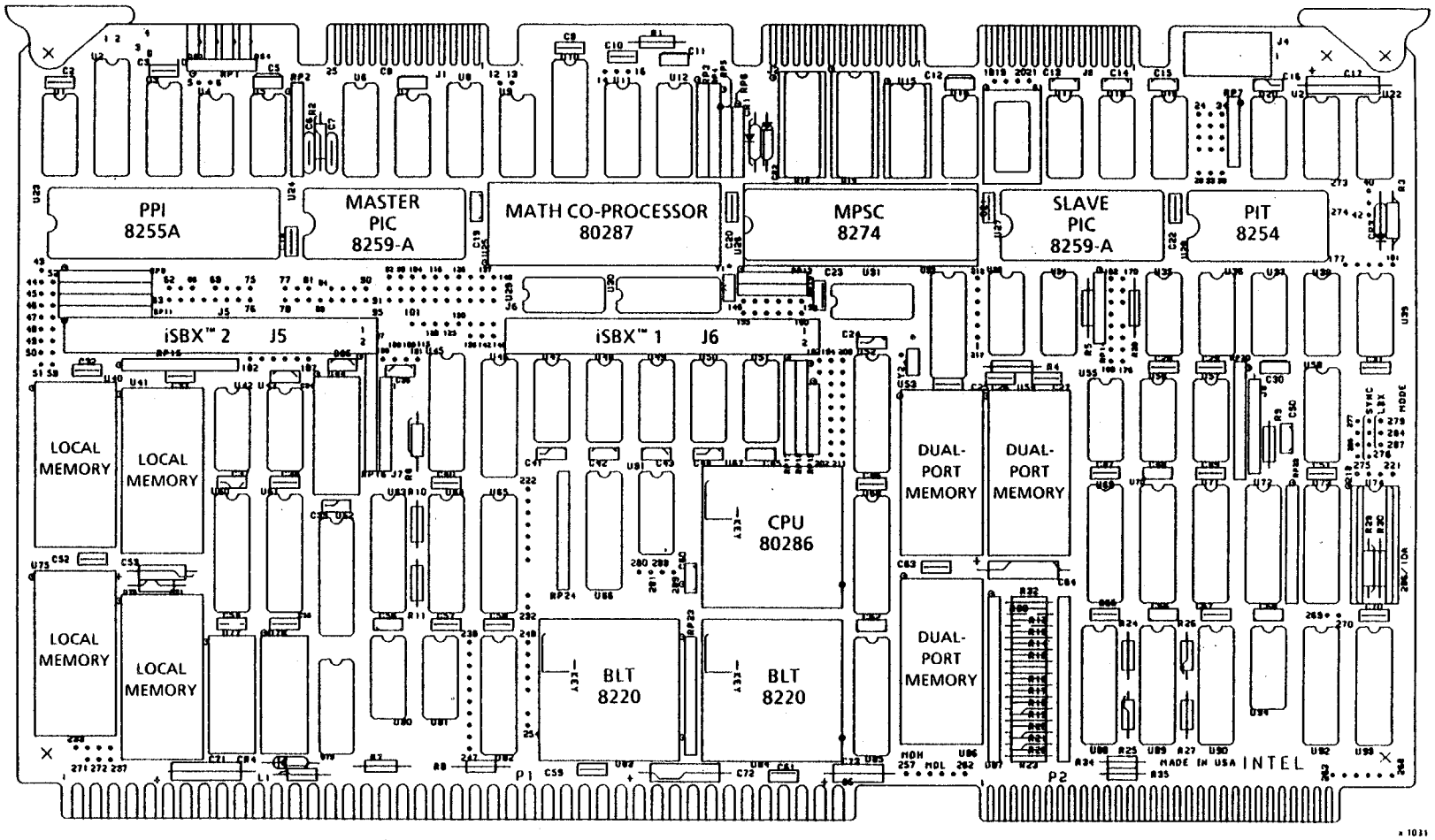

Figure 4. iSBC 286/10A Board Layout

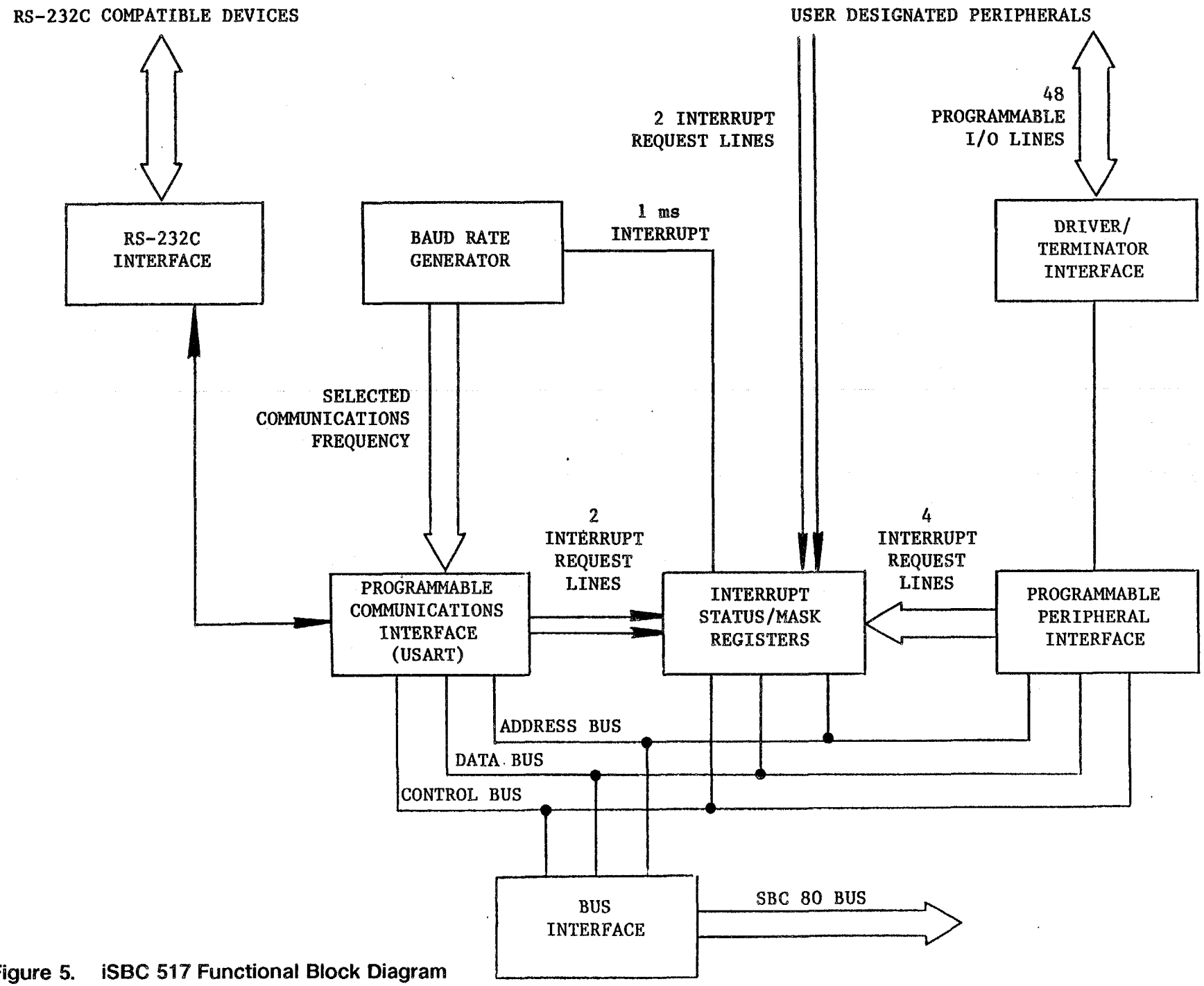

Figure 5. iSBC 517 Functional Block Diagram

the required program memory. The Vitelic 32 kB x 8 CMOS Static RAM was chosen to provide the required data memory. A maximum of 256 Kbytes of RAM will be available for data memory in the upgraded system.

Future Work

Future work will include modifications to the PLM code to accommodate the new hardware and to implement the planned enhancements to the software.

Once the software and hardware have been integrated and fully tested, the MHAC microprocessor control systems must be retrofitted with the new computer boards. Minimal modifications to existing wiring are expected because of the compatibility of the new and original microprocessor boards.

Reference

[1] R. H. Floersch, Microprocessor Controller for Mold Heating and Cooling (Final Report). Kansas City Division: BDX-613-3477 (Available from NTIS), April 1986.

Appendix A

Hardware Components

Existing Hardware:

Intel iSBC 80/24 Single Board Computer

Intel iSBX 332 Hardware Math Board

Intel iSBX 311 Analog-to-Digital Converter

Intel iSBC 464 Memory Expansion Board

iSBC 254 Bubble Memory Board

TCU 410 Clock Board

RTI 1201 Digital-to-Analog Converter Board

Reused Hardware:

Intel Model 660 Chassis

Intel iSBX 311 Analog-to-Digital Converter

iSBC 254 Bubble Memory Board

TCU 410 Clock Board

RTI 1201 Digital-to-Analog Converter Board

Hardware Procurement:

Intel iSBC 286/10A Single Board Computer

Intel 80287 Math Coprocessor Chip

Intel iSBC 517 I/O Expansion Board

Intel 27256, 32 kB x 8 EPROM (four per system)

Vitelic 32 kB x 8 CMOS Static RAM (four per system)

Appendix B

Development Tools

Development Tools Procurement

DESCRIPTION	PART NUMBER
Intel I2ICE System 8086/8088 Support kit	PIII010KITB
Intel I2ICE Interface Module for PC	III520AT954D
Intel 186/188 Emulation Module for I2ICE	PIII186A912B
Intel PROM Programmer	PIUP201
Intel PROM Personality Module	iUPF27128
Intel PROM Personality Module	iUPFAST27K
Intel 8086 Program Application Kit	D86PAK86NL
Intel 8086 PLM Compiler	D86PLM86NL