A Voltage Controlled Oscillator for a Phase-Locked Loop Frequency Synthesizer in a Silicon-on-Sapphire Process.

SEAN M. GARRISON

Bachelor of Science, Electrical Engineering,

University of Missouri-Rolla, 2004

Submitted to the Department of Electrical Engineering and Computer Science

and the Faculty of the Graduate School of the University of Kansas

in partial fulfillment of the requirements for the degree of Master of Science.

Signature: _____

Dr. Chris Allen (Chair)

Signature: _____

Dr. Shannon Blunt

Signature: _____

Dr. Jim Stiles

Date of Defense: May 21th, 2009

The Thesis Committee for Sean Garrison certifies

That this is the approved Version of the following thesis:

A Voltage Controlled Oscillator for a Phase-Locked Loop Frequency Synthesizer in a Silicon-on-Sapphire Process

Signature: _____

Dr. Chris Allen (Chair)

Signature: _____

Dr. Shannon Blunt

Signature: _____

Dr. Jim Stiles

Date approved: _____

ABSTRACT

Engineers from a government-owned engineering and manufacturing facility were contracted by government-owned research laboratory to design and build an S-band telemetry transmitter using Radio Frequency Integrated Circuit (RFIC) technology packaged in a Low-Temperature Co-fired Ceramic (LTCC) Multi-Chip Module. The integrated circuit technology chosen for the Phase-Locked Loop Frequency Synthesizer portion of the telemetry transmitter was a 0.25 um CMOS process that utilizes a sapphire substrate and is fabricated by Peregrine Semiconductor corporation. This thesis work details the design of the Voltage Controlled Oscillator (VCO) portion of the PLL frequency synthesizer and constitutes an fully integrated VCO core circuit and a high-isolation buffer amplifier.

The high-isolation buffer amplifier was designed to provide 16 dB of gain for 2200-3495 MHz as well as 60 dB of isolation for the oscillator core to provide immunity to frequency pulling due to RF load mismatch. Actual measurements of the amplifier gain and isolation showed the gain was approximately 5 dB lower than the simulated gain when all bond-wire and test substrate parasitics were taken into account. The isolation measurements were shown to be 28 dB at the high end of the frequency band but the measurement was more than likely compromised due to the aforementioned bond-wire and test substrate parasitics.

The S-band oscillator discussed in this work was designed to operate over a frequency range of 2200 to 2300 MHz with a minimum output power of 0 dBm with a phase-noise of -92 dBc/Hz at a 100 kHz offset from the carrier. The tuning range was measured to be from 2215 MHz to 2330 MHz with a minimum output power of -7 dBm over the measured frequency range. A phase-noise of -90 dBc was measured at a 100 kHz offset from the carrier.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

ACKNOWLEDGEMENTS

I would like to thank my advisor, Dr Chris Allen, for providing my design team with guidance and support in the early stages of the Phase-Locked Loop design process. He also provided me with much needed guidance during the final stages of writing my thesis and for this I am sincerely grateful. I would also like to thank Dr. Jim Stiles and Dr. Shannon Blunt for serving on my thesis committee. I have relied on knowledge gained from the RF and Microwave engineering courses taught by both of them in-order to work on this project and I would like to thank them for this. I am also deeply indebted to the engineers who worked on the project's design team, namely the project leader, Frank Smith. He gave me the opportunity to expand my intellectual horizons by working on this project and he willingly shared his knowledge of RF design on a daily basis; I will forever be grateful for this. Finally, I would like to thank my wife, Jennifer, for all of her encouragement and support throughout my writing of this thesis. Without her willingness to sacrifice her time and energy, I would never have been able to complete this thesis.

1. INTRODUCTION

1.1. Research Motivation and Background

Starting in 2007, engineers from a government-owned manufacturing and engineering facility were contracted by a government-owned research and development lab to provide a high-efficiency telemetry transmitter using Radio Frequency Integrated Circuit (RFIC) technology that utilized a Low Temperature Co-fired Ceramic (LTCC) package. The transmitter operates in the S-band frequency range (2200MHz to 2300 MHz). The purpose of this particular project is to research and design the associated RF circuits for a highly integrated phase-locked loop frequency synthesizer.

1.2. Thesis Description

This thesis covers the research, design, testing and redesign of a high-isolation, buffer amplifier and a voltage-controlled oscillator. The oscillator is intended to operate at S-band frequency range (2200 MHz to 2300 MHz). The remainder of the phase-locked loop circuitry for the frequency synthesizer was designed by other engineers at Honeywell FM&T and will only be mentioned in-passing. This thesis focuses exclusively on the design, testing and redesign of the VCO and buffer amplifier circuitry for the synthesizers. Figure 1.1 shows the block diagram of the phase-locked loop synthesizer with a red box around each circuit researched and designed in this project.

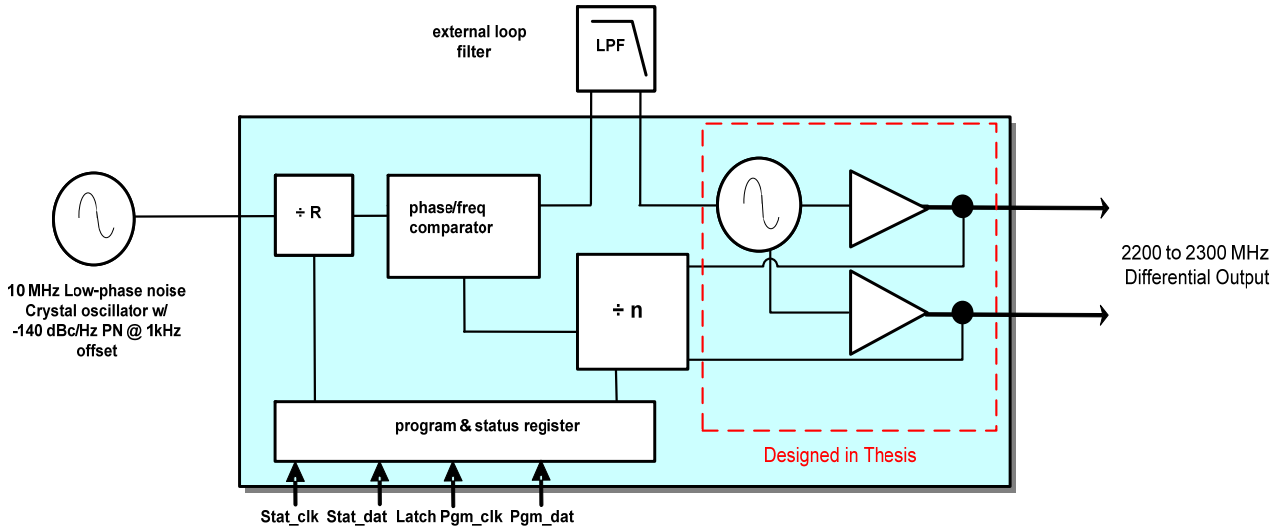


Figure 1.1: Telemetry LO phase-locked loop synthesizer block diagram

1.3. Thesis Organization

The remainder of this thesis consists of a brief description of the Peregrine Semiconductor GC process as well as the design and testing of the high-isolation buffer amplifier and voltage-controlled oscillator. Following these chapters, a chapter on redesigning the VCO components and a conclusion chapter summarizes the results and highlights of the research performed .

1.4. Peregrine GC Process Description

The foundry process that was chosen for this project was Peregrine Semiconductor's GC process. This process is a 3-metal layer, 1 poly layer, 0.25 µm channel length, Complementary Metal Oxide Semiconductor (CMOS) process that utilizes a highly

resistive sapphire substrate in-lieu of the more common bulk silicon substrate. The top metal layer is thick metal layer that is used for creating high-Q passive components such as inductors and metal-insulator-metal (MIM) capacitors. The sapphire substrate's high resistivity has several distinct advantages when compared to a bulk silicon substrate. These advantages include high isolation between digital and analog RF circuits and low-leakage current for transistors. The substrates high resistivity also reduces parallel substrate capacitance which has the effect of increasing the Q of integrated inductors. All of these process features make the Peregrine GC process very attractive for mixed signal applications and thus is the reason this process was used for the phase-locked loop synthesizer. Figure 1.2 shows a publically available Peregrine process stack-up [1].

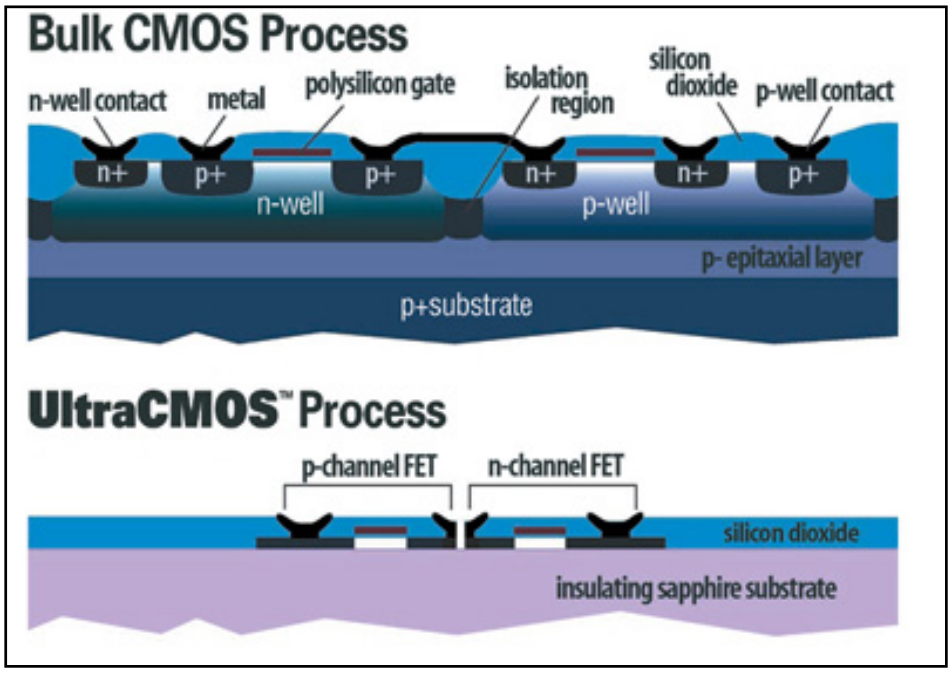


Figure 1.2: Peregrine Semiconductor's UltraCMOS Process Stack-up [1]

2. High-Isolation Buffer Amplifier

This chapter describes the design, layout and measurement of the high-isolation buffer amplifier. The amplifier was intended to be used by both the S-band telemetry oscillator and another PLL oscillator and was required to have a very high isolation (> 60 dB), operate over a wide frequency band (2.2 GHz to 3.5 GHz) and have enough gain to provide an output power of 0 dBm. The chapter begins with a brief list of specifications and gives a brief overview of the amplifier topology and design procedure. Finally, the measurements and results are presented and any differences in the measured versus simulated is discussed.

2.1. Buffer Amplifier Specifications

Frequency Range:	2200 MHz to 3495 MHz
RF Output Power:	0 dBm
Power Gain:	*
Isolation:	>60 dB
Supply Voltage:	2.5 V
Current Consumption:	< 40 mA
1- dB gain compression point:	> 1 dBm (referenced to the output power)
Output impedance	50 Ohms

*The gain value was not explicitly specified, the only requirement was for the gain to be high enough to amplify the oscillator output to 0 dBm.

2.2. Amplifier Design

The amplifier topology that was chosen was a multi-stage, common source topology with a simple resistor network to provide bias voltage for each stage. A multi-stage amplifier was chosen mainly due to the high isolation requirement. A common drain configuration (source-follower) for each amplifier stage was initially considered but early simulation showed that the common source amplifier has superior isolation. The common source amplifier has the added advantage of having higher than unity gain (unlike the source-follower amplifier)[2] which allows for attenuation to be added between the oscillator core and the amplifier for addition isolation.

The FET size for each amplifier stage was chosen to be relatively large (45 μm x 9 gate fingers) to handle the output power requirement of 0 dBm. The transconductance of the 45 μm x 9 FET fingers can be calculated from $G_m = 2K_n(V_{GSQ} - V_{TN})$ [1] where V_{GSQ} is the FET gate to source quiescent voltage and V_{TN} is the FET threshold voltage (0.45 V in the Peregrine GC process[2]). The conduction parameter, K_n, is derived from the formula, $K_n = \frac{W\mu_n\epsilon_{ox}}{2Lt_{ox}}$ [2] where W and L are the FET gate width and length (respectively), μ_n is the electron mobility in silicon and ε_{ox} and t_{ox} are the permeability and thickness of the oxide layer. For this particular process with a given FET gate width of 45 um x 9 fingers and a gate length of 0.25 um, the conduction parameter was calculated to be 363 mA/V^2. Using a 100 Ohm resistor in series with the MOSFET drain, the load line of the FET can be plotted and a quiescent drain voltage and current can be established for a given gate bias voltage.

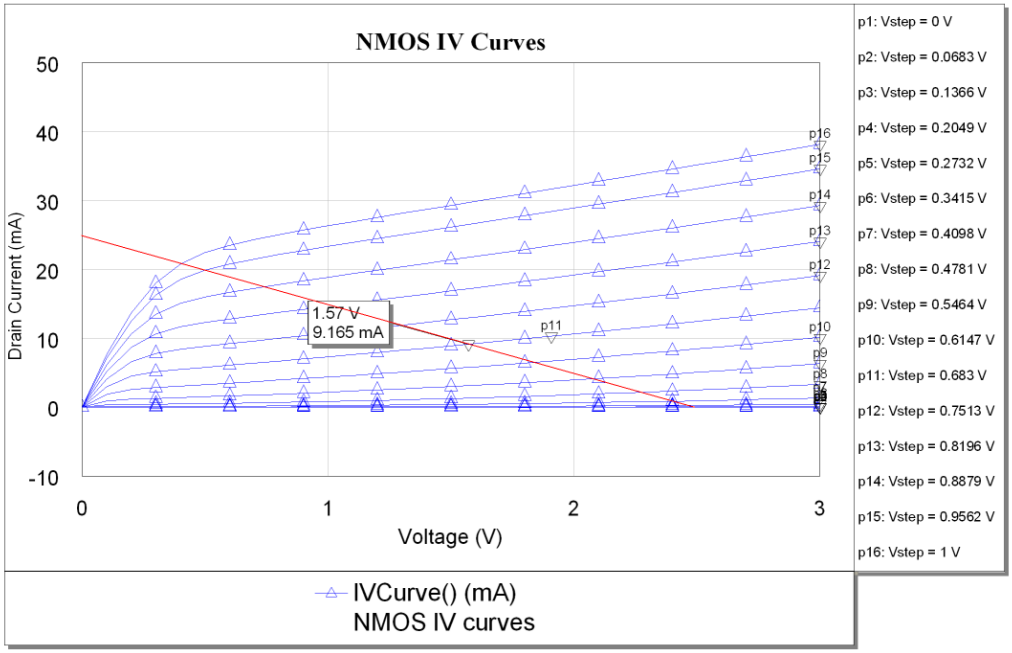


Fig 2.1: I-V curves and load line for a 45 x 9 um n-channel MOSFET with a 100 Ohm drain resistor

An examination of the 45 x 9 um MOSFET I-V curves reveal that for a quiescent gate-to-source voltage, V_{GSQ}, of 0.683 volts, the quiescent drain current, I_{DQ}, is 9.165 mA. A recalculation of the conduction parameter using the equation $K_n = \frac{I_{DQ}}{(V_{GSQ}-V_{TN})^2}$ [2] shows that the conduction parameter is actually 168.8 mA/V^2. The discrepancy between the simulated value and initial calculated value was likely due to an assumption made about electron mobility (a parameter not given the Peregrine design manual). The small signal voltage gain of the common source amplifier can be estimated from $A_v = -G_m(r_o // R_D)$ [2] where r_o is the MOSFET output

resistance and R_D is the series drain resistor. Using the new conduction parameter of 168.8 mA/V^2, the transconductance is calculated to be 78.8 mS. The output resistance of the MOSFET can be determined by examining the I-V curve since r_o is inversely proportional to the slope of the curve [2] which is 1.853 V/6.12 mA or 302.7 Ohms. This gives an initial calculation of the amplifier voltage gain to be equal to -0.078* (303.07 // 100) or -5.865 (the negative sign in-front of the gain value denotes a 180 degree shift in signal phase). However, this fairly simplistic gain calculation neglects several important intrinsic parasitic capacitances, such as the gate-to-source capacitance (C_{GS}), the gate-to-drain capacitance (C_{GD}) and the drain-to-source capacitance (C_{DS}). None of the previously mentioned parasitic capacitances can be conveniently calculated by hand but are included in the macro SPICE model where the small signal voltage gain can be simulated and compared with the earlier calculation.

The initial amplifier test circuit is configured like the circuit shown in figure 2.2, without the input and output coupling capacitors and with the input and output port impedances set to 1 MOhm. The results of the simulation (shown in figure 2.3) show that voltage gain of the amplifier is 3.9761 (at low frequencies) and 3.8878 at 3.5 GHz when the intrinsic parasitic capacitances are added. This amount of gain is adequate (as the buffer amplifier gain is not specified and only needs to be accurately predicted). Also, with the R_D set to 100 Ohms, the quiescent drain voltage is 1.509 V which allows a peak signal of 0.991 Vs (0.701 V_{RMS}) be output without clipping

which would give an output power of 9.8 mW (9.9 dBm) into a 50 Ohm load. This is well below the required output power of 0 dBm.

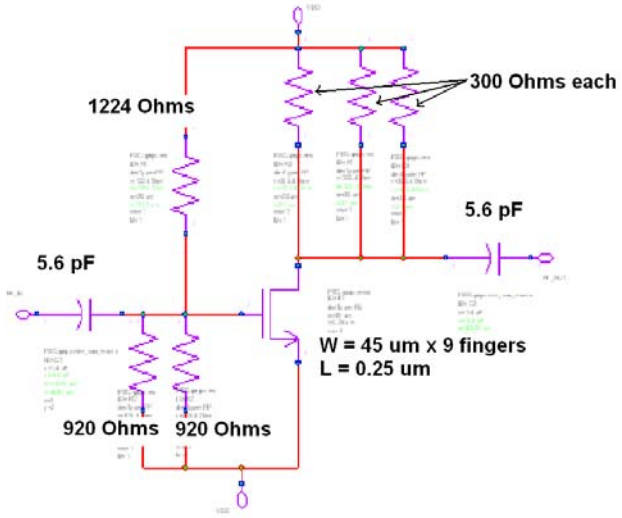


Fig 2.2: Single-stage amplifier circuit

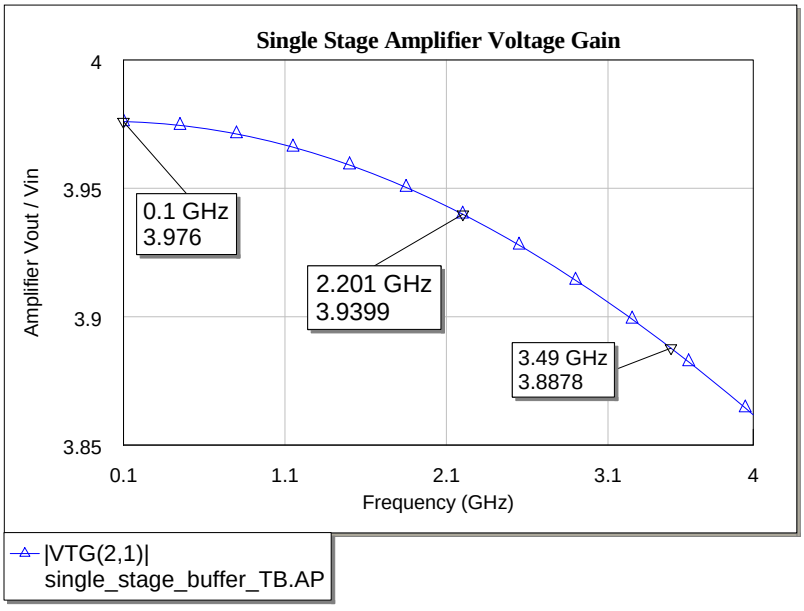


Figure 2.3: Single-stage amplifier voltage gain

Two 5.6 pF coupling capacitors were then added to the circuit and the amplifier S-parameters were simulated with the input and output port terminations set to 50 Ohms. The transducer power gain, G_T, is the ratio of power delivered to the load to the power available from the source [4]-[5]. For the special case that the source impedance and load impedance match, then $G_T = |S_{21}|^2$ [4] or if expressed as a logarithm, $20Log|S_{21}|$. The reverse transducer power gain (or isolation) is equal to $|S_{12}|^2$ assuming matching source and load impedances and can also be expressed by a logarithm as $20Log|S_{12}|$ [5]. Both of these amplifier parameters, along with the magnitude of the output reflection coefficient, were simulated and are shown in figure 2.4.

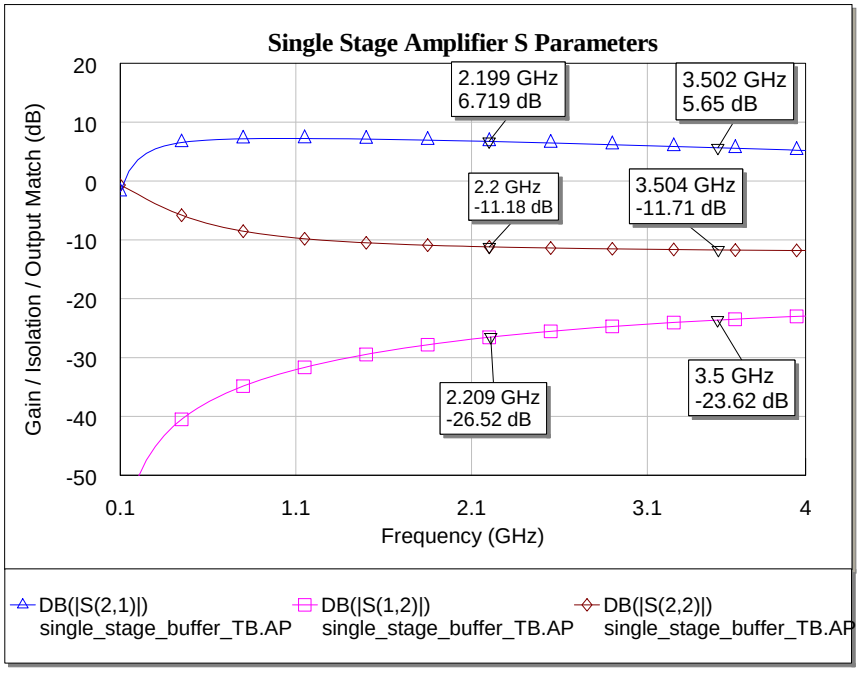


Figure 2.4: Single-stage amplifier S-parameters

This simulation shows that while the gain is adequate and varies less than 2 dB across the required bandwidth, the isolation is only -23.62 dB at the upper end of the band. In-order to meet the specified -60 dB of isolation, a total of 3 amplifiers, in this configuration, were needed. It is noteworthy to point out that the output reflection coefficient is better than -11 dB across the required bandwidth and, although no matching requirement was placed on the amplifier, a broadband output match is desirable. Figure 2.5 below, shows the completed 3 stage amplifier schematic complete with decoupling capacitors on the supply lines.

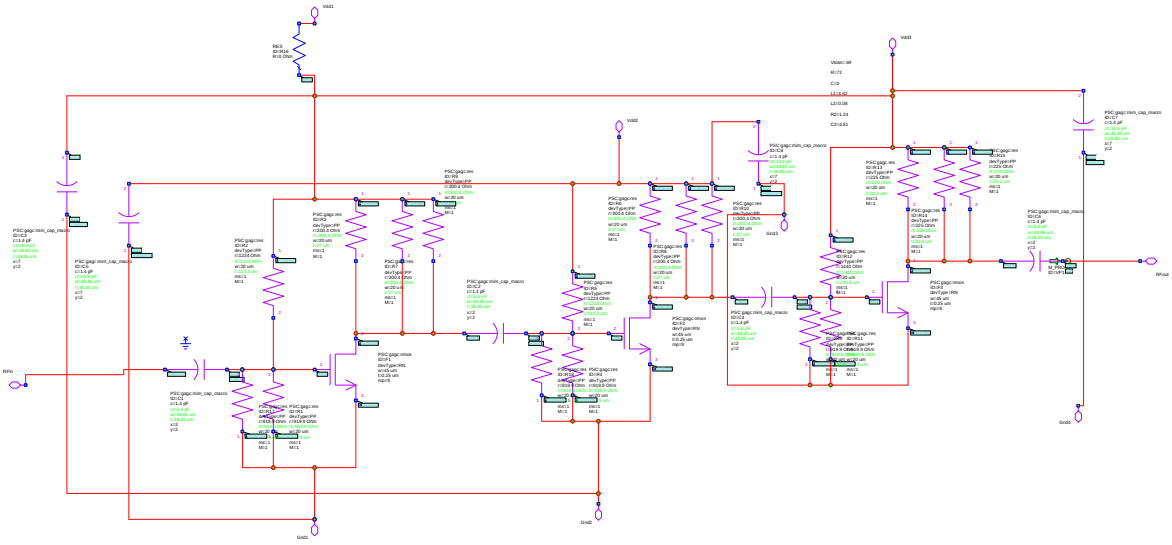


Figure 2.5: Complete, 3- stage, buffer amplifier schematic.

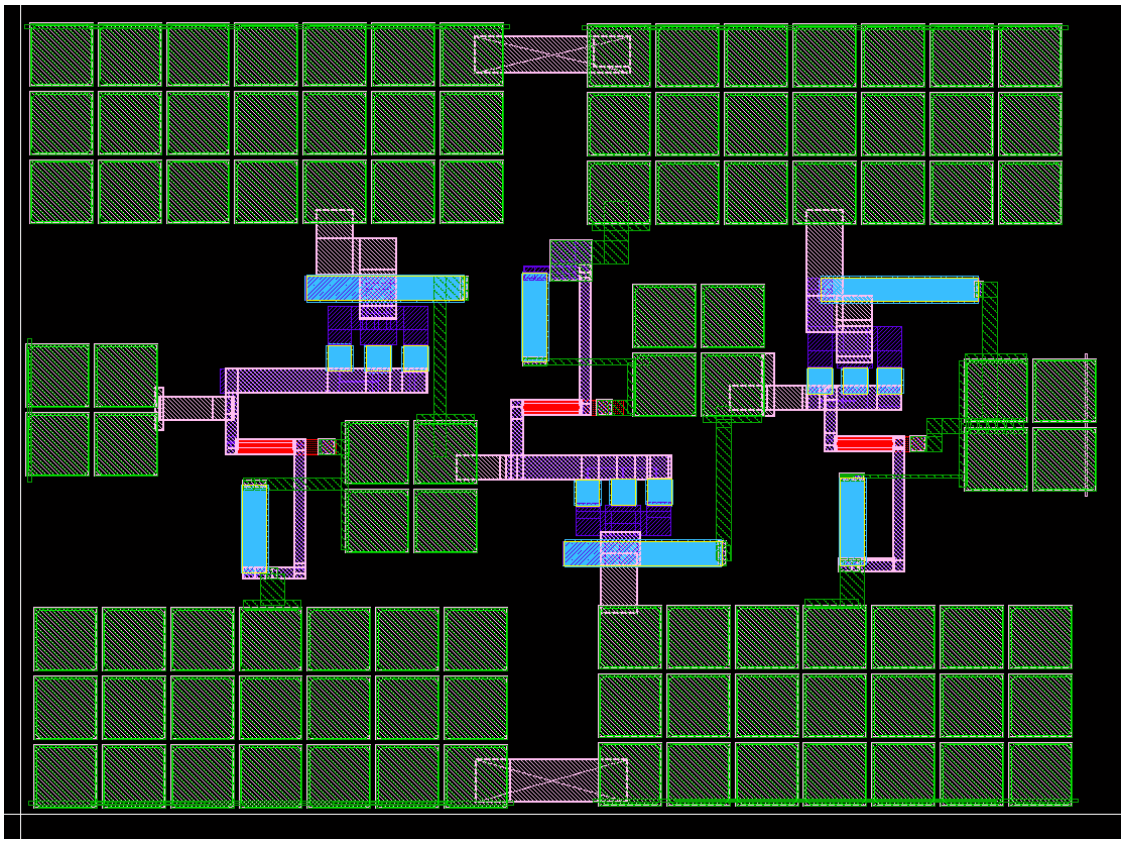


Figure 2.6: Complete, 3-stage, buffer amplifier layout

2.2.1. Amplifier Simulations

To ensure that the completed buffer amplifier meets all specifications, simulations of the transducer gain and isolation, DC current consumption and 1 dB compression point were performed across the required frequency band. The buffer amplifier's stability was simulated up to 20 GHz to ensure the amplifier will not oscillate at any frequency where the gain is greater than unity. All of the circuit simulations (along with schematic capture and layout) were performed using the CAD software Analog Office version 7.53 by Applied Wave Research[6].

The transducer gain and isolation, as mentioned in section 2.2, can be represented as as $20Log|S_{21}|$ and $20Log|S_{12}|$ (respectively) when the input and output impedances match. The S-parameter simulation shows that the complete 3-stage amplifier has a transducer gain ranging from 19.4 to 14.7 dB and a reverse isolation ranging from -80.7 to -73.4 dB over the entire specified frequency band. The simulation also showed that the amplifier's quiescent current consumption was 32.7 mA at 2.5 volts. A test bench of the amplifier and the S-parameter simulations are shown below in figure 2.7 and figure 2.8.

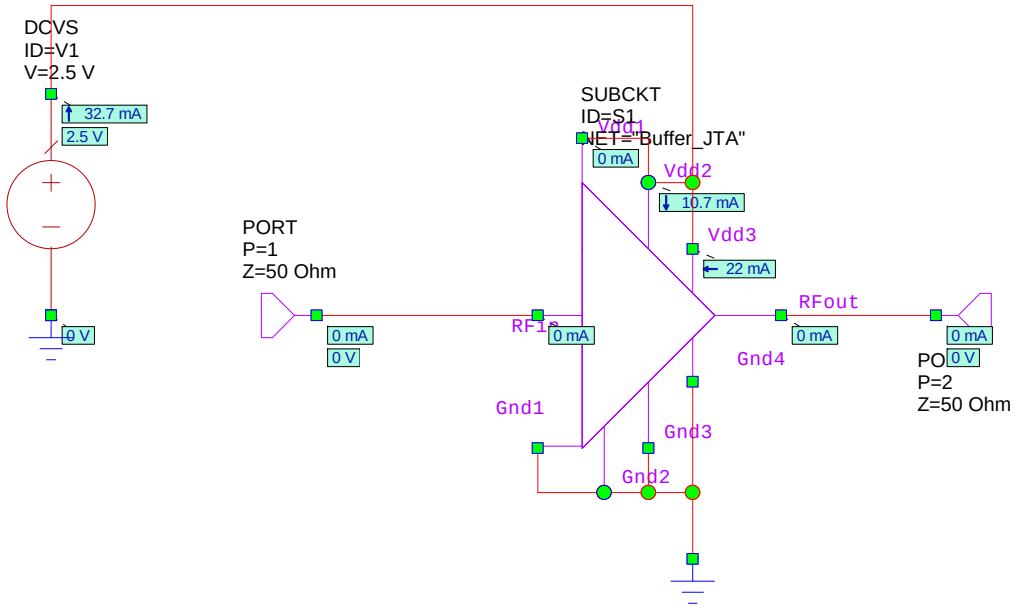


Figure 2.7: Complete buffer amplifier test bench

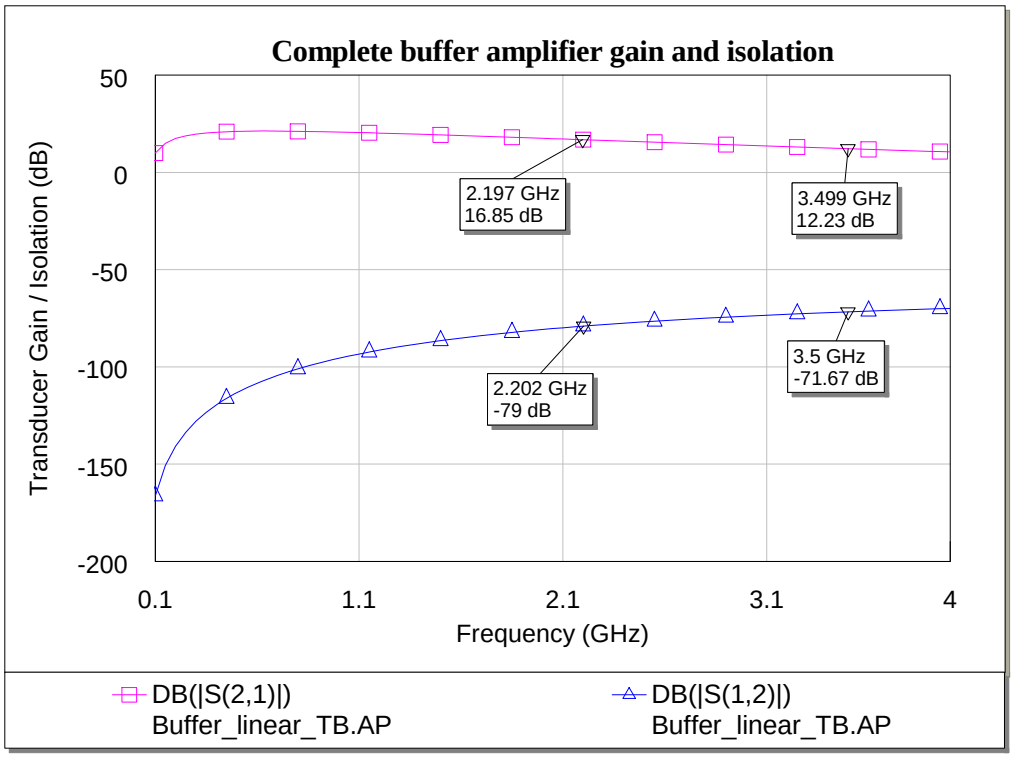


Figure 2.8: Complete buffer amplifier gain and isolation

The 1-dB gain compression point is defined as the power gain where the non-linearities of the transistor reduce the power gain by 1 dB over the small-signal linear power gain [4] or $G_{1dB}(dB) = G_o(dB) - 1$ where G_o (dB) is the small-signal power gain in decibels. Since the power gain can be defined as $G_P(dB) = P_{out}(dBm) - P_{in}(dBm)$ then the output power at the 1 dB compression point, $P_{1\,dB}$, can be written as $G_{1\,dB}(dB) = P_{1\,dB}(dBm) - P_{in}(dBm)$. Substituting $G_o(dB) - 1$ for $G_{1\,dB}$, yields the equation $G_o(dB) - 1 = P_{1\,dB}(dBm) - P_{in}(dBm)$ or said in another way, the 1-dB compression point is the point where the output power minus the input power (in dBm) is equivalent to the small-signal power gain

minus 1 dB [5]. Figure 2.9 shows a plot of the output power versus the input power of the amplifier at 3 evenly spaced frequencies across the required amplifier bandwidth (2.2, 2.85 and 3.5 GHz). The plot shows that at the three simulated frequencies, the 1 dB-compression point is greater than the 1 dBm requirement.

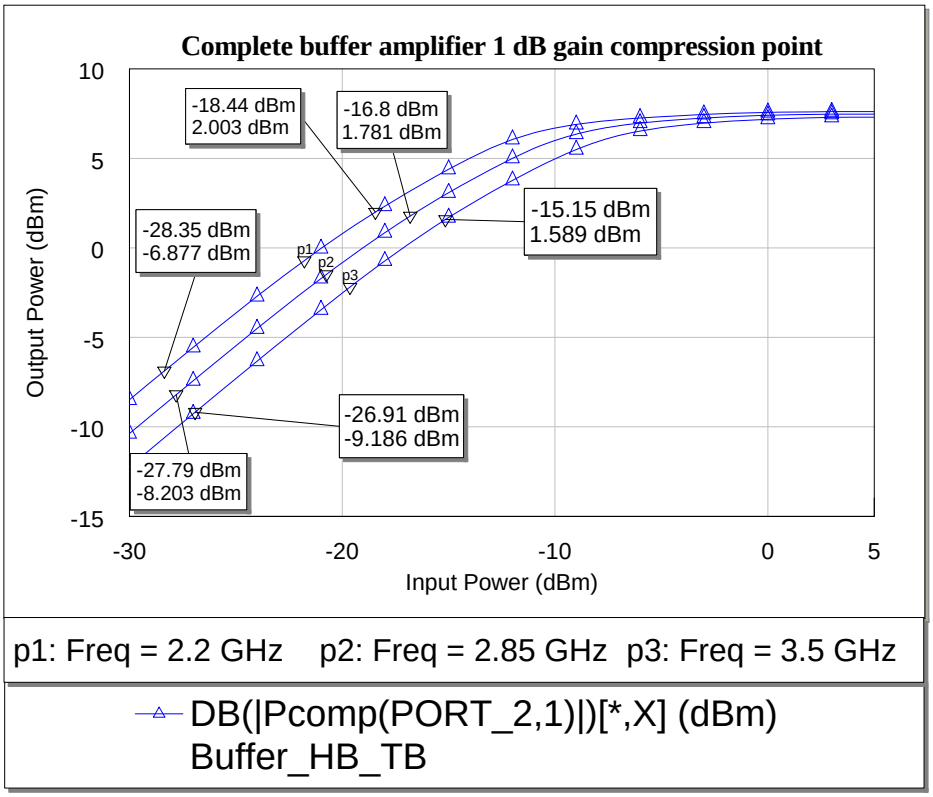


Figure 2.9: Complete buffer amplifier 1 dB compression point

Finally, the stability of the amplifier was simulated to ensure the amplifier was unconditionally stable from 10 MHz to 20 GHz. The amplifier was simulated using both an ideal 50 Ohm input and output impedance and a high VSWR input and output impedance with a reflection coefficient magnitude equal to 0.99 and a reflection

coefficient angle at 0, 90, 180 and 270 degrees. The stability parameters K and B_1 are defined by the following equations; $K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}S_{21}|}$ and $B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2$ where $\Delta = S_{11}S_{22} - S_{12}S_{21}$. For an amplifier to be considered unconditionally stable, both K >1 and B_1>0 simultaneously [5]. Figure 2.10 and 2.11 show the results of the stability simulations and it is apparent that the amplifier meets the both of the stability parameter requirements (although the B_1 stability parameter becomes very close to 0 below 1 GHz).

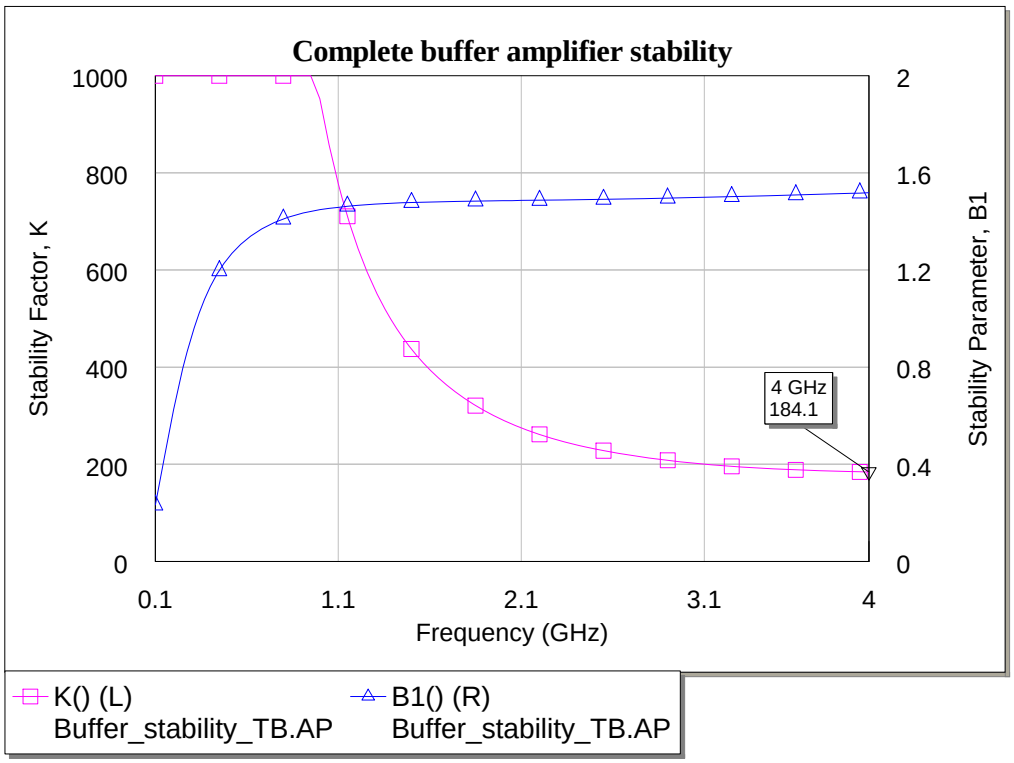


Figure 2.10: Amplifier stability parameters with an input and output impedance of 50 Ohms

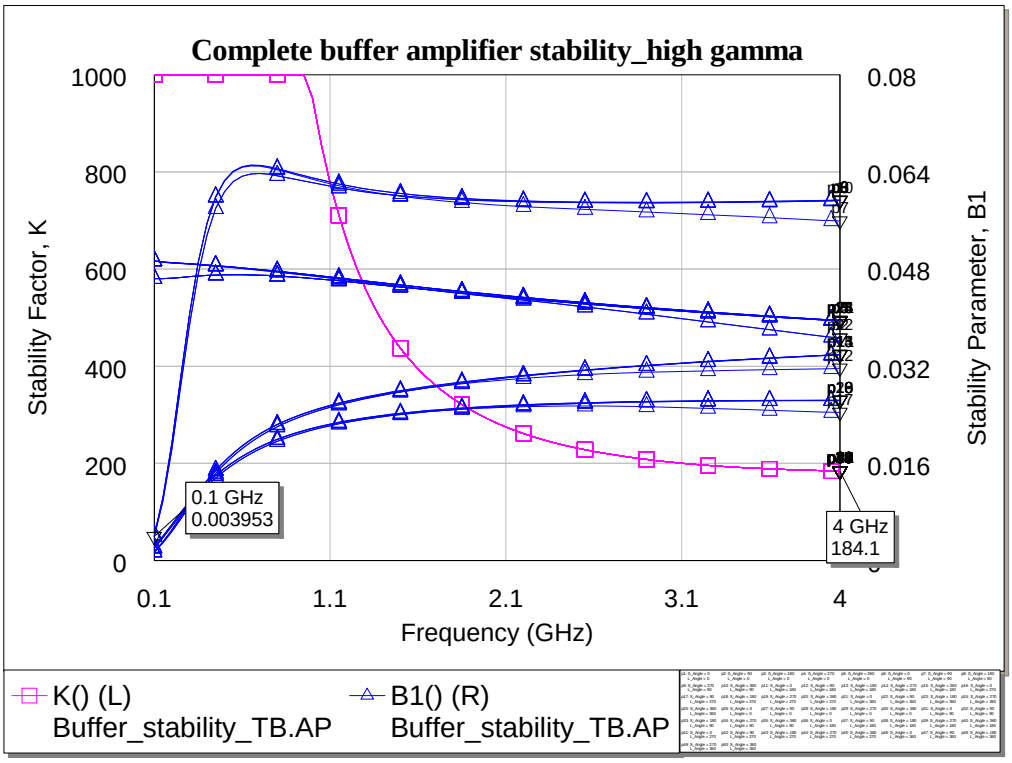


Figure 2.11: Amplifier stability parameters with a large impedance mismatch

2.3. Test and Measurement Results

The buffer amplifier was tested using a test circuit built on a 15 mil thick Roger's corporation TMM10i substrate on 32 mil thick brass backing. The traces were also plated with 150 microns of gold to facilitate wire bonding with 1 mil thick gold wire.

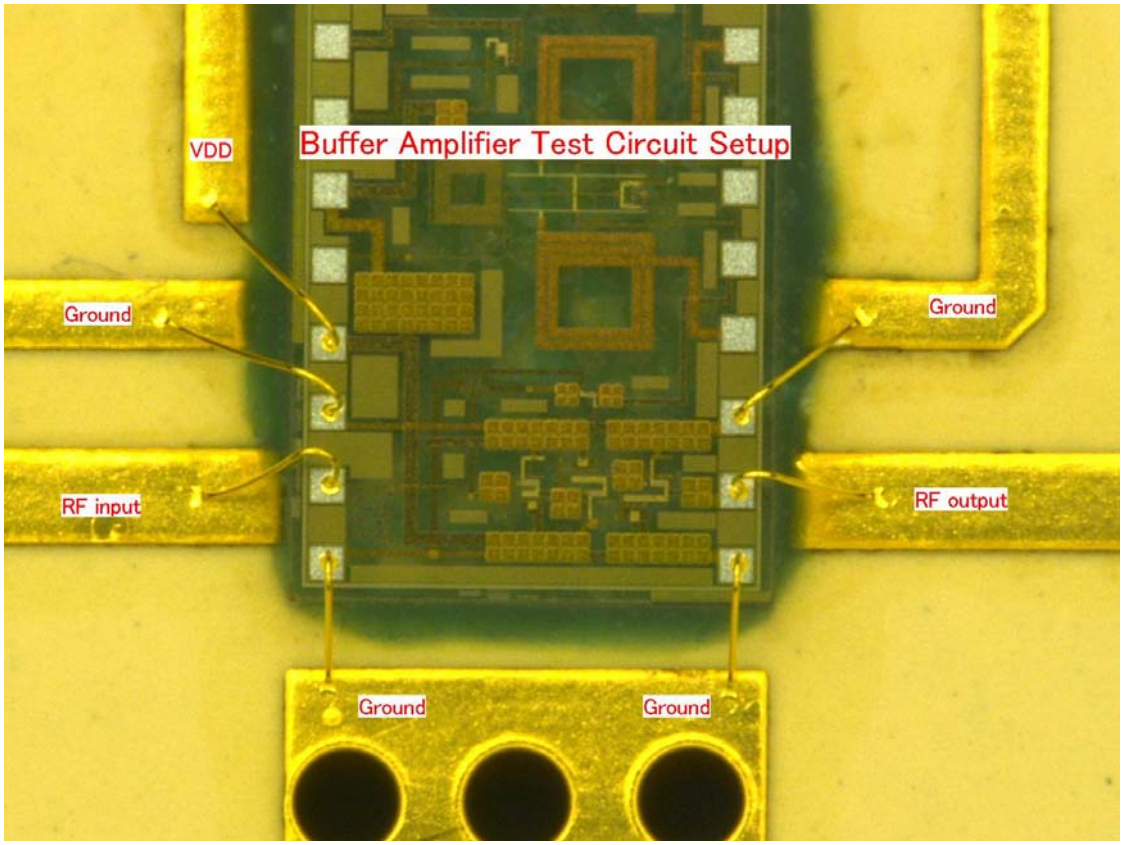


Figure 2.12: Buffer amplifier test circuit

Although it would be ideal to test the buffer amplifier in a stand-alone configuration, die space limitations would not permit it. Provisions were made on one of the complete oscillators to allow for a buffer amplifier to be powered on by itself along with bond-wire pads to allow access to the RF input and RF output of the buffer amplifier. A re-simulation of the transducer gain, isolation, 1 dB-compression point and stability was performed to include all of the micro-strip traces, bond-wires, off-chip decoupling capacitors and on-chip extraneous oscillator circuitry. All of these parasitic elements reduced the gain and dramatically reduced the isolation of the amplifier relative to the earlier "ideal" simulation but had no effect on the 1 dB

compression point or stability. In the re-simulation, the transducer gain dropped from 16.9 to 14 dB at 2.2 GHz and from 12.2 to 12 dB at 3.5 GHz while the isolation decreased from -80.69 to-29 dB at 2.2 GHz and 3.5 GHz. This dramatic decrease in the circuit's isolation will make any isolation measurement questionable at best and other indirect measurement techniques may have to be incorporated at a later period in time. The figure below shows the amplifier re-simulation test bench that includes all of the parasitics.

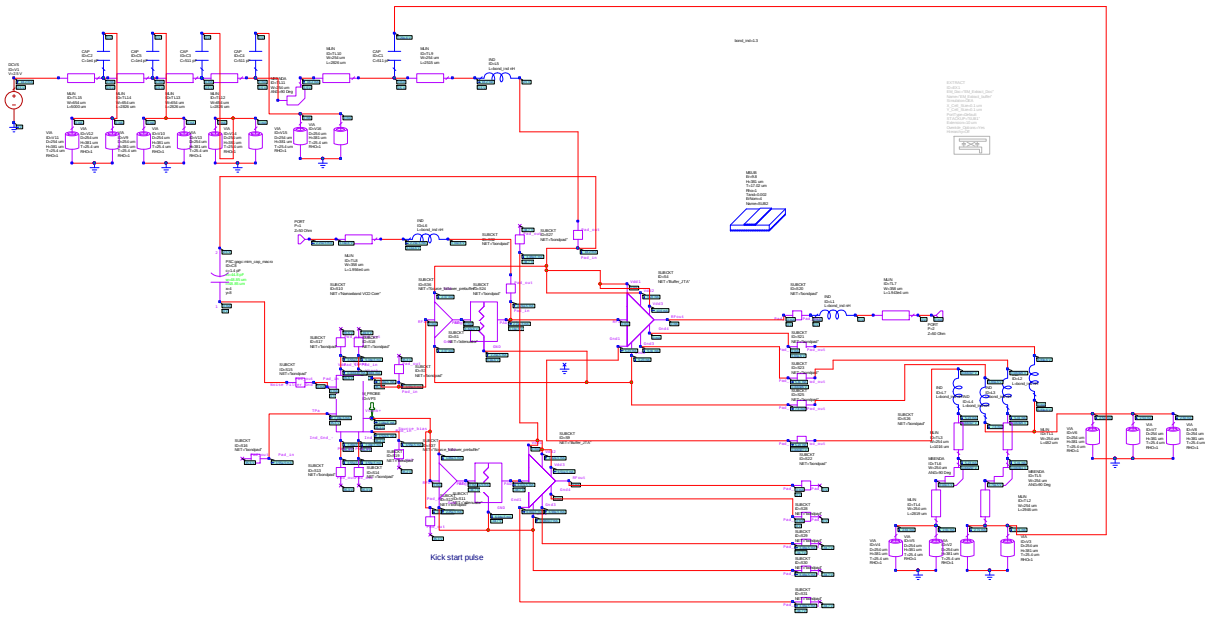


Figure 2.13: Buffer amplifier test bench including all parasitics

The amplifier's transducer gain and isolation where measured by an Agilent N5242 A Performance Network Analyzer (PNA-X). The transducer gain and isolation was

measured on two identical test circuits from 500 MHz to 4 GHz. Figures 2.14 and 2.15 show the buffer amplifier's transducer gain and isolation (respectively) as measured on the test circuits versus the re-simulation results.

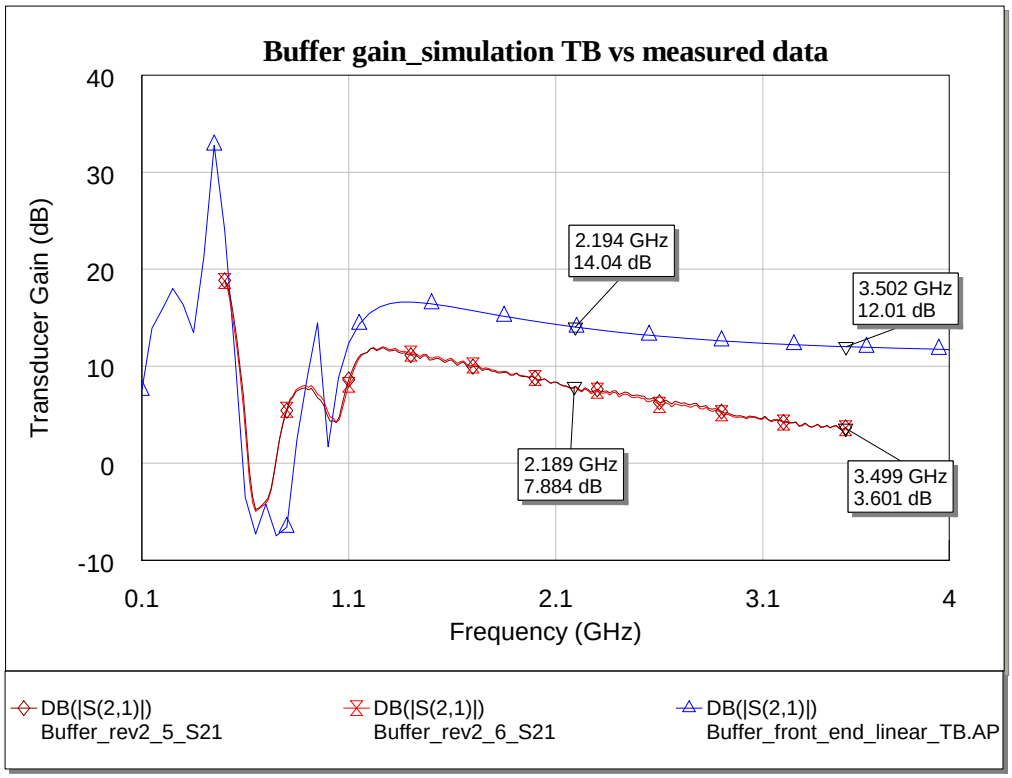


Figure 2.14: Buffer amplifier measured transducer gain vs simulated transducer gain

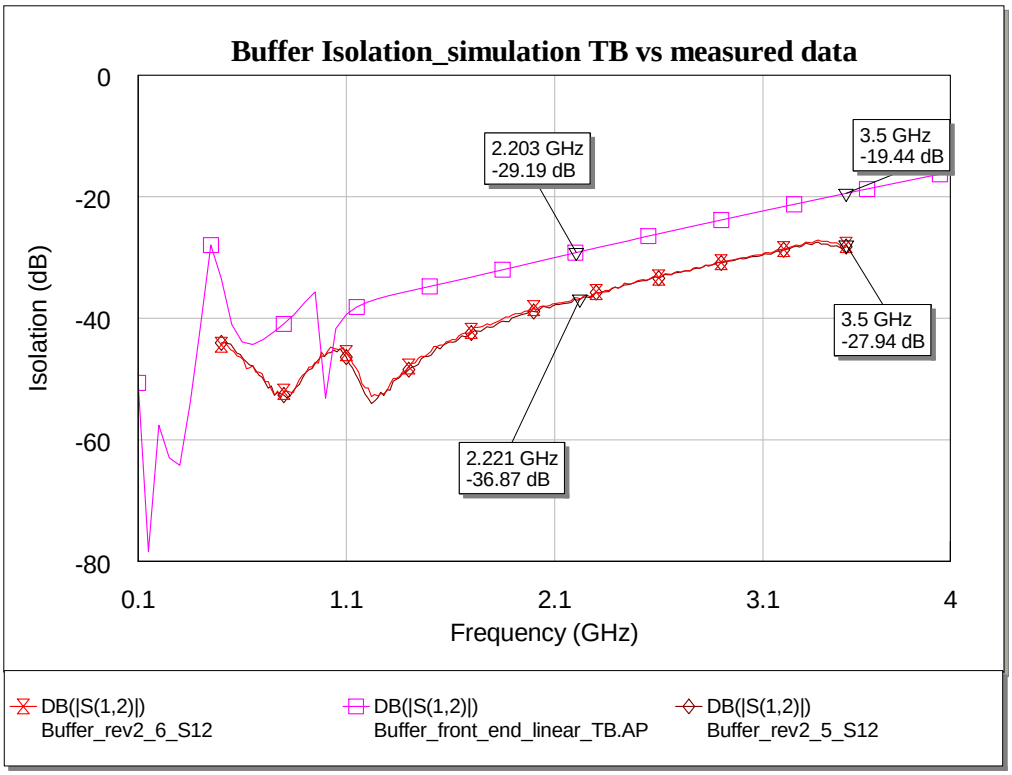


Figure 2.15: Buffer amplifier measured isolation vs simulated isolation

As shown in the figure 2.14, the transducer gain dropped from 14.0 dB in the simulation to 7.88 dB at 2.2 GHz and from 12.01 dB to 3.6 dB at 3.5 GHz. This discrepancy between the simulated vs measured data can be due to a few factors namely improperly modeled on-chip interconnect and gate poly parasitics (which will be discussed in more detail in chapter 4). Another major culprit of the gain discrepancy is more than likely caused by capacitance multiplication due to the Miller-effect.

The Miller-effect is described as a capacitance multiplication effect and comes from connecting a capacitance across 2 nodes that have an inverting voltage gain between them [7]. In the case of the common source amplifier, the capacitance that is multiplied is the gate-to-drain capacitance and the Miller-capacitance is given by the equation $C_M = C_{GD}(1 + G_m R_L)$ [5]. For a calculated voltage gain of 5.865, the Miller capacitance would be 6.865 times the modeled gate-to-drain capacitance and could cause the amplifier to have a lower than simulated gain roll-off. An examination of figure 2.14 shows this to be the case with a transducer gain difference of 3.92 dB at 2.2 GHz and a larger gain difference of 5.81 dB at 3.5 GHz. The Miller-effect can be eliminated by adding an additional FET in-series with the drain of the amplifying FET in an amplifier configuration known as a cascode amplifier [7] . The additional FET eliminates the Miller-effect by isolating the gate-to-drain capacitance of the amplifying FET from the output node of the amplifier.

The final potential cause of the amplifier gain discrepancy is large resistor tolerance variation in the FET bias circuitry. The Peregrine GC design manual states that there is a potential resistor skew variability that may cause the resistors to vary as much as $\pm 15\%$ [3]. As shown in section 2.2, the current amplifier bias circuitry is a simple voltage divider that sets the gate-to-source bias voltage at 0.63 VDC. With the bias resistors varied from one extreme to the other, the FET gate-to-source bias voltage could vary from 0.84 VDC on the high end to 0.54 VDC on the low end. This could cause the gain of the amplifier stage to vary wildly from wafer run to wafer run and is

clearly an unacceptable bias network for this particular IC process. This issue is illustrated by the fact that the amplifier's quiescent current consumption was simulated to be 36.45 mA (this includes some addition circuitry on the chip that could not be completely isolated from the amplifier's supply line) while the measured DC current consumption was 31.25 mA. The only reasonable explanation of this difference between simulated and measured DC current consumption is a difference in the bias circuitry.

The isolation, as shown in figure 2.15, was measured to be -36.98 dB at 2.2 GHz and -27.94 dB at 3.5 GHz. When compared to the simulation results (with all the off-chip parasitics), the measured isolation is 7.92 dB better at 2.2 GHz and 8.22 dB better at 3.5 GHz. This discrepancy in simulated vs measured isolation is more than likely due to a combination of improperly modeled off-chip circuit elements (such as modeled bond-wires as ideal inductors) and all of the factors that caused the transducer gain to measure low. As previously mentioned both the measured and re-simulated isolation were very far from the originally simulated isolation and, due to the off-chip parasitic components, will have to be measured indirectly by some other means (such as a measurement of the oscillator's frequency pulling).

The 1 dB compression point was also measured for 2.2, 2.85 and 3.5 GHz and is plotted below in figure 2.16. The measured 1 dB compression points for 2.2 and 2.85 GHz were 1.05 and 1.35 dBm (respectively) which were comparable to the simulated

1 dB compression point of 2.0 and 1.78 dBm. However the measured 1 dB compression point for the 3.5 GHz was -1.9 dBm which is nearly 3.5 dB lower than the simulated value of 1.59 dBm which is probably due to the Miller-effect that was detailed earlier.

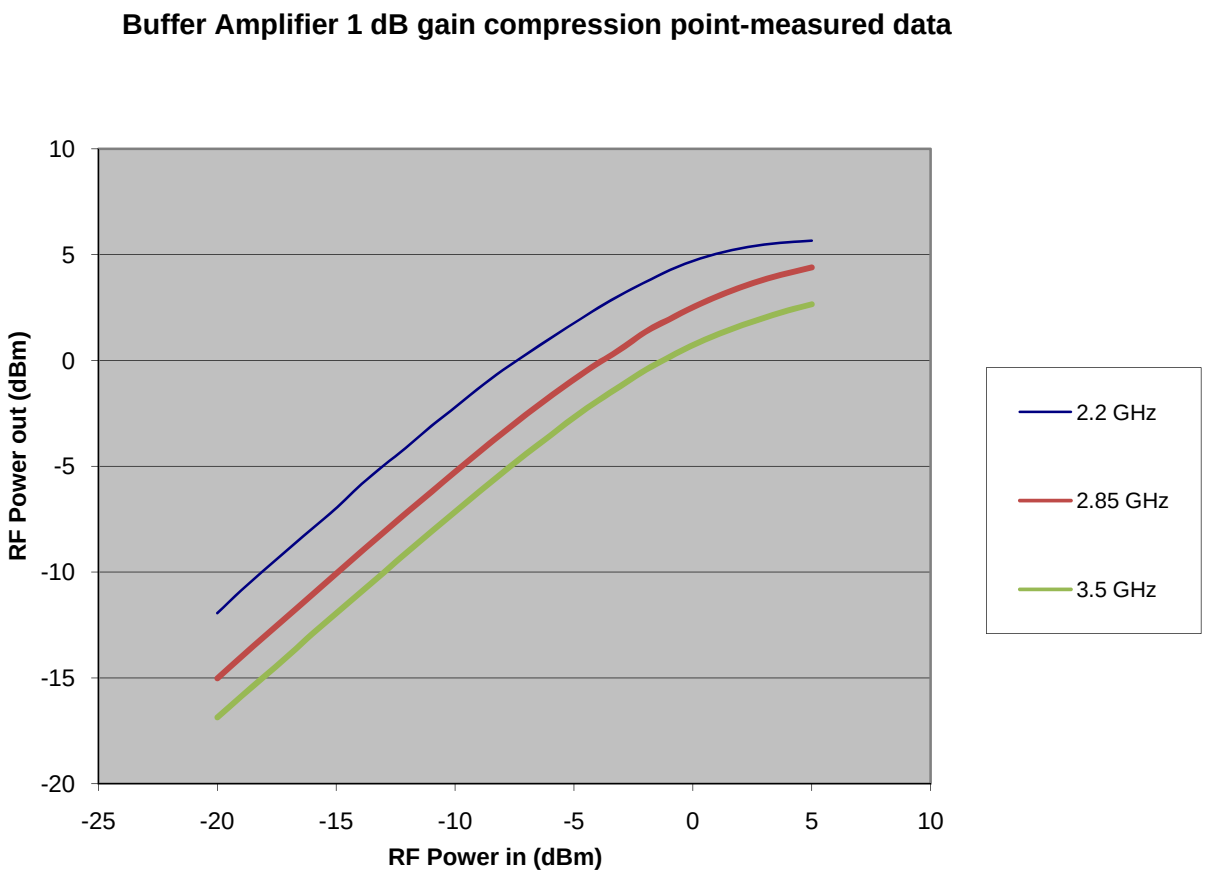


Figure 2.16: Buffer amplifier's measured 1 dB compression point

3. S-Band Voltage Controlled Oscillator

The following chapter describes design, simulation and test and measurement results of the complete voltage controlled oscillator. The PLL frequency synthesizer is intended to operate as a local oscillator in the S-band, telemetry transmitter. The chapter begins with a list of design specifications followed by an in-depth overview of LC oscillator design and phase noise then the oscillator topology and design procedure. Finally, the measurements and test results are presented and any discrepancies or problems are discussed.

3.1. VCO Specifications

Frequency Range:	2200 MHz to 2300 MHz
RF Output Power:	0 dBm minimum
Phase Noise @ 100 kHz offset:	-80 dBc/Hz
Harmonics Signals @ 1 KHz RBW:	<-45 dBc
RF Load Pulling:	< 10 kHz with a 3:1 load VSWR @ all phases
RF Output Type:	Differential output
Control Voltage:	0.25 V < Vcnt < 2.25 V
Control Voltage Tuning Slope:	50 MHz/V < K < 150 MHz/V
Supply Voltage:	2.5 V
Current Consumption:	<100 mA (with buffer amplifiers)

3.2. Tuned LC Tank Oscillator Overview

A tuned LC tank oscillator is a circuit that creates a time varying, periodic signal when supplied with DC power and can be described by the equation:

$$V_{out}(t) = V_o \sin(\omega_c t + \varphi)$$

where V_o is the amplitude, ω_c is the angular carrier frequency and φ is the phase [8]. For the circuit to be useful in a voltage-controlled application, the output frequency must be a function of an input tuning voltage such that:

$$\omega_c(V_{tune}) = 2\pi f_c(V_{tune})$$

The oscillator circuit itself can be described as a linear feedback network model, illustrated by figure 3.1, with the network transfer function of:

$$\frac{V_{out}}{V_{in}} = \frac{G(j\omega)}{1 - H(j\omega)G(j\omega)}$$

which will become unstable and oscillate when $|H(j\omega)||G(j\omega)| \geq 1$. The oscillation amplitude would continue to grow if $|H(j\omega)||G(j\omega)|$ were to stay greater than one but due to saturation effects and non-linearties of an actual oscillator circuit's negative feedback amplifier, a steady state amplitude is reached when $|H(j\omega)||G(j\omega)| = 1$. This is known as the Barkhausen criterion [8]. Assuming that the phase shift through the amplifier block, G(jω), is equal to zero, then the frequency of oscillation is set by the feedback block H(jω) and can readily implemented as an LC tank resonator that oscillates at a frequency equal to $\frac{1}{2\pi\sqrt{LC}}$.

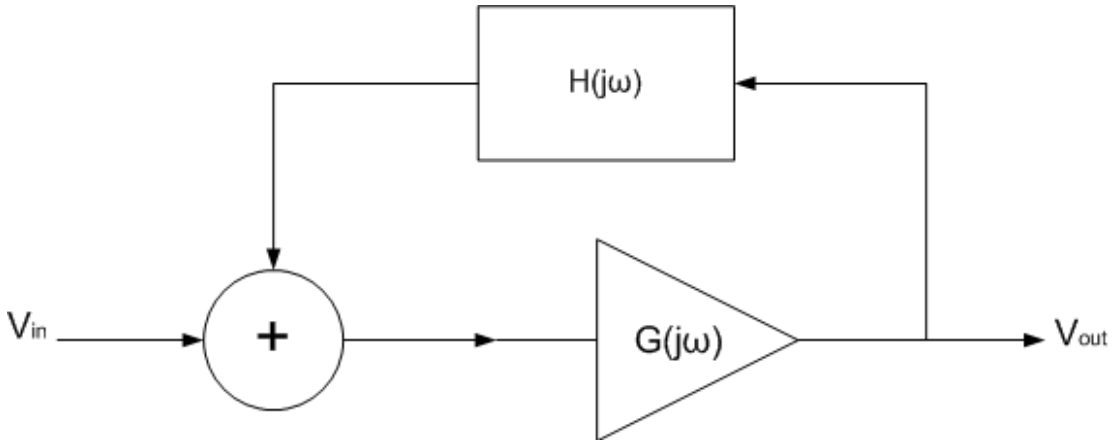


Figure 3.1 : 2-port , linear, Barkhausen oscillator model [8].

A tunable LC oscillator generally consists of an inductor and capacitor in a parallel configuration to create a resonant tank circuit and an active device of some kind to compensate for the losses associated with the finite Q's of these passive devices. This active device is typically known as a negative resistance generator because it creates the "negative resistance" (i.e. amplification) required to overcome the tank losses associated with passive devices.

Generally, a voltage tuned variable capacitor (or varactor) is an readily realizabl integrated circuit element thus is used as the tuning element in the oscillator circuit. The varactor's capacitance is proportional to the tuning voltage, V_{tune} , making the oscillators resonant frequency proportional to the tuning voltage fulfilling the requirement that $\omega_c(V_{tune}) = 2\pi f_c(V_{tune})$. It is important to note that while the tank inductance, L, is defined by an on-chip inductor and/or bond-wire inductance, the tank capacitance consists of the sum of the varactor capacitance and any parasitic

inductor coil capacitances as well as the active device capacitance and any output circuit load capacitance and must be carefully analyzed and accounted for to accurately predict the resonator's oscillation frequency [8].

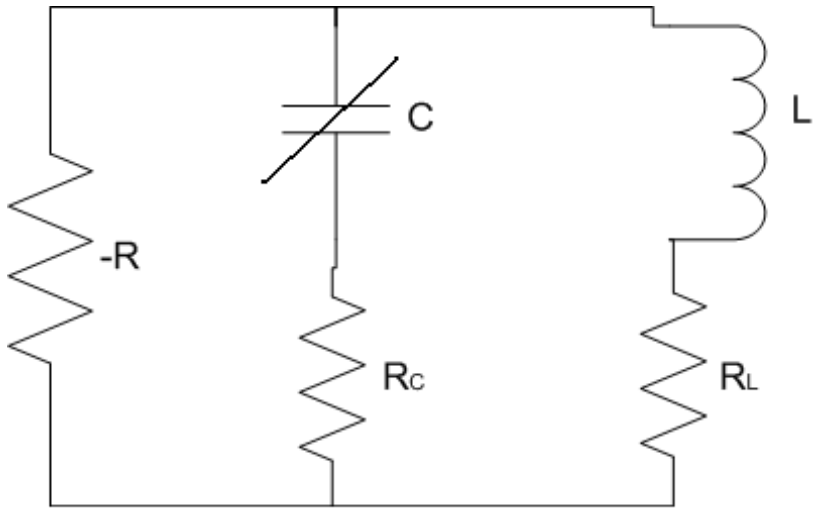


Figure 3.2: Simple LC-VCO model with passive component losses

3.2.1. Phase Noise Overview

One of the most important performance specifications that affects every oscillator design is that of up-close spectral purity, more commonly referred to as phase noise. As previously mentioned, an ideal oscillator creates a time-varying periodic signal defined by the equation:

$$V_{out}(t) = V_o \sin(2\pi f_c t + \varphi)$$

An examination of the frequency domain spectrum of the above signal reveals a Dirac-impulse at $\pm f_c$. An oscillator consisting of real components and active circuit elements is more realistically defined by the equation:

$$V_{out}(t) = V_o(t) sin\big(2\pi f_c t + \varphi(t)\big)$$

This new equation shows that the signal amplitude and phase are functions of time and any fluctuations in these parameters will result in sidebands close to f_c. The fluctuations in the frequency domain, translate into jitter in the time-domain which is defined as the random perturbation of a periodic signal's zero crossing [8]. Figures 3.3 and 3.4 show an ideal oscillator spectrum versus a realistic oscillator spectrum and the relationship between phase noise and time-domain signal jitter are directly taken from [8]. Minimization of phase-noise is one of the most important design goals of all frequency synthesizers. This is because phase noise can cause unwanted signal interference in adjacent frequency channels when the synthesizer is used in a transmitter application or can cause an adjacent channel frequencies to interfere with a desired frequency if used in a receiver application.

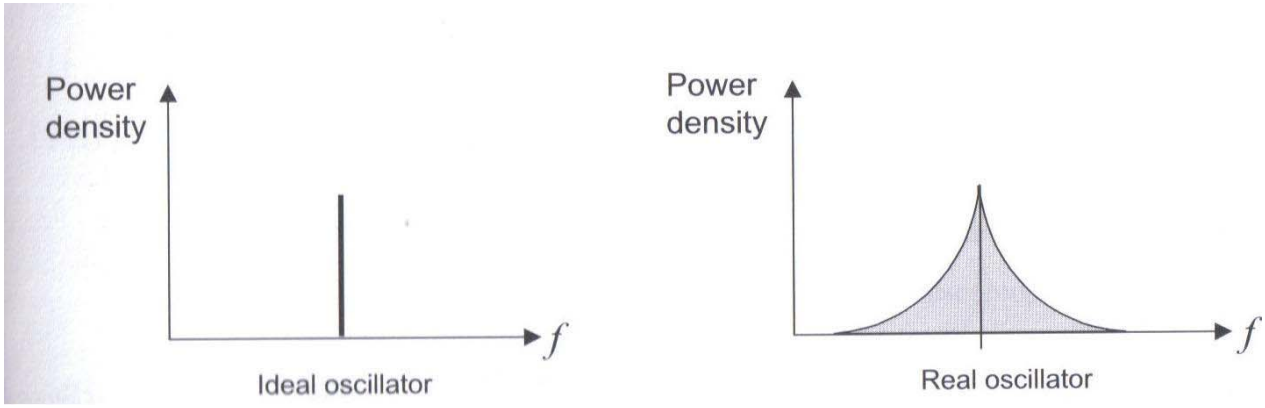


Figure 3.3: Frequency spectrum of an ideal and real oscillator [8]

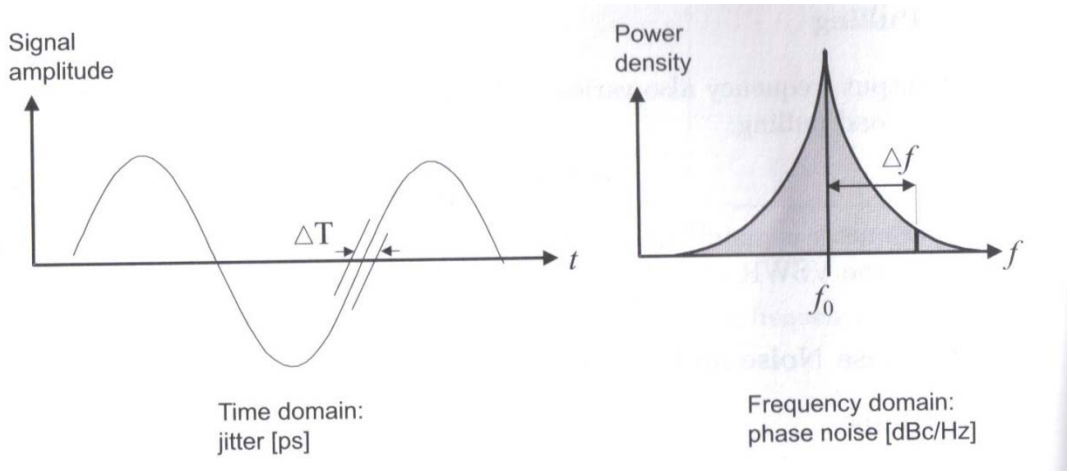
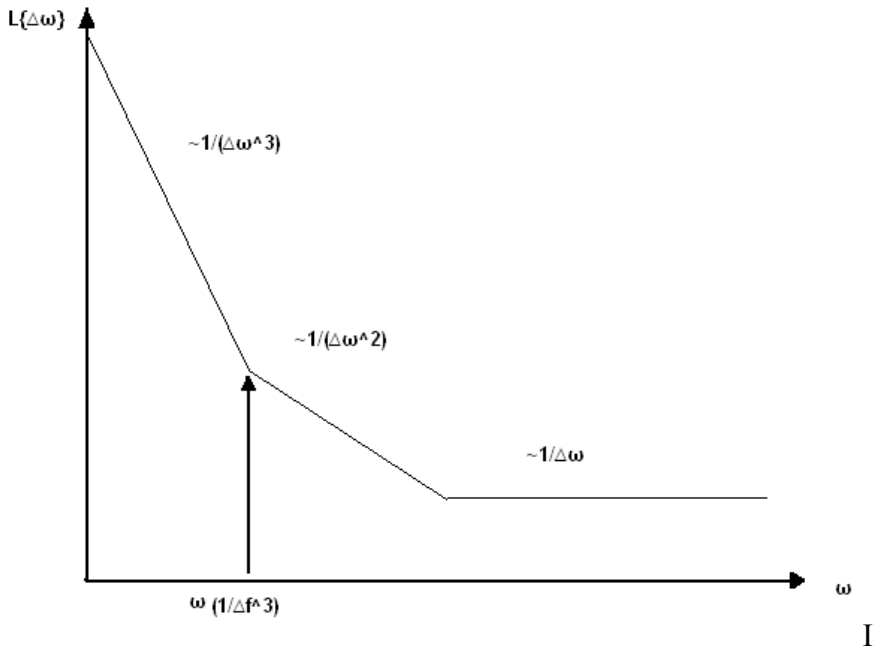


Figure 3.4: Relationship of time domain jitter and frequency domain phase-noise [8]

Phase noise of a resonant LC oscillator can be characterized by the empirically derived formula:

$$£(\Delta\omega) \;=\; 10\log\frac{2\mathrm{F}kT}{\mathrm{P_{sig}}}\left[1+\left(\frac{\omega_c}{2\mathrm{Q_L}\Delta\omega}\right)^2\right]\left(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)$$

where $\Delta\omega$ is the angular frequency offset; $\Delta\omega_c$ is the oscillator's carrier frequency; Q_L is the loaded tank quality factor; P_{sig} is the average signal power; F is the active device's noise excess factor; k is Boltzman's constant; T is the device temperature in kelvins; and ω_{1/f^3} is active device's flicker-noise corner frequency between the $1/f^3$ region and $1/f^2$ regions (see figure 3.5 for a detailed illustration). This is known as Leeson's empirical phase-noise model [9].



I

Figure 3.5: Typical single-sideband phase-noise with ω_{1/f^3} corner frequency highlighted

The flicker-noise corner frequency can generally be ignored when analyzing oscillators that will be used in a phase-locked loop frequency synthesizer as this portion of the phase noise is a function of the PLL's loop response and reference frequency phase-noise[10]. By ignoring this portion of the phase noise and letting the loaded tank circuit quality, $Q_{tank} = \omega_c L/R_S$ and the average signal power, $P_{sig} = V_{sig}^2/(2Q_{tank}^2 R_s)$, a simplified version of the Leeson's phase-noise model can be written as:

$$£(\Delta\omega) = 10 \log \left[\frac{k\mathrm{TFR_S}}{\mathrm{V_{sig}^2}} \frac{\omega_c^2}{\Delta\omega^2} \right] \qquad (3.1)$$

The above expression also assumes that the oscillator carrier frequency, $\omega_c >> \Delta\omega$. An examination of the simplified phase-noise expression shows that a practical approach to reducing phase-noise in any LC oscillator can be done by increasing the

oscillators voltage swing, V_{sig} ,which is defined as the difference between the minimum and maximum voltage level in the tank circuit and increasing the loaded tank quality factor by decreasing the tank's series resistance, R_s. The tank circuit's series resistance is usually dominated by the inductor resistance in an on-chip integrated inductor.

Another very important factor to consider when trying to design an oscillator with the lowest possible phase-noise is the active device's 1/f noise, or flicker noise. Flicker noise can very prominent in MOSFET devices relative to bulk devices such as heterojunction bipolar transistors due to the fact that MOSFET's are surface type devices where charge is trapped and released in surface defects and impurities [7]. To obtain good 1/f noise performance from a MOSFET, the largest practical device for a required transconductance must be used. This is because the larger MOSFET's gate capacitance smoothes out fluctuations in the channel charge as it moves back and forth between the drain and source [7]. The 1/f drain noise current is defined by:

$$\overline{i_n^2} = \frac{K}{f} \cdot \frac{g_m^2}{WLC_{ox}^2} \cdot \Delta f$$

where W and L are the MOSFET's gate width and length, C_{ox} is the MOSFET gate-oxide capacitance, g_m is the MOSFET transconductance , Δf is the noise-bandwidth and K is a device specific constant which is typically 50 times larger in NMOS devices than PMOS devices [7]. Given this fact and the fact that PMOS devices generally have roughly half the transconductance for a given size, the 1/f drain noise will be much less for a PMOS device than an NMOS device (for a given

transconductance). This makes using a PMOS transistor a superior choice when choosing a device for a negative resistance generator.

3.3. VCO Design

As previously mentioned, the oscillator circuit consists of an LC resonant tank and an active device negative resistance generator in a differential configuration. The tank circuit consists of a pair of on-chip inductors, a pair of NMOS varactors and a MIM capacitor. The negative resistance generator is a current mirror circuit is placed from the power supply line (VDD) to the PMOS device's source to help sustain oscillation and the resonator tank is connected to ground. This topology was chosen to make the oscillator circuit less vulnerable to power supply pushing but at a cost of added substrate ground noise [8]. In an attempt to lower the flicker noise up-conversion associated with the current mirror transistors, an LC filter was placed between the current mirror circuitry and the negative resistance generator FET's [11]. An off-chip resistor was used as a current source reference for the current mirror to provide an adjustable bias current for the oscillator core. An adjustable bias current allows for phase-noise and output power optimization.

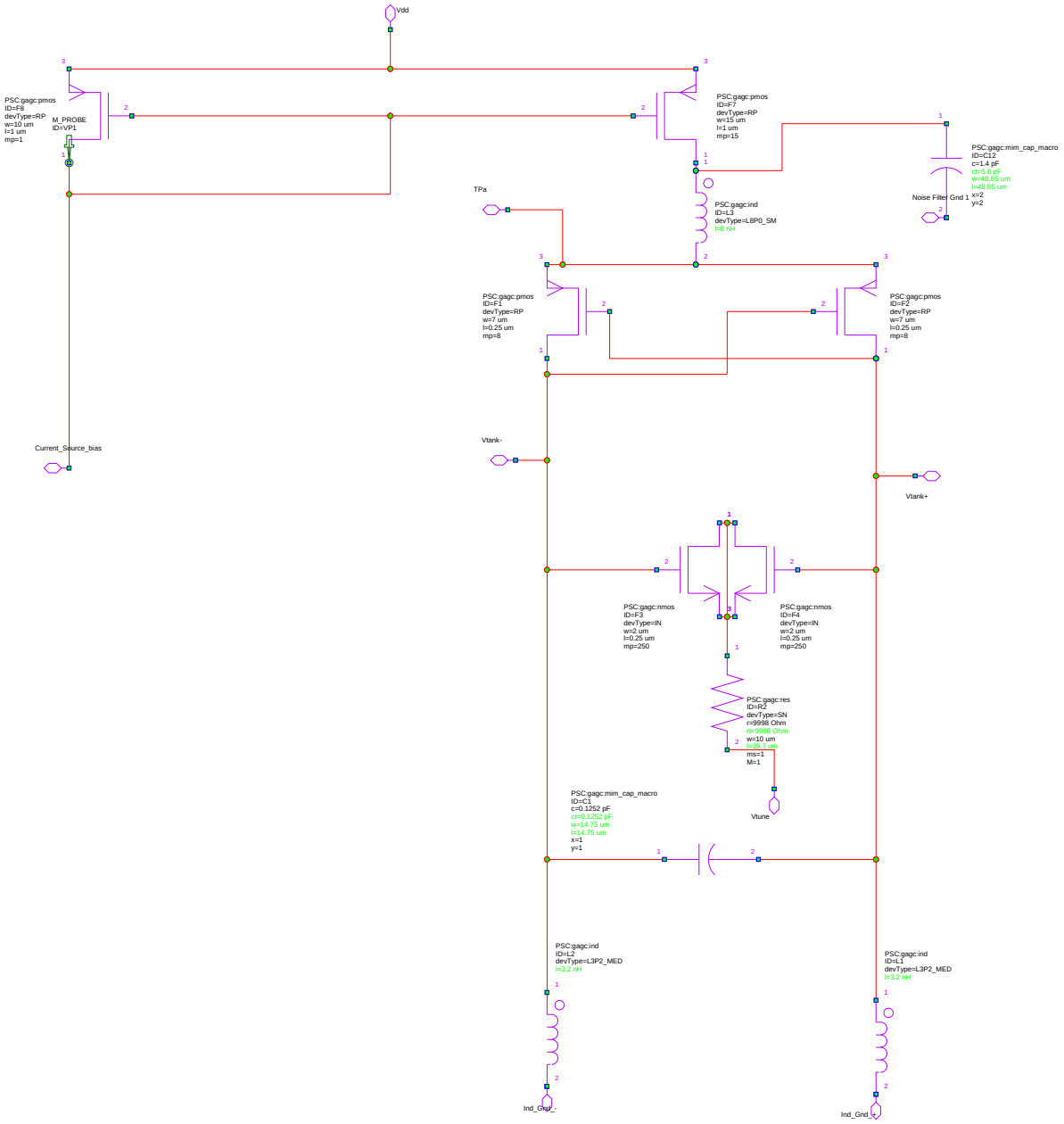


Figure 3.6: Differentially cross-coupled oscillator core for the telemetry-band VCO

3.3.1. Oscillator Core Frequency

Since the VCO core is a differential topology, an equivalent half-circuit analysis is required. The equivalent half-circuit consists of one of the PMOS active devices along with one of the grounded on-chip inductors, one of the NMOS varactors and half the value of the parallel MIM capacitor (see figure 3.7). The frequency of oscillation is determined by the equation:

$$F_{osc} = \frac{1}{2\pi\sqrt{LC}} \qquad (3.2)$$

where L is the inductance of the on-chip tank inductor and C is the MIM capacitor, varactor capacitance and any drain-to-gate capacitance associated with the PMOS device.

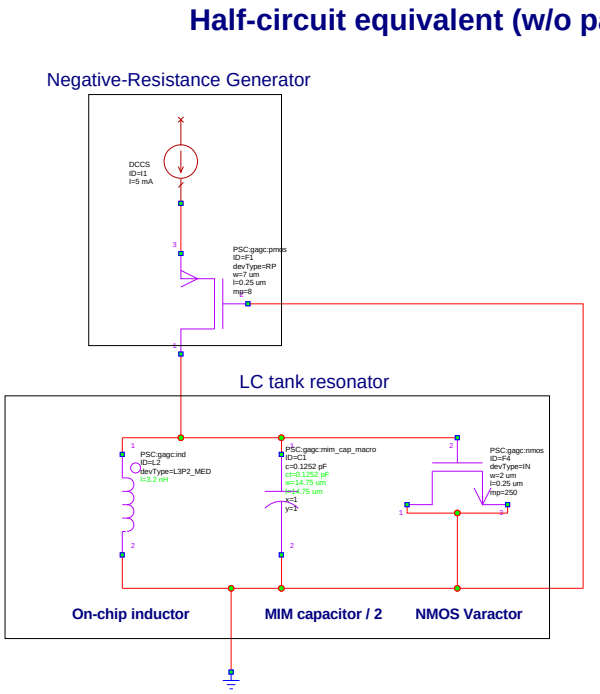


Figure 3.7: VCO half-circuit equivalent

The on-chip inductor was the first element to be selected and a pre-determined 3.2 nH Med-Q inductor was chosen from the Peregrine design kit. This particular inductor was selected due to the fact that it's peak Q was measured to be over 20 at 2.2 and 2.3 GHz by Peregrine Semiconductor [3]. Since the inductor will be in-series with a bond-wire to ground, the total inductance of the tank circuit will be the sum of these two elements. Using the approximation that a 1-mil long bond-wire has 1 nH of inductance, a 1.1 nH inductor element was added in-series with the Peregrine 3.2 nH inductor resulting in a total tank inductance of 4.3 nH. Rearranging equation 3.2 into:

$$C = \frac{1}{L(2\pi f_{osc})^2}$$

the required high and low required capacitance can be calculated. For 2.2 GHz and 2.3 GHz, the calculated capacitance is shown to be:

$$C_{2.2\ GHz} = \frac{1}{4.3\ e{-}9\cdot(2\cdot\pi\cdot 2.2\ e\ 9)^2} = 1.217\ \text{pF}$$

$$C_{2.3\ GHz} = \frac{1}{4.3\ e{-}9\cdot(2\cdot\pi\cdot 2.3\ e\ 9)^2} = 1.114\ \text{pF}$$

Calculating the difference between the upper and lower required capacitance, ΔC, shows that the MOS varactor element needs to have a range of 0.103 pF between 0.25 and 2.25 V to meet the minimum tuning range and control tuning voltage slope requirement. It was decided that a varactor with a tuning range closer to 0.15 pF would be used along with a MIM capacitor and off-chip capacitor to center the tuning

range at approximately 1.25 V. The off-chip capacitor allows for different values of capacitor to be added to the tank circuit to try and compensate for variations in length of the bond-wire that is in series with the on-chip inductor.

Through an iterative simulation approach, it was found that a 0.125 pF MIM capacitor, 0.1 pF off-chip capacitor and an intrinsic NMOS varactor with a gate width of 2 µm, gate length of 0.25 µm and 260 gate fingers would yield a capacitance and ΔC that will completely cover the required tuning range of 2.2 GHz to 2.3 GHz. The intrinsic channel NMOS device was found to make a inversion-mode varactor with a tuning curve that was more linear than the regular channel NMOS device. Figure 3.8 shows the VCO tuning range simulation results.

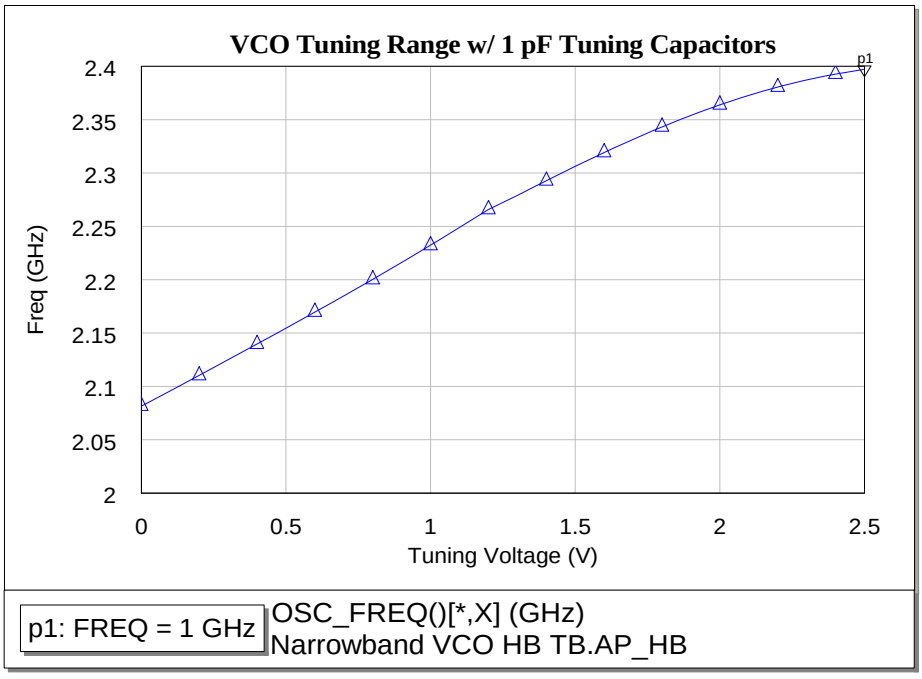


Figure 3.8: VCO frequency tuning range simulation results

3.3.2. Resonant Tank Q

The oscillator's resonant tank Q is very important to accurately predict as it is an important factor in estimating the phase-noise of an oscillator as well as determining the required negative resistance to ensure oscillator startup and sustained oscillation. Figure 3.9 shows that the simulated loaded tank Q of the resonator to be 11.67 at 2.2 GHz and 11.43 at 2.3 GHz. The tank is loaded with a 1500 Ohm resistive port, which corresponds to the input impedance of the source follower amplifier that the oscillator is feeding (see section 3.3.5.1 for more details).

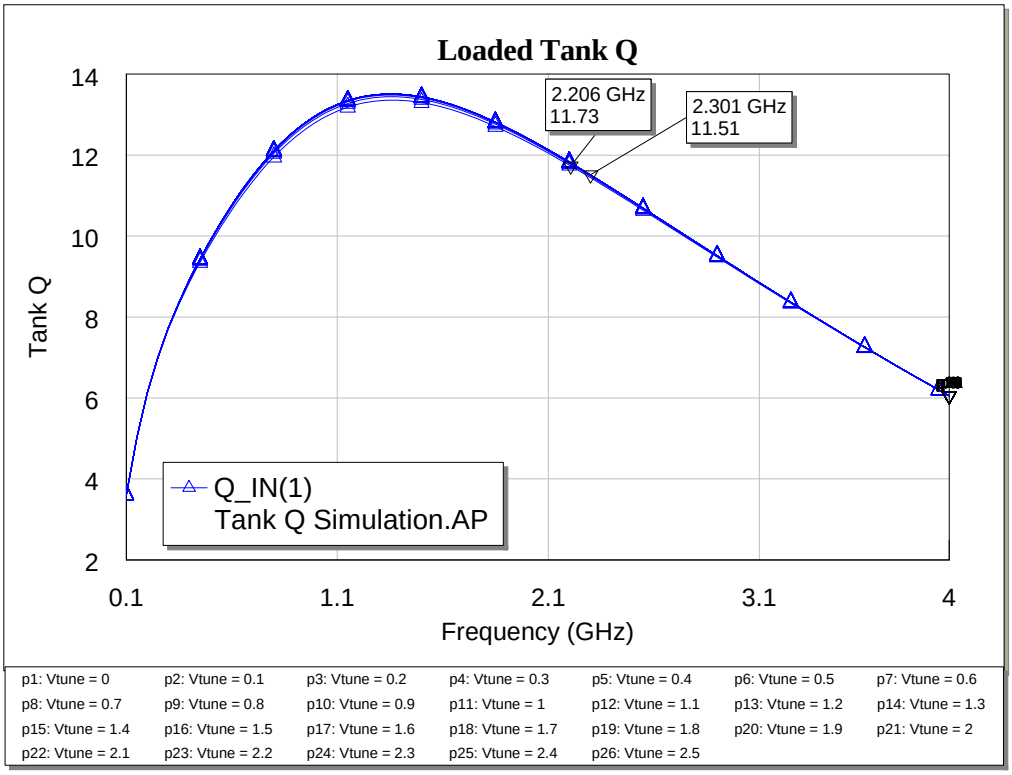


Figure 3.9: Loaded tank Q simulation results

3.3.3. Negative Resistance Requirements

As previously mentioned, the negative resistance generator circuit is an active device than compensates for the losses associated with the resonant tank. At resonance, the tank circuit's total parallel tank resistance can be written as $R_P = Q_{tank}^2 R_s$ [7] where R_s is the series resistance of the tank inductance and Q_{tank} is the loaded tank quality factor. This assumes that the resonant tank capacitor series resistance is much lower than the tank inductor series resistance, which is usually valid for integrated circuit components. The series resistance of the inductor is determined by the inductor's Q from the equation, $Q_L = \frac{reactance}{Series\ resistance}$ where the reactance is 2πf *L. Rearranging the equation, the series resistance can be determined by dividing the inductor's reactance by the inductor's Q (which was determined to be approximately 20 from [3]) to yield:

$$R_s = \frac{2 \cdot \pi \cdot 2.25e9\ Hz \cdot 3.2e-9\ H}{20} = 2.26\ \Omega$$

Using the results of the tank simulation in 3.3.2 and the above calculated series resistance of the inductor, the total parallel resistance can now be calculated as:

$$R_p = 11.67^2 \cdot 2.26 = 307.8\ \Omega$$

By examining the small-signal AC equivalent circuit of the oscillator, it can be shown that to overcome the losses associated with the tank circuit at resonance, the transconductance of the negative resistance circuit needs to be equal to or greater than the reciprocal of the parallel tank resistance or; $g_m \geq \frac{1}{R_p}$. Put another way, the small signal loop-gain, A_l, has been found to be [12]:

$$A_l = (G_m \cdot R_p)^2 \qquad (3.3)$$

for a differential oscillator circuit and reduces to one when the parallel tank resistance and negative resistance generator's transconductance equal each other, fulfilling the requirement for oscillation. In general, the loop gain is set to be at least three resulting in all of the poles being in the right hand plane thus ensuring oscillator start-up [12]. A PMOS device with a total channel width of 56 µm (7 µm width by 8 total fingers) and gate length of 0.25 µm was chosen for the active device. Examining the PMOS IV Curves, in figure 3.10, the transconductance can be determined by looking at the change in drain current divided by the change in gate voltage for a given drain voltage or:

$$G_m = \frac{\partial I_{DQ}}{\partial V_{GS}} \approx \frac{\Delta I_{DQ}}{\Delta V_{GS}} = \frac{-10.49\ mA - (-6.88)\ mA}{-2\ V - (-1.5\ )V} = 7.22\ mS$$

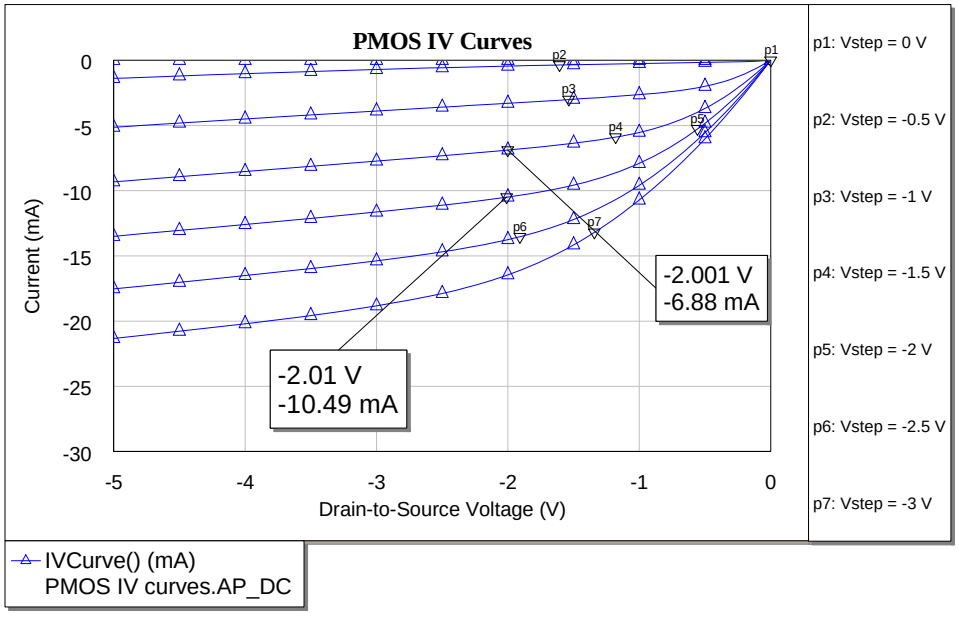


Figure 3.10: IV Curves for a 7 x 8 µm p-channel MOSFET

The small-signal loop gain can now be calculated from equation 3.3 as:

$$A_l = (7.22\ e-3\ S\ \cdot 307.8\ \Omega)^2 = 4.93$$

which is large enough to ensure oscillator start-up.

3.3.4. Current Mirror Bias Circuit

A current mirror circuit used to provide a constant bias current through the oscillator core and was designed to provide a constant 10 mA current (5 mA for each FET). This was found (through simulation) to provide an adequate enough current through the oscillator core to sustain oscillation and ensure a large voltage swing in-order to minimize the oscillator's phase noise (per equation 3.1). The current mirror is comprised of two PMOS devices in a configuration in which the gates of the devices are biased at the same voltage potential and the drain-to-source current of the output transistor and are determined by the gate width to length aspect ratios [2] or;

$$I_{output} = \frac{\left(W/L\right)_2}{\left(W/L\right)_1} \cdot I_{reference}$$

It was found that with a 0.5 mA current source (in the form of a 1 kOhm off-chip resistor), an aspect ratio of 22.5 was needed to ensure an output current of 10 mA into the oscillator core. A PMOS device with a 10 µm gate width and 1 µm gate length was used as the reference current transistor (M1) and a PMOS device with a 225 µm gate width (15 µm x 15 fingers) and 1 µm gate length was used as the output current transistor (M2). Figure 3.10 shows a schematic of a current mirror circuit using PMOS transistors.

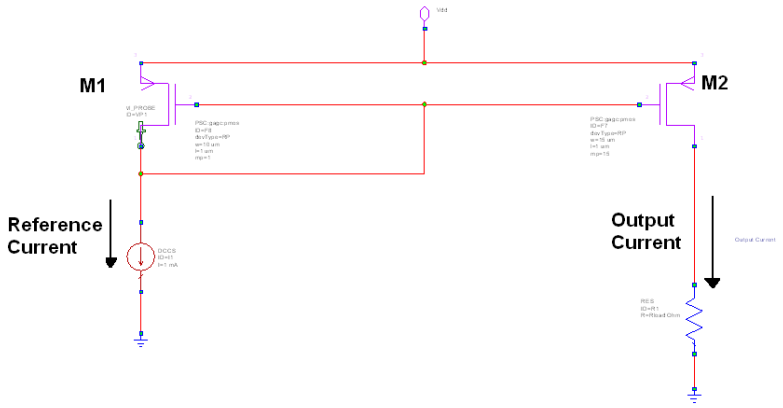


Figure 3.11: Current mirror circuit using PMOS devices.

3.3.5. Complete VCO Circuit

The complete voltage controlled oscillator circuit initially consisted of the oscillator core and high-isolation buffer amplifier circuit. During the initial synthesis and simulation portion of the design phase, it was decided that a source-follower amplifier and pi-attenuator circuit needed to be added. The source follower amplifier was used to provide the oscillator core with a high input impedance so as the oscillator core's resonant tank circuit isn't "loaded-down" with a low impedance which can degredate it's Q. The pi-attenuator circuit was used to lower the source-follower amplifier's output power to a proper level for the high-isolation buffer amplifiers so that they don't reach their 1 dB compression point. Figure 3.11 shows a schematic of the complete amplifier circuit as well as inductors that represent parasitic bond-wire inductances along and all of the off-chip components such as the 0.1 pF chip

capacitors, 1 kOhm current source resistor and two mini-circuit's LFCN 2250+ low-pass filters that are used to lower the 2nd, 3rd and 4th harmonic components of VCO.

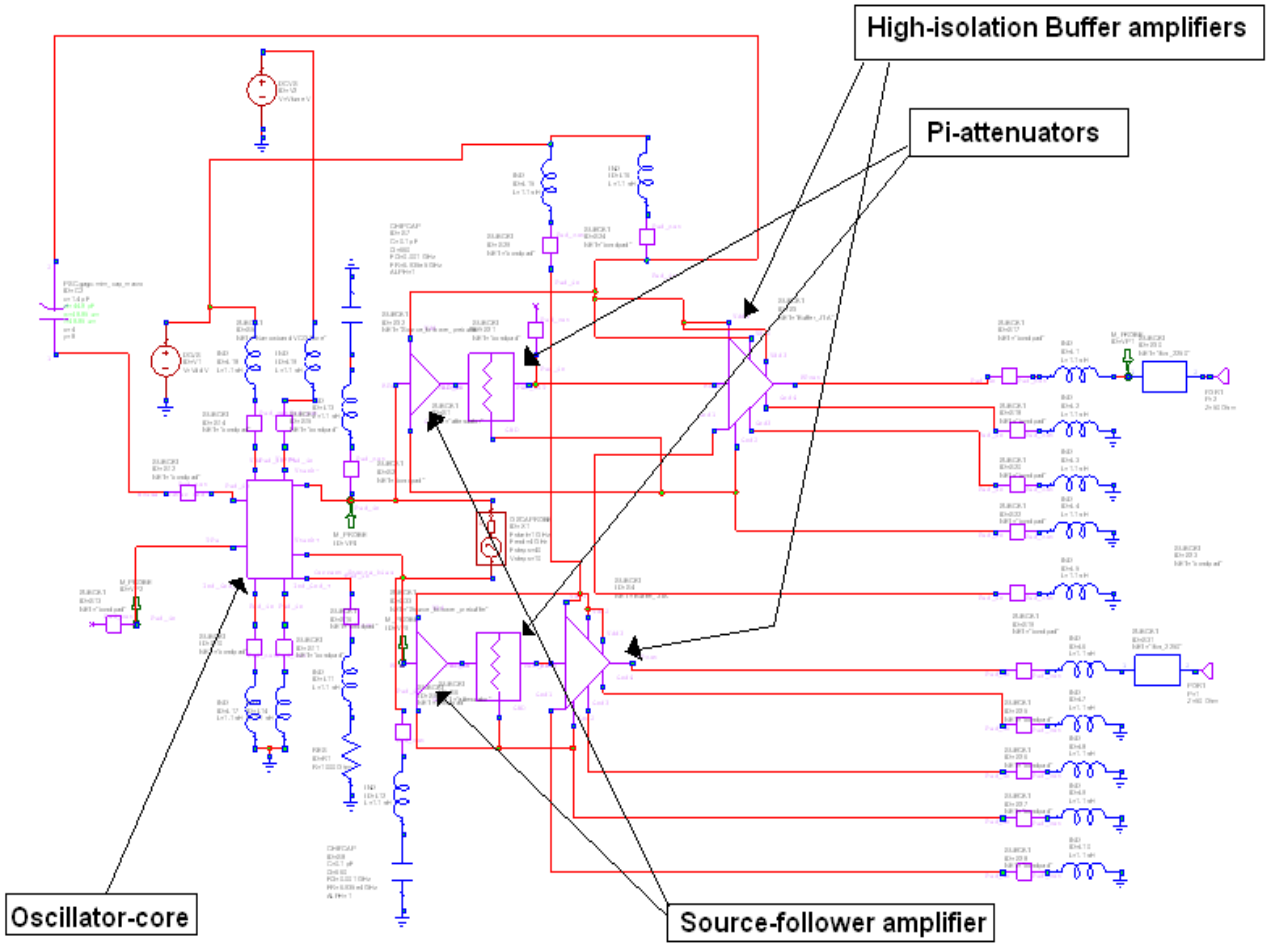


Figure 3.12: Complete Telemetry PLL VCO Schematic

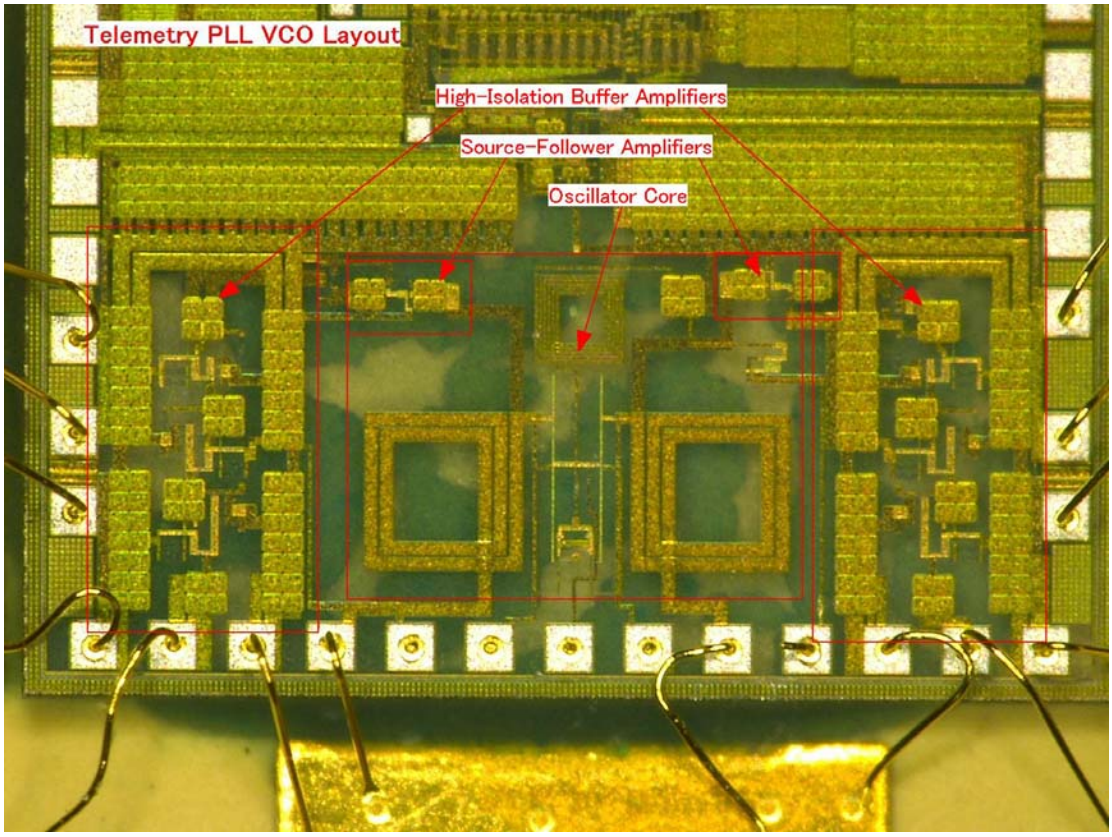


Figure 3.13: Complete Telemetry PLL VCO Layout

3.3.5.1. Source-Follower Amplifier

A source-follower amplifier (or common-drain amplifier) is an amplifier configuration that has a high input impedance (relative to a common-source or common-gate amplifier) and, at best, unity gain [2]. The common-source amplifier, shown in figure 3.11, was designed with a resistive voltage divider to bias the gate of the amplifier's NMOS transistor to 1.8 V. With the 9 kOhm and 25.7 kOhm biasing resistors, the input impedance of the amplifier is simulated to be approximately 1500 Ohms at 2.25 GHz (see figure 3.12) A 500 Ohm resistor was used as a source resistor

and gives the source-follower an output impedance of approximately 60 Ohms at 2.25 GHz (see figure 3.13). Three pF coupling capacitors were used on the input and output of the amplifier to block any DC voltages from incorrectly biasing or influencing the circuit in anyway. The insertion loss of the circuit was simulated to be 4.45 dB at 2.25 GHz, which was deemed to be acceptable due to the fact that an attenuator circuit was needed between the oscillator core and output buffer amplifier anyway and, in effect, the source-follower circuit just adds to the attenuation and is accounted for during the full-circuit VCO simulations. DC simulations also show the amplifier to consume only 2.4 mA of current with a 2.5-V power source.

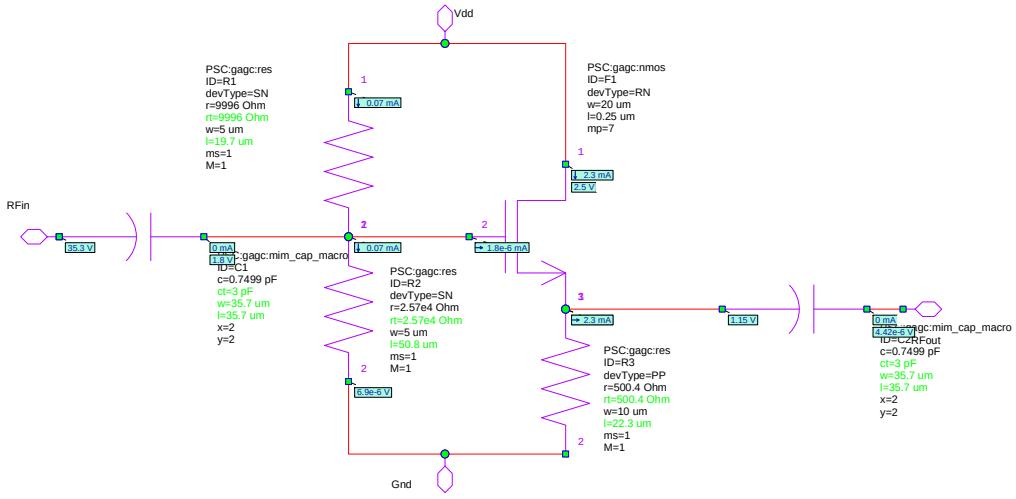


Figure 3.14: Source-follower amplifier circuit

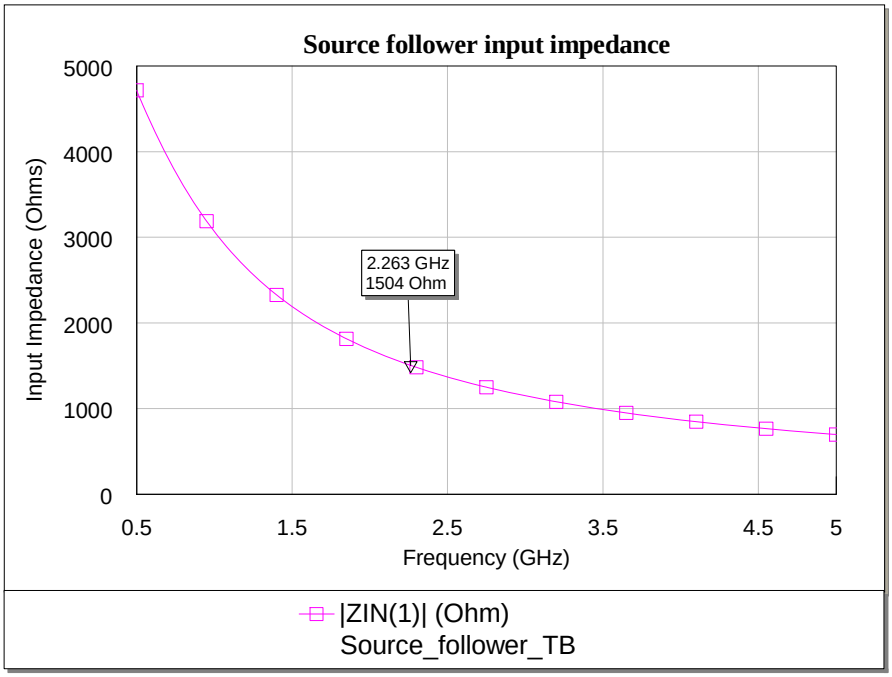


Figure 3.15: Source-follower amplifier's input impedance simulation

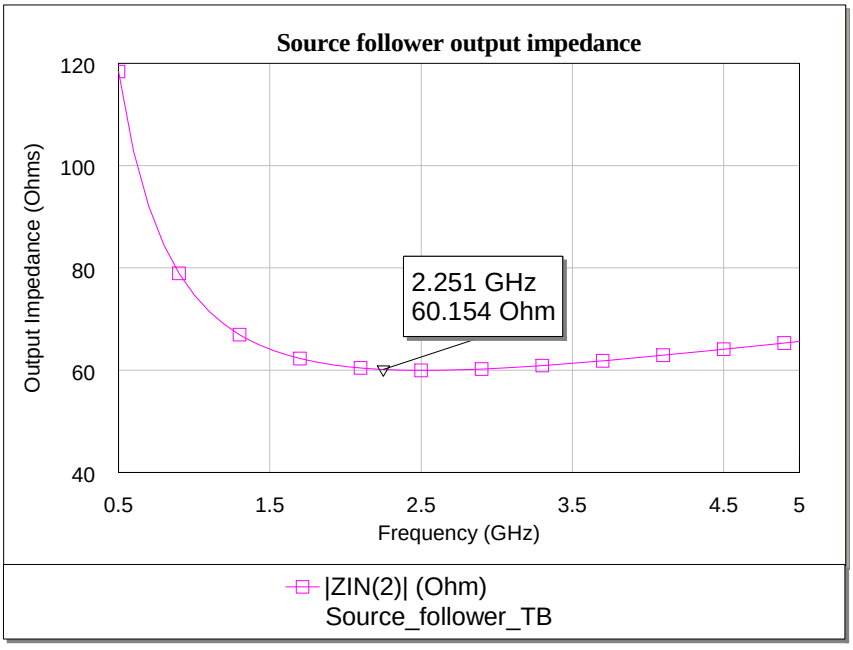


Figure 3.16: Source-follower amplifier's output impedance simulation

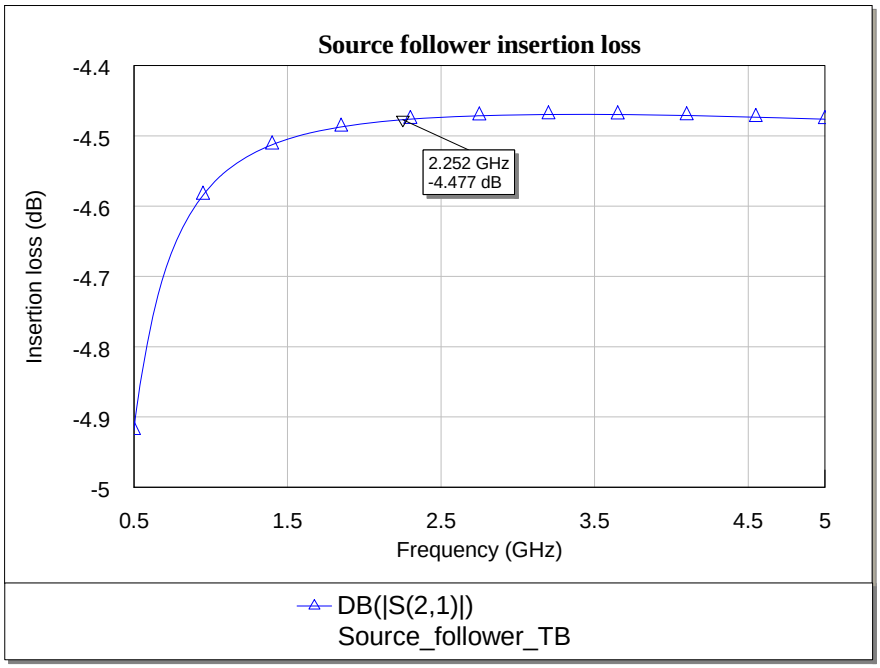


Figure 3.17: Source-follower amplifer's insertion loss simulation

3.3.5.2. Pi-Attenuator

A resistive pi-attenuator circuit was used as a means to adjust the complete oscillator circuit's output power to the proper levels and provide additional isolation to the oscillator tank circuit. The pi-attenuator 's resistor values are calculated using the following equations [13]:

$$R_1 = \frac{(K-1) * Z_1\sqrt{Z_2}}{(K+1)\sqrt{Z_2} - 2\sqrt{K * Z_1}}$$

$$R_2 = \frac{(K-1) * Z_2\sqrt{Z_1}}{(K+1)\sqrt{Z_1} - 2\sqrt{K * Z_2}}$$

$$R_3 = \frac{K-1}{2}\sqrt{\frac{Z_1 * Z_2}{K}}$$

Where Z_1 is the characteristic input impedance to the attenuator; Z_2 is the characteristic output impedance of the attenuator; K is the linear attenuation factor; R_1 is the input shunt resistor; R_2 is the output shunt resistor and R_3 is the in-series resistor. From earlier simulation results of the input and output impedances of both the source follower amplifier and high-isolation buffer amplifier, Z_1 is known to be 60.2 Ohms, Z_2 is known to be 86.2 Ohms. Therefore, a 16 dB attenuator will require R_1 to be 76.9 Ohms, R_2 to be 130.14 Ohms and R_3 to be 221.7 Ohms. Figure 3.15 shows the S-parameter simulation results of the pi-attenuator.

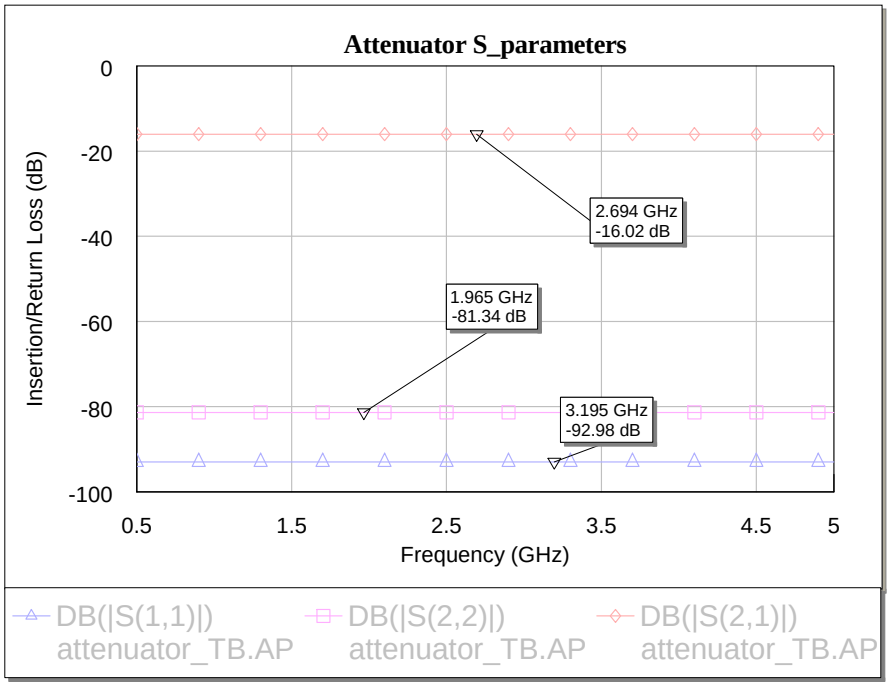


Figure 3.18: S-parameter simulation results for the resistive pi-attenuator

3.4. Full VCO Simulation Results

The entire VCO circuit (shown in figure 3.11) was simulated to ensure it met all of the specifications outlined in section 3.1 to include VCO output frequency, output power, phase-noise, power consumption and spectral content. Amplitude and phase balance as well as oscillator start-up was simulated as well. Initially a load-pull simulation was not done (it was incorrectly assumed that the amount of isolation between the VCO core and output buffer was adequate to meet specifications) but was done after a load-pull test was performed to check for correlation between the simulation and test results.

3.4.1. Output Frequency

The VCO frequency was simulated using both Harmonic Balance and HSPICE transient simulation techniques. Although slight differences in frequency were shown, the complete VCO circuit covered the entire required frequency range in the linear portion of the tuning curve with a tuning slope of approximately 142 MHz/V. The output frequency was covered with a 0.1 pF off-chip capacitor being used in the resonant tank circuit. Figure 3.8 shows a plot of the output frequency versus tuning voltage for the complete VCO circuit.

3.4.2. Output Power

A harmonic balance simulation was performed to ensure that the VCO circuit meet the minimum output power requirements while, at the same time, ensuring that the buffer amplifier isn't being driven into compression. Figure 3.16 is a plot of the output power versus tuning voltage and shows that between 0.8 V and 1.5 V (which correspond to 2200 MHz and 2300 MHz respectively), the output power of the VCO is between +1 dBm and 0 dBm. This meets the minimum required power output of 0 dBm. This simulation also shows that the output buffer amplifier has not reached its 1 dB compression point of +2 dBm.

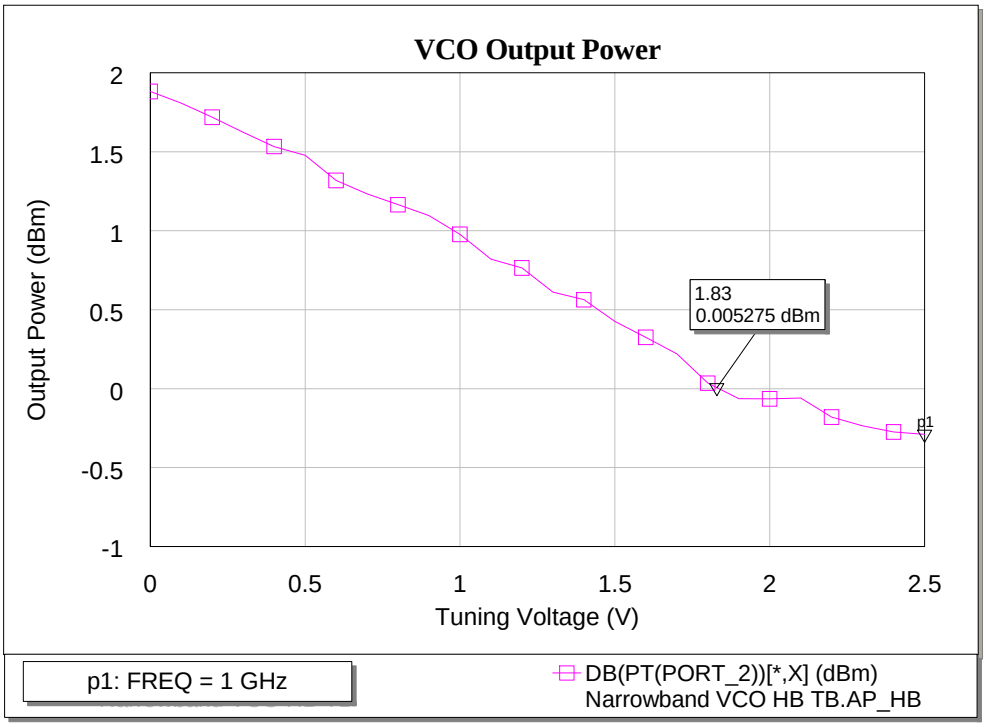


Figure 3.19: VCO output power harmonic balance simulation results.

3.4.3. Phase Noise

As previously mentioned, the phase-noise of an oscillator can be estimated using the simplified Leeson's phase-noise equation 3.1. This equation is, at best, a linear approximation of the phase-noise and is generally used as a guideline to show circuit designers that to achieve an oscillator with good phase-noise performance, the tank circuit voltage oscillation should be maximized while the series resistance of the tank inductor should be minimized. It also shows that a device with good $1/f^2$ noise corners plays a substantial role in the phase noise performance as well. There are other approaches in calculating the phase-noise such as using the Craninckx linear phase noise formula (which is nearly identical to the Leeson's model) or using Rael's non-linear mixer formula (again, very similar to the Leeson's model) [8]. All of these formula's require an accurate $1/f^2$ noise corner parameter and are usually not given for all device types (which was the case for the Peregrine design manual). Thus, a non-linear, harmonic balance simulation was used in determining if the oscillator meets phase noise requirements. Figure 3.17 shows that oscillator has a maximum phase-noise of -87.16 dBc/Hz at a 100 kHz offset thus meeting the requirement of -80 dBc/Hz specified in section 3.1.

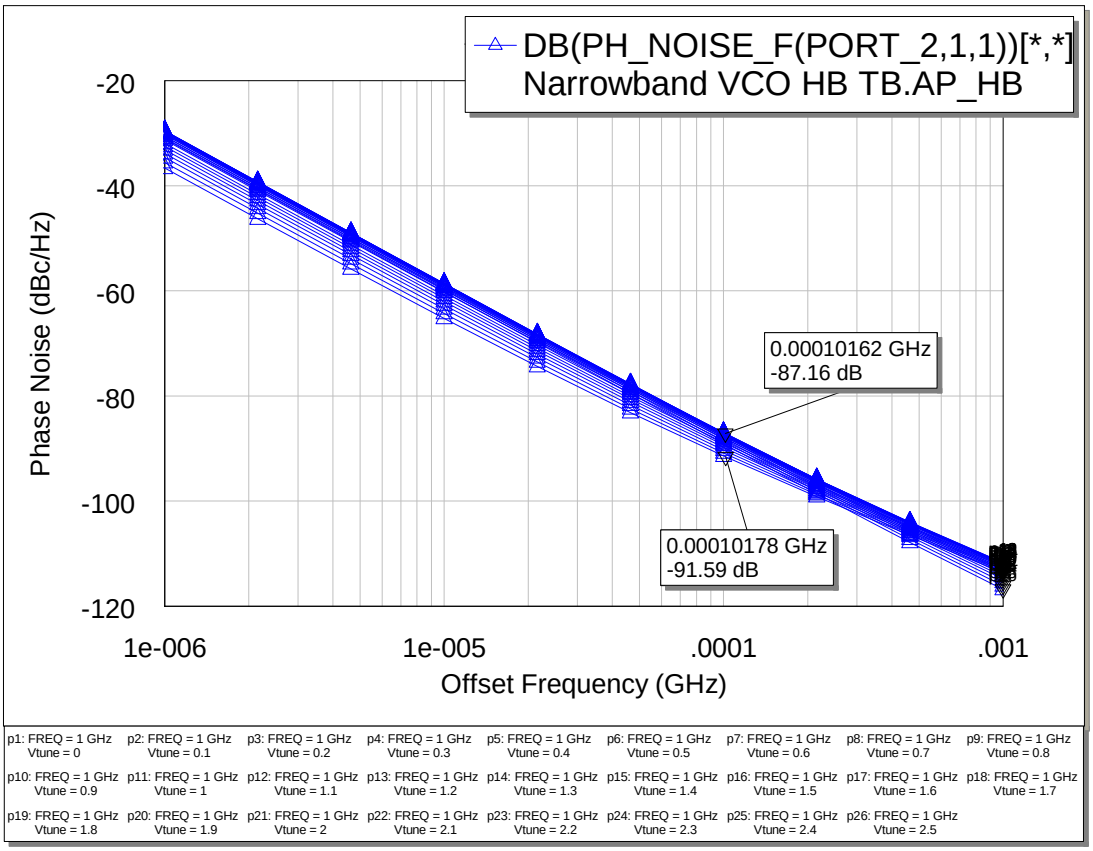


Figure 3.20: VCO phase-noise harmonic balance simulation results.

3.4.4. Spectral Purity

The spectral purity of the VCO was checked to ensure that the harmonics generated by the oscillator meet the minimum -45 dBc requirement. Generally LC oscillators have high (>-20 dBc) harmonic content due to relatively low tank Q's (when compared to oscillator's that have crystal or dielectric resonators with Q's in the thousands or tens of thousands). Since neither the high-isolation buffer amplifier or the source follower amplifier had any kind of input or output matching circuitry that

would provide harmonic rejection, a Minicircuits LFCN-2250+ low pass filter was used to lower the harmonics below the -45 dBc requirement (see appendix A for the LFCN-2250+ data sheet). Figure 3.18 shows that the oscillator meets all requirements for spectral purity.

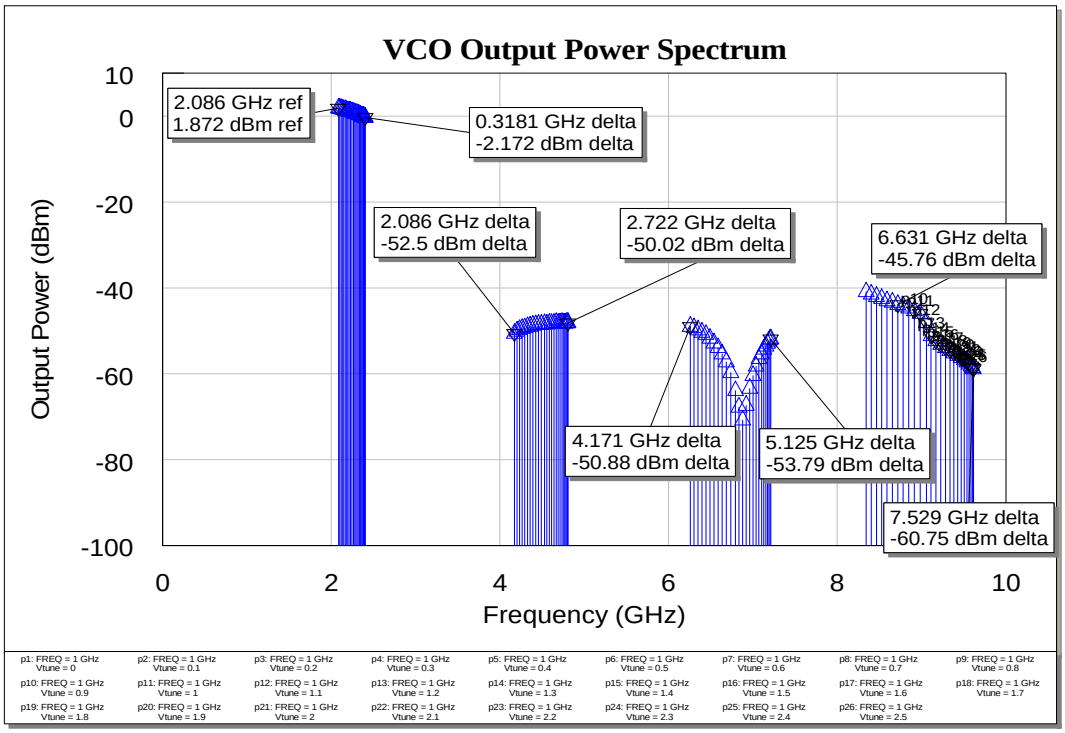


Figure 3.21: VCO output power spectrum simulation results.

3.4.5. Oscillator Start-up Transient

Oscillator start-up is an important condition to simulate to ensure the oscillator core has enough loop gain to overcome the resonator parallel resistance and begin oscillating. In the simulation, a small current spike (0.1 mA for 10 picoseconds) is

injected into the feedback loop in-order to simulate noise. This noise should "kick-start" the oscillator core into oscillating. The calculated loop gain was approximately 5 (from section 3.3.3) which should be enough to ensure start-up. Figure 3.21 shows that the oscillator starts up and attains steady state oscillation in approximately 25 nanoseconds.

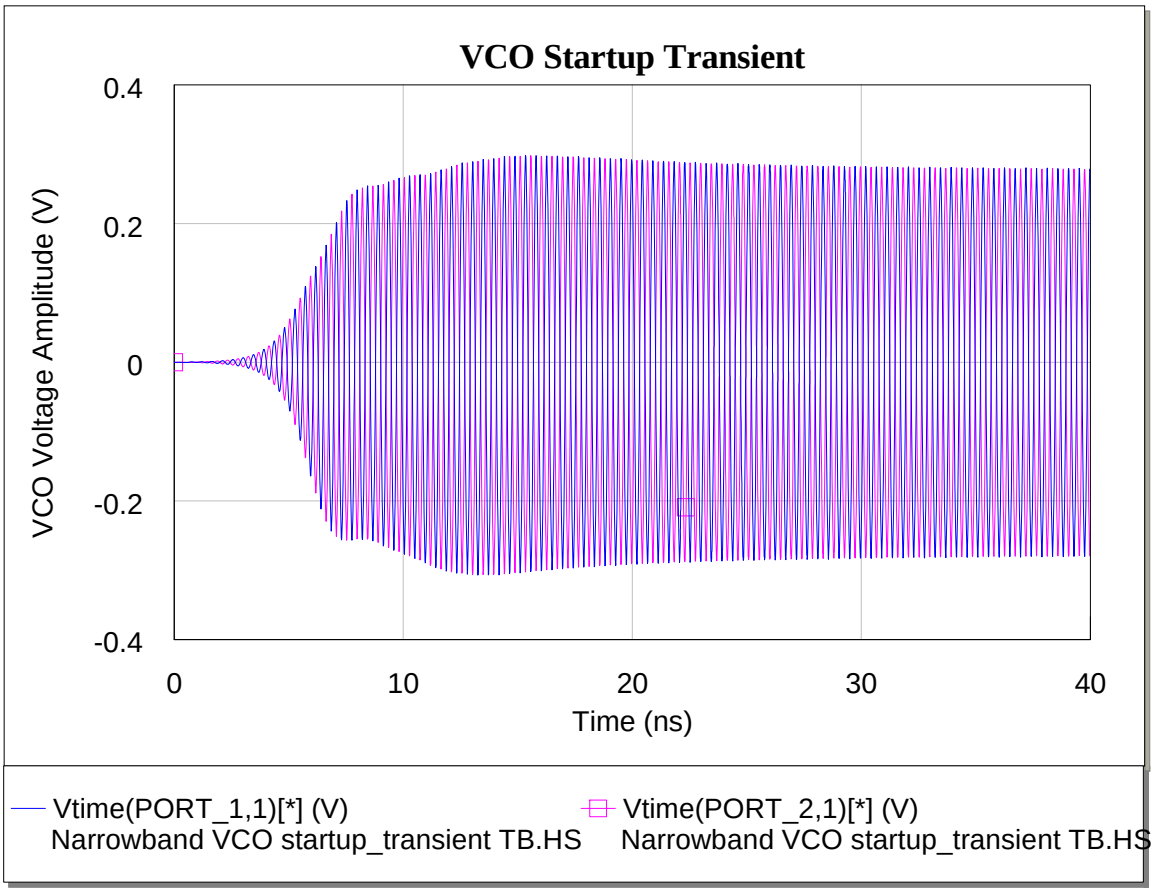


Figure 3.22: VCO start-up transient simulation results

3.4.6. Amplitude and Phase Balance

Another important parameter in differential oscillator design is amplitude and phase balance. Since the oscillator core is differential by design, the oscillating voltage amplitude on each output arm of the core should be exactly 180 degrees out-of-phase. Slight asymmetries in each single-ended tank circuit's inductive or capacitive properties can cause a small difference in relative oscillation frequency between both sides of the oscillator core. This difference in frequency translates into phase imbalance where the oscillator's output isn't exactly 180 out-of-phase. Amplitude imbalance will occur when there is a difference in loop gain between the two sides of the differential oscillator core which could be caused by a mismatch in PMOS device transconductance. Great care should be when matching the negative resistance generators FET sizes to minimize this amplitude imbalance. Figure 3.32 shows the single-ended output (referenced to ground) of both ports. The figure shows the relative phases of each output to be exactly 180 degrees out of phase and the amplitudes to be within 0.5 mV.

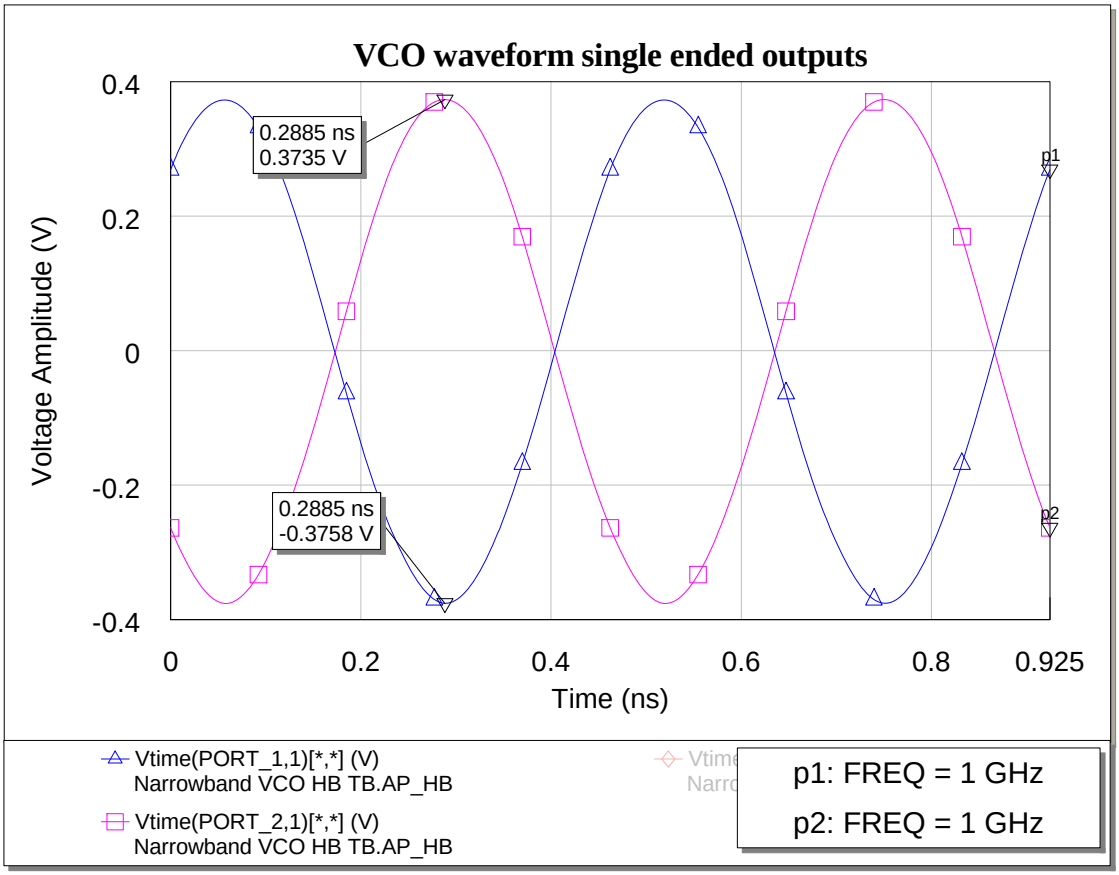


Figure 3.23: VCO single-ended waveform simulations

3.4.7. RF Load-Pulling

As previously mentioned, an RF load-pull simulation was not performed because it was incorrectly assumed that the high-isolation buffer amplifier, with 60 dB of simulated reverse isolation and the 16 dB pi-attenuator along with the reverse-isolation provided by the source follower amplifier would be adequate enough to prevent a 3:1 load mismatch from pulling the oscillator core by more than a few kHz.

Subsequent testing proved this to not be the case and a load pull simulation was performed after the testing to try and establish a correlation between testing and simulation. Figure 3.19 shows that a harmonic balance load pull simulation in which a 3:1 VSWR load was placed on one end of the oscillator's output (while the other end was driving a 50 Ohm load). The phase of the load was then moved from 0 degrees, to 90 degrees, 180 degrees and 270 degrees. The output frequency of the VCO was simulated to change by more than 560 kHz from 90 degrees to 180 degrees which does not meet the RF load pulling requirement of less than 10 kHz of pulling at all phases.

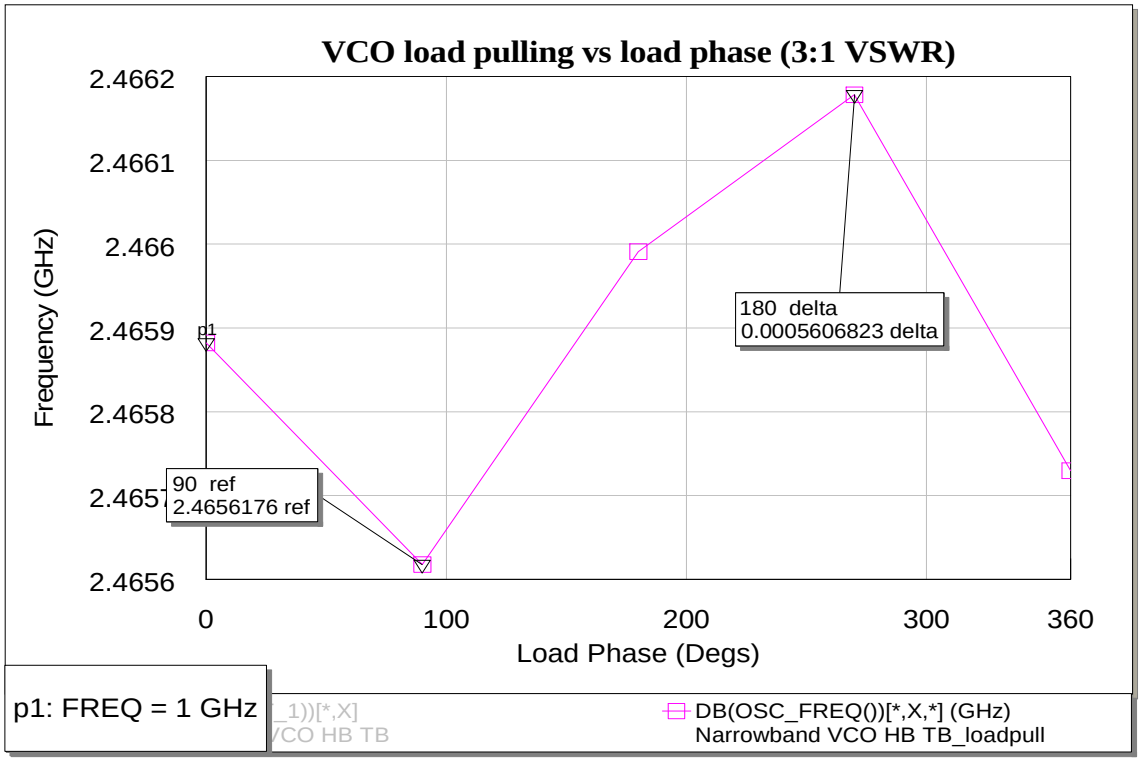


Figure 3.24: VCO load pulling vs phase simulation results.

3.4.8. DC Power Consumption

The full VCO circuit was simulated to dissipate approximately 83 mA of DC current with a 2.5 V power supply. This was less that the 100 mA maximum DC power consumption required in section 3.1

3.5. VCO Testing and Measurement Results

The VCO was tested by having a test circuit built on a 15 mil thick Roger's corporation TMM10i substrate. The test circuit was setup such that the VCO could be tested in an open loop configuration where the tuning voltage could be independently tuned and the output power for each port could be measured in a single-ended configuration. Figure 3.22 shows the test circuit with the off-chip tuning capacitors and 1 kOhm current-source resistor.

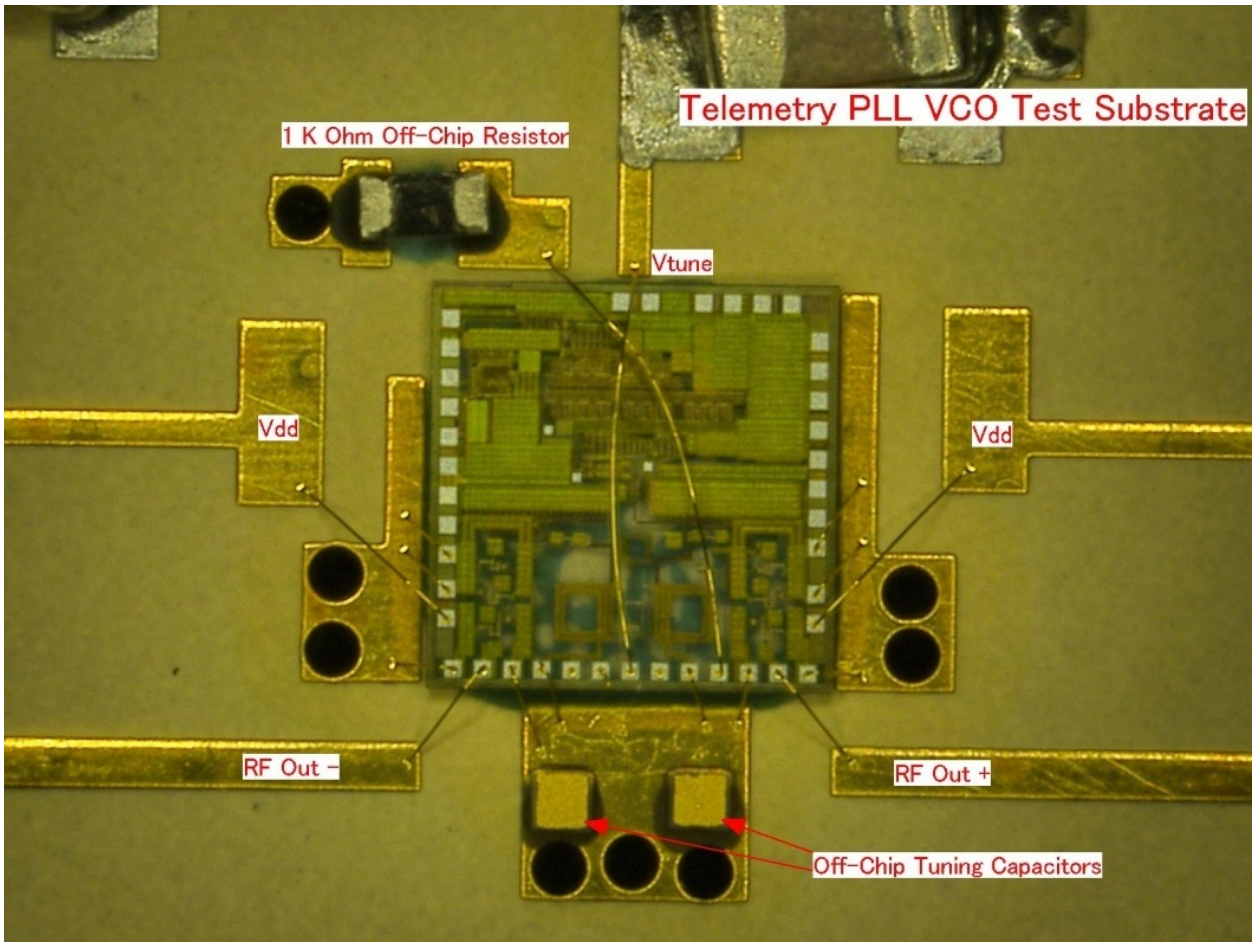


Figure 3.25: VCO test circuit

3.5.1. Measured Output Frequency and Power

The VCO output frequency was measured using an Agilent E4407 B series spectrum analyzer. The tuning voltage, V_{tune}, was stepped from 0 V to 2.5 V at 0.1 V increments and the frequency and power were measured at each interval. Figure 3.25 shows the simulated and measured output frequency versus tuning voltage with and without the 0.1 pF off-chip tuning capacitor being bonded onto the oscillator tank.

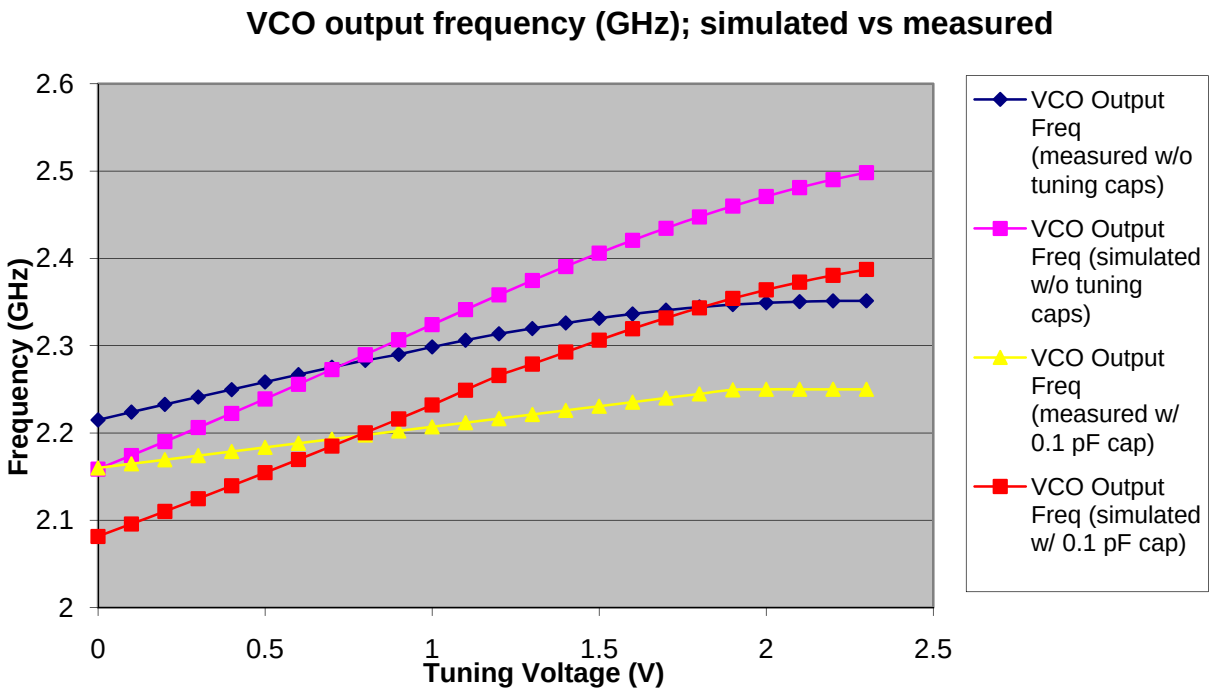


Figure 3.26: Simulated and measured VCO frequency vs tuning voltage

The above figure shows a discrepancy in the tuning range and tuning slope of the VCO when comparing the measured and simulated results. In simulation, it was found that, with an off-chip tuning capacitor with a value of 0.1 pF, the entire tuning range of 2.2 to 2.3 GHz could be covered from 0.8 V to 1.5 V giving a tuning slope of 142.8 MHz/V. When measured, the tuning range of the VCO, from 0 V to 2.25 V, was 2.215 GHz to 2.352 GHz without the off-chip tuning capacitor and 2.16 GHz to 2.25 GHz with the 0.1 pF capacitor in-place. This gives a tuning slope of 54.8 MHz/V and 36 MHz/V respectively. It is believed that the discrepancy between the simulated and measured results are due to a parasitic capacitances in the layout of the

tank circuit, along with potential modeling errors of the intrinsic NMOS inversion mode varactors.

To mitigate this problem for next design iteration, a parasitic extractor will be used to ensure all of the oscillator tank's parasitics are accounted for in the simulation. Also, an on-chip, FET switchable, capacitor will be employed to add a course frequency tuning step to the tank circuit. This will, in-effect, act like the off-chip capacitor that is in the current VCO design only the capacitor can be switched in and out by the internal PLL logic.

Figure 3.26 (below) shows the simulated and measured power versus tuning voltage for both output ports of the VCO.

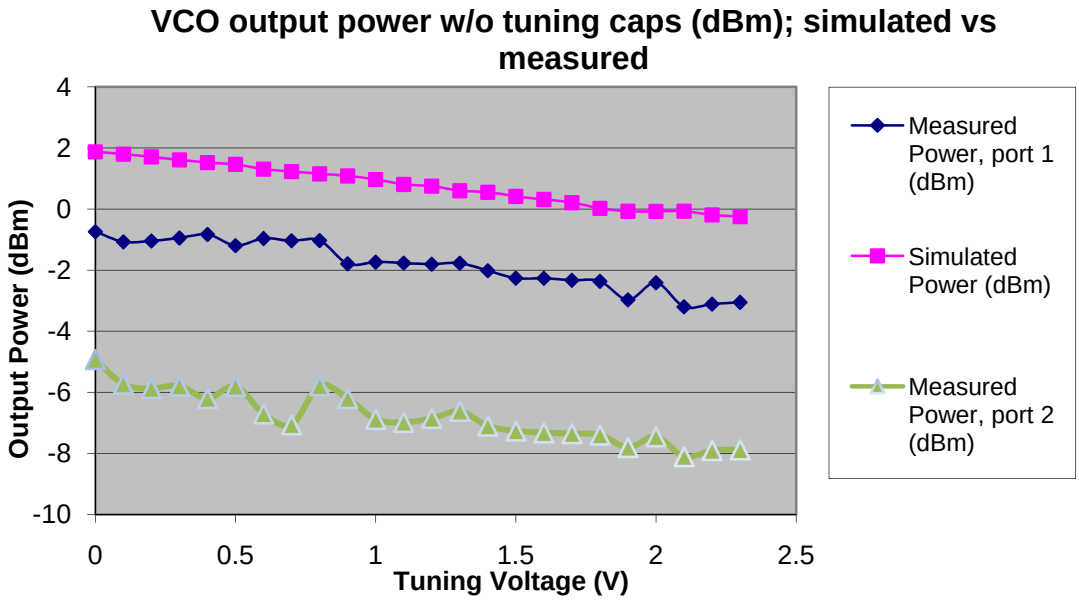


Figure 3.27: Simulated and measured VCO output power vs tuning voltage

The plots in the above figure shows an approximately 2.5 dB drop in output power when comparing the port 1 power and simulated power. The plot also shows a drop of approximately of 7 dB when comparing the port 2 power and simulated power as well. The low output power of both ports can be explained by the fact that there is lower than expected gain from the high-isolation buffer amplifier (see section 2.3). The difference in output power between the two ports, more than likely, can be attributed to the pi-attenuator circuit as the resistor values can be skewed ±15% which can cause a wide variance in attenuation thus causing a fairly wide variance in output powers.

In the next design iteration, the pi-attenuators will be removed and multiple lossy source follower amplifiers will be added to the VCO output chain to provide the required attenuation and isolation that the pi-attenuator provided. In-addition to these changes, the high-isolation buffer amplifier will be redesigned to be a fully differential, cascode-amplifier. This new amplifier configuration will help to ensure the output power is symmetrical and accurately portrayed in simulation.

3.5.2. Measured Phase Noise

The phase noise of the VCO was measured using an Aeroflex PN9000 Automatic Phase-Noise Analyzer. Although the measurement of the phase noise was taken while the VCO was in phase lock, the offset frequency of interest, 100 kHz, was well outside the loop bandwidth of the PLL. This region of the total phase-noise measurement is dominated by the phase noise contributions of the VCO [10]. Figure 3.27 shows that the measured phase-noise of the PLL was approximately -90 dBc/Hz at a 100 kHz offset meeting the requirement of -80 dBc/Hz .

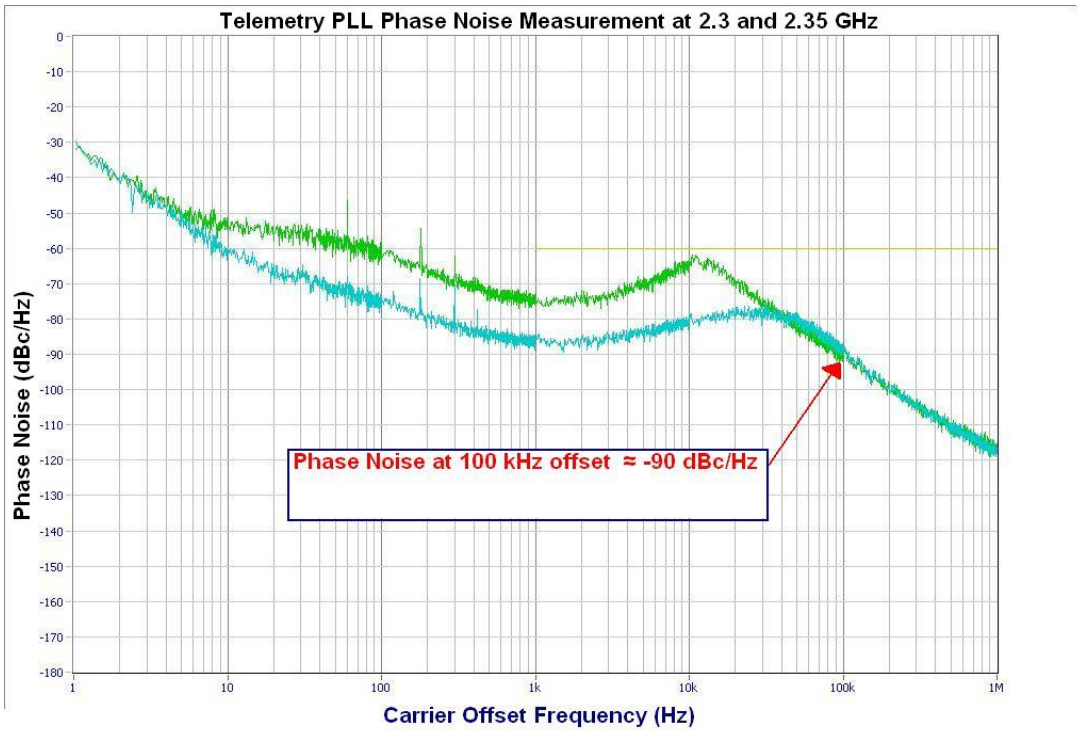


Figure 3.28: Measured phase-noise of the VCO at 100 kHz offset

3.5.3. Measured Spectral Purity

The harmonics of the VCO were measured at output port 1 while the output port 2 was terminated with a 50 ohm load. The VCO was tested at the low end of it's operational frequency range, at 2.215 GHz and then at the high end of frequency range, 2.35 GHz. The harmonics were measured out to the 4th harmonic and are shown below in table 1. The harmonic measurements meets spectral purity requirements put forth in section 3.1.

Table 1: VCO harmonic measurements

VCO Fundamental Frequency (GHz)	2nd Harmonic level (dBc)	3rd Harmonic level (dBc)	4th Harmonic level (dBc)
2.215	-50.1	-49.2	-45.1
2.35	-47.2	-51.5	-51.2

3.5.4. Measured Phase and Amplitude Balance

The phase and amplitude balance where checked by measuring each of the VCO output ports as single-ended signals and compared against each other. Figures 3.28 and 3.29 show a distinctive amplitude imbalance between the signals at port 1 and port 2. This imbalance was expected because the output power discrepancy measured in section 3.5. Figures 3.28 and 3.29 show the VCO output waveforms with horizontal cursors on port 1 and port 2 respectively. Port 1 shows a peak-to-peak amplitude of 296 mV while port 2 shows a peak-to-peak amplitude of 160 mV

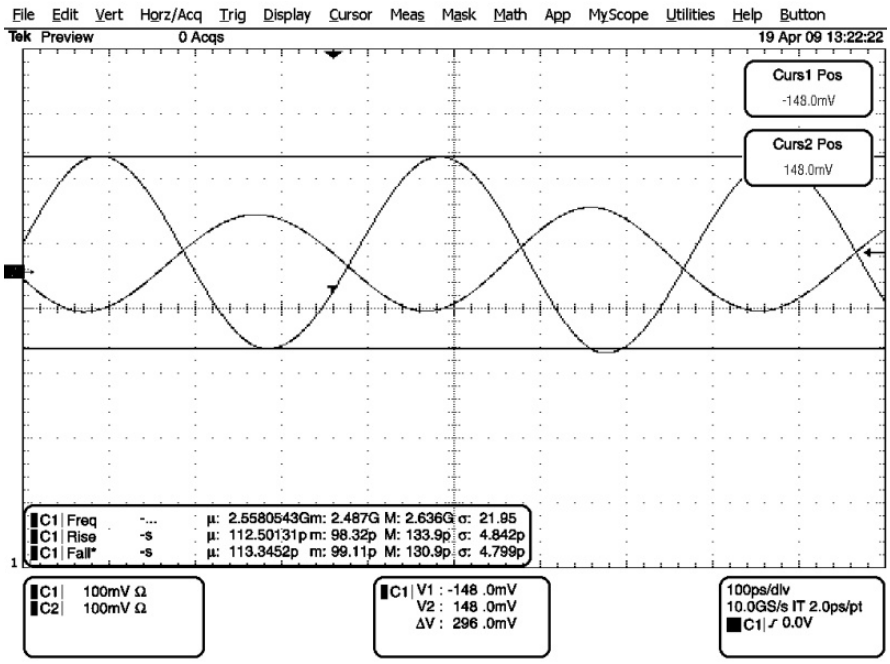


Figure 3.29: Measured VCO voltage waveform with horizontal cursors on port 1 output

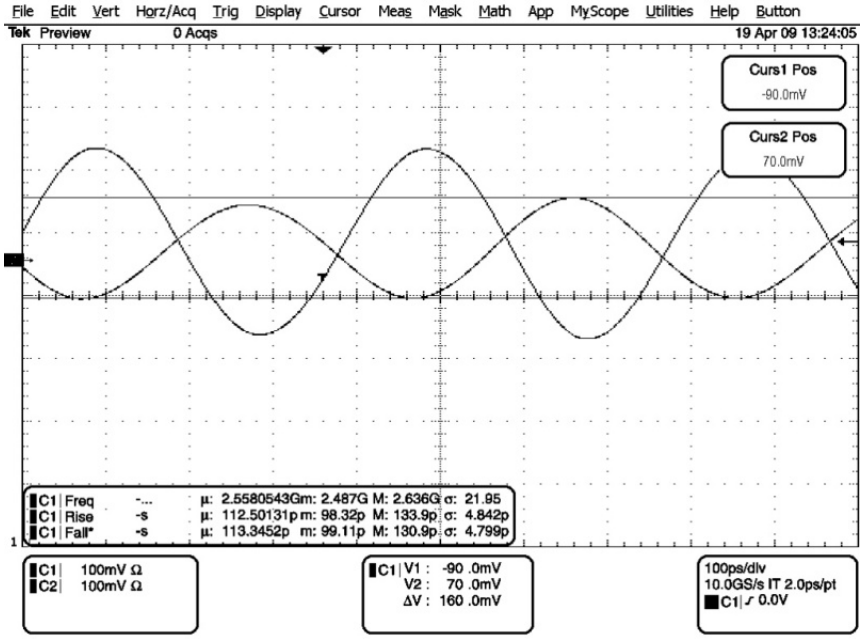


Figure 3.30: Measured VCO voltage waveform with horizontal cursors on port 2 output

The phase imbalance was measured by placing a vertical cursor on the positive peak of the port 2 waveform and the negative peak of the port 1 waveform. Figure 3.30 shows that the difference between the two peaks is 18 picoseconds which corresponds to a 4.17% phase-imbalance at waveform frequency of 2.315 GHz. This is more than likely due to slight geometry imbalances in the VCO tank circuit. This will be resolved in the next design iteration by ensuring that both sides of the tank circuit have a higher degree of symmetry than the current VCO tank circuit layout.

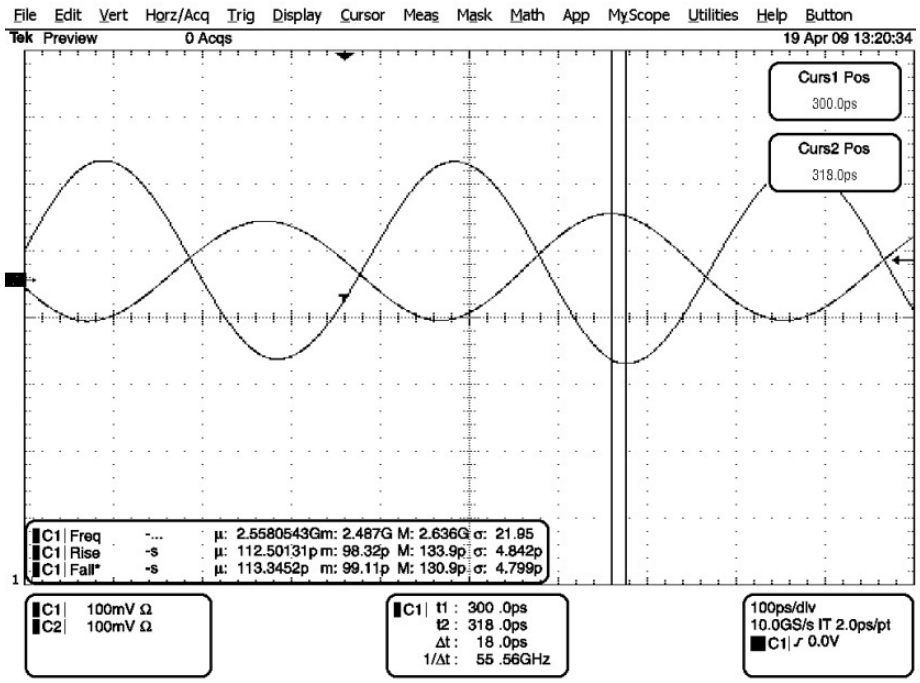


Figure 3.31: VCO voltage waveform with vertical cursors measuring phase imbalance.

3.5.5. Measured RF Load- Pulling

The RF load pulling was measured using a Maury Microwave load-pull test system. This test system allows the output load reflection coefficient to set as high as 0.95 at virtually any phase on the smith chart. The VCO was tested at 5 points on the Smith chart that correspond to the matched case (50 Ohms) and 4 points with a reflection coefficient of 0.5 at 0, 90, 180 and 270 degrees. Figure 3.31 shows the points on the smith chart that were tested and table 1 shows the frequency pulling test results.

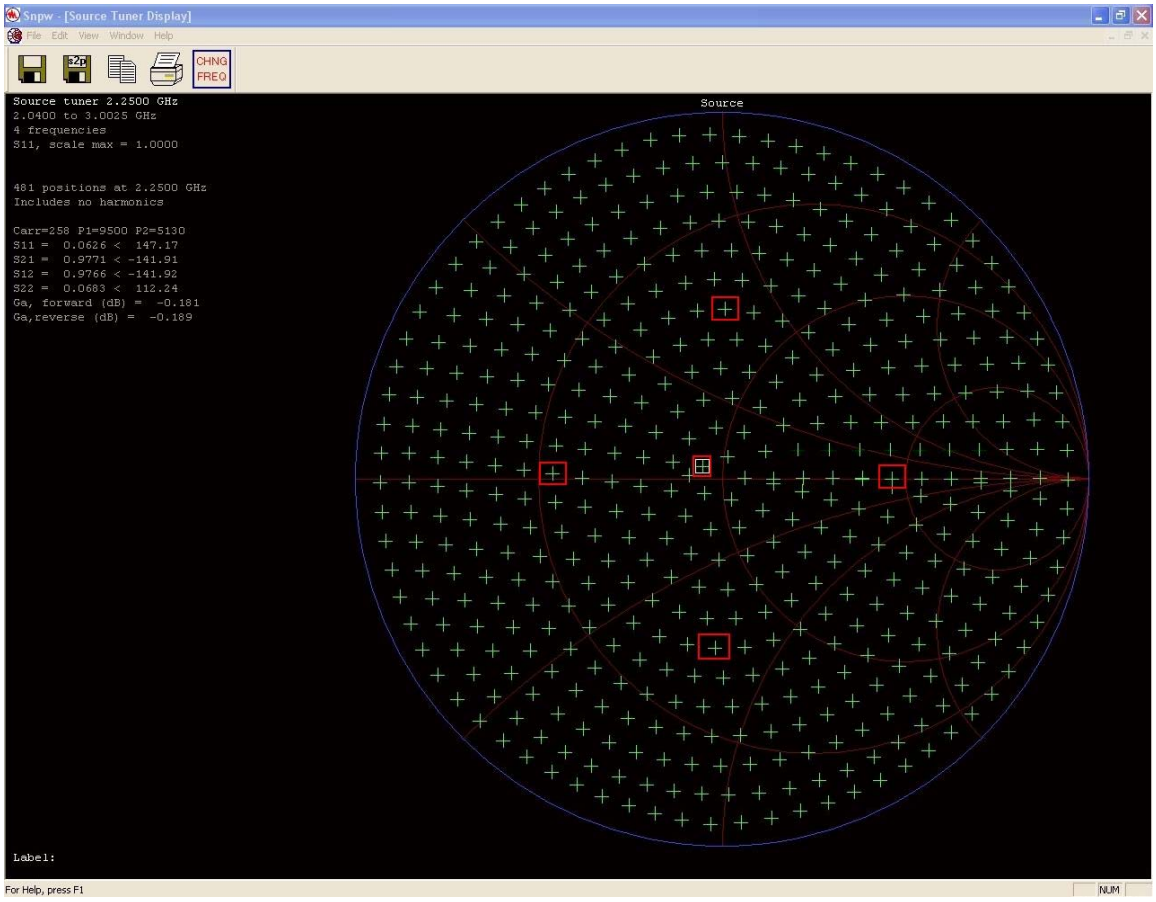


Figure 3.32: Smith chart showing RF load values where frequency pulling was measured

Table 2: RF load pulling measurements

VCO Frequency (GHz)	delta Frequency (Hz)	Load Reflection Coefficient (mag < angle in degrees)
2.257855	-	0.0626 < 147.17
2.257145	710000	0.541 < 177.41
2.257773	82000	0.546 < 92.31
2.257588	267000	0.545 < -0.06
2.257458	397000	0.542 < -89.5

The results from the load-pull test clearly show that the buffer does not provide the adequate isolation for a 3:1 all-phase mismatch. This was also shown in a load-pull simulation performed after the VCO was designed and sent to the foundry and will clearly need to be done at an earlier point in the design stage for the next design iteration.

3.5.6. Measured DC Power Consumption

The VCO consumed 85.2 mA of DC current with a 2.5-V power supply. This is within 3 mA of the simulated DC current draw and below the 100 mA

4. S-band Voltage Controlled Oscillator, Second Design Iteration

The second design iteration of the voltage controlled oscillator design incorporated all aspects of the lessons learned from the testing and measurement of the high-isolation buffer amplifier and complete S-band, voltage controlled oscillator. This chapter briefly describes the redesign of the high-isolation buffer amplifier and voltage controlled oscillator core.

4.1. High-Isolation Buffer Amplifier Redesign Summary

The high-isolation buffer amplifier's initial design, although met all of the put forth design criteria in simulation, failed to meet the requirements when actual measurement data was taken. This included isolation and gain predictability along with output 1 dB compression point at the upper end of the frequency band. The faults with the amplifier were mainly contributed to Miller-effect capacitive multiplication along with a potentially unreliable resistive biasing configuration. To overcome these issues, a fully-differential, cascode amplifier configuration was chosen to replace the previous buffer amplifier design. As previously mentioned, the addition of a cascoding FET in series with the drain of the amplifying FET eliminates the miller-effect by isolating the output node of the amplifier from the input node of the amplifier. By using a differential amplifier configuration, greater amplitude and

power balance between the differential output ports can be assured. Figure 4.1 below shows the amplifier schematic with all circuit elements circled or labeled.

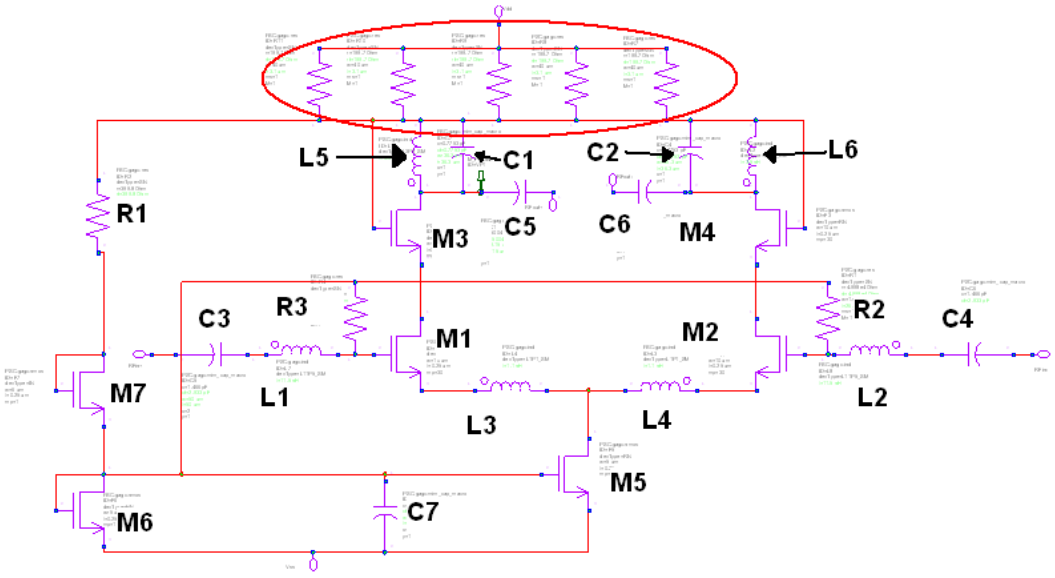


Figure 4.1: Differential, cascode amplifier schematic

In figure 4.1, FET's M1 and M2 are the common source amplification transistors for both sides of the differential amplifier while M3 and M4 are the cascoding FET's which are biased to always be in the saturation region. FET M5 is used as a constant current source for both sides of the amplifier and is itself biased by resistor R1 and the FET active loads M6 and M7. This biasing arrangement should provide a more consistent output power as both sides of the differential amplifier are biased by the same current source.

Inductors L3 and L4 are used as MOS source degeneration inductors which offsets the phase of the current flow through the source and the applied gate voltage. This has the effect of creating a resistive input impedance without the additive noise of a real resistor that is usually required for an optimum noise and power match [7]. Inductors L1 and L2 complete the input match for the differential amplifier by resonating out any gate-to-source capacitance. This arrangement provides a fairly narrowband match but we are interested in only providing a match from 2.2 GHz to 2.3 GHz. Inductors L5 and L6 along with capacitors C1 and C2 provide a tuned output match into the 50 Ohm system. The gates bias of M1 and M2 are provided by the same bias voltage that biases the gate of M5 through the high-value resistors R2 and R3. AC coupling for both the input and output ports of the amplifier are provided by capacitors C3, C4, C5 and C6. Bias decoupling is provided by capacitor C7. Finally, the resistors, circled in red, provide stabilization to the amplifier to ensure it is unconditionally stable.

4.1.1. Differential Amplifier Simulations

Simulations were run on the differential amplifier to determine the gain, isolation, input and output match, noise-figure and 1-dB compression point. Figure 4.2 shows the simulation results of the gain (S21), isolation (S12), input and output match (S11 and S22) and the amplifier noise-figure. This figure shows a narrowband gain at 2.25 GHz of 14.6 dB, an output match of -19.1 dB and noise figure of less than 2 dB . However, it shows an isolation of less than -40 dB which will require the use of

additional isolation circuit elements in the high-isolation buffer amplifier. Figure 4.3 shows that the amplifier is unconditionally stable up to at least 4 GHz with minimum stability factor K of 1.492 and stability parameter B1 of 0.036. Recall that for a amplifier to be unconditionally stabile, K must be greater than 1 and B1 must be greater than 0 simultaneously. Figure 4.4 shows that the 1-dB compression point to be approximately +1.2 dBm across the band.

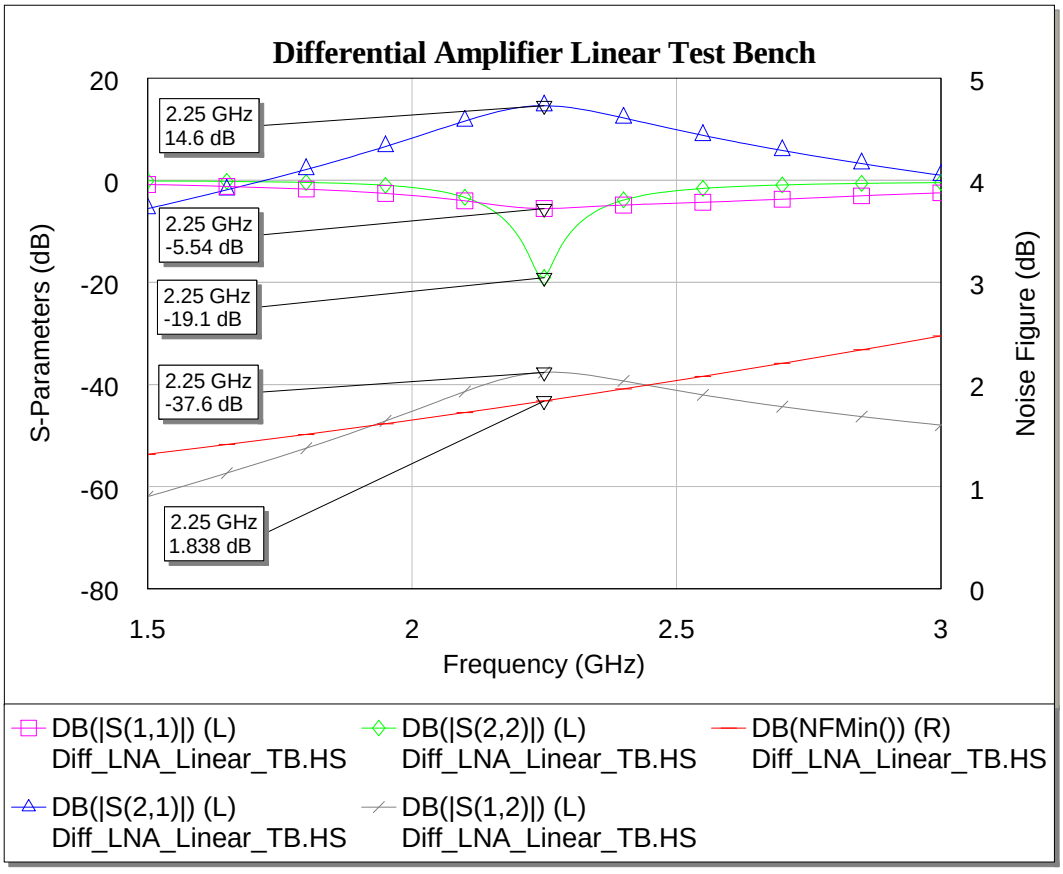


Figure 4.2: Differential amplifier linear test bench simulation results

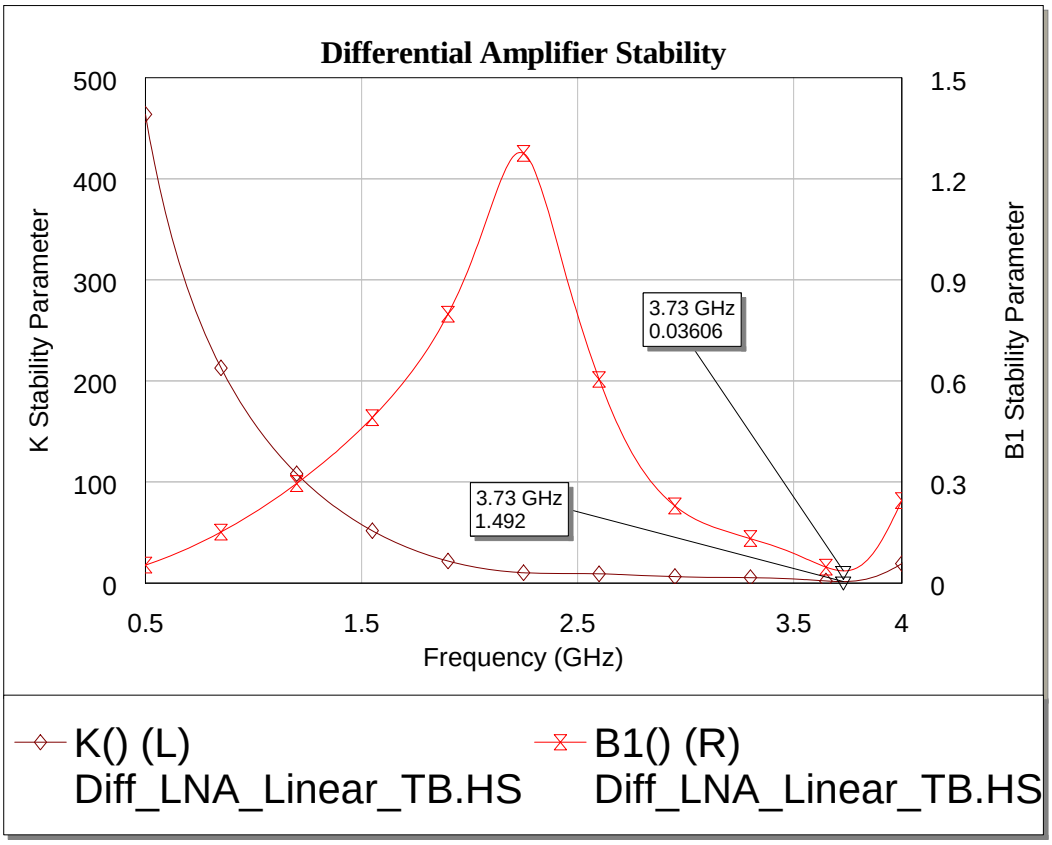


Figure 4.3: Differential amplifier stability simulation results

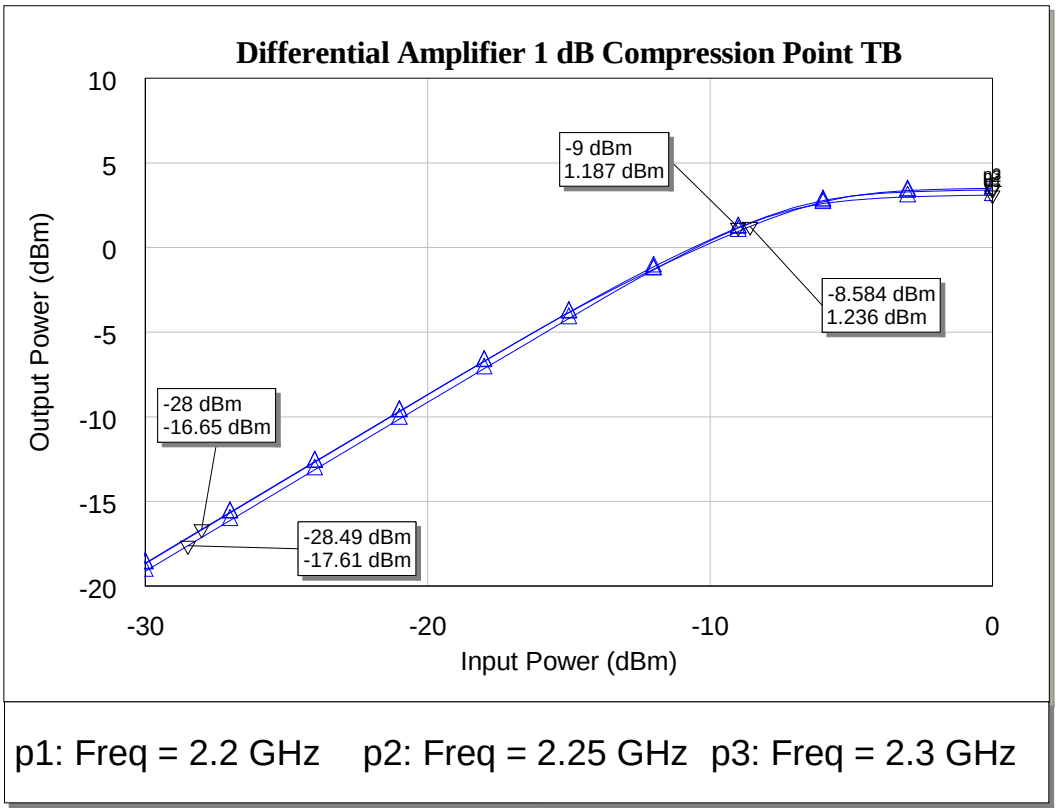


Figure 4.4: Differential amplifier 1-dB compression point simulation results

It was determined that to provide the additional isolation required by the buffer amplifier, a pair of source follower buffer amplifiers would be added to each differential path of the amplifier. The source follower circuit configurations are very similar to the circuit design in section 3.3.5.1 and a thorough examination will not be included here.

4.1.2. Completed High-Isolation Buffer Amplifier

Figure 4.5 shows a block diagram representation of the redesigned high-isolation buffer amplifier that includes the differential amplifier and 2 buffer amplifiers on each differential path. The addition of the source-follower amplifiers dropped the gain of the complete amplifier to 2.33 dB at 2.25 GHz and raised the noise-figure to 5.33 dB but the isolation increased from -37.6 dB to -92.3 dB. These trade-offs in performance were deemed acceptable and the simulation results are shown in figure 4.5. The layout of the new buffer amplifier front-end is shown in figure 4.7.

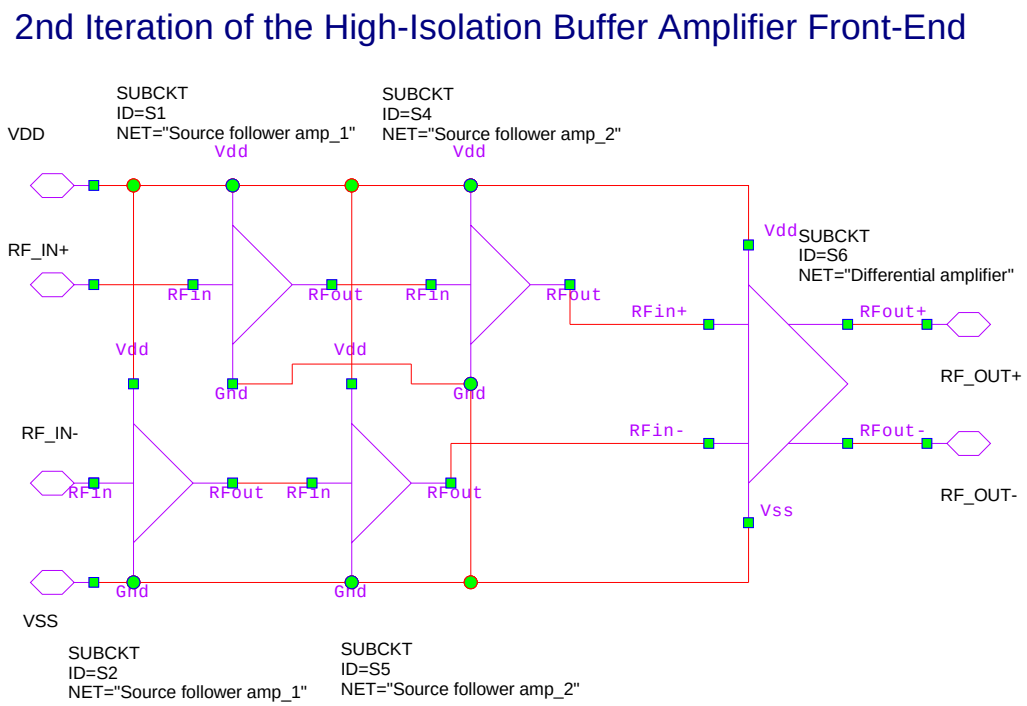


Figure 4.5: Second iteration high-isolation buffer amplifier block diagram

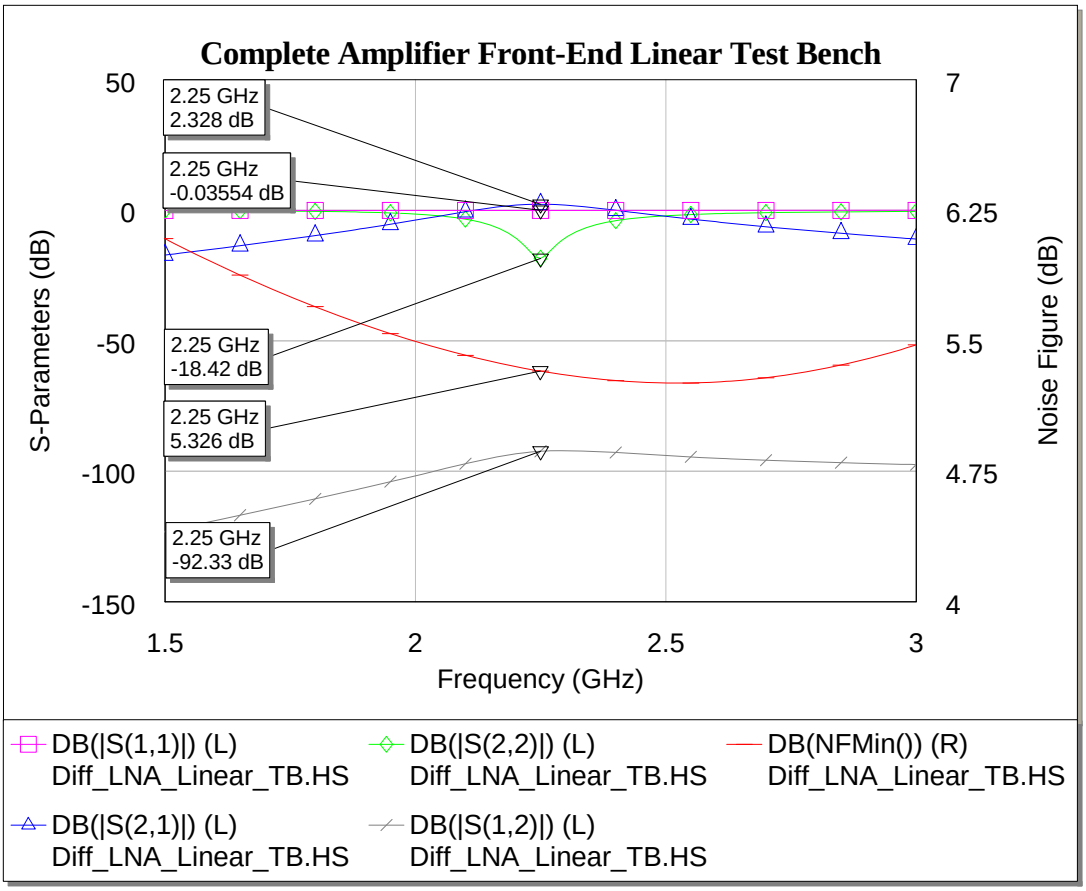


Figure 4.6: Complete buffer amplifier linear test bench simulation results

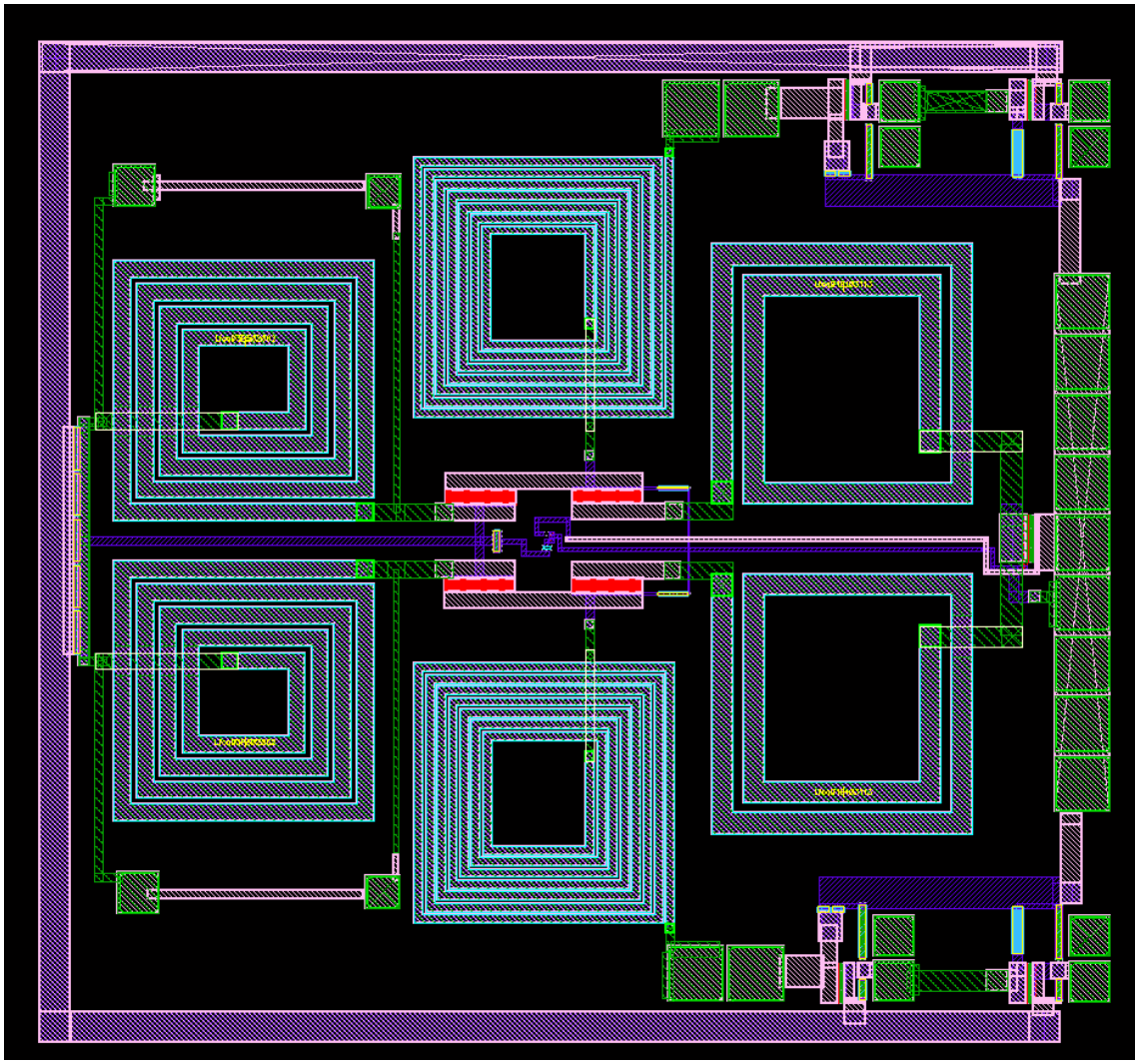


Figure 4.7: Layout of second iteration high-isolation buffer amplifier

4.2. Oscillator Core Redesign Summary

The VCO oscillator core had relatively few issues to resolve with the 2nd design iteration. The main issue that needed to be solved was that of accurate frequency prediction and tuning range. To solve the issue of frequency tuning range, an on-chip MIM capacitor along with a high-threshold FET was used to provide a course

frequency tuning step that is switchable by the PLL logic. This gives the VCO two distinctive frequency bands in which it operates that overlap thus giving the VCO an effective larger bandwidth in which to operate.

The other major change to the oscillator core topology comes in form of how the MOS varactors are biased. In the rev 1 VCO core design, the gates of the MOS varactors were biased to ground (thru the inductors) and the source and drain of the intrinsic NMOS device was tied to the control voltage. A simulation of the total varactor capacitance shows that a majority of the capacitance change occurs when the source-drain is negative with respect to the gate of the varactor. Since the PLL cannot provide a negative control voltage to the VCO, a large varactor was used to get the necessary 0.15 pF ΔC between 0.25 V and 2.25 V. To take advantage of the varactor's full capacitance change capability, the gate of the varactor was biased to 0.98 V using a high-impedance voltage divider and a 2 pF capacitor to provide AC coupling to the tank node of the oscillator. This allowed the MOS varactor to be scaled down from having 260 fingers to 50 fingers for a required ΔC of 0.15 pF. This also gave the VCO core a more linear frequency tuning curve than the previous topology. Figures 4.8 and 4.9 shows the varactor capacitance versus the source to drain voltage for the 260 x 2 μm x 0.25 μm device with the gate tied to ground and the 50 x 2 μm x 0.25 μm device with the gate tied to a 0.98 V bias voltage (respectively).

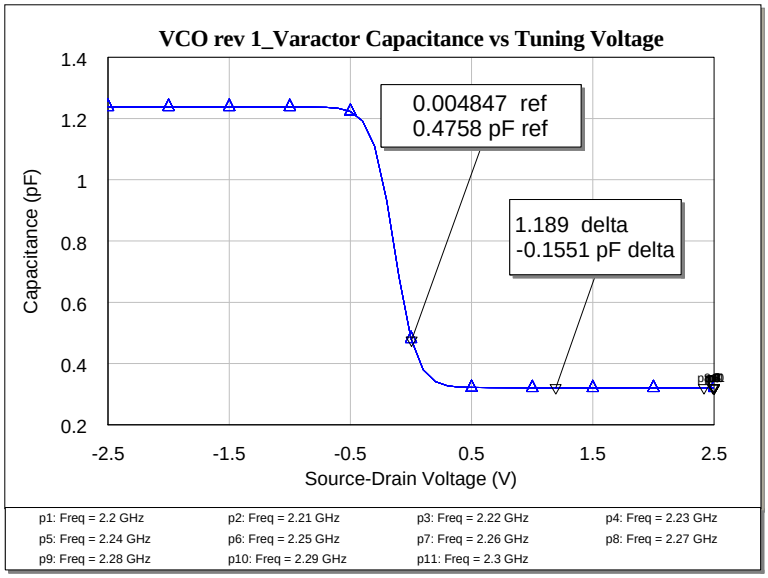


Figure 4.8: 260 X 2 µm X 0.25 µm device's capacitance vs source-drain voltage with the gate tied to ground.

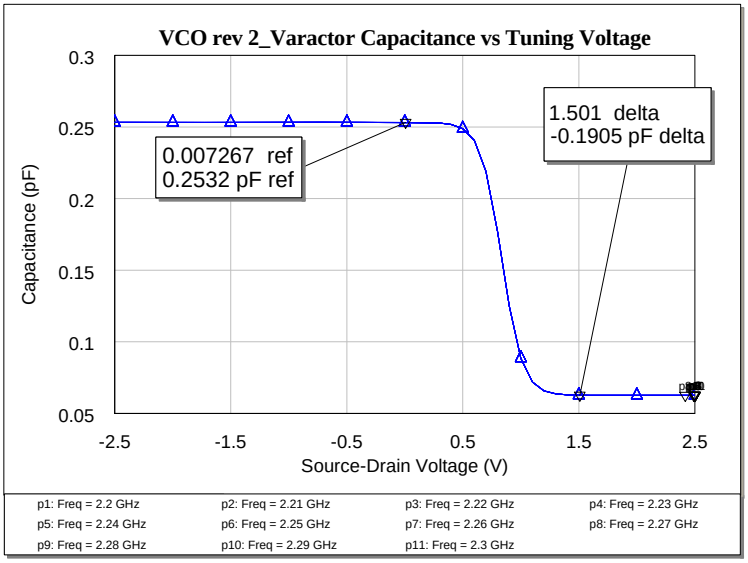


Figure 4.9: 50 X 2 µm X 0.25 µm device's capacitance vs source-drain voltage with the gate tied to 0.98 V.

In figure 4.10, the schematic of the rev2 VCO core is shown with all of the added components labeled. M1 and M2 are the high-threshold FET's that switch in C3 and C4 to give the oscillator the 2nd tuning band and extend the VCO's frequency range. The parasitic resistors P_R1 and P_R2 are not actually part of the circuit but are 1 MOhm parasitic resistors that were added to the schematic to help with convergence issues during the harmonic balance simulation. Capacitors C1 and C2 provide AC coupling to the varactors so that the bias voltage from the voltage divider from R1 and R2 doesn't affect the tank voltage node. They also help in reducing the finite varactor loss by a factor of $(C_{coupling}+C_{varactor})^2/C_{coupling}^2$ and decrease phase noise [15]. Additional source-follower amplifiers were also added to the core to provide more isolation to the entire VCO circuit

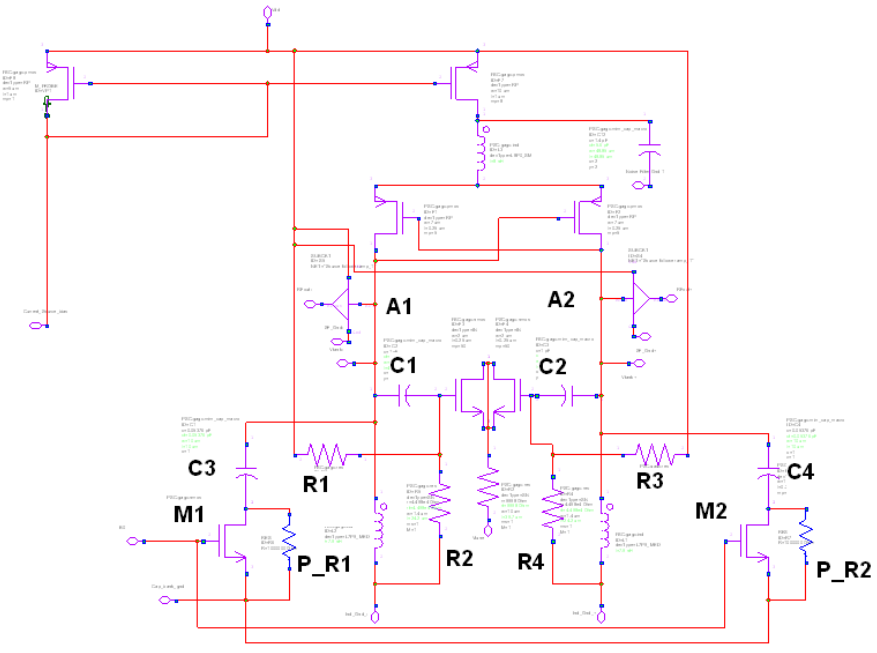


Figure 4.10: Second iteration of the oscillator core schematic.

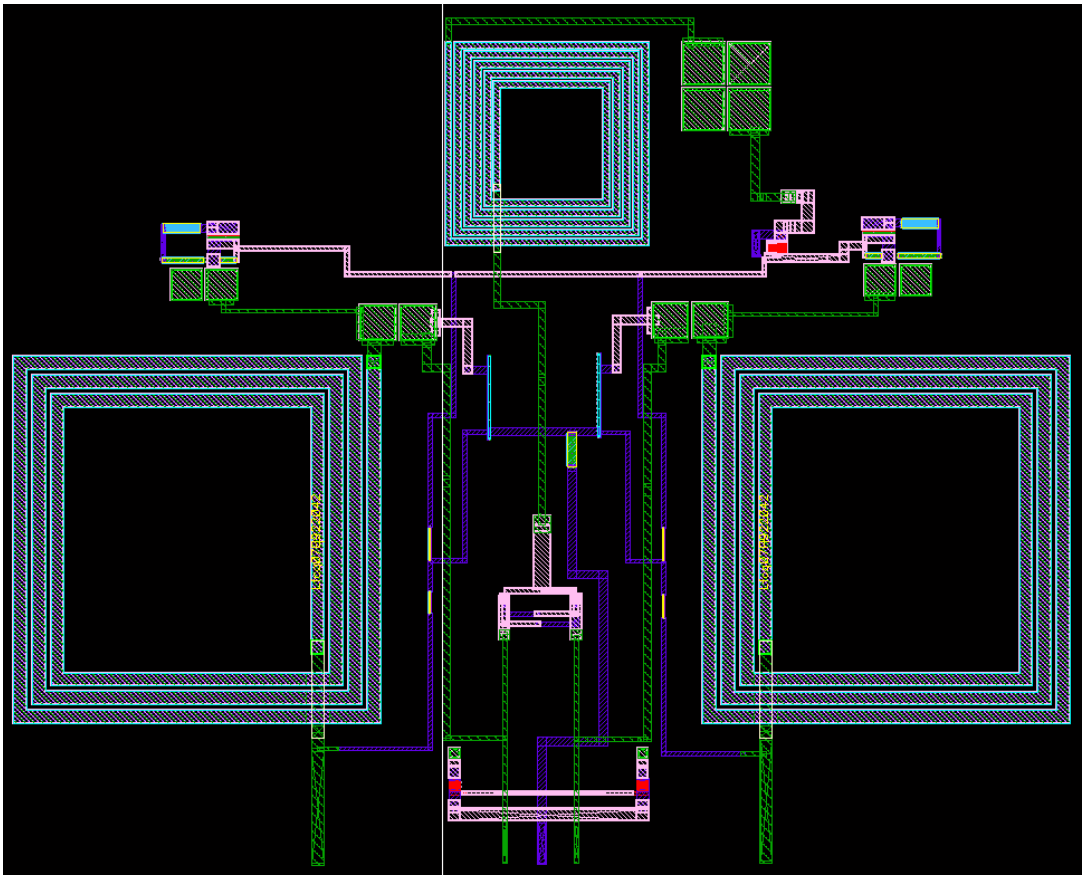


Figure 4.11: Layout of 2nd iteration VCO core

4.2.1. Second Iteration VCO Simulations

All of the simulations that were ran on the second design iteration of the complete VCO were done with all of the VCO core's interconnects extracted by a 1st order RLC extractor. The extractor takes into account all of the interconnects series resistance, net loop inductance and shunt capacitance and places these parasitic elements in the simulation. This was critical for the oscillator core as any unaccounted for parasitic elements in this portion of the tank circuit can cause the

oscillation frequency to be out of the intended frequency range. The unaccounted parasitics are more than likely the cause of the first VCO design to be off in frequency. The simulations were performed with the course tuning capacitor switched in and out by the switch bit B0. Figure 4.11 and 4.12 show the frequency tuning range and power versus tuning voltage. These simulations show that VCO meets the frequency range and output power requirements set forth by section 3.1.

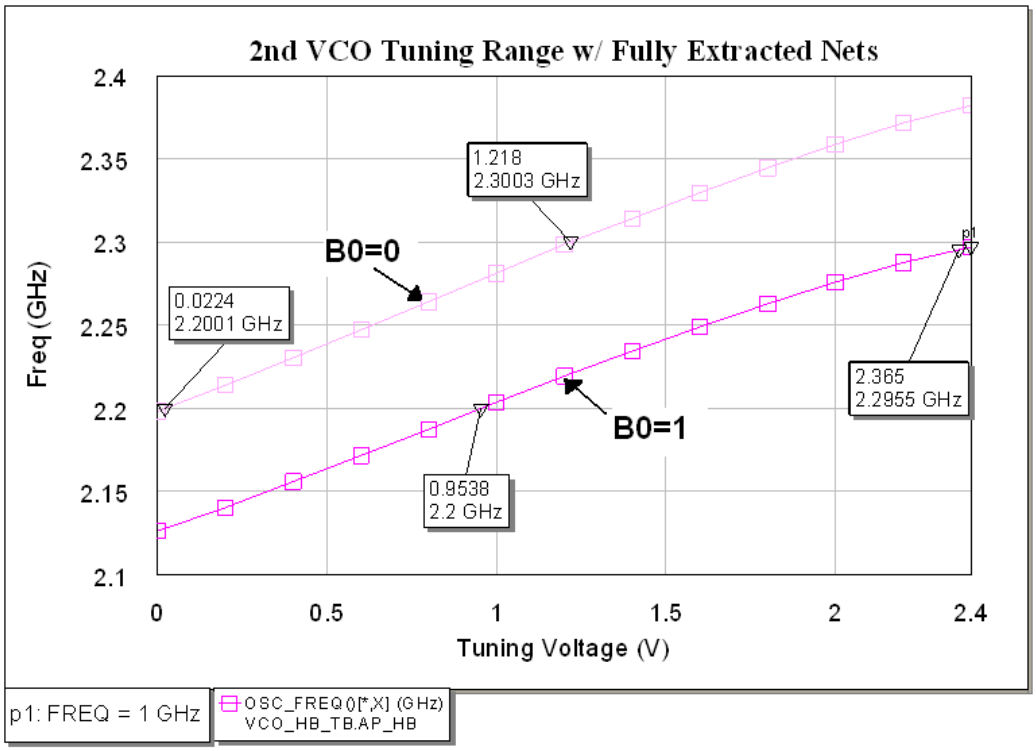


Figure 4.12: First iteration VCO frequency vs tuning voltage when course tuning bit, B0 equals 0 and 1.

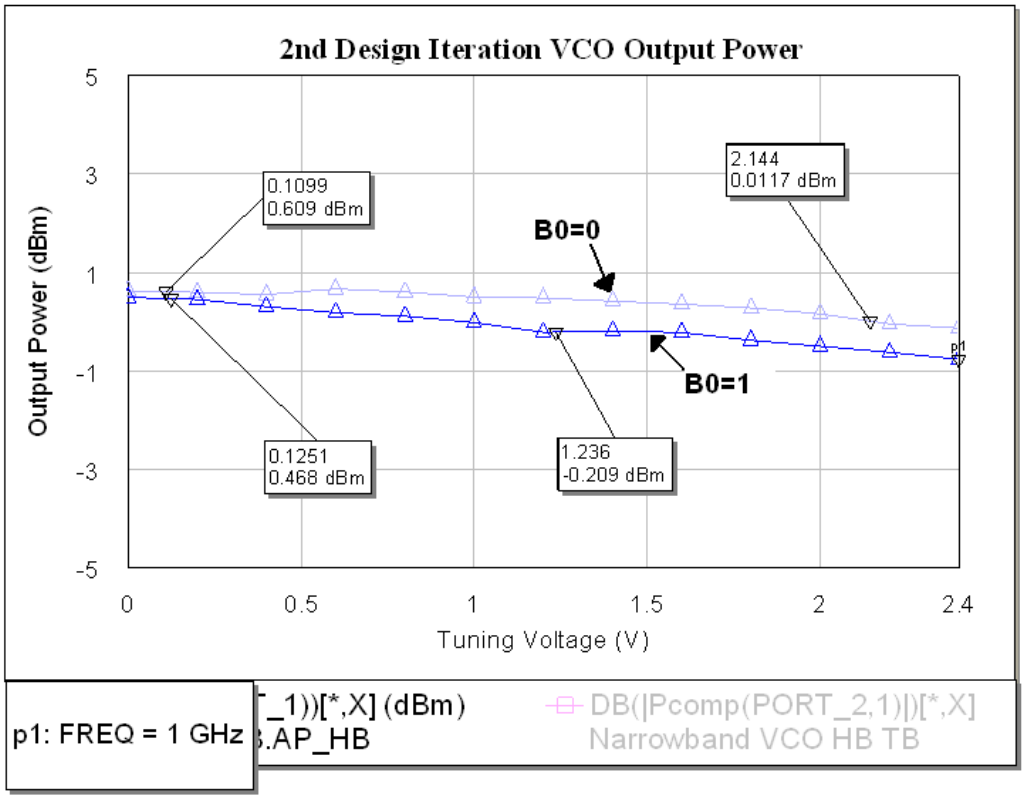


Figure 4.13: Second iteration VCO output power vs tuning voltage when course tuning bit, B0 equals 0 and 1.

A major issue with the first VCO design was its inability to handle phase variation in a 3:1 VSWR load mismatch. This was clearly evident in a lab measurement as well as a post measurement simulation. Prior to the design being released to the foundry, a load-pull simulation was performed to ensure that the VCO will meet the frequency pulling requirement of less than 10 kHz into a 3:1 mismatch at all phases. Figure 4:13 shows a frequency pulling simulation of less than 1 Hz for a 3:1 VSWR all-phase load.

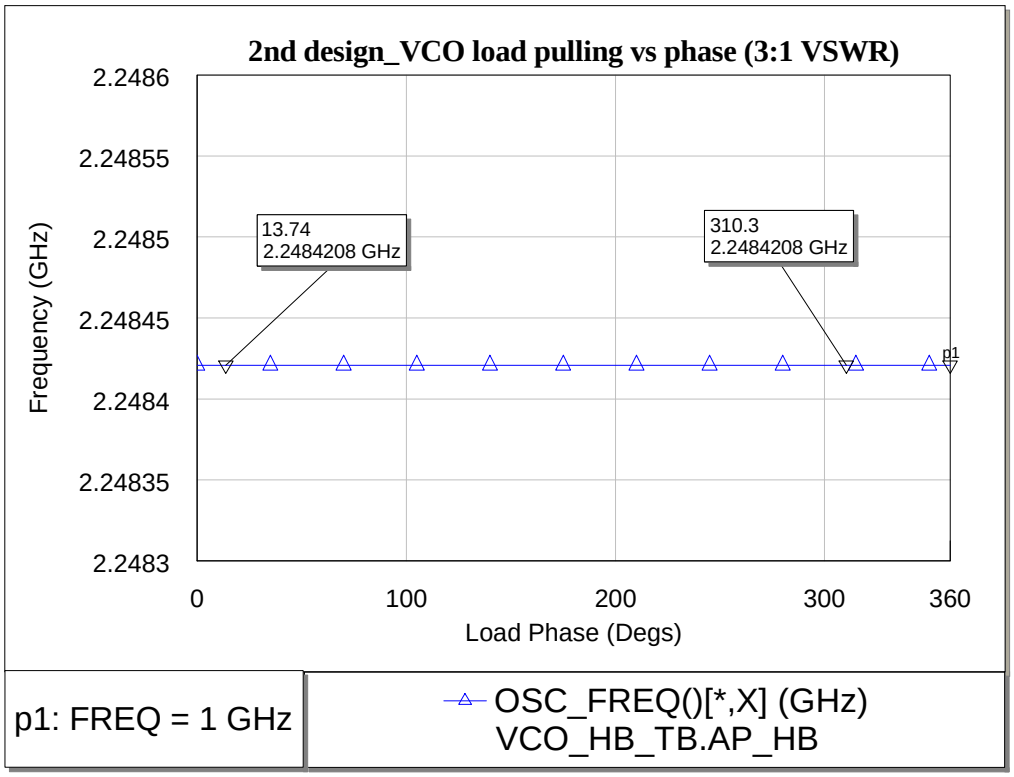


Figure 4.14: Second iteration VCO output frequency vs load phase for a 3:1 VSWR mismatch.

In addition to the VCO tuning range, output power and RF load pulling, the VCO phase-noise, amplitude and phase-balance, start-up transient, output spectrum and current consumption were re-simulated. Figure 4.13 shows that the phase-noise improved by approximately 5 dB at a 100 kHz offset when compared with the 1st design iteration. The amplitude and phase balance were checked in figure 4.14 and showed no amplitude mismatch and perfect phase-balance. Figure 4.15 shows that the 2nd VCO design iteration will start up and reach steady state oscillation in approximately 15 nanoseconds. Since the 2nd iteration VCO uses one differential

buffer amplifier in-lieu of 2 separate single-ended amplifiers a large drop in current consumption was to be expected. Simulation shows that the current used by the entire VCO dropped from 83 mA to approximately 34 mA, a savings of 49 mA. Finally, figure 4.16 shows that VCO exceeds the spectral purity requirement by having the closest harmonic at -52 dBc down from the fundamental frequency.

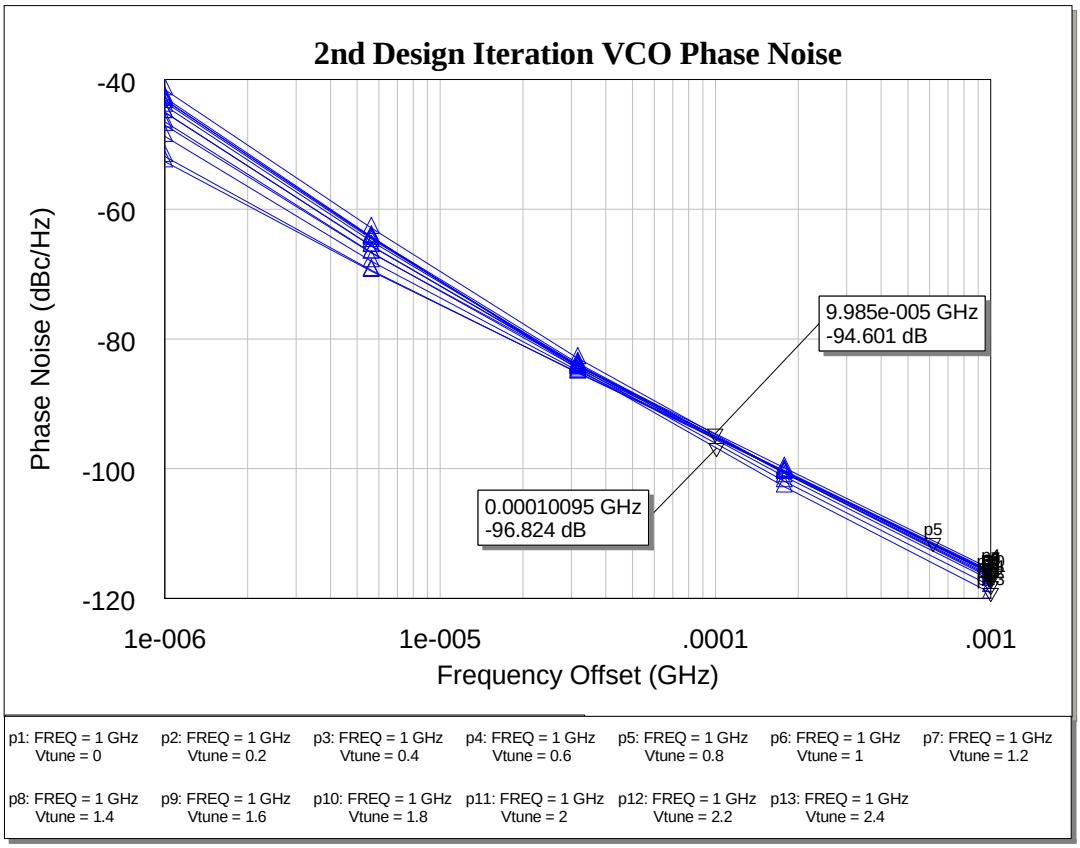


Figure 4.15: Second iteration VCO phase noise harmonic balance simulation results.

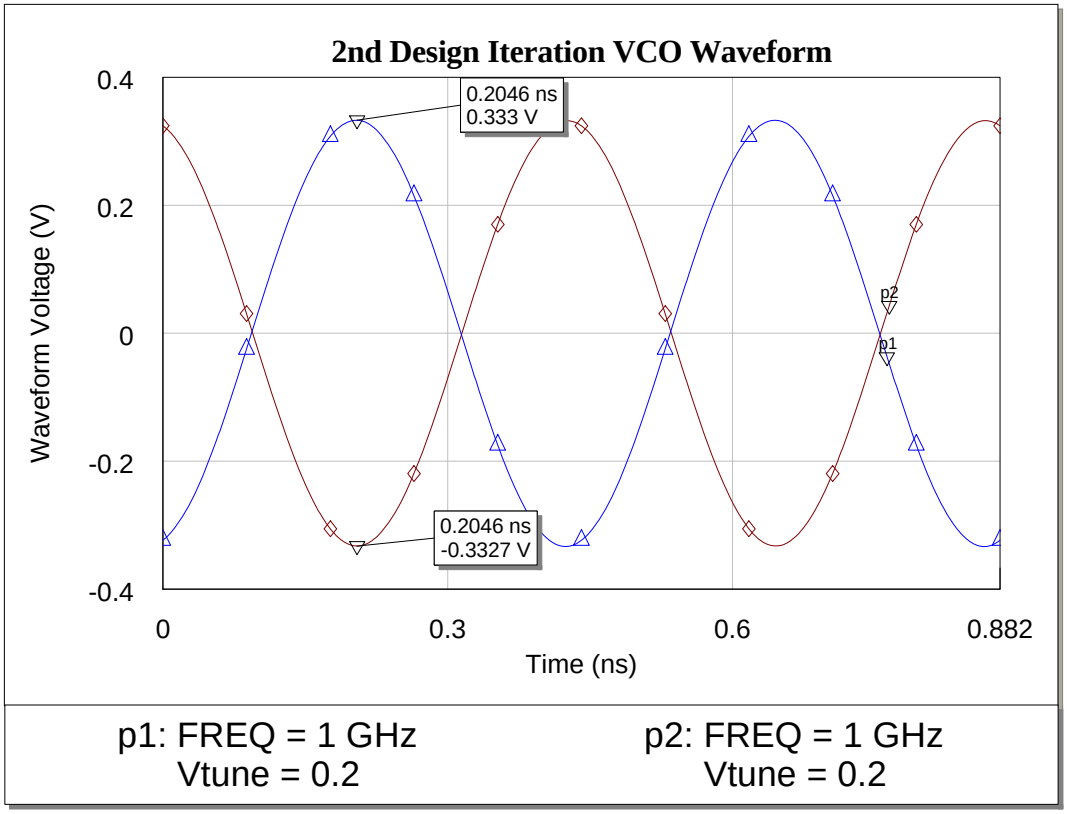


Figure 4.16: Second iteration VCO voltage waveform simulation results

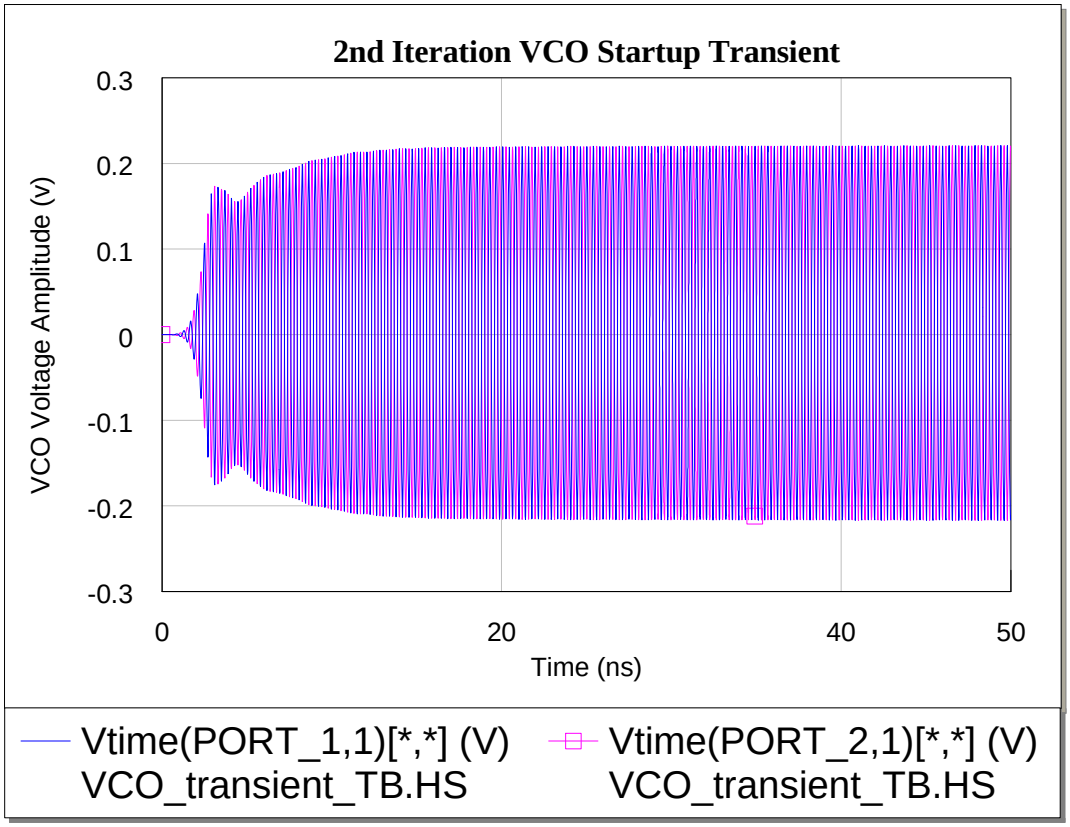


Figure 4.17: Second iteration VCO start-up transient simulation results

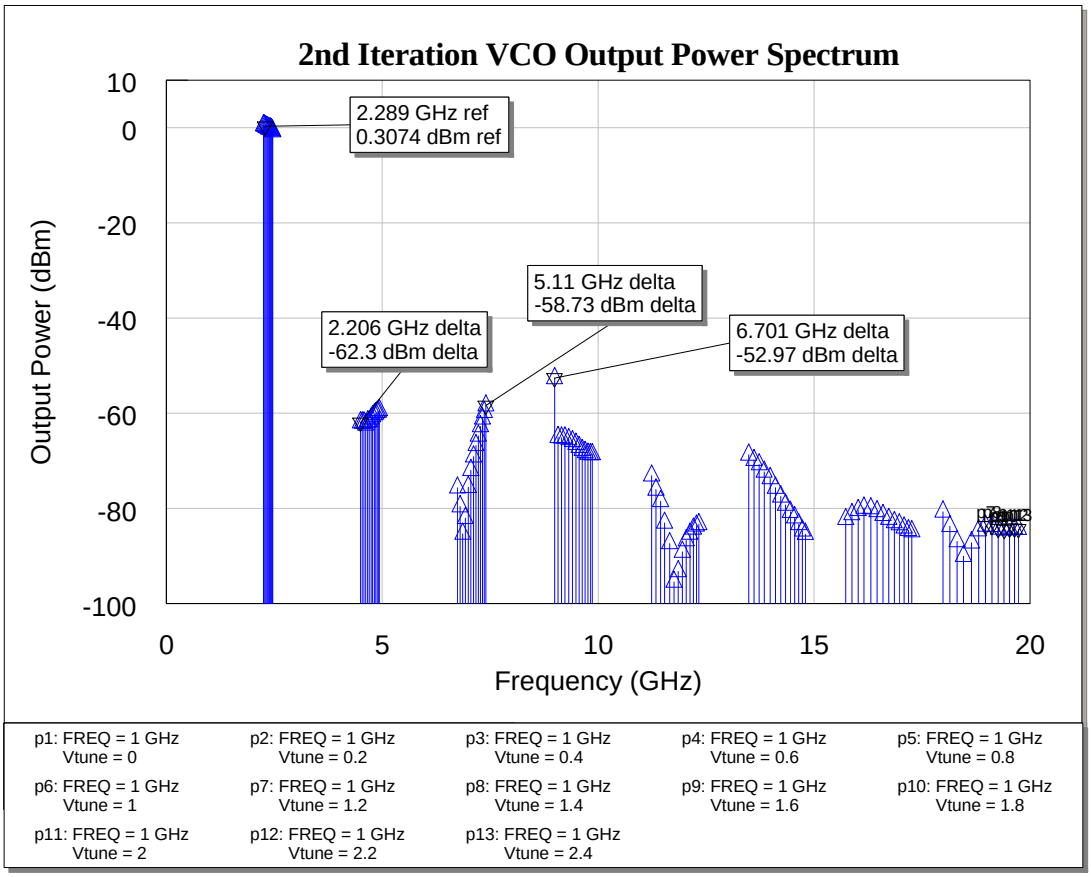


Figure 4.18: Second iteration VCO output power spectrum simulation results

5. Conclusions and Future Work

5.1. Conclusions

In-conclusion this thesis presented the design and testing of a high-isolation buffer amplifier and S-band voltage controlled oscillator both implemented in the Peregrine 0.25 μm GC SOS process. A redesign of the high-isolation buffer amplifier and voltage controlled oscillator was also presented.

The high-isolation buffer amplifier was designed to have a gain of 16 dB and isolation of greater than 60 dB for a frequency range of 2200 MHz to 3495 MHz. The intended purpose of the buffer amplifier was to provide isolation to the oscillator core to prevent frequency pulling into a 3:1 VSWR load mismatch. Actual measurements show that the gain was more than 5 dB off of the simulated gain at the upper end of the frequency band. This discrepancy was attributed to miller-capacitance effects and possible resistor skew variations in the amplifiers bias network. Direct measurements of the amplifier's isolation were shown to be unreliable due to board parasitics but a frequency pulling measurement on the VCO proved that the isolation was not adequate.

The S-band VCO was designed to operate from 2.20 GHz to 2.30 GHz with a minimum output power of 0 to +1 dBm. Measurements found that VCO meet requirements for the phase noise, spectral purity and power consumption but failed to

meet the requirements for frequency range, output power and RF load-pulling. The issues with the output power and load pulling can be directly contributed to low gain and isolation found earlier with the buffer amplifier. The frequency range issue was also attributed to unaccounted for parasitics in the oscillator core's tank circuit.

A second design iteration of the high-isolation buffer amplifier and VCO was performed to correct all of the aforementioned problems. The buffer amplifier was changed from a multi-stage, single-ended, common source amplifier to a completely differential, cascode amplifier. The cascode amplifier configuration eliminates the miller-effect capacitance and provides superior isolation when compared to a standard common source amplifier. Changing the amplifier topology from using 2 single-ended amplifiers to a differential amplifier, which will correct the output power level discrepancy between the differential ports. The VCO core was also changed by adding switched capacitors to extend the frequency tuning range with a PLL control bit. Smaller varactors were also used in the second iteration because more of the capacitance change in the varactor was able to be utilized with an addition of a bias network. Finally, a more accurate frequency simulation was performed on the oscillator because all of the interconnect parasitics where taken into account with a 1st order RLC parasitic extractor. All of these design changes made to the buffer amplifier and VCO core should make the S-band VCO meet all put-forth design requirements.

5.2. Future Work

One of the major issues with VCO design that was not addressed in this thesis is the issue of power-supply pushing. This was mainly due to the fact that future PLL design iterations will include a regulator circuit that will provide a clean, regulated 2.5 V. The second VCO design iteration exceeds the current phase-noise requirement of -80 dBc/Hz at a 100 kHz offset but a lower phase noise is always desirable and future VCO design iterations may be able to reach -100 dBc/Hz at a 100 kHz offset.

References:

[1] http://www.psemi.com/content/ultracmos/ultracmos_process_tech.html

[2] Neamen, Donald A. "Electronic Circuit Analysis and Design". 2nd ed. New York, NY: McGraw-Hill Companies Inc.

[3] "GX Rev 1.9 UltraCMOS^{TM} 0.25um SPICE MODELS" Version 1.9, May 2008. Peregrine Semiconductor

[4] Pozar, David M. "Microwave Engineering". 3rd ed. Hoboken, NJ: John Wiley & Sons

[5] Gonzalez, Guillermo. "Microwave Transistor Amplifiers". 2nd ed. Upper Saddle River, NJ: Prentice-Hall Inc.

[6] http://web.awrcorp.com/Usa/Products/Analog%2DOffice/

[7] Lee, Thomas H. "The Design of CMOS Radio-Frequency Integrated Circuits". 2nd ed. New York, NY: Cambridge University Press

[8] Tiebout, Marc. "Low Power VCO Design in CMOS". 1st ed. Berlin, Germany: Springer

[9] Leeson, D.B. "A simple Model of Feedback Oscillator Noise Spectrum". *Proc.IEEE,* pages 329-330, Feb 1966.

[10] Rogers, J., Plett, C., Dai, F., "Integrated Circuit Design for High-Speed Frequency Synthesis". 1st ed. Boston, MA: Artech House Inc.

[11] Andreani, P., Sjöland, H., "Tail-Current Noise Suppression in RF CMOS VCOs", *IEEE J. Solid-State Circuits,* VOL 37, NO 3, pp 342-348, March 2002

[12] Sneed, Nathan. "A 2-GHz CMOS LC-Tuned VCO using Switched-Capacitors to Compensate for Bond Wire Inductance Variation". MS Thesis, University of California, Berkeley, Dec 2000

[13] http://www.rfcafe.com/references/electrical/attenuators.htm

[14] http://www.minicircuits.com/products/filters_sm_low.html

[15] Berny, A.D., Niknejad, A.M., Meyer G.M.,"A Wideband Low-Phase-Noise CMOS VCO" *IEEE Custom Integrated Circuits Conference*, pp. 555-558, 2003

Appendix A:

Ceramic

Low Pass Filter

50Ω DC to 2200 MHz

LFCN-2250+
LFCN-2250

CASE STYLE: FV1206

Model	Price	Qty.
LFCN-2250+	$1.99	(10-49)
LFCN-2250	$1.99	(10-49)

+ RoHS compliant in accordance with EU Directive (2002/95/EC)

The +Suffix identifies RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications.

Maximum Ratings

Operating Temperature	-55°C to 100°C
Storage Temperature	-55°C to 100°C
RF Power Input*	10W max. at 25°C

** Passband rating, derate linearly to 3.5W at 100°C ambient.*

Pin Connections

RF IN	1
RF OUT	3
GROUND	2,4

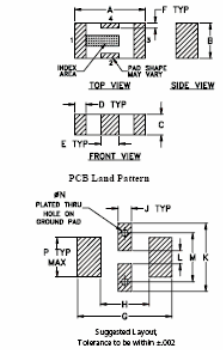
Features

- excellent power handling, 10W
- small size
- 7 sections
- temperature stable
- protected by U.S Patent 6,943,646

Applications

- harmonic rejection
- VHF/UHF transmitters/receivers
- lab use

Outline Drawing

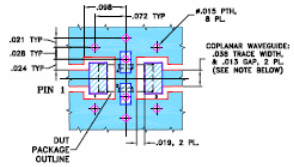


Outline Dimensions (inch / mm)

A	B	C	D	E	F	G
.126	.063	.037	.020	.032	.009	.169
3.20	1.60	0.94	0.51	0.81	0.23	4.29

H	J	K	L	M	N	P	wt
.087	.024	.122	.024	.087	.012	.071	grams
2.21	0.61	3.10	0.61	2.21	0.30	1.80	.020

Demo Board MCL P/N: TB-270
Suggested PCB Layout (PL-137)



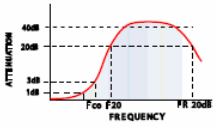
NOTES: 1. COPLANAR WAVEGUIDE PARAMETERS ARE SHOWN FOR ROGERS RO4350B WITH THICKNESS .020" ± .0015". COPPER: 1/2 OZ. EACH SIDE. FOR OTHER MATERIALS TRACE WIDTH & GAP MAY NEED TO BE MODIFIED.
2. BOTTOM SIDE OF THE PCB IS CONTINUOUS GROUND PLANE.
DENOTES PCB COPPER LAYOUT WITH SMOBC (SOLDER MASK OVER BARE COPPER)
DENOTES COPPER LAND PATTERN FREE OF SOLDER MASK

Electrical Specifications[1] (T_{AMB}=25°C)

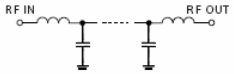
PASSBAND (MHz)	fco, MHz Nom.	STOP BAND (MHz) (loss, dB)			VSWR (:1)		NO. OF SECTIONS
(loss < 1.2 dB)	(loss 3 dB)	F 20	30	FR 20	Stopband	Passband	
Max.	Typ.	Min.	Typ.	Typ.	Typ.	Typ.	
DC-2200	2575	2900	3000-5000	7200	20	1.2	7

1. For applications requiring DC voltage to be applied to the input or output, use LFCN-2250D+ (DC Resistance to ground is 100 Mohms min.)

typical frequency response

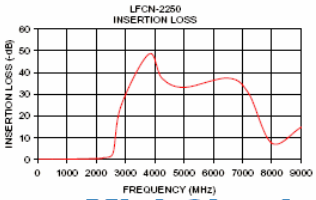


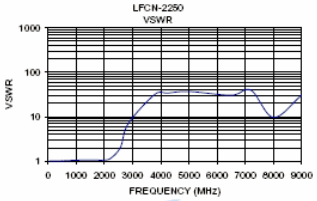
electrical schematic



Typical Performance Data at 25°C

Frequency (MHz)	Insertion Loss (dB)	VSWR (:1)
50.00	0.06	1.01
500.00	0.11	1.02
1000.00	0.15	1.05
1500.00	0.33	1.07
2000.00	0.51	1.06
2250.00	0.82	1.20
2575.00	2.84	2.10
2850.00	24.55	7.08
3800.00	48.40	32.18
4250.00	37.39	34.07
5000.00	33.16	36.97
6500.00	37.38	30.49
7200.00	30.64	39.49
8000.00	7.60	9.69
9000.00	14.79	30.49





Mini-Circuits®
ISO 9001 ISO 14001 AS 9100 CERTIFIED

minicircuits.com

P.O. Box 350166, Brooklyn, New York 11235-0003 (718) 934-4500 Fax (718) 332-4661 For detailed performance specs & shopping online see Mini-Circuits web site
The Design Engineers Search Engine Provides ACTUAL Data Instantly From MINI-CIRCUITS At: www.minicircuits.com
IF/RF MICROWAVE COMPONENTS

REV.H
M121640
LFCN-2250
ED-6469/5
AD/CP/AM
090218

This project was funded by the United States Department of Energy under Contract

DE-ACO4-01AL66850 and DE-ACO4-94AL85000