SAND99-0323J

BUSFET - A Novel Radiation-Hardened SOI Transistor

J. R. Schwank, M. R. Shaneyfelt, B. L. Draper, and P. E. Dodd
Sandia National Laboratories, P. O. Box 5800, MS-1083 Albuquerque, NM, 87185-1083

Abstract

The total-dose hardness of SOI technology is limited by radiation-induced charge trapping in gate, field, and SOI buried oxides. Charge trapping in the buried oxide can lead to back-channel leakage and makes hardening SOI transistors more challenging than hardening bulk-silicon transistors. Two avenues for hardening the back-channel are 1) to use specially prepared SOI buried oxides that reduce the net amount of trapped positive charge or 2) to design transistors that are less sensitive to the effects of trapped charge in the buried oxide. In this work, we propose a new partially-depleted SOI transistor structure that we call the BUSFET – Body Under Source FET. The BUSFET utilizes a shallow source and a deep drain. As a result, the silicon depletion region at the back channel caused by radiation-induced charge trapping in the buried oxide does not form a conducting path between source and drain. Thus, the BUSFET structure design can significantly reduce radiation-induced back-channel leakage without using specially prepared buried oxides. Total dose hardness is achieved without degrading the intrinsic SEU and dose rate hardness of SOI technology. The effectiveness of the BUSFET structure for reducing total-dose back-channel leakage depends on several variables, including the top silicon film thickness and doping concentration and the depth of the source. 3-D simulations show that for a doping concentration of 10^{18} cm^{-3} and a source depth of 90 nm, a silicon film thickness of 180 nm is sufficient to almost completely eliminate radiation-induced back-channel leakage. However, for a doping concentration of $3x10^{17}$ cm^{-3}, a thicker silicon film (300 nm) must be used.

I. INTRODUCTION

Silicon-on-Insulator (SOI) technology offers hardness advantages over bulk-silicon or epitaxial-silicon technologies for space and military applications. Properly designed SOI circuits are less prone to single-event upset (SEU) from energetic cosmic particles and can function without upset or failure after exposure to extremely high dose rate pulses of ionizing irradiation [1]. ICs have not been fabricated on bulk silicon that can function at dose rate levels achievable by properly designed SOI circuits. Because of the high levels of SEU and dose rate radiation hardness obtainable by SOI circuits, system applications not realizable with bulk-silicon circuits can be realized.

There are at least two mechanisms that can reduce the radiation hardness of SOI circuits. Floating body effects can degrade SEU and dose rate hardness, and back-channel leakage can degrade total dose ionizing radiation hardness. To reduce floating body effects, body ties can be used to tie the body to a fixed potential (normally the source) [2]. Unfortunately, body ties can significantly increase the size of transistors (and thus ICs). This can make them impractical for high-density circuits. Most common body tie techniques connect to the transistor's body region only at the extreme ends of the transistor, and this can limit their effectiveness for dose rate upset and SEU hardening [3].

The total dose hardening of SOI ICs can be more difficult than hardening bulk-silicon ICs due to the SOI buried oxide. Total dose ionizing radiation-induced back-channel leakage occurs as positive charge is trapped in the buried oxide near the silicon/oxide interface. Typical SOI buried oxides contain numerous defects that result in considerable radiation-induced charge trapping [4]. As charge is trapped in the buried oxide, the silicon becomes inverted at the silicon/buried oxide back channel, forming a conducting path between the source and drain. Note that the source and drain go all the way through the silicon for a standard thin-film SOI transistor. Techniques have been developed to fabricate hardened SOI buried oxides that minimize radiation-induced positive charge buildup near the back-channel interface [5,6]. Unfortunately, those processing techniques make hardened buried oxides more expensive. In addition, hardened buried oxides are not commercially available. One can also minimize back-channel leakage by increasing the silicon channel thickness such that the source and drain only partially penetrate the top silicon film. For this case, inversion of the back channel will not lead to a conductive path between source and drain and the total-dose hardness is considerably improved [7]. Unfortunately, this approach leads to large increases in junction area and an increase in charge collection volume reducing the dose rate and SEU hardness.

In this paper, we describe a novel body-tied partially-depleted SOI transistor structure that can be hard to total dose ionizing irradiation, while maintaining the high dose rate and SEU hardness levels intrinsic to thin-film SOI technology. We call this transistor the Body Under Source FET (BUSFET). For the BUSFET, total-dose hardness is obtained through the transistor structure and it is conceptually not necessary to use specially processed hardened buried oxides to minimize radiation-induced charge trapping. The BUSFET body-tie structure also requires less area than conventional body ties making BUSFET body ties more practical for high-density circuits. The fabrication and operation of the BUSFET is described. 3-D modeling of the BUSFET structure shows the validity of the BUSFET structure for minimizing back-channel effects.

DISCLAIMER

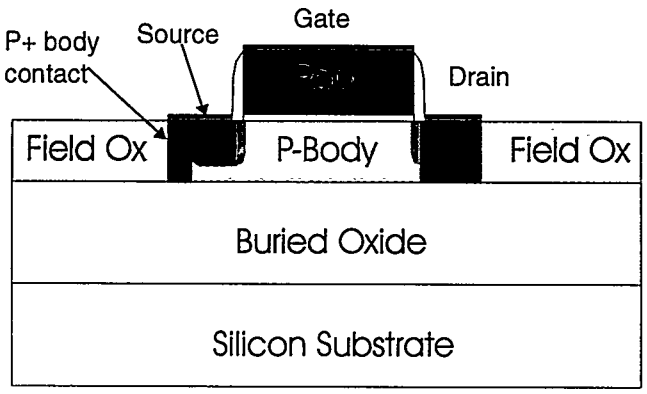

Figure 1: BUSFET cross section.

II. BUSFET DESCRIPTION

The BUSFET transistor structure is close to that of a standard MOS SOI transistor structure. A total of only two additional mask levels are required to fabricate a typical partially-depleted SOI IC using the BUSFET design. In this section, we describe the basic structure of the BUSFET and a process flow for obtaining the BUSFET structure.

The cross section for the BUSFET is shown in Fig. 1. The BUSFET is similar to a standard partially-depleted SOI MOSFET with two main exceptions. 1) The source does not extend completely through the top silicon layer. 2) Next to the source is a heavily doped p-type region that serves as the body contact. The effects of radiation-induced back-channel leakage in the BUSFET are significantly reduced or eliminated because the source region does not go completely through the silicon layer. Depending on BUSFET design (body doping concentration, source depth, silicon film thickness, etc.), a conducting path between the source and drain may not exist, even if the back-channel interface is inverted by charge trapping in the buried oxide due to total dose ionizing irradiation.

The process flow for fabricating a BUSFET transistor is very similar to that for a typical partially-depleted SOI transistor. To fabricate a BUSFET CMOS IC, only two additional mask levels (one for n-channel transistor drains and p-channel body contacts, and one for p-channel transistor drains and n-channel body contacts) are required. Note that p-channel BUSFETs are not likely required for total-dose hardening, but the body tie associated with the BUSFET p-channel transistor may be required for SEU and dose rate hardening, and reducing floating body circuit effects. A possible process flow for fabricating an n-channel BUSFET is outlined in Figure 2 (this portion of the process flow only includes the unique steps required to make a BUSFET; additional steps not specific to the BUSFET are required for fabricating the complete IC). Step 1: The polysilicon gate is defined using standard photolithographic and etching techniques. Step 2: n-type lightly doped drains (LDDs) are implanted into the source and drain regions. The LDD implants extend only partially through the silicon layer. Step 3: LDD spacers are deposited and defined using standard processing techniques. Using the same mask as for the LDD implants, a second n-type implant is performed to heavily dope the source and drain contact regions. Like the LDD implant, this implant goes only partially through the silicon layer. Step 4: A deep n-type implant is performed to form the drain region. This mask level is one of the two additional mask levels required for fabricating BUSFETs. Note that this mask level is also used to form the n+ body contact for p-channel transistors (not shown). Step 5: A deep p-type implant is performed to make the p+ n-channel body tie contact. This is the second additional mask level required to fabricate BUSFETs. It also is used to form the deep p+ drain regions for p-channel transistors. The deep n+ and p+ implants are not self aligned. However, this is not a major problem because the alignment is not critical. If the deep n+ implant is a few tenths of microns away from the channel region, it will not change the transistor response. The deep n+ implant is required only for SEU and dose rate hardening, and a slight misalignment will not significantly affect junction area. Step 6: A silicide strap is formed over the p+ body tie and n+ source contact, physically shorting the two together, as well as the polysilicon gate and drain. Note that the area consumed by the body tie leads to only a negligible (if any) increase in area. The width of the source/body contact region is determined primarily by the area required by the silicide strap and design rule constraints. This area is approximately the same for either the source contact alone or for the source and body contact together. One process variation that may be required to minimize the depth of the back-channel inversion layer, and thus, minimize the conductive path between source and drain, is to use a retrograde doping profile for the body region. This involves only adjusting the body region implant and does not require any additional mask levels.

III. 3-D SIMULATIONS

A. *Total Dose Performance*

We have performed device simulations using the 3-D code Davinci to compare the total-dose response of a partially-depleted SOI BUSFET to a standard partially-depleted SOI MOSFET. Figure 3 illustrates the total dose behavior of standard partially-depleted MOSFETs fabricated in a 0.35-μm gate length 3.3-V technology versus total dose. Figure 4 illustrates the total dose behavior of partially depleted BUSFETs fabricated in the same technology versus total dose. For both the standard MOSFETs and the BUSFETs, the gate width is 10 μm. We also assume a retrograde body doping profile with a back-channel concentration of 10^{18} cm^{-3}, a top silicon thickness of 180 nm, a source depth of 75 nm, and a buried oxide thickness of 370 nm. In the top panel of each figure are simulated subthreshold I-V curves as a function of back-channel interface charge density. The total-dose response is simulated by adding a sheet of radiation-induced charge at the back-channel interface. In reality, charge

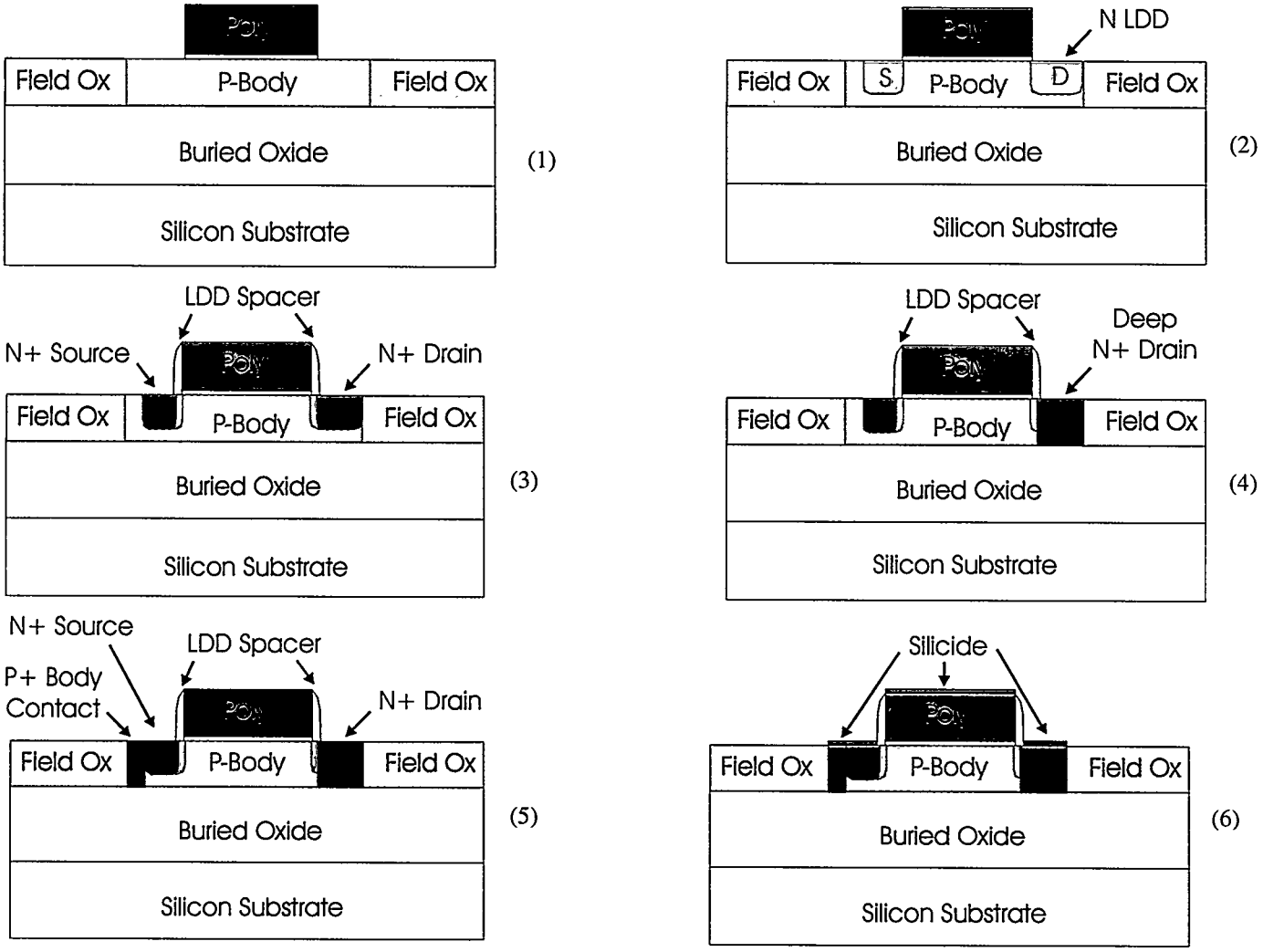

Figure 2: Process flow for fabricating an SOI BUSFET: step 1: poly gate definition, step 2: LDD implant, step 3: LDD definition, and shallow source and drain implants, step 4: deep n+ drain, step 5: p+ body contact implant, and step 6: silicide contact and strap definition.

generated in the buried oxide by total dose ionizing radiation is non-uniformly trapped throughout the oxide, and the trapping efficiency and charge yield depend on the material properties and local electric field. In these simplified simulations, we assume 100% trapping efficiency and charge yield, and that all of the charge is trapped at the back-channel interface (the worst-case scenario for charge location). Note that the charge density introduced in the simulations can be directly related to a worst-case total accumulated dose irradiation level. For example, 1 krad(SiO_2) of irradiation generates 8.1×10^{15} electron-hole pairs/cm^3 [8]. If all of the holes generated in the buried oxide escape recombination and become trapped at the interface, they correspond to a certain back-channel interface charge density (Q_{bc} in Figs. 3 and 4). The bottom panel of each figure is a plot of electron concentration for a back-channel net-positive charge density of 10^{16}/cm^2. This surface-charge density is much higher than is physically realizable. Again, it is an effective charge density resulting from charge trapping throughout the buried oxide.

In the standard SOI n-channel transistor (Fig. 3), we see significant back-channel leakage at very low radiation-induced charge densities. By about 10 krad(SiO_2), the standard SOI transistor shows considerable back-channel leakage (>10^{-7} A). In reality, leakage will not occur until a somewhat higher irradiation level because not 100% of the generated holes will be trapped, a large fraction of the generated positive charge created by trapped holes will be compensated by the negative charge generated by trapped electrons, and the trapped charge will not all be located at the interface [9]. As discussed previously and as illustrated in the bottom panel of Fig. 3, the large increase in leakage current is produced because the back-channel charge inverts the silicon near the interface and creates a direct conducting path between the source and drain regions. This path leads to a considerable leakage current as bias is applied to the drain (3.3 V in these simulations). In contrast, Fig. 4 shows the total-dose response of the SOI BUSFET. Even at very high levels of radiation (>30 Mrad(SiO_2)), there is no significant back-channel leakage. Again, keep in mind that because of our worst-case assumptions a back-channel interface charge density of

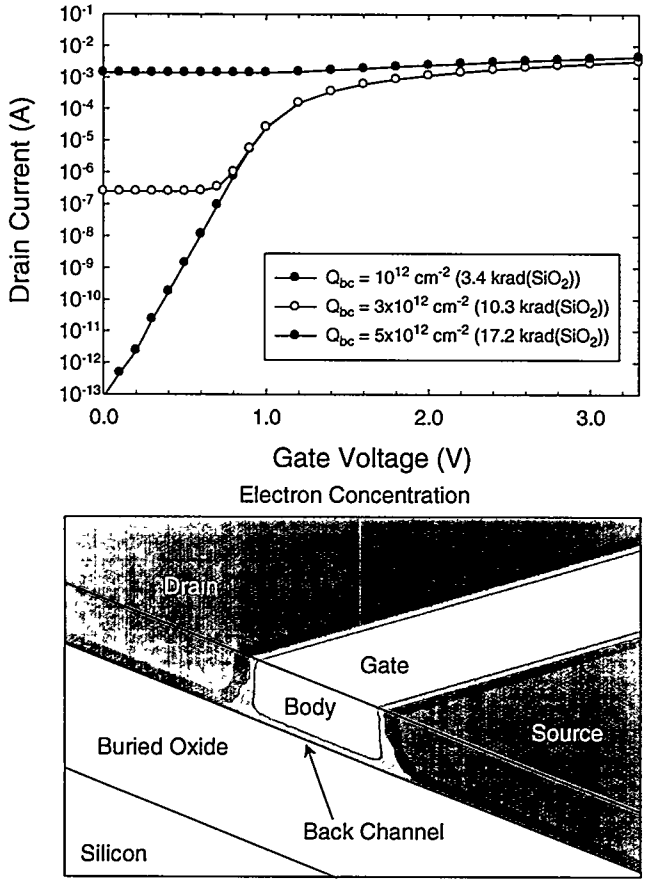

Figure 3: The simulated response of a standard partially-depleted SOI MOSFET to radiation-induced charge buildup at the back-channel interface. Top) Subthreshold I-V characteristics as a function of back-channel interface charge density. Bottom) Plot of electron concentration for a back-channel charge density of $5x10^{12}/cm^2$ illustrating the conducting path between the drain and the source.

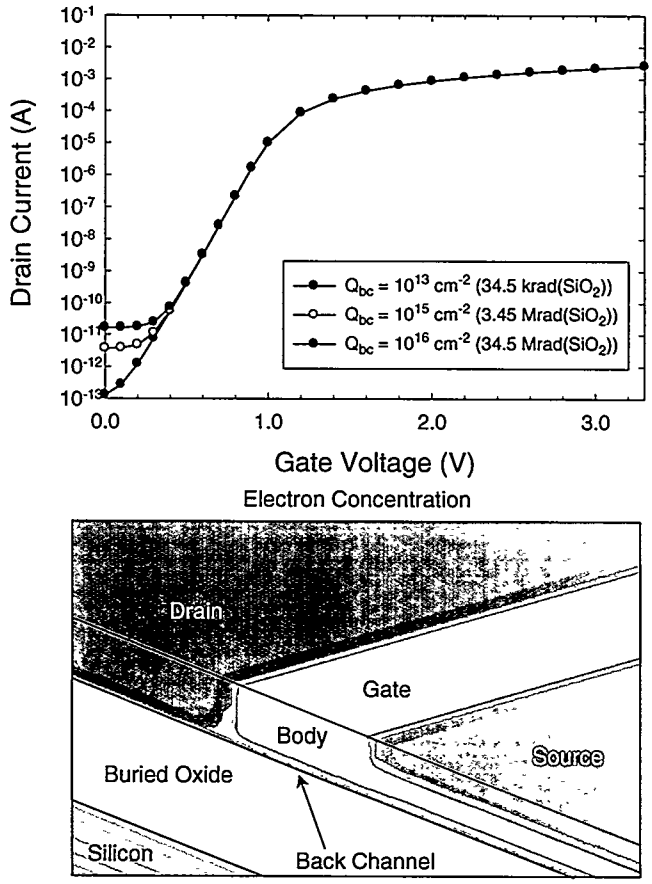

Figure 4: The simulated response of a partially-depleted SOI BUSFET to radiation-induced charge buildup at the back-channel interface. Top) Subthreshold I-V characteristics as a function of back-channel interface charge density. Bottom) Plot of electron concentration for a back-channel charge density of $10^{16}/cm^2$. Note that although the back-channel interface is inverted, there is no conducting path between the drain and the source.

10^{16} cm^{-2} would not actually be reached until a considerably higher irradiation level (if ever).

In any case, the simulations show that the BUSFET structure can significantly reduce the impact of radiation-induced charge buildup in the buried oxide. For the conditions presented here, the radiation levels producing back-channel leakage have been increased by more than three orders of magnitude. Of course, the overall hardness will also depend on the hardness of the gate oxide and the lateral field isolation. As illustrated in the lower panel of Fig. 4, although a back-channel inversion layer exists, there is no conducting path between the source and drain because the source is not deep enough to complete the leakage path.

B. SEU Performance

The main driving force for developing the BUSFET is to eliminate or substantially reduce problems associated with total-dose induced back-channel leakage. However, one requirement for the BUSFET is that it does not degrade either SEU or dose rate hardness. As long as the drain extends completely through the top silicon film, the BUSFET SEU upset cross section and the amount of p-n junction area (the primary contributor to dose rate effects) should be close to that for a standard BUSFET. Note that heavy-ion strikes at the source do not contribute to charge collection. In addition, because the source is physically shorted to the body tie, it cannot contribute to dose rate induced photocurrent. As such, the shallow source will not lead to enhanced charge collection following either a heavy-ion strike or exposure to a high dose rate pulse of irradiation. If the drain does not penetrate completely through the top silicon film, this will increase the SEU upset cross section and the amount of p-n junction area. Thus, a shallow drain will degrade SEU and dose rate hardness.

One possible mechanism by which the BUSFET could adversely impact SEU or dose rate hardness is by enhanced charge collection via floating body effects. For a heavy-ion strike, enhanced charge collection due to floating body effects will lead to a reduction in LET threshold. To verify that this is

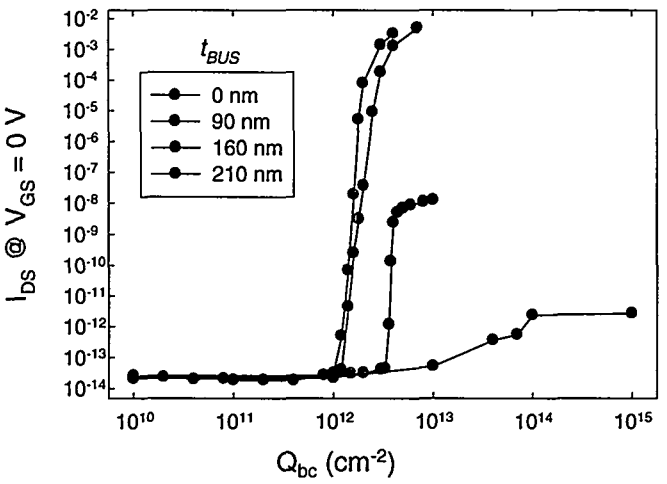

Figure 5: The simulated increase in BUSFET source-to-drain back-channel leakage, I_{DS}, measured at V_{GS} = 0.0 V to radiation-induced charge buildup at the back-channel interface for t_{BUS} = 0, 90, 160, and 210 nm. The bias supply was 3 V and the source depth was 90 nm. Note that t_{BUS} = 0 nm corresponds to a standard fully-bottomed SOI MOSFET.

not the case, we performed 3-D simulations on BUSFETs with and without conventional body ties and compared the results to 3-D simulations on standard SOI MOSFETs with body ties. Note that we are presently unable to perform 3-D simulations on MOSFETs without some type of body tie (either the intrinsic body tie associated with the BUSFET and/or a standard body tie). BUSFET transistors with a 0.75-μm gate width, a 0.35-μm gate length, and a 0.75-μm long source (the distance from the p+ body-contact implant to the channel body region underneath the source implant) were simulated. The bias supply was 3.0 V. The simulated LET thresholds for a BUSFET without a standard body tie, a BUSFET with a standard body tie, and a MOSFET with a standard body tie are 5.25 ± 0.75, 6.75 ± 0.75, and 6.75 ± 0.75 MeV-cm^2/mg, respectively. First note that these values for LET are low due to a low nodal drain capacitance and the fast switching speeds for the SOI transistors. To function reliably in space, some type of circuit hardening would be required. Secondly note that there is no significant difference in LET threshold between the BUSFET with a standard body tie and the MOSFET with a standard body tie. These results suggest that the BUSFET structure does not degrade SEU hardness. Instead, the BUSFET, by itself, may provide some improvement in SEU hardness by partially mitigating floating body effects. Although we are unable to simulate the response of a MOSFET without a body tie, we can reasonably expect the LET threshold to be smaller than 5 MeV-cm^2/mg for a standard SOI MOSFET transistor.

One must be cautious in applying the BUSFET body tie for improving SEU and dose rate hardness. These simulations were performed without taking into account charge trapping in the buried oxide. The effectiveness of the BUSFET body tie underneath the source will be diminished as charge is trapped in the buried oxide and the depletion width of the silicon inversion region at the back channel is increased. An increase in depletion width will increase the resistance of the BUSFET body tie underneath the source and reduce the efficiency of the BUSFET body tie. As such, BUSFET ICs used in combined total dose and heavy-ion irradiation environments will likely have to incorporate standard body ties in addition to the BUSFET body tie. However, in absence of total dose irradiation (e.g., terrestrial irradiation), the BUSFET body tie may improve SEU hardness over standard SOI MOSFETs without body ties. In fact, for the device conditions simulated above, the LET threshold of the BUSFET is high enough to eliminate upsets due to alpha particle strikes which have an LET of ~ 2 to 3 MeV-cm^2/mg. Thus, by itself, the BUSFET may provide sufficient SEU protection to eliminate upsets in commercial ICs caused by terrestrial irradiation (e.g., alpha particles emitted by impurities in metals and generated by terrestrial cosmic particles) [10].

C. *Silicon Thickness and Doping Level Effects*

Optimizing the BUSFET design involves tradeoffs between variables such as the body doping level, the depth of the shallow source, and the thickness of the top silicon film. One important variable is the thickness of the silicon under the source. We call this thickness t_{BUS} and define it as the total silicon film thickness minus the source depth. To eliminate radiation-induced back-channel leakage, the depletion region of the source cannot come into contact with the depletion region of the back-channel silicon inversion layer. Therefore, decreasing the source depth, increasing the top silicon film thickness, and increasing the silicon doping level near the back channel (reducing the back-channel silicon and source depletion widths) will all improve the effectiveness of the BUSFET for reducing total-dose induced back-channel leakage. However, other device and manufacturing constraints limit the practical range over which these parameters can be varied. For example, a doping level of 10^{18} cm^{-3} (Figs. 3 and 4) will cause junction breakdown near 5 V and is not usable for 5-V operation. Similarly, the top silicon thickness cannot be arbitrarily extended due to possible manufacturing constraints (e.g., the drain must extend completely through the silicon) and, eventually, due to a reduction in SEU and dose rate hardness.

The effects of silicon thickness on BUSFET back-channel radiation-induced leakage is demonstrated in Fig. 5 where the simulated back-channel leakage measured at V_{GS} = 0.0 V is plotted versus back-channel charge density (minimum total dose) for t_{BUS} = 90, 160, and 210 nm. Also plotted is the simulated leakage for a standard fully-bottomed MOSFET (t_{BUS} = 0.0). For these simulations the drain bias was 3 V, the silicon doping level was 3x10^{17} cm^{-3}, and the source depth was 90 nm. This doping level permits 5-V operation. For t_{BUS} = 90 nm, deposited charge densities of greater than 10^{12} cm^{-2} result in large increases in back-channel leakage. At this charge density, the depletion region of the silicon inversion region begins to make contact with the source depletion region forming a conducting path between source and drain. As t_{BUS}

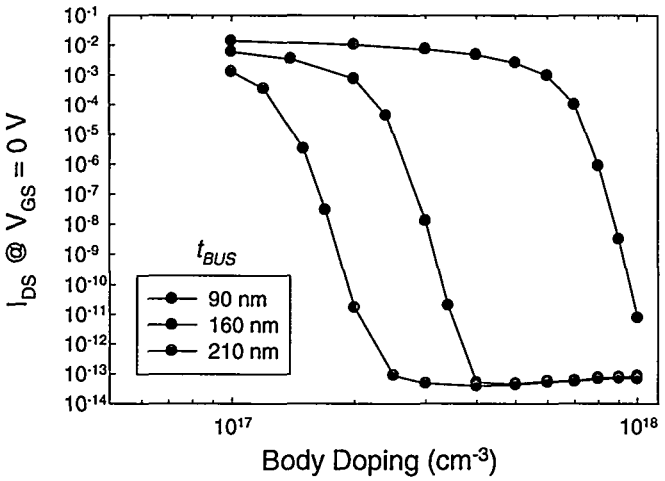

Figure 6: The simulated change in BUSFET source-to-drain back-channel leakage, I_{DS}, measured at V_{GS} = 0.0 V versus body doping concentration for t_{BUS} = 90, 160, and 210 nm. The bias supply was 3 V and the source depth was 90 nm.

is increased to 160 nm, the charge required to "turn-on" the back channel increases to ~$3x10^{12}$ cm^{-2}. However, the maximum back-channel leakage current for t_{BUS} = 160 nm is at least five orders of magnitude smaller than for t_{BUS} = 90 nm. For t_{BUS} = 210 nm, the depletion regions of the source and back-channel inversion region never come into contact for all charge densities examined, and no significant increase in leakage current is observed even for charge densities as high as 10^{15} cm^{-2}. Also plotted in Fig. 5 is the simulated back-channel leakage measured at V_{GS} = 0.0 V for a standard SOI MOSFET with a deep (fully bottomed) source and drain. Note that the increase in leakage current for the standard SOI MOSFET (t_{BUS} = 0.0) begins to increase at approximately the same charge density as for the BUSFET with t_{BUS} = 90 nm. This implies that for t_{BUS} = 90 nm, the source depletion region extends close to the silicon/buried oxide interface. Thus, the back-channel depletion width at the onset of inversion is sufficiently wide to make contact with the source depletion region.

The effects of body doping concentration on BUSFET back-channel radiation-induced leakage is demonstrated in Fig. 6 where I_{DS} measured at V_{GS} = 0.0 V is plotted versus body doping concentration for t_{BUS} = 90, 160 and 210 nm. The drain bias was 3 V and source depth was 90 nm. For each value of t_{BUS}, increasing body doping concentration causes a reduction in back-channel leakage. The minimum doping concentration for effectively eliminating back-channel leakage for t_{BUS} = 90 (180), 160 (270), and 210 (300) nm are approximately, ~10^{18}, $4x10^{17}$, and $2.3x10^{17}$ cm^{-3}, respectively. In the parentheses are the total silicon film thicknesses for a 90-nm source depth. Although a wide range of silicon film thicknesses are obtainable from commercial SOI wafer suppliers, typical SOI film thicknesses (unprocessed) are around 200 nm and less. Thus, with a source depth of ~90 nm and a doping concentration of $3x10^{17}$ cm^{-3}, it probably will be necessary to grow a thin epitaxial layer on top of the silicon film prior to processing. However, for doping concentrations of 10^{18} cm^{-3} and higher, epitaxial layers are likely not required. As technologies evolve to lower operating voltages, higher body doping levels can be used. Hence, this trend will further improve the total dose ionizing radiation response of BUSFETs.

IV. DISCUSSION

To harden SOI circuits to total dose ionizing irradiation, existing technologies use either specially processed buried oxides or very thick silicon layers. The typical steps required to fabricate a hardened buried oxide can be very expensive. The special processing can increase the cost of hardened SOI substrates by more than a factor of two over standard SOI substrates. The equipment required to harden an SOI buried oxide is not obtainable from standard commercial equipment suppliers. Although techniques to harden buried oxides have been demonstrated [5,6], hardened buried oxides are not commercially available. This makes hardened SOI wafer availability tenuous at best, especially as the commercial need for non-hardened SOI wafers increases [11].

Eliminating radiation-induced back-channel leakage simply by increasing the thickness of the silicon layer has serious drawbacks that negate most of the advantages of thin-film SOI technology. If the silicon layer is very thick, the source and drain regions will not penetrate completely through the silicon layer so there is no conducting path for radiation-induced back-channel leakage. However, if the source and drain (primarily due to the drain) do not go completely through the silicon layer, the amount of p-n junction area, the SEU upset cross section, and the charge collection depth will be greatly increased. As a result, the dose rate upset and SEU hardness will be reduced as compared to SOI ICs with fully-bottomed sources and drains. This will also greatly increase parasitic capacitance causing circuits to operate slower or consume more power; therefore, they will be less attractive to commercial or rad-hard users. Because the back-channel leakage path has been eliminated in the BUSFET, specially processed hardened substrates are not required for total dose hardening. Additionally, because the BUSFET is fabricated using a thin-film silicon layer and the drain contact goes completely through the silicon layer, critical p-n junction, SEU upset cross section area and charge collection depth are still minimized compared to bulk CMOS ICs. Note that the source and p+ body-tie contacts are physically shorted together. As a result the source/body junction will not significantly add to the amount of active p-n junction area that can contribute to high dose rate photocurrents. *Hence, the BUSFET will be hard to total dose ionizing irradiation (back-channel leakage), while maintaining the SEU and dose-rate hardness advantages inherent to SOI technology.*

The BUSFET body tie scheme offers advantages over conventional body ties [2]. Only a small p+ body-tie contact region is required and thus the body-tie area is minimized.

This makes the BUSFET body tie attractive to commercial circuit designers. Also, because the body-tie contact connects to the body under the source, *all sites along the width of the channel are connected to the source potential.* This should significantly reduce voltage drops along the width of the body and greatly increase the effectiveness of the body tie, especially for wide devices [3]. The primary drawback to the BUSFET body tie is that its effectiveness is reduced as radiation-induced charge trapping in the buried oxide generates a depletion region at the back-channel interface increasing the resistance of the BUSFET body tie. Thus, in combined SEU and total-dose environments, it is likely that BUSFET transistors will have to include conventional body ties.

For most circuit elements, designing the circuit around BUSFET transistors is straightforward. However, some circuit elements either cannot use BUSFET transistors or the transistor must be modified. For example, in a pass gate or transmission gate the body connection cannot be tied to the source. For some pass-gate bias conditions, this could lead to forward biased source-to-body p-n junctions. It is permissible to use a body tie (BUSFET or standard) with separate source and body tie contacts, and with the body tie connected to 0 V for n-channel transistors and V_{DD} for p-channel transistors. However, this will not use area as efficiently as standard pass gates resulting in increased circuit dimensions. It is also permissible to use shallow source and drains or deep source and drains for pass gate transistors. Shallow source and drains will degrade SEU and dose rate hardness. Deep source and drains may degrade total dose hardness.

VI. SUMMARY

We have proposed a novel transistor structure design called the BUSFET that can effectively eliminates total dose back-channel leakage without the need for specially prepared, hardened buried oxides and that does not degrade the intrinsic SEU or dose rate hardness of SOI technology. The BUSFET utilizes a shallow source and a deep drain. Radiation-induced charge trapping in the buried oxide cannot form a conducting path between source and drain. 3-D simulations show that the effectiveness of the BUSFET depends on several variables including the top silicon film thickness and doping concentration, and the depth of the source. As IC technologies advance and higher doping concentration levels are used, the effectiveness of the BUSFET is improved.

ACKNOWLEDGMENTS

The authors thank Peter Winokur, Rich Flores, Tom Hill, and Dan Fleetwood for technical discussions. Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy under Contract DE-AC04-94AL85000.

REFERENCES

[1] J. R. Schwank, "Space and Military Radiation Effects in Silicon-on-Insulator Devices," in 1996 IEEE International SOI Conference Short Course: Silicon-on-Insulator Circuits, ed. J. P. Colinge, pp. 5-1 to 5-75 (Sept. 1996).

[2] L. R. Hite, H. Lu, T. W. Houston, D. S. Hurta, and W. E. Bailey, "An SEU Resistant 256K SOI SRAM," IEEE Trans. Nucl. Sci. 39, 2121 (Dec. 1992).

[3] L. W. Massengill, D. V. Kerns, Jr., S. E. Kerns, and M. L. Alles, "Single-Event Charge Enhancement in SOI Devices, " IEEE Electron Dev. Lett. 11, 98 (1990).

[4] W. L. Warren, et al., "Paramagnetic Defect Centers in Irradiated BESOI and SIMOX Buried Oxides," IEEE Trans. Nucl. Sci. 40, 1755 (Dec. 1993).

[5] H. Hughes and P. McMarr, "Radiation-Hardening of SOI by Ion Implantation into the Buried Oxide," U. S. Patent No. 5,795,813.

[6] S. T. Liu, W. C. Jenkins, and H. L. Hughes, "Total Dose Radiation Hard 0.35 μm SOI CMOS Technology," IEEE Trans. Nucl. Sci. 45, 2442 (Dec. 1998).

[7] M. Dentan, et al., "Study of a CMOS-JFET-Bipolar Radiation Hard Analog-Digital Technology Suitable for High-Energy Physics Electronics," IEEE Trans. Nucl. Sci. 40, 1555 (Dec. 1993).

[8] J. M. Benedetto and H. E. Boesch, Jr., "The relationship Between ^{60}Co and 10-keV X-Ray Damage in MOS Devices," IEEE Trans. Nucl. Sci. 33, 1318 (Dec. 1986).

[9] H. E. Boesch, Jr., T. L. Taylor, L. R. Hite, and W. E. Bailey, "Time-Dependent Hole and Electron Trapping Effects in SIMOX Buried Oxides," IEEE Trans. Nucl. Sci. 37, 1982 (Dec. 1990).

[10] P. E. Dodd, "Basic Mechanisms for Single-Event Effects," in 1999 IEEE Nuclear and Space Radiation Effects Conference Short Course, ed. D. M. Fleetwood (July 1999).

[11] M. B. Alles, "Thin-Film SOI Emerges," IEEE Spectrum 34 (6), 37 (June 1997).