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A. J. Mendez, R. M. Gagliardi, V. J. Hernandez, C. V. Bennett

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RECEIVER ARCHITECTURE FOR 12.5 GB/S 16-ARY PULSE POSITION MODULATION (PPM) SIGNALING

A. J. Mendez[1], R. M. Gagliardi[2], V. J. Hernandez[3], C.V. Bennett[3]
[1]Mendez R&D Associates, El Segundo, CA
[2]University of Southern California, Los Angeles, CA
[3]Lawrence Livermore National Laboratory, Livermore, CA

Introduction

PPM is a signaling scheme that enables the transmission of multiple bits per symbol [1]. It has found favor in the regime of free space optical communications ("FSO" or "Lasercom"); however, PPM has yet to be widely applied to fiber optic-based communications. Its limitation in fiber results from the exceedingly high bandwidth requirements needed to electronically process a directly detected pulse, especially as the symbol rate increases and the pulse width correspondingly decreases. As a solution, we introduced the concept of a virtual quadrant receiver for receiving 1.25 Gb/s 4-ary PPM, where photonic processing reduced the number of required electronic components [2]. In this paper, we extend these photonic process techniques to a 16-ary, 12.5 Gb/s (10 Gb/s plus 8B/10B line coding) PPM communications system for fiber optic avionics, wherein much of the receiver processing is enabled by techniques based on planar lightwave circuits (PLCs). The architecture is applicable to higher input data rates and *M*-ary PPM. In the following, we present the PPM encoding and decoding architectures and numerically simulated results.

PPM Encoding

The PPM pulse encoder converts a data word into a specific pulse (delayed) position. In general, a pulse inputted into the encoder is mapped to one of *M* contiguous, non-overlapping pulse positions that constitute a data frame, according to the word that is transmitted. The word consists of $N=\log_2(M)$ bits and its numerical value may be expressed as $K = \sum_{i=1}^{N} a_i \cdot 2^i$, where a_i is the transmitted binary symbol (0,1). If *K* is made to correspond to the number of unit pulse shifts (0 to *M*-1) applied to the incoming pulse, then the encoder may be implemented using a sequence of serial switches and parallel delay lines, as illustrated in Figure 1. The figure depicts discrete components, but a PLC implementation is feasible. Each switch, in this case a dual output modulator, is controlled by the data bit a_i and sends the pulse through a delay line containing a relative delay of either 0 or 2^i. For the case of M=16 at 12.5 Gb/s, four such modulator/delay line pairs are required for implementation, resulting in PPM frame times of 160 ps and slot times of 20 ps. Each modulator is driven by the bits of the demultiplexed word at 3.125 Gb/s, and each parallel delay line can apply a delay of 2^i x 10 ps. The required input pulse train for the encoder must have pulse widths < 20 ps to fit within a slot and have a repetition rate of 3.125 GHz, correspond to the frame size.

PPM Decoding

The PPM decoder receives a tranmitted frame, determines the delayed postion of the pulse, and matches the position to the corresponding unique binary word according to a look-up table. The implemenation, shown in Fig. 2a, reduces the amount of electronic processing required to perform this process by using alternative optical components. The slots are mapped into a virtual 4x4 array in conjunction with the control laws in Table 1 that determine the row and column of the array occupied by the pulse. As in previous control laws [2,3], s_n indicates the slots of each frame. These slots are first aligned together using an optical splitter followed by delay line arrays consisting of *n* unit delays (20 ps for our design). Optical couplers can perform the addition and balanced receivers can be used to perform subtraction. If an optical gate is incorporated prior to the receiver, the receiver bandwidth and all subsequent electronics need only operate frame rate, rather than having to accommodate the bandwidth of the actual pulse. The control law can be implemented within a planar PLC with erbium doped waveguide amplifiers (EDWAs) integrated in order to minimize losses.

Concluding Remarks

The 4x4 virtual array receiver implementation was captured in the RSoft OptSIM software and test runs for 512 symbols (2048 bits) were executed. The results are shown in Figure 2b. It shows that that the corresponding constellations are quite compact and contained within their row/column assignment. We expect that this approach can be readily extended to higher bit rates and/or PPM *M*-ary modes.

References

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[3] A. J. Mendez, V. J. Hernandez, R. M. Gagliardi, C. V. Bennett, and W. J. Lennon, "Development of pulse position modulation/optical CDMA (PPM/O-CDMA) for Gb/s fiber optic networking," in *Proc. Avionics, Fiber-Optics and Photonics Technology Conf. (AVFOP)*, 2006, pp. 28-29.

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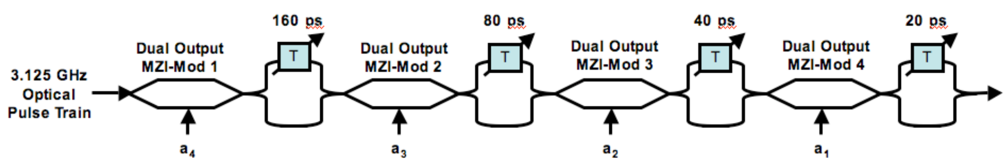

Figure 1. Cascaded Mach-Zehnder Interferometer (MZI) Design for the 10 Gb/s 16-ary Modulator.

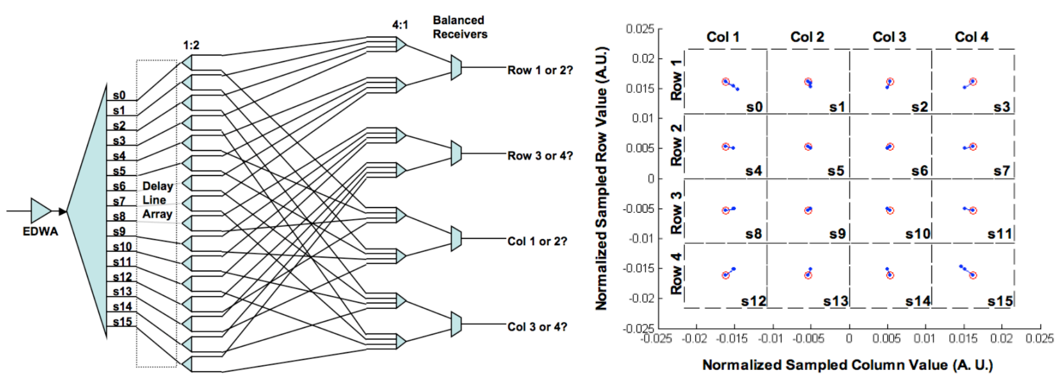

Figure 2. (a) PLC Implementation for the 16-ary PPM Demodulator/Receiver. (b) Output of receiver, showing mapping of 2^9 symbols into a look-up table. Circles indicate the transmitted symbol, dots the detected symbols.

Table 1. Summary of Control Laws for Virtual Array Receiver

Control Law	Result = 1	Result = -1
$(s_0+s_1+s_2+s_3)-(s_4+s_5+s_6+s_7)$	Row 1	Row 2
$(s_8+s_9+s_{10}+s_{11})-(s_{12}+s_{13}+s_{14}+s_{15})$	Row 3	Row 4
$(s_0+s_4+s_8+s_{12})-(s_1+s_5+s_9+s_{13})$	Column 1	Column 2
$(s_2+s_6+s_{10}+s_{14})-(s_3+s_7+s_1+s_{15})$	Column 3	Column 4

Note: If a control law result = 0, it indicates that the pulse is contained in the other two rows or columns.