Commissioning of the ATLAS pixel detector

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Abstract

The ATLAS pixel detector is a high precision silicon tracking device located closest to the LHC interaction point. It belongs to the first generation of its kind in a hadron collider experiment. It will provide crucial pattern recognition information and will largely determine the ability of ATLAS to precisely track particle trajectories and find secondary vertices. It was the last detector to be installed in ATLAS in June 2007, has been fully connected and tested in-situ during spring and summer 2008, and is ready for the imminent LHC turn-on. The highlights of the past and future commissioning activities of the ATLAS pixel system are presented.

Key words: Tracking and position-sensitive detectors, LHC, ATLAS, Pixel
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1. Introduction

The pixel detector is a critical component of the inner tracking system of the general purpose ATLAS detector [1] at the Large Hadron Collider (LHC). The first comprehensive proposal of the pixel electronic system was described in 1997 [2]. Production and quality assurance was performed at several sites and took place between 2001 and 2005. In 2006 the sub elements arrived at CERN and were tested. One pixel end-cap was operated and exposed to cosmic ray events. After the pixel package assembly on the surface the detector was installed in its final position in June 2007. The final connection took place in spring of 2008. Since then the detector has been commissioned and calibrated stand-alone. Future commissioning plans include cosmic rays data taking, beam-halo and beam-gas events and the combined data taking with the rest of the inner detector and the whole ATLAS experiment.

2. The ATLAS pixel detector

The ATLAS pixel detector [3,4] is the innermost element of the ATLAS Inner Detector [2] which provides charged particle tracking over the pseudorapidity range $|\eta| < 2.5$. The performance requirements for the pixel system are in particular: three-dimensional-vertexing capabilities, transverse impact parameter resolution of better than 15 μm and high efficiency and purity b-jet tagging capabilities. The design of the ATLAS pixel detector is driven by the L1 trigger rate (100 kHz) and latency (2.5 μs), the LHC bunch-crossing frequency (40 MHz) and the occupancy of $O(10^{-4})$ at a design luminosity of 10^{34} cm^{-2}s^{-1}.

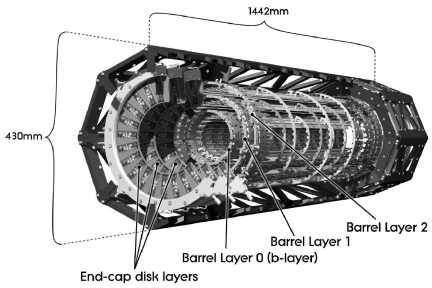

Fig. 1. Schematic view of the ATLAS pixel detector.

The major design choices are the smallest pixel size achievable which is limited by the electronics design, three pixel hits over the full pseudorapidity range, and the innermost layer at a minimum radius given by the beampipe radius. The latter two are realized by a system of three barrel layers at radii of 5, 9 and 12 cm and two end-caps with three disks each on either side of the barrel section (see Fig. 1). On the order of 1000 charged particles are created per bunch crossing at the design luminosity, which requires a high radiation dose tolerance up to 10^{15} n_{eq}cm^{-2} for the innermost layer, radiation hard electronics design and a low operating temperature of about $-10\,^{\circ}$C (realized by C_3F_8

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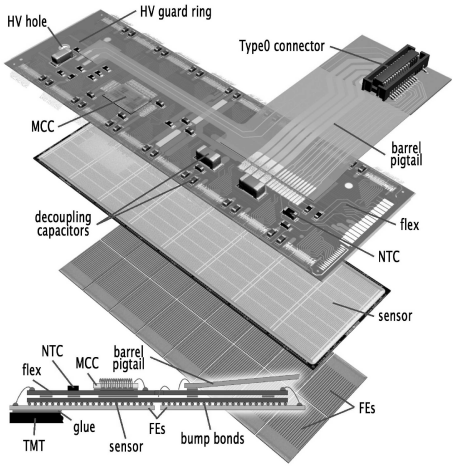

Fig. 2. Exploded view of an ATLAS pixel module.

evaporative cooling). Multiple scattering and secondary interactions are reduced by minimizing the material of all the elements in the system (thinned readout electronics, carbon support structure, aluminum cables and cooling tubes) leading to an interaction length of 10% X_0 at $\eta = 0$.

The pixel system consists of 80 million readout channels subdivided into 1744 identical pixel modules, giving a total active silicon area of about 1.7 m^2 and producing a power load of 10 kW.

2.1. *The pixel electronic system*

The ATLAS pixel module (see Fig. 2) is composed of a $250 \pm 3\,\mu$m thick oxygenated silicon sensor connected on the readout side to sixteen front-end chips by means of bump bonding and flip-chip technology and on the back side to a 100 μm thick fine-pitch, double-sided, flexible printed circuit (referred to as flex-hybrid) on which a controller chip (MCC) is situated. The n-bulk sensor contains n^+ implants on the readout side and a p-n junction on the other side with design features to provide maximum radiation hardness, single pixel isolation and minimal leakage current.

A charged particle traversing the sensor at normal incidence produces on average a signal of 20 000 electrons which is read out through the bump bond by the front-end chip. Each pixel cell of the chip has a size of 50 μm $\times$ 400 μm and contains an analog block where the signal is amplified and compared to a threshold. The charge-sensitive amplifier contains a feedback capacitor which is discharged by an adjustable constant current source, so that a nearly triangular pulse shape is obtained and the discriminator pulse width, so-called Time-over-Threshold (ToT), is proportional to the input charge.

The adjustable feedback current is tuned so that the average ToT for a minimum ionizing particle corresponds to 30 clock cycles which is optimized for high charge resolution and small pixel dead time. The adjustable threshold is tuned to 4000 electrons which is more than 10 σ away from the noise level. The fast rise time of the amplifier leads to

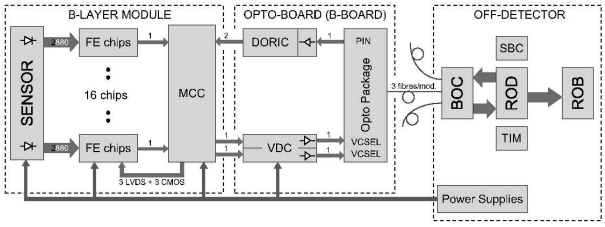

Fig. 3. Block diagram of the pixel detector system architecture.

a small timewalk which allows the assignment of the signal to the correct clock cycle if it consists of 5500 or more electrons.

The front-end chip contains 2880 pixels arranged in 9 column pairs and 160 rows. Pixel hits in a column pair are transferred to the end-of-column electronics and stored in a 64-hit buffer. The hits which are accepted by a level 1 trigger coincidence with the time stamp when the signal went above threshold are transferred to the controller chip using wire bond interconnections to the flex-hybrid and Low Voltage Differential Signaling (LVDS). The MCC, which also distributes off-detector Timing, Trigger and Control (TTC) to the front-end chips, collects the data from all sixteen chips, performs module based hit data event building and sends the data off-detector (see Fig. 3). The signals are transferred electronically through roughly one meter long micro-cables to optoboards which perform electrical-optical signal conversion and vice versa. Optical-fiber links have the advantage of high bandwidth, low radiation length and one can avoid ground loops and electromagnetic interferences.

The optoboards are composed of a PiN diode receiver that converts the optical data coming from the off-detector electronics (clock, trigger, control, configuration), and a VCSEL transmitter that performs the conversion of the data out of the detector at a maximum rate of 80 Mbit/s per optical fiber. The optical signal is transferred through roughly 80 m fibers to off-detector optical interface Back Of Crate (BOC) cards. Read-Out Drivers (ROD) perform further event building and data formatting. The RODs are then connected to the general ATLAS data acquisition system.

3. System test and cosmic rays operation

An 8% system test of one pixel end-cap was performed in a clean room at CERN from September 2006 to January 2007 as a realistic test of the detector operation. Production and pre-production services and off-detector components were used. The setup, including the DAQ readout and cooling was commissioned in long-run mode stress tests and the analog performance was measured. An automated service test system (referred to as connectivity test) was developed to verify functionality of the entire service chain including interlocks and the corresponding connectivity information in the slow control and detector calibration system. Procedures for operation, calibration and data taking

with cosmic rays were developed.

3.1. *Tuning of the optical communication*

An error-free data transmission requires the calibration of the optical links. The strategy for this tuning procedure was partially developed in the system test. In particular the data transfer from the detector to the BOC is critical for which three parameters need to be adjusted: one voltage for all 8 optical channels on an optoboard which controls the light output power of the VCSEL array, and at the receiving off-detector end the threshold and the data delay, determining the discrimination between a logical 0 and a logical 1 and the sampling time within the 40 MHz clock cycle, respectively.

An increased light output power-spread was discovered for lower optoboard temperatures which made it impossible to find parameter settings which guarantee error-free optical communication for certain channels. Therefore, it was decided to equip the optoboards with dedicated heaters to regulate the temperature up to 30 °C [4].

Some of the VCSELs on the optoboards produced very little or no optical power on all channels. This could be explained by a high common series resistance which results in an inadequate voltage to drive the VCSEL. A procedure to identify these flawed optoboards was defined and 7% of the total production was excluded.

3.2. *Analog performance and noise occupancy*

The threshold and noise of a pixel are measured with repeated charge injections into the pixel preamplifier by a pulse generator built into the front-end chip. A threshold scan measures the discriminator response versus the known injected charge. Analog performance and uniformity comparable with single module measurements [5] was reached for all tested modules in the end-cap: average threshold of $4002 \pm 1.3\,e^-$, threshold dispersion of $33 \pm 1\,e^-$ and average noise of $166 \pm 8.5\,e^-$.

The depletion voltage has a very characteristic evolution with fluence and its monitoring allows to predict the lifetime of the detector. With increasing irradiation of the sensor the depletion voltage decreases until type inversion occurs. Then the depletion voltage increases with irradiation. Above the maximum operating voltage of 600 V the depletion depth decreases. The measurement of the module noise occupancy versus sensor bias voltage allows the depletion voltage to be estimated before type inversion (below full depletion voltage the pixels are shorted resulting in a high noise occupancy). This method is sensitive to measured noise occupancies of 10^{-10} per pixel and clock cycle (less than 0.2% of the detector were identified as "hot" pixels with an occupancy larger than 10^{-5} and excluded). After type inversion the charge collection efficiency versus sensor bias voltage needs to be used, which has the disadvantage that it has to be evaluated periodically during data taking.

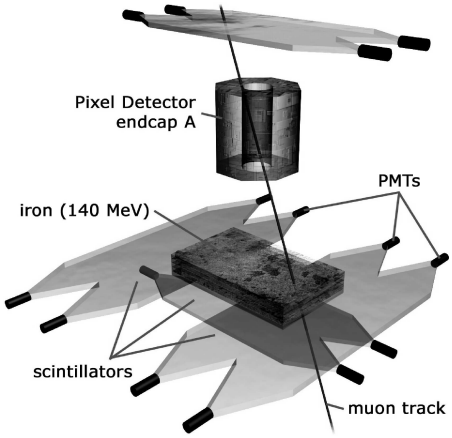

Fig. 4. Schematic drawing of the pixel end-cap cosmic setup.

3.3. *Cosmic rays operation*

The end-cap was oriented vertically to maximize the acceptance for cosmic rays (see Fig. 4). The trigger was provided by the coincidence of several scintillators, which were arranged to maximize the number of tracks passing through the three disks and at the same time to allow for inclined tracks. The rate of cosmic ray tracks traversing the sensitive area of all three disks was about 6 Hz.

A comparison between the cosmic ray data and the Monte Carlo simulation showed good agreement for distributions of ToT, number of pixel clusters on tracks, pixel cluster size and χ^2 of the tracks, which provides an important test of the ATLAS pixel detector simulation [6]. Approximately 24% of all tracks passed through regions of the detector where two modules overlap and a pair of hits is expected. This allowed to measure the pixel hit efficiency to be 99.5%. The same sample of tracks was used to derive an alignment correction. With the nominal geometry a spatial resolution in the precision coordinate of 23 μm was obtained. With the derived alignment correction this was improved to 16 μm close to the 14 μm expected from the Monte Carlo simulation.

4. Pixel package integration and installation

During spring 2007 the pixel detector was integrated with the service panels, the beampipe and the support structure. In parallel to the mechanical work the connectivity test that was developed during the system test (see Sec. 3) was performed to verify full functionality before installation. For the first time the whole detector was commissioned, operated and read out. The optical communication (see Sec. 3.1) was tuned for every module in the detector.

On June 25$^{\text{th}}$ 2007 the 7 m long pixel package was lowered 100 m into the ATLAS cavern, the following day it was inserted into the Inner Detector volume and on June 27$^{\text{th}}$ 2007 the ATLAS pixel detector reached its final position (see Fig. 5). Subsequently, the pixel services were deployed and all modules tested up to the end of the pixel package.

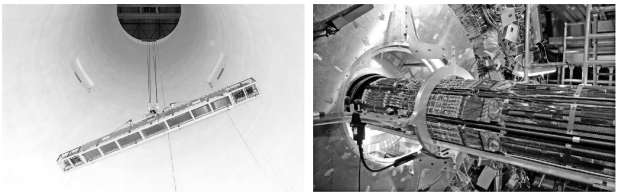

Fig. 5. Lowering and insertion of the pixel package.

11 returns of the bias voltage were found broken and all repaired successfully. At that stage 99.7% of the detector was known to be operational (0.1% module and optoboard failures and 0.2% pixel and front-end failures).

5. Final connection and commissioning

The final connection of the pixel detector was considerably delayed by several months due to problems related to other Inner Detector sub-detectors, in particular with the heaters of the evaporative cooling. End of 2007 the off-detector services were deployed and tested, and from February to March 2008 the final connection at the end of the pixel package took place (536 electrical, 588 optical and 88 cooling connections). Again the connectivity test (see Sec. 3) was performed to validate the electrical and optical connections: 11 out of 1744 modules were found to be non-operational and unrepairable (1 with a short and 10 without bias voltage), 37 have non-operational off-detector VCSEL channels but will be recovered as spares become available. These channels seem to keep dying with operation time. Diode IV curve measurements on the VCSELs are consistent with electro-static discharge (ESD) failures. Investigations are ongoing and a new production batch is ordered with improved ESD safety. For the time being the corresponding modules are disabled. A mapping problem was discovered at the end of March 2008 which required reconnection of half of the fibers at the BOC side.

Vacuum leak tests showed that 3 out of 88 cooling loops have leaks, all of them in the end-caps. Studies are ongoing to determine whether there are long-term problems with operation of these loops. Exhaust cooling pipes had to be rebuilt due to corrosion problems. All but one cooling loop could be operated and successfully handle the heat load of the detector both for a nominal power consumption of 4 W per module and the maximum power consumption of 6 W expected for the end-of-lifetime. Cooling loops were switched on one at a time, the temperature sensors were checked and used to validate the module-cooling loop mapping.

A cooling plant accident on May 1st 2008 prevented the completion of the sign-off. Three out of six compressors that liquefy the C_3F_8 fluid were affected. No significant fluid contamination reached the detector. The compressors were equipped with additional sensors and filters to prevent failures of the same kind, the cooling plant was fully cleaned and was recovered after $2\frac{1}{2}$ months.

At the end of July the LHC beampipe bake-out took place which was needed to improve the vacuum quality. Cooling of the innermost pixel layer and the end-caps was required to prevent permanent damage. The bake-out took 3 days and the temperature of the beampipe was brought up to 250-300 °C.

Subsequently the commissioning was resumed. On August 28th 2008 the whole detector was configured for the first time. All 88 cooling loops can be operated, which is straightforward for the top hemisphere, while in the bottom hemisphere the heat load from the modules is needed for stable operation. More than 99% of all modules can be powered without any problem, thresholds scans were performed for all of them, less than 5% with instabilities in the optical communication (expected to be fixed before turn-on). Data was taken with random triggers up to 10 kHz. All pixel opto-heaters are working at the target temperature of 20 °C.

6. Conclusion and outlook

The highlights of the past and future commissioning activities of the ATLAS pixel system have been presented. It has been a long way from design, production, system test, cosmic rays operation to the pixel package integration, installation, final connection and commissioning. In particular over the last two years many unforeseen problems have appeared with the mechanics, the cooling and the optical communication. All of them have been overcome so far.

The first ATLAS global run including the pixel detector is scheduled for the first week of September 2008. On September 10th the first LHC beam at 0.45 TeV will be injected with collisions at 10 TeV before the end of the year. Cosmic, beam-halo, beam-gas and collision data will be used to commission, calibrate and align the detector further to ensure high quality pixel data taking.

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