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Abstract-- **An Integrated Circuit (IC) readout chip with four channels arranged so as to receive input charge from the corners of the chip was designed for use with 5- to 7-mm pixel detectors. This Application Specific IC (ASIC) can be used for cold neutron imaging, for study of structural order in materials using cold neutron scattering or for particle physics experiments. The ASIC is fabricated in a 0.5-µm n-well AMI process. The design of the ASIC and the test measurements made will be reported. Noise measurements will also be reported.**

I. Introduction

As sources of cold neutrons have increased in brightness, the need for faster response and improved simultaneous time of flight measurements has grown. The ASIC described in this paper was designed to be used with a three-dimensional imaging array for cold neutron detection. Sub-arrays of pixels are to be interlaced in such a manner as to reduce the dead zone between them. Each of these pixel sub-arrays will have an ASIC placed on a read-out card aligned to the intersection of 4 pixels. The ASIC, which has four channels on the chip, includes a low-noise, fixed-gain preamplifier circuit that detects positive going input charges. A bipolar pulse shaper circuit with a 1µs full-width half-max (FWHM) follows the preamplifier. The signal from the shaper is passed through a gain-buffer stage before being brought to a pin for monitoring. The signal after the first shaper is also input to another gain stage prior to the discriminator that outputs a trigger pulse. The output of the discriminator is then converted to a current pulse output to minimize crosstalk effects. Two of the four channels also have a 300ns period one-shot circuit following the discriminator to evaluate the effect of constant pulse-width versus variable pulse-width current outputs. The ASIC also has internal Digital to Analog Converters (DACs) for setting the discriminator threshold and for preamp feedback resistance adjustment. There is an on-chip band-gap PTAT reference circuit to provide the reference voltage 'Vref' as shown in the channel block diagram. The four channels are identical except for the inclusion of a one-shot circuit between the discriminator and the voltage to current pulse converter in two of the four channels. The ASIC is fabricated in a standard 0.5µm n-well CMOS process. A block diagram of a single channel of the ASIC chip is given in Fig. 1.

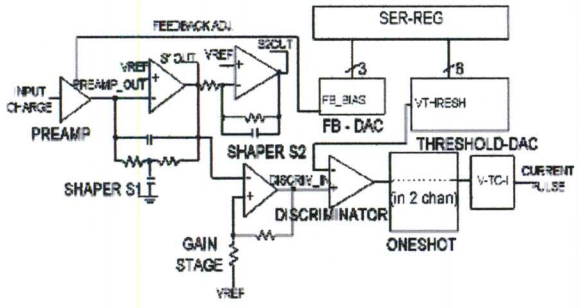

Fig. 1. Single channel block diagram.

II. Preamplifier and Shaper

The preamplifier section consists of a single fixed gain stage. It is a basic charge to voltage amplifier with a gain of 3.5mV/fC. The preamplifier circuit is a low noise, positive-polarity charge amplifier circuit. The design is based on the low noise preamp topology previously published [1]. The preamplifier is an inverting, single gain stage, cascode amplifier followed by an active resistor divider stage with a combined 0.25pF poly-poly feedback capacitor. The preamplifier input is referenced to the positive power supply rail and its output swings towards the negative rail for positive input charges. The feedback has a gate controlled transistor whose resistance can be changed to adjust the preamp output decay. A schematic of the preamplifier structure is shown in Fig. 2.

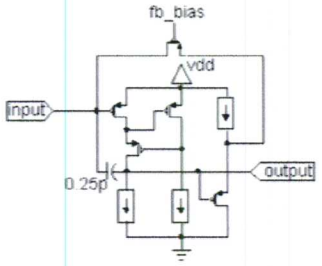

Fig 2. Charge Sensitive Preamplifier.

The first stage shaper has a gain of 2.5V/V, rise time of 100 ns and a bipolar shaping of about 1µs FWHM for the first lobe. The output of this shaper stage goes to a second stage shaper buffer and also to a gain stage that feeds the discriminator input. The second stage shaper buffer has a gain of 2V/V and the output of this shaped and buffered signal is routed to the output pad. A schematic of the shaper section is shown in Fig. 3.

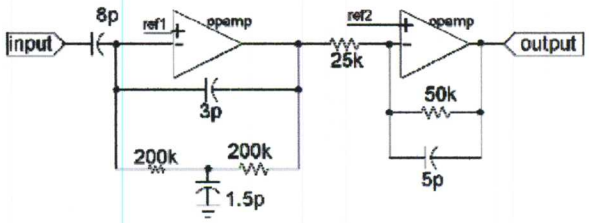

Fig. 3. Schematic of the Shaper section.

III. Discriminator, DACs and Serial Control

An extra gain stage of 3V/V is inserted prior to the discriminator input. The leading-edge discriminator has a differential input with a second stage to convert the differential output to a single ended output [2]. In two of the channels a one-shot circuit, built to convert the variable pulse widths of the discriminator to a constant pulse width of about 300 ns, follows the discriminator circuit in the channel. All channels have a voltage-to-current converter to convert the digital voltage output to an equivalent output current pulse of about 70uA [3]. This minimizes crosstalk feedback when the

channels fire. Each channel also has a constant current reference of 35 uA for implementing the interface circuitry. The on-chip DACs are used for remote control of the chip parameters such as discriminator threshold and preamp feedback adjustment via the serial string. The discriminator threshold is adjusted by a 6-bit voltage DAC and has a minimum threshold of approximately 1fC. The preamplifier feedback resistance can also be remotely adjusted by using a 3-bit selectable divider string to set the feedback bias voltage of the preamp feedback transistor. This effectively changes the preamp time to return to baseline after a pulse and is used to compensate for the detector leakage current. Each channel therefore has a 9-bit serial register to set the discriminator threshold DAC and the preamp feedback DAC values. The chip has a total of 36 serial bits which can be daisy-chained to the next chip for readout and control. The serial control also has a non-destructive read-back feature that can be used to verify proper loading of the chip serial data values. The chip generates its own reference voltage using an internal band-gap reference circuit to provide the reference value of approximately 2.785V which is used by the different circuits in the channel. A separate VMID bus that can utilize an external reference voltage is also included. This chip has a test channel with all its intermediate test points brought out to pads for probing. The chip also has separate power buses for the preamp power, analog power and digital power.

IV. Chip Layout and Readout Card Structure

The layout of the ASIC with four channels was approached with the readout card requirements and detector geometry in mind. An arrayed structure would have lead to routing constraints so the chip was designed such that the input of each channel was aligned to a corner of the chip. A picture of the actual layout of the chip is shown in Fig. 4 with the four channels along the four sides of the chip, the DAC structure in the center and power rings for the power supplies around the periphery.

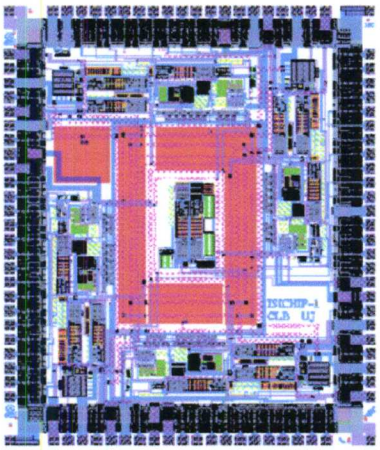

Fig. 4. Diagram of the chip layout.

The readout card on which the bare die will be mounted matches the dimension of the pixel array. There will be a bare-die chip (which is 3.5mm.x 3.0mm.) at the intersection of every four pixels [4]. The inputs will be connected directly down to the pixel via a wire interconnect bonding [5]. The current outputs from all the channels will be routed to a 48-channel Digital Memory Unit (DMU) bare die that will process the current output and relay relevant information. A readout card with the die placement design for a 6X6 array is shown in Fig. 5. This DMU was originally developed for a PHENIX experiment in conjunction with the University of Lund. The readout card will be aligned with the pixel detector and the input wire will be dropped through a via on the ROC and bonded directly to the pixel detector below it.

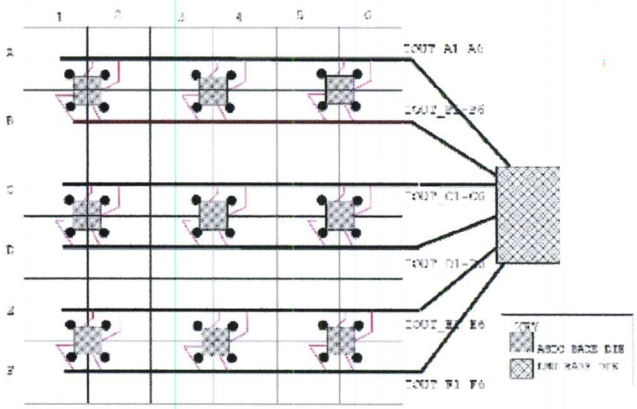

Fig. 5. Placement of bare die on a Readout Card.

V. Test Results

The test results are from a multi-layer board-level bench test of packaged die. The testing was done on the chip to ensure that all channels and other major features of the chip such as serial data flow and DAC functions were functional and to characterize the chip. The equivalent noise curve vs. input capacitance is given in Fig. 6.

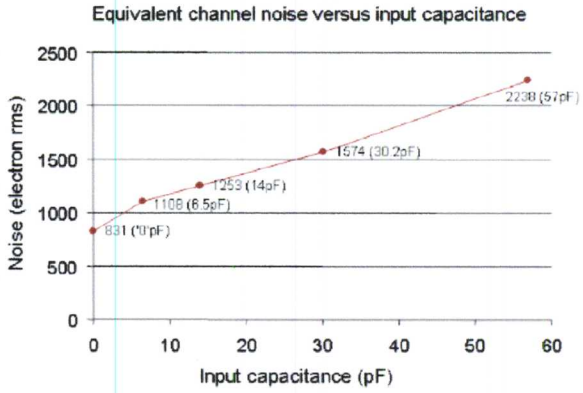

Fig. 6. Equivalent noise vs. input capacitance.

The above noise measurements were made with the input capacitor tied to the preamp positive power supply to emulate the pixel detector set-up. The '0'pF noise measurement is the output noise measure with the input bond wire removed for that

channel. The digital signals used for serial control were disconnected for this test.

One of the four channels was a test channel with all its intermediate nodes brought out for observation. All the designed features on the chip were functional. The measured preamp gain between different channels on a chip as well as between different chips was within 3% of the designed value. The preamp showed good linearity over a 1.6V range. The measured nonlinearity for the preamplifier was less than 1%. Measured transfer curves and range limits for the preamp, shaper and gain outputs are given in Fig. 7. Measured DAC outputs were within 3% of the simulated values. Testing of the chip with the readout card aligned to the pixel array is planned in the near future.

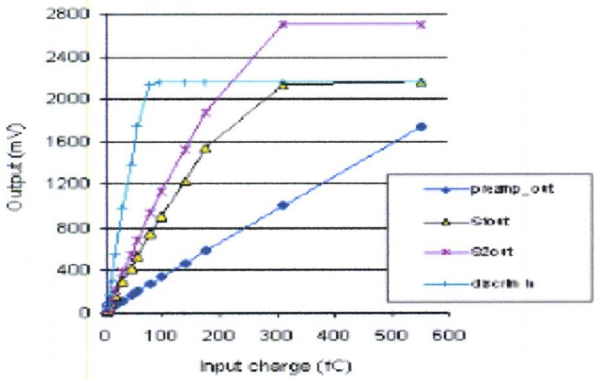

Fig. 7. Preamp, shaper and gain stage transfer curves.

VI. Conclusion

The minimum pickup of the discriminator on the board level bench tests was about 1.8 fC. However, the minimum pickup over noise that resulted in a zero noise counts per second fell short of expectations and a factor of three worse than what the noise measurement shown in Fig. 6 would suggest. Some of the reasons for this could be attributed to the fact that the tests were done on a packaged die with long bond wires which contributed to crosstalk, and significant digital noise from the serial setup which could not be disconnected during testing without resetting the serial string to its default values. The test channel with all its intermediate nodes brought out was also a noise source in terms of crosstalk. The one-shot channels also produced more noise while switching compared to the channels without them. Tests to be conducted on the actual pixel detector with the bare die mounted on the readout card would give a true value of the minimum signal pickup possible without picking up noise.

VII. References

[1] C. L. Britton, Jr., M. N. Ericson, S. S. Frank, J. A. Moore, M. L. Simpson, G. R. Young, R. S. Smith, L. G. Clonts, J. Boissevain, S. Hahn, J. S. Kapustinsky, J. Simon-Gillo, J. P. Sullivan, H. van Hecke "A 32-Channel Preamplifier Chip for the Multiplicity Vertex Detector at PHENIX ", Review of Scientific Instruments, Vol. 70, No. 3, pp. 1684-1687, March 1999.

[2] W. L. Bryan, U. Jagadish, et al., "TGLD: A 16-Channel Charge Readout Chip for the PHENIX Pad Chamber Detector Subsystem at RHIC1"

[3] R. S. Smith, et. al., " A Discriminator with a Current-Sum Multiplicity Output for the PHENIX Multiplicity Vertex Detector," *IEEE Transactions on Nuclear Science*, Vol.44, No.3, pp.389-392, June 1997.

[4] J. Walter, et al., "A CMOS Signal Conditioning ASIC for Large Silicon Pixels," in *IEEE NSS Conference Record*, 1996, pp. 509.

[5] E. H. M. Heijne., "A 1006 Element Hybrid Silicon Pixel Detector with Strobed Binary Output," *IEEE Transactions on Nuclear Science*, Vol.38, No.9, pp. 654-661, August 1992.