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Integrated Optical MEMS using Through-Wafer Vias and Bump-Bonding

Scott K. Frederick, Frederick B. (Rick) McCormick

Prepared by
Sandia National Laboratories
Albuquerque, New Mexico 87185 and Livermore, California 94550

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Scott K. Frederick, Frederick B. (Rick) McCormick

Integrated Microdevice Systems, Applied Photonic Microsystems

Sandia National Laboratories

P. O. Box 5800

Albuquerque, NM 87185-0385

Abstract

This LDRD began as a three year program to integrate through-wafer vias, micro-mirrors and control electronics with high-voltage capability to yield a 64 by 64 array of individually controllable micro-mirrors on 125 or 250 micron pitch with piston, tip and tilt movement. The effort was a mix of R&D and application. Care was taken to create SUMMiT™ (Sandia's ultraplanar, multilevel MEMS technology) compatible via and mirror processes, and the ultimate goal was to mate this MEMS fabrication product to a complementary metal-oxide semiconductor (CMOS) electronics substrate. Significant progress was made on the via and mirror fabrication and design, the attach process development as well as the electronics high voltage (30 volt) and control designs. After approximately 22 months, the program was ready to proceed with fabrication and integration of the electronics, final mirror array, and through wafer vias to create a high resolution OMEMS array with individual mirror electronic control. At this point, however, mission alignment and budget constraints reduced the last year program funding and redirected the program to help support the through-silicon via work in the Hyper-Temporal Sensors (HTS) Grand Challenge (GC) LDRD. Several months of investigation and discussion with the HTS team resulted in a revised plan for the remaining 10 months of the program. We planned to build a capability in finer-pitched via fabrication on thinned substrates along with metallization schemes and bonding techniques for very large arrays of high density interconnects (up to 2000 x 2000 vias). Through this program, Sandia was able to build capability in several different conductive through wafer via processes using internal and external resources, MEMS mirror design and fabrication, various bonding techniques for arrayed substrates, and arrayed electronics control design with high voltage capability.

Acknowledgment

Contributors (early):
Rufner, Judith (Heidi) (Program Manager)
McCormick, Frederick B. (Principle Investigator)
Frederick, Scott K. (integration)
Bogart, Gregory R. (vias and mirrors)
Dagel, Daryl (vias, mirrors, bonding)
Fleming, James G. (vias)
Shul, Randy J. (vias)
Jokiel Jr., Bernhard (bonding)
Hsia, Alexander H. (electronics)
Cowan, William D. (electronics)

Contributors (later):
McCormick, Frederick B. (Program Manager)
Frederick, Scott K. (Principle Investigator)
Chanchani, Rajen (bonding)
Anderson, Robert C. (vias)

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Introduction

Project Purpose (Early)

Many evolving applications share a common need to densely integrate arrays of sensors or actuators with their associated addressing and control circuitry. Optical micro electro-mechanical systems (OMEMS) are the key technology to building large micro-mirror arrays that will improve optical target identification capability by a factor of 3. This project will also provide Sandia with a differentiating strength in advanced free-space communication links, phased-array radar antennas, hyperspectral imagers, and chemical agent detectors.

Our approach involves the direct bonding of MEMS die to complementary metal-oxide semiconductor (CMOS) substrates via metal interconnects and matching metal bumps and will lead to arrays 10 times larger than standard packaging approaches permit. Noise, attenuation, complexity, and cost limit the size of current mirror arrays packaged by wire bonding techniques, while direct integration approaches in which the MEMS fabrication process is fundamentally altered to accommodate the electronics or vice versa suffer from compromises that reduce usefulness and applicability.

The intent of our effort is to bypass these limitations and compromises by realizing through-wafer vias that are compatible with Sandia's ultraplanar, multilevel MEMS technology (SUMMiT™). To fully develop and demonstrate this integration process, we will leverage "standard" SUMMiT MEMS processes to fabricate and test a 4096 OMEMS mirror array and bond it to a suitable addressing/control integrated circuit.

Project Purpose (Later)

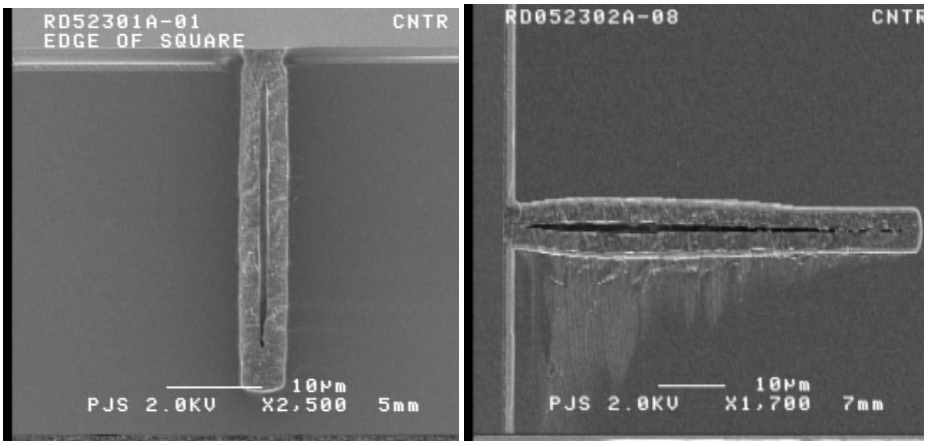
Leverage the through wafer via development and manage the reduced 3rd year resources to benefit Sandia's efforts in developing chip-stacked FPA technology.

Early Program accomplishments

Vias and Mirrors

2005

Through Wafer Vias (TWV) ***(Patent Caution)***



(a) (b)

Figure 1. Poly plug demonstrating silicon nitride liner and polysilicon fill. Minor key holes are observed for the fill process. (a) ~5x40µm via (b) ~6x60µm high aspect ratio via.

A novel process flow has been developed to generate a TWV with high density and high voltage capability >100V (see Figure 1) and a technical advance has been written on this process. The poly plug design for the front side allows for a high density fill factor. Other approaches were considered with this approach being the best fit for capabilities available and highest flexibility. A high aspect ratio silicon etched hole on the backside is one approach to gain contact with the via plug. The two sided approach utilizing the via plug design would allow for wafer thinning, or with the high aspect ratio silicon etched hole, a polysilicon fill or electroplated metal fill process. Work has been initiated with Sandia's Microsystems and Engineering Applications (MESA) microfabrication facilities and DuPont to develop a dry resist film process for patterning films in the presence of deep holes or trenches. The 9 mask set was designed and ordered. Two wafer lots incorporating SUMMiT tilt-mirrors on top of arrays of poly-plug vias were started in Sandia's Microeletronics Development Laboratory (MDL) and completed in 2006. A via test plan was developed to test the final structures once fabricated.

Some of the main challenges so far include two-sided processing (its additional complexity), maintaining uniform high aspect ratio silicon etch depths across the array, and keyhole management. Future challenges include backside patterning and etching and scaling to SUMMiT V.

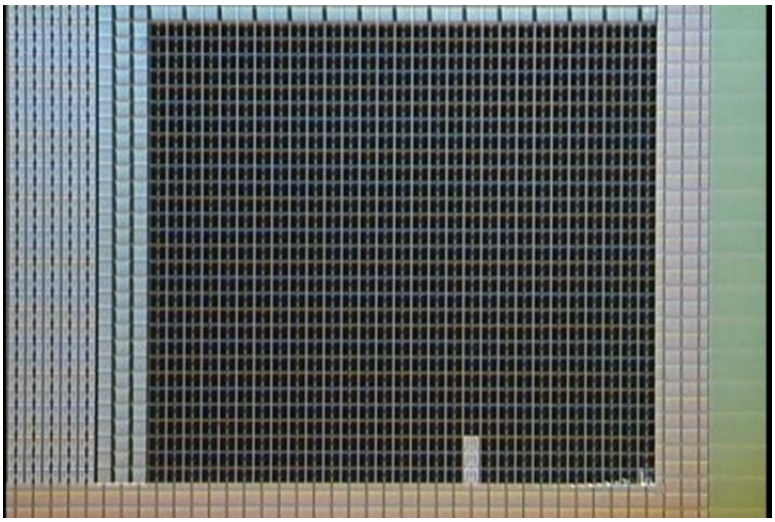


Figure 2. Lower right quadrant of 64 x 64 mirror array tilted with approximately 10 V.

2006

More wafer lots were started incorporating SUMMiT tilt-mirrors on top of arrays of poly-plug vias to support two approaches to MEMS wafer backside metallization and reductions in via impedance. See Figure 3 for backside etch example. See Figure 4 for backside metallization example. We manufactured and used mirror wafers to support bonding experiments. We assessed circuit viability by comparing the footprints of various circuit approaches to the unit cell areas. Based on assessment, it was determined that a pitch of 125 microns would be used.

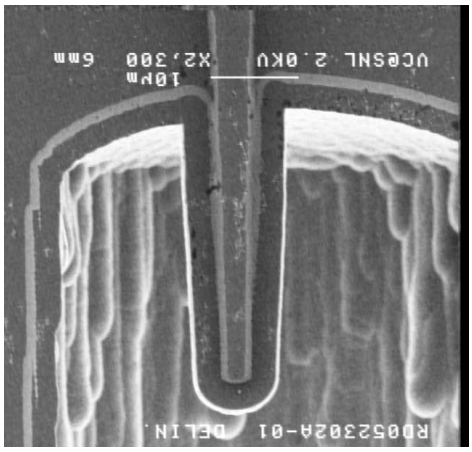


Figure 3. Top side via with back-side etch and polysilicon.

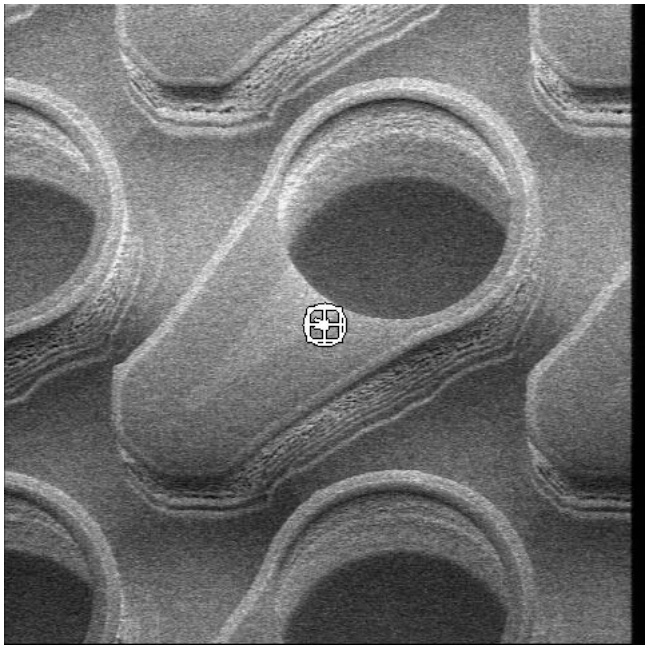


Figure 4. Post etch negative resist back-side metallization.

Summary

All technical difficulties for creating conductive through wafer vias on 600 micron thick substrates were resolved through design, peer review, and experimentation. A SUMMiT compatible process was created and used for the conductive vias. Back side substrate metallization in conjunction with vias was successful. Micro-mirror fabrication and demonstrations showed greater than 99% yield on via conductivity.

Bonding

2005

Backside Bumps and Chip-to-Chip Attachment

Two key packaging issues were the bump-attachment technology selection and the underfill material selection and process development. Several solutions for the bump-attachment process were investigated. The original intent of the packaging process was to create a solder micro-ball grid array on the back of the mirror array die over the through wafer vias. However after a detailed look at the metal reflective surface (Cr-Au)

that was anticipated to be used, it was discovered that the microstructure changes when heated to over 100C caused irreversible mirror deformation. From experiments on other Cr-Au coated MEMS mirror surfaces, it was determined that thermal excursions had to be lower than 80C to guarantee the integrity of the Cr-Au film. The lowest temperature solder system is a Sn-In eutectic at 117C, which is still too high to be of use for this application. Therefore the idea of creating solder bumps on the back of the MEMS was abandoned for conductive epoxy bumps.

In this approach gold studs are electroplated over the MEMS vias or offset pads (Figure 5). The ends of the studs are coated with a silver-filled electrically conductive epoxy with a low cure temperature (lower than 80C). The die is the placed on the target location and the epoxy is cured. This process has gained favor in recent years in Japan and Europe for chip-on-flex electronic devices. To test this process a test vehicle consisting of three different via test structures was created. The test structures consist of 70x70 array of electrical connections and are compatible with the via test structures supporting 125um x 125um unit mirror cells. The test structures were created using lift off of a Cr-Pt-Au stack on BK-7 glass. Target chips have been fabricated and the gold studs were electroplated on what would be the MEMS chip. Work was started on creating a thin conductive epoxy layer by blading. The bumped chip would be picked up and dipped into the thin epoxy layer to apply epoxy uniformly to the entire bump array at one time. Earlier attempts at thinning epoxy by spinning were not satisfactory as the silver flakes in the epoxy would separate from the binder.

The underfill epoxy is used to preserve the chip, electrical connection and package, while allowing the silicon MEMS device to be released during a HF-HCl acid soak. Initial experiments were performed to select promising underfill materials. Three low temperature curing epoxies were purchased along with four different underfill epoxies that are claimed to be resistant to acid attack. Epotek 377 was found to perform very well against the release chemistry (Figure 6), while U300 did not. Epotek 377 was tested for low-temperature curing (87C for 24 hours). Epotek 353 went through a release chemistry screening to test acid resistance. A Masterbond underfill was experimented with but not pursued.

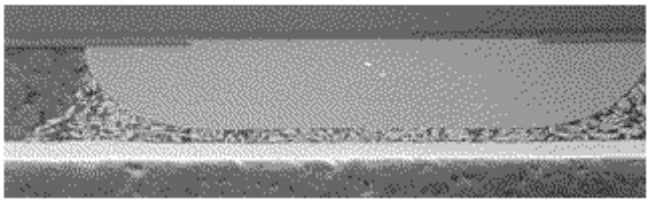


Figure 5. (above) Polymer flip-chip consists of a Ni-Au bump with a coating of silver-filled epoxy to provide electrical continuity to the underlying pad.

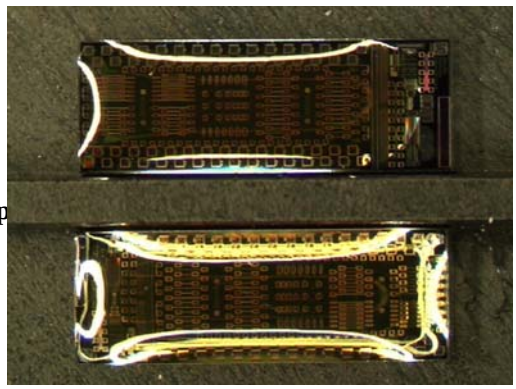


Figure 6. (right) Epotek 377 underfill cured for 1 hour at 150C shows very good acid resistance during a 40 minute soak in a 49% HF solution.

2006

We investigated several solutions for the bump attachment process and selected a conductive epoxy over gold bumps (See Figure 7) approach rather than a higher-temperature solder reflow approach. We made special fixtures to apply H20E-PFC, to silicon substrates with metallized pads and gold bumps. One of these substrates was bonded to an interposer and underfilled with Epotek 353ND and subsequently survived the MEMS HF-HCl release process. More work is needed to increase bonding success observed through continuity testing

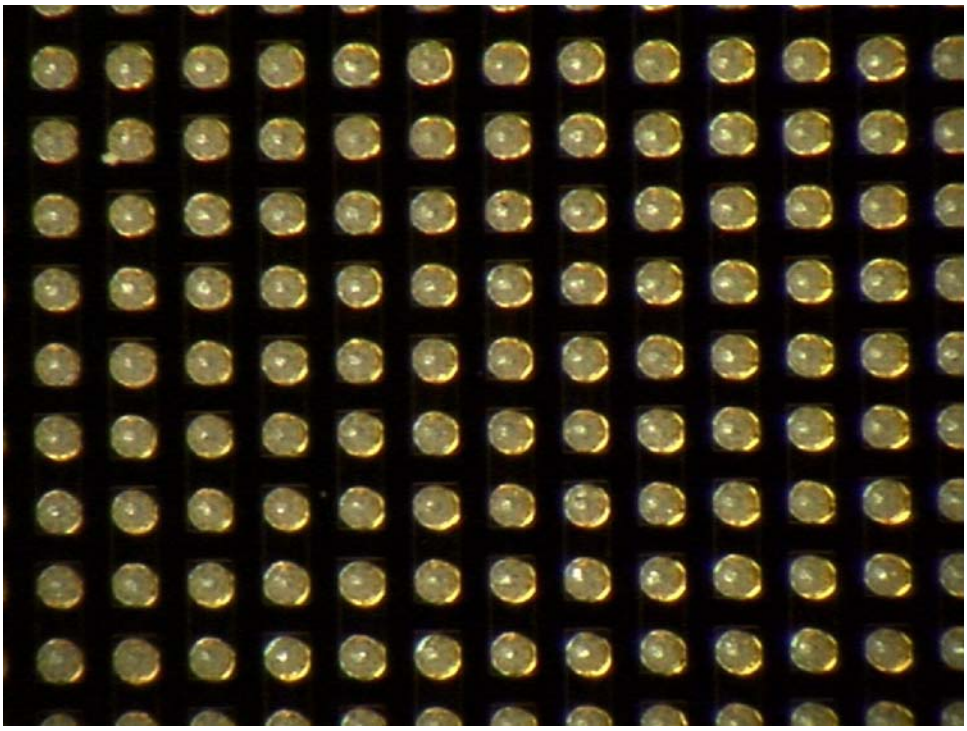


Figure 7. Conductive Epoxy over gold bumps

Summary

A low temperature bonding and underfill process was developed for bonding substrates with 2 dimensional arrayed metallization on 125 um pitch. Extensive effort went into experimentation to determine the best process for the target attach application and then

into determining the best method for applying conductive epoxy to properly sized gold bumps. Extensive effort went into identifying and using an underfill to strengthen bonded substrates. Substrates were designed to facilitate continuity testing.

Electronics

2005

Pixel Electronics Design

The goal of the circuitry design effort depicted in Figure 8 below was to develop a set of general guidelines to support varied high voltage OMEMS applications. Circuit viability was assessed by comparing the footprints of various circuit approaches to the unit cell areas (both 125 um and 250 um square were considered). This first order assessment represents a low cost method for screening circuit viability and continued throughout the project. For example, a localized charge pump architecture (which would otherwise be attractive because it eliminates the high voltage supply) proved to be much too large for our unit cells. Conversely, a digital level shifting circuit with CMOS switching and power dissipation characteristics appears to be an attractive approach for digital modulation of mirror electrodes due to the small number of transistors required. Other schemes with as few as 2 transistors per electrode have been defined and simulated.

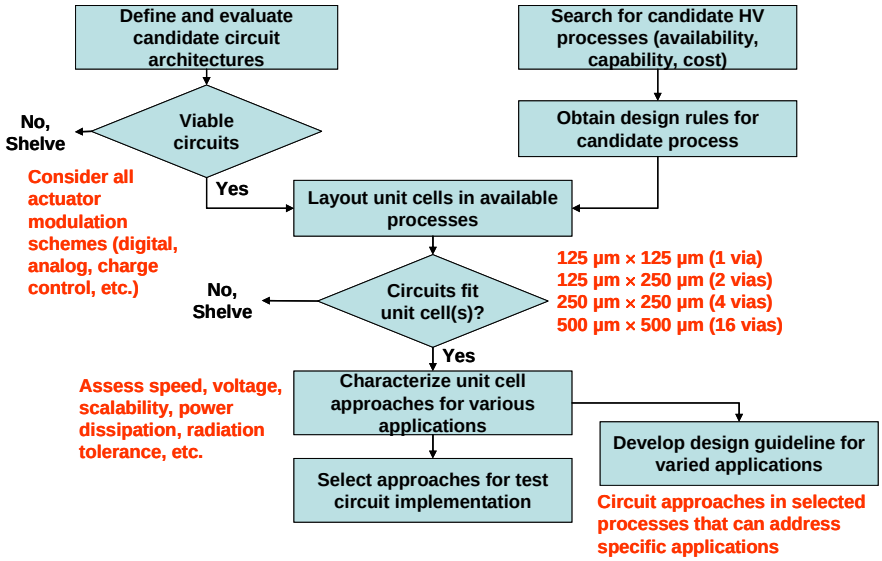


Figure 8. Circuitry development approach.

In parallel, a search for HV circuit processes was conducted to support our initial test chip fab runs. None of Sandia's current and planned CMOS processes are well suited to HV circuitry because the process changes made for radiation hardness are often incompatible with HV transistors. The search for external vendors was constrained to vendors that offer a multiproject foundry capability to allow low cost implementation of test circuits. Several companies have been identified as having technology that could be

used in our design, and NDA's are in place with two of them (Austriamicrosystems and PolarFab).

2006

Through simulation we made substantial progress toward determining the best architecture for 125 square micron high-voltage (30 V) unit cells (see Figure 9) with an emphasis on scalability. We determined that the multiproject foundry Jazz Semiconductor (formerly PolarFab) offers the high-voltage process best suited to Sandia. We completed the majority of the work to integrate Sandia design rules with Jazz Semiconductor design rules (significantly more challenging than it sounds). System level architectures, high-voltage unit cells, and control and interface electronics have all been schematically captured and simulated. The building blocks and sample array for the digitally modulated architecture were partially laid out for Jazz Semiconductor's PBC4 process.

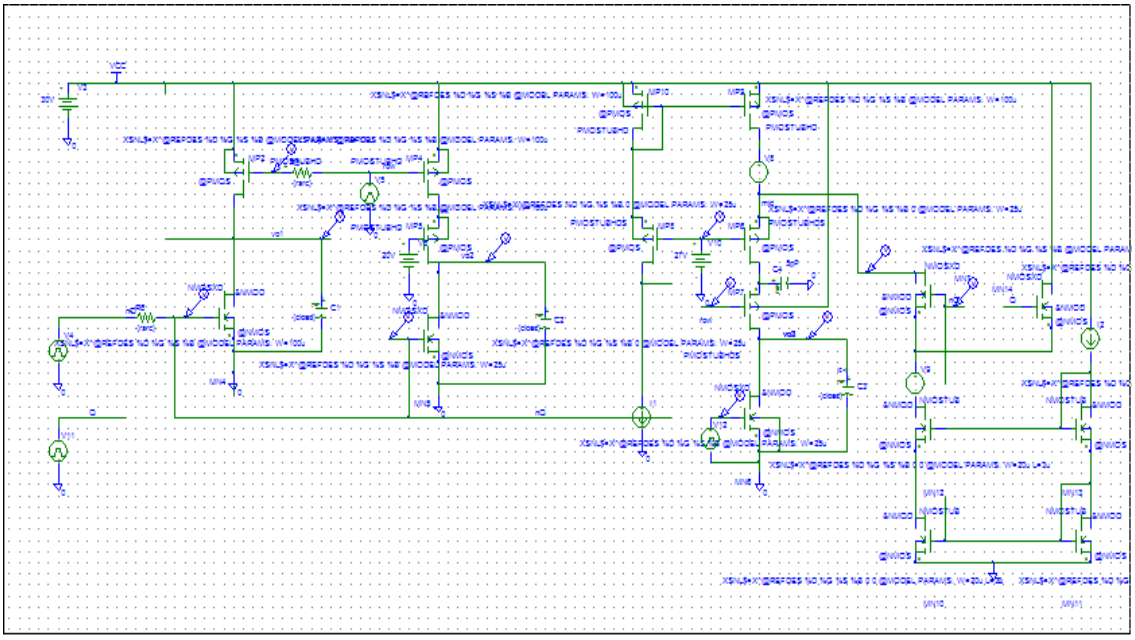


Figure 9. High Voltage Unit Cell Simulation

Summary

Basic fabrication architecture issues make Sandia CMOS fabrication tools unsuitable for high voltage (30V+) electronics. Extensive work was done to identify suitable fabrication

resources, establish non-disclosure agreements, integrate the resource design rules into Sandia design tools, select the primary resource, and complete simulations of the resulting designs. Much of this work had to be repeated as PolarFab was purchased by Jazz Semiconductor and significant delays were realized. This change also resulted in increased fabrication costs. A request was submitted to the LDRD office to fund a fabrication run of a completed arrayed high voltage electronics design, but this request was denied. The impending program funding reduction and change of program direction stalled the electronics effort at this point. It is the author's opinion that the best interests of Sandia National Labs were not served by failing to fund the needed fabrication run to support high voltage electronics and control electronics for arrayed micro-technologies. Program administrators do not agree. If Sandia has a future need for individually controlled, arrayed micro-technologies, those involved with this effort should consult with the contributors to this program.

Integration

2005 and 2006

Microsystem Integration

The successful integration of the novel electronics, deep via and mirror arrays, and ball bumping and packaging approaches described previously in this report will require careful risk assessment and mitigation to avoid problems and delays at the microsystem level. Some of the risks identified are: 2-D array pitch incompatibility for assembly, metallization and surface for bonding could be incompatible with the bonding process, insufficient voltage to drive a MEMS mirror, proof of concept exercises need major modification to work in the system, insufficient preparation for testing of sub assemblies, proof of concept exercises not easy to test, impedance and isolation of vias, and stress and temperature during assembly.

Risk mitigation activities were executed throughout the program. While the initial electronics effort was mostly for high voltage proof of concept, controlling mirrors with one electrode will make subsequent three electrode efforts only an incremental change. Thorough discussion of metallization requirements took place with all groups from the standpoint of adhesion, composition, compatibility and reliability. Time was built into the schedule for tweaks related to specific ball size, pitch of balls/pads and amount of epoxy required for reliable device operation while minimizing unwanted electrical shorts. Discussions of stress and temperature concerns for assembly of finished product led to a primary bonding choice of conductive epoxy to bond MEMS wafer to electronics wafer post mirror release which better supports existing process flow. Offset pads have been designed to offer a mechanically stable surface for ball bonding of MEMS wafers. Capacitance and insulation capabilities of vias have been calculated. Absolute minimum voltage for full scale mirror movement is estimated at 20V, and initial electronics design should offer up to 40V for single ended drive. A torsion spring was attached to the mirrors allowing easy visual test of piston only controlled mirrors. Suitability of existing test equipment was verified for this effort.

Recent Program Accomplishments

Prior to getting started on developing via processes and substrates, bumping processes, and bonding processes, several months of time went into understanding the needs of the HTS Grand Challenge (GC) LDRD. As this project was in the early stages, it was not straightforward to simply identify "something" that could be built that would ultimately benefit the FPA work. Time spent sorting out the needs of the HTS GC LDRD was well spent, as it helped benefit this project and pushed the FPA work forward (decisions had to be made).

Vias and Wafer Thinning

2007

Tungsten Vias were created in the device layer of an SOI (silicon on insulator) wafer. Vias were 1.5um (microns) in diameter and on a pitch of 20, 30, 40 and 60um in different regions of the wafer. Via lengths were the entire thickness of the device layer, at 20um thick. This produced a challenge during the silicon etch portion of fabrication to deliver an aspect ratio of over 13. A clean near vertical sidewall via was created, spanning from top surface of wafer to the buried oxide. The chemical vapor deposition (CVD) Tungsten (W) fill was virtually complete with only one small keyhole located approximately 5um from top surface of via. Figure 10 shows the W via during etch development before CMP of W film back to 1.5um oxide film. They are slightly rough because no surface grinding or polishing was done after cleaving the sample. These images show that the via did not land on the buried oxide on this development wafer, however the depth was adjusted for the remainder of the product wafers.

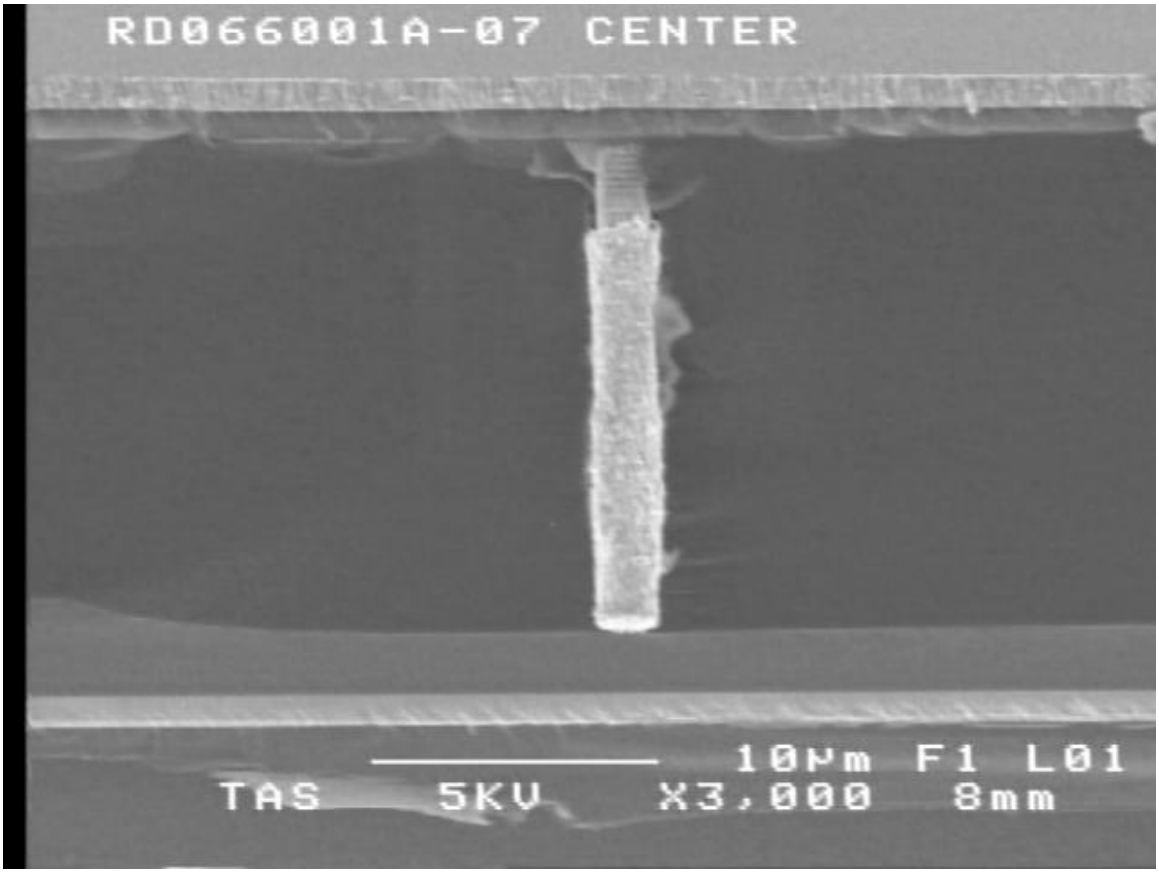


Figure 10. Tungsten via. Etch step was just short of buried oxide layer.

Summary

Successful conductive vias were fabricated on thinned substrates. Via layout was designed to support bonding experiments and continuity testing.

Bonding

2007

One goal for the portion of the program was to design a four quadrant layout for a 6 inch wafer to support pads and daisy chain interconnects for vias. Each quad was 50mm x 50mm (see Figure 11. Via pitch and pad diameters as follows:

Quad 1: 20 um pitch, 10 um pads
Quad 2: 30 um pitch, 15 um pads
Quad 3: 60 um pitch, 30 um pads
Quad 4: 40 um pitch, 20 um pads

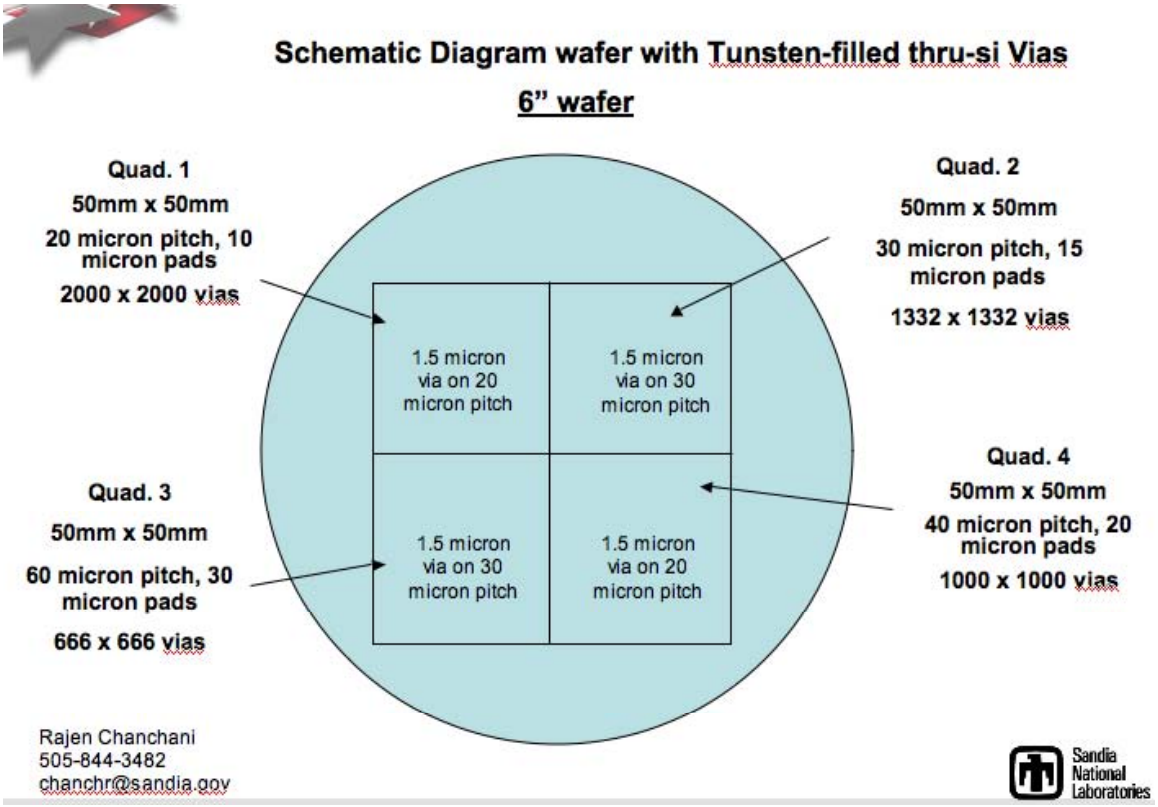


Figure 11. Wafer map with 4 quadrants

The layout work involved design support from TLMI.

A process was designed to allow for attachment of a top and bottom substrate to a via substrate and allow for daisy chain measurements through exposed pads on bottom die. The end result is illustrated in Figure 12.

The process was basically:

1. Pattern/metallize bottom die (50 mm x 50mm) at TLMI on wafer.
2. Indium bump bottom die at TLMI.
3. Use un-thinned Sandia fabricated via wafer with metallization (metallization done at TLMI), dice, and flip chip bond to bottom die.
4. Thin top wafer down to vias.
5. Sandia to metallize top surface pattern.

6. Access to chains between 10 and one million will be available depending on the pitch. See Figure 13.

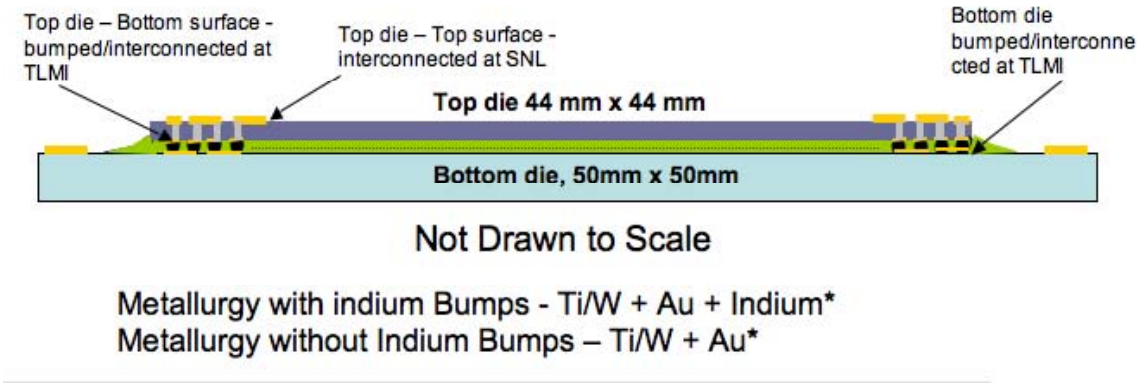


Figure 12. Diagram of desired finished product with interconnected vias.

# of vias in daisy chain	# of Daisy Chains
10	80
100	80
1K	48
10K	40
100K	40
1M	4

Figure 13. Example of connected via daisy chains for 20 um pitch quadrant.

Some assembly was started with the 60 and 40 micron pitched substrates. Some of the needed metalized and flip chip bonded substrates were delivered to Sandia after the end of the program. It is hoped that a small amount of HTS GC LDRD money will be available to continue the assembly process and test a few substrates for continuity and yield.

Summary

The number one significant impact of the work in FY07 was building expertise in arrayed interconnects. Several internal and external customers have a vested interest in the

success of arrayed, through-wafer interconnects (vias). By going through the exercise of designing and fabricating a "system" of pads and interconnects, knowledge was gained in these areas:

1. Tungsten vias.
2. Metallization that will offer continuity to tungsten vias.
3. Indium bumping on various pitches and pad sizes (always a key aspect of developing a successful bonding process).
4. Experience with developing substrates that can be properly aligned.
5. Experience developing a system of interconnects that can be tested.
6. Understanding the difficulties of layout, metallization, fabrication, wafer thinning and order of events.

In an R&D and product realization environment knowledge will save time and money. By truly understanding what is and is not technically difficult, we can save money as we interact with external vendors and create more realistic schedules for them and Sandia. When the HTS GC LDRD completes, some of the success of the final product will be tied back to this work on the OMEMS LDRD.

Resources

External resources (early):

PolarFab (now Jazz Semiconductor)

Jazz Semiconductor
Jamboree Road
Newport Beach, CA 92660-3007
Phone: (949) 435-8000

austriamicrosystems USA, Inc.
5201 Great America Parkway
Suite 320
Santa Clara CA 95054
Phone: (408) 345-1790

Jet Process Corporation
57B Dodge Avenue
North Haven, CT 06473
Phone: (203) 985-6000

Aspen Technologies
5050 List Drive
Colorado Springs, CO 80919
Phone: (719) 592-9100

External resources (later):

TLMI Corporation
2111 W. Braker Lane #500
Austin, TX 78758-4054
Phone: (512) 833-7075

Conclusion

Substantial progress has been made within the key areas of the early program: through-wafer vias, pixel control and drive electronics, MEMS Chip-to-Electronics attachment, optical MEMS array test and characterization, and overall microsystem integration. Additionally, substantial progress was made in the later program in these areas: higher density via fabrication and pad metallization, Indium bumping and bonding.

Center 1700 has established knowledge and capability in each of the above areas and has identified industry resources that can help with product realization in the areas of high voltage electronics, substrate patterning and design, substrate metallization, bump bonding, and die attach.

The program managers and technical contributors were able to maintain flexibility to support changing program needs. The cost of this flexibility was an incomplete OMEMS microsystem demonstration. The benefit was increased knowledge and experience in high density conductive interconnects on thinned wafers, indium bumping, low temperature substrate bonding and design and test considerations for high density, high count two dimensional arrayed substrates.

It is anticipated and expected that this knowledge base and experience will directly benefit the HTS GC LDRD and other Sandia efforts needing high density two dimensional arrayed interconnect technologies.

References

None.

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