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Final Technical Report

Deep Trek
High Temperature Electronics Project

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Abstract

This report summarizes technical progress achieved during the cooperative research agreement between Honeywell and U.S. Department of Energy to develop high-temperature electronics. Objects of this development included Silicon-on-Insulator (SOI) wafer process development for high temperature, supporting design tools and libraries, and high temperature integrated circuit component development including FPGA, EEPROM, high-resolution A-to-D converter, and a precision amplifier.

Contents

1.0 Glossary and Acronyms

AC Specifications	Refers to parameters that define periodic and/or transient performance characteristics (e.g., frequency, transition times, etc.).
A-to-D or ADC	Analog-to-Digital , or Analog to Digital Converter
Atmel	A commercial supplier of integrated circuits, including FPGA's. The High-temperature FPGA design that is used in this project is a fully-licensed high-temperature version of Atmel's AT6010 product.
Behavioral Model	Refers to a structured text-based representation of a design that defines circuit functional behavior using a "Hardware Description Language" (see HDL). A behavioral model may define a design or sub-block in terms of its inputs and outputs, functionality, and timing behavior. Behavioral models describe the design at a high level of abstraction and can be used to quickly capture and simulate operation of major system building blocks.
Cadence	A commercial supplier of integrated circuit development software, including tools for schematic entry, simulation, layout, and layout verification.
Configuration	In this context, refers to the process or data that defines the application-specific functionality of a Field-Programmable Gate Array (FPGA).
CCLK	Configuration CLocK: This is a signal generated within the HTFPGA that is used during the configuration of the device.
CMOS	Complementary Metal Oxide Semiconductor: A term generally applied to integrated circuit processes that use two types of field-effect transistors; employing n-channel (electron) and p-channel (hole) conduction. The n-channel transistors are turned on (conduct) by applying a positive gate voltage (relative to the source terminal), while p-channel transistors are turned on by applying a negative gate voltage.
DC Specifications	Refers to parameters that can be specified in terms of static conditions, without reference to any time dimension (e.g., standby current, static drive current, input/output voltage levels, etc).

1.0 Glossary and Acronyms (Continued)

Die	An individual integrated circuit that has been cut from a silicon wafer (see "Wafers").
DOE	Department Of Energy
EEPROM	Electrically Erasable Programmable Read-Only Memory: A memory device that can be used to store data by electrical means (programming), that retains such data even when power is interrupted, and that can also be erased (and subsequently re-written) by electrical means.
ESD	Electro-Static Discharge
Foundry	A facility providing silicon wafer processing for 3rd party designs. As an adjective describes items that are used to support 3rd party designers (e.g., "foundry toolkit").
FPGA	Field Programmable Gate Array: A digital device (Gate Array) where on-chip connections (and thereby functionality) can be defined and/or altered by the user in the field.
Gate Array	A component or design-style that makes use of predefined transistors and/or logic gate fabricated on silicon wafers where application-specific functionality is defined by the way in which the transistors or logic gates are interconnected.
Gate-level Model	Refers to a representation of a digital design that describes a circuit in terms of logic gates, flip-flops, or latches. Each of these circuit elements has a corresponding transistor-level design and physical layout that can be placed and routed within an integrated circuit.

1.0 Glossary and Acronyms (Continued)

HDL	Hardware Description Language: Refers to one of several standard forms for describing integrated circuit behavior. Specific examples of HDL's are Verilog and VHDL.
HITEC	HIgh Temperature Electronics Conference: A bi-annual conference sponsored by IMAPS, held in the United States.
HITEN	HIgh Temperature Electronics Network: A consortium of academic and industrial entities promoting research and development of high-temperature electronics. Also the name of a bi-annual European conference.
HT2000 or HT2K	Refers to Honeywell's "High Temperature 2000" family of gate array products and/or design tools.
HTEEPROM	High Temperature EEPROM (see EEPROM)
HTFPGA	High Temperature FPGA (see FPGA)
HTSOI	High-Temperature Silicon-On-Insulator: An SOI integrated circuit manufacturing process that is optimized for extreme temperature applications (see SOI)
HTSRAM	High Temperature SRAM (see SRAM)
HW	Honeywell
IC	Integrated Circuit
I/O	Input/Output
IMAPS	International Microelectronics And Packaging Society (www.imaps.org). IMAPS sponsors high-temperature electronics conferences (HiTEC and HiTEN).
IP	Intellectual Property: Frequently used to refer to designs and/or licenses that are procured for implementation.

1.0 Glossary and Acronyms (Continued)

Masks	See "Photo-masks"
Mentor	A software company that provides design automation software for the electronics industry
NETL	National Energy Technology Laboratory – A division of the U.S. Department of Energy
Non-volatile	In this context refers to a memory element or circuit that retains data content even if power is interrupted.
PDK	Process Design Kit: Terminology employed by Cadence, Inc. In this context refers to a structured collection of process and design information specific to an integrated circuit foundry that enables usage of Cadence tools to develop designs targeted to that foundry.
PGA	Pin-Grid Array: Refers to an integrated circuit package which is constructed such that signals are presented in a 2-dimensional array of pins that project from the package body. The pins can be inserted through holes on a board-level assembly.
Photo-masks	This is generally synonymous with "masks" (Sometimes also referred to as a "reticle"). A photo-mask is a glass plate with patterns that are transferred to silicon during wafer processing by shining ultra-violet light through the photo-mask onto a silicon wafer that has been pre-treated with light-sensitive coatings. Up to 27 different photo-masks may be involved in processing a single integrated circuit as described within this report.
RTL	Register Transfer Level: Refers to a means of capturing the behavior of a digital integrated circuit in terms of the data that is stored in data registers. Such a description is like a state-machine where the state changes with each clock cycle. Data is transferred between on-chip registers synchronously using one or more system clocks. An RTL description defines the registers, and how their contents are determined from one clock cycle to the next.

1.0 Glossary and Acronyms (Continued)

SRAM	Static Random Access Memory: A memory device in which data is stored at specific addresses where these addresses can be accesses in any sequence (i.e., randomly) by forcing address input bits to the desired state. A "static" memory means that a clock does not have to be running in order for the device to retain data (as opposed to a Dynamic Random Access Memory, or DRAM, which requires a clock or a minimum operating speed to function properly).
SOI	Silicon On Insulator: An integrated circuit device structure where all the transistors/devices are individually isolated by a silicon dioxide insulating layer as opposed to silicon p-n junction isolation.
SOPO	Statement Of Project Objectives: The section in DOE's agreement with Honeywell that defines the tasks to be completed on the program.
SPI	Serial Peripheral Interface: Refers to a commonly used protocol that establishes means for serial data communication between a master and multiple slave devices.
SPICE	A generic name for a variety of commercially available circuit simulation programs. Electrical behavior is modeled at the device level (i.e., circuit elements are transistors, resistors, capacitors, etc.)
SRAM	Static Random Access Memory. Refers to a data memory circuit where the data can be randomly accessed by means of the data "address" inputs. "Static" refers to the fact that the memory retains data as long as power is applied without any requirement for periodic "refreshing" (i.e., re-writing) the data.
Synthesis	In this context, synthesis refers to the process of creating a Gate-level Model of a design that is functionally equivalent to a Behavioral or Register-Transfer-Level (RTL) representation of that design.
TBD	To Be Determined

1.0 Glossary and Acronyms (Continued)

Volatile	In this context, refers to memory or a circuit that can store data as long as power is applied, but where that data is lost if power is interrupted.
Wafers	Specially prepared sections of single-crystal silicon that are processed to produce integrated circuits. Wafers on this program have a 6-inch diameter and are approximately 675 microns thick. Many individual integrated circuits are produced on a wafer and these are cut apart at the completion of wafer processing.
WBS	Work Breakdown Structure

2.0 Executive Summary

The DeepTrek High-temperature Electronics project was completed to improve the economics for deep oil and gas exploration and production by developing extended high-temperature electronic technology and components that can be used in used in down-hole drilling tools and processes. Reliable high-temperature performance (up to 225°C, ambient) is a requirement due to the extreme temperatures encountered in deep wells. Objectives of this program focused on two aspects of high-temperature electronics development:

1. High-temperature Electronics Manufacturing Technology and Design Toolkits
   - Integrated Circuit (IC) wafer fabrication technology and design platforms (simulation and IC layout tools and libraries)
2. High-temperature Electronics Component Development, specifically
   - EEPROM (Electrically-Erasable Programmable Read-Only Memory)
   - FPGA (Field Programmable Gate Array)
   - Dual Precision Amplifier
   - High-resolution Analog-to-Digital (A-to-D) Converter

This project began in October 2003 and continued through July 2007. All of the program tasks in the final Statement of Project Objectives have been completed. The program objectives have been achieved, in that the technology is accessible for commercial development and the components positioned for market introduction.

A Silicon-On-Insulator (SOI) CMOS wafer process, optimized for high-temperature operation has been established as a production-level process. This technology is therefore ready for use by Honeywell to fabricate high-temperature products developed by Honeywell. It is also ready to offer on a wafer-foundry basis for wafer fabrication of 3rd party designs.

High-temperature design toolkits and libraries have been put in place to support IC design of products targeted for fabrication in the HTSOI4 wafer process. This includes design infrastructure for gate-array designs with a capacity for up to 275K user-gates on a single chip. It also includes design tools for full-custom design and layout, including schematic capture, layout, pre-layout and post-layout design simulation, and layout verification. User manuals and guides are available for use by 3rd party designers who want to develop products targeted for fabrication using the high-temperature HTSOI4 process flow.

High-temperature EEPROM technology has been developed and demonstrated at 250°C. This includes demonstration of capability for programming and reading at high temperature, verification of high-temperature data retention, and characterization of data-cycling. This has all been accomplished on using the production technology put in place on this program and has culminated in the design and fabrication of a complete 32K x 8 bit EEPROM that is configurable for serial data interface or parallel data interface, incorporating all of the features and functionality of industry standard architectures. When introduced to the market, this will be first in the world commercial non-volatile memory for applications above 200°C.

A High-temperature Field-Programmable Gate Array (FPGA) has been designed, fabricated and comprehensively tested. FPGAs are alternative to dedicated hardware designs where low up-front costs and/or fast-turn development are requirements. FPGA's allow users to define functionality of individual hardware units after it has been delivered by the manufacturer or even

it is assembled into a board or deployed in an application. This high-temperature FPGA is a fully licensed functional equivalent to a standard-temperature commercial product, the AT6010 FPGA manufactured by Atmel. The FPGA provides 30,000 programmable logic gates.

The high-temperature FPGA configuration is based on embedded blocks of logic that are programmed by writing configuration data into on-chip memory. Configuration is typically performed on power-up and is controlled by dedicated configuration pins and dual-function pins that double as user I/O pins when the device is in operation. The high-temperature EEPROM developed on this program has been designed to serve as a non-volatile memory device that can be used to configure the FPGA. The HTFPGA can be re-programmed indefinitely. The HTFPGA can be partially reconfigured while in operation; portions of the device not being modified remain operational during reconfiguration.

A high-resolution Analog-to-Digital (A-to-D) converter has been developed that captures data in digital format for subsequent digital signal processing. This allows digitization of low-frequency signals at a level of resolution that has not previously been achieved at temperatures above 200°C. It is a full-featured complete A-to-D converter, incorporating all required clocks, references, digital filtering and a standard serial data interface and control. It also provides on-chip temperature measurement and digital output using an auxiliary 8-bit A-to-D converter. This represents a level of features, functionality and performance that is unprecedented in a single-chip A-to-D converter at high temperature.

A high-temperature Dual[1] Precision Amplifier has been developed and fully characterized. Amplifiers are needed for down-hole oil and gas data acquisition, especially for buffering high-impedance sensors. When used in high-resolution data acquisition systems, low input offset current, very low offset voltage and good low-frequency noise response are primary considerations. The dual high-temperature precision amplifier offers very low input offset voltage (typically less than 10 micro-volts) and drift, and low noise performance (5 micro-volts peak-to-peak from 0.1 to 10 Hz.) This makes this amplifier suitable for input conditioning for high-resolution DC or low-frequency applications. This amplifier has been demonstrated functionality at temperatures up to 375°C, and sustained operation for hundreds of hours at 300°C

Integrated circuit development under this program is complete. All that remains are some incremental manufacturing readiness tasks (such as package and test development) before all of these components become commercially available for the oil and gas industry.

[1] "Dual" means that there are two complete amplifiers on this integrated circuit component.

3.0 References

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4.0 Project Objectives

Electronics are widely used in modern oil and gas exploration to collect, log and/or process data such as heading and inclination, weight on the bit, vibration, seismic/acoustic response, temperature, pressure, radiation and resistivity of the strata. Drilling time and costs escalate when the target reservoir is very deep. The biggest obstacle for electronic data acquisition systems in deep wells is the high temperature (>170°C, 337°F) encountered at great depth. Commercial electronics are not designed for these temperatures, and conventional integrated circuit (IC) technology is not capable of operating at these temperatures. Reliable high-temperature performance (up to 225°C, ambient) is a requirement due to the extreme temperatures encountered in deep wells.

To help overcome this limitation, this DeepTrek High-temperature Electronics project was undertaken (starting in October 2003) to improve the economics for deep oil and gas exploration and production.

The first objective of the project was to establish production-level integrated circuit (IC) manufacturing technology along with IC design tools (software and simulation elements) to meet requirements for the design and manufacture of IC components capable for reliable, high-temperature operation. Pre-existing technology was insufficiently developed to provide the simulation fidelity and manufacturing repeatability necessary to ensure successful IC product development.

The second objective was to employ the high-temperature technology platform to develop specific high-temperature IC components that were considered urgently needed for down-hole applications.

Specific objectives, such as technology features and IC components chosen for development, were adjusted over the course of this development. Technical guidance (and financial support) has been provided by a Joint Industrial Participation (JIP) consortium. JIP member companies have been BP, Baker Hughes, Goodrich Aerospace, Halliburton (through 2005), Honeywell, IntelliServ, Quartzdyne, and Schlumberger. For example the original project plan called for the development of two different IC technology platforms, one with a 0.8 micron minimum transistor dimension for operation at 5-volts and a second process with 0.35 micron minimum transistor dimension for operation at 3.3V. Based on JIP direction the latter technology platform development was stopped early in the program (March 2004). These adjustments, along with others in the statement of project objectives, were made at that time in order to focus on the components that were determined by JIP consensus to have the highest priority for development. These changes were captured in a revision to the Statement of Project Objectives (SOPO) dated March 23, 2004.

As a result, four high-temperature integrated circuit components were targeted for development.

EEPROM (Electrically Erasable Programmable Read-only Memory)
FPGA (Field Programmable Gate Array)
Dual Precision Amplifier
High-resolution (18-bit) Analog-to-Digital (A-to-D) Converter

These components have remained the focus for development from March, 2004 through the end of the program. The program vision was that all of these components should be

commercially available at the conclusion of the program. Therefore the adjusted scope in the Statement of Project Objectives contained provisions in the work breakdown structure (WBS) for tasks not only to develop and demonstrate these functions, but also to develop product documentation, test and screening procedures, reliability assurance, and so on in order to achieve full commercialization of these designs.

There were two additional SOPO revisions during the course of the program (September 2, 2005 and February 8, 2007). These SOPO revisions were required as it became clear that the program would not have sufficient budget to achieve full commercialization of all four components. These subsequent revisions adjusted scope according to the interim progress and consensus priorities of the JIP partners. In general these changes prioritized product design and fabrication of the targeted components over testing and commercialization tasks to the extent that keeping within the budget required. This strategy presumes that successful design and fabrication would ultimately lead to commercial availability based on a valid commercial requirement for these components.

5.0 Technical Approach

The overall technical approach for this project has been described over the various phases of the program by the Statement of Project Objectives (SOPO) which forms part of the cooperative research agreement between U.S. DOE and Honeywell.

5.1 Technology Development

The original Statement of Project Objectives (SOPO) included completing development and taking to production status two separate and distinct IC manufacturing process flows (wafer processes). These were a 5-volt process featuring 0.8 micron minimum transistor dimensions (referred to herein as the HTSOI4 process) and also a 3.3-volt process featuring 0.35 micron transistor dimensions. Early in the program the industrial partners in the JIP re-aligned the program priorities, embodied in a SOPO revision on March 23, 2004. With this revision the 0.35 micron wafer process was removed, leaving the HTSOI4 process in the program. In addition to developing the HTSOI4 wafer process flow, the program objectives included modifying and/or creating tools and processes for the creation and verification of integrated circuit designs targeted to the HTSOI4 technology.

5.1.1 Wafer Process

It is well known that Silicon-on-Insulator (SOI) CMOS is a viable alternative to bulk CMOS technology for high temperature, primarily due to improved device-to-device isolation and reduced high-temperature leakage. Although junction leakage is reduced by SOI, sub-threshold leakage in low-voltage SOI processes may render them unusable for extreme high temperature because of unacceptably high standby current.

Therefore, some tailoring of the process for extreme temperature applications is needed, especially for very large digital circuits (memory, microprocessors, etc.).

The Deep Trek program took the approach of upgrading to production status a High-Temperature SOI (HTSOI) process developed by making relatively minor but critical changes to an SOI production-level process that had been developed for high-reliability aerospace applications [3, 4]. This allowed the program to take advantage of years of production experience and yield improvements achieved over the life of the parent process. The main steps undertaken to optimize the process for high-temperature were:

(1) Removal of process steps required for military and space applications but not required for commercial high-temperature,

(2) Re-targeting the threshold voltage implants to address sub-threshold leakage and render the technology functionally useful up to 300°C

Much of the preliminary effort to establish the HTSOI4 process was accomplished before the program began. However much of this early work was accomplished using equipment and operating procedures that had changed since the initial development. Under the DeepTrek program, a Device Characterization Test Chip (DCTC) was used to fabricate multiple wafer lots. Test structures (transistors, resistors, capacitors, diodes, etc.) on the DCTC were tested and characterized to re-qualify the process technology and to provide data on manufacturing variations, temperature characteristics, etc. The DCTC wafer runs were also used to provide material for modeling to support simulation.

An abbreviated outline of the wafer process development plan follows:

1. Device Characterization Test Chip (DCTC) Fabrication: Three wafer lots.
2. DCTC Device Testing and Report
3. High Temperature Simulation Modeling (SPICE models):
   a. Models developed for Cadence SPECTRE simulator
   b. Temperature range for the models is -55C to 250C (junction temp).
   c. Models extracted for NMOS, PMOS, NDMOS and PDMOS devices, including noise parameters.
   d. Models extracted for NDMOS and PDMOS (extended drain device) devices.
   e. Fixed-geometry models developed for the ESD protection diode.
   f. Fixed-geometry models developed for the lateral PNP (for DC applications only).
   g. Models developed for resistors and capacitors.
   h. Parameters extracted from device measurements used to generate a "typical" model.
   d. Statistical variations from Process Monitor (PM) testing used to create "process corner" models.
4. Technology Reliability Assessment
   a. Data Review & Qualification Plan Development
   b. Qualification Hardware and Software Development
   c. HT SOI4 Technology Qualification Test, Review Data
5. HTSOI4 Mixed Signal Cell Benchmark Evaluation: Establish that the wafer process, layout rules, SPICE models, etc. are capable for developing mixed-signal circuits up to 225C ambient (250C junction) by testing circuits carried on the Device Characterization Test Chip (DCTC) and comparing results to simulation.
   a. Evaluation Planning

b. Schematic entry and simulation.

c. Hardware/Software development.

d. Wafer probe evaluation, sample assembly, and temperature testing

e. DCTC Circuit Evaluation Report

6. Wafer process production upgrade reviews and documentation.

5.1.2 Design Libraries and Toolkits

A criterion for wafer process development was to retain HTSOI4 layout-rule and photo-mask compatibility with Honeywell's military-aerospace technology out of which the HTSOI4 process flow was derived. This allowed the program to take advantage of previously developed digital ASIC design platforms and other design tools

Pre-existing SOI ASIC infrastructure included fully supported pad frames, under-layers, probe cards and packages that are available for the high-temp community to support new analog, digital and mixed signal chip ASIC designs.

Different design flows may be used in the implementation of a high-temperature IC; one design path analog (or full-custom digital) blocks and a separate path for digital logic functions (i.e., digital circuitry implemented from pre-defined structures implementing logic functions such as AND, OR, and NOT as well as clocked storage elements such as data registers). Purely analog (or full-custom digital) blocks are implemented using traditional analog tools and processes, including transistor-level schematic entry and SPICE-based simulation methodologies. This is done using a Process Design Kit (PDK) which is an integrated collection of schematic capture symbols, models, layout rules, and other items to allow use of design software available from Cadence (a commercial IC design software vendor). Cadence Virtuoso® Schematic Editor is used for schematic entry. Cadence Spectre® and Ultrasim® are used for analog core simulation. Cadence tools are also used for analog core layout, parasitic extraction, merging analog and digital layout databases and for layout verification.

Meanwhile, purely digital blocks use conventional digital Hardware-Description-Language (HDL) based development tools and flows. Many HDL simulation tools are commercially available for functional and timing simulation of the synthesized blocks. Functional blocks defined in an HDL netlist can be physically placed and routed using the pre-existing Gate-array toolkit and platforms. Post-route timing analysis and design verification tools are available to ensure that the final design faithfully implements the functionality initially captured in the HDL functional viewpoint.

For ASICs implementing a mix of analog and digital blocks, two parallel and concurrent design paths may converge during mixed mode simulation of the entire chip and again during layout of the complete mixed signal ASIC. Designs are implemented in a hierarchical manner. In order to simplify the simulation and back-end tool flows, the analog and digital sub-modules of mixed signal ASIC designs are segregated into separate sub-modules and are inserted into the chip top-level netlist. Interconnection of the analog and digital cores may be verified by the Cadence AMS Designer simulator or other mixed mode simulation tools. Physical layouts of the analog and digital sections are merged to construct the final top-level chip layout.

The complete design can consist of a number of component blocks including an analog core, embedded custom SRAM, digital sub-blocks, I/O and top-level interconnect blocks. It may also include design for test features such as digital scan chain (inserted by software to enable Automated Test Pattern Generation, ATPG).

In addition to supporting 3rd party software from a variety of design synthesis and simulation tool vendors, the design flow also incorporates proprietary software (i.e., specific to Honeywell's ASIC family) that check for loading violations, violations of electro-migration current density rules (limits are tailored specifically for high-temperature use), digital edge-rate violations, I/O placement errors, etc. The supported vendor tools help maintain highest design quality and help ensure an error free design.

In summary, the DeepTrek program approach to IC design creation and verification used previously developed design processes and toolkits and adapted these for high-temperature applications. This involved extending the applicable range for high-fidelity simulation (by modeling and characterization) up to 250°C. In addition, verification parameters and other data used in conjunction with the design tools were adjusted so that design checking would be modified in accordance with high-temperature requirements. These include parameters involved with timing and also parameters to ensure interconnect reliability by conformance to high-temperature electro-migration rules[2]

5.2 Component Development

The original Statement of Project Objectives (SOPO) called for the development of a set high-temperature IC components including: (1) a 16-bit micro-controller core based on the Intel 80186 instruction set; (2) a Filed-Programmable Gate Array; (3) a precision amplifier; (4) an A-to-D converter targeting 16-bit resolution. The original SOPO also included development of a board-level demonstration system incorporating all of the components.

Early in the program the JIP partners directed changes to this original set of components, and these changes were embodied in the March 2004 revised SOPO. The primary reason for these changes was the JIP consensus that the first priority for components should be the development of a non-volatile memory, taking the form of a high-temperature EEPROM. To establish a budget for the EEPROM development the 16-bit micro-controller core and the board-level demonstration were removed from the program.

5.2.1 EEPROM

High-temperature non-volatile memory was considered essential to the program due to the complete lack of programmable memory devices with specified operation above 175°C. An additional consideration was the fact that the Field-Programmable Gate Array targeted for development relies for configuration on data down-loaded from another device, typically in the form of non-volatile memory. Therefore the FPGA would be of little value if non-volatile memory were not available. The data in the non-volatile memory programs the connectivity, and therefore the functionality, of the FPGA.

[2] Electro-migration (EM) is a phenomenon whereby the metal in on-chip interconnections may move in the direction of electron flow. This occurs over time and is a strong function of current density in the conductors and also is a strong function of operating temperature. If not properly handled this can result in opens and shorts due to metal migration.

After a short feasibility study, it was decided that the non-volatile memory should take the form of an Electrically-Erasable Read-Only Memory (EEPROM) as opposed to alternatives such as one-time programmable memories using fusing or anti-fusing approaches for programming. The EEPROM planned to use a memory cell programmed to a logic "1" or logic "0" by injecting or removing charge onto the floating gate terminal of a transistor. This process, referred to as Fowler-Nordheim tunneling, involves passing current through a thin-oxide. The oxide is normally non-conductive. Current is passed through the oxide by the application of voltages higher than those used in normal operation.

This approach represented additional technology challenges because gate-current conduction involved in Fowler-Nordheim (F-N) tunneling is a non-standard operation and is not supported by computer simulation models. In addition, creating the conditions for F-N tunneling requires applying voltages to the memory cells that are above the normal operating voltage of the HTSOI4 devices. This required the application of new device layout techniques for extended-drain transistors that could apply (and withstand) the high-voltages to the devices being programmed.

Finally, the ability to store charge (and hence data) for a useful time period is significantly compromised by high-temperatures (charge tends to leak off at a much faster rate when the device is hot).

The development plan to address these issues included the use of design consultants with expertise in EEPROM development. In addition, empirical methods were employed to assess options for memory cell construction, to characterize the programming mechanism, and to determine whether the wafer process would prove capable for the requirements.

Assessing the need for FPGA programming as well as for other applications it was determined that EEPROM development targets would include:

Memory Size
- GOAL: 32K by 8
- MINIMUM: 17K by 8

Features
- Read and write over full temperature range
- Parallel interface (required for ease-of-use with the FPGA)
- On-chip high-voltage generation for project/erase (with external caps)

Temperature:
- -55C to 225C ambient

Speed:
- Read access: 50 nsec (goal)
- Write time: To Be Determined (Not critical)

Data Retention at 250C (junction)
- GOAL: >2000 hours (83 days)
- MINIMUM: 1000 hours (42 days)

Endurance
- GOAL: >10000 program-erase cycles
- MINIMUM: >1000 program-erase cycles

An abbreviated outline of the development plan included:

1. Assess trade-offs, develop technical approach and product goals
2. Design/conduct experiments on selected wafer process adjustments
3. Design, fabricate and evaluate a test chip for the purposes of individual memory cell optimization and initial data-retention testing. Process multiple lots in order to assess various process adjustments that could enhance high-temperature data retention.
4. Design, fabricate and characterize a test chip for the purposes of demonstrating an array of memory cells along with the means to address individual cells for read/write access without disturbing adjacent data. Also optimize waveforms for programming/erasing memory cells and assess data retention and data-cycling.
5. Design, fabricate and characterize a first-pass product configuration, including development of custom packages and product test software.
6. Design, fabricate and characterize a second pass product configuration, as required.

5.2.2 FPGA

Low-volume digital applications are often addressed by the use of programmable logic devices. A subset of this category of products is a Field-Programmable Gate Array (FPGA). An FPGA contains logic gates where the internal connectivity (and thereby the functionality) of the unit is programmable.

The DeepTrek FPGA goal was to develop a functional equivalent to a commercial FPGA, the Atmel AT6010. It is a re-programmable, FPGA that contains the equivalent of 32,000 programmable logic gates and 204 programmable inputs/outputs. It is configured (programmed) by loading data into SRAM that is distributed across the die. This has the advantage that it can be re-programmed any number of times, but the disadvantage that the configuration memory is volatile, meaning that the configuration is lost when power is interrupted. Therefore an external means for storing the configuration data is required. Configuration memory is typically provided by an external non-volatile device such as an EEPROM. Configuration data can be loaded into the FPGA on power-up.

The Atmel AT6010 architecture was chosen because Honeywell had a pre-existing licensing agreement with Atmel (for aerospace/defense applications) that is applicable for a commercial high-temperature product. Honeywell also had previously implemented and verified this architecture in a 0.35 micron SOI wafer process flow.

The initial design approach was to modify (simplify) the prior design and fabricate the FPGA in a high-temperature version of the 0.35 micron process. However, the development for the high-temperature 0.35 micron process was removed from the program to allow for the EEPROM development. However, it was determined that the objective design could be implemented in the 0.8 micron HTSOI4 process flow. The cost of this change in direction is a much larger die size due to the larger transistors (and other devices) in the HTSOI4 process relative to the 0.35 micron SOI implementation. This is a relatively large design. The military/aerospace design in 0.35 micron technology employed over 8-million devices and hundreds of chip-level I/O.

The design methodology followed the previously successfully implementation at Honeywell. This involved creating a functional equivalent design to the AT6010 based

on transistor-level schematics obtained from Atmel. Note that the schematics and simulation did not employ the Cadence PDK tools developed within this project. Instead design tools from Mentor Graphics were used, along with device models extracted for the HTSOI4 technology within this project. This approach was employed to take advantage of the experience Honeywell staff involved with the FPGA had with the Mentor design tools. The same personnel had used these tools to successfully design the 0.35 micron FPGA implemented by Honeywell prior to the start of this program.

An abbreviated outline of the revised development plan included:

1. Planning and specification, including assessment of feasibility and project performance, as well as approaches for design simplification and die-size management.
2. Preliminary design included schematic capture and simulation using HTSOI4 design tools.
3. Physical layout and analysis of layout impacts on design performance.
4. Photo-mask and wafer fabrication.
5. Development of test hardware and software, and characterization of performance at high temperature
6. Development of a custom package.
7. Completion of a second-pass design, fabrication, and test sequence (as required).

5.2.3 High Resolution A-to-D Converter

Prior to the DeepTrek program there were no viable high-resolution A-to-D converters (16-bits or more) capable of high-temperature operation. The maximum resolution achieved above 200°C was about 14 bits for partial and/or multi-chip (rather than single-chip) implementations. The original Statement of Project Objectives (SOPO) for the DeepTrek program called for the development of a high-temperature single-chip A-to-D converter with 16-bits of resolution. The JIP group consensus was to ask Honeywell to attempt to achieve an even higher resolution. The revised SOPO dated March 2004 called for development of a single-chip, complete A-to-D converter targeting the following performance and features:

- 18-bit A-to-D converter in a 24 pin dual in-line package (DIP) - later changed to 28-pin DIP.
- 2nd Order Sigma-Delta Architecture[3]
- 100Hz Update Rate with TBD Clock
- -55 °C to 225°C Ambient Operating Range (reduced accuracy below 0 °C)
- Fully Differential Input and Reference
- 1-bit Modulated Data Output and Input Supports Test and Off-Chip Digital Filters
- Data transfer and configuration control using 3-wire Serial Peripheral Interface (SPI)

[3] For a technical description of this type of design architecture refer to Boser and Wooley [5].

- Single Pin Clock Selection (Internal Oscillator or External Clock)
- On-Chip 2.5 V Precision Voltage Reference
- PTAT (Proportional To Absolute Temperature) Current Source Output
- Coarse Temperature Measurement (~ 1.4 °C resolution) via Built-In ADC
- Single Supply 5 V Operation
- 5mA Maximum Supply Current
- Low Current Sleep State When Not Performing A-to-D Conversion
- Over range Indication

Second-order sigma delta architecture with a single-bit output was chosen for its unconditional stability and to ease implementation of on-chip digital filtering.

A mixed analog/digital implementation using the HT2000 framework was planned. That requires partitioning the design into analog and digital sections. The digital section would be designed as Register-Transfer-Level (RTL) behavioral HDL code and simulated using HDL functional simulators. After functional verification the digital section would be synthesized into the HT2000 digital library and completed per the HT2000 digital design flow. A full-custom device-level design flow using the Cadence PDK toolkit was planned for the analog section. The two sections would be combined at the chip level and implemented within an HT2000 I/O ring. Note that this implementation plan exercises all of major design library and toolkit functionality developed per the design library and toolkit portion of the technology development effort within this program.

At Honeywell's suggestion, personnel at Oak Ridge National Laboratories were engaged by DOE to perform some of this work, based on demonstrated expertise in the design and testing of high-temperature sigma-delta modulators and associated digital filtering functions [6]. All of the other design and layout tasks were assigned to Honeywell staff.

An abbreviated outline of the development plan included:

1. Creation of a design architecture specification; partitioning the design into analog and digital blocks (and sub-blocks) and defining all interfaces. This also includes defining design for test approaches and test interfaces. It also includes defining power-supply connectivity for analog and digital blocks as well as input/output structures
2. Preliminary design; schematic capture and simulation of analog blocks, and register-transfer-level (RTL) functional design and simulation of digital blocks, culminating in preliminary design reviews
3. Finalizing analog core design and creating physical layout of all analog blocks.
4. Chip-level physical floor-planning, including assignment of all input/output locations and power-supply routing.
5. Synthesis of gate-level netlists of the digital sections, implementation of design for test features such as scan-path insertion, and simulation to verify equivalence with RTL-level behavioral netlists and to create functional test vectors and Automated-Test-Pattern-Generated (ATPG) test vectors.

6. Completion of digital section place and route, insertion of routing delays into the simulation data base, and post-route timing analysis and simulation to verify equivalence of pre-route and post-route design databases.
7. Completion of chip-level layout verification, including verification of analog/digital interface connectivity by chip-level simulation.
8. Completion of final design reviews and associated actions, followed by design release for fabrication.
9. Procurement of photo masks and wafer fabrication.
10. Package design and procurement
11. Test hardware and software development
12. Characterization testing.
13. Completion a second pass cycle of design, fabrication and testing (as required).

5.2.4 Dual Precision Amplifier

Signal conditioning amplifiers are needed in down-hole oil and gas data acquisition tools, especially for buffering high-impedance sensor outputs. Many applications involve DC-coupled sensors. When used in high-resolution data acquisition systems, low input offset current, very low offset voltage and good low-frequency noise response are primary considerations. For the DeepTrek program, a first application of the amplifier is to amplify and buffer sensor inputs and reference inputs to the A-to-D converter.

Features and performance targets for a Precision Amplifier were identified in the March, 2004 Statement of Project Objectives as follows:

- -55°C to 225°C Ambient Operating Temperature Range
- Continuous Input Offset Auto-Zeroing With Internal Clock
- No External Capacitors Required
- Input Offset Voltage ±100 micro-volts Max Over Temperature
- Input Offset Drift 0.2 micro-volts/°C Max
- Input Range Includes Lower Supply Rail
- Output Swings Rail to Rail
- High Gain, CMRR, PSRR: 100dB Min
- Gain-Bandwidth Product: 1.5MHz
- Single 5V Supply Operation
- Sink and source 25mA
- 2mA Maximum Supply Current/Amplifier

Given the nature of the design, it was natural to develop the amplifier using a full-custom design style. The development of this circuit provided the first opportunity to utilize the upgraded wafer process technology and full-custom design toolkit developed early in the program.

An abbreviated outline of the development plan included:

1. Specification development
2. First pass design, layout and wafer fabrication
3. Package design and procurement
4. Test hardware and software development
5. Wafer saw, assembly, and characterization testing
6. Second pass sequence of design, fabrication, assembly and testing (as required).

6.0 Results and Discussion

All of the tasks contained within the final Statement of Project Objectives have been completed, in accordance with development plans laid out within first amended SOPO (March, 2004).

6.1 Discontinued Tasks

Several tasks were initiated with the program award in October 2003 (in accordance with the original Statement of Project Objectives (SOPO) but discontinued with the SOPO revision of March 23, 2004. These tasks included: (1) initial feasibility assessment and pilot wafer processing for a high-temperature 0.35 micron wafer process; and (2) planning and specification activity associated with 16-bit micro-controller development that was not pursued.

6.2 Technology Development

The technology development objectives of the program have been achieved. Results have been reported at high-temperature electronics industrial conferences. See appendices 1 and 2 for additional descriptions of the technology development and outcomes.

6.2.1 Wafer Process

Under the Deep Trek electronics program the HTSOI process has been fully re-characterized at the device level. This included running multiple wafer-lots containing device-level characterization structures so that statistical process variation is established. Screening tests for wafer-lot acceptance have been developed. The wafer process is defined and controlled by extensive documentation at Honeywell, including wafer process specifications, operating procedures, layout rules, and electrical rules, and simulation models for computer aided design (SPICE models). The technology was upgraded to production status by action of Honeywell's Technology review board in January, 2005. Outcomes from the DeepTrek process qualification and upgrade activities included tailored final wafer acceptance screening (to ensure reliable high-temperature operation), and process adjustments to extend the transistor maximum voltage ratings and provide additional operating margin.

This was accomplished by executing the wafer process elements of the development plan as previously described. Note that the design and evaluation reports for the Device Characterization Test Chip were delivered to DOE under this program.

As a result of this outcome, Honeywell is able to use this wafer process technology for the manufacture of High-temperature electronic components. Honeywell can now also provide information and support to other companies (after execution of propriety non-disclosure agreements) and offer access to this technology on a foundry basis so that

other companies can manufacture their proprietary designs using Honeywell's high-temperature HTSOI4 wafer process.

6.2.2 Design Libraries and Toolkits

Honeywell has also successfully developed and demonstrated design libraries and toolkits that support analog, digital, and mixed analog/digital IC design. This development activity and the resulting capability are presented in Appendix 2.

Full-custom designs are supported utilizing Cadence design and layout software in conjunction with Honeywell's HTSOI4 Cadence PDK kit. This design kit is available to Honeywell staff. Other companies wishing develop their own proprietary designs may also receive the HTSOI4 Cadence PDK tool kit (after execution of proprietary non-disclosure agreements).

Honeywell and other parties can use the HT2000 Data Book, the VDS-V User's Manual and Honeywell's VDS-V digital ASIC toolkit to develop high-temperature digital ASIC's using Honeywell's family of HT2000 gate arrays. This design process is described in detail in Honeywell's VDS-V user's manual, while characteristics and design considerations specific to High-temperature and the HT2000 gate arrays are described in detail in the HT2000 Databook [2].

Note that during the course of this program the Cadence PDK toolkit was used extensively in the development of the Dual Precision amplifier, and the HTEEPROM. Full-mixed signal capability utilizing both the HT2000 design platform and toolkit and the Cadence PDK toolkit has been proven in conjunction with the A-to-D design.

6.3 Component Development

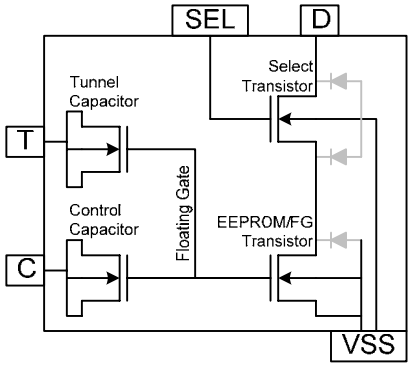
All of the components targeted for development have been designed and fabricated. The FGPA and Dual Precision Amplifier have comprehensively tested and proven to be successful within a single design/fabrication cycle. Two design cycles have been completed on the A-to-D product design, which has been functionally verified. As for the EEPROM, non-volatile memory capability has been established by fabrication and characterization of test chips test-chips. This has been followed by design and fabrication of a complete 32K by 8 bit EEPROM product design.

These outcomes have been reported at high-temperature electronics industrial conferences. See appendices 3 and 6 for additional information on component development and outcomes.

6.3.1 EEPROM

The EEPROM component development was the single largest element of this program, consuming approximately 35% of the budget. The EEPROM that was developed is based upon a floating gate memory cell (see Figure 1) where the memory state is defined by adding or removing charge place on the gate terminal of a transistor by passing current through the normally non-conducting gate-oxide layer. This floating gate is otherwise not electrically connected to any other device. Current through the gate oxide is induced by applying voltage of the appropriate polarity across the gate oxide. These voltages are always more than those voltage used in normal transistor operation. When the voltage magnitude is properly chosen, then the gate oxide will

conduct current without significantly changing its non-conductive quality over the normal range of operation. This means of passing current through a thin gate-oxide layer is known as Fowler-Nordheim (F-N) tunneling. If the voltage is too high, then the transistor gate oxide will be permanently damaged. Therefore it is critical to understand and characterize the Fowler-Nordheim tunneling current characteristics.



- **Charge is added or removed from the floating gate by Fowler-Nordheim tunneling through the tunneling capacitor oxide (voltage applied to terminals "T" and "C"**
- **Net effect is an apparent threshold voltage shift in the EEPROM transistor**
- **Memory cell is read by turning on the EEPROM transistor by capacitive coupling using the Control Capacitor**
- **Drain current is sensed to detect the difference between a "programmed" cell (stored 1) and an "erased" cell (stored 0)**

Figure 1: Single-poly Floating Gate Memory Cell

Note that the data that is stored in the memory cell depends on retaining the charge stored on the floating transistor gate. This charge will eventually leak away and the data will be lost. This leakage, and hence the data retention capability of the cell, is a strong function of temperature (leakage increases at high temperature). It is therefore critical to also understand the data-retention characteristics of the bit cell.

Finally, the capability for passing current through the gate-oxide by F-N tunneling is degraded as charge is repetitively added and removed from the gate. This limits the "durability" of the memory cell, or the number of times that it can be cycled between storing logic-state "1" to storing logic-state "0.

Commercial vendors that use F-N tunneling to manufacture conventional-temperature EEPROM's in large volumes generally optimize the wafer process flow to include special features specifically for the sake of optimizing tunneling characteristics for their particular device and process topologies. In the case of this project, that was not an option due to the cost that would be involved for developing and sustaining a process flow given the program budget and low-volume production rates for a high-temperature product.

No prior characterization F-N tunneling characteristics, data-retention, or durability had been done in the high-temperature SOI technology used in this program (or for any SOI technology manufactured by Honeywell). It was thus necessary for the program to characterize F-N tunneling, data-retention, and cycling characteristics of the available devices. A memory cell structure would then need to be developed that could be used to build a practical array of such memory cells. It would then also be necessary to develop the means on-chip to generate and apply voltages to program and/or erase these memory cells, without altering the memory state of adjacent cells. This would necessarily require applying and routing voltages that exceed the normal operating voltages of technology. Finally all of these concepts would need to be incorporated in a practical product design with the features and functionality required (as determined by JIP group consensus).

All of this was accomplished on the program. It required several cycles of design and wafer fabrication to achieve the final result.

6.3.1.1 Short-loop Wafer-process Experiments

One of the early technology concerns was the quality and characteristics of the oxides isolating the floating-gate from the rest of the circuitry. It was initially believed that wafer-process modifications might be necessary in the formation and geometries of these oxides (and underlying structures). This concern was addressed by using a pre-existing product mask set to complete an abbreviated sequence of processing steps (since the full wafer process flow was not completed these are called “short-loop” experiments). Variations in the means of forming the oxides surrounding gate structure were introduced on different wafers. Data was then collected to characterize the ability to retain charge induced onto the gate node by F-N conduction through the gate oxide. It was thereby determined that the existing process flow was equally capable in this respect to the proposed improvements. As a result, no changes were made to the process flow for the EEPROM.

6.3.1.2 Test chip 1

While completing the short-loop, a test-chip was designed for the purpose of studying consideration for memory cell design and optimization. The test chip contained a large number of geometries and device types to assess trade-offs for programming and read-out as well as to optimize the geometries for compact layout and suitability for arraying in a large-memory format.

There were many choices available for the structure underlying the tunneling oxide that could affect tunneling and read-out characteristics (doping of underlying silicon; doping, construction, and spacing adjacent source/drain structure, etc.). In all 134 permutations for the topology were identified. Arrays of devices were designed to study tunneling and capacitance vs. voltage characteristics (important for read-out considerations). Wafers were processed in multiple small batches to incorporate effects of manufacturing process variations in the findings.

This activity allowed the selection of a specific topology for the tunneling and readout devices. A long-term high-temperature data-retention study was initiated on that memory cell topology which continued for 8,000 hours at 250°C (see appendix 4, figure 6).

6.3.1.3 Test chip 2 and Demonstration Memory

As test-chip 1 evaluation was being completed, design of test chip 2 was underway. The primary objective of test-chip 2 was to apply the findings of test chip 1 to the construction of a demonstration memory. This would address the practical aspects of developing a product design around the selected bit-cell structure. Circuit design and layout considerations for the demonstration memory included:

- Layout considerations for accessing a two-dimensional array, including aspect ratio, cell area, interconnect by abutment, etc.
- Row and column interfaces capable of accessing memory cells by address, and for applying voltages required to program/erase addressed bit cells without disturbing adjacent cells

- Effect of leakage currents on accessing and reading out individual cell data and circuit approaches to mitigate the effects of high-temperature transistor leakage
- Providing means to apply externally generated high-voltage waveforms for the purpose of optimizing program/erase operations.
- Demonstration and testing of critical memory sub-blocks and devices, such as sense-amps, logic level shifters, and extended-drain transistors (for extended voltage range operation).

The Test Chip 2 design was completed and fabricated on using a mask set and wafer lot which also carried the first pass A-to-D converter design. Test chip 2 contained a 4K x 8 bit memory (1/8th the size of the planned 32K x 8 bit product design). Extensive testing was completed, and the results of testing documented in a report delivered to DOE (DeepTrek EEPROM TC-2 Test Report, reference 8). Testing involved the design and development of dedicated evaluation boards. Scope of testing including:

- Functional testing of the demonstration memory including reading and writing at 250°C
- Characterization of writing versus program/erase waveforms (amplitude, duration, and rise-fall times).
- High-temperature data retention testing
- Testing of memory sectoring as a means to address high-temperature leakage impact on read-out.
- Effects of data cycling on the bit cell write and data retention characteristics (at 25°C and 250°C).
- Sub-block testing (Sense Amplifier and Level Shifters)

Outcome of this testing supported the continuation on to full product design. Test chip 2 enabled the specification of the waveform requirements (amplitude and duration) for the product design. It also allowed for prediction of the combined effects of data cycling and high-temperature operation on data retention. The memory cells should be capable of supporting over 10,000 program/erase cycles while retaining capability to retain data for 1,000 hours at 250°C. Data retention can be extended by periodically refreshing (re-writing) the memory, a feature that was incorporated into the product design.

6.3.1.4 Product Design and Fabrication

The results from test-chip 2 made it possible to proceed with complete product design and fabrication. The product design and fabrication was completed in the last few months of the program. The product design started from core of the demonstration memory, expanded the memory array to the full 32K x 8 bits, added control logic for reading and writing the memory, charge-pumps and analog circuitry for high-voltage supplies and write-waveform generation, interface circuitry for autonomously loading an FPGA on power-up, timers and system-level interface for periodic memory refresh, and a serial-mode “wrapper” so that the die can be configured for operation either as a memory with a serial data interface (incorporating all of the functionality of “25C256” industry standard devices) in addition to functioning as a parallel memory (as with “28C256” memory devices).

Configuration for serial vs. parallel data interface can be exercised by a single digital input pin. Manufacturing test features and interfaces were also integrated into the design. Seven external capacitors are required to support high-voltage supply generation for on-chip writing. It is envisioned that 10nF ceramic chip capacitors could be incorporated inside a hermetically sealed high-temperature ceramic package to serve this purpose.

The resulting design has the following features and/or performance targets

- 5 V Operation, ± 5%.
- -55 °C to 225 °C temperature range (250°C die temperature)
- Read and write over full temperature range
- 5 year continuous operation at 225°C
- 10,000 data write cycles
- 1,000 hour intrinsic (no refresh) data retention at 250°C die temperature
- Read access: < 200 ns
- Available as parallel or serial interface, modeled after industry 28C256 and 25C256 components (configure by pad connection)
- Includes FPGA configuration loader
- Incorporates EEPROM High Temperature Data Management
    - 5-year data retention at >225C with periodic refresh (re-write)
    - Refresh hand-shake request on POR (cleared after 20 seconds)
    - Refresh hand-shake request at 30-day intervals

Fabrication was completed in June, 2007. A die photo is shown in Figure 2 below. A block diagram and description of I/O is provided as Figure 3.

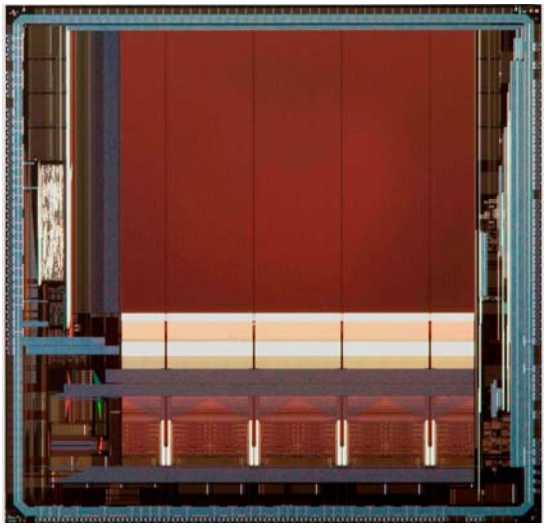


Figure 2: EEPROM Die Photo

Die Size is 12.3mm x 12.77mm

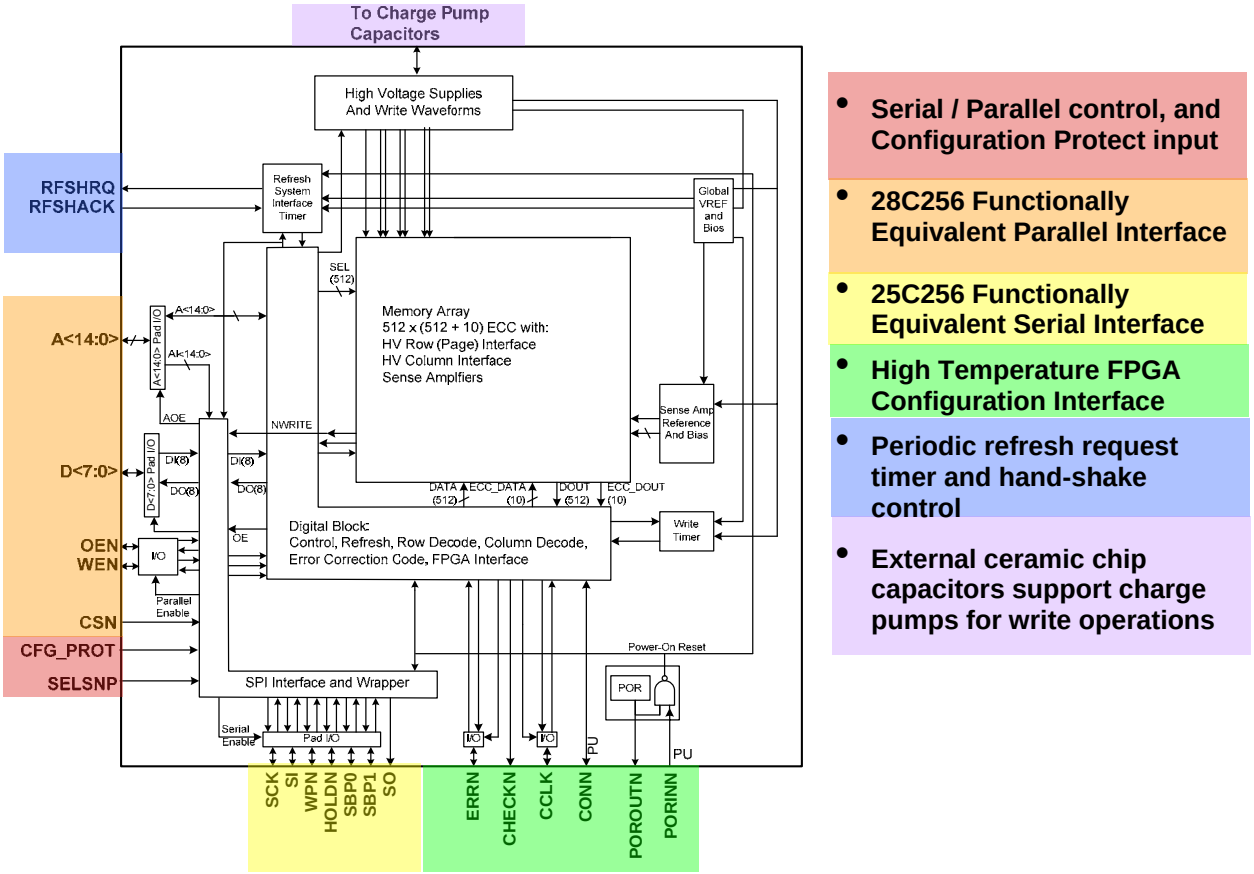


Figure 3: EEPROM Block Diagram and I/O (color keyed by usage)

6.3.2 FPGA

The FPGA was implemented in accordance with the development plan established by the March, 2004 Statement of Project Objectives, with a few revisions.

6.3.2.1 Initial Planning and Feasibility

Between the program start in October 2003 and the first SOPO revision the JIP group provided direction that the program tasks/budget needed to be adjusted to accommodate the EEPROM development. A military temperature range version of the FPGA had been previously implemented for defense and space applications by licensing and functional emulation of the Atmel AT6010. Atmel documentation [1] provides a thorough description of the features and operation of the AT6010. This documentation is also applicable for describing the features and operation of Honeywell's FPGA designs, both the previous military-aerospace FPGA and the high-temperature FPGA developed on the DeepTrek program.

This prior implementation was accomplished in 0.35 micron SOI process technology. Development of a high-temperature version of that technology was part of the original program scope. However, given the requirement to fund the EEPROM development, it was proposed that the 0.35 micron SOI high-temperature process development should be removed from the program. This raised the question as to whether or not the FPGA could continue as a program element.

The initial activity for the FPGA therefore focused on the question of whether it would be feasible to develop this component in the HTSOI4 technology which would make this die significantly larger due to the 0.8 micron minimum feature size for HTSOI4. This required careful analysis, because it soon became clear that the estimated die size in HTSOI4 would be very close (if not over) the maximum die size that could be implemented in the process due to photo-mask size constraints and other wafer process considerations. This feasibility analysis was completed with the conclusion that the die could be make to fit by careful design and re-layout of the configurable-logic-blocks that comprised the bulk of the die area, along with development of custom programmable I/O cells (prior implementations used gate-array I/O cells).

6.3.2.2 Design and Fabrication

Design and layout for the HTSOI4 version of the HTFPGA began in June 2004, and would continue through July 2005. The design process used has been described in the Technical Approach section. Physical layout of the device was started from scratch with the layout of repeated internal structures and working out through interconnect and power-distribution routing to the I/O ring. Functional equivalence between the top-level design and the previous versions of the design was ensured by simulation. Selected test patterns from production tests were applied to the gate-level representation of the design database to verify that the response to test stimulus matched that of the previously produced versions. This is actually a very complex process due to the nature of functional testing of the FPGA. The FPGA first goes through an autonomous re-boot sequence wherein the contents of all of the internal configuration memory bits are cleared. This is followed by a configuration process where the FPGA is configured using configuration pins dedicated for that purpose. Only after the FPGA is thus configured can the functional stimulus be applied and the response captured.

The HTSOI4 FPGA design completed fabrication in September 2005. A die photo of the FPGA is shown in figure 4. Note that the die is very large. A 6-inch HTSOI4 wafer contains 56 die.

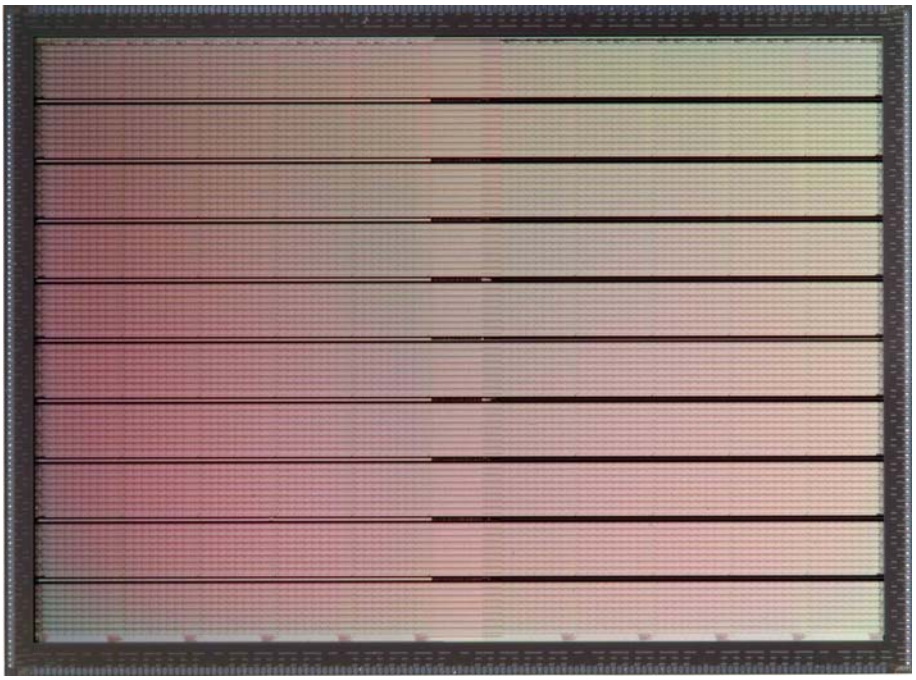


Figure 4: FPGA Die Photo. Die size is 16.1mm x 12.0mm

6.3.2.3 Test Development and Evaluation

Wafer-level test hardware and software development and testing were completed from October 2005 through April 2006. Test patterns used for production testing of the military-aerospace version of the FPGA were applied to the new HTSOI4 FPGA. This involved a process of conversion due to a different arrangement of I/O between the two designs. Other test parameters were also adjusted. A high-temperature 352-pin wafer-level probe-card was ordered and configured for use with a Schlumberger ITS 9000 test system. There was a fabrication error with the probe-card that required a vendor replacement. Test debug was complicated by the asynchronous nature of the FPGA autonomous power-on reboot sequence versus the tester requirements for a synchronous interface. Eventually these were overcome and the test vector files were used to validate the FPGA design.

The production test patterns used for the FPGA consisted of 136 separate vector files. For each test vector file the FPGA was re-booted and configured prior to functional testing of configured performance. The manufacturing test vector set was designed to provide detection of logic faults to a level of greater than 99% of all possible faults. Eventually three FPGA wafers were fully tested at wafer temperatures of 25°C and 200°C. Yield from this wafer-level probe testing was in line with normal manufacturing production requirements.

The initial development plan made provision for a second pass design iteration. This was not necessary due to the success of the first pass design. The plan also called for the development of a high-temperature package. This was not done. Likely users among the JIP members indicated that they would most likely take delivery of the FPGA in die form. A further complicating factor is the flexibility of the design itself. It is not clear what an “optimal” package configuration would be. The programmable I/O arrangement of the FPGA lends itself to a wide variety of potential packaging scenarios, from very high lead counts to very low lead counts. It was therefore decided remove the package development element from the program.

6.3.3 High Resolution A-to-D Converter

A high-resolution A-to-D converter has been developed, including a first pass design and a second pass design iteration. Functionality of the designs has been verified by laboratory testing at wafer-probe level and also by testing of packaged devices using evaluation boards and PC-based software developed specifically for that purpose.

6.3.3.1 A-to-D Planning and Specification

Detailed specification and planning for the A-to-D design was initiated in second quarter of 2004. A very high-level block diagram for the A-to-D is shown in Figure 5. Figure 5 shows 28 I/O (including power supply pins). The design was originally intended for commercial offering in a 24 pin DIP. This was later changed to 28 pin DIP as the specification evolved with JIP group review and directions.

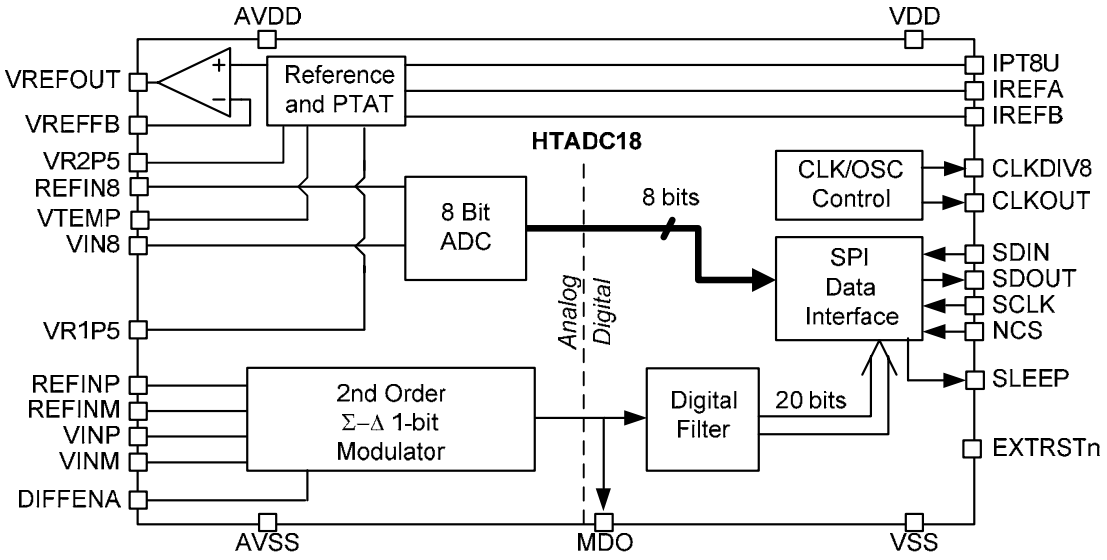


Figure 5: A-to-D Converter Block Diagram

Referring to Figure 5, the high-resolution A-to-D converter is represented by the blocks labeled "2nd Order Σ-Δ 1-bit Modulator" (where "Σ-Δ" is read as "sigma-delta") and "Digital Filter". A description of sigma-delta A-to-D operation is beyond the scope of this report. It will be sufficient here to state the modulator is clocked at 204.8 KHz and produces a bit stream (1-bit wide) at that rate which is the input to the digital filter. The digital filter processes the data and produces an output after 2048 samples that is a digital representation of the analog input voltage imposed on the differential input pins VINP and VINM. The output is proportional to the reference voltage that is imposed on the differential reference input pins REFINP and REFINM.

The digital output provided has 20-bitis of resolution. However, the useful resolution will be less than 20 bits.

The other functions shown on Figure 5 included reference voltage sources and buffered outputs, and an on-chip oscillator that generates the clock 204.8 KHz clock needed to operate the A-to-D converter. The A-to-D data is provided to the system in a serial format by means of the Serial Peripheral Interface (SPI) block. The SPI also provides means for controlling A-to-D operation, such as power-management features, output control, and data format. The 8-bit ADC is an auxiliary function that is primarily intended to provide temperature data to the system. The reference block also provides an output which is a proportional to temperature. This may be connected to the input of the 8-bit ADC. However, the 8-bit ADC could be used for other purposes by connecting it to an external source.

Detailed planning and specification for the A-to-D converter development started in second quarter of 2004. In May 2004 Honeywell proposed that DOE/NETL arrange to obtain consulting and design service from the Monolithic Systems Group at Oak Ridge National Laboratory (ORNL). ORNL staff began working with Honeywell on the project in June 2004. ORNL was given design responsibility for the core 18-bit A-to-D converter blocks (sigma-delta modulator and digital filter). Honeywell retained responsibility for all of the other functions, all physical layout,

and chip-level assembly. A Design Architecture Specification was drafted. This internal document defined in detail the design hierarchy, including identification of all sub-blocks in terms of functionality, I/O, and key performance parameters. During all phases of the A-to-D development DOE and the JIP group were kept informed of specifications and design progress at a high level of detail. This was accomplished by quarterly DOE/JIP reviews and other topical updates.

6.3.3.2 A-to-D First Pass Design and Wafer Fabrication

The design was built on a physical design platform of an HT2000 digital gate array. Multiple power-supply domains were defined to separate sensitive analog sections from each other and especially from the digital section of the design. The objective is to minimize noise coupling and interference via the power grid.

Full-custom design was employed for the analog portions of the design. As it became available Honeywell provided ORNL staff with technology data and Cadence software licenses to enable them to use the Cadence PDK design tools on the analog portion of the design. These were also in use by Honeywell designers for the analog blocks developed by Honeywell.

Digital blocks were implemented using gate array cells. ORNL's digital design was done at the functional level. ORNL provided HDL netlists representing the digital filter functionality at the Register-Transfer-Level of design abstraction. Honeywell synthesized the ORNL deliverable into HT2000 logic gates and integrated ORNL's design with other digital blocks developed at Honeywell. Honeywell also inserted all design for test features of the digital blocks. All subsequent synthesis, layout, timing analysis, and insertion into HT2000 I/O rings were performed by Honeywell.

One of the original design targets was to implement the complete A-to-D on an HT2080 gate-array platform. The HT2080 is one of several base arrays in the HT2000 family of gate arrays. It contains roughly 80,000 unconnected gates of digital logic, ready for customization using design-specific interconnect layers. ORNL and Honeywell took all reasonable steps to minimize the number of gates required to meet the digital filter requirements. Nevertheless, early trial syntheses of the digital netlists showed that there would not be enough gates on the HT2080 do accomplish the task. Therefore the decision was made to implement the design on the larger HT2160 gate array, which provided roughly 160,000 gates of digital logic (twice the capacity of the HT2080). The completed design ended up using approximately 90,000 logic gates (this does not include any allowance for the analog blocks). In terms of overall area the HT2160 is approximately 65% larger than the HT2080 (the HT2080 carries a larger overhead for I/O and power grid than the HT2160).

It was also decided to add three pins:

DIFFENA: A DC input to re-configure the sigma-delta modulator front end for either single-ended (ground-referenced) input signals or differential (mid-supply referenced) inputs.

SLEEP: A DC output asserted under SPI control when the ADC goes into sleep mode (one of the power-management features of the A-to-D)

FSDIV64: The 18-bit A-to-D sampling frequency divided by 64. This was provided for use as a clock source for auto-zeroing the dual precision amplifier.

This required growing the targeted package size from 24 pin DIP to 28 pin DIP.

Figure 6 shows the top-level partition of the ADC between analog and digital sections. It also represents the division of the I/O ring into three sections in accordance with the three power-supply domains that were implemented. It also shows all I/O signals, including those that were provided for wafer-level test and/or initial characterization (as opposed to those signals which would be accessible in the 28-pin DIP. An advance data sheet showing the proposed 28-pin DIP pin out is provided as Appendix 7.

In order to meet target requirements for some of key parameters, the design of some of the analog blocks made provisions for trimming to be accomplished by laser at wafer-level probe test. This includes trimming for voltage reference initial value and temperature coefficient, oscillator frequency, and thermometer output (VTEMP) offset. Note that some of these trims require wafer level testing at two temperatures in order to calculate trim parameters.

First pass design and layout activity culminated in a final design review and release for fabrication in June 2005. The design was fabricated on the same mask set and wafer run as the EEPROM Test Chip. Wafer fabrication was completed in October 2005.

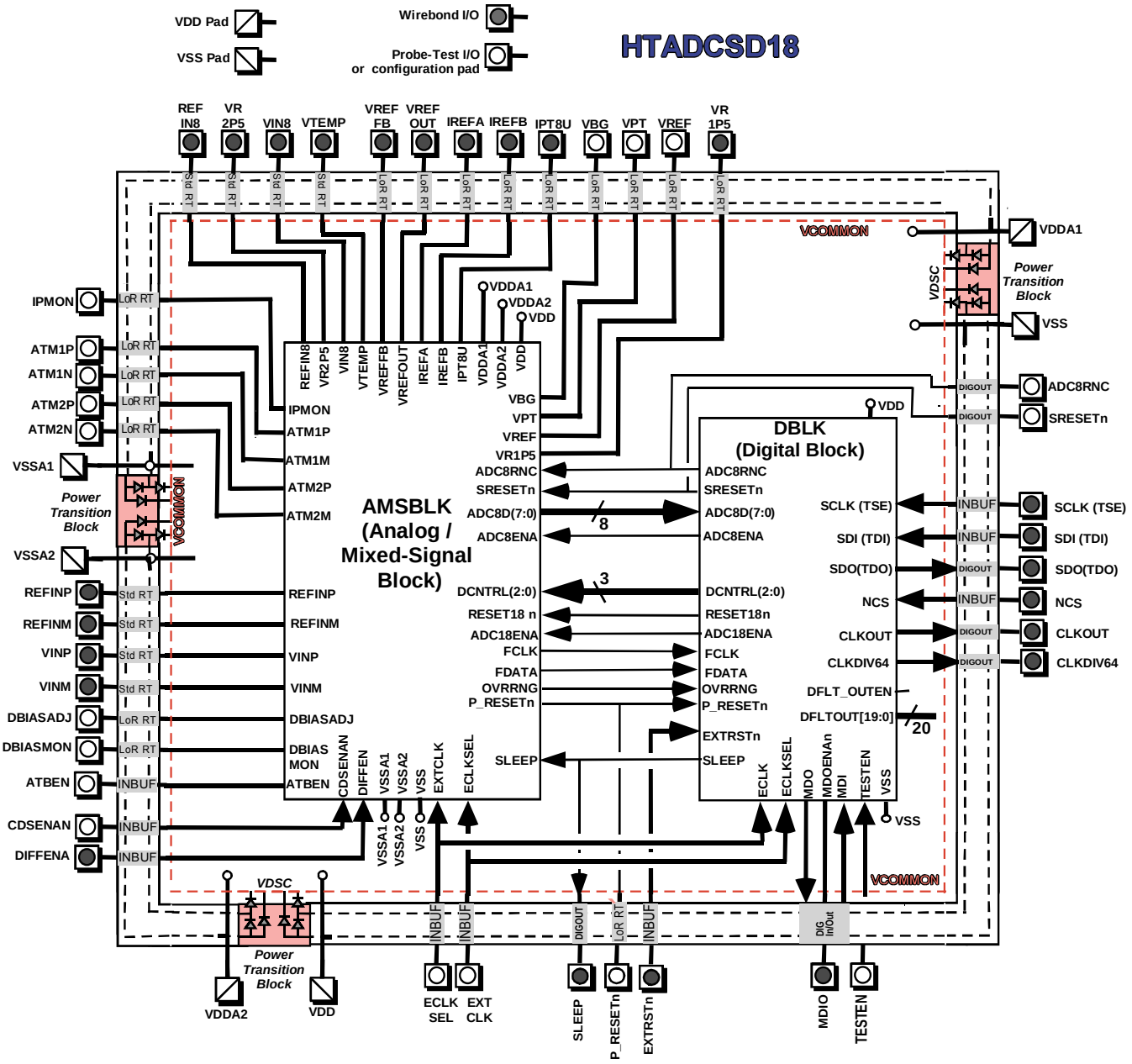


Figure 6: A-to-D Top-level Design Partition Showing I/O by type

6.3.3.3 A-to-D First Pass Test and Evaluation

It was decided to forego first-pass wafer-level trimming in favor of assembly of untested die. In addition to the signals provided for pin out in 28-pin DIP, there were a number of additional I/O for the purpose of test and evaluation. Therefore, for initial prototype evaluation the A-to-D die were assembled in a 208 Pin-Grid-Array (PGA) package that had been previously developed for use with HT2160 die. Evaluation boards were designed specifically for the purpose of testing this package configuration.

While the A-to-D assembly and evaluation board design and procurement were in progress, characterization was begun on the reference block of the A-to-D. The

reference block layout had been extracted from the A-to-D design and replicated so that is could be fabricated on the same wafers as the complete A-to-D but assembled and characterized separately as an isolated function block. A small number of reference blocks were assembled and characterized. In addition, a small number of die were manually laser trimmed at wafer level and characterized over temperature. After initial testing, a number of the packaged reference blocks were tested for over 1000 hours at 250°C. Results of this testing were reported at HiTEC 2006 in May of 2006. These results are provided as Appendix 5.

Meanwhile, evaluation board procurement and assembly was completed and a number of samples were tested over temperature and supply by Honeywell. This testing showed that the design was functional over the full operating supply and temperature range. Honeywell's characterization software exercised the part by applying DC inputs and sweeping the input values over the full inputs. After completing this DC characterization testing Honeywell separately funded ORNL to conduct additional testing using sinusoidal input waveforms and AC analysis techniques. Significant successes from first pass testing included:

- Complete functional verification including:
  - Power-up initialization and operations as expected
  - SPI works to configure operating mode & output format
  - 18-bit converter exercised from analog input to serial digital output
  - Operated with both internal and external references
  - Operated with internal and external clock sources
  - Control and output via the SPI interface
  - Data processed through the digital filter
- Consistent performance part to part
- Functional wafer-process and assembly yield is good
- Functionality verified over full operating supply voltage range
- All utility functions verified, including temperature output, 8-bit A-to-D and references (with one exception, discussed below).

Parametric test results were mixed. On the positive side:

- All auxiliary circuitry (oscillator, references, and 8-bit ADC) showed parametric performance consistent with design requirements over the full temperature range.
- The A-to-D linearity achieved the goal of plus/minus 20ppm of full-scale at -55°C and 225°C (see Figure 8).
- The Effective-Number-of-Bits (ENOB) calculated from 225°C AC test data was approximately 17.4 bits.
- Effected RMS resolution at 25°C and 225°C was 17.6 bits and 17.7 bits respectively (based on output noise for a 0V DC input, see Figure 9).

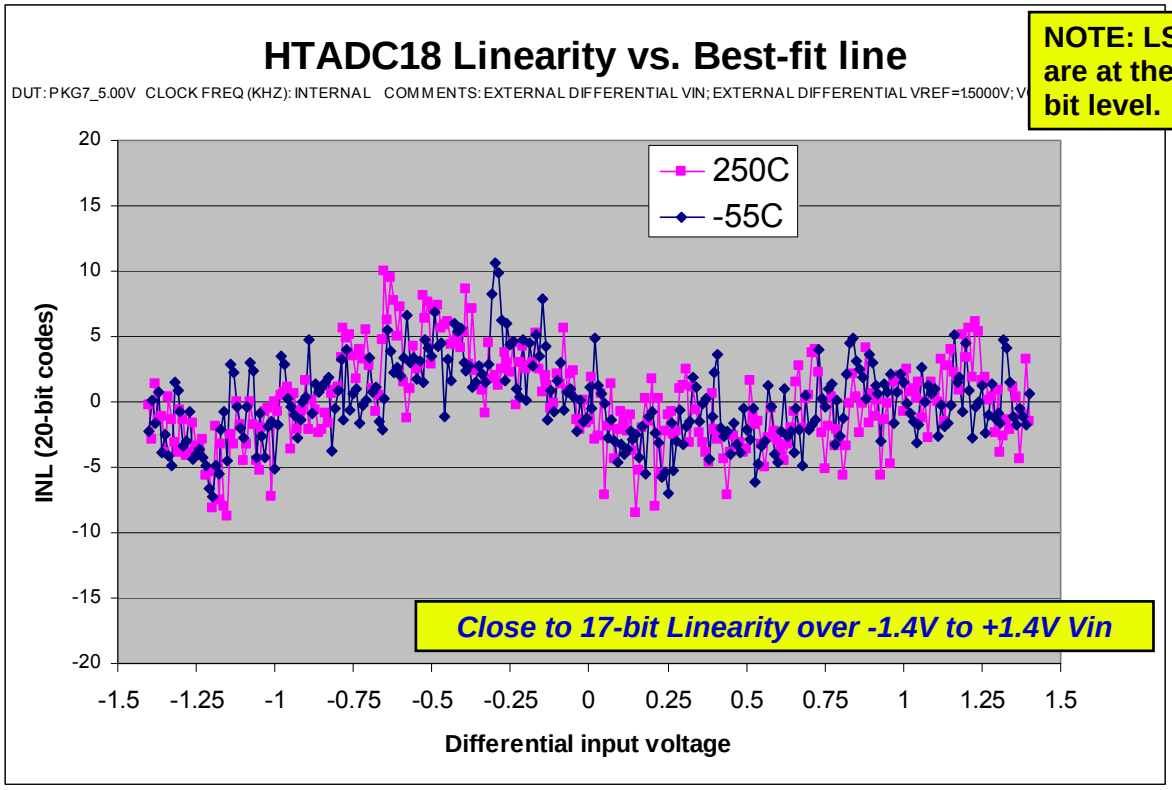
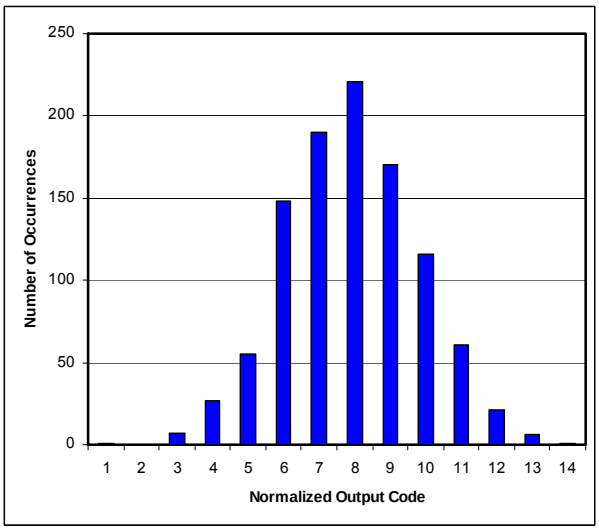
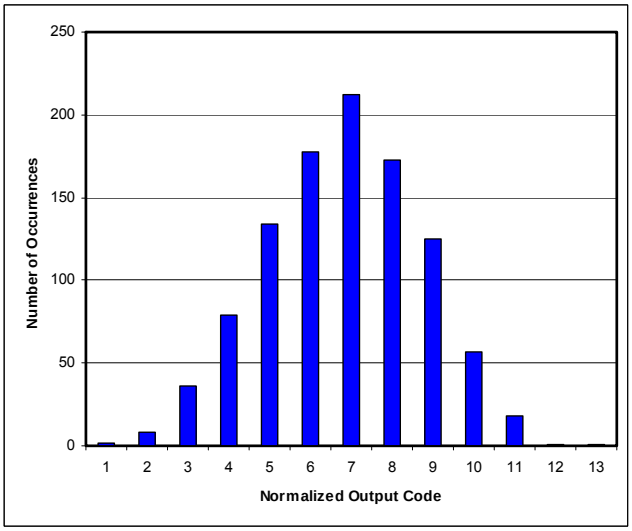


Figure 8: High resolution A-to-D Typical Linearity at 5.0V supply





σ= 4.18, Output RMS Noise ~ 12μV$_{rms}$
Effective Resolution = 107.9 dB = 17.6 Bits
Peak-to-Peak Resolution = 14.9 Bits

σ=3.89 , Output RMS Noise ~ 11.1μV$_{rms}$
Effective Resolution = 108.6 dB = 17.7 Bits
Peak-to-Peak Resolution = 15.0 Bits

Figure 9: Effective RMS output noise
Zero-volt DC input is applied; 1024 samples used to calculate the output RMS noise

On the negative side, it was observed that at intermediate temperatures DC linearity was degraded by several bits (worst-case at 30°C to 40°C). AC testing also showed increased levels of distortion, reducing the effective AC resolution by several bits. Significant effort was made to identify root-cause for this degradation, including additional testing under many different operating conditions and variations in test configuration. These efforts were unsuccessful in identifying any root-cause from the test hardware/software, operating conditions, or IC design and layout. However, as this report is being written there is now strong evidence that this degradation is associated with the IC assembly means. The most likely cause is mechanical stress that affects electrical response of the sigma-delta modulator. Such stresses at specific temperature can arise as a result of the method for bonding the die to the ceramic package, and differences in coefficient of thermal expansion (CTE) of the materials involved.

On the functional side, two errors were discovered: (1) there was an interconnect error that rendered one of the buffered voltage reference outputs non-functional. However, this did not prevent verification of the rest of the design; (2) there was a design error in the implementation of a dither control circuit. This circuit was introduced as empirically based risk mitigation for A-to-D DC performance. It is known that introducing low-level random noise at the input (at a frequency that is filtered out by the digital filter) can improve DC linearity at the expense of AC distortion in sigma-delta A-to-D converters. This feature was not required in order to assess baseline performance.

6.3.3.4 A-to-D Second Pass Design and Fabrication

It was decided to proceed with a second pass design iteration for the A-to-D converter. In addition to correcting known design errors (reference buffer and dither circuit) it was determined that changes were required to the serial interface (SPI). The previously implemented SPI did not fully conform to common industry implementations. This could lead to problems in using the A-to-D for applications where it shared serial data bus connections with other system components.

It was also determined to make some other modifications in the output data format. These were primarily motivated by system “ease-of-use” considerations. These included provided A-to-D configuration status as the leading bits for all data transfers, and providing means to specify the 18-bit A-to-D data format (2’s complement or binary).

Other minor second pass design modifications included:

- Circuit adjustments were made to optimize reduce oscillator and current reference temperature coefficients
- Modified “sleep” mode to leave reference circuitry on during sleep mode. Maintaining reference circuits under electrical biased has been observed to reduce high-temperature drift with time

Second pass design and layout changes were completed, culminating in a second pass final design review and release to fabrication in March 2007. Second pass wafer fabrication was completed at the end of May 2007. Although no second pass testing was completed within this program, it has been verified that all of the second pass design changes were successfully implemented with one small exception: the corrected dither circuit does not shut-off as intended during “sleep”

mode (one of the A-to-D power management features). This can be easily corrected by a modified metal interconnect mask on the next wafer lot.

6.3.3.5 A-to-D Package Development

A 28-pin DIP package was designed and procured for use with the second pass design. This package features optimized placement of package wirebond pads for proximity to the die wirebond pads, as well as customize power and ground planes and the capability for mounting ceramic chip capacitors directly on the package for power-supply noise suppression. Although no second pass testing was completed within this program, it is known by independently funded Honeywell testing that these packages are correctly implemented and functional for use.

6.3.4 Dual Precision Amplifier

The dual precision amplifier was the first component developed under the program. First pass design, fabrication, assembly and testing was completed. Based on the successful outcome of the first pass design, no second pass design was required.

6.3.4.1 Amplifier Design, Layout and Fabrication

Design and layout were completed using the Cadence PDK and full-custom design and layout approach. The amplifier employs continuous auto-zero to cancel internal offset voltage and reduce amplifier low-frequency noise. The overall approach is similar to that employed by Opris and Kovacs [8]. This is discussed in more detail in Appendix 3. First pass critical design review was completed in October, 2004. The die size is approximately 2.3mm x 1.8 mm. A dedicated mask set was procured and wafer lot was fabricated. Each wafer contains 2790 die. Figure 10 is a photo of the die.

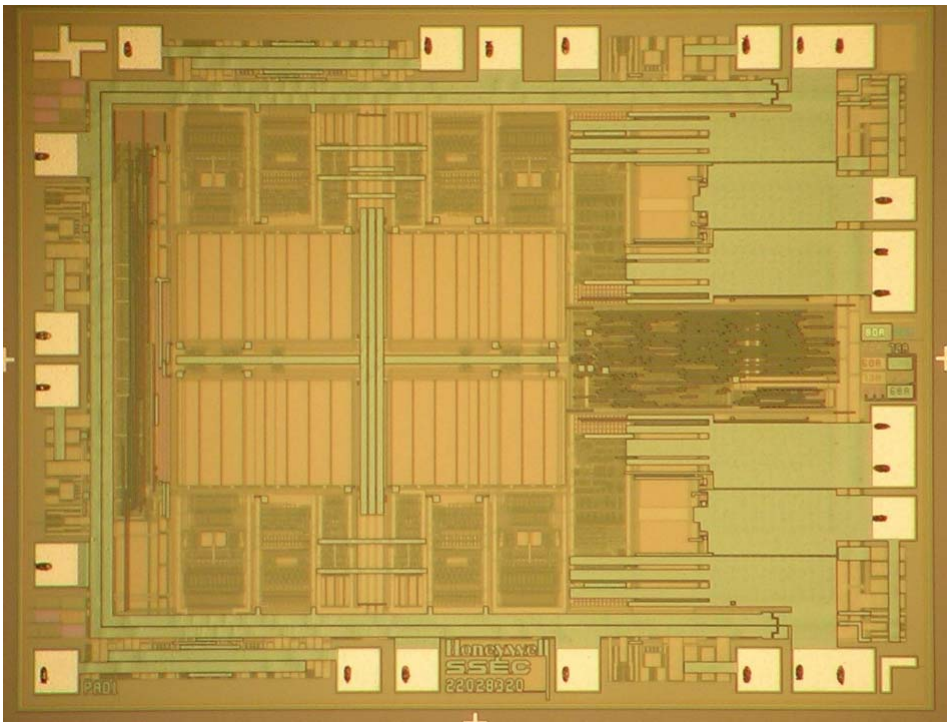


Figure 10: Dual Precision Amplifier Die Photo

6.3.4.2 Precision Amplifier Assembly and Testing

Wafer-level probe-cards were procured for wafer-level probe testing using Honeywell's production automated test equipment. In addition a custom 14-pin DIP package was developed and a test interface board procured for package level testing using the same tester.

The initial wafer lot was tested and all wafers provided high yield to the prescribed tests. Wafer level testing was performed at 25°C. One wafer was sawed and diced and an assembly lot of 50 units was packaged. Package level testing was conducted at three temperatures (-55°C, 25°C, and 225°C). Samples from this initial package lot were then distributed to the JIP group and DOE. Results have been reported at HiTEN in 2005 (see Appendix 3). Based on the successful results the JIP agreed that a second pass design iteration was not required. No further development was performed under the program. In 2007 the remaining wafers were sawed and all die were made available for distribution to the DOE and JIP group.

A preliminary data sheet for this component (designated for marketing purposes as the HTOP01) has been developed and is provided as Appendix 8.

7.0 Summary and Conclusions

The Deep Trek High Temperature Electronics project objectives have been met.

An integrated circuit process technology and supporting design/development tools have been upgraded to production and demonstrated by the successful development of high-temperature integrated circuits. This is the first time a production technology and design tools have been established in the United States (perhaps the world) specifically targeting applications extending to 225°C and beyond.

All of the IC components targeted for development have been designed and fabricated. Only the EEPROM remains to be functionally verified in its intended product configuration. In all cases, the components that have been developed embody a level of performance, complexity and precision that has not been previously attained in the laboratory, much less as a commercial product.

The results of this program show that when up-front investment in integrated circuit technology and design tools is made, that successful development of complex and high-precision IC components can be achieved. This is a good start, but is certainly does not meet all of the needs for high-temperature down-hole oil and gas instrumentation. There were elements of this program that had to be dropped for insufficient funding, including high-temperature development for 0.35 micron technology and microcontroller development. The oil and gas industry is accustomed to using higher levels of performance and functionality in digital processors than can be achieved by the 0.8 micron technology. On the opposite end of the integrated circuit technology continuum, power devices are also needed for DC-DC converters, motors and generators that can operate reliably at high voltages take the heat down-hole. It would certainly be of benefit to the oil and gas (and geothermal) industries to have a wider range of high temperature technologies than are represented within this program alone.

As for the components developed on this program, they are well on their way to the objective of commercialization. The package stress issue that affects the A-to-D converter will require additional engineering to establish a viable low-stress alternative. Otherwise, testing, burn-in and screening flow development will be accomplished for all of the components as they are brought to market.

Many more components will need to be developed to meet the needs for all of the applications that the oil and gas industry would like to see extended. Hopefully the success of this project will stimulate additional high-temperature electronics development and economic activity in the oil and gas industry and in adjacent high-temperature market applications, such as aerospace, defense, and industrial controls.

Appendix 1

High Temperature 0.8 Micron 5V SOI CMOS for Analog/Mixed Signal Applications

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Abstract

A 0.8 micron, 5-volt silicon-on-insulator wafer process with analog/mixed-signal device extensions has been developed for High-temperature applications. Previously, this process technology has been used for purely digital high-temperature applications where parts are 100% tested at 225°C. In addition to previously developed standard NMOS and PMOS transistors, the wafer process flow has been augmented to include options for thin-film CrSiN resistors and linear capacitors. Layout techniques have been developed for extending drain-to-source breakdown voltage. Designs are layout and design rule compatible with a military temperature range wafer process. Devices and analog/mixed-signal test circuits will be characterized at high temperature (225°C). This work is co-funded by U.S. Dept. of Energy and industry for down-hole oil/gas drilling applications.

Introduction

The absence of high temperature electronics is an obstacle to accessing untapped energy resources (deep oil, gas, and geothermal) [1]. At extreme depths (15,000 to 20,000 feet) environmental temperatures of up to 225°C may be encountered.

In previous papers SOI CMOS process technologies have been reported that are capable for operation at 225°C and above [2,3]. High Temperature products have been implemented using these processes and reliable operation at high temperature has been established [4]. However, there has been little support for combining both analog and digital circuits on a single high-temperature SOI process. Instead, analog circuits have typically been implemented using processes that are relatively low density but have analog features (e.g., resistors and capacitors). Often analog products are implemented in processes that have only two layers of interconnect. Digital circuits typically require higher density and at least 3 or 4 layers of metal interconnect. This approach compounds the issue of commercializing high-temperature electronics. The high temperature (>150°C) electronics market is very low-volume by semiconductor manufacturing standards. Trying to support multiple process flows, one analog and another digital, for a small market is not an easy task.

This paper describes an SOI CMOS process technology that is being developed specifically for high temperature applications. The technology baseline is a 5V digital process technology. To make this process "friendly" for analog applications additional devices will be supported for high temperature. These include thin-film CrSiN resistors, linear capacitors, and extended-drain (lateral DMOS) transistors to support high drain-source voltages. Other important requirements are to provide accurate device models for the full operating temperature range, and to provide support for industry accepted design and layout tools. The goal is to provide high

[1] Development partially funded by the DeepTrek program of the National Energy Technology Laboratory, U.S. Dept. of Energy (DOE).

temperature technology that will be accessible on a foundry basis for commercial high-temperature applications. The high temperature process benefits from the fact that it is very similar to a military aerospace process. The benefit of this similarity is that the two processes most of the same equipment, operations, layout rules, and design flows. A high-reliability, production process is adapted to high temperature as opposed to developing a new process to support the high-temperature market.

Process Trade-offs and Features

Features of the mixed analog/digital process are shown in Table 1. It is well known that supporting analog and digital applications in a single process flow is an art of compromise. Commercial needs drive conventional digital electronics to ever increasing density and speed. This in turn leads to power management issues and therefore pressure to operate at lower and lower supply voltages. This impacts analog applications negatively in terms of reduced signal swings and lower signal-to-noise ratios.

Table 1

Process Feature	Typical Characteristics
Gate Oxide	150 angstroms
Min transistor length	0.8 microns
Max. Gate Ox. Voltage	5v
Target Vtn/Vtp • 25°C • 250°C	 1.2V / -1.3V 0.85V / - 1.0V
Sub-Vt slope (mV/dec) • 25°C • 250°C	NMOS PMOS 150 180 260 320
Transistor "Off current" • Nch, 250°C • Pch, 250°C	 0.8 nA/micron width 0.5 nA/micron width
# of metal layers	3 or 4
Top Si Thickness	0.2 microns
Buried Oxide Thickness	0.4 microns
Partially/Fully depleted	Partially depleted
Poly-silicon resistors	90 ohms per square 415 ppm/°C
CrSiN resistors	2.5K ohms per square ± 300 ppm/°C
DMOS layout (drain/source breakdown)	 Nch: >25V VDS Pch: < -30V VDS
Linear Capacitor	670 angstroms <150 ppm/Volt
Laser trim fuse links	Yes
Lateral PNP VREF	For delta-Vbe only

Wide temperature range applications add the complications of parametric device shifts, including threshold, mobility, and junction leakage. These parametric shifts tend to erase whatever voltage "headroom" may be available for analog signal processing in a low-voltage digital process.

The high-temperature mixed-signal flow builds from a digital technology foundation that features 0.8 micron minimum gate lengths, supports 5V operation, and provides up to 4 layers of metal interconnect. This is not "state of the art" relative to commercial electronics for conventional applications. However it is technically capable of supporting relatively complex functions (e.g., SRAM up to 1 Mbits or digital ASIC's in range of 200K gates). At the same time it provides sufficient operating voltage to support device parametric shifts that occur over a wide temperature range and still support analog signal processing. In order to support high-gate-count digital circuits at high temperatures, the room-temperature threshold voltage is increased. This is necessary since both threshold voltage and sub-threshold slope decreases with temperature as can be seen in Figure 1. Without threshold voltage adjustment digital "off" leakage at high temperature may be dominated by sub-threshold conduction rather than junction leakage. To prevent this, the digital process has a relatively high threshold voltage so that high-temperature "off current" is dominated by junction leakage rather than sub-threshold leakage at temperatures below approximately 250°C.

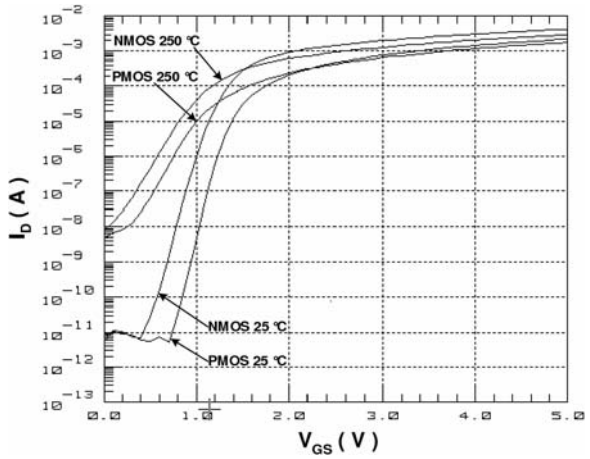

Figure 1: Log ID vs. Vgs for a 10/0.8 micron device at VDS=5V

NMOS/PMOS Transistors

This process is a partially depleted SOI process, meaning that the top-silicon is not fully depleted before the onset of inversion and the formation of the conducting channel. In this type of process the transistor body may be contacted directly and "floating-body" effects avoided. Note that unlike conventional bulk CMOS, the body connection for partially depleted SOI is a lateral connection. Methods for connecting the body in an NMOS device are shown in Figure1. The body terminal may be connected using a "body-tie" silicon region that extends outside of the transistor source-drain. This body-tie silicon is the same well material as the transistor channel region. An ohmic contact to P-well (N-well) is provided by a P+ (N+) implant region for Nch (Pch) devices. For source-to-body tied transistors this is illustrated in the top-left portion of Figure 1. In order to avoid parasitic lateral bipolar conduction from source to drain, it is desirable to limit the resistance of the lateral body-tie connection from the middle of the transistor to the ohmic body-tie contact. This is managed by layout rules that limit the maximum width of the devices. This is not usually a concern for on-chip digital logic, but is often a constraint for analog and/or devices that must have good matching, low noise, low on-resistance or conduct large currents.

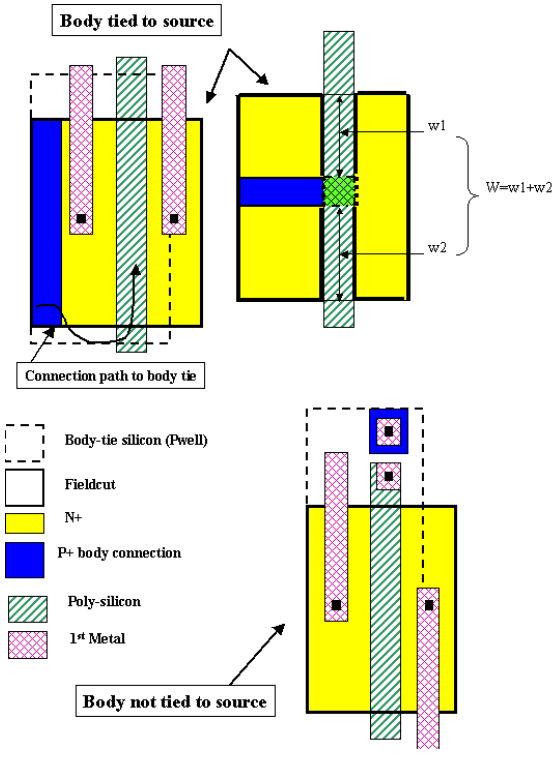

Figure 2: N-channel Body-tie Connections for Partially Depleted SOI

A more area-efficient method for body contact is shown in the top-right portion of figure 1. This method applies only to source-to-body connected devices, but does not employ the "body-tie region" outside of the source-gate-drain area. A minor drawback of this technique is that there is some ambiguity about the "electrical" width of the device and the "drawn" width of the device. The figure shows that "W" may be calculated as the sum of the width of two segments, but this is an inexact calculation due to the geometry of the source that has the embedded body connection. In other words, the transistor width at the source end is different than the transistor width at the drain end of the channel.

Finally, it is not always practical to connect transistors in source-to-body configuration. The lower-right portion of figure 2 shows a connection for a device that can conduct in either direction (i.e., source and drain are inter-changeable).

Resistor / Capacitor Options

For analog circuits two types of resistors are available within the process flow. Resistors made of poly-silicon deposited on field oxide have a target sheet resistance of 100 ohms per square (at 25°C). A thin-film CrSiN resistor option is also available with a sheet resistance of 2500 ohms per square (at 25°C). Normal wafer-to-wafer process variation in sheet resistance on both types of materials is in the range of ±25%. Although this may seem to be a large variation, matching of resistors on the same die can be achieved to as close as 0.1% and therefore designs that depend on resistor ratios rather than absolute values do not require any resistor trimming. Where absolute values of resistance must be controlled to tighter tolerances it is necessary to design and layout serial/parallel combinations of resistors that may be adjusted by cutting out links with a laser at wafer-probe test. Self-heating is another issue where very high levels of resistor matching may be required. It has been determined by high temperature probe characterization that self-heating effects may be avoided for the CrSiN resistors if the current density in the material is limited to approximately 14 micro-amps per micron of resistor width.

Capacitor options are also available within the process flow. Often standard MOS transistors are employed as capacitors by connecting the source-drain-and body terminals together as one terminal and the transistor gate is used as the other terminal. Note that in SOI processes this type of connection is available for both NMOS and PMOS devices. This is a simple means of creating high-density capacitance

on chip, but has the disadvantage that the capacitance varies with voltage when the voltage is applied in a polarity where the area under the gate poly may be depleted (prior to the onset of inversion).

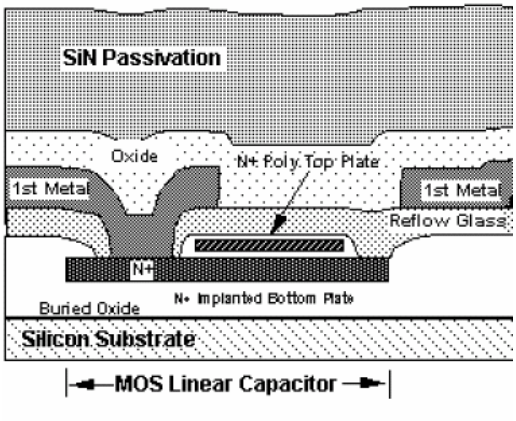

Figure 3: Linear Capacitor Structure

In order to provide a capacitor that does not vary with voltage applied in either polarity, this process incorporates a capacitor "bottom-plate" N-type implant that is integrated as one of the initial steps of the wafer process (see Figure 2). The capacitor dielectric is formed by the same process sequence that forms the gate-dielectric for standard devices, and the top-plate is formed from gate poly-silicon. Since the bottom plate is heavily implanted voltage-dependent depletion spreading under the poly-silicon is minimized and the capacitance is therefore constant with voltage. The "price" for this approach is that the capacitance per unit area is reduced. This is due to the fact that the thermal oxide growth rate is accelerated over the heavily implanted N+ bottom plate, and the dielectric is much thicker than for the standard transistors. Measured capacitance typically is 0.6% lower at 250°C than at 25°C. Measured capacitance variation with voltage is less than 0.03% over ±5V range.

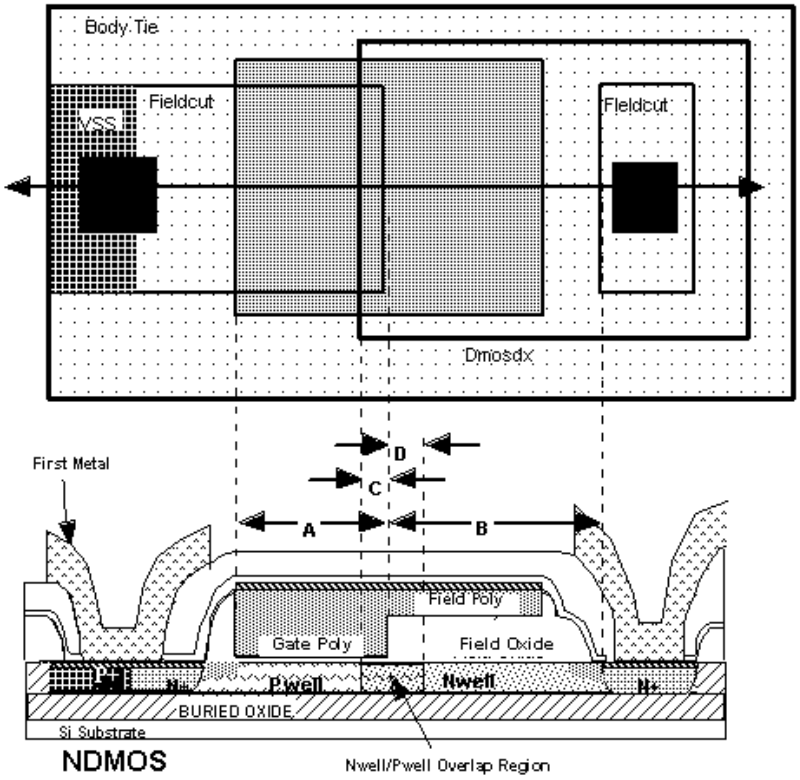

Figure 4: Drain-extended (Lateral DMOS) Construction for an N-channel Device

Extended-Drain (Lateral DMOS) Transistors

A common problem with using conventional digital processes for analog applications is that the analog supply and/or analog I/O may require signal swings that exceed the capability of the digital devices (usually limited by gate-oxide thickness first, and source-to-drain or source-to-body breakdown voltage second). This limitation may be at least partially overcome by layout techniques that emulate "lateral DMOS" approaches previously reported [5]. This technique has been used to develop large transistors with low Rds-on and relatively large drain-to-source hold-off voltage. This technique as it applies to this process is illustrated in Figure 4 for an N-channel device. P-channel devices may also be constructed by "inverting" the N/P type regions shown in Figure 4. The idea is to pull the N+ drain region away from the conducting channel and to extend the drain to the channel using the N-well implant. This is done to minimize the maximum electric field applied across the gate oxide at the drain end of the device.

Unlike a standard device, this layout technique results in a device where the drain implant is no longer self-aligned to the transistor gate. This introduces layout sensitivities that affect performance. Some critical dimensions are illustrated in Figure 4. These are:

- "A" = Nominal transistor length as defined by the thin-oxide region defined at the source end by the edge of the poly feature, and at the drain end by the edge of the "field-cut" feature.
- "B" = Nominal drain extension as defined by the edge of the "field cut" at the N+ drain contact and by the edge of the "field-cut" feature at the drain end of the transistor channel.
- "C" = Region of N-well implant that extends under the region of thin gate oxide.
- "D" = Region of P-well implant that extends beyond the region of thin gate oxide.

Note that regions "C" and "D" represent an area that is implanted by both N-well and P-well implants, where the net impurity type depends on the implant levels. Also note that none of the Nwell, Pwell, or Field cut regions are "self-aligned" with respect to each other. Alignment sensitivities affect NMOS and PMOS devices somewhat differently.

In order to develop DMOS structures that are practical (given these alignment sensitivities) a semi-empirical approach has been utilized. A test-chip was used to explore a large number of device layouts where the dimensions defined above were varied. Criteria for selecting layouts included the drain-to-source breakdown voltage and the sensitivity of the effective threshold voltage to misalignment. After a first down-selection based on empirical measurement, a process simulator was employed to verify that voltage across the drain oxide remains within process limits under the extremes of DC bias conditions (i.e., conducting and non-conducting devices). Layout rules were then established to fix all of the dimensions. A typical I-V curve (at room temperature) is shown for an N-channel device in Figure 5.

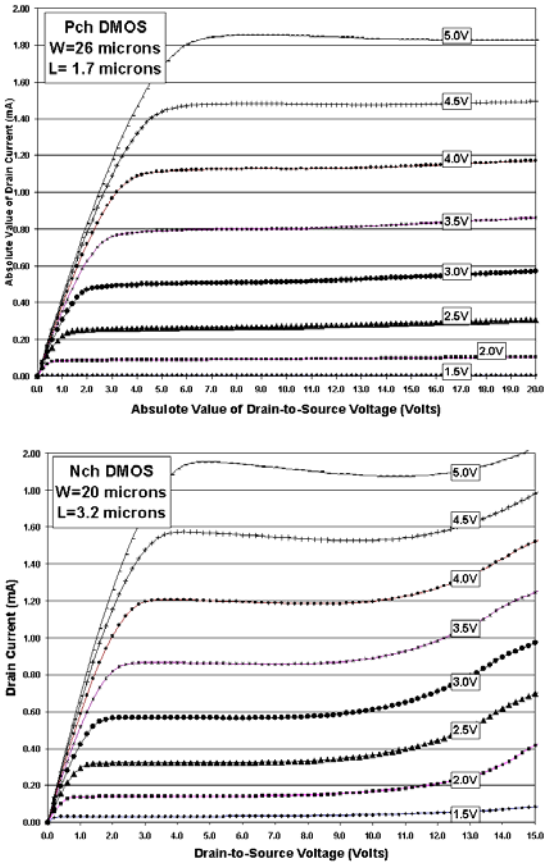

Figure 5: Typical Extended Drain (DMOS) I-V Characteristics

High-temperature characterization and modeling of these devices is currently in progress. Device modeling is challenging, especially for the Nch DMOS device. In addition to self-heating at Gate-to-source voltages >4V, the I-V curves slope upward above about 10V due to high electric field affects. The Pch DMOS device is better behaved. In order to constrain the modeling problem, the DMOS devices are supported on a fixed-length basis (i.e., the models do not scale with transistor length). This should not

be a burdensome constraint for most applications that generally call for devices with a high width-to-length ratio. Wide devices are constructed by arrays of fixed-geometry unit transistors.

Lateral Bipolar Transistors

Lateral bipolar transistors can be fabricated in an SOI process essentially by re-arranging the terminals so that source becomes emitter, drain becomes collector, and body-contact (i.e., Nwell/Pwell) becomes the base terminal. In this case the gate should be connected so that it does not affect device operation (most conveniently accomplished by connecting gate to emitter). Lateral transistors made this way suffer from very high base resistance and are therefore typically limited to very low frequency and/or low-current applications. For this reason it is not expected that lateral bipolar transistors will be used except within band-gap reference circuits. In that case the primary variable of interest is Vbe vs. IC at DC (over temperature). Based on that parameter alone delta-Vbe band-gap voltage references may be constructed [7,8]. Bipolar transistors will be supported for these applications, meaning that schematic symbols will be provided, standard device layouts will be available, and that models for the purpose of DC applications will be provided.

SPICE Modeling

Commercial SPICE simulators and SPICE parameter extraction software support SOI specific models. These help in modeling effects of transistor self-heating, which can be especially important for analog [8]. SOI models also model parasitic bipolar effects, which are not as important when body-tie connections are made according to the layout rules for this technology. An important limitation in extending models to high temperature is that there is usually no accurate means for adjusting junction leakage over temperature or for changing sub-threshold slope characteristics over temperature. For this reason, the approach is taken of fitting the models to the high-temperature data, meaning that the models will be pessimistic for predicting sub-threshold slope and leakage at conventional temperatures.

Summary

A mixed-signal analog/digital process flow has been described that will be supported for high-temperature applications. This process shares many features with a production SOI CMOS process developed for military temperature range. A major difference is the scaling of the threshold voltage so that large digital applications may be supported without un-reasonable "off-current" leakage. In addition, a number of analog features are added including support resistors and capacitors. The process supports 5V operation, 4 layers of metal, and 0.8 micron gate lengths and is viewed as a supportable compromise between digital and analog capabilities. It is intended that the process will be supported including device modeling for high-temperature foundry access.

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Appendix 2

Technology and Tool Kit Development for the U.S. Department of Energy Deep Trek Program

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Introduction

This paper is an update of the high-temperature SOI electronics processes and toolkits that are being developed and utilized under the U.S. Department of Energy (DOE) Deep Trek High-Temperature Electronics program [1]. This program began in late 2003 and is expected to be complete by early 2007. The motivation for the Deep Trek program is to support technology development that makes deep oil and gas drilling economically viable. Down hole data acquisition systems are necessary to make deep drilling and reservoir production cost-effective. High temperature encountered at great depth (>200°C) is the single biggest obstacle for electronic data acquisition systems in very deep wells. Electronics needed in these environments include signal conditioning, A-to-D conversion, digital processing and control electronics, and memory (including non-volatile memory).

Commercial electronics are not designed for these temperatures, and conventional silicon integrated circuit technology is not capable of operating at these temperatures. It is well known that SOI CMOS is a viable alternative to bulk CMOS technology for high temperature [2]. However, most commercial SOI processes are optimized for consumer digital applications (i.e., optimized digital speed/power trade-off). These processes tend to be limited in terms of supply voltage, making analog and mixed-signal applications difficult. In addition, although junction leakage is reduced by SOI, sub-threshold leakage in low-voltage SOI processes may render them unusable for extreme high temperature because of unacceptably high standby current.

Therefore, some tailoring of the process for extreme temperature applications is needed, first to provide capability for analog as well as digital applications, and secondly to deal with sub-threshold leakage in very large digital circuits (memory, microprocessors, etc.). While the need for deep well instrumentation is compelling, and the ability to tap deep oil and gas is clearly in the public interest, electronic component manufacturers have not stepped up to meet this need because of the small market size relative to the investment required. The number of SOI foundries that specifically support high-temperature design (with wafer processes, models, high-temperature qualification, etc.) is very small. This is a major reason for U.S. DOE of support the Deep Trek program.

The specific objectives of the Deep Trek program include development and commercialization of a first set of high-temperature components to be used for down-hole data acquisition and control. These include a precision amplifier, a field-programmable gate array (FPGA), a high-resolution A-to-D converter, and non-volatile memory. To enable this development the Deep Trek program funding also supports the wafer process and design infrastructure which are the topics of this report.

The Deep Trek program uses a High-Temperature SOI (HTSOI) process developed with relatively minor changes to an SOI production-level process developed for high-reliability aerospace applications. In fact, this approach has been in use for some time, and is well established in terms of high-temperature capability [3, 4]. However, while the "baseline" aerospace process has been continuously maintained at production status as equipment and facilities have changed (including transition from 4" to 6" wafers), the HTSOI derivative process had become "out of date". Thanks to the Deep

Trek program the HTSOI process has been updated and re-established at production status. In addition, the Deep Trek program funds have enabled qualification of process/device features to support high temperature analog applications, including on-chip thin-film resistors, capacitors, and lateral bipolar transistors (for voltage reference application). The result is a commercial IC process that is capable both for large-scale digital and precision analog applications operating reliably at 225°C and above [5]. Deep Trek is continuing to fund device research and development to support high-voltage devices and floating-gate memory cells that are needed for high-temperature non-volatile memory.

It is not sufficient just to be able to fabricate high temperature silicon wafers. Front-end design processes and back-end assembly, test, and screening processes must also be supported. Required design support includes the ability to simulate performance over the full operating temperature. The Deep Trek program has developed SPICE models suitable for use up to 250°C. Digital ASIC cell libraries have been characterized for high temperature as well. Design processes are thus developed that support both full-custom analog flows and Hardware-Description-Language (HDL) based digital design flows. These are being employed under the Deep Trek program in the development of mixed analog/digital standard product designs. Standardized wafer test, assembly, and burn-in capability complete the mixed-signal ASIC capability.

High Temp. Wafer Process

Features of the mixed analog/digital process are shown in Table 1. NMOS and PMOS drain current vs. gate voltage curves are shown in Figure 1. These show the "leakage floor" (see the y-intercept of the curves) which increases by 3-orders of magnitude from 25°C to 250°C. It can also be seen that threshold voltage decreases at high temperature (curves shift left) and that the sub-threshold slope decreases. In most commercial SOI processes all of these effects would combine to contribute to "off-state" leakage. In the HTSOI process the threshold voltage is increased relative to the conventional temperature range process. This enables HTSOI to support high-gate-count digital circuits at high temperatures. With this threshold voltage adjustment it can be seen that leakage at high temperature is dominated purely by junction leakage up to 250°C and not increased by sub-threshold conduction.

For analog circuits two types of resistors are available within the process flow. Resistors made of poly-silicon deposited on field oxide have a target sheet resistance of 90 ohms per square (at 25°C). A thin-film CrSiN resistor option is also available with a sheet resistance of 2500 ohms per square (at 25°C).

An optional linear capacitor implant is also available within the process flow (see Figure 2). This results in an MOS capacitor structure where the capacitor bottom-plate is a heavily-doped N-type implant. The capacitor dielectric is formed by the same process sequence that forms the gate-dielectric for standard devices, and the top-plate is formed from gate poly-silicon. Measured capacitance typically is 0.6% lower at 250°C than at 25°C. Measured capacitance variation with voltage is less than 0.03% over ±5V range.

Table 1 : HTSOI Process Features

Process Feature	Typical Characteristics
Gate Oxide thickness	150 angstroms
Minimum transistor length	0.8 microns
Maximum Gate Oxide Voltage	5v
Target Vtn/Vtp 25°C 250°C	1.2V / -1.3V 0.85V / - 1.0V
Sub-Vt slope (mV/dec) 25°C 250°C	NMOS PMOS 150 180 260 320
Transistor "Off current" Nch, 250°C Pch, 250°C	 0.8 nA/micron width 0.5 nA/micron width
# of metal layers	3 or 4
Top Silicon Thickness	0.2 microns
Buried Oxide Thickness	0.4 microns
Partially/Fully depleted	Partially depleted
Poly-silicon resistors	90 ohms per square, 415 ppm/°C
CrSiN resistors	2.5K ohms per square, ± 300 ppm/°C
Linear Capacitor	670 angstroms, <150 ppm/Volt
Laser trim fuse links	Yes
Lateral PNP VREF	For delta-Vbe voltage reference generator only.

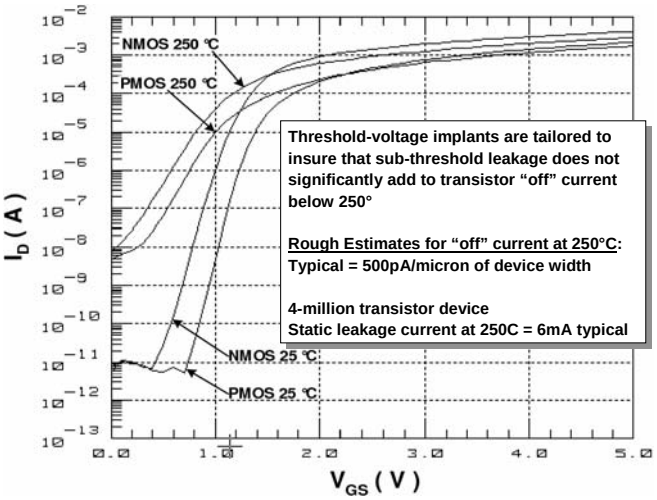

Figure 1: Log ID vs. Vgs for a 10/0.8 micron device at VDS=5V

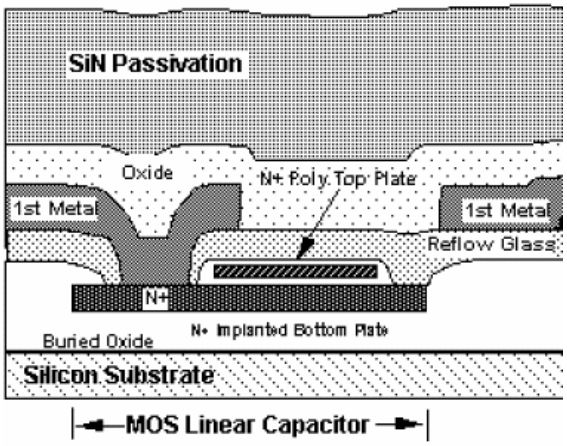

Figure 2: Capacitor Structure

One of the components to be developed under the Deep Trek program is a non-volatile memory. This will be based on data storage using a floating-gate device structure. To generate the tunnelling current to program/erase the memory bits will require the generation and switching of voltage on-chip that are on the order of 12V to 15V. This is beyond the capability of the standard transistors. This limitation may be overcome by layout techniques that emulate "lateral DMOS" approaches. The idea is to pull the N+ drain region away from the conducting channel and to extend the drain to the channel using the N-well implant (see Figure 3). This is done to minimize the maximum electric field applied across the gate oxide at the drain end of the device.

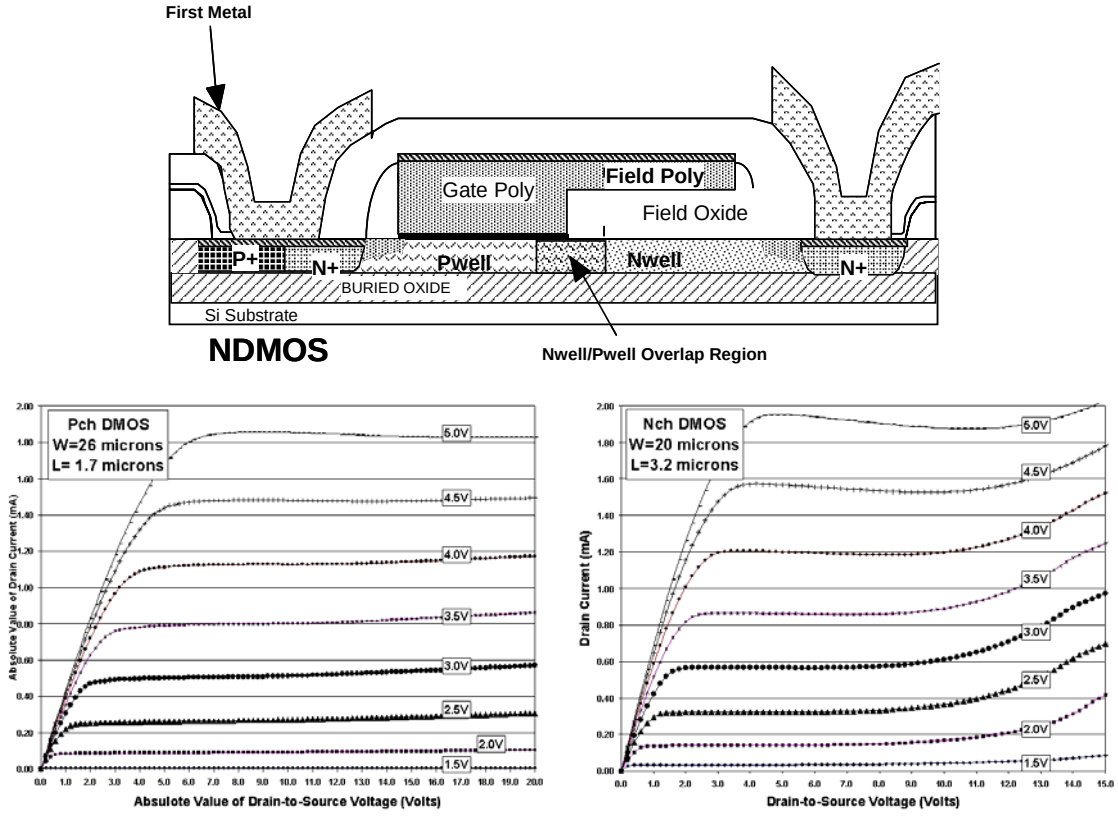

Figure 3: Extended Drain (DMOS) I-V Characteristics

I-V curves (at room temperature) are shown for an N-channel and P-channel devices in Figure 3. The I-V characteristics of these devices are strongly dependent on layout geometry. For the non-volatile memory application DMOS devices at much

narrower widths will be required relative to the devices shown in Figure 3. Work is in progress to characterize and model DMOS devices of various geometries in order to optimize the layout for the non-volatile memory application.

Lateral bipolar transistors can be fabricated in a partially depleted SOI process by re-arranging the terminals of the MOSFET so that source becomes emitter, drain becomes collector, and body-contact (i.e., Nwell/Pwell) becomes the base terminal. In this case the gate should be connected so that it does not affect device operation (most conveniently accomplished by connecting gate to emitter). Lateral transistors made this way suffer from very high base resistance and are therefore typically limited to very low frequency and/or low-current applications. For this reason it is not expected that lateral bipolar transistors will be used except within band-gap reference circuits. They can also be used to generate bias current and/or voltage sources with PTAT (Proportional To Absolute Temperature) characteristics. Characteristics for a bandgap reference circuit are shown in Figure 4.

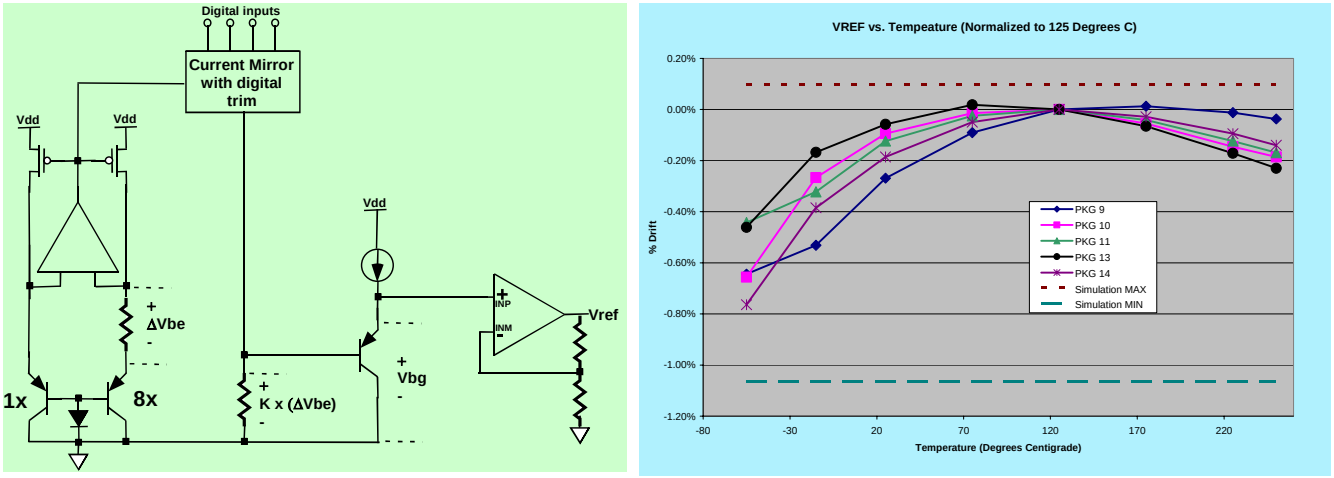

Figure 4 : Bandgap Voltage Reference Using Lateral PNP Transistors

Wafer Process Development Summary

Under the Deep Trek electronics program the HTSOI process has been fully re-characterized at the device level. This included running multiple wafer-lots containing device-level characterization structures so that statistical process variation is established and used to form criteria for wafer-lot acceptance as well as simulation. This update was necessary since many equipment and process flow changes had taken place since the initial high-temperature process work was completed for digital applications only. These process flow changes, including the conversion from 4-inch wafers to 6-inch manufacturing, made it risky to use existing SPICE models and digital timing parameters. The process changes also included the addition of 4th layer metal, and incorporation of analog process enhancements already discussed. As a result the HTSOI wafer process has been fully upgraded to production status.

ASIC Design Infrastructure Features and Flow

The HTSOI wafer process used by the Deep Trek program is layout-rule and photo-mask compatible with Honeywell's military temperature range aerospace technology. This has made it possible to leverage previously developed gate array platforms and design processes for digital ASICs and to provide Deep Trek program participants with a complete high-temp ASIC design platform [6]. This existing SOI ASIC infrastructure includes fully supported pad frames, under-layers, probe cards and packages that are available for the high-temp community to support new analog, digital and mixed signal chip ASIC designs. These allow high-temp devices having the features outlined in Table 2 to be designed and fabricated.

Honeywell's HTSOI ASIC design flow can be used to develop ASICs having almost any combination of analog and digital blocks. These capabilities range from full-custom analog to mixed analog and digital to completely digital ASICs. Analog designers have access to a library of SPICE primitives as well as a small library of digital cell primitives to use when implementing their designs. For digital designs, Honeywell's HTSOI4 digital cell library has been fully characterized for operation over the -55°C to +250°C temperature range. For the Deep Trek program, the "nominal" operating condition has been assumed to be +175°C and timing models are specifically developed to represent this typical condition as well as the other temperature extremes. Standard digital flows provide support for many industry standard digital tools. Full

custom analog and digital blocks can be dropped into the gate array and verified by simulation and layout verification tools. The gate array toolkit has been tailored to incorporate multiple power-supply domains, allowing for separation of analog vs. digital supplies. This includes separation of ESD protection networks which are otherwise a means for supply coupled crosstalk between analog and digital domains. The design libraries, tools and flows were proven out during the implementation of a mixed signal Sigma-Delta A-to-D converter developed by the Deep Trek program.

Table 2: High-Temperature ASIC Features

Product	Total Gates	Maximum Packaged Signal I/O	Max Available Signal I/O	Usable Gates 3 Metal Layers	Usable Gates 4 Metal Layers
HT2080	84,512	172	176	52,000	72,000
HT2160	159,528	240	240	91,000	126,000
HT2300	295,392	320	336	156,000	216,000
HT2400	389,120	320	338	200,000	275,000

Different design flows are used in the implementation of a high-temp ASIC; one design path for the analog block and a separate path for the digital block. Purely analog (or full-custom digital) blocks are implemented using traditional analog tools and processes, including schematic entry and SPICE based simulation methodologies. This is done using a Process Design Kit (PDK) which is an integrated collection of schematic capture symbols, models, layout rules, and other items to allow use of design software available from Cadence. Cadence Virtuoso® Schematic Editor is used for schematic entry. Cadence Spectre® and Ultrasim® are used for analog core simulation. Cadence tools are also used for analog core layout, parasitic extraction, merging analog and digital layout databases and for layout verification.

Meanwhile, purely digital blocks use conventional digital HDL-based development tools and flows. Conventional Honeywell HT2000 ASIC design tools and techniques are used to implement the high-temp ASIC. Digital functions are translated from functional RTL (Register-transfer-level) HDL code into structural gate-level netlists, typically using Synopsys Design Compiler® software. Many HDL simulation tools are available for functional and timing simulation of the synthesized blocks. These are placed and routed in the Gate-array core and loading and routing parasitics are extracted and annotated onto the netlists. Timing is verified using Synopsys Primetime® and timing models specifically developed for fidelity at high-temperatures.

For ASICs implementing a mix of analog and digital blocks, the two parallel and concurrent design paths will converge during mixed mode simulation of the entire chip and again during layout of the complete mixed signal ASIC. Designs are implemented in a hierarchical manner and, in order to simplify the simulation and back-end tool flows, the analog and digital sub-modules of mixed signal ASIC designs are segregated into separate sub-modules and instantiated into a single Verilog netlist module that implements the chip top-level interconnect. Interconnection of the analog and digital cores is verified by the Cadence AMS Designer simulator or other mixed mode simulation tool. Physical layouts of the analog and digital sections are merged to construct the final top-level chip layout.

The complete design can consist of a number of component blocks including an analog core, embedded custom SRAM, digital sub-blocks, I/O and top-level interconnect blocks. It may also include digital scan chain (inserted by software to enable Automated Test Pattern Generation, ATPG) and clock and reset multiplexing implemented using a mix of VHDL and Verilog languages. Note that VHDL RTL designs are converted to Verilog during logic synthesis to provide a consistent netlist for back-end tools and to allow for mixed mode simulation using cell primitives

In addition to supporting 3rd party software from a variety of CAE tool vendors, the design flow also incorporates proprietary software (i.e., specific to Honeywell's ASIC family) that check for loading violations, violations of electro-migration current density rules (limits are tailored specifically for high-temperature use), digital edge-rate violations, I/O placement errors, etc. The supported CAE tools help maintain highest design quality and help ensure an error free design.

Results: Sigma-delta A-to-D Converter Design Implementation

The design and process infrastructure developed for the Deep Trek High-Temperature Electronics Program have been used to develop a mixed-signal ASIC implementation of a high temperature sigma-delta A-to-D converter (Figure 5). This A-to-D includes the sigma-delta modulator, on-chip voltage reference, digital filters, and serial interface. It is implemented using the HT2160 gate-array with custom analog drop-in section and multiple power-supply domains. This design is currently in wafer fabrication and testing is expected to begin during fourth quarter of 2005.

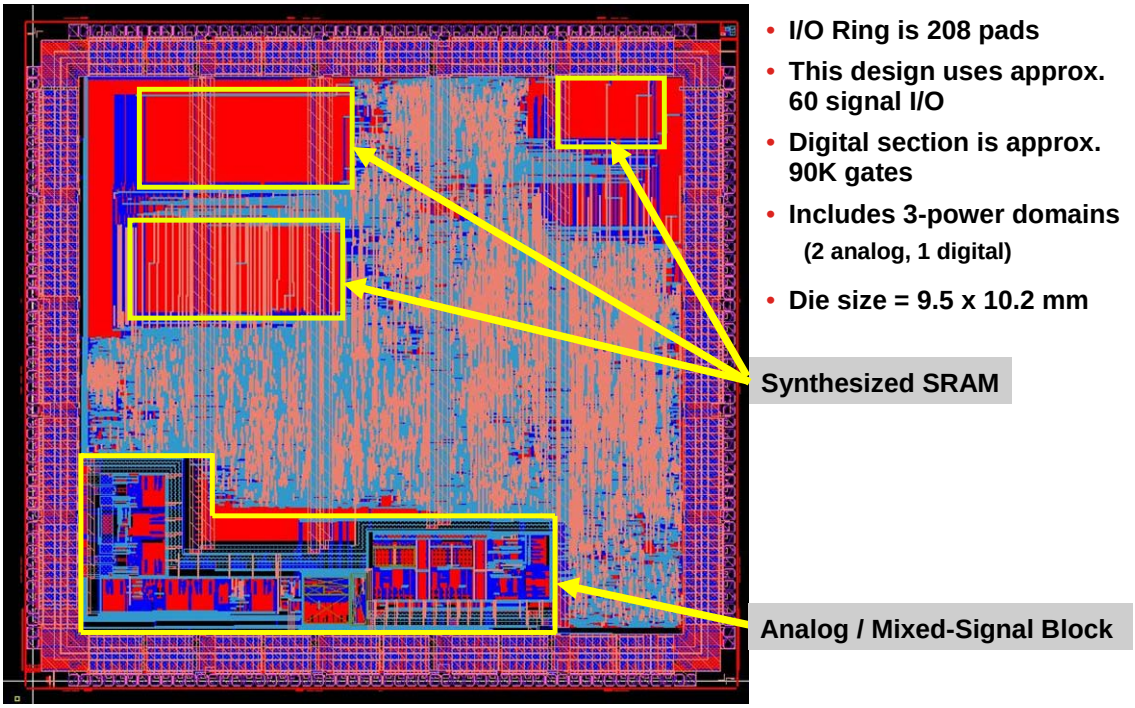

Figure 5: A-to-D Converter Layout

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Appendix 3

High Temperature Precision Amplifier

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Abstract

Signal conditioning amplifiers are needed for down hole oil and gas data acquisition, especially for buffering high-impedance sensors. A dual high-temperature precision amplifier has been developed for down hole instrumentation, offering very low input offset voltage and drift, and 1/f noise suppression. The amplifier has been developed as a commercial, standard product offering in a ceramic DIP package, meeting requirements for operation from -55° to 225°C. All necessary auto-zero clock signals are generated internally, and no external capacitors are needed. The amplifier is completely self-biasing. Offsets at 250°C are typically less than 10 micro-volts, and input noise from 0.1 to 10 Hz is typically 5 micro-volts pk-pk. This makes this amplifier suitable for input conditioning for high-resolution DC or low-frequency applications. This design has been developed under the U.S. Dept. of Energy Deep Trek program.

1. Introduction

Signal conditioning amplifiers are needed in down-hole oil and gas data acquisition tools, especially for buffering high-impedance sensor outputs. Many applications involve DC-coupled sensors. When used in high-resolution data acquisition systems, low input offset current, very low offset voltage and good low-frequency noise response are primary considerations. For High-Temperature High Pressure (HTHP) wells these characteristics must be maintained at the high-temperatures encountered down hole.

Bulk CMOS amplifiers for high-temperature applications have been demonstrated [1-3]. One of these specifically addresses low-input offset voltage [4], reporting less than 200μV of offset voltage and 1nA of leakage up to 200°C. In general these require special design technique and expertise to overcome leakage and/or latch-up issues at high-temperature using bulk CMOS. It seems that there are no bulk-CMOS commercial offerings with established long-term reliability for temperatures above 200°C. More recently, activity in high-temperature amplifiers and signal conditioning circuits has exploited the superior high temperature behaviour of SOI CMOS to reduce leakage and eliminate device latch-up. [5-7]. However, the specific issues of low input offset voltage (and current), and low 1/f noise for DC/low-frequency applications have not been fully addressed in SOI CMOS.

This paper reports results for an SOI CMOS precision amplifier chartered by the High-Temperature Electronics Project under the U.S. Department of Energy (DOE) DeepTrek program. This program targets high-temperature electronic components needed for the development of very-deep HTHP oil and gas reserves. Industrial partners are involved in this program as a Joint Industrial Participation (JIP) consortium. The JIP prioritizes component development and determines target specifications. For this precision amplifier JIP development priorities are very-low input offset voltage and current, low noise especially for DC to 100Hz. signals, long-life and high reliability, and operating temperature range to at least 225°C (ambient). In addition, power consumption should be kept to a minimum. This should be achieved without reliance on external components (especially capacitors that are hard to find for these operating temperatures). It is a primary DOE objective that the components developed under this project should be available as commercial offerings at the conclusion of the program.

2. Design and Application Considerations

As with all of the components that are being developed under the DeepTrek High Temperature Electronics program, this development was completed using a partially-depleted High-Temperature SOI (HTSOI) CMOS process [8]. This is a 0.8μ, 5-

volt process that includes optional linear capacitor implant, lateral PNP bipolar transistor for reference/bias current generation, and thin-film CrSiN resistors. The SOI characteristics are used to achieve low-leakage and low-input bias current at high temperature. This technology has a track record of proven reliability for high-temperature applications. To achieve long operating life of the on-chip inter-connect (primarily aluminium) maximum current-density rules are applied to the layout.

Means for continuous compensation of offset-voltage and 1/f noise are required. A ping-pong architecture was selected which does not require that the auto-zero clock frequency is higher than the input signal bandwidth. Therefore, the amplifier may be used for applications beyond DC coupled/low-frequency signal conditioning. It is still the case that the output signal spectrum will have some content at the clock-frequency. Depending on the input signal and/or system application it is not clear if this is an issue. In any case, it is very desirable that clock-generation for offset compensation should be accomplished on-chip. Any capacitors required for offset compensation should be provided on-chip.

Power management is a trade-off vs. many other performance characteristics (such as drive current, slew-rate, bandwidth, etc.). Since many applications require only periodic measurement, duty-cycling may be used as a means to manage power without significantly compromising other parameters. Therefore it was decided to implement a "shutdown" feature to put the entire amplifier in a low-current mode with a high-impedance output.

A dual amplifier configuration was chosen for development. The project also included developing a custom package layout optimized for low-offset and isolation of the inputs between amplifiers and from digital noise. At the same time, it is expected that wafer/die level screening at high temperature will support delivery in die form. The intention is that this shall be a fully independent component suitable for production manufacturing including incorporation of ESD protection, short-circuit current limit, and capability for driving reasonable resistive or capacitive loads. A summary of the design goals arrived at by consensus among the JIP partners is shown in Table 1.

TABLE 1 : Precision Amplifier Design Targets for -55°C to 225°C

Parameter	Target Value
Input Offset Voltage	100 μV maximum
Mean Input Offset Voltage Drift	0.2 μV/°C maximum
Input Bias Current @ 225°C	±150 nA,
Input Offset Current @ 225°C	±1nA,
Input Noise Voltage RS=100Ω, 0.1Hz – 10Hz	3 μV pk-pk
Input Noise Current @ 225°C	1.0 pA/√Hz
Input Range	V_{SS} to V_{DD} -2.0
Common Mode Rejection Ratio (DC)	100 dB, minimum
Power Supply Rejection (DC)	100 dB, minimum
Large Signal Voltage Gain (DC); RL = 10kΩ	100 dB, minimum
Gain-Bandwidth Product; RL = 10kΩ, CL = 20pF	2.0 MHz
Slew Rate; RL = 10kΩ	1.5 V/μs (typical)
Output Source/Sink (swing to 0.3V from either rail)	±20 mA
Output Short-Circuit Current Limit	±50 mA
Operating Supply Range	5.0 Volts, ±5%
Supply Current, Total Package	5.0 mA, maximum
Supply Current with Shutdown asserted	150 μA, maximum

3. Implementation

The ping-pong architecture follows that described by Opris and Kovacs [9]. Operation is illustrated in Figure 1. The ping-pong amplifier consists of two matched transconductance input amplifiers, A1 and A2. Each amplifier contains a primary pair of differential inputs, an auxiliary pair of differential inputs, and a single-ended output. The primary inputs handle the externally applied input signals, while the auxiliary inputs handle the internal offset voltage correction signal. Capacitors C2 and C4 store the offset correction voltages for A1 and A2, respectively, while capacitors C1 and C3 store a reference voltage level. A two-phase, non-overlapping clock provides the necessary switch timing.

A1 and A2 are alternately auto-zeroed: When A1 is being auto-zeroed, A2 is switched into the main signal path and provides amplification; when A2 is auto-zeroed, A1 is switched into the main signal path and provides amplification. Thus, the overall amplifier "ping-pongs" between A1 and A2, providing a continuous signal path from input to output.

The outputs of A1 and A2 are alternately switched to a common output node C, which in turn is connected to an output buffer stage A3, which provides the overall amplifier output. A3 provides rail-to-rail output swing with ±50mA drive capability over temperature.

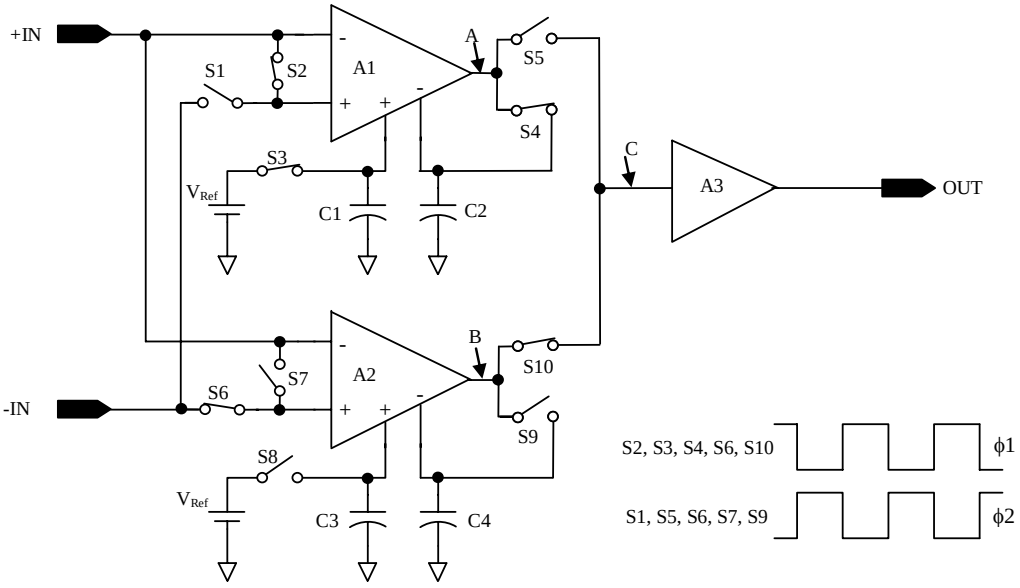

FIGURE 1 : Ping-Pong Amplifier Block Diagram

Figure 1 shows A1 being auto-zeroed, while A2 is "online" as the main signal amplifier. When A1 auto-zeroes, S2 closes, shorting together the main inputs of A1. S1 simultaneously opens (preventing the input terminals from shorting), while S3 and S4 also close. S3 connects a voltage reference to A1's (+) auxiliary input, while S4 connects A1's output, node A, to the (-) auxiliary input. This creates a unity-gain feedback loop and node A goes to approximately Vref. C2 charges to this voltage.

At the end of the auto-zero cycle, S3 and S4 open, storing the reference voltage and offset correction voltage on capacitors C1 and C2, respectively. The difference between the voltages on these capacitors ($V_{C1} - V_{C2}$) is the offset correction voltage, and is applied directly to the auxiliary differential inputs. A1 has now been auto-zeroed. The auto-zero procedure for A2 proceeds in an identical manner. This block diagram serves to describe the operation of the Ping-pong amplifier. However, it is a simplified block diagram in that additional circuitry to reduce switching transients at the output is not shown.

Note that the SOI technology is a key enabler for this design. A primary limitation in the offset accuracy is the leakage on the offset/reference storage capacitors. In this symmetrical architecture C1 and C2 experience similar magnitude of leakage, and thus the drift at the auxiliary inputs is largely common mode rather than differential. It is also highly beneficial that on-chip SOI switches and capacitors have much lower leakage than they would in a bulk technology.

A block diagram of the complete chip, the die layout, and the 14-pin DIP pin assignment are shown in Figure 2. The amplifier chip is completely self biasing. Within the bias generator block is a current source that provides PTAT (Proportional To Absolute Temperature) bias currents to the amplifiers. The PTAT characteristic is derived in a conventional manner using lateral PNP bipolar transistors operated at different current densities. This develops a ΔV_{be} mismatch between the two devices that has a PTAT characteristic. This PTAT voltage is converted to current by replication across a thin-film CrSiN resistor using a feedback loop. The PTAT current is mirrored as needed around the chip to bias the amplifiers. By properly sizing the input devices within the amplifiers, they can be operated in weak-inversion where the transconductance (gm) is almost inversely proportional to temperature. At the same time, gm is roughly proportional to PTAT bias current, and thus remains nearly constant over temperature. Consequently, PTAT bias renders the overall amplifier bandwidth roughly independent of temperature so that uniform and stable operation is achieved over a very wide temperature range.

The amplifier is also completely self-contained in terms of clock generation for operating the amplifier switches. An on-chip R-C oscillator provides the time base for switching. High precision is not required. However, a general concern in using this architecture and of having the digital clock switching on the same chip is the amount of clock noise that feeds through to the output, and the effect that it may have on the effectiveness of the offset compensation. To avoid discrete frequency spurs at the output, a frequency randomizer is part of the clock generation. The on-chip oscillator runs at a base frequency of roughly 4MHz. This is "randomized" using a pseudo-random sequence generator in the frequency divider chain resulting in a switching frequency that randomly varies between roughly 2KHz to 4KHz. This feature can be defeated (i.e., switching at a single discrete frequency) by the RND control signal.

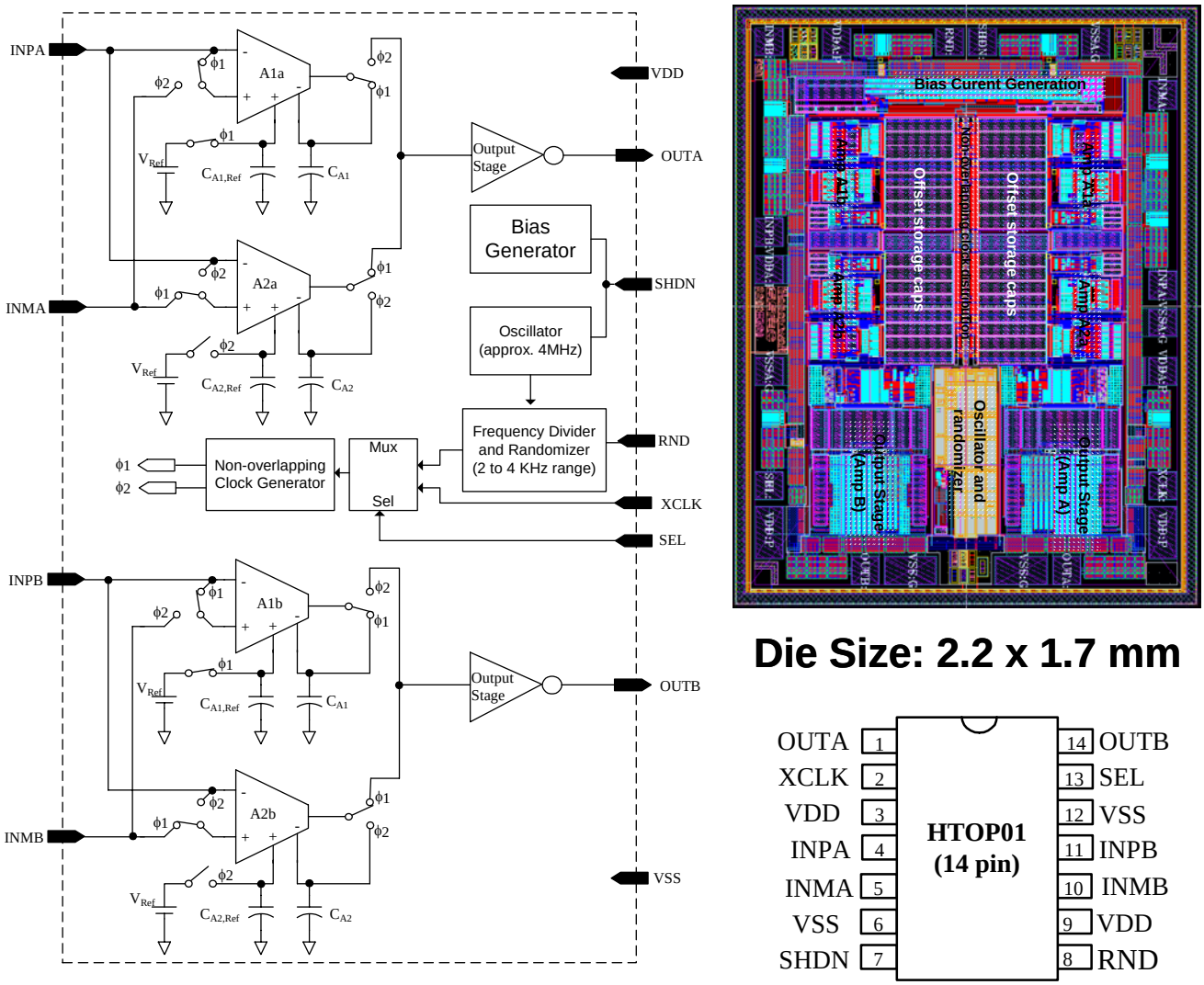

Figure 2: Full-chip Block Diagram, Die Layout, and 14-pin DIP Pin-Out

A "Select" pin provides means for selecting an external clock source in lieu of the on-chip clock. This may be advantageous in sampled data systems where the output of the amplifier is synchronously sampled by a down-stream component (e.g., an A-to-D). It also provides a convenient means for characterizing the amplifier response to different clock frequencies. Although not shown in the diagram, it is the case that when the external clock is selected, the internal oscillator and frequency divider are shut off. This makes it possible to determine the impact on accuracy of digital noise from on-chip clock generation relative to providing an off-chip clock source.

Careful attention was paid to layout for both the chip and the package. Digital functions are physically separated from the analog inputs, and on-chip power-supply routing is kept separate for analog and digital sections. ESD protection networks are matched and inter-digitated to reduce input leakage current mismatch as much as possible. The power-supply and output routing for the amplifier outputs are physically sized to handle the currents required without risk for failure from electro-migration at high temperature.

4. Results

A proof lot of the high temperature amplifier has completed fabrication and testing. Wafer probing was completed using a hot-chuck at 200°C centigrade, follow by package assembly in 14-pin DIP and automated testing at -55°C, 25°C, and 225°C (Thermo-stream® air temperature). This has been supplemented by laboratory bench testing for various parameters. Results are shown in Table 2 and Figure 3.

Automated offset voltage measurement of 47 packages using the internal clock verifies that offset voltage is within the 100μV target over the full temperature and input range. Bench testing on a sample basis shows that offset voltage performance is significantly improved by using an external clock. Typical measured offsets are less than 1μV at room temp. and within ±5μV over the full operating range when an external clock is used. Measurement of offset at these levels requires careful attention to the test set-up, especially using an external clock source. Sandia National Laboratory completed testing at 300°C (Figure 3a) after 438 hours of 300°C operation (117 hrs. in 5% hydrogen atmosphere). Results show the offset is still within 10μV up to about 2.25V input. Above 2.25V there is a curious spike in the offset voltage (up to 24μV) that is not yet explained. These results were obtained using an external clock at 3KHz.

The noise behaviour of the amplifier is also very interesting. Figures 3c and 3d show noise characteristics vs. temperature and clocking frequency respectively. It can be seen that the noise performance actually improves at 225°C relative to lower temperatures. Furthermore, it can be seen that low-frequency noise suppression is improved as the clock frequency increases from 1KHz. At about 30KHz. the 1/f noise is suppressed to approximately the wide-band channel noise level of the amplifier. Interesting noise characteristics are also observed (depending on test apparatus) when using the internal clock. Figure 3a used the internal clock and showed a flat noise response. Figure 3b also includes a curve using the internal clock but shows a peaking in the noise characteristic at about 100Hz. This remains to be fully explained. More testing will need to be completed to validate and refine these results.

TABLE 2 : Selected Package Test Data (-55°C to 225°C) unless noted

Parameter	Target Value	Measured Results
Input Offset Voltage	±100 μV (max.)	±5 μV (external clock)
Supply Current (5.25V supply, 225°C)	5 mA	1.85 mA
Open-loop Gain (-55°C to 225°C)	> 100dB	> 114dB
Input Noise Voltage RS=100Ω, 0.1Hz – 10Hz (internal clock) (External clock at 30KHz)	3 μV pk-pk	5.7 μV pk-pk @ 23°C 4.6 μV pk-pk @ 225°C 1.4 μV pk-pk @ 23°C
Input Noise Current @ 225°C	1.0 pA/√Hz	To be measured
Input Range	V_{SS} to V_{DD} -2.0	V_{SS} to V_{DD} – 1.7
Output Source/Sink (swing to 0.3V from either rail)	±20 mA	> 20 mA
Output Short-Circuit Current Limit	±50 mA	51 mA (average)
Supply Current with Shutdown asserted	150 μA, maximum	13 uA, typical

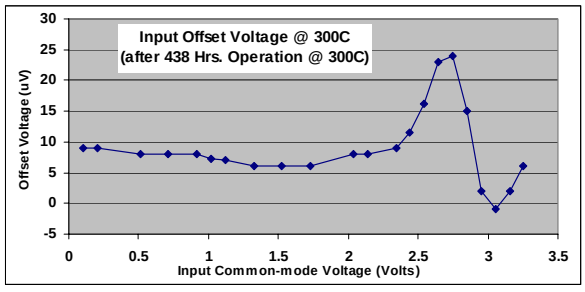

Figure 3a

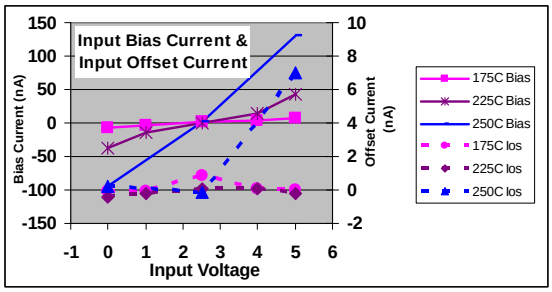

Figure 3b

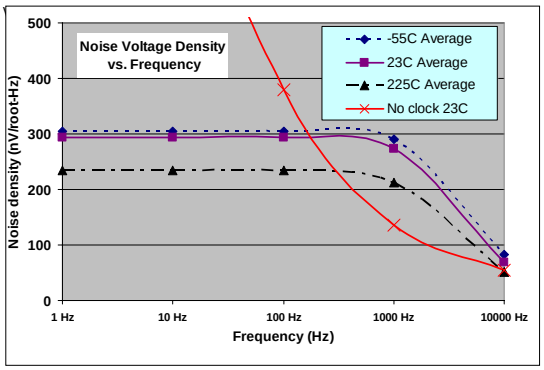

Figure 3c

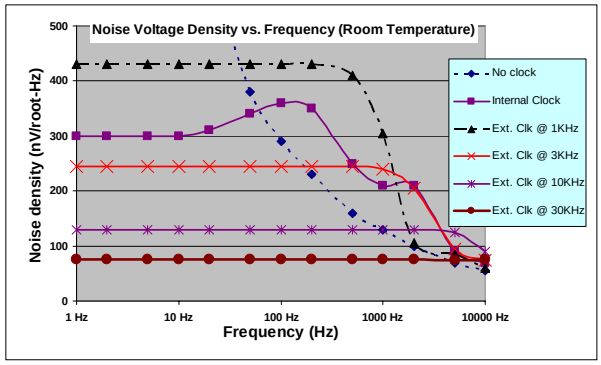

Figure 3d

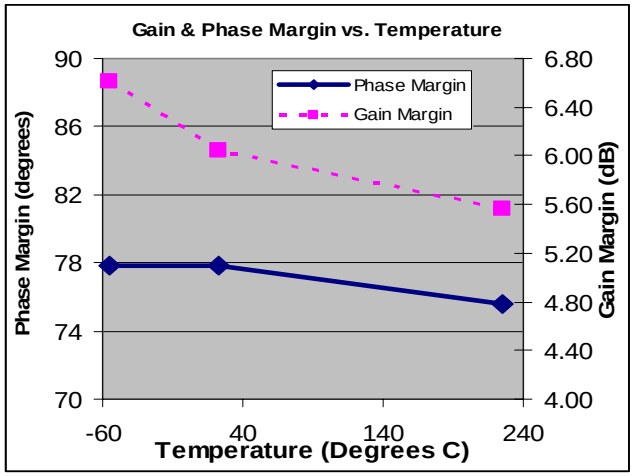

Figure 3e

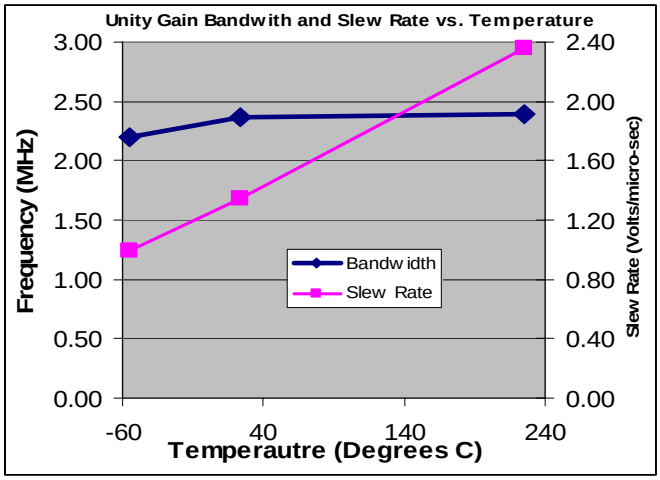

Figure 3f

5. Summary and Conclusion

A dual high-temperature precision amplifier requiring no external component has been successfully developed and demonstrated at temperatures ranging from -55°C to 300°C. Excellent offset performance, low offset drift with time and temperature, and effective suppression of 1/f noise make this amplifier suitable for use in high-temperature precision DC and/or low-frequency applications. However, it is apparent that performance is improved by using an external clock source at higher frequencies relative to the internal clock. This suggests that low-frequency noise suppression could be further improved by simple changes to the design (by increasing the internal clock frequency, for example).

Acknowledgements

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Appendix 4

Progress Update on Honeywell's Deep Trek High Temperature Electronics Project

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Abstract

The U.S. Department of Energy's Deep Trek program focuses on development and commercial application of drilling and completion technologies in order to recover deep oil/gas resources. Under this program Honeywell, in collaboration with a consortium of industrial partners, is applying Silicon-On-Insulator (SOI) CMOS technology to develop electronic components that operate reliably in very hot (>225°C) environments to support deep well drilling. The program was awarded in 2003 and concludes in mid-2007. In additon to the SOI process, the program scope includes high temperature simulation models, design toolkits, and libraries for new component development. The program is developing an EEPROM, a Field-Programmable Gate Array (FPGA), a dual precision operational amplifier, and a high resolution (18-bit) analog-to-digital converter. These components are developed for reliable long-term operation (15-years at 150C, 5 years at 225C). A simple system controlled by a Field Programmable Gate Array (FPGA) and Electrically Erasable Programmable Read-Only-Memory (EEPROM) can support down-hole data-logging applications. The FPGA is SRAM-based with an 80 X 80 array of programmable logic blocks (30,000 usable gates) and is ideal for use as reconfigurable coprocessor or other computationally intensive logic structures. The FPGA is functionally equivalent to the AT6010 made by ATMEL® Corporation. The EEPROM, which is in development, will be used to store FPGA configuration data. The FPGA will also be able to write and read to/from the EEPROM for data logging purposes. The EEPROM organization is 32k X 8-bits and can be configured as a functional equivalent to 28C256 parallel interface EEPROM or 25C256 SPI serial interface EEPROM. Circuitry in the EEPROM and FPGA allows synchronization of power-on initialization and configuration to guard against "dirty" power environment operation. This paper provides an update on the progress of the program, as well as discussion of additional high-temperature electronics component and infrastructure needs and outlook.

Key words: High-temperature electronics, EEPROM, FPGA, Analog-to-Digital Converter, Amplifier

1.0 Introduction

Deep oil/gas reservoirs are still not being developed for lack of data acquisition tools that handle the heat in the well. In addition, post-completion production controls that could enable more complete extraction and production efficiency cannot be deployed because electronics are not available that operate reliably for long periods (years) at even moderately high temperature (above 150°C). Prior experience and currently funded programs have established that viable electronics technology exists for 250°C and above, and is available now [1-13]. Yet this doesn't achieve its highest impact if critical components needed to build a complete, useful system are missing. Additional development and commercialization are required to "complete the system" so that new tools can be developed for deep well domains.

This paper is an update of a High-Temperature Electronics (HTE) project operating under the umbrella of the U.S. Dept. of Energy's DeepTrek program [14-15]. The Deep Trek initiative focuses on development of drilling and completion technologies operating in the high temperature (>250°C) environments of deep wells. Electronics needed in these environments include signal conditioning, A-to-D conversion, digital

processing and control electronics, and memory (including non-volatile memory). DeepTrek projects are administered by the Strategic Center for Natural Gas (SCNG), an organization of the National Energy Technology Laboratory [16].

2.0 Program Objectives and Organization

The specific objectives of the Deep Trek program include development and commercialization of a first set of high-temperature components to be used for down-hole data acquisition and control. These include a precision amplifier, a field-programmable gate array (FPGA), a high-resolution A-to-D converter, and a non-volatile memory (EEPROM). Deep Trek program funding has also supported the prerequisite wafer process and design infrastructure that are being used in these component developments.

The program scope and the components in development have been defined and specified in collaboration with a consortium of industrial partners within a Joint Industrial Participation (JIP) organization. Current JIP members are Baker-Hughes, BP America, Goodrich Aerospace, Honeywell, Intelliserv, Quartzdyne, and Schlumberger.

3.0 Development Activity

3.1 Wafer Process Technology and Design Tools

At best, it is very difficult to use conventional bulk-silicon integrated circuit technology at temperatures above 150C, and nearly impossible above 200C. Primary operation is constrained by leakage current from PN junction isolation. In addition, today's low-voltage CMOS electronics employ short-channel transistors that have elevated sub-threshold leakage current at high temperatures.

It is well known that Silicon-On-Insulator (SOI) CMOS is a viable alternative to bulk CMOS technology for high temperature, since SOI CMOS has inherently reduced junction leakage. However, most commercial SOI processes are optimized for consumer digital applications (i.e., optimized digital speed/power trade-off). These processes tend to be limited in terms of supply voltage, making analog and mixed-signal applications difficult. In addition, although junction leakage is reduced by SOI, sub-threshold leakage in low-voltage SOI processes may render them unusable for large-scale IC's at extreme high temperature because of unacceptably high standby current.

Therefore, some tailoring of the process for extreme temperature applications is needed, first to provide capability for analog as well as digital applications, and secondly to deal with sub-threshold leakage in very large digital circuits (memory, microprocessors, etc.).

The Deep Trek program uses a High-Temperature SOI (HTSOI) process developed with relatively minor changes to an SOI CMOS process developed for aerospace applications. Among the changes is an adjustment of transistor threshold implants to manage sub-threshold leakage at 250°C. Standby leakage can be kept to a few milliamps for a 4-million transistor IC. Without threshold adjustment leakage current could be at least an order of magnitude higher. Deep Trek program funds have also been used to insert and qualify analog devices, including on-chip thin-film resistors, capacitors, and lateral bipolar transistors (for voltage reference applications). The result is a production commercial IC process that is capable both for large-scale digital and precision analog applications operating reliably at 225°C and above [17]. Some of the important features of this technology are listed in Table 1.

Table 1: HTSOI Process Features

Process Feature	**Typical Characteristics**
Gate Oxide thickness	150 angstroms
Minimum transistor length	0.8 microns
Max. Gate Oxide Voltage	5V
Target Vtn/Vtp 25°C 250°C	 1.2V / -1.3V 0.85V / - 1.0V
Sub-Vt slope (mV/dec) 25°C 250°C	NMOS PMOS 150 180 260 320
Transistor "Off current" Nch, 250°C Pch, 250°C	 0.8 nA/micron width 0.5 nA/micron width
# of metal layers	3 or 4
Top Silicon Thickness	0.2 microns
Buried Oxide Thickness	0.4 microns
SOI: Partially/Fully depleted	Partially depleted
Poly-silicon resistors	90 ohms per square, 415 ppm/°C
CrSiN resistors	2.5K ohms per square, ± 300 ppm/°C
Linear Capacitor	670 angstroms, <150 ppm/Volt

The HTSOI wafer process used by the Deep Trek program is layout-rule and photo-mask compatible with Honeywell's military temperature range aerospace technology. This has made it

possible to leverage previously developed gate array platforms and design processes for digital ASICs. This provides Deep Trek program participants with a complete high-temp gate-array design platform. An HTSOI gate-array digital cell library has been fully characterized for operation over the -55°C to +250°C temperature range. Available high-temperature gate-array platforms are summarized in table 2.

Table 2: High-Temperature ASIC Features

Gate-Array Product	Total Gates	Maximum Packaged Signal I/O	Usable Gates 4 Metal Layers
HT2080	84,512	172	72,000
HT2160	159,528	240	126,000
HT2300	295,392	320	216,000
HT2400	389,120	320	275,000

Purely analog (or full-custom digital) blocks are implemented using commercial analog tools and processes, including schematic entry and SPICE based simulation methodologies. To extend these methods to high-temperature, HTSOI transistors have been characterized and SPICE models developed that are optimally fit to data obtained at 175°C to 250°C. This enables high-accuracy transistor-level simulation for high-temperature analog and digital circuit blocks.

The HTSOI process and design tools can therefore be used to develop components combining of analog and digital blocks and their associated design flows. Under the DeepTrek program, the technology and design infrastructure have been used to develop custom analog, digital, and mixed-signal analog/digital components for high-temperatures.

3.2 Deep Trek High-Temperature Components

High-temperature data acquisition and/or control systems are needed to make deep oil and gas drilling and production cost-effective. Figure 1 shows a conceptual block diagram of a generic data acquisition and control system. The Deep Trek High-Temperature Electronics program aims to develop (and commercialize) components that may serve as key building blocks in such a system.

In addition to high-temperature gate array family that has already been discussed, this project is under-taking the development of four high-temperature standard-products. These are:

- HTOP01: A dual precision operational amplifier
- HTFPGA: 30K-gate field programmable gate array
- HTEEPROM: 256Kbit electrically-erasable programmable read-only memory
- HTADC18: high-resolution (18-bit) analog-to-digital converter.

Insertion of these components into the target oil and gas (or other high-temperature) application is shown by the blue items in Figure 1. All of the components and technology in the program are being developed to provide 5-year continuous operation at ambient temperatures up to 225°C.

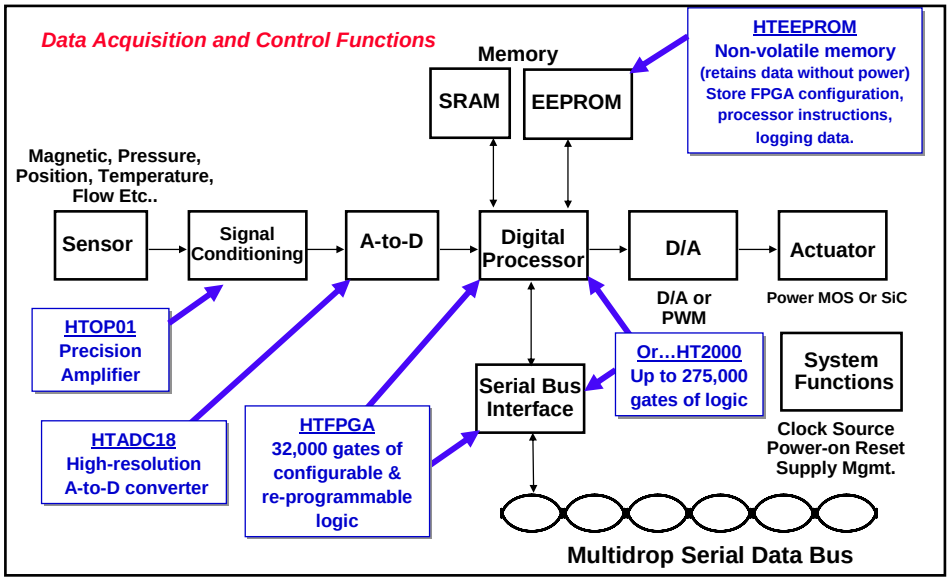

Figure 1: Deep Trek Components Application in a Data Acquisition and Control System

3.3 Precision Amplifier

A precision amplifier is critical for acquisition of low-frequency and/or DC-coupled signals. Amplifiers are used to buffer and scale low-level signals so that they can drive down-stream A-to-D converters and fully utilize the available A-to-D input range. Key challenges for this component include maintaining a very high signal-to-noise ratio (that is, low DC offset + noise) and very high input impedance (so as not to distort the input signal).

The HTOP01 dual precision amplifier of this project continuously and autonomously performs offset and/or low-frequency noise compensation to achieve high DC precision and long-term stability with no external components required for offset compensation. Features include:

- Low-power (sleep) mode, invoked by an external input
- Option for an external auto-zero clock for synchronous system applications.

High-input impedance and very low input offset current are addressed by very careful attention to the design and layout of the diodes that serve as ESD protection devices at the amplifier inputs. Amplifier performance targets (applicable from -55°C to 225°C) are listed in Table 3.

TABLE 3: Amplifier Design Targets

Parameter	Target Value
Input Offset Voltage	100 μV max.
Input Offset Voltage Drift	0.2 μV/°C max.
Input Bias Current @ 225°C	±150 nA,
Input Offset Current @ 225°C	±1nA,
Input Noise Voltage RS=100Ω, 0.1Hz – 10Hz	3 μV pk-pk
Input Noise Current @ 225°C	1.0 pA/√Hz
Input Range	V_{SS} to V_{DD} -2.0
Common Mode Rejection (DC)	100 dB, min.
Power Supply Rejection (DC)	100 dB, min.
Large Signal Voltage Gain (DC); RL = 10kΩ	100 dB, min.
Gain-Bandwidth Product; RL = 10kΩ, CL = 20pF	2.0 MHz
Slew Rate; RL = 10kΩ	1.5 V/μs (typ)
Output Source/Sink (0.3V from either rail)	±20 mA
Short-Circuit Current Limit	±50 mA
Operating Supply Range	5.0V ±5%
Supply Current, Total Package	5.0 mA, max.
Supply Current, (in Shutdown)	150 μA, max.

3.4 Analog-to-Digital Converter (ADC)

A high-resolution ADC captures data in digital format for subsequent digital signal processing. This ADC focuses on DC and/or low-frequency signals at a level of resolution that has not previously been achieved at temperatures above 200°C. An externally scalable buffered voltage reference is included. Other features include:

- Fully differential input and reference
- Optional single-ended input mode
- Correlated double-sampling front end
- 4-wire serial data & control interface
- Internal oscillator or external clock
- Temperature-scaled current source output
- Auxiliary reference current sources
- Auxiliary 8-bit ADC
- Temperature measurement via 8-bit ADC (~1.4°C resolution)
- Low current sleep state when not in use

An inherently stable 2nd-order sigma-delta modulator approach was selected for this converter. The over-sampling ratio is 2048 which results in a 100 Hz output sample rate using a 204.8 KHz input clock. All digital decimation, filtering and output formatting logic is provided on-chip. The 1-bit output of the sigma-delta modulator (i.e., prior to any digital processing) and the modulator clock is available off-chip to support test/evaluation. The auxiliary 8-bit ADC is a charge-redistribution successive approximation converter. It was conceived as a means of providing temperature measurement when used with an on-chip PTAT (Proportional-To-Absolute-Temperature) voltage source.

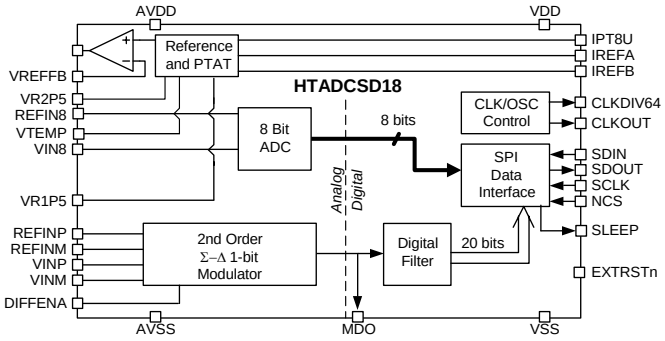

Figure 2: 18-bit ADC Block Diagram

A 28-pin DIP package is planned for this ADC. Full 18-bit output range is available when operating in differential mode (differential input

and differential reference). The converter can optionally operate single-ended at 17-bits resolution. Input mode is selected by a dedicated control input. Data output and control input are accomplished by means of a 4-pin serial interface.

3.5 Field-Programmable Gate Array (FPGA)

A diverse set of digital functions and/or components are needed for even "simple" down-hole systems. These include data and/or control processors, communications interfaces, control and "glue" logic, timers, counters, and others. Extreme-temperature down-hole applications are low-volume and may not be able to overcome the economic hurdle associated with developing a comprehensive set of digital hardware typically used in data acquisition and control.

Field-Programmable Gate Arrays are a good alternative to dedicated hardware designs where low up-front costs and/or fast-turn development are requirements. FPGA's allow users to define functionality of individual hardware units after it has been delivered by the manufacturer or even after it is assembled into a board or deployed in an application. An FPGA is configured by electrical means, such as writing to configuration memory (in the case of a reconfigurable FPGA) or else by a process of permanently configuring the part by electrical fusing.

FPGA products are not commercially available for the extreme high temperature environment (at or above 225°C) required by the Deep Trek program. This project therefore has undertaken development of a high-temperature FPGA. The FPGA that is being developed is fully licensed functional equivalent to a commercial product, the AT6010 FPGA manufactured by Atmel. Replicating an existing commercial product obviates any program requirements developing and supporting hardware or software development systems for FPGA configuration.

The Atmel AT6010 is a reconfigurable FPGA, meaning that it can be configured any number of times. It is however, a volatile configuration. This means the FPGA configuration is not preserved through a cycling of the power supplies. Therefore an external means for storing the configuration data is required. Configuration data can be loaded into the FPGA on power-up. Configuration memory is typically provided by an external non-volatile device such as an EEPROM.

The high temperature FPGA has been designed using the HTSOI process for specified operation at 225°C. Configuration is controlled by dedicated configuration pins and dual-function pins that double as user I/O pins when the device is in operation. The devices can be partially reconfigured while in operation; portions of the device not being modified remain operational during reconfiguration.

Other features of the FPGA include:

- Up to 204 bidirectional user I/O with two levels of output drive
- Six different configuration modes
- 30,000 usable gates, up to 6,400 registers

3.6 Electrically-Erasable Programmable Read-only Memory (EEPROM)

EEPROM refers to memory that can be both written/read multiple times and that retains data when power is interrupted. It is "read-only" not in the sense that it literally can't be re-written, but in the sense that write-access time is typically orders of magnitude longer than read-access time. The relevance of EEPROM to the high-temperature system is obvious from the previously described FPGA, which requires an external non-volatile data-storage device to configure it on power-up. Other applications include storing instruction code for digital-processors, storing hardware configuration data such as serial numbers and calibration coefficients, and data logging.

The high-temperature EEPROM developed in this program has a capacity of 256Kbits organized as 32K x 8 bits. The EEPROM incorporates the functional equivalent of a standard parallel-interface 28C256 EEPROM. This can be used to configure an AT6010-based FPGA in configuration mode 5. However, some additional hand-shake control features must be added to the high-temperature EEPROM so that configuration of the FPGA can be completed automatically each time the devices are powered up.

Non-volatile memory capable of storing and retrieving data at high-temperature is a challenge. There are long-term reliability issues with one-time programmable anti-fuse approaches (commonly used in FPGA's), as well as with re-programmable floating-gate charge storage approaches (commonly used in flash-EEPROM). High-temperature degrades data retention in both cases. Since data-logging at high-temperature is desired, a re-programmable device is preferred to a one-time programmable device. Assuming that a viable re-programmable approach is developed, long-term data retention can be achieved by a combination of inherent data-retention capability of

the bit-cell structure and the fact that the data can be periodically "refreshed" by the user and/or system.

The inherent (i.e., without refresh) data retention goal for this memory was 1000 hours (or about 6 weeks) at 250°C. This is more than long enough for a typical well-logging mission. When this project began there was not an established floating-gate memory structure within the HTSOI process. Neither was there budget for significant modifications of the process flow. Therefore, the preferred approach would be to develop a floating-gate memory cell that is compatible with the baseline HTSOI wafer process. This approach requires development of a single-poly floating gate memory cell. Large-volume commercial floating-gate memories use a dual-poly structure to achieve higher memory density, but such development was beyond the scope of this program.

Writing data to a floating-gate device can be achieved by various means, all of which typically involve applying terminal voltages to the floating-gate structure that are beyond the normal operating supply voltage for the technology. Therefore, means must be provided (typically charge pumps) for generating high voltages on-chip for programming and erasing the memory cells. Due to accelerated high-temperature leakage, it is expected that external capacitors will be required for use with the EEPROM device in order to provide sufficient charge storage for reliable high-voltage write operations at high-temperature.

A final objective is capability to configure the EEPROM as serial interface 25C256 equivalent. Serial interfaces are preferred in many applications to reduce the number of interconnections.

4.0 Results and Plans

4.1 Technology and Design Infrastructure

The 0.8-micron high temperature SOI-CMOS wafer process previously described (HTSOI) is in production, fully supported by schematic capture tools, high-temperature simulation models and libraries, and layout verification software.

The HTSOI process and design tools have been successfully used within the DeepTrek program to develop analog, digital, and gate-array based digital ASIC's. An example of a mixed-signal (analog plus digital) design using an HT2000 digital gate array platform with a full-custom analog drop-in block is the 18-bit ADC design, shown in Figure 3. This chip contains 90K logic gates placed and routed by the gate-array toolkit, plus a full-custom analog section and split analog/digital power supply domains.

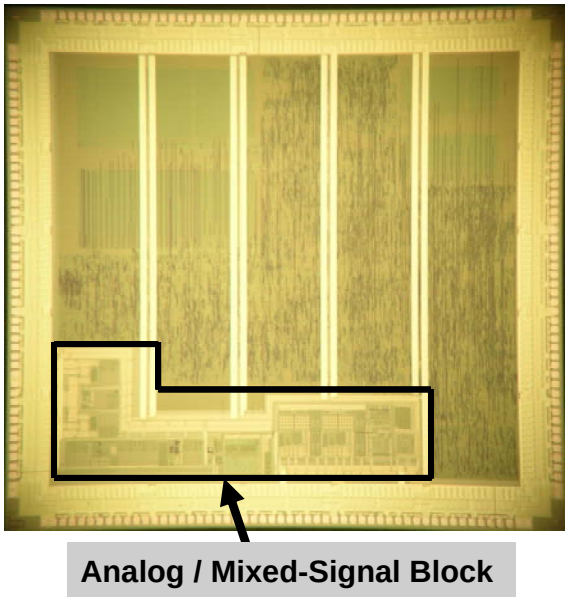

Figure 3: 18-bit ADC die photo

4.2 High-temperature Precision Amplifier

The HTOP01 high-temperature precision amplifier was the first component to be developed and verified within the Deep Trek HTE program. It has met all the major design objectives in the first design pass [18]. Functionality has been demonstrated up to 375°C. A plot of input offset voltage vs. common-mode input voltage is shown in Figure 4. This data is courtesy of Randy Normann at Sandia National Laboratory, and was obtained at 300°C after several hundred hours of operation at 300°C.

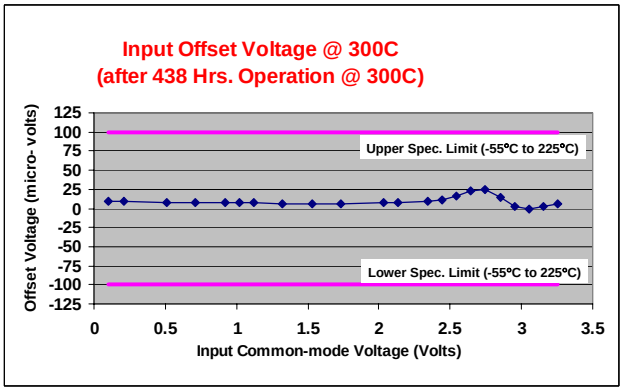

Figure 4: Amplifier Offset at 300°C

4.3 High-temperature 18-bit ADC

Design and fabrication of the 18-bit ADC has been completed. The digital filtering and control logic was synthesized from functional

Verilog code and implemented using high-temperature digital libraries and placed and routed using the HT2000 gate array design process. The voltage and current reference block and the second- order sigma-delta modulator have been designed and laid out as a full-custom block dropped into the HT2000 digital gate-array I/O frame.

Evaluation samples of the A-to-D have been packaged in a 208-pin grid array package. This package configuration gives access to circuit nodes that are not available in the 28-pin production configuration. This will facilitate independent verification of sub-blocks of the overall design. An evaluation board has been developed that will enable performance testing in an oven environment. Testing will be initiated during 2nd quarter of 2006.

4.4 High-temperature FPGA

Design and fabrication of the FPGA has been completed. A die photo is shown in Figure 5. This is a large die (approx. 12mm x 16mm). Over half of the die bond-pads are power/ground pads to facilitate low-impedance supply connections in a variety of assembly configurations. A rectangular rather than square aspect ratio is intentional since some down-hole applications are constrained to fit into narrow places. For the same reason, all of the configuration pads are placed on one end of the die (across the right as shown in the photo) which makes it feasible to develop application scenarios that do not require wire-bonding on the top/bottom of the die. This further aids in fitting the FPGA into narrow dimensions.

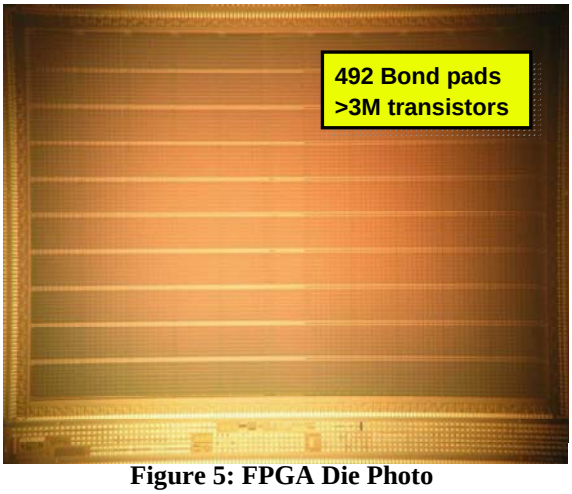

Figure 5: FPGA Die Photo

A comprehensive set of functional tests has been developed to exercise the FPGA. These configure the FPGA and exercise the configured functionality for a large number of test applications. At this time 85% of these tests have been run and no functionality issues have been observed. Based on the scope and content of those tests already successfully completed, it's not expected that any functional issues will be observed in the remaining tests. All tests have been conducted at wafer-probe level. Wafer probe testing is limited by the test equipment to a hot-chuck temperature of 200°C. After of wafer-level tests are finished, assembly is planned that will enable testing to the full specified temperature range.

4.4 High-temperature EEPROM

Much of the initial EEPROM development has focused on characterization of floating-gate charge storage structures. Two EEPROM device-level characterization test-chips have been designed and fabricated.

EEPROM operation is based upon shifting the threshold voltage of floating-gate transistors by adding or removing charge by Fowler-Nordheim tunnelling. The threshold shift is read by turning on the floating gate device by capacitive coupling and detecting the difference in current resulting from a positively versus negatively shifted transistor threshold. Figure 6 shows data retention results from the first EEPROM test chip. This shows that there is still over 1.5V threshold voltage difference retained between a positively vs. negatively shifted device after 8000 hours at 250°C.

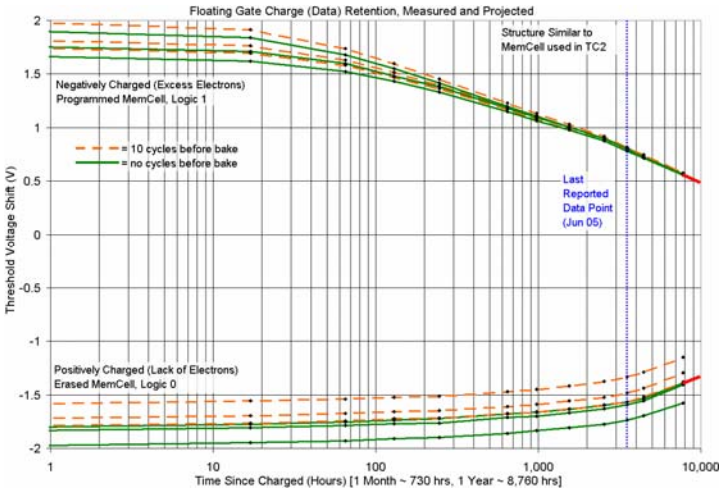

Figure 6: 250°C Floating Gate Threshold Shift vs. Time

In addition to floating-gate and memory cell characterization, the first test-chip was used to optimize layouts for extended-voltage devices that

will be required to apply program/erase waveforms used to write the memory. Both the floating gate bit-cells and the high-voltage write-interface are achieved without any modification of the production HTSOI4 wafer process.

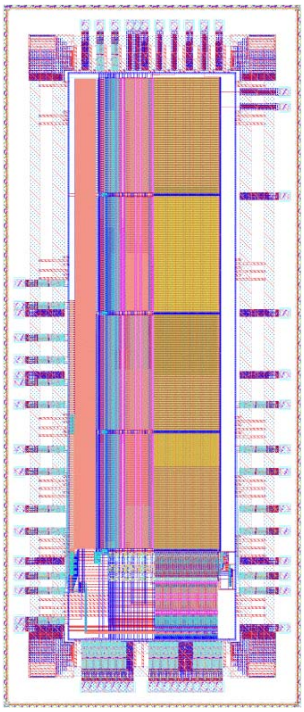

Figure 7: 4K x 8 EEPROM Test Memory

Based on results from the first test-chip, a non-volatile memory array has been developed along with row and column interfaces resulting in a 32Kbit EEPROM memory core that is currently being evaluated. This memory core (shown in Figure 7) has been designed so that it can be easily expanded to the full 256Kbit objective for the EEPROM product design. Design and layout of the 256Kbit EEPROM memory is in progress and will be completed before the end of 2006.

5.0 Summary and Conclusions

The Deep Trek High-temperature Electronics program is succeeding at meeting its objectives. An SOI CMOS process flow and supporting design infrastructure targeted to high-temperature has been put into production and successfully applied to the design of Deep Trek components. The precision amplifier and FPGA have been successful with the first design pass. A high-resolution A-to-D has been fabricated and is awaiting test. Non-volatile data storage has been demonstrated and applied to a demonstration memory in advance of full product design which is yet to be completed under the program.

Hopefully these developments will help to overcome some of the "chicken-and-egg" issues associated with high-temperature electronic systems. There still are issues with the low-volume nature of high-temperature applications and the economics required to develop needed components. This program has sought to focus all of the key components into a single process flow to help establish a sustainable economic case. However, this process does not address all system needs, especially needs for power storage, power management, and high-power actuators. SOI CMOS data acquisition and control electronics for high-temperature are one piece in the high-temperature system that may include high-temperature batteries, passives, power-devices (such as SiC and/or GaN), a growing catalog of high-temperature components and means for packaging and delivering system-level modules.

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Appendix 5

An SOI Precision Reference and Bias Circuitry for Operation to 250°C

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Abstract

An SOI precision voltage reference has been developed and verified that provides a buffered, low-noise output well suited for general purpose high temperature and/or wide temperature range applications. The reference provides 0.3% accuracy from 25℃ to 225℃, with rms output noise of less than 5μV at 225℃. This reference was designed for use as a reference source for high-resolution A-to-D converter. The reference is buffered to provide up to 5mA source/sink capability and is adjustable via external components and a feedback pin. Associated with the reference on the same die are bias and utility functions. These include Proportional to Absolute Temperature (PTAT) current-mode and voltage-mode thermometer outputs and reference current sources. A wide variety of applications and temperature compensation schemes can be supported by this combination of functions in a single component. The reference uses lateral bipolar transistors fabricated in an SOI CMOS using the standard CMOS layout layers. This work has been performed within the Department of Energy DeepTrek Program with the participation of industry partners in a Joint Industrial Participant (JIP) program.

Key words: High-temperature electronics, EEPROM, FPGA, Analog-to-Digital Converter, Amplifier

1.0 Introduction

In extended temperature range electronic systems there is almost always a requirement for a temperature stable reference voltage (or current source). In any system involving sensors, it is also very useful to have access to voltage and/or current sources with linear temperature dependence, either as a means of measuring temperature, biasing the sensors, or for temperature compensation or scaling of the sensor response.

CMOS has long been the work-horse of the integrated circuit industry. CMOS designs have long exploited approaches adapted from earlier bipolar technologies for integrated voltage references. Most integrated circuit references are based on bipolar devices, including those implemented in CMOS processes [1]. For extreme high-temperature applications (>200°C) Silicon-on-Insulator (SOI) CMOS is generally required. Lateral bipolar transistors have been used to develop high-temperature SOI band-gap reference circuits [2-6].

This paper describes a general purpose SOI CMOS voltage reference and bias circuits. This circuit is embedded within a high-resolution A-to-D converter. The A-to-D converter is being developed with the U.S. Department of Energy's DeepTrek program, administered by the Strategic Center for Natural Gas (SCNG), at the National Energy Technology Laboratory [7-9]. The key features of this circuit block have been specified by industrial partners collaborating with DOE on the project.

For this application, a buffered voltage reference is needed, capable of fast-settling when sampled by the input structure of the A-to-D's sigma-delta modulator. The reference also must have very-low 1/f noise. Beyond that, the industrial partners working on this program were keen to have features and outputs beyond what is strictly required to service the A-to-D. This arises from other applications within the system and the fact that high-temperature stable and/or linear reference components are not generally available. Hopefully these additional features will serve to maximize the utility of this development.

Deep Trek program industrial partners are Baker Hughes, BP America, Goodrich Aerospace,

Honeywell, Intelliserv, Quartzdyne, and Schlumberger.

2.0 Design Application and Objectives

A block diagram of the reference and bias block that has been developed is provided in Figure 1. The features that have been included can be described in terms of some of the potential applications which they may serve. As Figure 1 shows, there is a basic voltage reference (VREF) block. As will be described later, within this block is a band-gap circuit that employs lateral PNP transistors. Inherent in this approach is the development of a Proportional-to-Absolute-Temperature (PTAT) current. These two signals, a temperature stable voltage and a linear temperature-dependent current are buffered and/or combined to provide the primary outputs of the circuit.

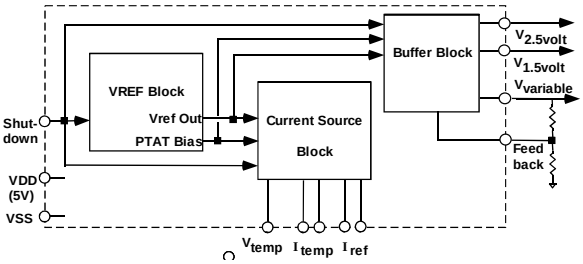

Figure 1: Reference and Bias Block Diagram

The buffer-block (on the right in Figure 1) has three voltage-mode outputs. The first of these is a 2.5V fixed-voltage ($V_{2.5Volt}$). This is a buffered source with active push-pull output that can nominally source or sink 5mA. It has current-limiting feature on the output with a nominal short-circuit current of ±30mA. In this project this output serves as the full-scale reference for an auxiliary 8-bit A-to-D converter, but can also be used off-chip. For example, it has sufficient drive capability to bias resistive pressure, temperature, or magnetic sensors. It can also provide a convenient mid-supply reference for differential analog sensing and control topologies in a 5V-suppy system.

The second voltage-mode output is a 1.5V fixed voltage ($V_{1.5Volt}$). This output has a source-follower output stage with limited current-sinking capability. It is intended to directly drive the reference input for a high-resolution (18-bit) over-sampled A-to-D converter. It is required to settle to less than 0.5 LSB (3μV) of its final value within 5μsec when sampled onto a 10pF load. This reference must also have very low 1/f noise (less than 1 LSB in the 0.1 to 50Hz band).

The third voltage-mode output is a variable reference output ($V_{Variable}$) that can be scaled by external resistors to any value from1.5V to 4.5V. This has an output stage similar to the fixed 2.5V output, and can likewise actively source/sink current and has short-circuit current limiting. This is a general-purpose, low-noise buffered reference. It is ideally suited for driving bridge type transducers.

All three voltage-mode outputs are referenced from a common reference source; they all track one another over temperature and aging. They are therefore well-suited to applications such as bridge transducers where bridge bias and full-scale reference are scaled versions of a common reference. With this type sensing and measurement configuration it is possible to develop measurement systems that (to first order) are independent of reference variations.

The "Current Source Block" in Figure 1 provides primarily current-mode outputs. However, the first output discussed is actually a voltage-mode output. It is the output labelled "V_{temp}" and is a thermometer output (i.e., a voltage-mode temperature signal). In precision applications, especially those involving wide-temperature range, it is often useful (or necessary) to know the local ambient temperature so that temperature-compensating means may be applied for offsets and non-linearity in the measurement system. The V_{temp} output is specified to provide a temperature signal that nominally traverses from 0V to 2.5V as the temperature ranges from -55°C to +285°C.

The remaining outputs are current-source outputs. There are two temperature-scaled current sources (labelled I_{tmep1} and I_{temp2}). Both of these are nominally specified to be 8μA at room temperature. I_{temp2} is specified to be a true PTAT output. Given that the nominal design target is 8μA at 298°K, then it follows that the temperature sensitivity of this current is approximately 40nA/°C. PTAT bias sources can be very useful in electronics systems. For example, amplifiers biased with PTAT currents achieve a very good over-all trade-off between gain, bandwidth, and common-mode range over a wide temperature span. Another use of PTAT current sources is to apply the output to a temperature stable resistor, yielding a PTAT voltage that can be scaled by the resistor value.

One shortcoming of a strictly PTAT signal for many applications is that it's full dynamic range

includes temperatures that are not useful (i.e., extremely cold). What is preferable in most cases is a signal that is Proportional-to-Reference-Temperature (PTRT). That is the intent of I_{temp1}. I_{temp1} is nominally specified to have an output of 0μA at a temperature of -55°C, the minimum specified temperature range of this application. The scale factor on this output is nominally 100nA/°C.

Finally there is a "Shutdown" control signal in Figure 1. Many of the high-temperature system applications targeted by the Deep Trek program use batteries and therefore power management is critical to extending mission life. The shut-down control provides means for putting all of the VREF and bias circuitry into a low-power state when operation is not required. This is generally done by shutting off bias current sources.

A summary of some of the key design targets/features of the VREF and bias block is provided in Table 3 below.

TABLE 3: Design Targets

Parameter	Target Value
Supply voltage	5V ± 5%
Variable reference output voltage range	1.5V to 4.5V
Temperature Variation: 0°C to 225°C	1.1% max.
Output noise, 0.1Hz to 10 Hz	15μV rms (max).
Constant-current outputs	200μA, typ.
Current source matching	±2%
Constant-current source temperature variation: 0°C to 225°C	2.3% max.
Temperature scaled current sources: 25°C output I_{temp1} output I_{temp2} output Temperature scale factor I_{temp1} output I_{temp2} output	 8μA 8μA 0.1μA/°C 0.04μA/°C (PTAT)
V_{Temp} Thermometer voltage -55°C output 25°C output 285°C output	 0.0V 0.6V 2.5V

4.0 Implementation

4.1 Lateral PNP Devices in SOI

A multi-purpose high-temperature SOI CMOS process has been used on this project [10-12]. In this process the standard P-channel MOS transistor may be used as a lateral PNP transistor (see Figure 2). The source, body, and drain terminals function as emitter, base, and collector. The gate of the MOS transistor is typically biased in accumulation so that there is not any complication from the "parasitic" PMOS action. This results in a device that has low 1/f noise relative to a standard MOS device.

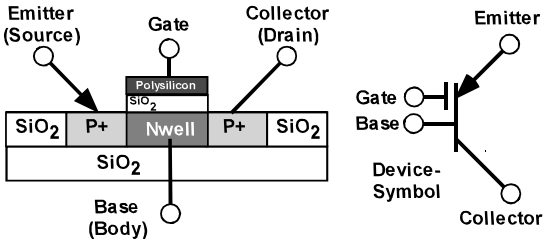

Figure 2: Lateral PNP Structure and Device Symbol

Due to the relatively large base width (MOS gate length, 0.8 microns in this process) and the high resistance of the base, this is not a high performance bipolar transistor. It is sufficient for operation at relatively low currents and serves for band-gap voltage circuits.

An advantage of SOI technology in this regard is the fact that all the terminals of the bipolar transistor may be connected independently and there are no parasitic devices as in some bulk CMOS processes (for example, reference [1]).

4.2 Bandgap Reference

A simplified schematic of the band-gap reference block is provided as Figure 3. This circuit employs lateral PNP transistors. It is based on generating a PTAT voltage (ΔVbe) by forcing equal currents to flow in the 1x and 8x PNP transistors. The 8x transistor is eight times larger than the 1x device and therefore is biased at lower current density. The difference in base-emitter voltage between bipolar transistors operated at different current densities is given by the familiar equation:

$$\Delta Vbe = \ln A \bullet (kT/q)$$

"A" is the ratio of current density in the 1x device relative to the 8x device. In the circuit configuration shown, ΔVbe is impressed across R1, and therefore to the extent that R1 is temperature invariant (or at least linear with temperature) the current flowing in R1 is PTAT.

Equal currents are forced in the 8x / 1x pair by the feedback loop established by OTA1,

M1 and the current mirrors. Note that ΔVbe is amplified by the ratio of R4 to R1 before being applied at the input to OTA1. This topology is a key to reducing the 1/f noise of the reference. The noise of OTA1 referred back to the "input" (ΔVbe) is attenuated by this gain. OTA1 is implemented as a folded-cascode transconductance amplifier with Pch input and uses very large input devices as well as N-channel loads to maintain low 1/f noise and low offset voltage. Although not shown, it is worth noting that the current mirrors are implemented using lateral PNP transistors to take advantage of the much lower 1/f noise of these devices relative to standard PMOS cascode current mirrors.

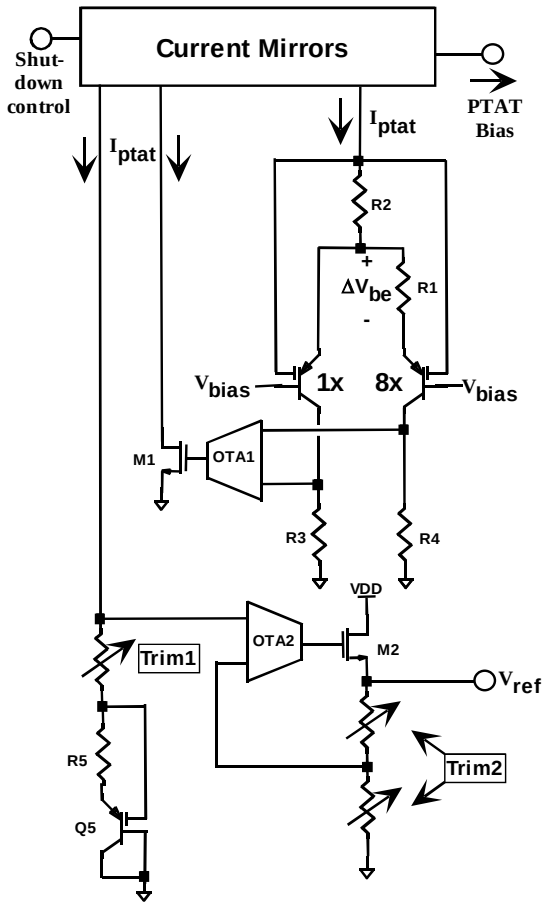

Figure 3: VREF Block Structure

The rest of the task of generating the reference voltage consists in amplifying the PTAT voltage such that when summed with a forward diode drop (lateral PNP Vbe) which has a relatively linear negative temperature coefficient. The result is a temperature invariant voltage.

In the circuit of Figure 3 the ΔVbe amplification is accomplished by the combination of lateral PNP current mirrors and applying PTAT current across resistor R5. The voltage across both R5 and the trim network (Trim1), when summed with the Vbe of transistor Q5 results in a temperature insensitive voltage.

All of the resistors in Figure 3 are implemented as thin-film CrSiN resistors. Trim1 is laser-trimmed to achieve the required low temperature drift. This trimming is done at wafer level test after collecting data at 200°C using a hot-chuck wafer probe.

After trimming to achieve the required temperature stability, another low-noise (large device geometry) OTA is used in connection with a second trim network (Trim2) to trim the output voltage, VREF, to precisely 1.5V. The shut-down control may be used to shut down the circuit by turning off the current mirrors and "starving all of the devices" for current. Not shown are start-up circuitry and resistor-capacitor networks used to insure loop-stability.

The primary outputs of the VREF block are a 1.5V un-buffered reference, and a PTAT current source. The PTAT current source is mirrored with appropriate device geometry scaling to provide the PTAT current source output (I_{temp2}). In fact, the PTAT current is scaled and replicated multiple times in this application for other on-chip functional blocks of the Deep Trek A-to-D converter.

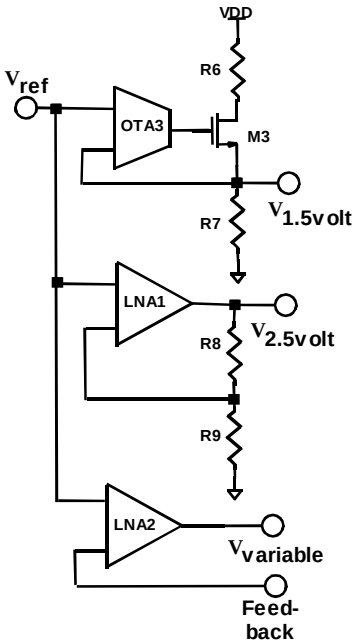

Figure 4: Buffer Block

4.3 Voltage Buffer Block

The buffer block is shown in Figure 4. This block consists of two low-noise amplifiers and a low-noise OTA with an N-channel source-follower output. The LNAs have the same input stage as the OTAs, but additionally have an active push/pull output driver. The reason that the 1.5V output does not use an LNA is that it is required to have a fast-settling output (to drive the sigma-delta A-to-D front end). Adding an output stage requires additional compensation to insure loop stability. Given the very large device geometries employed to manage 1/f noise, it was not possible to compensate an output stage and simultaneously meet the settling requirements of the A-to-D.

4.3 Current Reference Block

The current reference block is shown in Figure 5. This block generates two matched temperature-stable 200 μA current sources, I_{ref1} and I_{ref2}. This is accomplished by the voltage-to-current converter (OTA4, source-follower and resistor) that generates a constant (i.e., temperature-stable) current. This is mirrored by the current mirror network to provide outputs I_{ref1} and I_{ref2} directly. The mirror network can be laser-trimmed if required to precisely scale the output current values.

The Current Reference Block also generates the voltage-mode and current-mode PTRT thermometer outputs, V_{temp} and I_{temp1}. A PTAT voltage is developed across R10 by impressing on it PTAT current from the VREF block. This PTAT voltage is replicated across R11 by OTA5 and feedback from the source-follower output. Part of the PTAT current flowing in resistor R11 is comprised of temperature-stable (i.e., constant) current from the mirror network shown. That being the case, the current flowing in the leg that includes the source-follower after OTA5 is forced by the feedback of OTA5 to be I_{PTAT}-$I_{CONSTANT}$. Subtracting the constant current term introduces an offset in the PTAT current, rendering it PTRT with the reference point established by the trimmed mirror network. A final trim to scale the output may be applied in a second laser-trimmed mirror network.

All of the resistors and trim-networks in this block are made using thin-film CrSiN. This material has a typical temperature coefficient of resistance of -100ppm/°C. The same material is used in the band-gap where I_{ptat} is derived. Therefore I_{ptat} will vary as the CrSiN resistance varies. If I_{ptat} is mirrored or scaled and then applied to another CrSiN resistor (to develop a voltage output as in the case of V_{temp}), the CrSiN variation with temperature drops out. However, in the case of the current-mode outputs, I_{temp1}, I_{temp2}, and I_{temp1}, I_{temp2} the output current varies directly with the CrSiN temperature coefficient.

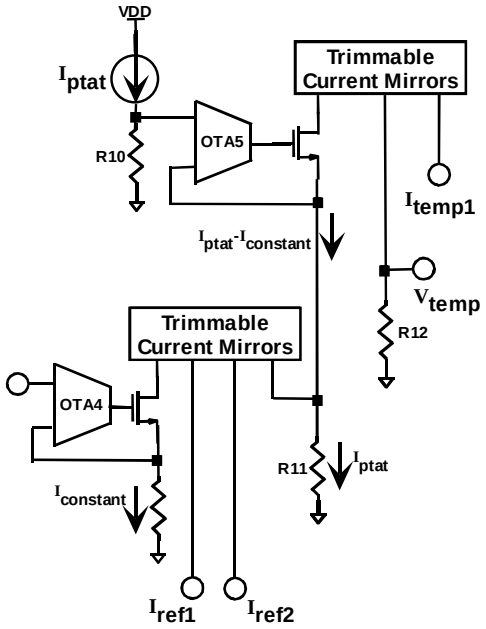

Figure 5: Current Reference Block

5.0 Results

At this time, testing of this block has been limited to wafer-level probe testing mostly un-trimmed die. Additional package-level test results will be presented at the HiTEC conference.

5.1 LNA Results

It has been stressed that low-noise and offset voltage are critical to this application. This is largely dependent on the offset and noise-characteristics resulting from the OTAs and LNAs that are used multiple times. Recall that the noise and offset performance derives from the input pair and load transistor geometries that the OTAs and LNAs have in common.

Thirty-nine LNA die were wafer-probed at room temperature to measure their offset voltage. The average magnitude (absolute value) of the offset voltage was 198μV. Offset mean and standard deviation of the offset voltage are 92μV and 232μV respectively.

Room temperature noise-voltage density results measured on one sample at room temperature are as follows:

1Hz : 360nV/root-Hz.
10Hz: 110nV/root-Hz.
100Hz: 38nV/root-Hz.

The roughly 3x reduction per decade confirms that this follows a 1/f noise characteristic. It cannot be determined from this data what the wide-band noise floor is, other than to predict it is less than 38nV/root-Hz. These results suggest that the LNAs and OTAs are significant in terms of noise contribution, but not solely dominant.

5.2 Buffered VREF Output Results

Voltage reference trims (Trim1 and Trim2) were completed on a handful of die followed by wafer-level probe testing. Results are shown in Figures 6 and 7.

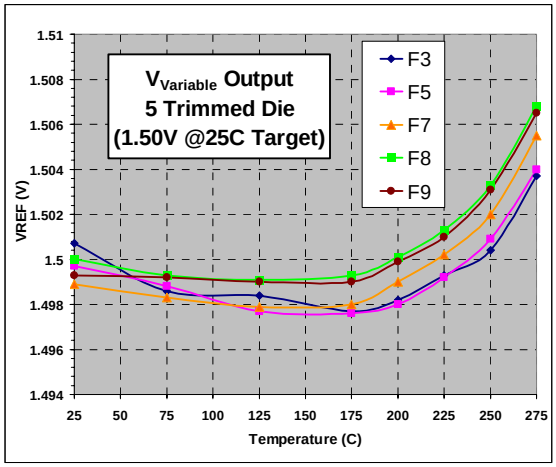

Figure 6: Buffered Reference Output vs. Temperature

Figure 6 shows measurements obtained at the output of the adjustable buffered output ($V_{Variable}$) operated at 1.5V (unity-gain voltage-follower). Results are shown for five die at 25°C intervals from room temperature to 275°C. It can be seen that from 25°C to 225°C the output variation is within 3mV (0.2%) in all cases. Total variation doubles by 275°C, but the reference is clearly still functioning well at this temperature.

Figure 7 shows noise voltage density results at the buffered output ($V_{Variable}$) for 3 die at 25°C and at 225°C. It can be seen that the 1/f noise corner is between 10Hz and 100Hz. From these results total rms output noise in the band from 0.1Hz to 50 Hz can be calculated at about 5μV. This is slightly less than 1 LSB for a 1.5V full-scale signal at 18-bits resolution.

Figures 8 and 9 show the temperature-scaled current outputs. These are for the case of un-trimmed die where the internal reference voltage (VREF) was externally forced to 1.5V. It can be seen that the scale factors and linear output are very close to target.

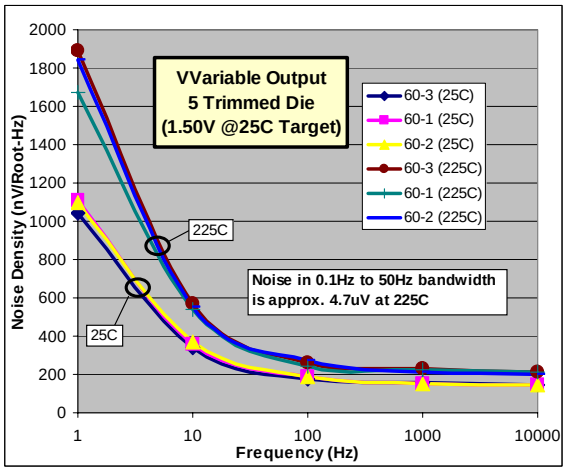

Figure 7: Buffered Reference Output Low-Frequency Noise Characteristics

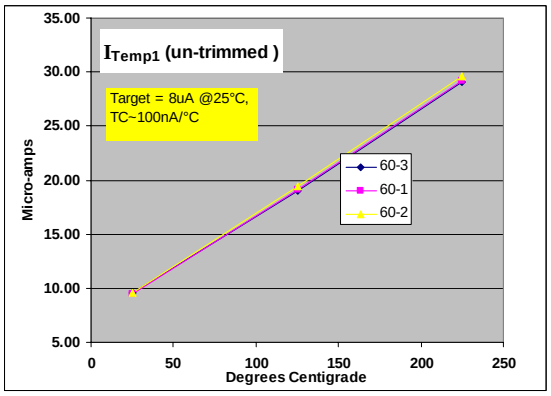

Figure 8: Temperature-scaled Current Source, Itemp1 Output

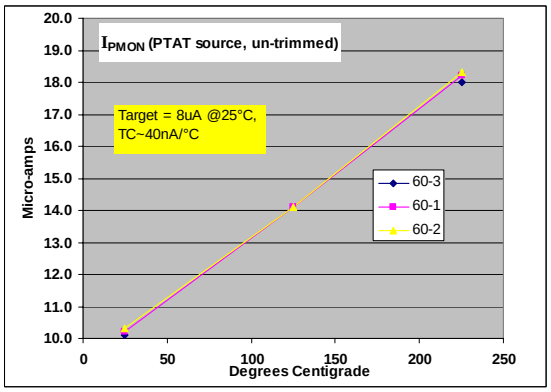

Figure 9: Temperature-scaled Current Source, Itemp2 (PTAT) Output

Wafer-level results were also obtained for the matched constant-current outputs (I_{ref1} and I_{ref2}) up to 225°C. The outputs are within 0.2% of the specified 200uA Worst-case mismatch between the two outputs measured on three die is 0.4%.

6.0 Summary and Conclusions

A general purpose voltage reference and bias block has been realized in SOI CMOS, with demonstrated operation to 275°C. Further testing could extend that result. Very good temperature stability and output noise results have been achieved up to 225°C (0.2% and 5μV rms respectively). Utility reference and thermometer outputs are part of this circuit. This design is meeting all of the performance levels required of the A-to-D converter for which it was developed.

Although this circuit was developed as an embedded block within an A-to-D converter, it could easily be turned into a stand-alone function in a relatively small package (e.g., 14-pin DIP). The test-site implementation reported here is equivalent to about 0.08 inches square (about 2mm x 2mm).

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Appendix 6

Updated Results from Deep Trek High Temperature Electronics Development Programs

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Introduction

Electronics are used in modern oil and gas exploration to collect, log, and/or process data such as heading and inclination, weight on the bit, vibration, seismic/acoustic response, temperature, pressure, radiation, and resistivity of the strata. High-temperature electronics are needed that can reliably operate in deep-well conditions (up to 250°C). The U.S. Department of Energy Deep Trek program has funded two projects led by Honeywell. The first project, launched in 2003 and completed this year, established a production-level integrated circuit (IC) manufacturing process, components and design tools [1-4] specifically targeting high-temperature environments (up to 250°C). The second project, launched in 2006 and completing in 2008, will develop rugged packaging suitable for down-hole shock and vibration environments which will be used to house and demonstrate components developed in the earlier project. This paper describes updated results of these successful projects.

Deep Trek Projects

Oil and gas drilling time and costs escalate when the target reservoir is very deep. Relative to more conventional well depths it is therefore even more important to be able to monitor down-hole conditions in deep wells (>15,000ft, 4,575m). This creates a catch-22 situation because electronics that can reliably operate in deep-well conditions have not been available, primarily due to the high temperature (up to 250°C, 481°F) encountered at great depth. Commercial electronics are not designed for these temperatures, and conventional integrated circuit (IC) technology is not capable of operating at these temperatures. To help overcome this limitation, the U.S. Department of Energy Deep Trek program has funded two projects led by Honeywell to develop electronic components that can handle the heat and deliver the data operators need to undertake deep-reservoir development.

The first project, launched in 2003 and completed this year, established a production-level IC manufacturing process along with IC design tools (software and simulation elements) specifically targeting high-temperature environments. These IC technology and design tools were then employed to develop prototype high-temperature IC components, with the objective that these will be made available to the industry as commercial products. This project was completed in collaboration with a Joint Industrial Participation (JIP) consortium of commercial partners. The JIP partners defined priorities and specifications for components developed and demonstrated within the project. These include:

- a dual precision amplifier,
- a field programmable gate array (FPGA),
- a high-resolution A-to-D converter,
- a high-temperature non-volatile memory (EEPROM).

An additional outcome of this project is a family of metal mask programmable gate-arrays suitable for use up to 250°C.

The second project, launched in 2006 and scheduled for completion in 2008, will develop rugged multi-chip-module (MCM) packaging suitable for down-hole shock and vibration environments. An MCM package developed under this project will be used to house and demonstrate components developed in the earlier project.

High Temperature Wafer Process Technology

A partially depleted 0.8 micron SOI CMOS IC manufacturing process has been developed and established in factory production specifically for high-temperature applications [5]. The wafer process flow was adapted from a previously established SOI technology in use for aerospace products. This adapted technology has been successfully applied in the manufacture of all of the proto-type IC components within these Deep Trek projects. All of the devices in this process are suitable for long-term operation (5 years at 225°C) using 5V supplies. Besides the use of SOI structure, the primary feature of the wafer process to address high temperature includes the adjustment of transistor threshold voltages to minimize sub-threshold leakage. Up to four layers of aluminium interconnect are available. Inter-connect electro-migration reliability is established by characterization and adherence to design rules limiting the maximum current density in the conductors, either through de-rating of operating frequency (for digital applications) or through high temperature optimized interconnect layout (primarily power bus and/or DC output conductors). Analog elements (CrSiN thin-film resistors, MOS capacitors, and lateral PNP transistors) are available and supported.

Temperature-compensated biasing techniques for analog circuits are employed to maintain gain and bandwidth over an extremely wide temperature range. Design toolkits have been updated and applied for high temperature applications. These include development of SPICE models applicable from -55°C to 250°C.

Purely analog (or full-custom digital) blocks are implemented using traditional analog tools and processes, including schematic entry and SPICE based simulation methodologies. This is done using a Process Design Kit (PDK) which is an integrated collection of schematic capture symbols, models, layout rules, and other items to allow use of design software available from Cadence. Laser-trimming and high temperature wafer probing can be combined to adjust voltage reference temperature coefficients, or for tailoring other temperature-dependent circuit performance.

Now that the first Deep Trek project has been completed this wafer process, layout rules, SPICE models, and Cadence design and layout toolkit items may be accessed on a foundry basis.

High Temperature Digital Gate Arrays and Design Infrastructure

Digital functions are commonly defined at a behavioural level in the form of hardware description language (HDL) netlists. Once defined by this means they are commonly implemented in hardware by a process of synthesis into a gate-level structure which is then fabricated using gate-array IC platforms. A family of metal-mask programmable gate arrays suitable for manufacture in the 0.8 micron SOI process (described above) has been validated for high-temperature use. This gate-array family (HT2000) uses established HDL-based development tools and flows [6, 7]. The conventional Honeywell design tools and techniques have been extended for high-temperature application. This includes simulation timing models that are applicable at 250°C, and load-checking routines for adherence to rules appropriate to address high-temperature electro-migration concerns. The HT2000 family of high-temperature gate-arrays incorporates a family of die encompassing a ranging from 27,000 to 275,000 usable gates. For ASIC designs incorporating a mix of analog and digital blocks, sub-modules of analog and/or custom digital circuitry may be embedded inside the gate-array I/O ring. For example, this was the means for implementing one of the high-temperature A-to-D converters in this project.

Dual Precision Amplifier

A high-temperature dual precision amplifier has been developed and fully-verified at 225°C with additional testing up to 375°C [8]. The component die size is 2.3mm x 1.8mm. The amplifier is continuously auto-zeroed to achieve very low offset and low-frequency noise, making it suitable for low-frequency DC-coupled sensor-interface applications. The auto-zero function requires a clocking source. The chip can provide this clock autonomously via an on-chip oscillator, or there is the option of providing an off-chip clock. Using an off-chip clock can provide more optimal performance, especially for sampled-data systems where usage of an off-chip clock can allow synchronization with the sampling period. The dual precision amplifier also has a sleep-mode feature to conserve power when the amplifier is not in use. Previously reported data from prototype characterization is summarized in Table 1 below. Manufacturing test programs have been developed and test/assembly flows have been established for commercial sales in the form of 14-pin DIP packages or as deliverable die.

TABLE 1 : Dual Precision Amplifier Packaged Test Data (-55°C to 225°C) unless noted

Parameter	Target Value	Measured Results
Input Offset Voltage	±100 μV (max.)	±5 μV (external clock)
Supply Current (5.25V supply, 225°C)	5 mA	1.85 mA
Open-loop Gain (-55°C to 225°C)	> 100dB	> 114dB
Input Noise Voltage RS=100Ω, 0.1Hz – 10Hz (internal clock) (External clock at 30KHz)	 3 μV pk-pk	5.7 μV pk-pk @ 23°C 4.6 μV pk-pk @ 225°C 1.4 μV pk-pk @ 23°C
Input Range	V_{SS} to V_{DD} -2.0	V_{SS} to V_{DD} – 1.7
Output Source/Sink (swing to 0.3V from either rail)	±20 mA	> 20 mA
Output Short-Circuit Current Limit	±50 mA	51 mA (average)
Supply Current with Shutdown asserted	150 μA, maximum	13 uA, typical

High-temperature Field Programmable Gate Array

Low-volume digital IC applications are often addressed by the use of programmable logic devices. These go by a variety of names, including Field Programmable Gate Arrays (FPGAs). FPGAs apply the economic advantages of batch processing to low-volume or application-specific digital components by enabling the user to customize components on a unit-by-unit basis. An FPGA is configured by electrical means, such as writing to configuration memory (in the case of a reconfigurable FPGA) or else by a process of permanently configuring the part by electrical fusing.

FPGA products are not commercially available for the extreme high temperature environment (at or above 225°C) required by the Deep Trek program. Therefore, a high-temperature FPGA has been developed under the Deep Trek program. It is a licensed functional equivalent to a commercial FPGA, the Atmel AT6010 [9]. The high temperature FPGA has been designed using the HTSOI process for specified operation at 225°C. It is a re-programmable, SRAM-based FPGA that provides 30,000 programmable logic gates and 204 programmable inputs/outputs. Configuration is controlled by dedicated configuration pins and dual-function pins. Dual function pins double as user I/O pins after the device is configured and in operation [10]. The devices can be partially reconfigured while in operation; where portions of the device not being modified remain operational during reconfiguration. The high-temperature FPGA has been fully verified by wafer-probe testing at 200°C (391°F). The design includes more than 3 million transistors, yet standby leakage current at 200°C is still under 0.5mA. This design will be offered in die-form, as well as embedded within the RPDA multi-chip module described later.

High-temperature A-to-D Converters

Two complete high-temperature A-to-D converters have been proto-typed. The first, a high-resolution A-to-D was funded under the Deep Trek program [4]. The second, a 12-bit successive-approximation A-to-D was completed in parallel with the Deep Trek program. A comparison of features and performance is provided in Table 2.

The Deep Trek A-to-D was developed to digitize DC and very-low frequency signals to a high level of resolution. The design provides 20-bits of resolution, although effective performance was not expected beyond 18-bits. The Deep Trek program intent is to develop a high-resolution A-to-D (targeting 18-bit performance) suitable for industry use as a commercial product (referred to as HTADC18). A block diagram of the HTADC18 is shown in Figure 1. The core A-to-D function is provided by a 2nd-order sigma-delta modulator with a single-bit output at an over-sampling ratio of 2048 (single-bit modulator output rate is 204.8KHz). An on-chip digital decimation and filter processes the modulator output to develop a 20-bit conversion result at 100 samples per second. Other features include a Reference and PTAT (Proportional-To-Absolute Temperature) block [11]. This block generates voltage-reference and current-reference outputs, as well as a PTAT current source, and a "thermometer" voltage. The thermometer voltage was designed for use as an on-chip temperature monitor. The HTADC18 also includes an auxiliary 8-bit successive approximation A-to-D which can be used to digitize either this temperature signal or an external signal source depending on the user's preference. The HTADC18 incorporates a self-contained oscillator so that the A-to-D can function autonomously, and a serial I/O block (Serial Peripheral Interface, or SPI). Using the SPI the HTADC18 can be configured to operate in several modes, or be placed into sleep state to minimize power consumption when not in use. Also via the SPI the HTADC18 can be configured so that the raw modulator output and 204.8KHz sampling clock are available on the MDO and CLKOUT pins respectively. This last feature enables potential use

with external decimation and filtering functions that might be employed to achieve faster update rates at the price of overall resolution.

TABLE 2 : High-temperature A-to-D Converter Features and Prototype Performance

Feature	Deep Trek High-Resolution A-to-D	12-bit A-to-D
Output Resolution	20 bits	12 bits
Architecture	2nd order sigma-delta	Successive Approximation
Update Rate	100 Samples/sec	100K Samples/sec
Input	Differential (with single-ended option)	Single-ended
Output format	Serial	Parallel
DC Linearity at 225°C	16.7 bits	10.7 bits
Power Dissipation at 225°C	35mW	*No data at this time*
ENOB at 225°C	17.4 bits	
Output repeatability	17.7 bits (RMS), 15 bits pk-to-pk	
Die Size	10.4 mm x 9.5 mm	3.2 mm x 2.8mm
Prototype Package Configuration	28-pin DIP	28-pin DIP

The HTADC18 was implemented by partitioning the design between analog functions (oscillator, modulator, 8-bit ADC, Reference and PTAT block) and digital functions (digital filter and serial data interface). Analog functions were collected into a single analog/mixed-signal block and dropped into a high-temperature gate-array die which contains all digital functions. Digital blocks are synthesized from behavioural HDL using the high-temperature HT2000 toolkit and design platform.

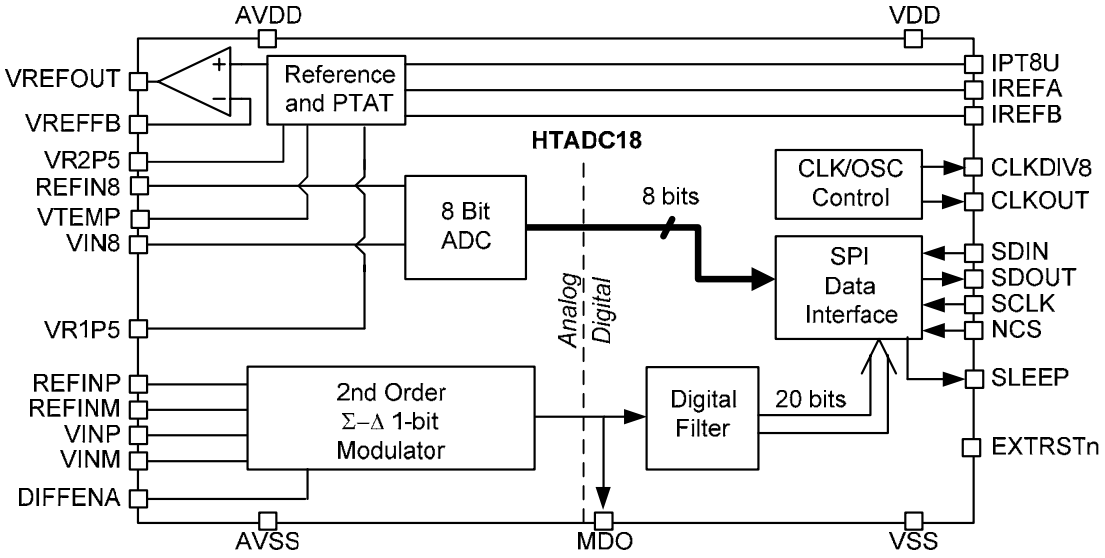


FIGURE 1: Deep Trek High-Resolution A-to-D (HTADC18) Block Diagram

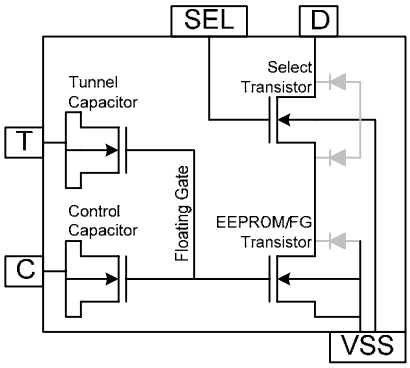
Two design iterations of the HTADC18 have been completed. After a final assembly process flow is developed the HTADC18 will be capable for commercial sale in a 28-pin DIP package.

The 12-bit A-to-D converter is a successive approximation A-to-D based using an embedded capacitive charge re-distribution DAC. This recently fabricated design is an extension to 12-bit resolution of the auxiliary 8-bit ADC that is embedded within the Deep Trek HTADC18. Prototype evaluation over temperature shows a repetitive non-linearity that occurs with every 64 output codes. This is most likely caused by a systematic matching error in the capacitor array of the DAC. Including this error, overall linearity is within plus/minus 2.5 LSB's. This should be easily improved to plus/minus 1.5 LSB's assuming that the systematic DAC error can be identified and eliminated.

High-temperature EEPROM

A high-temperature non-volatile memory was one of the chief component objectives of the Deep Trek High-Temperature Electronics program. The resulting high-temperature EEPROM (HTEEPROM) development was logistically constrained to an approach that could be implemented in the Deep Trek HTSOI wafer process flow with no additional processing steps. For this reason a single-poly floating gate structure was chosen as the basis for a non-volatile memory cell.

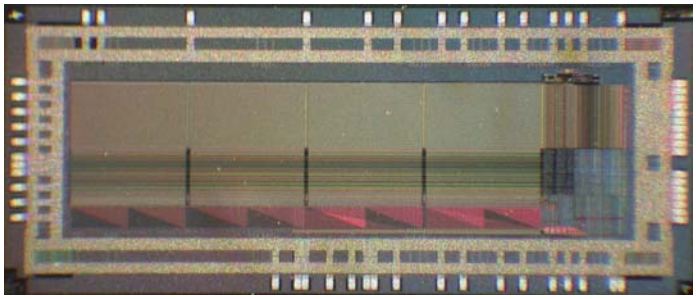
During the course of the program three cycles of design and fabrication have been completed. The first was focused on development and characterization of single-poly floating-gate memory cells (see Figure 2). EEPROM operation is based upon shifting the threshold voltage of floating-gate transistors by adding or removing charge by Fowler-Nordheim tunnelling. The threshold shift is read by turning on the floating gate device by capacitive coupling and detecting the difference in current resulting from a positively versus negatively shifted transistor threshold. Memory cell structures selected for further development were tested for data retention at 250°C for over 11,000 hours.



- **Charge is added or removed from the floating gate by Fowler-Nordheim tunneling through the tunneling capacitor oxide (voltage applied to terminals "T" and "C"**
- **Net effect is an apparent threshold voltage shift in the EEPROM transistor**
- **Memory cell is read by turning on the EEPROM transistor by capacitive coupling using the Control Capacitor**
- **Drain current is sensed to detect the difference between a "programmed" cell (stored 1) and an "erased" cell (stored 0)**

FIGURE 2: Single-poly Floating Gate Memory Cell

After the first round of silicon (focused on memory cell development), a second round of silicon was dedicated to a test-chip that focussed on arraying cells into a typical product configuration and validating means for accessing individual cells within the array for reading and writing. The demonstration vehicle was a 32Kbit memory array accessible as a 4K by 8 bit memory. This incorporated high-voltage row/column interface circuitry required for memory cell writing. High-voltage generation and waveform shaping for memory cell program/erase were generated off-chip. This demonstration memory (Figure 3) was used to verify capability for reading and writing over the full temperature range as well as further testing of data retention and data cycling in the array.



- **Off-chip program/erase waveform generation**
- **Demonstrated read/write at 250°C**
- **Data retention testing >500hrs @250°C**
- **Memory array program/erase to 100K cycles**

FIGURE 3: 32Kbit Demonstration Memory Array

Based on results from these first two test chips, a 32K x 8 HTEEPROM product design has been designed and fabricated. By means of a configuration input pin, this memory can be configured for either parallel or serial interface. The parallel interface incorporates the functionality of industry standard 28C256 parallel memories (see Figure 4). In addition it adds six I/O that are dedicated for use with the High-Temperature FPGA (these are identified by the blue font in the table embedded in Figure 4). These I/O enable the HTEEPROM to serve as a non-volatile programming device (i.e., configuration memory) for the High Temperature FPGA, capable of autonomously configuring the FPGA on power-up. The HTEEPROM also adds pins for connection to external capacitors that are required for the charge pumps that generate the high-voltage (plus/minus 8.25V) supplies needed to write the HTEEPROM.

Pin Name	Description
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
FPOR	**FPGA Power On Reset**
CCLK	**Configuration Clock**
ERR	**Configuration error flag**
CON	**Configuration Handshake**
DEFCON	**Enable FPGA SRAM Check**
CHECK	**Start SRAM Check Cycle**
A0-A14	Address Inputs
D0-D7	Data Inputs/Outputs

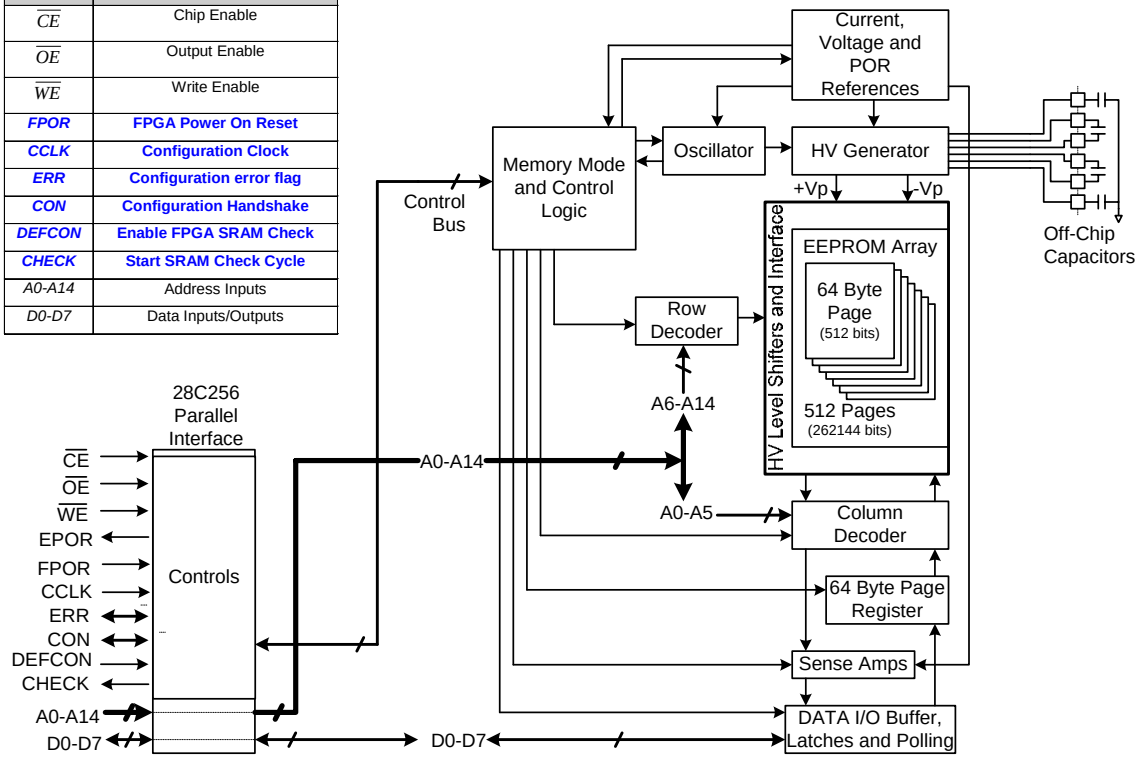
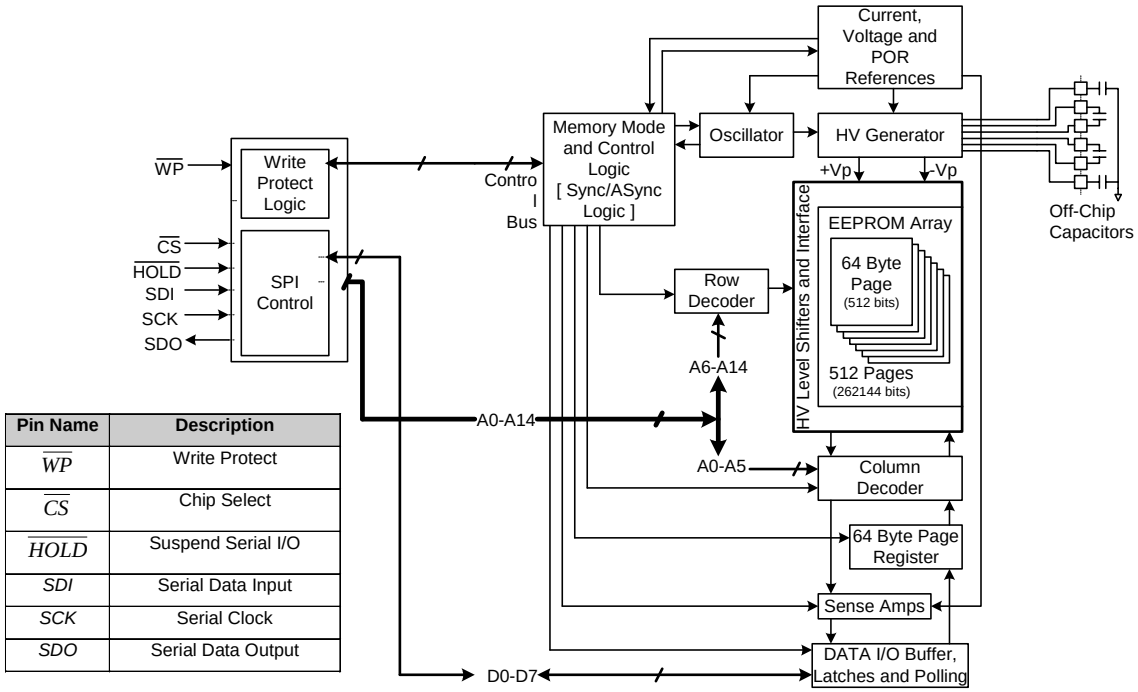


FIGURE 4: HTEEPROM Parallel Interface Configuration
(Signals listed in blue font are used for High-temperature FPGA configuration)

The serial interface configuration is shown in Figure 5. Comparison to figure 4 shows that the core functionality is not changed between the two approaches. A small amount of logic is added to the core to implement the serial interfaced control shown in Figure 5. The serial configuration incorporates the functionality of industry standard 25C256 memory devices.



Pin Name	Description
$\overline{WP}$	Write Protect
$\overline{CS}$	Chip Select
$\overline{HOLD}$	Suspend Serial I/O
SDI	Serial Data Input
SCK	Serial Clock
SDO	Serial Data Output

FIGURE 5: HTEEPROM Serial Interface Configuration

The complete 32K x 8 HTEEPROM product design has recently completed fabrication. Design verification testing will be completed during the second half of 2007. It is expected that this design will be commercialized in the form of deliverable die as well as in packages. Package development has yet to be completed.

High-temperature Multi-chip Module / RPDA Project

Honeywell was awarded a second Deep Trek project in 2006 that focuses on packaging aspects of high-temperature electronics. This new project is entitled Re-configurable Processor for Data Acquisition (or RPDA). The objective is to develop a rugged co-fired ceramic multi-chip module suitable for down-hole oil and gas exploration and/or down-hole permanent installation applications. The RDPA package will house the Deep Trek High-temperature FPGA, the HTEEPROM, and a previously developed high-temperature SOI 32K by 8 bit SRAM (HT6256). The floor-plan of the top-view looking into the RPDA package is shown in Figure 6. The underside of this package is populated with 147 pins arranged as a 7 by 21 grid on 0.1 inch spacing. In addition to the FPGA, EEPROM and SRAM, the package also will house ceramic chip capacitors required for the EEPROM charge pumps as well as power-supply transient by-pass capacitors. These capacitors, as well as all other components and materials will be capable for use at 225°C or higher.

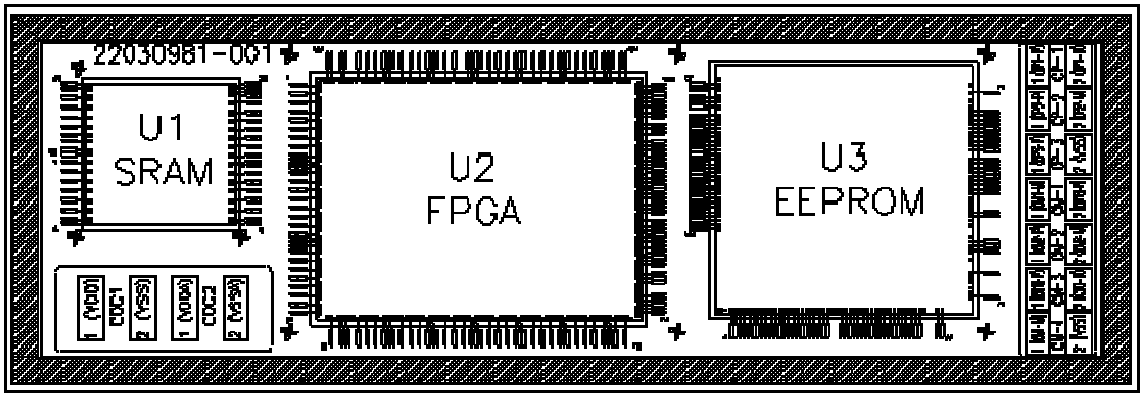


**FIGURE 6: RPDA Package Component Floorplan, Top View.
Overall dimensions are 5.558 cm by 1.905cm**

The RPDA package will have multiple layers of embedded interconnect. The inter-connect and I/O assignment are designed so that comprehensive testing of the individual IC's can be performed after all components have been assembled in the package. The FPGA and EEPROM interconnect will facilitate configuration of the FPGA by multiple modes, including autonomous configuration of the FPGA using data that can be pre-loaded into the EEPROM. The package will provide 55 fully configurable I/O which the user can define according to the FPGA configuration. An additional 57 I/O will have direct access to the SRAM and/or EEPROM, but can also be configured by the user. At this writing the MCM package is in the final design phase, and fabrication is planned for completion in early 2008.

In addition to the package development, the RPDA program also is chartered to develop and demonstrate configuration of the RPDA for a data acquisition function. At this time the planned configuration targets using the RPDA module to control and capture data from an external HTADC18 A-to-D converter under sampling schedules that may be established remotely via a master SPI control device. By the completion of the program in the first half of 2008 the RPDA package will be developed, fully assembled, and demonstrated in both an un-configured state as well as configured for the targeted data acquisition functional demonstration.

Summary

U.S. government and industry collaborative research under the Deep Trek programs have resulted in the successful development of SOI technology and design infrastructure for applications up to 250°C, including a family of high-temperature mask-programmable gate arrays. These have been utilized for the development, prototyping, and high-temperature functional and parametric validation of multiple components. These components, important for the realization of practical down-hole electronic systems, include high temperature versions of a dual precision amplifier, two complete A-to-D converters, and a field-programmable gate array. In addition, technical feasibility has been established for high-temperature non-volatile memory in the HTSOI process, and this has resulted in the design and fabrication of a complete 32K by 8 HTEEPROM that is currently in design verification. Additional development under the Deep Trek program will result in a rugged package suitable for down-hole applications to house multiple components in order to develop a flexible Reconfigurable Processor for Data Acquisition (RPDA). All of these items, including design tools, wafer foundry access, and components are planned to be accessible by commercial channels within six to twelve months.

Acknowledgements

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The authors would also like to thank the member companies of the Deep Trek High Temperature Electronics Joint Industrial Participation (JIP) consortium for financial and technical support. JIP members have been: BP, Baker Hughes, Goodrich Aerospace, Halliburton (through 2005), Honeywell, IntelliServ, Quartzdyne, and Schlumberger.

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Appendix 7

Honeywell

High Temperature 18-bit Differential Input ΣΔ ADC with Built-in Clock, Voltage Reference and SPI Interface

HTADC18

Advanced Information

The HTADCSD18 is an 18-bit, fully differential, bipolar input Analog-to-Digital Converter (ADC) designed for high-temperature environments (> 200ºC) using sigma-delta architecture and Honeywell's proprietary High-Temperature Silicon-on-Insulator (HTSOI) process. Full Scale (FS) input range can be up to ±1.5V using the differential reference inputs or it may also be operated in single-ended (VSS-referenced) mode at 1-bit lower resolution.

The HTADCSD18 includes laser trimmed, on-chip, precision 1.5 V and 2.5V voltage references, an adjustable (1.5V to 4.5V) buffered voltage reference, reference current sources, and temperature signal for monitoring chip temperature. All reference signals (voltage and current) are generated from a common master voltage reference. When used as a means for biasing external bridge-transducers this allows for ratiometric measurement systems that are 1st-order independent of reference voltage and/or reference drift with time and temperature.

Chip temperature can be monitored using an auxiliary 8-bit ADC. The 8-BITs representing the on-chip temperature, with a resolution of 1.4ºC, are made available through the SPI interface. Alternatively, an external signal can be digitized by the auxiliary 8-bit ADC. ADC clocks are generated on-chip, with no external components required. Clock and Modulator data are accessible on external pins.

The HTADC18SD can be put into a low-current "sleep" mode to save power. Data exchange, control of ADC conversion, and sleep states are supported through a 4-wire Serial Peripheral Interface (SPI).

APPLICATIONS

Down-Hole Measurement Applications, Strain Gauge Transducers, RTD Temperature Sensing, High Temperature Instrumentation, High Resolution Data Acquisition, and Low Power Measurement Applications

FEATURES

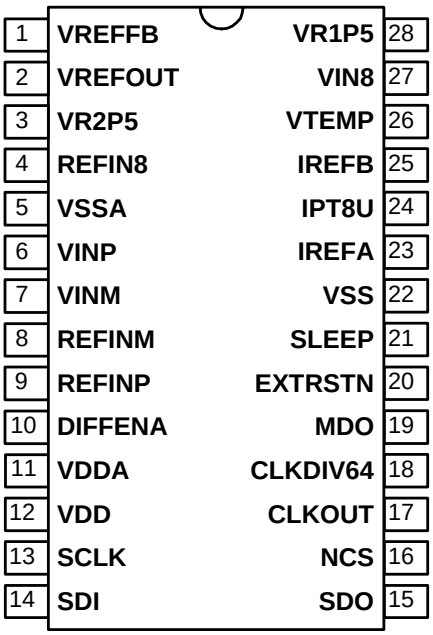
- 18-bit ADC in 28 Pin DIP package
- 2nd Order ΣΔ Architecture
- Complete on-chip digital filtering and data formatting
- 18-bit Output Date Rate 100Hz with Internal Clock (45 Hz signal bandwidth)
- -55 °C to 225°C (Ambient) Operating Range (reduced accuracy below 0 °C)
- Fully Differential Input and Reference
- Optional single-ended Input Mode
- 1-bit Modulated Data Output Supports Test and/or user-defined Off-Chip Digital Filters
- Low Current Sleep State When Not Performing A-to-D Conversion
- Single Supply 5 V Operation
- 4-wire SPI Data & Control Interface
- Single Pin Clock Selection (Internal Oscillator or External Clock)
- On-Chip 1.5 V Precision Voltage Reference
- PTAT* Current Source Output
- Utility Reference Current Sources
- Auxiliary 8-bit ADC
- 6.4 KHz 8-bit ADC Output Data Rate
- Temperature Measurement via Built-In 8-bit ADC (~1.4 °C resolution)
- 15mA to 20 mA Maximum Supply Current (depending on operating mode)

* Proportional to Absolute Temperature (PTAT)

HTADC18

PINOUT DIAGRAM

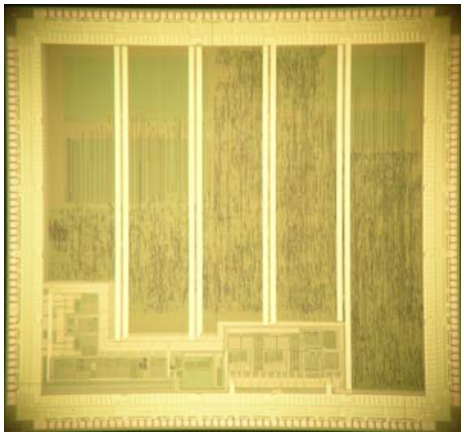
HTADCSD18



Top View

PIN NAME	FUNCTION
VREFFB	Adjustable Reference Feedback Input
VREFOUT	Adjustable (1.5V to 4.5V) Reference Output
VR2P5	2.5V Reference Output For Use With 8-bit ADC
REFIN8	8-bit ADC Reference Voltage Input
VSSA	Analog Circuit Ground (0 V)
VINP	18-bit ADC Analog Voltage Input, Positive
VINM	18-bit ADC Analog Voltage Input, Negative
REFINM	18-bit ADC Reference Voltage Input, Positive
REFINP	18-bit ADC Reference Voltage Input, Negative
DIFFENA	Differential Operation Enable Input
VDDA	Analog Circuit Power Supply (5 V)
VDD	Digital Circuit Power Supply (5 V)
SCLK	SPI Clock Input
SDI	SPI Data Output
SDO	SPI Data Input
NCS	SPI Data Chip Select Input (active low)
CLKOUT	Modulator Clock Output (204.8 KHz)
CLKDIV64	1/64th Frequency Clock Output (3.2 KHz)
MDO	Sigma-Delta Modulator 1-bit Data Output
EXTRSTN	External Global Reset Input (Active low)
SLEEP	Sleep State Output
VSS	Digital Circuit Ground (0 V)
IREFA	Reference Current Source Output A
IPT8U	PTAT Current Source Output, 8 μamps @ 25°C
IREFB	Reference Current Source Output B
VTEMP	Temperature Output
VIN8	8-bit ADC Voltage Input, Single Ended
VR1P5	1.5V Reference For Single-ended Conversion

DIE PHOTO



Find out more

For more information on Honeywell's High Temperature Electronics visit us online at www.ssec.honeywell.com/hightemp, or contact us at 800-323-8295 or 763-954-2474. Customer Service Email: ssec.customer.service@honeywell.com.

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Form #900336
January 2006

Appendix 8

Honeywell

High Temperature Dual Operational Amplifier HTOP01

PRELIMINARY

DESCRIPTION

The HTOP01 is a precision low power op amp, offering very low input offset voltage and drift over an operating temperature range of -55°C to 225°C. Using auto-zeroing techniques input offset voltage is continuously sampled and compensated, providing near perfect offset voltage compensation over temperature and time.

An internal oscillator and logic provides all necessary auto-zero clock signals, and no external capacitors are needed.

The internal auto-zero clock generator produces a pseudo-random clock frequency operating between 2kHz – 4kHz that effectively "spreads out" the clock noise frequency spectrum over a 2kHz span. This greatly reduces detectable clock noise in the amplifier's output spectrum.

Additionally, an external clock input pin (XCLK) is provided along with a select input pin (SEL) to choose between the internal clock and an optional external clock.

The external clock option allows timing flexibility for synchronously sampled systems, where no clock energy can be tolerated in the sampled amplifier output.

To save power, a power shutdown pin (SHDN) de-powers all analog circuitry when asserted (active high). The current with SHDN asserted is <150μA over temperature.

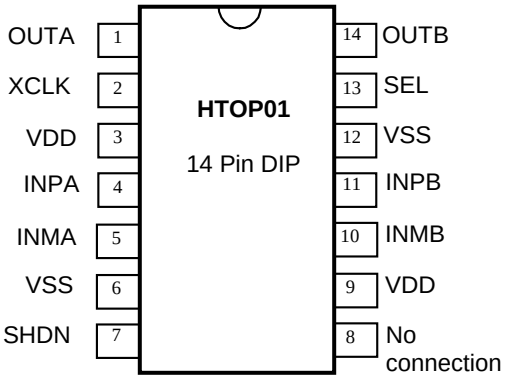
APPLICATIONS

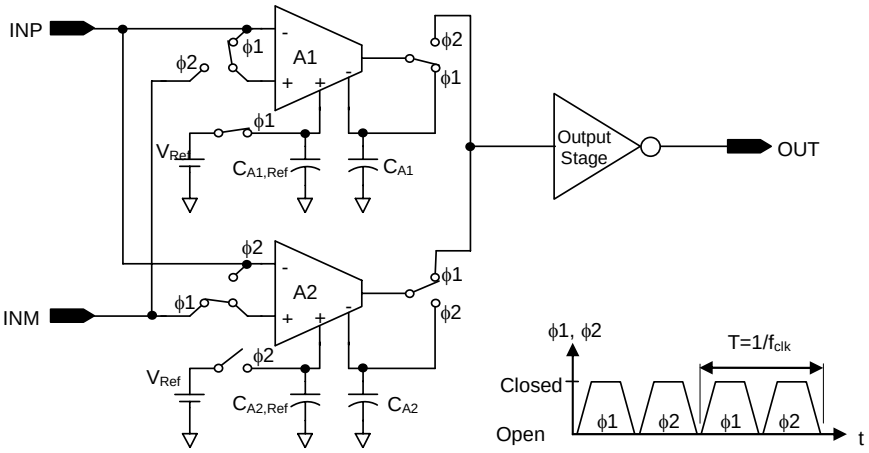
- Downhole Drilling Measurement and Production Tools
- Strain Gauge Transducers
- RTD Temperature Sensing
- High Temperature Instrumentation
- High Resolution Data Acquisition
- Low Power Measurement

FEATURES

- -55°C to 225°C Ambient Temperature Range
- Continuous Input Offset Voltage Auto-Zeroing With Internal Clock
- Input Offset Voltage ±100μV Max Over Temperature
- Input Offset Drift 0.2μV/°C Max
- High Gain, CMRR: 100dB Min
- Available in 14 lead DIP package
- Gain-Bandwidth Product: 2.0MHz Typical
- Single 5V Supply Operation
- 5.0mA maximum Supply Current
- Power shutdown pin provided
- External clocking option for synchronous systems

FUNCTIONAL BLOCK DIAGRAM





SIGNAL DESCRIPTION

Pin Name	Pin Number	Description
SEL	13	Digital input pin. Selects either internal clock (SEL=0) or externally applied clock (SEL=1).
XCLK	2	Digital input pin. External clock input. When SEL=1, XCLK is enabled, and the internal ping-pong amplifier action occurs on each XCLK edge. When SEL=0, XCLK is disabled. When not used, XCLK should be connected to VDD or VSS.
SHDN	7	Digital input pin. Power Shutdown control input. When SHDN=1, all analog circuitry is de-powered/disabled, and only leakage current will flow into VDD. When SHDN=0, normal circuit operation occurs.
INPA, INPB	4, 11	Non-inverting amplifier inputs for amplifier “A” and “B” respectively.
INMA, INMB	5,10	Inverting amplifier inputs for amplifier “A” and “B” respectively.
OUTA, OUTB	1, 14	Amplifier “A” and “B” outputs.
VDD	3, 9	Positive supply connection.
VSS	6,12	Negative supply connection.
No connect	8	Pin not used.

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter		Rating		Units
			Min	Max	
VDD	Supply Voltage (2)		-0.5	6.5	Volts
VPIN	Voltage on Any Pin (2)		-0.5	VDD+0.5	Volts
TSTORE	Storage Temperature		-65	300	°C
IOUT	Average Output Current			50	mA
ESD	Electrostatic Discharge Protection Voltage (3)		2000		V
PJC	Package Thermal Resistance (Junction-to-Case)	14 Pin DIP		2.0	°C/W

(1) Stresses in excess of those listed above may result in immediate permanent damage to the device. These are stress ratings only, and operation at these levels is not implied. Frequent or extended exposure to absolute maximum conditions may affect device reliability.
(2) Voltage referenced to VSS.
(3) Class 2 Electrostatic Discharge (ESD) input protection voltage per MIL-STD-883, Method 3015

RECOMMENDED OPERATING CONDITIONS (1)

Symbol	Parameter	Description			Units
		Min	Typ	Max	
VDD	Supply Voltage	4.5	5.0	5.5	Volts
TC	External Package Temperature	-55	25	225	°C
VPIN	Voltage on Any Pin	-0.3		VDD+0.3	Volts

(1) Voltages referenced to Vss.

ELECTRICAL CHARACTERISTICS

V_{DD}=5V, V_{SS} =0V unless otherwise noted. Values apply over the full –55°C to 225°C ambient temperature range except where denoted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	SEL=0 (Internal Clock) See Note 6			100	µV
ΔV_{OS}	Average Input Offset Voltage Drift				0.2	µV/°C
I_B	Input Bias Current	T_A = 25°C T_A = -55°C to +225 °C See Note 1		±10	±50 ±150	pA nA
I_{OS}	Input Offset Current	T_A = 25°C T_A = -55°C to +225 °C See Note 1		±10 ±1		pA nA
e_n	Input Noise Voltage	RS=100Ω, 0.1Hz – 10Hz, SEL=0 See Note 6		5.7		µV rms
I_R	Input Range		V_{SS}		V_{DD} - 2.0	Volts
CMRR	Common Mode Rejection Ratio	VCM = 0V to V_{DD} – 2.0V (Measured at DC)	100			dB
PSRR	Power Supply Rejection Ratio	V_{SS} = 0, 4.75V ≤ V_{DD} ≤ 5.25V (Measured at DC)	90			dB
A_{VOL}	Large Signal Voltage Gain	RL = 10kΩ (Measured at DC)	100			dB
GBWP	Gain-Bandwidth Product	RL = 10kΩ, CL = 20pF		2.0		MHz
SR	Slew Rate	RL = 10kΩ		1.5		V/µs
I_O	Output Current	Output swings (V_{DD}-0.3V) – (V_{SS}+0.3V) See Note 2	±20			mA
I_{OSC}	Output Short-Circuit Current	Output shorted to V_{DD}, V_{SS} See Note 4		±50		mA
f_{CLK}	Clock Frequency	Internally generated clock. See Note 5	1.7	2 - 4	5.2	kHz
V_{DD} - V_{SS}	Operating Supply Range		4.75		5.25	Volts
I_{SUP}	Supply Current, Total Package	See Note 3			5.0	mA
V_{IH}	Digital Input High Voltage	Applies to XCLK, SEL, SHDN pins	V_{DD} – 0.3		V_{DD} + 0.1	Volts
V_{IL}	Digital Input Low Voltage	Applies to XCLK, SEL, SHDN pins	V_{SS} – 0.1		V_{SS} + 0.3	Volts
I_{SHDN}	Supply Current w/SHDN asserted	SHDN=1			150	µA

Notes

(1) As temperature increases, current into the op amp inputs becomes dominated by leakage current from the input protect diodes. At 250°C junction temperature, diode leakage current can reach ±100nA when the input level is near VDD or VSS. Net leakage current drops significantly as the input level approaches mid-rail, and is at a minimum when the input level is precisely midway between VDD and VSS.

Additionally, the diode structures on each input are well matched to each other, and will exhibit nearly identical leakage current behavior. Consequently, offset current IOS between the two inputs is typically about ±1% of the IB level. Thus, if the input level is maintained near mid-rail, IOS is very low (<|1nA|), even at 250°C junction temperature.

(2) Output drive current capability is related to output swing magnitude. The HTOP01 will sink and source 20mA minimum over temperature with the output swinging to within 300mV of either rail. At lesser loads, the output can swing closer to the supply rails; at loads of ≤1mA, the output will reach to within ~10mV of either rail. For applications where the output remains ≥500mV away from the rails, up to ±40mA output current is available. Current limiting activates when output current exceeds approximately ±50mA.

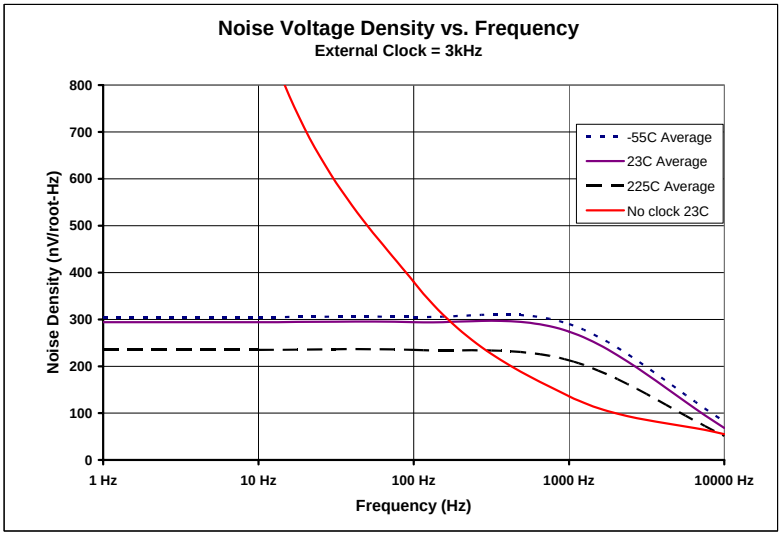
(3) Supply current consumed by each op amp is PTAT (Proportional To Absolute Temperature) in nature, and as the name suggests increases proportional to temperature. The 5.0mA maximum current given in the table reflects the maximum current consumed at 250°C junction temperature by both amplifiers. At 25°C junction temperature, supply current is typically 2mA. PTAT biasing maintains a near-constant amplifier bandwidth over temperature, a desirable characteristic.

(4) The HTOP01 is designed to handle ±50mA output current per amplifier continuously over temperature, with no reduction in rated product life. In the event of an overload condition, current limiting activates and limits output current to ~50mA nominally. However, due to fabrication process variations, the current limiting threshold can vary up to ±30%. Consequently, it is possible to have a current limiting threshold as high as ~65mA. In this situation, if the overload (65mA) is allowed to continue indefinitely at 225°C ambient, there can be a reduction in rated product life. For maximum product life, it is recommended that any overload output current situation (>50mA) be attended to promptly.

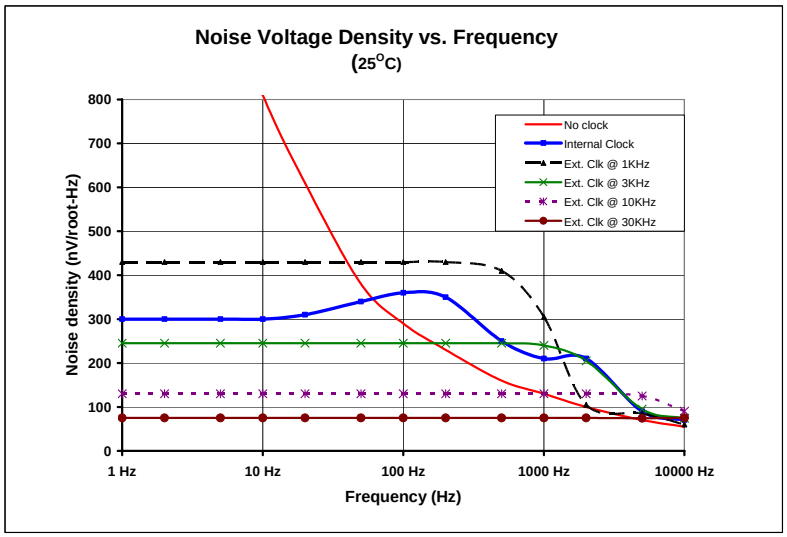
(5) The amplifier auto-zero clock is derived from an on-chip oscillator running at a nominal frequency of 4.0MHz.

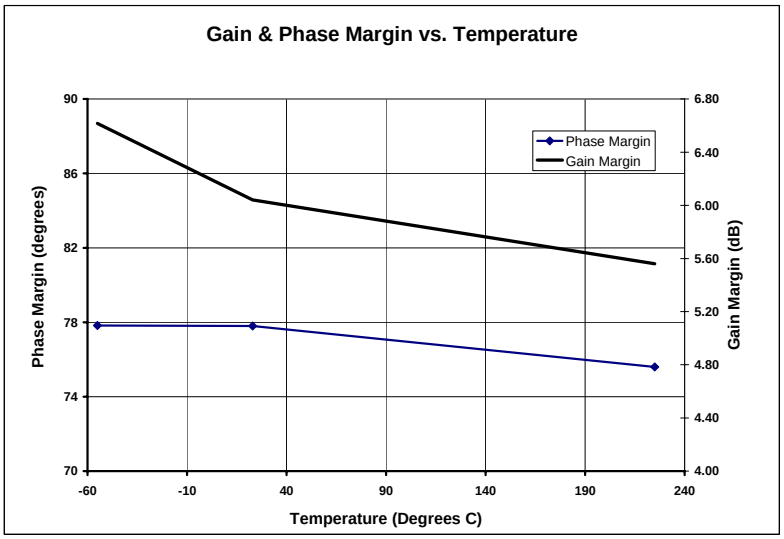
(6) With SEL=0 the HTOP01 uses an internally generated clock for offset compensation. Setting SEL=1 and using an external clock provides superior offset performance over the internal clock. The recommended frequency range for an external clock is from 4KHz to 100KHz. Optimum performance is achieved with an external clock frequency of approximately 30KHz.

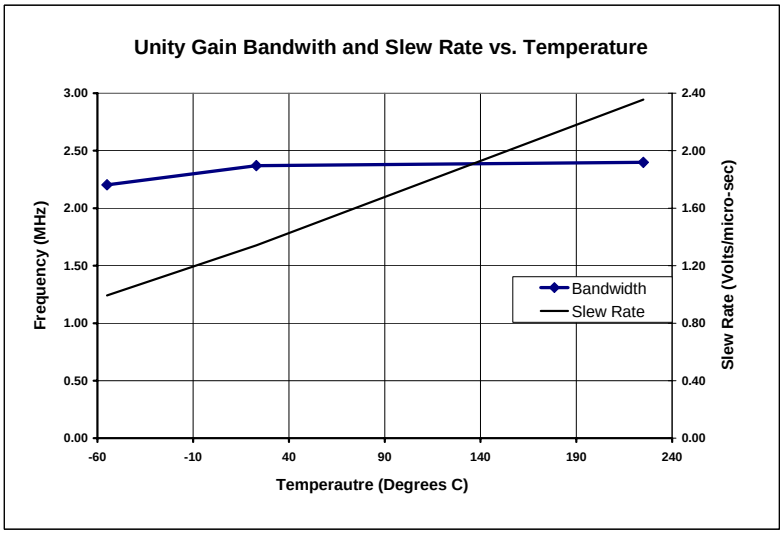
TYPICAL PERFORMANCE PLOTS



TYPICAL PERFORMANCE PLOTS

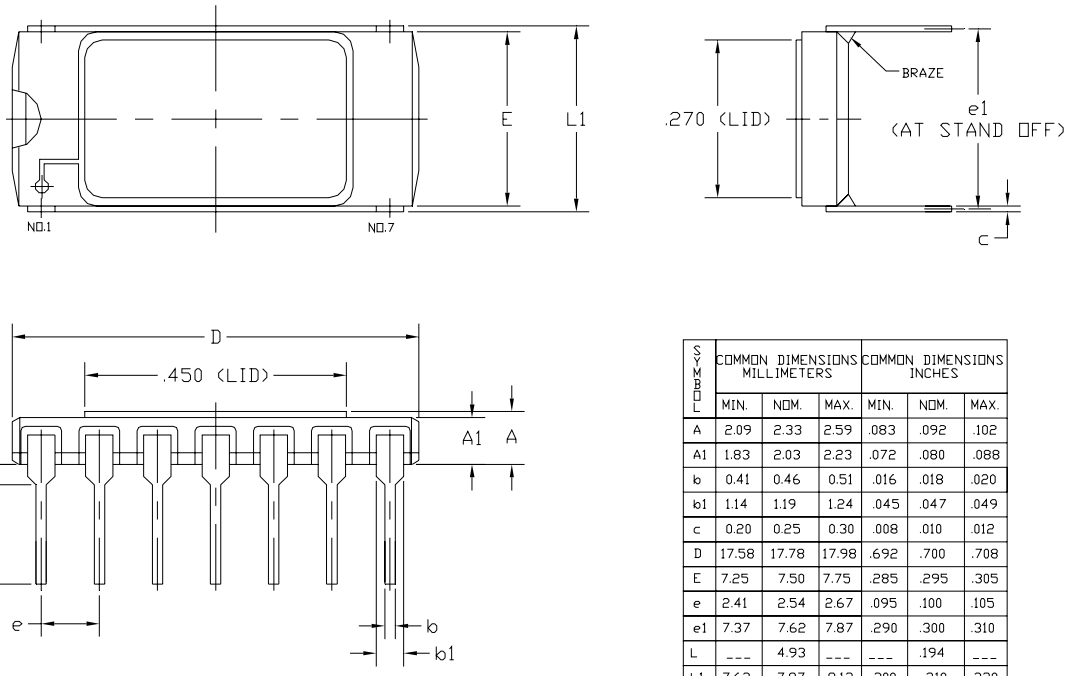






PACKAGE INFORMATION

14 Lead Ceramic DIP Package



SYMBOL	COMMON DIMENSIONS MILLIMETERS			COMMON DIMENSIONS INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	2.09	2.33	2.59	.083	.092	.102
A1	1.83	2.03	2.23	.072	.080	.088
b	0.41	0.46	0.51	.016	.018	.020
b1	1.14	1.19	1.24	.045	.047	.049
c	0.20	0.25	0.30	.008	.010	.012
D	17.58	17.78	17.98	.692	.700	.708
E	7.25	7.50	7.75	.285	.295	.305
e	2.41	2.54	2.67	.095	.100	.105
e1	7.37	7.62	7.87	.290	.300	.310
L	---	4.93	---	---	.194	---
L1	7.62	7.87	8.12	.300	.310	.320
Q	0.64	0.89	1.14	.025	.035	.045

APPLICATION NOTES

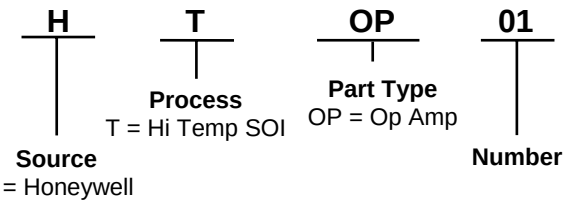
1. SUPPLY BY-PASS CAPACITANCE

In order to minimize the effects of supply-coupled clock noise on amplifier output it is recommended that a supply by-pass capacitor with low equivalent series resistance be connected between VDD and VSS.

2. INPUT IMPEDANCE MATCHING

At high temperature input currents into the HT0P01 will increase due primarily to leakage of the input ESD protection diodes. It is therefore helpful to minimize and/or balance input impedance to avoid voltage offsets from input current flowing in external connections.

ORDERING INFORMATION [(1)]



Notes

1. Bare die deliverable is an option with the HTOP01. Contact factory for more information and availability.

Find out more

For more information on Honeywell's High Temperature Electronics visit us online at www.honeywell.com/hightemp, or contact us at 800-323-8295 or 763-954-2474. Customer Service Email: ssec.customer.service@honeywell.com.

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