U.S. Department of Energy
FreedomCAR and Vehicle Technologies, EE-2G
1000 Independence Avenue, S.W.
Washington, D.C. 20585-0121

FY 2007

POWER MODULATION INVESTIGATION FOR HIGH TEMPERATURE (175°C–200°C) AUTOMOTIVE APPLICATION

Prepared by:

Oak Ridge National Laboratory

Mitch Olszewski, Program Manager

Submitted to:

Energy Efficiency and Renewable Energy
FreedomCAR and Vehicle Technologies
Vehicle Systems Team

Susan A. Rogers, Technology Development Manager

April 2006

OAK RIDGE
NATIONAL LABORATORY
MANAGED BY UT-BATTELLE
FOR THE DEPARTMENT OF ENERGY

ORNL/TM-2007/046

Engineering Science and Technology Division

POWER MODULATION INVESTIGATION FOR HIGH TEMPERATURE (175°C–200°C) AUTOMOTIVE APPLICATION

Dr. F. Patrick McCluskey
University of Maryland

Publication Date: April 2007

Prepared by the
OAK RIDGE NATIONAL LABORATORY
Oak Ridge, Tennessee 37831
managed by
UT-BATTELLE, LLC
for the
U.S. DEPARTMENT OF ENERGY
Under contract DE-AC05-00OR22725

UT-BATTELLE
ORNL-27 (4-00)

Final Report

Power Module Investigation for High Temperature (175°C-200°C) Automotive Application

Prepared for:

Ms. Laura Marlino
Program Technical Manager, Transportation APEEM
U.S. Department of Energy
Knoxville, TN

Principle Investigator: F. Patrick McCluskey, Ph.D.

Technical and business contact:

Dr. F. Patrick McCluskey
2811 St. John's Lane
Ellicott City, MD 21042
(410)-218-3094

March 30, 2007

Disclaimer: The information contained in this report represents the author's best knowledge at the time and is for educational purposes only. Anyone taking any action based on this information is fully responsible for that action. No liability is assumed by the author for the use of this information in any manner, whether that information be correct or incorrect and whether it be correctly or incorrectly applied.

Table of Contents

INTRODUCTION **3**

HYBRID VEHICLE AND HYBRID VEHICLE ENVIRONMENT 3
ELEMENTS OF AN INVERTER 4

COMPONENT ISSUES **9**

SEMICONDUCTORS 9
CAPACITORS 16
OTHER PASSIVES 18
PC BOARDS 20
Delamination *21*
Conductive Filament Formation *22*
Plated Through Hole (PTH) issues *24*
Surface mount versus through hole technology *25*
Limitations in number of layers *26*

PACKAGING TYPES **26**

CHIP AND WIRE PACKAGE 27
Wirebond *28*
Chip and Substrate Attachment *29*
Substrate *32*
DOUBLE SIDED ATTACH MODULE 34
PLANAR PACKAGING TECHNOLOGY 36
PRESSPAK TECHNOLOGY 38
JOHN HSU CONTACT APPROACHES 40

SUMMARY AND CONCLUSIONS **42**

COLLECTED SUGGESTIONS FOR FURTHER RESEARCH 42

REFERENCES **43**

F. Patrick McCluskey, Ph.D.
Consulting

2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

Introduction

Hybrid Vehicle and Hybrid Vehicle Environment

Hybrid electric vehicles were re-introduced in the late 1990s after a century dominated by purely internal combustion powered engines[1]. Automotive players, such as GM, Ford, DaimlerChrysler, Honda, and Toyota, together with major energy producers, such as BP-Amoco, were the major force in the development of hybrid electric vehicles. Most notable was the development by Toyota of its Prius, which was launched in Japan in 1997 and worldwide in 2001. The shift to hybrids was driven by the fact that the sheer volume of vehicles on the road had begun to tax the ability of the environment to withstand the pollution of the internal combustion engine and the ability of the fossil fuel industry to produce a sufficient amount of refined gasoline. In addition, the number of vehicles was anticipated to rise exponentially with the increasing affluence of China and India.

Over the last fifteen years, major advances have been made in all the technologies essential to hybrid vehicle success, including batteries, motors, power control and conditioning electronics, regenerative braking, and power sources, including fuel cells. Current hybrid electric vehicles are gasoline internal combustion – electric motor hybrids. These hybrid electric vehicles range from micro-hybrids, where a stop/start system cuts the engine while the vehicle is stopped, and mild hybrids where the stop/start system is supplemented by regenerative braking and power assist, to full hybrids where the combustion motor is optimized for electric power production, and there is full electric drive and full regenerative braking. PSA Peugeot Citroen estimates the increased energy efficiency will range from 3-6% for the micro-hybrids to 15-25% for the full hybrids.[2] Gasoline-electric hybrids are preferred in US because they permit long distance travel with low emissions and high gasoline mileage, while still using the existing refueling infrastructure.

One of the most critical areas in which technology has been advancing has been the development of electronics that can operate in the high temperature environments present in hybrid vehicles. The temperatures under the hood for a gasoline-electric hybrid vehicle are comparable to those for traditional internal combustion engines. This is known to be a difficult environment with respect to commercial-grade electronics, as there are surface and ambient temperatures ranging from 125°C to 175°C. In addition, some hybrid drive electronics are placed in even harsher environments, such as on or near the brakes, where temperatures can reach 250°C. Furthermore, number of temperature cycles experienced by electronics in a hybrid vehicle is different from that experienced in a traditional vehicle. A traditional internal combustion vehicle will have the engine running for longer periods, whereas a mild or micro-hybrid engine will experience many more starts and stops.[3] This means that hybrid automotive electronics will undergo more cycles of a potential wider temperature cycle than standard automotive electronics, which in turn see temperature cycles of 2 to 3 times the magnitude of the ΔT = 50°C-75°C experienced by commercial-grade electronics.

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

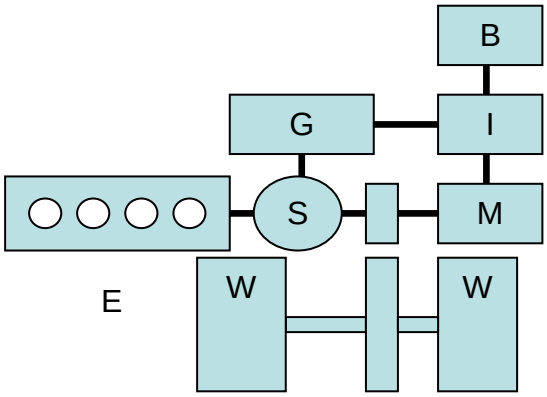
This study will discuss the effects of these harsh environments on the failure mechanisms and ultimate reliability of electronic systems developed for gasoline-electric hybrid vehicles. In addition, it will suggest technologies and components that can reasonably be expected to perform well in these environments. Finally, it will suggest areas where further research is needed or desirable. Areas for further research will be highlighted in bold, italic type.

It should be noted that the first area where further research is desirable is in developing a clearer understanding of the actual hybrid automotive electronics environment and how to simulate it through accelerated testing, thus:

Developing specific mission profiles and accelerated testing protocols for the underhood environment for hybrid cars, as has previously been done for gasoline-powered vehicles, is an important area for further study.

Elements of an inverter

Before discussing the high temperature performance and reliability of specific components and technologies, it is important to point out the elements of a typical hybrid automotive electronic system. The most advanced hybrids, such as the Toyota Prius, combine the best of both series and parallel configurations, as shown in Figure 1. When the vehicle is starting from rest, moving slowly, or going down a gradual slope - situations in which the engine does not operate efficiently – the engine is shut off. Only the electric motor powers the wheels by drawing power from the battery. Under constant-speed driving conditions, a fuel-efficient, 1.5 liter, four-cylinder engine delivers its output to both the generator and the wheels, through a planetary gear (power-split) device. The generator supplies power either to the electric wheel motors or to recharge the battery. During full throttle acceleration or under heavy load, the power from the battery is added to the power from the engine to boost the motor power driving the wheels. During deceleration or braking, the motor works as a generator to transform kinetic energy from the wheels into electrical energy to charge the battery.[4]



B = Battery (Fuel Cell)

I = Inverter

M = Motor

G = Generator

S = Power Splitter

E = Engine

W = Drive Wheels

Figure 1 A series/parallel hybrid system (Toyota THS)[4]

F. Patrick McCluskey, Ph.D.
Consulting

2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

An essential part of the hybrid drive system is the inverter, which converts DC power from the batteries/fuel cells or DC generator to AC power fed to the drive motor for the wheels. The inverter ensures the supply to the motors has a variable, controllable frequency. The inverter consists of a power semiconductor switching part that handles the main power flow through the inverter, and control circuitry that controls the power semiconductors and feeds back operating condition information to the main control center of the vehicle. The inverter in a hybrid vehicle is similar in its operation to the inverter part of a frequency converter widely used in industry.

Inverters are widely used in industry in a variety of applications, including variable frequency drives. A variable frequency drive controls the operating speed of an AC motor by using an inverter to control the frequency and voltage of the power supplied to the motor. In most cases, the variable-frequency drive includes a rectifier so that DC power for the inverter can be provided from mains AC power. Since an inverter is the key component, variable-frequency drives are sometimes called inverter drives or just inverters. It is these adjustable speed motor control inverters that are the main application for inverters in hybrid electric highway vehicles such as the Toyota Prius, as well as in some electric and diesel-electric locomotives. Various improvements in inverter technology are being developed specifically for electric vehicle applications.

There are a wide variety of inverter designs. In the simplest inverter circuit, DC power is connected to a transformer through the center tap of the primary winding. A switch is rapidly pulsed to allow current to flow back to the DC source following two alternate paths first through one end of the primary winding and then through the other. The alternation of the direction of current in the primary winding of the transformer produces alternating current (AC) in the secondary circuit. Power semiconductor devices, such as SCRs, Thyristors, GTOs, IGBTs, and transistors are used to do the switching.

The switch in the simple inverter described above produces a square voltage waveform as opposed to the sinusoidal waveform that is the usual waveform of an AC power supply. Using Fourier analysis, periodic waveforms, such as these square waveforms, are represented as the sum of an infinite series of sine waves. The sine wave that has the same frequency as the original waveform is called the fundamental component. The other sine waves included in the series, called *harmonics*, have frequencies that are integral multiples of the fundamental frequency. The quality of the inverter output waveform can be expressed by using the Fourier analysis data to calculate the total harmonic distortion (THD). The quality of output waveform that is needed from an inverter depends on the characteristics of the connected load. Some loads need a nearly perfect sine wave voltage supply in order to work properly. Other loads may work quite well with a square wave voltage.

The issue of waveform quality is addressed by using a variety of more advanced inverter designs with different power circuit topologies and control strategies. The approach selected depends on the way that the inverter is intended to be used. Capacitors and inductors can be used to filter the waveform. If the design includes a transformer,

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

filtering can be applied to the primary or the secondary side of the transformer or to both sides. Low-pass filters are applied to allow the fundamental component of the waveform to pass to the output while limiting the passage of the harmonic components. If the inverter is designed to provide power at a fixed frequency, a resonant filter can be used. For an adjustable frequency inverter, the filter must be tuned to a frequency that is above the maximum fundamental frequency.

Since most loads contain inductance, feedback rectifiers or antiparallel diodes are often connected across each semiconductor switch to provide a path for the peak inductive load current when the semiconductor is turned off. The antiparallel diodes are somewhat similar to the *freewheeling diodes* used in AC/DC converter circuits.

Modulating, or regulating the width of a square-wave pulse, called pulse-width modulation (PWM), is often used as a method of regulating or adjusting an inverter's output voltage. When voltage control is not required, a fixed pulse width can be selected to reduce or eliminate selected harmonics. Harmonic elimination techniques are generally applied to the lowest harmonics because filtering is more effective at high frequencies than at low frequencies. *Multiple pulse-width* or *carrier based* PWM control schemes produce waveforms that are composed of many narrow pulses. The frequency represented by the number of narrow pulses per second is called the *switching frequency* or *carrier frequency*. These control schemes are often used in variable-frequency motor control inverters because they allow a wide range of output voltage and frequency adjustment while also improving the quality of the waveform.

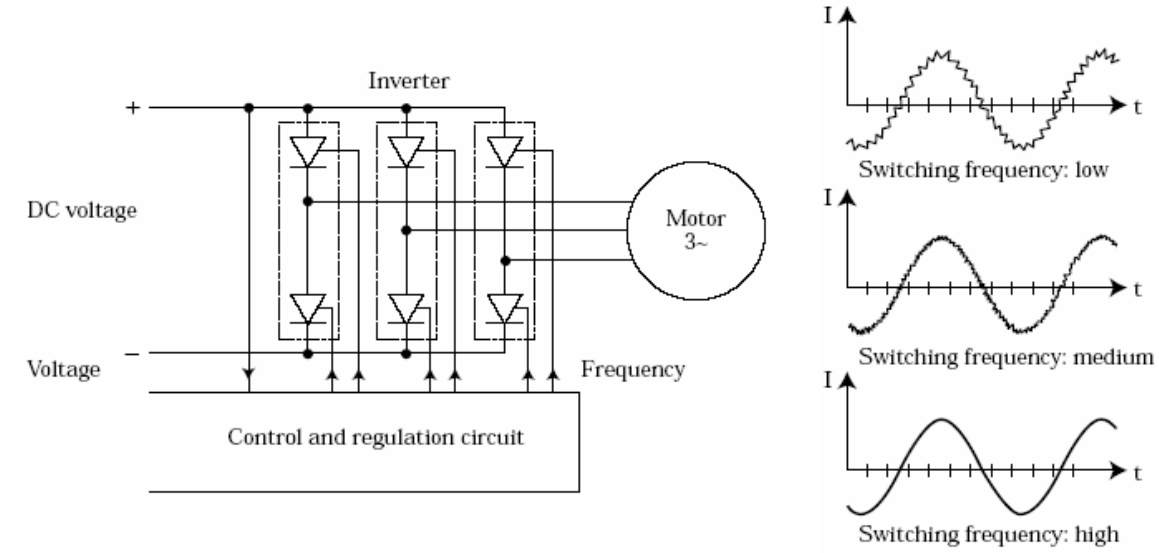


Figure 2 Inverter for variable or constant input voltage and output current dependent on the switching frequency. [5]

Three-phase inverters are used for variable-frequency drive applications and for high power applications such as HVDC power transmission. A basic three-phase inverter

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

consists of three single-phase inverter switches each connected to one of the three load terminals. For the most basic control scheme, the operation of the three switches is coordinated so that one switch operates at each 60 degree point of the fundamental output waveform. This creates a line-to-line output waveform that has six steps. The six-step waveform has a zero-voltage step between the positive and negative sections of the square-wave such that the harmonics that are multiples of three are eliminated. When carrier-based PWM techniques are applied to six-step waveforms, the basic overall shape, or *envelope*, of the waveform is retained so that the 3rd harmonic and its multiples are cancelled.

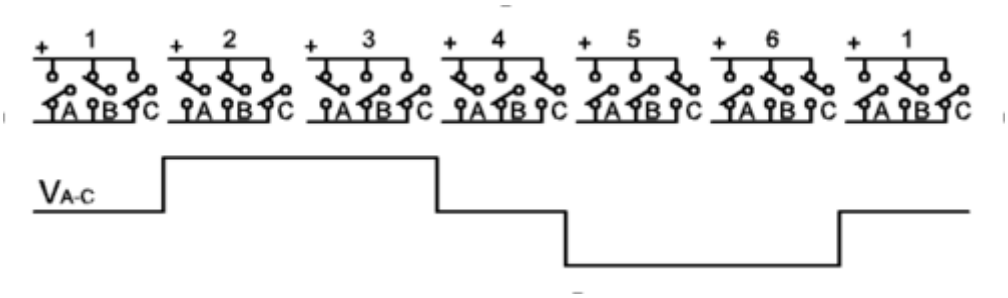


Figure 3 Three-phase inverter switching circuit showing six-step switching sequence. [5]

To construct inverters with higher power ratings, two six-step three-phase inverters can be connected in parallel for a higher current rating or in series for a higher voltage rating. Although inverters are usually combined for the purpose of achieving increased voltage or current ratings, the quality of the waveform is improved as well.

The typical three-phase inverter has 6 power semiconductors that are turned on and off by signals generated by the control circuit.[5] The inverter switching frequency is a balancing act as high frequency switching leads to high peak voltages and motor winding heating. On the other hand low switching frequency can lead to high acoustic noise. Power semiconductor switches fall into the following four main categories:

- Thyristors
- Bipolar Transistors
- Unipolar Transistor (MOSFET)
- Insulated-Gate-Bipolar Transistor (IGBT)

Bipolar transistors and Thyristors can pass large quantities of current with low on-state losses. MOSFETs provide fast switching speed with low switching losses. Today, IGBT transistors are the most widely used power switches as they combine the fast and low loss switching properties of the MOSFET with the high current carrying capability and low on-state losses of bipolar transistors and thyristors.[5] This permits them to control near thyristor levels of power at near MOSFETs switching frequencies as shown in figure 4.

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

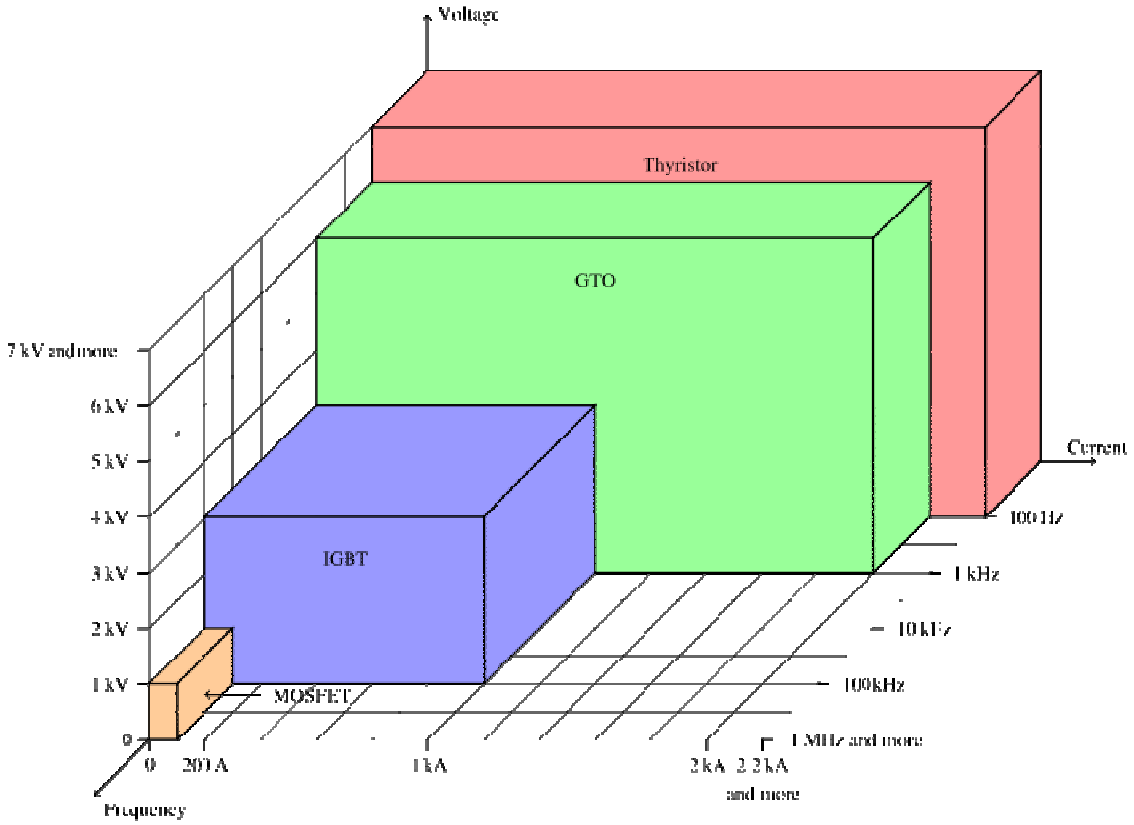


Figure 4 Power and frequency range of power transistors.[6]

Typical components for hybrid inverters make use of diodes and transistors rated for use in the 100-1200 VDC range and up to 100A, as used in frequency converters. One of the key factors in designing the circuitry for inverter drives is to keep the currents in the system as low as possible to reduce the conductive losses in the system.[7]

Silicon-based diodes and MOSFETs are available for operation over temperature ranges from -55°C to 150°C and Silicon-based IGBTs are available for operation over temperature ranges from -55°C to 175°C from a wide variety of manufacturers including ABB Semiconductor, Advanced Power Technology, Infineon, International Rectifier, IXYS, ON Semiconductor, Powerex, and others. These devices need to be capable of high temperature operation not only because of the 125°C to 175°C environment in which they are placed but also because of additional increases in temperature resulting from self-heating (i.e. Joule heating) due to power losses in the component. This is one of the major reasons why silicon carbide based power devices are now coming into widespread commercial use as well, with diodes and JFETs available for operation at temperatures to 300°C from SiCED, SemiSouth Laboratories, and Cree. SiC devices also have a number of other advantages over silicon devices for power applications besides the ability to operate reliably at higher temperatures. These include higher reverse bias blocking voltage owing to a higher dielectric breakdown field strength, faster switching

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

speed because of a higher saturated electron drift velocity, and better heat dissipation due to greater thermal conductivity.

Further effort is needed in the development of SiC MOSFETs and IGBTs and their associated packaging.

In addition to the power switches, the inverter also interfaces with control circuitry, the task of which is to turn the power switches on and off according to the chosen strategy of modulation, typically PWM. It is also the task of the control circuitry to forward input from the drive train to the main control of the car. The control circuitry consists of small signal (i.e. low voltage) semiconductors. These devices handle smaller power levels than the power switches and therefore have little self heating. However, they are often located in close proximity to the power devices or other heat dissipating components such as the brakes or engine top. Therefore, the control circuitry experiences the same harsh under-the-hood environment as the power semiconductors.

Component Issues

Semiconductors

The most fundamental limitation to the use of any semiconductor at elevated temperatures is the increasing density of intrinsic carriers, which is shown in Figure 5[8]. Intrinsic carriers arise from the thermal generation of electron-hole pairs across the entire bandgap, and they are the only carriers in a pure (undoped) semiconductor material. Semiconductor devices are based on the interaction between areas of the semiconductor that are donor doped (n-type), and those which are acceptor doped (p-type). As the temperature is increased, eventually the intrinsic carrier concentration reaches the same order of magnitude as the doping concentration. At this point, semiconductor devices become inoperable as the ability to differentiate between n and p regions is lost. One way to counteract this effect is to increase the doping density. However this has the effect of decreasing the junction width and thus decreasing the reverse bias needed for junction breakdown.

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

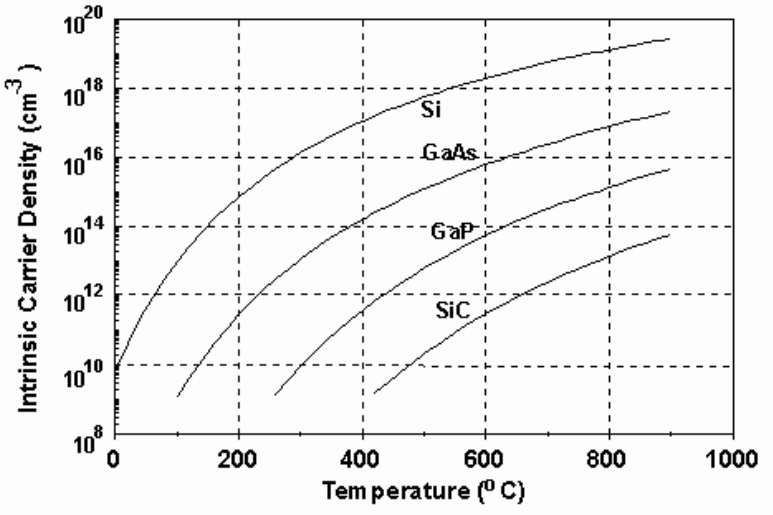


Figure 5 Effect of temperature on the intrinsic carrier concentration *[8].*

The higher intrinsic carrier concentration produces a number of adverse effects in silicon devices including increased reverse bias junction leakage current in p-n diodes, altered gain in bipolar transistors, shifts in the threshold voltage of MOSFETs, and latch-up in MOSFETs as a result of increased leakage across the p-n isolation junctions.

The increase in leakage current with increasing intrinsic carrier concentration was observed experimentally by Bromstead [9]. Bromstead found that I_{CE} leakage current in bipolar devices increases 8% /K. This increase in leakage current subsequently resulted in increased gain and decreased efficiency in bipolar devices.

It is this increase in leakage current which limits the operating temperature of power diodes, bipolar junction transistors, IGBTs, and thyristors. Silicon devices typically have a safe operating area that permits operation at junction temperatures to 175°C. This equates to ambient temperatures of up to 175°C with derating of current as the ambient temperature rises, from full current at 125°C to zero current at 175°C. Derating lessens the power generation and therefore the self-heating in the device. For temperatures greater than this, much research is ongoing into the development and use of SiC diodes, and JFETs. These devices take advantage of the wider bandgap in SiC and its corresponding smaller intrinsic carrier concentration to reduce leakage levels. Working devices have been made that can be operated reliably at temperatures to 400°C.

With the elimination of the micropipe problem, limitations to SiC power devices now rest with screw dislocation assisted reverse breakdown, ohmic contact issues, interconnection and packaging.

The effects of increased temperature on MOSFET devices include decreasing the threshold voltage. The threshold voltage decrease (dV_T/dT) in a typical n-MOSFET is 2mV/K to 6mV/K depending on the thickness of the gate oxide and the doping density [10]. The reduction in threshold voltage lessens the immunity of the circuit to noise,

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

thereby making it more likely for the device to turn on solely on the basis of a noise pulse, rather than an actual signal. Therefore, while MOSFET transistors can be used as switches at high temperatures, designs must account for reduced noise margins.

Low field carrier mobility is also degraded at elevated temperatures [11], which lowers the transconductance in MOSFETs in the linear regime below saturation. This reduces analog device gain and can slow digital device switching speeds. High temperatures can slow switching speeds even further by increasing the resistance of the metallization traces, thereby increasing the time delay due to the on-chip interconnections. This often has a greater effect than the decrease in the low field mobility.

For this reason, it is necessary to slow the clock speed of circuits containing microprocessors if they are to be used at elevated temperatures. Linear and analog devices can be used in a more straightforward manner at high temperatures, but the change in their parameters must be taken into account in the design.

Power MOSFETs, like small-signal MOSFETs, are susceptible to changes in threshold voltage, noise immunity and switching speed at high temperatures. For these reasons, typical silicon power MOSFETs are limited to temperatures less than 175°C with appropriate current derating as discussed for the bipolar devices. SiC power MOSFETs have been made that can operate at junction temperatures greater than 175°C, however, to date, the poor quality of the SiC-SiO_2 interface has produced high levels of trapping and leakage, and limited their maximum junction temperature to below 250°C.

It is the adverse effect of leakage current on CMOS devices, however, that is perhaps of the most importance to small signal controls, such as are used in the engine control, braking control, and HEV control computers. Leakage current, first and foremost, increases the susceptibility of CMOS devices to latch-up. Latch-up refers to the unintentional turning on of the parasitic SCR formed by the four layer $p^+np^-n^+$ structure between the ground and the power rail, which exists in every *p*-substrate *n*-well CMOS device. To initiate and maintain this state, a minimum value of current, called the trigger current (I_{trg}), must initially be supplied to the base of one of the transistors, and a minimum value of current, called the holding current, must continue to flow through the device. [12].

Latch-up can have devastating consequences as it shorts the power rail to ground in the particular device in which it is observed, and it can generate sufficient heat to cause other devices and/or the entire integrated circuit to fail as well. The following four factors lead to increased latch-up susceptibility at increased temperature:

- Lower values of trigger and holding currents at higher temperatures
- Higher leakage currents at higher temperatures which can serve to trigger latch-up
- Higher values of well and substrate resistances at higher temperature, causing a greater voltage drop which facilitates the feed-forward current loop.
- Increased bipolar current gains (b_n and b_p) and common base current gains (a_n and a_p) at higher temperatures which facilitate the feed-forward current loop.

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

Almost all CMOS devices succumb to latch-up at high temperatures. The temperature at which this occurs depends on the geometry and technology of the device with bulk devices beginning to exhibit latch-up at temperatures as low as 125°C, and epitaxial layer devices exhibiting latch-up at temperatures above 200°C. The most cost-effective technology providing immunity to latch-up at temperatures up to 300°C is silicon-on-insulator (SOI). Silicon-on-insulator technology uses an insulating layer such as SiO_2 to partially isolate the n-MOS and p-MOS devices, instead of relying solely on reverse biased p-n junctions. By placing the devices in epitaxial silicon on SiO_2, the junction area between the devices is reduced [13, 14]. As the leakage current across a silicon n+p junction is proportional to the junction area, a decrease in junction area significantly lowers the leakage current, ensuring latch-up immunity [13]. This decrease in leakage current is shown in Figure 6. Honeywell currently markets a line of SOI devices for high temperature and radiation-hard applications that can be used reliably for up to 5 years at 225°C, and for short periods up to 300°C.

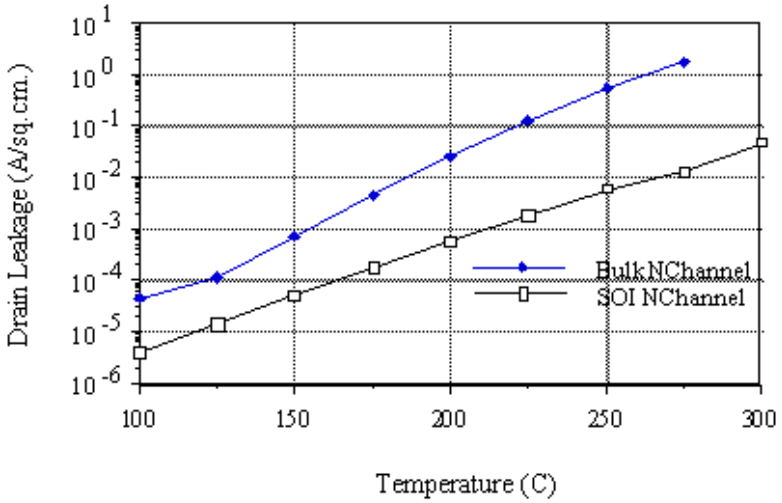


Figure 6 Temperature dependence of leakage current in bulk and SOI CMOS [13]

The effects described above limit the maximum ambient use temperature of junction isolated small-signal silicon devices to 175°C -200°C.[15] However, the performance of silicon devices at the highest levels of integration may begin to degrade at even lower temperatures. 200°C operation depends on circuit design tailored for high temperature applications, which includes scaling the gate in channel length to improve the transconductance, while increasing the channel width to inhibit latch-up. Other high temperature design rules include providing adequate spacing, aligning transistors source to source, and using guard structures [16].

While understanding parameter shifts in silicon devices is critical to using them at elevated temperatures, it is also important to address the more insidious reliability concerns. Time dependent dielectric breakdown of the gate oxide in a MOSFET is accelerated at elevated temperatures [17], and can cause failure of the device in several hours at 200°C and 8 MV/cm field strength. However, decreasing the field strength to 2 MV/cm, removes this concern [10]. The appropriate choice of oxide thickness can thus reduce the electric field sufficiently to eliminate high temperature concerns. However,

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

with today's extremely small channels and correspondingly scaled effective oxide thicknesses of less than 2 nm, it becomes increasingly difficult to limit the occurrence of this failure mechanism at elevated temperatures. The decreasing gate voltage (from 5V → 2.5 V or less) does help somewhat to mitigate this concern.

Similar tradeoffs must be addressed for electromigration. Aluminum, the primary metallization for silicon systems, is resistant to electromigration in highly integrated devices at temperatures below 150°C. By designing for high temperature use, which includes increasing the cross-section of the lines and using lower current densities, concerns can be avoided up to 250°C [9]. However, new microprocessors contain copper metallization, which, when processed correctly with good adhesion to the underlying dielectric, promises greater electromigration resistance and lower resistivity. However, poor adhesion of the copper to the underlying dielectric can actually lower electromigration resistance over that seen in aluminum metallization.

Furthermore, high temperature ohmic contacts to SiC and the resistance of the gold-based metallizations to electromigration are topics requiring additional study.

While the above discussion provides absolute limits to the use of silicon devices and other device technologies, most small-signal semiconductor devices in widespread circulation today are specified for use in the "commercial" 0 to 70°C, and to a lesser extent in the "industrial" -40 to 85°C, operating temperature range, thus satisfying the demands of the computer, telecommunications, and consumer electronics and their markets. There is, however, demand for parts rated beyond the "industrial" temperature range, primarily from the aerospace, military, oil and gas exploration, and automotive industries. However, the demand is often not large enough to attract and retain the interest of major semiconductor part manufacturers in producing extended temperature range parts.[18] Nevertheless, a method has been suggested to enable the use of commercial-off-the-shelf control circuitry semiconductor devices at an elevated temperature condition, such as the automotive underhood environment. This is to apply uprating methodologies to packages specified to more common temperature ranges. Uprating may permit the use in harsher environments of components that incorporate the latest technological advancements in the electronics industry in terms of performance, cost, size, and packaging styles.

The discussion of uprating in this document is not meant to be an endorsement of this procedure and is only submitted for educational purposes.

Electronic parts are currently being used outside their specifications in many applications and industry sectors [19, 20], such as oil and gas exploration and recovery, home appliances and commercial, avionics and defense electronics among others. Uprating has been successfully implemented in several government and air transport products (e.g., avionics for Boeing 777) since 1994 [21]. Even the Federal Aviation Authority (FAA) of the United States conditionally accepts the use of parts outside the manufacturer's specifications. It states that "If the declared installation temperature environment for the EEC (Electrical and Electronic Components) is greater than that of the electronic parts

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

specified in the engine type design, the applicant should substantiate that the proposed extended range of the specified components is suitable for the application."

On the other hand, some electronic part manufacturers are critical of the use of parts outside their ratings. National Semiconductor, for example, states that using parts in applications or environments for which they were not intended can lead to part or system failure. National Semiconductor strongly recommends that its products be used only within the electrical and environmental limits published in their respective datasheets [22]. Intel has also stated that it will not accept any legal responsibility for failures that occur due to the deliberate misuse of its products, including any damages resulting from the practice of uprating. Similarly, there are warnings from other manufacturers and trade associations such as Analog Devices [23], Xilinx[24], Texas Instruments [25, 26], and Semiconductor Industry Association (SIA)[27].

Parts are uprateable for temperature because part manufacturers generally provide a margin between the recommended operating temperature specification of a part and the actual temperature range over which the part will operate. This margin helps maximize part yields, reduce or eliminate outgoing tests and optimize sample testing and statistical process control (SPC). Sometimes this margin can be exploited, and thus the part can be uprated. For example, Motorola notes [28] that, "There is no manufacturing difference between PEMs (plastic encapsulated microcircuits) certified from 0 to 70^{o}C and those certified from -55 to 125^{o}C. The same devices, the same interconnects, and the same encapsulants are used. The only difference is the temperature at which the final electrical testing is done." In fact, many electronic parts manufacturers have used the same die for various "temperature grades" of parts (commercial, industrial, automotive, and military). For example, Intel[29] stated in their military product data book: "there is no distinction between commercial product and military product in the wafer fabrication process. Thus, in this most important part of the VLSI manufacturing process, Intel's military products have the advantages of stability and control which derive from the larger volumes produced for commercial market. In the assembly, test and finish operations, Intel's military product flow differs slightly from the commercial process flow, mainly in additional inspection, test and finish operations."

The best way to see if a part is uprateable, is to obtain the simulation and characterization data from the part manufacturers. The data include product objective specifications, product and packaging roadmaps, device electrical simulation models, and temperature characterization data. Depending on the part manufacturer, some of these data are available freely, while other may be available upon request or in some cases by signing a non-disclosure agreement.

The effects of temperature (and other factors such as voltage and frequency) on different electrical parameters can be estimated using models available from part manufacturers. Often the device electrical simulation models are made available to the public, although the models are often 'sanitized' so that any proprietary information is masked [30]. Simulation models of devices can be used to calculate the effects of temperature variation on device parameters (e.g., the BSIM3 model for short channel MOSFETs) [31]. Device

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

simulations therefore can be used to estimate if the part will be uprateable, and what parameter changes may be expected at application operating conditions.

There are three types of uprating (viz. parameter conformance, parameter re-characterization, and stress balancing). Parameter conformance is a process of uprating in which the part is tested to assess if its functionality and electrical parameters meet the manufacturer's recommended operating conditions over the target temperature range. The tests are of a "go/no-go" type, and are generally performed at the upper and lower ends of the target application conditions. A margin may be added to the test, either in a range wider than the target application conditions or in tighter electrical parameter limits for the test. The electrical parameter specifications in the datasheet are not modified by this method.

Parameter re-characterization is a process of uprating in which the part functionality is assessed and the electrical parameters are characterized over the target application conditions, leading to a possible re-specification of the manufacturer-specified datasheet parameter limits. The parameter re-characterization method of uprating seeks to mimic the part manufacturer's characterization process. Electrical testing is followed by data analysis and margin estimation.

Stress balancing is a process of thermal uprating in which at least one of the part's electrical parameters is kept below its maximum allowable limit to reduce heat generation, thereby allowing operation at a higher ambient temperature than that specified by the semiconductor part manufacturer[32]. The process assesses the possibility that the application may not need to use the full performance capability of the device, and that a power versus operating temperature trade-off for the part may be possible.

Uprating deals with performance over a wider temperature range not reliability, Reliability is the ability of a part to perform within specified performance limits, for a specified period of time, under the life cycle application conditions. Reliability assessment MUST be performed independently of the performance assessment step (where uprating may be carried out), because the recommended operating conditions that are stated in the part datasheet, relate only to the electrical parameter limits. Generally, the manufacturing, qualification and reliability monitoring data are used to help in the reliability assessment[33].

In general, the manufacturer's part qualification process is not based on the part's recommended operating conditions but rather on accelerated reliability testing methods[34]. In other words, part operating temperature ratings are set for performance reasons as opposed to reliability reasons. The limits for reliable operation of parts are designated by the absolute maximum ratings (most often wider than the recommended operating conditions). In fact, there have been several studies where the reliability of parts has been tested beyond their manufacturer-specified recommended operating temperature limits and the reliability demonstrated for the application [32, 35-38]. There have also been studies where the reliability of parts has been tested beyond their absolute maximum ratings and the reliability has been demonstrated for the application [39]. The cause of uprating does not necessarily compromise reliability [40, 41].

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

Nevertheless, the uprating assessment of a part only determines the electrical functional capability of parts in their target application conditions. This determines whether a part "can work" in a given environment. However, to determine if a part "won't fail" in the application environment, the reliability of the part needs to be determined for the application. As temperature often accelerates failure in electronic components, and since the manufacturer has no responsibility to ensure reliability outside the recommended temperature range of operation, it is the responsibility of the part user to establish part reliability over a wider temperature range, before using the device outside the recommended temperature range. The methods of determination of reliability can vary and may include assessment of manufacturers' qualification test results, additional tests performed by the equipment manufacturers and virtual qualification.

Capacitors

One of the most difficult technological barriers to the development of high temperature electronic systems is the creation of compact, thermally stable, high energy density capacitors. Fundamental properties of traditional, perovskite ceramic, dielectric materials dictate that stability of capacitance with respect to temperature and voltage must be sacrificed to achieve large values of the dielectric constant.

	Manufacturer	**Voltage**	**Performance Range**	**Temp Range**
Ceramic	KEMET	100 - 200 Vdc	16 pF - 0.1uF	+ 200 C
		101 - 200 Vdc	1000 pF - 1.0 uF	+ 200 C
		50, 100, 150 Vdc	1.0 pF - 0.12 uF	+125 C
		50, 100, 150 Vdc	100 pF - 6.8 uF	+125 C
	Johanson	50, 100, 200 Vdc	470 pF - 0.075 uF	-55 - 200 C
		50, 100, 200 Vdc	3900 pF - 1 uF	-55 - 200 C
	Syfer	25, 50, 100, 200 Vdc	1 nF - 1.80 uF	-55 - 150 C
	Novacap	25, 50, 100, 250, 500 Vdc	120 pF - 18 uF	-55 - 200 C
		25, 50, 100, 250, 500 Vdc	5600 pF - 15 uF	-55 - 150 C
		25, 50, 100, 250, 500, 1000, 2000, 3000, 4000 Vdc	47 pF - 390 nF	-55 - 200 C
	AVX	16,25,48 V	270 pF to 0.47 uF	-55 to 150 C
	TDK	25, 50, 100 Vdc	150 pF - 4.7 uF	-55 - 150 C
	Murata	50 Vdc	2700 pF - 0.022 uF	-55 - 150 C
		50 Vdc	0.047 uF - 0.33 uF	-55 - 150 C
		16, 50 Vdc	0.22 uF - 2.2 uF	-55 - 150 C
Film	AVX	25 - 250 Vdc	1 nF - 33 nF	-55 - 140 C
	Evox Rifa	50, 100, 250, 400 Vdc	1 nF - 3.3 uF	-55 - 150 C
		50, 100, 250, 400 Vdc	1 nF - 22 uF	-55 - 150 C
		50, 100, 250, 400 Vdc	1 nF - 0.56 uF	-55 - 150 C
		100, 250, 400, 630 Vdc	470 pF - 0.68 uF	-55 - 150 C
	Custom Electronics	100, 200, 400, 600 Vdc	Call for range	< 200 C
		200, 400, 600 Vdc	Call for range	< 200 C

Figure 7 Typical ratings for capacitors for extreme temperature environments.

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

As seen from Figure 7, only a few capacitors are available for the hybrid automotive temperature environment.

Low dielectric constant materials ($\varepsilon_r < 50$), which are used in temperature compensating capacitors, such as C0G or NP0, are highly stable with respect to temperature, have a predictable temperature coefficient of capacitance, and exhibit few adverse effects of aging. However, the volumetric energy density is so low that it takes hundreds of very thin layers to produce even a 1 μF capacitor. Higher dielectric constant titanates which are used to provide higher energy density for general purpose ceramic capacitors, such as X7R, exhibit wide variations in dielectric constant with increases in temperature, including a rapid drop in dielectric constant above 150°C. In fact, the capacitance of X7R at 200°C can easily be less than 60% of the room temperature value. In addition, the leakage currents in these titanate materials become unacceptably high at elevated temperatures, making it more difficult for the capacitor to hold a charge, and the increased dissipation factors can lead to thermal runaway. For the regime 150°C to 300°C, the preferred method is to eliminate as many capacitors as possible from the design, and then to use stacks of highly thermally stable NP0 dielectrics to achieve the desired capacitance. Glass-K capacitors have also shown promise in this temperature range.[42] Much materials research is currently ongoing to push out this power density/temperature stability tradeoff. One example of this is the use of different heating rates and atmospheres in the manufacture of PLZT ceramics to create highly volumetrically-efficient capacitor dielectrics with long-term stability at high operating temperature (T > 200°C) and moderate applied voltage [43]. Another is the development of a new family of relaxor ferroelectric materials based on $BiMeO_3$-PT, where Me^{+3} is a metal ion that can be Sc^{+3}, Yb^{+3}, Y^{+3}, Fe^{+3}, or others. These materials have dielectric constants of more than 10,000 and dissipation factors less than 2% over a wide temperature range with maximum operating temperatures ranging from 300°C to as high as 600°C. These relaxors have been used to create capacitors with volumetric efficiencies greater than 1.4 $\mu F/cm^3$ at 300°C [44]. Capacitors made with these new dielectric materials are now commercially available from TRS Ceramics.

As for capacitors based on metallized polymer films, those polymer dielectrics that are mechanically and electrically stable to the highest temperatures, such as polyimide and teflon, are also the films which have the lowest dielectric constants and are the most difficult to manufacture in very thin layers. For many years, polyester film dielectrics have been the mainstay of the energy storage capacitor industry. However, polyester dielectric capacitors have been viewed as weak candidates for high temperature applications exceeding 150°C because of their relatively low glass transition temperatures, although some previously accepted limitations are likely to be more related to packaging and manufacturing than to the basic properties of the polyester film [45].

For applications at temperatures to 200°C, a number of different dielectrics have been examined, including Nomex 410 and 418 aramid papers; Voltex 450 aramid paper; polybenzimidazole (PBI), a linear thermoplastic supplied by Hoescht Celanese [46-48]; FPE Polyimide [49], Kapton [50], Polyimide (PI), Perfluoroalkoxy (PFA) resin, and Polyparaxylene (PPX) [51]. Of these, the best candidates were the FPE polyimide, which exhibited stable capacitance and dissipation factor up to 225°C for up to 500 hours, and

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

PFA, which combined stable mechanical and thermal properties with a low dielectric loss and a relative permittivity which remained within ± 10% of the room temperature value to 200°C.

Despite these investigations, clearly the outstanding polymer candidate for 200°C capacitors is still PTFE because of its stability with respect to temperature. For 1.0 mF components, aged in an air ambient for 2000 hours (12 weeks) at 200°C, and then brought to room temperature, teflon capacitors exhibited very little change in capacitance at 50 khZ and only a gradual decrease in capacitance at 20 kHz to 98% of the original value. The dissipation factor of the capacitors tested increased slightly and gradually, at 50 Hz, throughout the duration of the testing.[52, 53] Further information can be found in review articles on polymer film capacitors [42, 54].

Other Passives

Inductors are often the largest and heaviest components in power electronic systems [55]. Therefore, efforts to miniaturize inverters for use in hybrid electric automotive applications must necessarily consider improvements in these devices. Furthermore, these applications will require that these components operate at elevated temperatures. Advancements in magnetic materials for power electronics are needed to permit both reduction in the size and weight of inductive components and facilitate their use at elevated temperatures.

The desired technical properties for soft magnetic materials are high permeability, low hysteresis loss, low eddy current loss, large saturation and remnant magnetization, and high Curie temperatures. Permeability describes the magnetic induction, B, produced by a given applied field, H. Hysteresis loss is the energy consumed (and dissipated as heat) in cycling a material between a field of –H and H. Eddy current losses are losses at high frequencies related to the material's electrical resistivity. Saturation induction, B_s, is important to provide a large induction in a small size device. Curie temperature is the temperature at which magnetic ordering in the material is lost. Some material properties for common soft magnetic materials [56] are given in Table 1 below.

Table 1: Properties of Some Common Soft Magnetic Materials[56]

	Permeability	**Saturation Induction**	**Curie temperature**
Bulk Materials			
Silicon steel	10^4	1.6-1.8 T	750°C
Supermalloy	10^6	0.6-0.8 T	400°C
Hiperco	10^3	2.0-2.45 T	930°C
Ferrites			
Mn-Zn	10^4	0.3-0.5 T	100°C-250°C
Ni-Zn	10^3	0.1-0.36 T	100°C-500°C

Bulk ferromagnetic materials for power transformers are typically silicon steels that are processed into thin sheets and laminated. These are limited to low frequency (60 Hz) and

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

moderate frequency applications. Amorphous metal magnets can possess much higher permeabilities and resistivities, which provides advantages in frequency response. However, synthesis of these alloys requires stabilization of the glassy phase through the addition of a significant fraction of non-magnetic glass forming species. This reduces the saturation induction and Curie temperatures of these materials. Furthermore, the alloys have relatively low crystallization temperatures. This makes them unstable for use at elevated temperatures, especially above 300°C. High resistivity ferrites are also limited in their operation at elevated temperatures, as many interesting high frequency ferrite materials have Curie temperatures below 300°C. A promising new option for high temperature power applications are nanocrystalline and bulk amorphous magnetic materials [57]. Such materials have been shown to have excellent properties at high frequencies (10-100 kHz range and higher). These materials possess saturation induction values of 1.6 – 2.1 T, which are three to five times those of ferrites and twice those of amorphous magnets, allowing for proportional reduction in component size. Furthermore, nanocrystalline soft magnetic alloys have been developed over the past decade with high permeabilities, high Curie temperatures, and without the magnetic hardening associated with the crystallization of amorphous alloys. This limits the core losses. Core losses can reduce efficiency and increase the temperature of surrounding components leading to failure well below the Curie temperature [58]**.** Fe-based nanocrystalline alloys, such as FINEMET and NANOPERM, however, suffer problems at elevated temperatures associated with the decoupling of the exchange interactions between nanocrystals. A new Fe-Co based nanocrystalline alloy, HITPERM has been shown to retain excellent magnetic exchange coupling and other properties at temperatures as high as 500°C – 600°C, making it an excellent candidate for use in high temperature electronic applications [59-61]**.**

Resistors have been shown not to be a major concern, as most thick film surface mount chip resistors and thick film paste resistors, such as the Heraeus-Cermalloy 900 Series, perform reliably after many hours at 300°C and above [62]. These resistors are made of a fired RuO_2 paste on an Al_2O_3 insulating ceramic base with a silver inner electrode and a nickel outer electrode. They have good temperature stability in the range 300°C to 500°C with a thermal coefficient of resistance of ± 200 ppm, owing to their manufacture at temperatures of 500°C-1000°C. They exhibit a resistance drift of only a few percent after 2000 hours at 300°C – 400°C. The ultimate limit to their use is softening of the glass frit at temperatures above 500°C [62]. Thin film surface mount chip resistors consist of a vacuum deposited film of TaN or Ni-Cr on an Al_2O_3 base. High temperature versions, using the Ni-Cr film, are less thermally stable than thick film resistors, and have a maximum operating temperature of 200°C to 300°C [62].

Wirewound discrete resistors, such as the power resistors made by Dale, are made of a resistive wire (NiCr, CuMn, FeCr) wound around a ceramic bobbin with Au plated Ni axial leads and end caps. These high precision resistors are stable under powered/unpowered aging to 300°C and some commercial version are capable of 500°C operation. This is not true of film or carbon composition resistors, which are not recommended for use at elevated temperatures [62].

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

PC Boards

Traditionally, the push to use ceramic substrates for high temperature electronics has resulted from concerns related to the use of standard FR4 organic board material at temperatures above 135°C, its glass transition temperature (T_g). Printed wiring boards (PWB) and substrates must provide mechanical support for components, thermal dissipation, and electrical interconnection. Above T_g, organic boards begin to lose mechanical strength due to resin softening, and exhibit large discontinuous changes in their out-of-plane coefficient of thermal expansion, which can cause in-board delaminations and loss of adhesion to the copper traces. In addition, organic boards exhibit significant decreases in their insulation resistance above T_g.

Advances in materials technology, however, have produced a number of organic laminates with T_g in excess of 135°C, including bismaleimide triazine (BT), and high temperature, tetrafunctional FR4 materials, which operate to 180°C. Boards based on cyanate ester or polyimides can be used at temperatures as high as 260°C. The glass transition temperatures and key electrical and mechanical properties of many of these new materials are provided in Table 2 shown below:

Table 2 Properties of organic printed wiring board materials [63, 64]

Material	Supplier	Tg (°C)	Dielectric Constant	CTE-Z ppm°C	CTE-X ppm°C	CTE-Y ppm°C	Approximate Cost Adder over Fr4	Dissipation Factor @ 1 MHz
FR4 Tetrafunctional	Polyclad Nelco N4000-2	135 142	4.5	60	15	15	Tetrafunctional 1 (baseline)	.019
FR4 Tetra II #370	Polyclad Nelco N4000-6	175	4.4	60	15	15	1.2x	.012
FR4 Tetra II Plus #370-G	Polyclad	180	3.9	45	14	14	1.3x	.010
Getek	G.E	180	3.9	50	13	13	1.4x	.013
B-T	Norplex/Oak Nelco N5000	180	4.1	50	13	13	1.5x	.015
Thermount	Nelco N7000-2T	220	4.1	85	8.5	8.5	3.5x	.022
Polyimide Blend	Nelco N7000-2	225	4.3	70	13	13	2.5x	.014
Cyanate Ester E-Glass	Nelco N8000	250	3.8	55	12	12	2x	.009
Cyanate Ester S-Glass	Nelco N8000S	250	3.6	50	9	9	6x	.009
Polyimide 85NT	Arlon	250	3.9	100	6-9	6-9		.015
Polyimide E-Glass	Nelco N7000-1	260	4.3	70	13	13	3x	.013

E-glass/ PTFE laminates have a T_g greater than 300°C, but are not recommended for use above 120°C because of weakening adhesion of the copper layer, although advances in this technology are continuing.[63, 64]

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

Problems with these polymer based board materials [65] include the following:

1) The resins that have high glass transition temperatures, such as CE, PI, and BT, also have high cost.
2) While PTFE is used for digital and microwave applications requiring low dielectric constant and dissipation factor, Cu-clad PTFE is thick and heavy, with poor thermal dimensional stability, and a CTE as high as Cu in plane and even higher out-of-plane.
3) The CTE mismatch between silicon and the board material cannot be tolerated by flip chip interconnections.
4) Use of underfills and silicone elastomers to mitigate CTE mismatch is not possible for high temperature applications as these materials are not fit for high temperature use and cannot withstand large numbers of wide temperature cycles. Three underfill materials have been identified for use to 150°C. These materials have more crosslinking leading to a higher glass transition temperature, higher CTE, lower modulus, and better adhesion. However, none have been proposed for 175°C. [66]

A new polymer-based film, PIBO, has been proposed to address these issues. PIBO is a high temperature stable polyimide film with resistance to plasma degradation. The film has high strength and stiffness, low dielectric constant and dissipation factor, and excellent thermal properties. It has a CTE of 3 ppm/K and it does not exhibit a glass transition temperature, Tg, or a melting point, Tm, up to 600°C. Direct bonding of copper as opposed to adhesive bonding is possible using plasma followed by sputtering and subsequent electroplating. This film has demonstrated a life of more than 2000 thermal cycles making this material promising for automotive applications that require shock and vibration combined with temperature cycling. [65]

The critical failure mechanisms which limit the use of PC boards at high temperatures are delamination of the copper from the laminate and delamination within the laminate, conductive filament formation, and PTH fatigue and separation. These are discussed in further detail below.

Delamination

Delamination is defined as a separation between the layers of the printed circuit board (PCB), such as between the FR4 and the copper foil, or between the epoxy resin and the glass fiber.[67] The latter form of separation can lead to a reduction in insulation properties by entrapping processing solutions and can provide a path for conductive filament formation. Delamination is a particular issue in high temperature applications, both because of the use temperatures and also because of the temperatures needed for assembly with high temperature solder materials, where the reflow temperature is well above that for standard tin-lead solder.

Delamination occurs when environmental stresses resulting from temperature changes, mechanical bending, and/or moisture, exceed the interfacial strength. Delamination is especially prevalent when the Tg of the polymer resin is exceeded, because of its large,

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

discontinuous increase in CTE above Tg. This results in a high CTE mismatch between the resin and the glass or between the resin and the copper. Delamination stresses are thus increased over those for the same change in temperature in a material that is still below its Tg. This makes the use of high Tg materials like polyimide preferable for high temperature applications. The maximum acceptable temperature for polyimide is about 260°C, while that for G-10 and FR-4 is only about 135°C. The electrical characteristics of polyimide are similar to epoxy, but polyimide has improved chemical resistance. The disadvantages of polyimide are its high price, poor peel strength (half of copper-clad epoxy at room temperature), higher cure temperature (220°C versus 175°C for epoxy), and longer post-cure time.

Figure 8 Delamination of copper above Tg, Cyanate Ester at 250°C.

An additional factor that should be considered for printed circuit boards for automotive use is the fact that at higher temperatures the absolute volume expansion and contraction of the epoxy-resin outside the bundles is much greater than that inside the bundles, increasing the thermal stresses during thermal cycling at the glass-fiber bundle edges. Once the stresses exceed the bonding stress, delamination can occur. In terms of resistance to severe thermal excursion, cyanate ester boards provide greater performance than the widely used FR-4 [68].

Conductive Filament Formation

CFF is an electrochemical process that involves the transport (usually ionically) of a metal through or across a non-metallic medium under the influence of an applied electric field [69-71]. CFF is a potential reliability problem, in that it can cause current leakage, dielectric breakdown and electrical shorts between conductors. The biased conductors act as electrodes providing a driving potential while ingressed moisture between the organic resin and the fiber reinforcement will serve as an electrolyte (see Figure 9). As metallic ions migrate and form a bridge between two biased conductors, the loss of insulation resistance results in a current surge. The current surge will eventually result in a short and a large increase in localized temperature. This increase in localized temperature can manifest itself as a burnt or charred area between the two conductors.

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

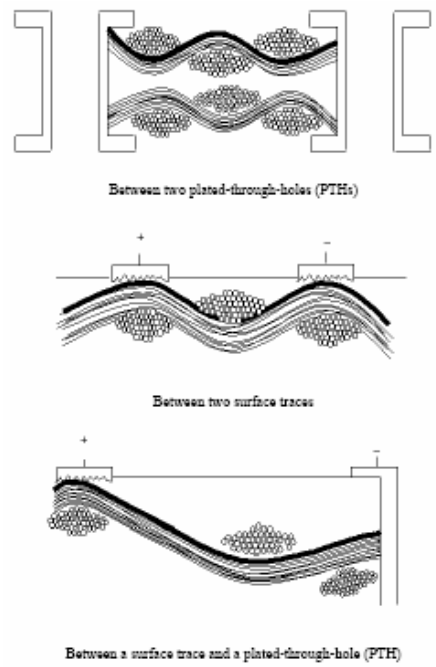


Figure 9 Conductive filament formation (CFF) configurations[72].

The prime factors influencing CFF are board features (resin materials, conformal coatings, and conductor architecture) and operating conditions (voltage, temperature, and relative humidity). The accelerating effects of temperature and relative humidity make this mechanism of specific concern in automotive applications. Furthermore, path formation, necessary for the occurrence of CFF, will occur due to interfacial delamination of the interface between the individual fibers and the organic resin matrix. This degradation is often due to thermal cycling (see Figure 10) and is exacerbated by use of the board over its Tg as discussed in the previous section on delamination. Previous studies have gathered data on the quantitative effect of these various elements [73-75].

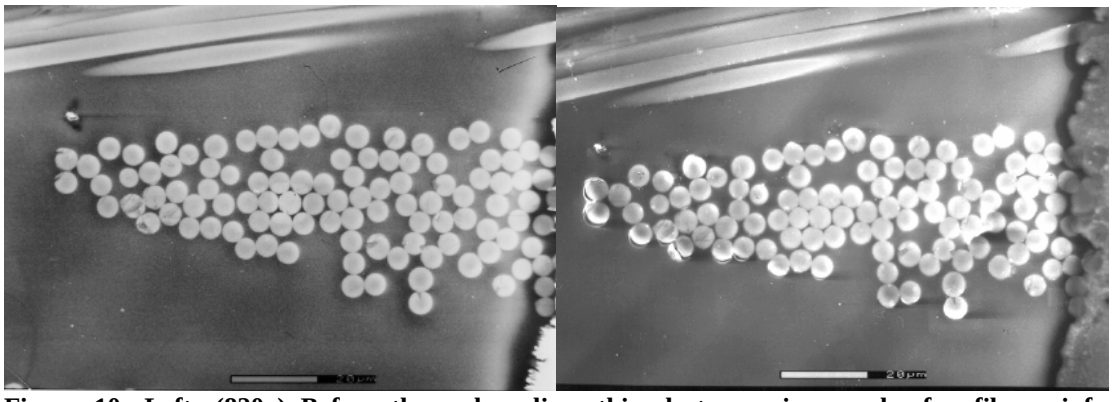


Figure 10: Left: (820x) Before thermal cycling, this electron micrograph of a fiber-reinforced laminate shows good interfacial bonding at the fiber/epoxy resin interface prior to thermal cycling. Right: (820x) After thermal cycling, several instances of interfacial degradation (debonding) can be seen to have occurred at the fiber/epoxy resin interface[72].

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

Based upon this empirical evidence, models have been presented that predict the operational lifetime assuming an eventual failure mechanism of CFF [75, 76].

Experiments have shown that CFF can also occur in the presence of hollow fibers [77, 78]. The environmental considerations are the same, however in this case the path formation occurs within the fiber itself, instead of along the fiber/matrix interface. The scenario of electromigration within the fiber and its effect on time-to-failure has also been modeled [79].

Plated Through Hole (PTH) issues

Plated through hole (PTH) misregistration can lead to cracking between adjacent PTH's. This crack can serve as a path for CFF (Figure 11). The time for CFF is also accelerated because the distance between two PTH's or a PTH and a transmission line is shortened through misregistration.

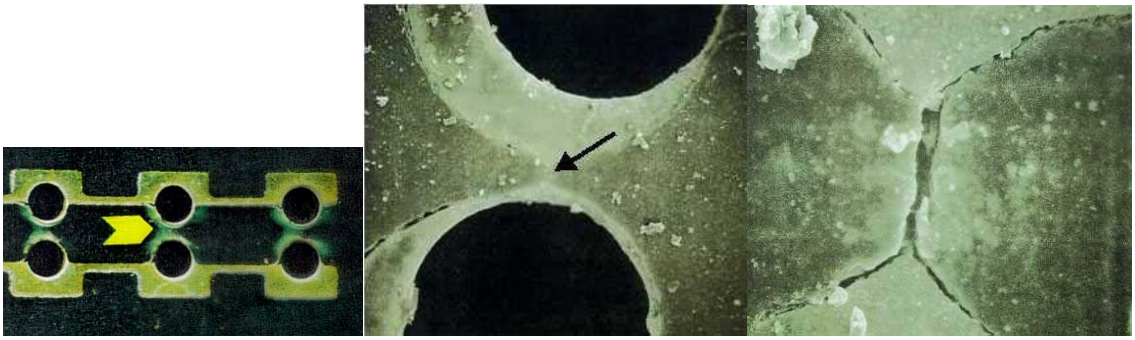


Figure 11 Spacing of the PTHs not propper and a crack developed a path between PTHs [67].

Besides being a contributing factor to the development of conductive filament formation through hole technology presents a number of other elevated temperature use concerns over surface mount technology.

PTHs are normally created by a drilling process. Any burrs or resin smear covering inner layer interconnects are removed. Deburring slightly roughens the hole and allows for subsequent plating. The hole is then coated by electroless copper deposition. The thickness of the electroless layer is typically 80 to 100 millionths of an inch. The barrel of the hole is then electroplated with copper to a thickness of one mil.[80]

For automotive environments, PTHs may see the following failure mechanisms:

- Fatigue Crack in PTH Wall
- PTH Wall Pad Separation

A fatigue crack in the PTH Wall is a crack that propagates around the circumference of the PTH or Via due to cyclic stresses that exceed the fatigue strength of the copper wall [67]. PTH fatigue cracks usually occur in the field and can be a cause of infant mortality. They are generally a result of poor design, a non-optimized manufacturing process, defective material or customer misuse. Poor design can be difficult to discern and may require stress analysis or accelerated testing (such as interconnect stress testing (IST)),

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

especially if the product is leading-edge technology. Besides fatigue fracture occuring from CTE mismatch between the PC board and the PTH, this failure can also occur at elevated temperatures due to PTH wall recession. The PTH wall recession is when resin has backed away from the hole wall. As the temperature rises, the material becomes more flexible and this failure becomes more likely. Above Tg, the resin material becomes very soft.

PTH Wall-Pad Separation is separation of the inner layer pads/lands from the PTH due to stresses that exceed the adhesion strength. A picture of wall separation, also known as breakout of internal lands, can be seen in Figure 12

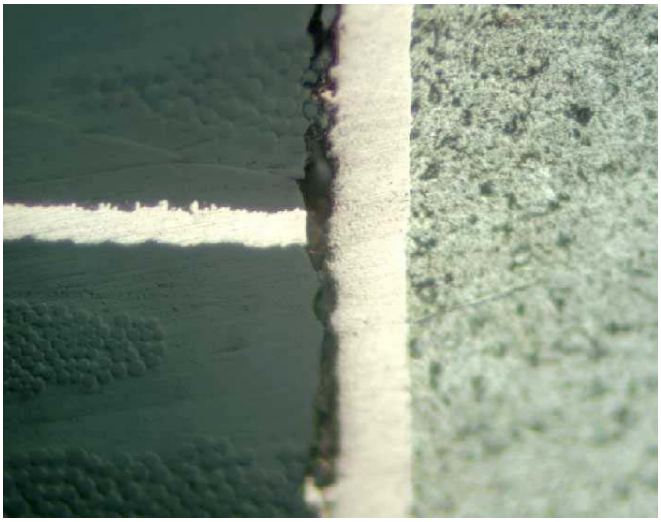


Figure 12 Example of PTH wall separation [67].

PTH Wall separation usually occurs during printed board manufacturing and assembly, which indicates an overstress mechanism. Separation can also occur during the field, but this is often an indication of a separation that occurred during manufacturing or assembly that was not detected, or did not fully propagate, until operation. The wide temperature ranges seen in automotive applications can serve to propagate the separation, especially if the Tg is exceeded. Note that wall separation is not resin pullback.

Surface mount versus through hole technology

Assembly processes are classified based on attachment configuration as follows: through-hole assembly, surface-mount assembly, and mixed through-hole and surface-mount assembly. Through-hole assembly involves inserting component leads into plated through-holes (PTH) in the board and soldering them. [81]. In surface-mount assembly, the component leads are soldered to the surface of the printed wiring board. The solder joint, now the sole mechanical and electrical connection between the printed wiring board and the component, bears a significant amount of the stress from any vibrational or thermomechanical loads on the board. [81].

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

The main difference between these two technologies for use at elevated temperatures is in the dominant failure mechanism. In the surface mount technology, the main concern is the delamination of the copper pads and layers from the resin, while in the through-hole technology it is the fracture of the PTHs. In addition, high temperature operation is more of a concern for surface mount assemblies than for through-hole assemblies, because of the greater strains on the solder joints in surface mount technology which makes SMT assembly reliability more sensitive to wide temperature swings than through-hole assembly reliability.

Limitations in number of layers

PC boards can be manufactured in single sided, double sided, or multilayer form factors, which can contain up to 24 different layers. Typically the need for a multilayer board comes from complex signal routing in computing or RF applications. Typical PC boards used in power applications have 2 to 4 layers, where 2 are used for signal currents and 2 are used for power currents. Since the currents carried by the copper layers in the board are significant, self heating of the conductor layers is an issue and is typically addressed by adding more area to the board or using thicker copper layers.

There is no established rule of thumb for the number of layers allowed at any temperature. However, it stands to reason that strain in the resin and between the resin and the copper layers due to CTE mismatch and the subsequent susceptibility to delamination will increase slightly with increasing numbers of thicker copper layers. Therefore, at higher temperatures, especially above Tg, and wider temperature swings, it is may be necessary to use a smaller number of thinner copper layers to minimize strain. This may require a trade-off, however, in power boards where the increased temperature makes it more important to have thicker copper layers to limit the power dissipation and subsequent additional heating. In addition, it may be necessary to limit the overall thickness of the board, as well, to minimize the axial strains on PTHs and vias, caused by CTE mismatch that can result in PTH or via plating fracture.

Packaging types

The power electronics that are used in the inverters of a hybrid electric vehicle consist of power switching devices, diodes, capacitors, resistors, and inductors, all of which have been discussed above. However, there is another critical factor in reliable operation of these electronic systems at elevated temperatures and that is the associated packaging.

Typical inverter modules are three-phase pulse width modulated (PWM) devices each with six arms. Each arm consists of one power switch and its associated free-wheeling diode. The typical power switch is an insulated gate bipolar transistor (IGBT), although power MOSFETs or thyristors can be used instead. The power switches and diodes are attached to direct-bonded copper (DBC) aluminum oxide (or nitride) substrates using a

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

lead-based or lead-free solder. The substrates are, in turn, attached to a copper heat spreader using the same metallic solder. The IGBTs and diodes are then interconnected by one of several different technologies. [82] The most common of these different technologies for packaging and interconnection of the devices are provided below.

Chip and Wire Package

Chip and wire packages use multiple thick wires to interconnect the top surfaces of the die to each other, to the DBC substrate, and/or to I/O pins on the side of the module. For current chip and wire technology, gold or aluminum wires are used as interconnections. An example of a wire-bonded module can be seen below. These modules are widely available from all major power electronic device manufacturers including Semikron, ABB, Toshiba, Siemens, and others.

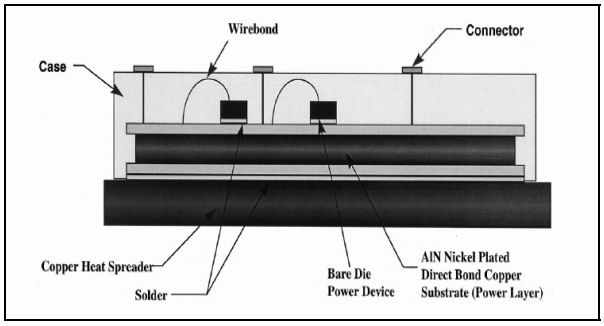


Figure 13 Chip and Wire module.[83]

While this process utilizes well-known technology and a simple, low-cost fabrication process, it has several disadvantages. First, it is prone to noise, oscillations, and fatigue caused by large currents passing through the wires. Also, large electromagnetic fields are generated as currents pass through adjacent wires, thus creating uneven current distributions among the wires. Another disadvantage of wire-bonds is that all cooling must occur through the bottom of the die, which greatly restricts heat dissipation from the module [84]. This, combined with the localization of current flowing into the top of the device, creates hot spots on the top surface of the die at each wirebond. These hot spots are also areas of high temporal thermal gradients when power is rapidly switched on and off. Lastly, wire-bonded modules have a low power density and a low silicon-to-footprint ratio due to their packaging structure[85].

Several reliability studies of wire-bonded power modules have shown that the wire-bond is the dominant failure site. This is due both to wire flexure fatigue resulting from the wide ambient temperature swings in automotive environments and to wire liftoff resulting from the creation of these hot spots and high thermal gradients at the wirebond-to-die interface at the top of the device. Additionally, the large solder area of the bond can fatigue and delaminate under thermal cycling [84] resulting in poor heat transfer over large areas of the attach under the die. This increases the temperature of the hot spots above these areas, accelerating wire liftoff failure. These two packaging technologies, wirebonding and die attach, critical to reliable operation of chip and wire modules are

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

discussed in detail below. Despite these reliability weaknesses, wire-bonds are still the most common interconnection technique in today's microelectronics packaging.

Wirebond

Wires and wirebonds are subject to failures in high temperature electronic systems as a result of the wide temperature excursions. The thermal expansion mismatch between the chip and the substrate in unencapsulated cavity packages, and between the chip, the substrate and the encapsulant in silicone filled power modules or in small signal plastic encapsulated microcircuits, generates a significant thermo-mechanical stress in the internal interconnection wires joining these elements, particularly when thermal cycles from -55°C to 200°C are encountered. The failures seen from thermo-mechanical stresses are wire flexure fatigue caused by the thermal mismatch between the wire and the substrate in encapsulated and unencapsulated modules, along with shear of the bond pad (wire liftoff) due to the thermal mismatch between the bond pad and the underlying substrate, and finally failure due to axial tension of the wire caused by the thermal mismatch between the wire and the encapsulant in which it is enclosed.[86] The highest concentration of expansion stresses is at the wire terminations, where the wire is immobile and unable to flex to accommodate the strain. Typical failure sites for flexural fatigue are the neck of a ball bond, and the heel of a wedge or stitch bond. The failure site for wire lift-off is the bond interface between the wire and the bond pad; and the failure site for axial fatigue is in the middle of the wire length. The location of the failure is dependent on the relative strength of the wire and the wirebond, and new models for this failure mechanism are being developed [87].

Further research in the area of fatigue of aluminum wirebonds would be very advantageous for improving power electronic module reliability. As power devices switch to copper metallization, research into copper wire-copper bondpad liftoff is also needed.

High temperature applications can also weaken both the wire and the wirebond by annealing of the wire and intermetallic reaction at the bond site, respectively. Annealing is the removal of damage and defects induced in the wire during the low temperature portion of the thermal cycle by recrystallization and grain growth during the high temperature portion of the thermal cycle. The larger grains reduce the strength and fatigue resistance of the wire. This effect is particularly pronounced in the neck of gold ball bonds. The second effect, intermetallic reaction, takes place in the following manner. Two dissimilar metals placed in contact diffuse into each other at different rates, leaving behind a supersaturation of vacancies on the side of the fast diffusing metal. These vacancies coalesce into voids, known as Kirkendahl voids, which act as stress concentrators, reducing the fatigue resistance of the wirebond. The two metals may also react with one another forming one or more intermetallic phases. These phases typically have complex crystal structures, and thus are usually brittle and more susceptible to

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

fatigue flexure damage than the pure metals. When the component is then exposed to differential thermal expansion stresses, fracture often initiates at the voids and propagates through brittle intermetallic layers, causing failure at the bond site [88].

Wirebond degradation resulting from intermetallic reaction is often seen in the Au wire and Al bond pad wirebonding system typically used in commercial integrated circuits. The intermetallic formation process is governed by the diffusion of gold into aluminum, with Au_5Al_2 forming first followed by $AuAl_2$. The higher diffusivity of gold leads to voiding on the gold side of the interface. Below 175°C, intermetallic growth in the gold-aluminum system is not primarily dependent on steady-state temperature, but rather on the defect density [89], with poorly welded joints failing by interdiffusion and intermetallic formation at times and temperatures significantly less than those predicted from lattice diffusion alone. In fact, intermetallics have been observed to form at temperatures as low as 75°C in joints having many grain boundaries, vacancies, and dislocations. However, in well bonded systems, an intermetallic-related decrease in bond strength is not observed in use at temperatures less than 125°C [90, 91]. Intermetallics are not a concern in chip and wire power modules as the bonding on the die is almost exclusively mono-metallic (i.e. Al wires to Al bond pads). There can be a concern between the Al wires and the Au plating on the DBC or the copper on the DBC. However, the use of nickel plated DBC will eliminate this concern, as Al wires on Ni plated DBC have not been seen to exhibit intermetallic formation at 1000 hours at temperatures up to 350°C [92].

Chip and Substrate Attachment

Chip and substrate attachment refers to the use of conductive and non-conductive adhesives to attach the silicon chip to the underlying substrate, and the use of similar adhesives to attach the substrate to the underlying heat spreader. Die attach in power modules has three main functions. First and foremost, it has the mechanical function of holding the chip in place and affixing it to the substrate. Next, it has the thermal function of providing sufficient heat transfer from the chip to the package to permit the device to operate at high power without exceeding its maximum operating temperature. Finally, it has the electrical function of providing an electrical contact between the chip backside and the wiring on the substrate. This electrical function is specific to power devices and is a result of the fact that the backside of the die is typically electrically active. This is different from planar small signal devices where all the interconnections are made from the top surface of the die. As a result of this electrical function, die attaches for power devices must be highly electrically conductive. As such, power die attaches are typically made of metal alloys as opposed to the filled polymers which are typically used to attach small signal devices.

The most critical reliability concern for die attach is fatigue cracking and delamination leading to die debonding. Die debonding is the dominant failure mechanism for chip and wire modules subjected to passive thermal cycling, such as would be the case for changes in the ambient temperature under the hood of an automobile. While eventually, die debonding will progress to the point where the die becomes detached from the substrate,

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

failure of the device will most likely occur much earlier. Failure typically results from the increase in thermal impedance that comes in the initial stages of die debonding. Low thermal impedance is critical to keeping chip temperatures in the range of reliable operation. Die debonding reduces the heat transfer, leading to overheating of the die which results in both parametric and functional device failure. Die debonding can be caused either by fatigue crack growth in the bulk die attach, or by deadhesion of the solder at the interface. Deadhesion is due to manufacturing defects such as poor wetting of the solder to the interface metallurgy, voiding in the solder, or the presence of dross in the solder. As such, it is to be controlled through the proper choice of soldering materials and proper manufacturing parameters.

Fatigue cracking, on the other hand, will occur whenever the solder is subjected to a thermo-mechanical stress/strain field resulting from expansion mismatch between the die and the underlying substrate during temperature cycling. The most obvious source of these stresses and strains is the global coefficient of thermal expansion mismatch between the components and the substrate in addition to a more local CTE mismatch between the component and solder, and the solder and substrate.

The high power requirements of power devices combined with the need for high electrical and thermal conductivity has led to the widespread use of tin-lead based solders as die attach materials. Examples of typical die attaches are Pb10Sn, Pb5Sn, Pb5Sn2.5Ag, Pb2Sn2.5Ag, and Sn37Pb. These solders are often grouped by melting point, with the low melting point solders being preferred for applications where the operating temperatures are relatively low and the chips are large (less than 1 cm x 1 cm) as would be the case for silicon power devices, while the high melting point solders are preferred for applications where the operating temperatures are high and the chips are small (less than 1 cm x 1 cm) as would be the case for SiC devices. In addition to these lead-based solders, one lead-free solder has been widely used, Sn25Ag10Sb, also known as J-alloy. This lead-free die attach, while used in some plastic packaged components, has a number of drawbacks, including a high price and poor manufacturability. Other lead-free solders, such as Sn3.5Ag, have been used in moderate temperature applications, $-20°C < T_{amb} < 100°C$, but have some reliability concerns related to the size and distribution of Ag_3Sn intermetallic particles. These intermetallics can strengthen the die attach when they are small and well distributed, but act as crack initiation sites when large and concentrated. The natural tendency is for the intermetallics to coarsen with time at temperature. This tendency toward intermetallic coarsening, combined with a relatively low melting point of 217°C and poor reliability under thermal cycling at Tmax > 125°C, makes this solder ill-suited for high temperature applications. This is also true for many of the ternary and quaternary versions of this solder, which add small amounts of Cu, Ni, Sb, and Bi to improve reliability.[93],[94] Sn-0.7Cu is another copper containing tin-based solder that exhibits a similar microstructure and similar properties to Sn-3.5Ag. However, in addition to high temperature fatigue concerns, the high tin content makes this solder prone to whisker growth.

Gold-based eutectic alloys (i.e. Au12Ge, Au3Si, and Au20Sn) are an option for high temperature soldering, because of their excellent creep and corrosion resistance together

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

with high strength. However, these alloys are very expensive and hard to process. In addition, their hardness and brittleness causes them to transmit rather than absorb a great deal of the thermomechanical stress of the joint [95].

Another approach which is now commercially available in a number of inverter modules, including ones from Semikron, is attachment by means of high temperature sintering of noble metal powders. This technology provides the ability to create attachments at low temperatures (< 300°C) that are reliable to very high temperatures (>900°C). In particular, silver powder is preferred because of its high electrical and thermal conductivity, its high melting point (960°C), its high fatigue resistance, and its low cost relative to gold.

The approach most widely used at present is based on the work of Schwartzbauer [96] who originally proposed the low temperature sintering of small (sub-micron) silver flakes that are dispensed as a paste onto the substrate surface. With this approach, joints are made at 220°C – 250°C, a temperature well below the melting point of silver, at pressures of about 40 MPa in one minute in air [96]. It is believed that applying external pressure assists the densification process by eliminating some fraction of pores through compression/deformation, thus increasing the contact area between the silver particles [97]. In this strategy, a hot press is used to apply a quasi-hydrostatic external pressure on the device assembly. Commercial silver paste with a particle size in the range of 1-3 μm can also be used [97]. The finished joint typically has a porosity of 80-85%, a thermal conductivity of about 250 W/mK, and electrical conductivity of 40 MS/m. The thermal and electrical conductivity are consistent with pure silver of similar porosity [98], and are significantly better than those of eutectic SnPb die attach. The adhesion strength of the sintered silver joint was also found to be higher than that of the eutectically soldered joint [97]. Furthermore, the uniform microporous silver microstructure provided additional compliance which acted to relieve the thermo-mechanical stresses due to CTE mismatch, thus improving the joint reliability under thermal or power cycling. Joints made in this way have shown a twenty times improvement in power cycling reliability at $\Delta T_j = 130°C$ over that of eutectic solder joints in standard modules, as determined from an extrapolation of the reliablilty model [98].

The application of external pressure has a drawback because it makes automation in manufacturing very difficult to implement and thus increases the cost [99]. Furthermore, applying pressure may cause device cracking [99]. Alternative methods are therefore being researched to lower the needed pressure by using either Ag and Au nanopowders [100]. The reduction in the size of the powders to the nanoscale increases the surface energy of the particles, which then increases the driving force for agglomeration, reducing the pressure needed for the sintering operation [101]. Nevertheless, it appears that a pressure of around 4 MPa and a temperature of 250°C-300°C is still necessary for bonding. Furthermore, the high levels of liquid binder needed in the colloidal suspensions used to deliver the powder are difficult to bake out from under large die, resulting in high levels of voiding. In addition, these high binder levels result in microcracking of the attach due to shrinkage upon drying and firing. Other limitations of

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

this technique include the fact that silver powder bonds poorly to nickel or copper. This means that DBC substrates must be silver or gold plated for good adhesion. However, the silver or gold plating will create intermetallic formation problems with Al wires bonded to the substrate. Therefore, selective plating of the substrate is required – a costly and difficult process. Another concern with this technology is the tendency for silver to migrate under bias, and the high cost and stiffness of gold attach.

Use of solder in the liquid state has also been proposed. In particular, the Nb-In-Sn system has been considered for the development of liquid solder joints at 192°C. However, it may take up to one month to get sufficient intermetallic to form a good solder joint. Also the reliability of containing a liquid solder interconnection is questionable at best.[102] Similarly, liquid phase transient bonding has been proposed, but the length of time needed for sufficient solid-state diffusion to occur to form a bond is often greater than desired from a manufacturing standpoint [103]. Nevertheless, this approach does hold promise.

Further research on the reliability of sintered silver nanopowders and other high temperature solder techniques is needed.

Substrate

Ceramics are the traditional substrates for use above 125°C. There are three ceramic materials which have traditionally been used for substrates in this approach, the properties of which are given in Table 3 shown below:

Table 3 Properties of ceramic substrate materials[104]

Material	Thermal Conductivity (W/mK)	Thermal Expansion (ppm/K)	Dielectric Constant @1MHz	Loss Tangent @ 1 MHz
AIN	170	4.6	8.6	0.0005
Al_2O_3 (96%)	25	7.4	9.0	0.0001
BeO	260	8	6.5	<0.0004

Aluminum oxide (Al_2O_3) is the preferred selection for low cost applications. The disadvantage of Al_2O_3 is its poor thermal conductivity, which makes it acceptable for systems which operate in high ambient temperatures, but not acceptable for systems where a significant fraction of the heat is generated by the die and must be dissipated through the substrate, such as power conditioning systems. For high temperature, high value, power electronics, AlN is the preferred choice [104-107] because of its close thermal expansion match to both Si and SiC, and its high thermal conductivity, as shown in Figure 14 and Figure 15. In recent years, the improved metallization and lower cost of AlN has driven BeO, with its toxicity concerns, from the market.

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

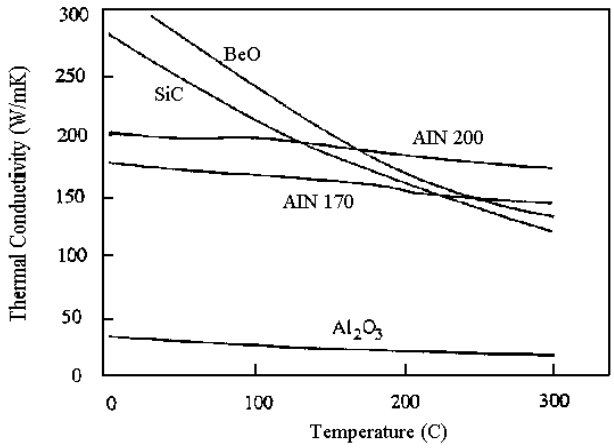


Figure 14 ***Thermal conductivity of ceramic substrate materials [107]***

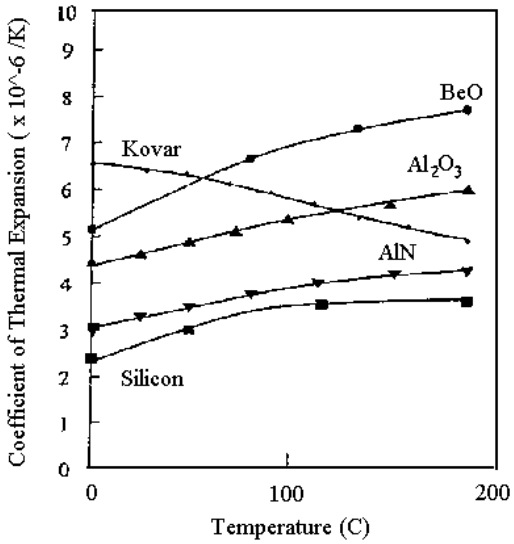


Figure 15 ***Thermal coefficients of expansion (CTE) of ceramic substrate materials [105]***

These substrate ceramics can be processed in a number of different ways. Low Temperature Cofiring (LTCC) is useful for small signal substrates that have a maximum use temperature of 300°C. Above this temperature, the noble metals used for metallization begin to degrade and delaminate and it is necessary to switch to High Temperature Cofiring, which uses more thermally stable, but lower conductivity, refractory metals. High Temperature Cofired Ceramics (HTCC) can be used up to 500°C.

Power substrates are typically manufactured using direct bonded copper (DBC) techniques. Direct bonding of copper is done by creating a ceramic eutectic joint between copper oxide and aluminum oxide at the copper interface to either aluminum

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

oxide or oxidized aluminum nitride. This approach is used in order to bond a layer of copper on the ceramic that is thick enough to handle the large currents in power applications. The bond is extremely strong and will not delaminate. The failure mechanism in wide temperature range cycling is brittle fracture of the ceramic under the copper due to localized CTE mismatch.

In addition to being considered as a possible high temperature power semiconductor material, SiC is also being investigated as a possible high temperature insulating board or substrate material. This is because co-fired ceramic boards are expensive, have poor thermal conductivity, and are easily cracked under shock loading. All these problems can be solved, if metal traces and alternating layers of ceramic are bonded to silicon carbide without co-firing or the use of glues. SiC is a good heat conductor, is very strong, and can be used in layers along with conductive vias. In work at the Idaho National Engineering and Environmental Laboratory, conductive traces were mechanically bonded by plasma spray or electroplating onto SiC with sufficient bond strength to remain functional at 350°C. There was no deterioration of current capability in these traces with temperature cycling. These traces can be used to propagate signal or power, act as temperature indicators, or act as component attach. Three passes of the spray gun leave a Ni – 5% Al trace that is 1.5 mils thick over a 0.8 mil thick plasma sprayed alumina insulating layer.[108]

Another substrate that is being explored for power modules is silicon nitride, Si_3N_4. Its advantage is a fracture toughness which at 5 MPa-$m^{1/2}$ is twice as high as Al_2O_3 or AlN. This leads to the ability to survive more and wider temperature cycles. However, silicon nitride cannot be metallized using DBC techniques and must have the metal applied using active metal brazing. This results in an inferior adhesion that causes early failure due to delamination. In addition, silicon nitride substrates are currently in very short supply.

Further research into silicon nitride substrates and their metallization is in order.

Double Sided Attach Module

The double sided attach approach is a three-dimensional packaging technique that provides high electrical and thermal conductivity. In this approach, each semiconductor device is sandwiched between a metallized ceramic lid above the die and a metallized ceramic substrate below the die. The device is attached to the lid and substrate by reflowed solder or other similar attach material. A simple manufacturing process is followed, making only three connections (source, gate, and drain)[109].

The ThinPak™ is an example of a double-sided attach module. In this package, the lid is soldered directly to the top surface of the chip with a high lead (Pb10Sn) solder. A pattern of metallized holes in the lid permits the solder to flow through, providing electrical conductivity through the lid. The top side of the lid is bonded with eutectic solder (Sn37Pb) to a copper strap that forms the anode terminal. In later versions, the copper straps are eliminated and connection to the source and gate is made integral to the

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

lid, which is now a piece of DBC alumina, and connection to the drain is made integral to the DBC substrate. An optical micrograph image of a direct solder package is shown below. Power modules using this technology are available from SPCO, while encapsulated single chip packages using this technology are available from International Rectifier, Vishay, and others.

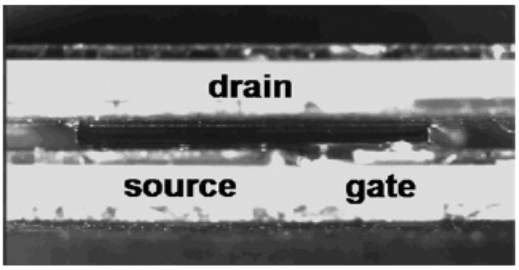


Figure 16 Direct solder interconnect [109]

The main advantage of this approach is the ability to cool the device from both sides, leading to improved heat transfer for high power dissipating components. A double sided attach module can dissipate up to 50% of its heat through the lid. Also, the very large contact area, provided by the copper leads, permits larger currents and lower thermal resistance, which improves the thermal management of the package. Other advantages include the elimination of wire bonds in this package, which results in the absence of wire bond related failures. Furthermore, the removal of wirebonds reduces package inductance (~0.5 nH), thus increasing switching speed and current rating. In addition, the inherent low forward voltage drop in ThinPak^{TM} (<1.5V at > 100A/cm^2) [110] when combined with the low electrical resistance of the lid greatly reduces power dissipation levels up to switching frequencies of several tens of kHz. Thus, this technology offers one of the highest areal (>90%) and volumetrically efficient approaches for packaging discrete power semiconductor devices, while improving heat transfer.

There is a drawback, however, to the large contact area of the straps or DBC lid/substrate, in that it leads to stresses caused by large CTE mismatch. Cracking in the solder attach at the die-to-DBC interface can be a failure mechanism in these modules due to the CTE mismatch between the DBC ceramic and the die. In modules where the final connection is made by soldering copper straps to the DBC, instead of by integral connections, cracking at the strap to DBC interface overwhelms cracking at the die-to-DBC interface. Lastly, the thin solder layer on both sides of the die makes the structure less compliant to induced stresses and strains [109].

Previous studies [111] have subjected the ThinPak^{TM} to –55°C to 125°C temperature cycling with ramp rates of 5°C/min up and 10°C/min down, and a dwell time at the maximum and minimum temperatures of 10 minutes. Early failures revealed weakness in the eutectic solder attachment of the copper strap to the top of the lid. This was due to the large CTE mismatch between the unconstrained copper strap (16 ppm/K) and the underlying alumina ceramic lid (4 ppm/K). These straps were removed and the testing

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

continued to the next failure. The second failure occurred at the eutectic solder region where the bottom of the die was attached to the DBC substrate. This interface had a smaller CTE mismatch than the copper strap attachment, with the DBC substrate having a CTE of 10-11 ppm/K, and the silicon die having a CTE of 3 ppm/K. No failures were observed at the high lead solder attach between the alumina ceramic lid (4 ppm/K) and the silicon die (3 ppm/K) either after 2000 thermal cycles or 50,000 power cycles, most likely because of the very close thermal match.

These results show that the double-sided attach approach does have electrical, thermal, and mechanical reliability advantages over a more traditional wirebonding interconnect approach. However, the reliability of the interconnect is STRONGLY dependent on the global CTE mismatch between the surfaces to be joined. Close CTE match between the substrate, lid, and device is necessary, as is the selection of a high temperature solder with good fatigue resistance [109].

Planar Packaging Technology

One of the most recent trends in packaging techniques for power modules is planar packaging, also known as embedded power. In this technique, wire bonds are replaced by direct on-chip interconnections. This eliminates the wire failure mechanisms discussed in the chip and wire modules, and mitigates the attachment fatigue mechanisms critical in the double sided attach module. The use of direct on-chip interconnections leads to very large interfaces between materials. These modules are currently in development by major universities and power electronic system leaders, such as General Electric and Siemens. The layout of materials used is shown in the image below.

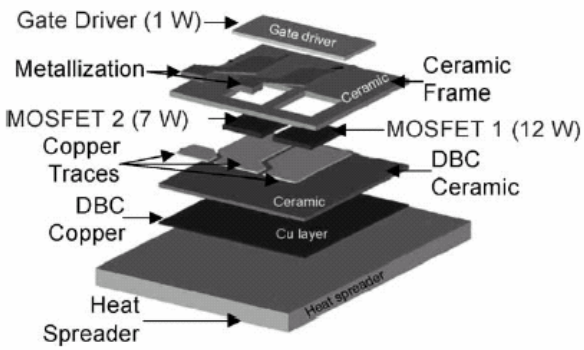


Figure 17 Structure of an Embedded power device[112]

This type of module has three major parts. They are the embedded power transistors and diodes, the electronics circuit, and the base substrate. The fabrication process involves embedding dice into a ceramic frame, which is then coated with a dielectric. Currently, this dielectric is a polymer, which limits the maximum use temperature of this type of package to 200°C-250°C. Later, vias are added to provide a direct copper contact to the gate and emitter pads [113]. Connection to the collector is achieved by soldering the part to the metallized base of the ceramic frame. Thus, this module is susceptible to die attach fatigue and substrate fracture as was the case in the chip and wire module and the double

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

sided attach module. However, the structure mitigates the stresses causing these failures thereby reducing their occurrence.

Research is needed into new high temperature dielectrics that can be incorporated into planar power modules to create versions that can reliably operate at higher maximum temperatures.

As with the other packaging techniques previously discussed, embedded power also has its own unique set of advantages and disadvantages. First of all, there is a very large contact area, which permits the passage of large currents and good heat transfer. However, this can also lead to additional problems due to the large CTE mismatch between the direct copper interconnects and the underlying devices. Expansion mismatch can cause thermal deformation and delamination of the planar interconnections [112]. One element that helps to counteract these stresses is that the polyimide and epoxy dielectric layers work as stress buffer layers, that absorb stress and improve reliability [114]. Perhaps the greatest advantage of this type of packaging is that the planar structure enables the construction of three-dimensional integrated power electronics systems. A major disadvantage is that little is known about this new technology in terms of failure mechanisms and the actual stress levels in the various embedded layers.

Additional study of the failure mechanisms in planar packaged devices and experimental stress measurements in the embedded layers are in order.

What is known about reliability, however, is that the major issue is the thermomechanical strain between different layers. The top copper layer and the semiconductor device have the highest stresses due to their higher elastic moduli. Thermal and power cycling have been used to test the lifetime and reliability of the modules. An experimental analysis of the reliability of a simplified model, which includes only the polyimide substrate and the copper deposition, has already been completed [114]. The test sample is shown below.

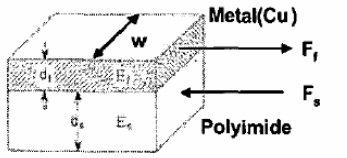


Figure 18 Simplified model of Embedded power Device [114].

From this study, it was found that the most common failure modes are yielding of the copper or polyimide, cracking of the copper, and delamination of the copper. This study also showed that 70% of the simplified models failed after only 250 power cycles of ΔT at 80K starting at a base temperature of -10°C, while 10% failed after only 600 temperature cycles between 0°C and 100°C [114].

A similar packaging technique is Planar Power Polymer Packaging, or P4, developed at GE. This technique interconnects power devices with direct metallurgical contacts to the chip pads[115]. Cross-sectional views of the module at various stages of the fabrication process are shown below.

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

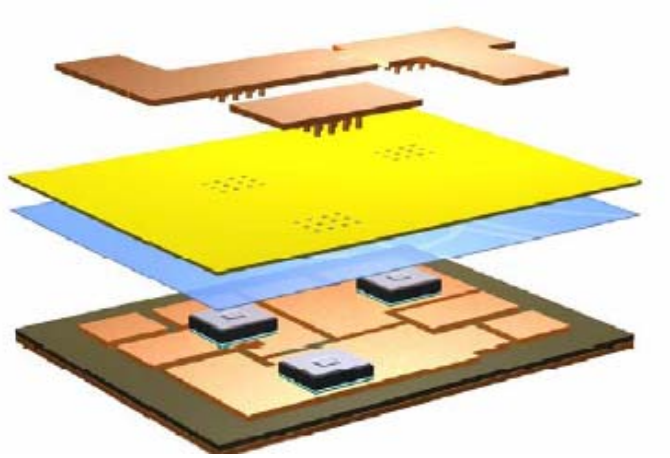


Figure 19 Structure of Planar Power Polymer Packaging device [115]

As with the similar embedded power technique, the P4 packaging technique produces power modules that have a greatly reduced footprint and height, which creates better power density. Also, resistive and inductive interconnect parasitics are reduced by this structure. Lastly, the planar structure eliminates unnecessary structures in the cooling path, which greatly improves the thermal performance of the modules[115]. However, it is susceptible to the same failure mechanisms related to direct copper attach, die attach fatigue, and substrate cracking, and it has the same limitations in use temperature due to the choice of polymer dielectrics. Preliminary reliability studies reveal that the dominant failure mechanism is delamination/cracking of the direct copper attach.

Thus, further reliability analysis of the P4 technology is warranted.

PressPak Technology

A completely different approach to power device packaging is embodied in the IGBT PressPak modules that have been developed in recent years to provide a superior high power alternative to conventional IGBT modules with respect to performance and reliability. A PressPak involves soldering the backside or drain/collector side of silicon transistors and diodes to a metallized ceramic substrate and then interconnecting the top side with a series of springs that apply a constant pressure to obtain good electrical and thermal contact. A PressPak structure eliminates wirebonds, direct copper, and soldered top-side connections and their related failure mechanisms [116]. In order to minimize bowing and shear associated with the thermal mismatch, the PressPak uses sliding contacts, as opposed to a permanent bond such as solder, between the high and low CTE components of the package.

A PressPak power electronic module utilizes compressed springs to connect leads to the IGBT emitter pads and gates. The spring contacting the emitter surface is a bevel spring using inconel washers which are compressed at very high loads in the assembled state (around 500 kN). The inconel washers provide a constant spring constant at high temperatures with little stress relaxation, while signals are shunted around the springs by

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

a small copper strap for improved electrical conductivity. The gate contact area on the IGBT chips (around 2.5-mm^2), is a significantly smaller area than the emitter surface (around 100 mm^2) as seen in Figure 20. As a result, a smaller point contact spring is required for contacting the gate. Due to the reduction of surface area contact, a lower loaded spring is required so as to avoid excessive penetration of the gate pad, which can cause a short circuit.

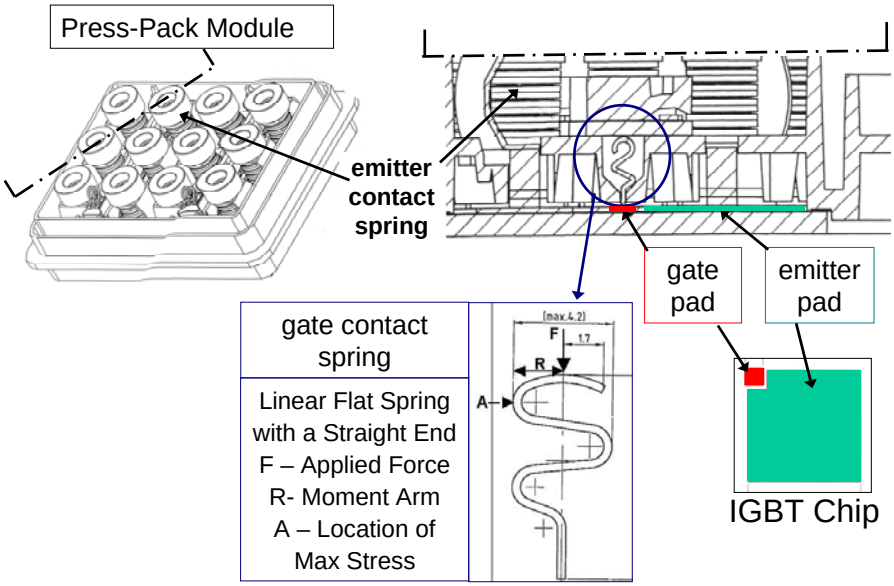


Figure 20 PressPak module and its gate contact spring.

The gate contact spring is typically made of beryllium(2%)-copper C17200 for its good thermal and electrical conductivity and high stiffness properties. BeCu is also known to provide low stress relaxation to temperatures of 175°C – 200°C. Higher use temperatures, up to 300°C-400°C, can be achieved without appreciable stress relaxation by substituting beryllium-nickel. The configuration of the spring is a two dimensional multi-bend configuration known as a flat spring. In order to maintain contact, the spring is initially compressed a fixed displacement when the package is sealed. The point contact at the bottom of the spring must contact the top metallization layer above the gate. However, the spring tip can not be allowed to penetrate to the semiconductor chip. In order to maintain contact and to ensure the operation of the device over its desired lifetime, the gate spring cannot penetrate the metallization layer, and cannot lose contact with the metallization surface during its lifetime. This requires that the chosen initial stress be small enough not to penetrate the metallization layer, but large enough to keep contact with the metallization despite any vibration/shock, or thermal expansion/contraction strains that would act to cause a separation, even when that stress is reduced over time due to stress relaxation at the operating temperature.

The PressPak assembly has additional benefits in very high power applications where high voltage series connections are used. The failure mode of the PressPak IGBT is a short circuit due to the pressure contact structure [117]. This means that if one IGBT

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

fails, it will operate in a Short Circuit Failure Mode (SCFM) allowing the system to continue to conduct the total current in the system, requiring replacement only during scheduled maintenance. One method of achieving the SCFM is to metallurgically alloy the silicon with an optimized contact partner. If the partner is chosen properly, a low melting compound is formed leading to a highly conductive path through the chip. This compound will form quickly even at low power. The alloying of the chip occurs immediately after a high current strike causes the metallurgically optimized material to melt and react with the underlying silicon. The result is reliable SCFM performance after device failure [118]. Conventional IGBT modules have a failure mode that is open which prevents the entire system from working in the event of a single IGBT failure. Compression mount devices such as the PressPak have been in use for some time for high power applications because of their superior reliability. Thyristors and GTO thyristors are examples of devices which have been fabricated using a compression mounting assembly.

While PressPaks eliminate the conventional failure mechanisms of wirebond lift-off and mitigate solder fatigue, unsatisfactory mechanical device configurations may lead to unexpected damage and failures. In fact, the non-uniformity of the applied pressure and thermal cycling of materials with high thermal expansion coefficient mismatch can lead to fretting on the gate pads and thermal fatigue of the springs used in the package. Preliminary failure analysis of PressPak devices has confirmed these failure mechanisms [116, 119]. Further research in this area is warranted.

John Hsu Contact Approaches

John Hsu has been examining a contact method that is a variant of the interconnections discussed in the double-sided attach module above. His plans call for the use of one of three types of bonding scenarios. The first is a double-sided soldering approach in which two copper straps are joined with a sintered silver technology to opposite sides of a chip. The use of silver paste instead of eutectic tin-lead solder would make this approach possible at higher temperatures. However, this approach still has the concerns associated with the large CTE mismatch between the copper straps and the silicon die that was mentioned above. As with that attachment, reliability would be improved by keeping the copper strap as thin as possible and ensuring a bend in the copper strap for stress relief. The use of porous and lower modulus silver powder should ameliorate some of the concern, as it has been shown that sintered silver flake manufactured using the 40 MPa pressure approach has a much longer life than eutectic solder in a fixed application, but it would still be necessary to conduct modeling and accelerated testing to establish that the technique would provide sufficient reliability for this intended application. Such testing would include thermal cycling while monitoring forward voltage.

The second approach is similar to the first, but includes the division of the copper strap into a series of copper fingers. This approach will have improved reliability over the first approach because it limits the strain field generated by the CTE mismatch with no appreciable downside, except for some localization of current and some reduction in heat

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

transfer, neither of which should significantly impact the reliability. The number of fingers should be large enough to reduce the strain field, but not so large as to induce current crowding and distribution effects. Three to eight fingers is usually optimal. Furthermore, it would be a good idea to run a conduction thermal analysis to determine the change in ΔT that occurs during power on/off cycles as a result of the smaller heat transfer surface.

The third approach is a variation on the second approach, but it includes a spacer to limit the susceptibility of the joint to failure by shock and vibration. While the spacer would limit the potential displacement and curvature of the copper strap during vibration loading, it would be useful to conduct a vibration analysis to determine the maximum expected displacement in the fundamental mode to see if use of the spacer is needed. Furthermore, it is important that the spacer be of a ceramic that is thermally matched to the silicon, so that it does not cause expansion related peeling stresses on the copper strap during thermal excursions.

John Hsu is also investigating the effect of placing wirebonds, copper straps, or similar interconnects into a boiling cooling fluid. Wirebonds or similar interconnections exposed to the agitation of a boiling fluid would be subjected to a number of stresses. First, at the initiation of boiling, small bubbles would form and then rapidly collapse. Each time a bubble collapsed, it would send a shock wave through the fluid. These shock waves can be quite sizeable in force and could cause vibration of the wirebonds. Second, as boiling proceeded, the circulation of the fluid could cause wire sweep and lateral motion of the wirebonds, which would be a function of the viscosity of the fluid. Fluorinert, or other insulating fluorocarbon liquids, have viscosities (1.4 cP) on the order of water and should be somewhat benign in this respect. The wires, however, should be spaced well apart in order to ensure that they do not brush against one another in the swirling liquid which, if it occurred, would cause intermittent shorting. Copper straps, and thicker (5-15 mil), wedge bonded aluminum wires such as are typical in power electronics, would be more immune to all these forces than thinner (0.8-1.2 mil), ball bonded gold wires. In fact, it is quite common in thermal management and cooling experiments to place exposed thick wirebonds directly in the cooling fluid. At least in the short run and from the standpoint of overstressing the wires, this does not appear to generate any practical concern. The location on the chip where the boiling is occurring is far enough away from the wirebonds to minimize the stress, and no overstress failures of the wirebonds have been observed. The long term reliability effects of fatigue due to small lateral motions of the wires has not yet been investigated, but, it appears from these initial studies, that wirebonds are able to withstand the boiling with minimal damage. This is much different from the case of ultrasonic agitation of very thin gold bond wires in which the wirebonds effectively couple the high frequency vibration energy and fail rapidly.

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

Summary and Conclusions

Technology related to the development of electronics that can operate in the high temperature environments present in hybrid vehicles has been advancing rapidly. The latest technology developments, commercially available components, and packaging approaches have been detailed in this report. Each of these elements has advantages and disadvantages that must be traded off in order to design an optimum high temperature electronic system containing both small signal control and power electronic devices. Furthermore, each element is susceptible to different failure mechanisms that must be mitigated to provide reliable long term operation. Where the commercially available elements were not up to the challenge of long term operation in the hybrid vehicle environment, alternative designs were suggested or further research was recommended.

Collected Suggestions for Further Research

- Develop specific mission profiles and accelerated testing protocols for the underhood environment for hybrid cars, as has previously been done for gasoline-powered vehicles.
- Further effort in the development of SiC MOSFETs and IGBTs and their associated packaging.
- Address limitations to SiC power devices, including screw dislocation assisted reverse breakdown, ohmic contact issues, interconnection and packaging.
- Address the resistance of the gold-based metallizations to electromigration
- Model fatigue of aluminum wirebonds to improve power electronic module reliability.
- Model copper wire-copper bondpad liftoff failures as power devices move to copper metallization.
- Model the reliability of sintered silver nanopowders and develop alternative high temperature solder/attach techniques.
- Develop silicon nitride substrate technology, especially metallization.
- Develop new high temperature dielectrics that can be incorporated into planar power modules to create version that can reliably operate at higher maximum temperatures.
- Investigate failure mechanisms in planar packaged devices and conduct experimental stress measurements in the embedded layers of P4.

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

References

[1] K. Motavalli, *Forward Drive: The Race to Build Clean Cars for the Future*. New York: Sierra Club Books, 2000.

[2] J. Beretta, Martin, G-M., " PSA Peugeot Citroën Diesel Hybrid Technology," in *International Conference on Automotive Power Electronics* Paris, 2006.

[3] P. Miller, "Mission Profiles for Hybrid Automotive Applications and their Application to Battery," in *International Conference in Automotive Power Electronics* Paris, 2006.

[4] A. Kawahashi, "A New Generation Hybrid Electric Vehicle and Its Implications on Power Electronics," in *CPES Power Electronics Annual Seminar*, Blacksburg, VA, 2004, pp. 15-20.

[5] Danfoss, *Facts worth knowing of Frequency converters*, 1998.

[6] Wikipedia, "Power Semiconductor Device," 2007.

[7] J. K. Pedersen, "Voltage levels in power electronics for hybrid cars," Aalborg, 2007.

[8] D. M. F. P. L. Dreike, D. B. King, D. C. Sprauer, and T. E. Zipperian, "An Overview of High-temperature Electronic Device Technologies and Potential Applications," *IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part A*, vol. 17, p. 594, 1994.

[9] J. R. Bromstead, and Baumann, E.D., "Performance of Power Semiconductor Devices at High Temperature," in *First International High Temperature Electronics Conference*, Albuquerque, NM, 1991, pp. 27-35.

[10] P. L. Dreike, "Chapter 2.3: Silicon MOSFETs," in *High Temperature Electronics*, P. McCluskey, Grzybowski, R.R., and Podlesak, T.F., Ed. Boca Raton, FL: CRC Press, 1996.

[11] R. Muller, and Kamins, T.I., *Device Electronics for Integrated Circuits*, 2 ed. New York: John Wiley & Sons, 1986.

[12] R. R. Troutman, *Latchup in CMOS technology: The Problem and its Cure*. Boston, MA: Kluwer Academic Publisher, 1986.

[13] P. L. a. L. Brusius, M., "Chapter 2.4: Silicon-on-Insulator Technology," in *High Temperature Electronics*, P. McCluskey, Grzybowski, R.R., and Podlesak, T.F., Ed. Boca Raton, FL: CRC Press, 1996.

[14] I. B. I. S. Technology-Corporation, "SIMOX for High Temperature Applications," Danvers, MA 1991.

[15] P. L. Dreike, Fleetwood, D.M., King, D.B., Sprauer,D.C., and Zipperian, T.E., "An Overview of High-temperature Electronic Device Technologies and Potential Applications," *IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part A*, vol. 17, p. 594, 1994.

[16] R. B. Brown, Terry, F.L., and Wu, K.C., "Temperature Microelectronics - Expanding the Applications for Smart Sensors," in *International Electron Devices Meeting, IEDM87*, Washington D.C., 1987, p. 247.

[17] J. S. Suehle, Chaparala, P., and Messik, C., "High Temperature Reliability of Thin Film SiO2," in *Second International High Temperature Electronics Conference*, Charlotte, NC, June 1994, pp. VIII-15.

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

[18] D. Das, Pecht, M., and Pendse, N., *Rating and Uprating of Electronic Products* College Park, MD: CALCE EPSC Press, 2004.
[19] A. D. Systems, "Hot! Hot! Hot! Extending the Temperature Range for 32 Bit Embedded Systems." vol. 2001, 2001.
[20] J. Rhea, "COTSCON Attendees Agree: Upscreening is Here to Stay," *Military and Aerospace Electronics*, June 1, 1999.
[21] T. Brennom, and Anderson, N, "Uprating Experience by an Avionics OEM," in *Commercialization of Military and Space Electronics*, Los Angeles, CA, February 12-15, 2001, pp. 317-323.
[22] NationalSemiconductor, "Note from the Editor," *National Semiconductor Navigator*, vol. 16, 1999.
[23] GIDEP, "GIDEP Alert CM2-P-98-01," *Analog Devices*, April 20, 1998.
[24] J. Fabula, "Up-Screening of Xilinx Products," Xilinx Inc July 28, 2002.
[25] R. Biddle, "Reliability Implications of Derating High-Complexity Microcircuits," *COTS Journal*, pp. 39-43, February 2001.
[26] R. J. Kroeger, "Letter to Customer," Texas Instruments 10 September 1997.
[27] R. C. Byrne, "SIA/GPC Addresses the Importance of Understanding COTS," Semiconductor Industry Association (SIA), 1997.
[28] N. Lycoudes, "Advanced Technology," in *Acquisition, Qualification and Reliability Workshop* Newport Beach, CA: Motorola Semiconductors, August 15-17, 1995.
[29] Intel, *Military Product Data Book*, 1990.
[30] MicronSemiconductor, "TN-00-07 - IBIS Behavioral Models," 1998.
[31] D. Foty, *MOSFET Modeling with SPICE: Principles and Practices*. Upper Saddle River, NJ: Prentice Hall PTR, 1997.
[32] L. Condra, Kromholt, G., Pecht, M., and Hakim, E., "Using Plastic-Encapsulated Microcircuits in High Reliability Application," in *Annual Reliability and Maintainability Symposium*, January 24-27, 1994, pp. 481-493.
[33] D. B. Cotton, "COTS Design Testing and Production Qualification for Rugged Environments," *COTS Journal*, pp. 48-59, September 2001.
[34] UnitedStatesDepartmentofDefense, *Mil-Std-883: Test Method Standards - Microcircuits*, 1996.
[35] L. Condra, Wenzel, G., and Pecht, M., "Reliability Evaluation of Simple Logic Microcircuits in Surface Mount Plastic Packages," in *ASME Winter Annual Meeting*, New Orleans, LA, November 1993, pp. 85-100.
[36] D. Emerson, et. al, "Plastic-Encapsulated Microcircuit Reliability and Cost Effectiveness Study," *IEEE Transactions on Reliability*, vol. 45, pp. 19-22, 1996.
[37] M. Pecht, and Biagini, R., "The Business, Product Liability and Technical Issues Associated with Using Electronic Parts Outside the Manufacturer's Specified Temperature Range," in *Pan Pacific Microelectronics Symposium and Tabletop Exhibit*, Maui, HI, February 5-7, 2002, pp. 391-398.
[38] S. Tam, "Demonstrated Reliability of Plastic-Encapsulated Microcircuits for Missile Applications," *IEEE Transactions on Reliability*, vol. 44, pp. 8-12, 1995.

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

[39] N. Pendsé, and Pecht, M., "Parameter Re-characterization Case Study: Electrical Performance Comparison of the Military and Commercial Versions of All Octal Buffer," *Future Circuits International*, vol. 6, pp. 63-67, 2000.

[40] J. Chapman, ""Crisis Overstated", Letter to the Editor," *Military and Aerospace Electronics*, vol. 14, April 2003.

[41] J. Powell, "The Case for COTS," *COTS Journal*, pp. 65-68, May 2002.

[42] R. R. Grzybowski, and McCluskey, F.P., "The performance of Polymer Capacitors at Elevated Temperatures," in *Third International High Temperature Electronics Conference*, Albuquerque, NM, June 1996, pp. 6-15.

[43] E. Furman, Lanagan, M.,Jones, B.,Shrout, T., Yoon, S-Y., Schwarze, G.E., "Dielectric Materials Development for High Temperature Capacitors," in *2004 IMAPS International Conference and Exhibition on High Temperature Electronics*, Santa Fe, NM, May 17-20, 2004.

[44] E. F. Alberta, Hackenberger, W.S., Randall, C.A, and Shrout, T.R., "High Temperature Ceramic Multilayer Capacitors," in *2004 IMAPS International Conference and Exhibition on High Temperature Electronics*, Santa Fe, MN, May 17-20.

[45] R. E. Bauer, and Clelland, I.W., "Performance of a Multilayer Film Capacitor in Severe Applications," in *CARTS 1990 - Proceedings of the Capacitor and Resistor Technology Symposium*, San Fransisco, CA, 1990, pp. 128-133.

[46] A. N. Hammoud, et. al, "High Temperature Power Electronics for Space," NASA Lewis Research Center, Cleveland, OH NASA Technical Memorandum 104375, 1991.

[47] A. N. Hammoud, and Myers, I.T., "Evaluation of High Temperature Capacitor Dielectrics," NASA Lewis Research Center, Cleveland, OH NASA Technical Memorandum 105622, 1989.

[48] A. N. Hammoud, and Suthar, J.L., "Characterization of Polybenzimidazole (PBI) Film at High Temperatures," NASA Lewis Research Center, Cleveland, OH NASA Technical Memorandum 189174, 1992.

[49] J. O. Harris, "Energy Density Capacitor Technology at Sandia National Laboratories," in *Workshop on High Temperature and Radiation Hardened Electronics*, Albuquerque, NM, 1989, pp. C8-C14.

[50] R. S. Buritz, "Advanced Capacitor Development," in *Workshop on High Temperature and Radiation Hardened Electronics*, Albuquerque, NM, 1989, pp. C8-C14.

[51] J. L. Suthar, Khatchen, W., Laghari, J.R.,Hammoud, A.N., Myers, I.T., and Domitz, S., "Dielectric Films for High Temperature High Power Electronics Applications," in *First International High Temperature Electronics Conference*, Albuquerque, NM, 1991, p. 105.

[52] E. Overton, Hammoud, A.N., Baumann, E.D, and Myers, I.T., "Thermal Aging Effects on the Electrical Properties of Film and Ceramic Capacitors," in *Electrical/Electronics Insulation Conference*, Chicago, IL, 1993, pp. 201-206.

[53] R. R. Grzybowski: United Technologies Research Center, 1997.

F. Patrick McCluskey, Ph.D.
Consulting

2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

[54] M. A. Carter, "Film Materials for High Temperature Operation," in *2004 IMAPS International Conference and Exhibition on High Temperature Electronics*, Santa Fe, NM, May 17/20 2004.

[55] C. W. T. McLyman, *Transformer and Inductor Design Handbook*. New York: Marcel Dekker, 1988.

[56] M. E. McHenry, Hsiao, A., Willard, M.A., and Harris, V.G., "Magnetic Materials for Use in Passive Components for High Temperature Power Electronic Applications," in *5th International Conference on High Temperature Electronics*, Alberquerque, NM, June 2002.

[57] M. E. McHenry, Willard, M.A, and Laughlin, D.E., *Prog. Mat. Sci.*, vol. 44, p. 291, 1999.

[58] R. R. Grzybowski, "High Temperature Electronics Short Course," in *4th International High Temperature Electronics Conference*, Albuquerque, NM, June 1998.

[59] M. A. Willard, Laughlin, D.E., McHenry, M.E., Thoma, D., Sickafus, K., Cross, J.O. and Harris, G., *Journal of Applied Physics*, vol. 84, p. 6773, 1998.

[60] M. A. Willard, Franchetti, C., Huang, M-Q., Laughlin, D.E., McHenry, M.E., Cross, J.O., and Harris, V.G., *Journal of Applied Physics*, vol. 85, pp. 4421-23, 1999.

[61] H. Iwanabe, Lu, B., McHenry, M.E., and Laughlin, D.E., *Journal of Applied Physics*, vol. 85, pp. 4424-26, 1999.

[62] R. K. Kirschman, "Passive Components," in *High Temperature Electronics*, R. K. Kirschman, Ed. New York, NY: IEEE Press, 1999, pp. 639-659.

[63] M. G. Pecht, and Agarwal, R., "Physical Architecture of VLSI Systems," in *Electronic Packaging Matererials and their Properties*, R. J. Hanneman, Kraus, A.D., Pecht, M.G., Ed. Nyw York, NY: John Wiley & Sons, 1994.

[64] R. R. Grzybowski, "Third Quarter Progress Report," in *High Temperature Distributed Control System TRP Meeting* West Palm Beach, FL, April 1997.

[65] D. A. Dalman, and Hoover, M.F., "PIBO Film Dielectric for Advanced Microelectronics Packaging," in *2004 IMAPS International Conference and Exhibition on High Temperature Electronics*, Santa Fe, NM, May 17-20 2004.

[66] T. Braun, Becker, K-F., Koch, M., Bader, V., Aschenbrenner, R., and Reichl, H. , "High Temperature Potential of Flip Chip Assemblies," in *2004 IMAPS International Conference and Exhibition on High Temperature Electronics*, Santa Fe, NM, May 17-20, 2004.

[67] CALCE, "Defects Webbok," College Park, MD: CALCE EPSC.

[68] M. J. Li, Gohari, K., Pecht, M., "Effect of Temperature and Humidity Cycling on FR-4, bis-maleimide Triazine, and Cyanate Ester Printed Wiring Boards," in *7th International SAMPE Electronic Conference*, 1994.

[69] G. Kohman, Hermance, H., and Downes, G., "Silver Migration in Electrical Insulation," *The Bell System Technial Journal*, pp. 1115-1147, 1955.

[70] D. Lando, Mitchell, J., and Welsher, T., "Conductive Anodic Filament in Reinforced Polymeric Dielectrics: Formation and Prevention," in *Seventeenth International Reliability Physics Symposium*, 1979, pp. 51-63.

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

[71] M. Pecht, Wu, B., and Jennings, D., "Conductive Filament Formation in Printed Wiring Boards," in *Thirteenth IEEE/CHMT International Electronics Manufacturing Technology Symposium*, 1992, pp. 74-79.

[72] K. Rogers, Hillman, C., and Pecht, M., "Conductive Filament Formation Failure in a Printed Circuit

Board," *Circuit World*, vol. 25, pp. 6-8, 1999.

[73] J. Lahti, Delaney, R., and Hines, J., "The Characteristic Wearout Process in Epoxy-Glass Printed Circuits for High Density Electronic Packaging," in *Seventeenth International Reliability Physics Symposium*, 1979, pp. 39-43.

[74] S. Krumbein, "Metallic Electromigration Phenomena," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, vol. 11, pp. 5-15, 1988.

[75] B. Rudra, Pecht, M., and Jennings, D., "Assessing Time-to-Failure due to Conductive Filament Formation in Multi-Layer Organic Laminates," *IEEE Transactions on Components, Packaging and Manufacturing Technology, Part B: Advanced Packaging*, vol. 17, pp. 269-276, 1994.

[76] B. Rudra, and Jennings, D., "Failure-Mechanism Models for Conductive-Filament Formation," *IEEE Transactions on Reliability*, vol. 43, pp. 354-360, 1994.

[77] A. Shukla, Pecht, M., Jordan, J., Rogers, K. and Jennings, D., "Hollow Fibers in PCB, MCM-L and PBGA Laminates May Induce Reliability Degradation," *Circuit World*, vol. 23, pp. 5-6, 1997.

[78] A. Shukla, Dishongh, T., Pecht, M., and Jennings, D., "Hollow Fibers in Woven Laminates," *Printed Circuit Fabrication*, vol. 20, pp. 30-32, 1997.

[79] M. Pecht, Hillman, C., Rogers, K., and Jennings, D., "Conductive Filament Formation: A Potential Reliability Issue in Laminated Printed Circuit Cards with Hollow Fibers," *IEEE Transactions on Electronics Packaging Manufacturing*, 1999.

[80] M. Osterman, and Stadterman, T., "Reliability and Performance of Advanced PWB Assemblies," in *High Performance Printed Circuit Boards*, C. A. Harper, Ed. New York, NY: McGraw-Hill, 1999.

[81] M. Pecht, Nguyen, L.T., and Hakim, E. B., "Plastic Encapsulated Microelectronics," New York, NY: John Wiley & Sons, 1994.

[82] A. Kawahashi, "A New Generation Hybrid Electric Vehicle and Its Implications on Power Electronics," in *CPES Power Electronics Annual Seminar*, Blacksburg, VA, April 18-20, 2004, pp. I-15-I-20.

[83] A. Lostetter, Barlow, F., and Elshabini, A., "An overview to integrated power module design for high power electronics packaging," *Microelectronics Reliability*, vol. 40, p. 14, 2000.

[84] S. Haque, Xing, K.,Suchicital, C., Nelson, D.J., Lu, G-Q.,Borojevic, D. and Lee, F.C., "Thermal Management of High-Power Electronics Modules Packaged With Interconnected Parallel Plates," in *SEMI-THERM*, 1998, pp. 111-119.

[85] S. Haque, Xing, K.,Lin, R.L.,Suchicital, C.T.A., Lu, G.Q, Nelson, D.J., Borojevic, D., and Lee, F.C, "An innovative technique for packaging power electronic building blocks using metal posts interconnected parallel plate structures," *IEEE Transactions on Advanced Packaging*, vol. 22, May 1999.

F. Patrick McCluskey, Ph.D.
Consulting

2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

[86] M. Pecht, *Product Reliability, Maintainability, and Supportability Handbook*. College Park, MD: CRC, 1995.

[87] K. Meyyappan, P. McCluskey, and P. Hansen, "Wire Flexural Fatigue Model for Asymmetric Bond Height," in *InterPACK*, Maui, HI, July 7-11, 2003.

[88] F. P. McCluskey, "Wires and Wirebonds," in *High Temperature Electronics*, F. P. McCluskey, Grzybowski, R.R., and Podlesak, T.F., Ed. Boca Raton, FL, 1996.

[89] M. Pecht, *IC, Hybrid, and Multichip Module Package Design Guidelines*. New York: John Wiley and Sons, 1994.

[90] J. L. Newsome, et al., "Metallurgical Aspects of Aluminum Wirebonds to Gold Metallization," in *14th Annual Proceeding of the IEEE Electronic Components Conference*, 1976, p. 63.

[91] W. Takei, J., and Francombe, M.H., "Measurement of Diffusion Induced Strains at Metal Bond Interfaces," *Solid State Electronics*, vol. 11, pp. 205-208, 1968.

[92] J. Benoit, Chin, S.,Grzybowski, R.,Lin, S.,Jain, R., and McCluskey, P., "Wire Bond Metallurgy for High Temperature Electronics," in *Proc. of the 4th IEEE Int'l High Temperature Electronics Conference*, Albuquerque, NM, June 14-18, 1998, pp. 109-113.

[93] D. R. Frear, "High Temperature Solder Materials and Conductive Adhesives," in *High Temperature Electronics*, F. McCluskey, P., Grzybowski, R.R., and Podlesak, T.F., Ed. Boca Raton, FL: CRC Press, 1996.

[94] N. C. Lee, "Getting ready for lead-free solders," in *SMTA Learning Institute*, Ellicott City, MD, April 1997.

[95] S. Jin, "Developing Lead-free Solders: A Challenge and Opportunity," *Journal of Metals*, vol. 7, p. 13, 1993.

[96] H. Schwartzbauer, Kuhnert, R., "Novel Large Area Joining Technique for Improved Power Device Performance," *IEEE Transactions on Industry Applications*, vol. 27, pp. 93-95, 1991.

[97] Z. Zhang, and Lu, G-Q., "Pressure-Assisted Low-Temperature Sintering of Silver Paste as an Alternative Die-Attach Solution to Solder Reflow," *IEEE Transactions on Electronics Packaging Manufacturing*, vol. 23, pp. 279-283, 2002.

[98] R. Amro, Lutz, J., Rudzki J., Thoben, M., and Lindemann, A., "Double-Sided Low-Temperature Joining Technique for Power Cycling Capability at High Temperature," in *EPE* Dresden, 2005.

[99] Z. Zhang, Calata, J.N.,Bai, J.G., and Lu, G-Q., "Nanoscale Silver Sintering for High-Temperature Packaging of Semiconductor Devices," in *Materials Processing and Manufacturing Division Fifth Global Symposium*, 2004, pp. 129-135.

[100] F. P. McCluskey, "Fatigue and Intermetallic Formation in Lead Free Solder and Die Attach," in *MRS Spring Meeting 2001: Microelectronics and Microsystems Packaging, Symposium N. Materials Research Society*, Boston, MA, April 2001.

[101] Z. a. L. Zhang, G-Q., "Low Temperature Sintering of Silver Paste as a Viable Die-Attach Solution for High Temperature Packaging," in *2004 IMAPS International Conference and Exhibition on High Temperature Electronics*, Santa Fe, 17-20 May.

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

[102] S. H. Mannan, and Clode, M.P., "Molten Solder Interconnects: Long Term Reaction Studies and Applications," in *2004 IMAPS International Conference and Exhibition on High Temperature Electronics*, Santa Fe, NM, May 17/20.
[103] M. Dr. Shaw, April 18 2004.
[104] T. Bloom, "CTS Technical Memorandum," CTS Corporation, Elkhart, IN 1996.
[105] H. K. a. C. Charles Jr., G.V., "Packaging Considerations for High Temperature Operation," in *Second International High Temperature Electronics Conference*, Charlotte, NC, June 1994, pp. IX-3.
[106] M. Bratcher, Yoon, R.J., and Whitworth, W., "Aluminum Nitride Package for High Temperature Applications," in *Third Internationall High Temperature Electronics Conference*, Albuquerque, NM, 1996.
[107] T. Martin, and Bloom, T., "High Temperature Aluminum Nitride Packaging," in *Third International High Temperature Electronics Conference*, Albuquerque, NM, 1996.
[108] K. A. Moore, and Siahpush, A.S., "High Temperature Electrical Printed Wiring Board Functions at 350C," in *2004 IMAPS International Conference and Exhibition on High Temperature Electronics*, Santa Fe, NM, May 17-20 2004.
[109] J. N. Calata, Bai, J.G., and Liu, X.S., "Three-Dimensional Packaging for Power Semiconductor Devices and Modules," *IEEE Transactions on Advanced Packaging*, vol. 28, Aug. 2005.
[110] V. Temple, "Advanced silicon power devices for pulsed power applications," in *European Pulse Power Conference* St. Louis, France, 2002.
[111] K. Ghosh, McCluskey, F. P., Temple, V.A.K., "Mechanical Reliability Evaluation of Chip Scale Power Package," in *Int'l Mechanical Engineering Congress and Exposition*, Orlando, FL, 2005, p. Paper 81111.
[112] N. Zhu, Van Wyk, J.D., Liang, Z.X., and Ordendaal, W.G.H., "A study of thermal stress and intrinsic residual stress in planar metallization for integrated power modules," *IEEE Transactions on Industry Applications*, vol. 41, Dec 2005.
[113] S. Dieckerhoff, Guttowski, S., and Reichl, H., "Performance Comparison of Advanced Power Electronic Packages for Automotive Applications," in *Automotive Power Electronics Conference* Paris, June 2006.
[114] N. Zhu, Van Wyk, J.D. , and Liang, Z.X., "Thermal-Mechanical Stress Analysis in Embedded Power Modules," in *35th Annual IEEE Power Electronics Specialists Conference*, Aachen, Germany, 2004, pp. 4503-4508.
[115] R. Fillion, Delgado, E., Beaupre, R., McConnelee, P., "High Power Planar Interconnect for High Frequency Converters," in *Electronics Packaging Technology Conference*, 2004.
[116] P. Cova, Nicoletto, G., Pirondi, A., Portesine, M., and Pasqualetti, M, "Power Cycling on Press-Pack IGBTs: Measurements and Thermomchanical Simulations," *Microelectronics Reliability*, vol. 39, pp. 1165-1170 1999.
[117] Y. Uchida, Seki,Y., Takahashi,Y., and Ichijoh,M. , "Development of High Power Press-Pack IGBT and its Applications," in *Proceedings 22nd International Conference on Microelectronics*, Servia, 14-17 May, 2000, pp. 125-129
[118] H. Zeller, and Lange, T, "Short Circuit Resistant IGBT Module." vol. EP0989611

F. Patrick McCluskey, Ph.D.
Consulting
2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

[119] A. Pirondi, Nicoletto,G., Cova, P., Pasqualetti, M., and Portesine, M., "Thermo-Mechanical Finite Element Analysis in Press-Packed IGBT," *Design. Microelectronics Reliability*, vol. 40, pp. 1163-1172, July 2000.

F. Patrick McCluskey, Ph.D.
Consulting

2811 St. Johns Lane
Ellicott City, MD 21042
(410)-218-3094

DISTRIBUTION

Internal

1. D. J. Adams
2. K. P. Gambrell
3. E. C. Fox
4. L. D. Marlino
5. M. Olszewski
6. Laboratory Records

External

7. R. Al-Attar, DCX, raa9@dcx.com.
8. T. Q. Duong, U.S. Department of Energy, EE-2G/Forrestal Building, 1000 Independence Avenue, S.W., Washington, D.C. 20585.
9. R. R. Fessler, BIZTEK Consulting, Inc., 820 Roslyn Place, Evanston, Illinois 60201-1724.
10. K. Fiegenschuh, Ford Motor Company, Scientific Research Laboratory, 2101 Village Road, MD-2247, Dearborn, Michigan 48121.
11. V. Garg, Ford Motor Company, 15050 Commerce Drive, North, Dearborn, Michigan 48120-1261.
12. G. Hagey, Sentech, Inc., 501 Randolph St., Williamsburg, Virginia 23185.
13. E. Jih, Ford Motor Company, Scientific Research Laboratory, 2101 Village Road, MD-1170, Rm. 2331, Dearborn, Michigan 48121.
14. K. J. Kelly, National Renewable Energy Laboratory, 1617 Cole Boulevard, Golden, Colorado 80401.
15. A. Lee, Daimler Chrysler, CIMS 484-08-06, 800 Chrysler Drive, Auburn Hills, Michigan 48326-2757.
16. F. Liang, Ford Motor Company, Scientific Research Laboratory, 2101 Village Road, MD1170, Rm. 2331/SRL, Dearborn, Michigan 48121.
17. M. W. Lloyd, Energetics, Inc., 7164 Columbia Gateway Drive, Columbia, Maryland 21046.
18. F. Patrick McCluskey, 2811 St. John's Lane, Ellicott City, Maryland 21042.
19. M. Mehall, Ford Motor Company, Scientific Research Laboratory, 2101 Village Road, MD-2247, Rm. 3317, Dearborn, Michigan 48124-2053.
20. J. A. Montemarano, Naval Surfae Warfare Center, Carderock Division; Code 642, NSWD, 9500 MacArthur Boulevard; West Bethesday, Maryland 20817.
21. N. Olds, United States Council for Automotive Research (USCAR), nolds@uscar.org
22. J. Rogers, Chemical and Environmental Sciences Laboratory, GM R&D Center, 30500 Mound Road, Warren, Michigan 48090-9055.
23. S. A. Rogers, U.S. Department of Energy, EE-2G/Forrestal Building, 1000 Independence Avenue, S.W., Washington, D.C. 20585.
24. G. S. Smith, General Motors Advanced Technology Center, 3050 Lomita Boulevard, Torrance, California 90505.
25. E. J. Wall, U.S. Department of Energy, EE-2G/Forrestal Building, 1000 Independence Avenue, S.W., Washington, D.C. 20585.
26. B. Welchko, General Motors Advanced Technology Center, 3050 Lomita Boulevard, Torrance, California 90505.
27. P. G. Yoshida, U.S. Department of Energy, EE-2G/Forrestal Building, 1000 Independence Avenue, S.W., Washington, D.C. 20585.