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Delay Locked Loop Integrated Circuit

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Delay Locked Loop Integrated Circuit

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Abstract:
This report gives a description of the development of a Delay Locked Loop (DLL) integrated circuit (IC). The DLL was developed and tested as a stand-alone IC test chip to be integrated into a larger application specific integrated circuit (ASIC), the Quadrature Digital Waveform Synthesizer (QDWS). The purpose of the DLL is to provide a digitally programmable delay to enable synchronization between an internal system clock and external peripherals with unknown clock skew. The DLL was designed and fabricated in the IBM 8RF process, a 0.13 μm CMOS process. It was designed to operate with a 300MHz clock and has been tested up to 500MHz.

Contents

Nomenclature

ADS	-	Agilent Corporation's Advanced Design System software
ASIC	-	Application Specific Integrated Circuit
CMOS	-	Complementary metal oxide semiconductor
dBm	-	Decibels relative to one milliwatt
DC	-	Direct current
DDA	-	Differential difference amplifier
DLL	-	Delay locked loop
FY	-	Fiscal Year
GSG	-	Ground-signal-ground probe type
GSSG	-	Ground-signal-signal-ground probe type
GHz	-	Giga Hertz (billion cycles/sec)
HP	-	Hewlett Packard Corporation
IBM	-	International Business Machines Corporation
IC	-	Integrated circuit
IDDQ	-	Quiescent drain current testing
IF	-	Intermediate Frequency
I/O	-	Input / output
ISM	-	Instrumentation, Scientific, and Medical frequency band
LDRD	-	Lab Directed Research and Development
LSB	-	least significant bit
MATLAB	-	Simulation software available from MathWorks
MHz	-	Mega Hertz (million cycles/sec)
Mm	-	Milli-meters
NPN	-	A type of bipolar transistor
PCB	-	Printed Circuit Board
PFD	-	Phase frequency detector
PMOS	-	P-type metal oxide semiconductor transistor
PSEC	-	pico-second
QDWS	-	Quadrature digital waveform synthesizer
RF	-	Radio Frequency
SAW	-	Surface Acoustic Wave
SiGe	-	Silicon germanium technology
SMA	-	Subminiature type 'A' connector
SPICE	-	Simulation Program with Integrated Circuit Emphasis

Introduction

When Dante wrote the Divine Comedy in 1321, he stated the medieval belief that the world had only one time zone. For practical purposes communication was so slow that clock variations between terrestrial regions were not observable. Captain Cook made a journey around the world primarily to perform a transit measurement of Venus across the Sun in 1776 to enhance the ability of mariners to synchronize their clocks on long sea voyages. During Cook's era, clock variations between large regions had significance for only a select few. The completion of the U.S. transcontinental railroad in 1869 highlighted the need for universal synchronization of clocks across zones hundreds of miles across. It was shortly after this milestone that universal time zones began to be instituted. These changes highlight the fact that increases in communication speed lead to ever smaller domains across which one must synchronize clocks. The problem of synchronizing clocks between a microprocessor and its peripherals led to the development of the first delay locked loop (DLL) for the MIPS R3000 chip set in 1988 [1]. The use of the phase locked loop (PLL), common for decades in FM demodulators, became ubiquitous for synchronizing clocks across a single large integrated circuit by the late 1990's. Extrapolating this trend leads to an easy prediction: future applications will require local synchronization of clocks for ever smaller domains.

As operating frequencies increase into the microwave range and overall chip dimensions greatly exceed a wavelength at the operating frequency, integrated circuit sub-elements increasingly appear as distributed, rather than lumped circuits. That is, transmission line effects dominate for communication between these ever smaller blocks. High speed integrated circuits face particular difficulties with providing a coherent clock to all portions of the circuit. Since the clock edge is assumed to provide a stable reference to all portions of a digital circuit, it is critical that shifts or skews in that edge be maintained within controlled bounds. In order to supply a clock with a synchronized edge, in situations where the latency at the time of design is unknown, a simple, selectable approach is to insert a DLL to provide a programmable delay between the input clock and the desired output clock. Each block can then be independently synchronized after the final circuitry is assembled.

The DLL is a simple means of providing a programmable clock delay between input and output to provide for clock synchronization. It is significantly simpler and more robust than a PLL. The PLL is capable of producing programmable frequency outputs from a single input frequency; the DLL is typically just used for clock synchronization. Since the physical sizes of clock domains are on a rapidly decreasing slope, it is important to focus on the simplest, easiest to miniaturize block that will accomplish clock synchronization. This block is the DLL.

Simple Open Loop Delay Circuit

Before considering the full DLL circuit, it is instructive to consider a simple, open loop delay circuit (Figure 1). Such a circuit is often considered for its simplicity, so it is appropriate to think about its advantages and disadvantages. A simple, programmable digital delay circuit can be built from a programmable low pass filter and a Schmitt trigger inverter. An additional inverter can be added to buffer the input digital signal.

The use of a Schmitt trigger inverter on the input is optional; the gate could be a simple buffer or inverter. The input buffer is followed by a low pass filter with a time constant close to the expected input signal period. The use of a variable resistor provides for the programmability of the delay. If digital programmability is required, a digital potentiometer can be used in the low pass filter. If a wide range of expected input signal frequencies must be accommodated, then variable capacitance values must also be switched into or out of the low pass filter. This can be built in the same manner as a digital potentiometer, by connecting an array of capacitors through a switch matrix. The low pass filter gives an exponential rise and fall time delay to the input digital signal.

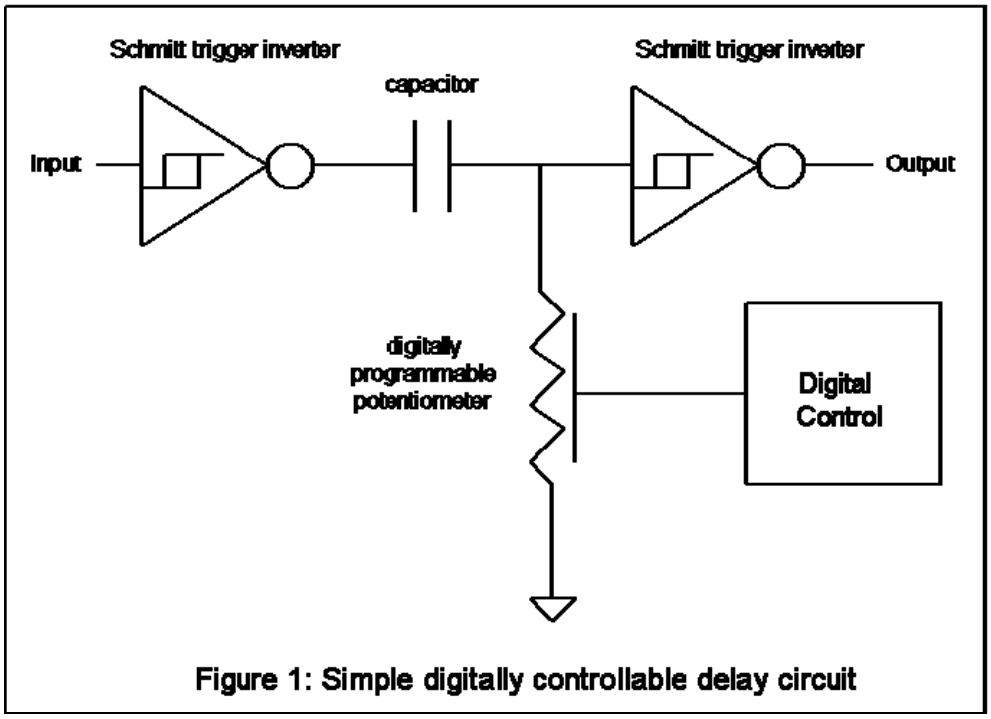

Figure 1: Simple digitally controllable delay circuit

The use of a Schmitt trigger inverter following the analog low pass filter is critical. A Schmitt trigger inverter has hysteresis in its input-to-output transfer function. Noise superimposed on a monotonically changing input signal will cause a conventional logic gate to trip multiple times as the input waveform passes through its trip point. At very high frequencies, the logic gate may not change state, but phase noise is introduced into the output signal, as the noise on the input signal introduces an uncertainty as to the exact location of the trip point in time. The Schmitt trigger inverter provides a much higher gain at its initial trip point to reduce the phase noise at very high frequencies, and its hysteresis prevents signal chatter due to multiple output transitions at lower frequencies.

The advantage of the circuit in figure 1 is its simplicity. Its disadvantages are several. First, the circuit operates in an open loop configuration. It has no capability for automatically tracking input frequency or phase changes with variations in temperature, operating voltage, etc. Second, the circuit is single ended rather than differential, so it will be strongly subject to variations in supply voltage. Third, the loop depends for its

timing on capacitance and resistance values, which will vary with temperature and operating voltage.

Delay Locked Loop Overview

To overcome the limitations of the simple digital delay circuit, a Delay Locked Loop (DLL) can be used instead. The DLL is a phase-locked device, so it tracks most variations in the input signal. Also, the DLL described here is a differential device, so it mitigates variations in supply voltage and temperature. The DLL integrated circuit was designed and fabricated as a stand-alone test circuit in the IBM 8RF 0.13 µm CMOS process. It was then integrated into the Quadrature Digital Waveform Synthesizer (QDWS) IC. This report deals with the DLL as a stand-alone test chip, even though the DLL was designed for integration into a larger ASIC. It can be used for multiple purposes, but it was designed for use as a clock synchronization block – to enable synchronizing an internal ASIC clock to an external peripheral device.

The DLL described here is a 5-bit device designed to operate at 300MHz. That is, it is designed to accept a differential input clock at 300MHz and produce from it a selectable 300MHz differential output clock with variable delays in steps of 1/32 of the input clock. At 300MHz, the selectable step size is 104 psec for each LSB on the selection lines. The IBM 8RF process uses a core voltage of 1.5v and an I/O voltage of 2.5v. The DLL was originally designed to run at the core voltage, but subsequent testing has revealed that full performance is achieved with the DLL operating at the I/O voltage.

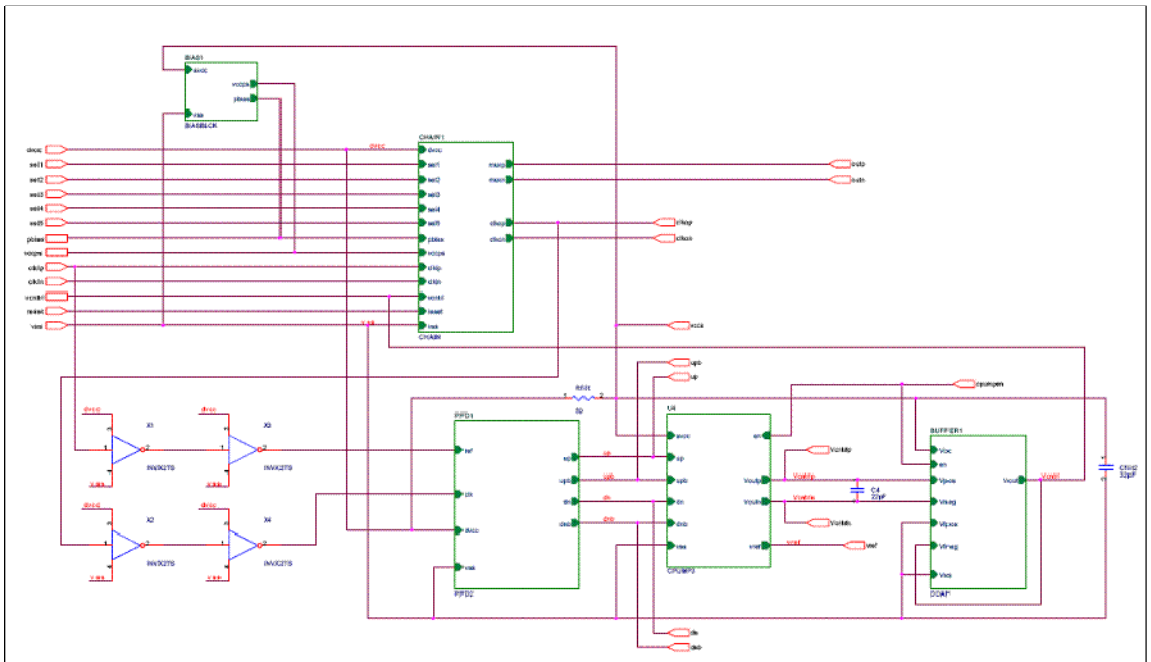

Figure 2: DLL Top Level Schematic

Schematics

The top level view of the DLL is shown in figure 2. It consists of five main blocks, the chain, phase-frequency detector (PFD), charge pump, differential difference amplifier

(DDA), and bias block. The chain block provides the variable delay, while the PFD, charge pump and DDA provide a mechanism for sensing and providing feedback on the adjustments to the amount of delay. The output of the 32 element chain block is fed back to be phase compared to the input via the phase-frequency detector. The digital output of the PFD is turned into a differential analog signal by the charge pump. The differential analog signal generated by the charge pump is converted to a single-ended ground-referenced signal by the differential difference block. The output of the differential difference block controls the response time of the chain block, thus closing the loop on the DLL between input and output.

The DLL test chip has 25 pins used for both I/O and observing internal states of the device. The pins essential for controlling the operation of the DLL are the DVCC and VSS pins for power (V_{cc} = 2.5V) and ground, the five SELx pins for selection of the output state of the DLL, the differential input clock CLKIP and CLKIN pins, the CPUMPEN and RESET pins to control starting and stopping, and the differential output OUTP and OUTN pins. The pins for observing the internal state of the DLL are the PBIAS, VCCPS, VCNTRL, VCNTRLP, VCNTRLN, and VREF pins which output analog bias levels, the UP, UPB, DN, and DNB pins monitor the output state of the PFD, and the differential CLKOP and CLKON pins for monitoring the output clock. The functionality of these pins will be elaborated in subsequent pages.

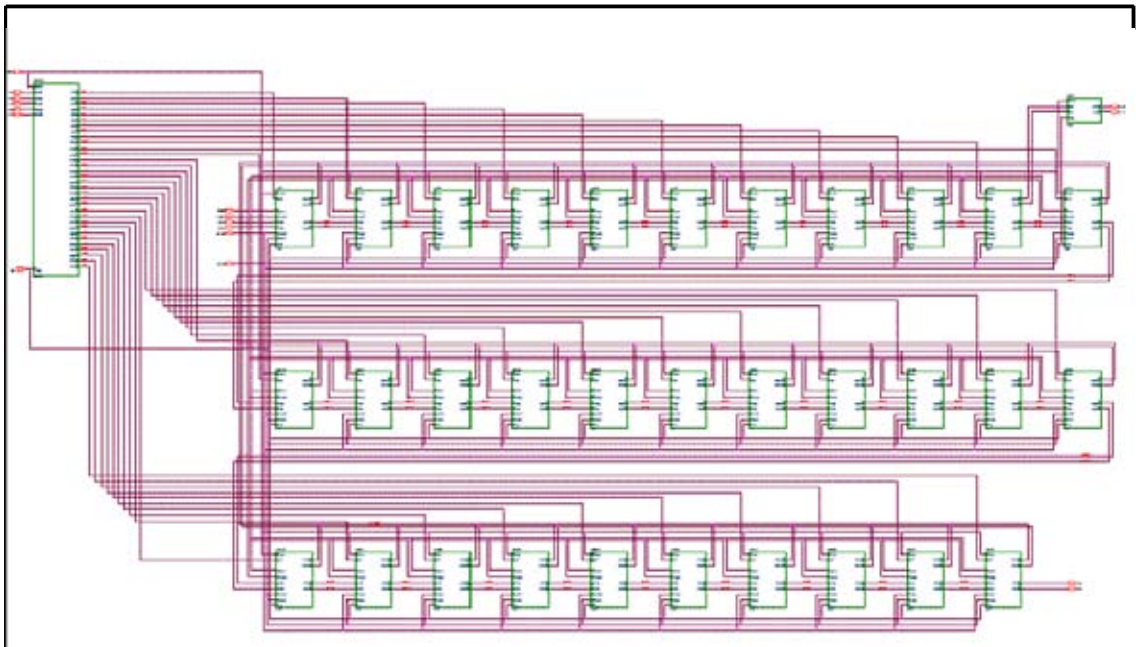

Figure 3: Chain block of the DLL

The heart of the DLL is the chain block (figure 3). It consists of a demultiplexer to decode the 5 bit input selection into 32 control lines, a loop of 32 delay cells referred to as “links” to provide the variable delay, and an output multiplexer to buffer the selected delay line to circuitry outside of the chip. The demultiplexer is a block built using conventional AND and inverter logic cells from the Artisan/IBM standard cell library

(figure 4). It is not required to change output conditions very frequently in normal operation of the DLL, and its 300MHz operating frequency is sufficient for all operating conditions of the DLL.

Figure 4: Demultiplexer sub-block of the chain block

The link sub-block of the chain block is shown in figure 5. It consists of two differential inverters and one multiplexer. The link block is essentially a delay buffer element with a differential input and output. It includes an analog voltage input, VCNTRL, to control the amount of delay and a multiplexer output to serve as a buffer for the tap output of the delay element. The PBIAS and VCCPS lines into the block monitor bias levels fed to each link block. Each differential inverter provides a 180^{o} phase shift along with a variable delay. The effect of two differential inverters in series in the link block is to provide a time delay of 360^{o} plus a variable amount delay. The net effect in a continuous wave (CW) application is that the link block behaves like a variable delay cell. The multiplexer makes the delayed output of each link block available for output selection by the top level multiplexer in the chain block.

The differential inverter portion of the link block is shown in figure 6; this is the diffcell block. The diffcel2 block differs from diffcell only in that the gate of its M1 FET is tied to VCNTRL instead of RESET. The differential inverter has a number of special features and is the most significant circuit in the DLL. The differential inverter is a PMOS-input source-coupled differential amplifier with variable resistance loads as pull-down devices. The two-sided differential gain, A_{DM}, is given by

(1) $$A_{DM} = g_m \cdot R_L$$

where g_m is the PMOS transconductance and R_L is the resistance of the pull-down device. The differential gain determines the switching time and, as a result, the minimum

resolvable step size achievable in a given technology. For a differential PMOS transistor amplifier, the 3 dB response frequency, f_{3dB}, is given by

(2)
$$f_{3dB} = \frac{1}{2\pi\left[R_s\left(C_{gs} + C_{gd}\left(1 + A_{DM}\right)\right)\right]}$$

where R_s is the input resistance, equal to the output resistance of the preceding stage, C_{gs} is the gate-to-source capacitance, and C_{gd} is the gate-to-drain capacitance. This can be approximated as

(3)
$$f_{3dB} \cong \frac{1}{2\pi\left[R_s\left(C_{gd}\left(1 + A_{DM}\right)\right)\right]}$$

This indicates that the minimum delay time of the differential amplifier will be determined by the process and device determined parameters, R_s and C_{gd}, and the controllable differential gain.

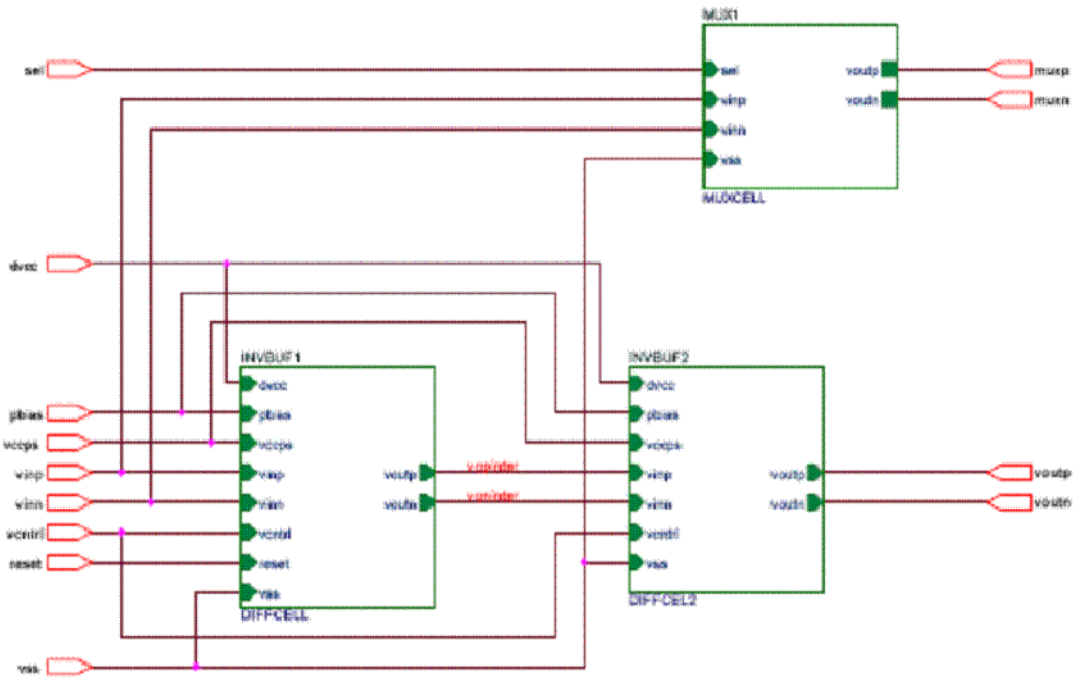

Figure 5: Chain cell "link" consisting of two differential inverters and a mux.

Normally, one would not choose a PMOS input differential pair, as the transconductance of a PMOS transistor is about 1/3 that on an NMOS device in the same technology. This means that the maximum speed of the PMOS differential amplifier will be much slower than a comparable NMOS device. The reason PMOS input pairs were used for the differential amplifiers here was to limit the response of the circuit to power supply-

induced noise. The PMOS input differential amplifier uses a high impedance current source to serve as a resistor to the noisy power supply rail. This current source is provided by a single PMOS device with a source resistor. Its effective input resistance looking into its drain terminal, R_{tail}, is given by

(4) $$R_{tail} = R_{E1} + r_o\left[1 + g_m \cdot R_{E1}\right]$$

Where R_{E1} is the source degeneration resistor, r_o is the output small signal resistance of the PMOS current source device, and g_m is the transconductance of the same device. The transconductance of the PMOS device is given by

(5) $$g_m = \sqrt{2 \cdot k_p^{'} \cdot \frac{W}{L} \cdot I_D}$$

Where $k_p^{'}$ is the process specific hole mobility multiplied by gate oxide capacitance ($k_p^{'} = \mu_n C_{ox} = -50\mu A/V^2$ for the IBM 8RF/DM process PMOS), W is the device width, L is the device length, and I_D (= 200µA) is the DC drain current. For this device, g_m is about 4.1 mS. The small signal output resistance is given by

(6) $$r_o = \frac{1}{\lambda \cdot I_D}$$

For this device, r_o is about 140 kΩ, and the resulting R_{tail} is about 570 kΩ. Using this current source PMOS device to the V_{cc} rail greatly reduces noise that can otherwise couple in from the V_{cc} rail and contribute to phase noise in the DLL.

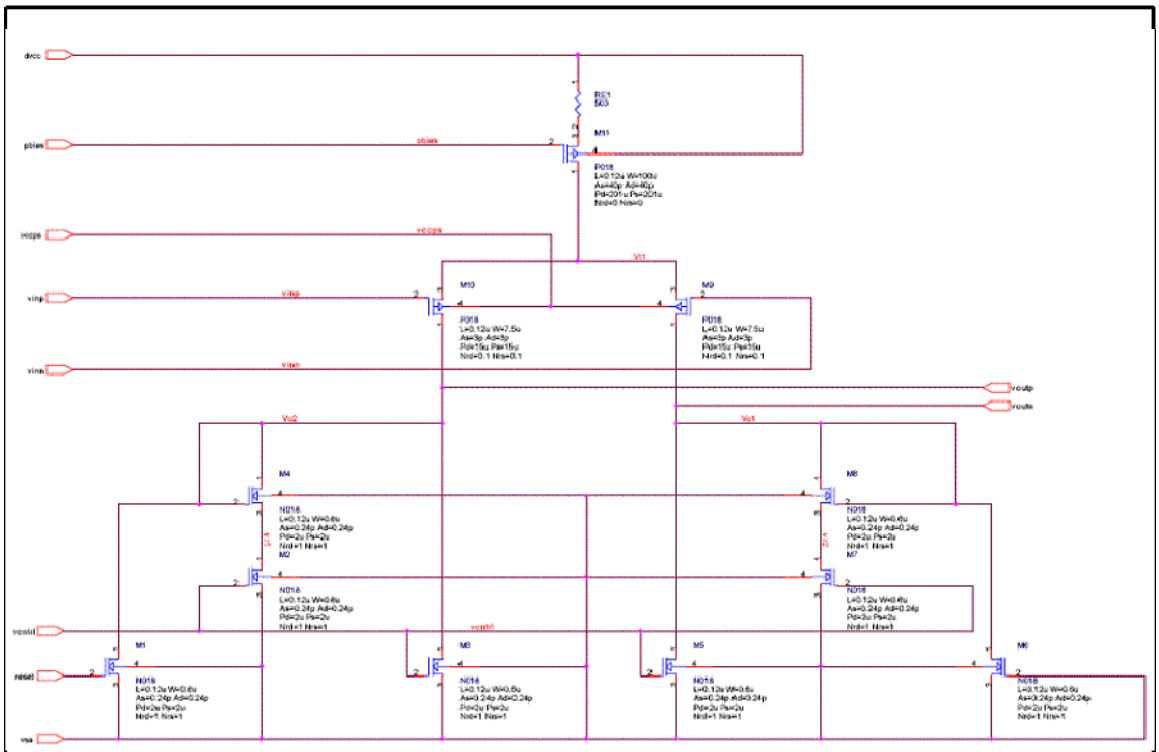

Figure 6: Diffcell inverter element of the link block

Another innovative aspect of the differential inverter block is the voltage variable resistor load used to provide R_L. The voltage variable resistor is provided by the parallel combination of an NMOS device in saturation and another NMOS device operating in the linear or triode region. A third NMOS device is used to provide a positive bias to the source of the saturated NMOS device's source. The resulting circuit provides a linear resistance over a voltage range from zero to over 2.5V [2].

The linear resistor is a parallel combination of an NMOS device in saturation and another NMOS device in the triode region of operation. The drain current of the NMOS device in saturation can be written as

$$I_{D2} = \frac{k'}{2}\left(\frac{W}{L}\right)\left[V_{GS2} - V_t\right]^2 \tag{7}$$

And the drain current of the NMOS device operating in the triode region can be written as

$$I_{D1} = k'\frac{W}{L}\left[\left(V_{GS1} - V_t\right)V_D - \tfrac{1}{2}V_D^2\right] \tag{8}$$

with V_{GS1} and V_{GS2} representing the respective device gate-to-source voltages, V_t representing the approximately equal threshold voltage for each device, and V_D is the triode device drain voltage. The input node, V_{IN} shown in the schematic of figure 6 as V_{c1} or V_{c2}, of this resistor can be replaced by

$$V_{IN} = V_D = V_{GS2} - V_{N1} \tag{9}$$

with V_{N1} representing the node voltage of the drain of the bias NMOS device added below the saturated NMOS device. The combined current can of these two devices is the parallel combination of the two drain currents, after equating the voltages in (9) and applying the requisite algebra:

$$I_{IN}\left(V_{IN}\right) = I_{D1} + I_{D2} \tag{10}$$

This current versus voltage relationship is plotted in figure 7. The parallel combination of the nonlinear red and blue lines produces the approximately linear green line. The slope of this line represents the input resistance to the load of the differential amplifiers that comprise the link block of the delay chain in the DLL. The significance of the linearity of these load resistors stems from equation (1) above. The R_L referred to in that equation is the I_{IN} versus V_{IN} response of figure 7. A linear R_L will also result in a linear gain response at large signal voltage levels. While such a high degree of linearity is not needed to provide basic functionality for the DLL, the wide operating range of such a load resistor is important for low voltage operations that need to make use of as much of the available supply voltage as possible. As an interesting aside, one should note that the oscillator formed by the differential amplifiers shown in figure 6 will also provide low harmonic distortion output. This is not a requirement for the DLL in its present application, but such a feature could be an advantage in possible future applications.

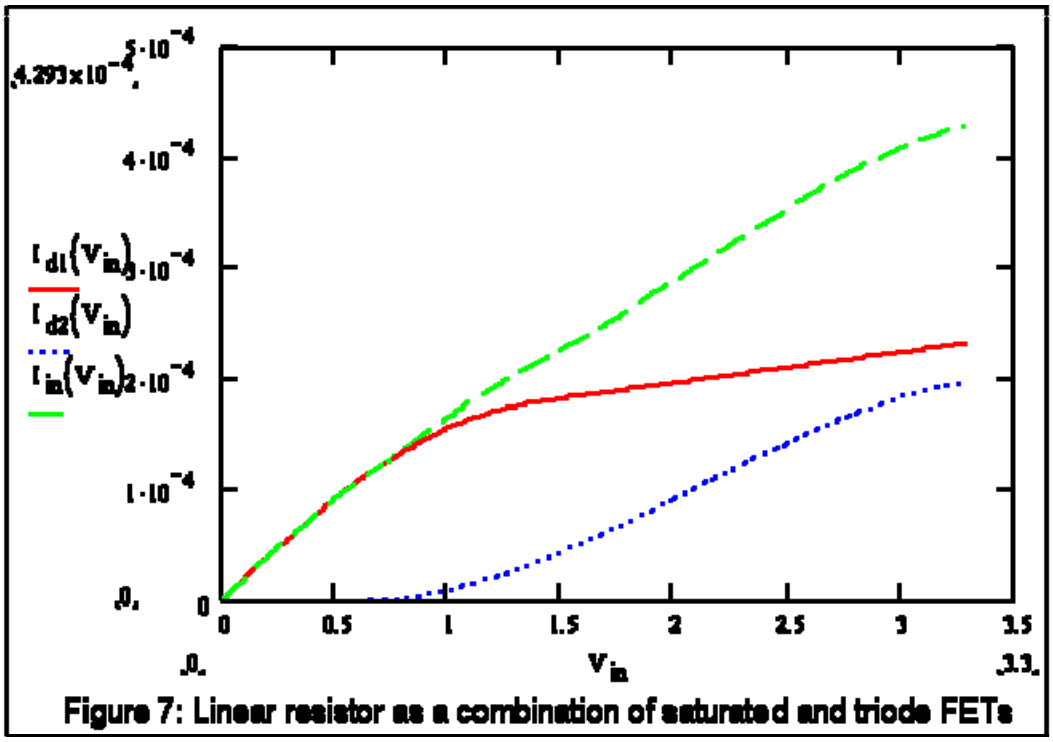

Figure 7: Linear resistor as a combination of saturated and triode FETs

The multiplexer for the DLL is a distributed structure consisting of 32 sub-elements, one in each link block, and a top level multiplexer in the chain block. The muxcell block used in the link block is shown in figure 8. This is the block used to connect between the 32 wire-OR connected link multiplexers and any circuitry outside of the DLL. The cmux block used in the chain block is shown in figure 9. This is the block that is replicated 32 times in each delay block of the DLL. It serves as a differential transmission gate to tap each output delay element out to the top-level muxcell and out of the DLL.

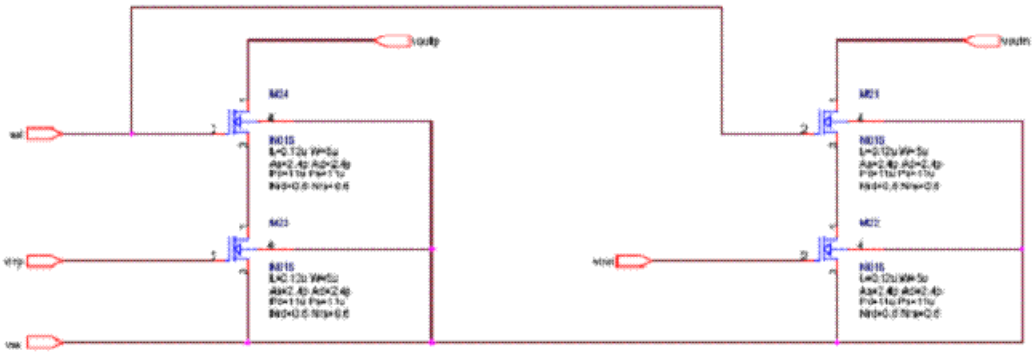

Figure 8: Muxcell element of the link block

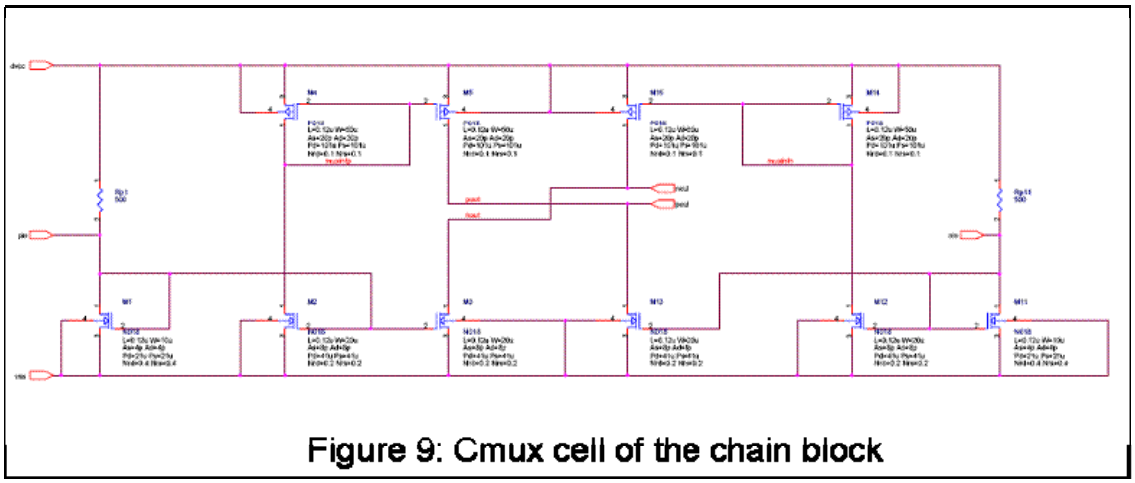

Figure 9: Cmux cell of the chain block

The phase-frequency detector (PFD) is shown in figure 10. It is a standard type single-ended PFD implemented using Artisan/IBM standard cells, 2-, 3-, and 4-input NAND gates and inverters. The PFD output signal depends not only on feedback clock phase error relative to the input clock, but it also has a dependence on frequency error. The PFD is built from two NAND latches, whose outputs are designated as “up” or “down”. The PFD can be in any of four different states, with the “up” or “down” outputs either in a 0 or 1 state. However, the state (up=1 and down=1) is disallowed by the 4-input NAND in the heart of the PFD. For the remaining states, (up=1 and down=0) drives the charge pump to increase loop speed, (up=0 and down=1) drives the charge pump to decrease loop speed, and (up=0 and down=0) idles the charge pump.

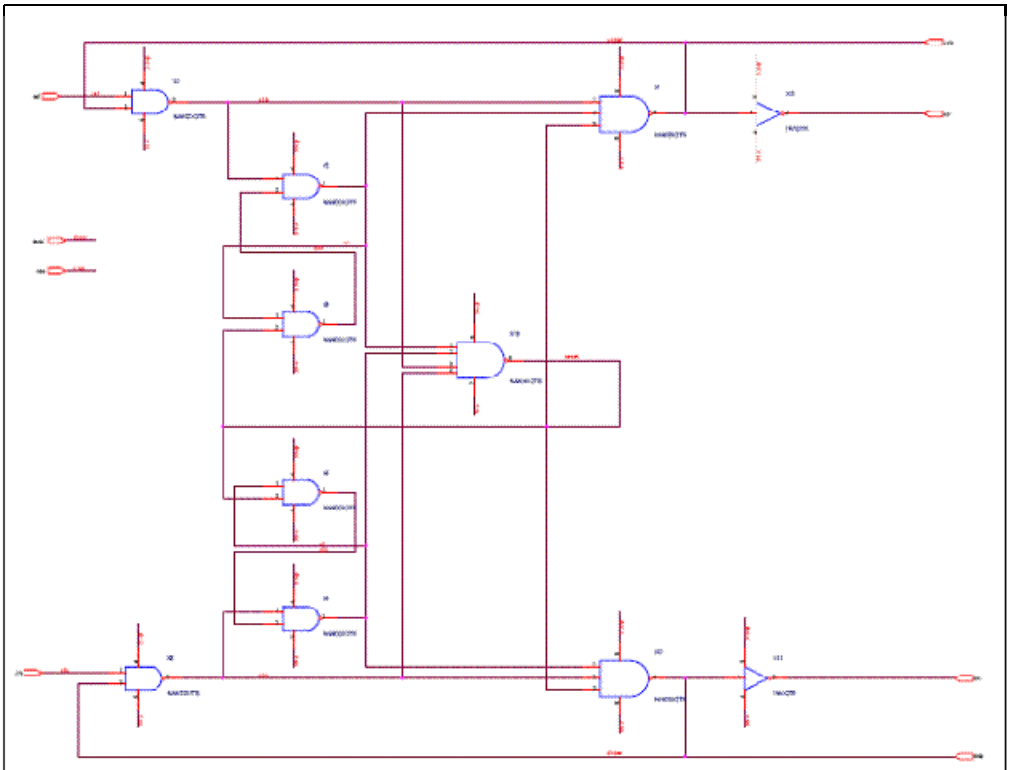

Figure 10: Phase-frequency detector

The charge pump is shown in figure 11. The purpose of the charge pump is to convert the digital commands from the PFD into a voltage across a differential capacitor. This voltage is then converted into a single-ended drive signal by the dual differential amplifier (DDA). The charge pump consists of two mirrored half circuits. It has a dual differential input for both up and down commands. Each command is handled by a separate differential amplifier. Each differential amplifier, in turn, drives a cross coupled current mirror structure. The output drive circuit is a differential current mirror capable of sourcing or sinking current from either side. Maximum drive current out of either side of the charge pump is about 25 µA for V_{cc} = 1.5V or 100 µA for V_{cc} = 2.5V. The filter capacitor that is differentially driven by the output of the charge pump is 22 pF. The time constant of the combined charge pump/filter is about 1 µsec at V_{cc} = 1.5V and about 250 nsec at V_{cc} = 2.5V. This translates into about 80 psec of timing jitter, the inverse of phase noise, for V_{cc} = 2.5V.

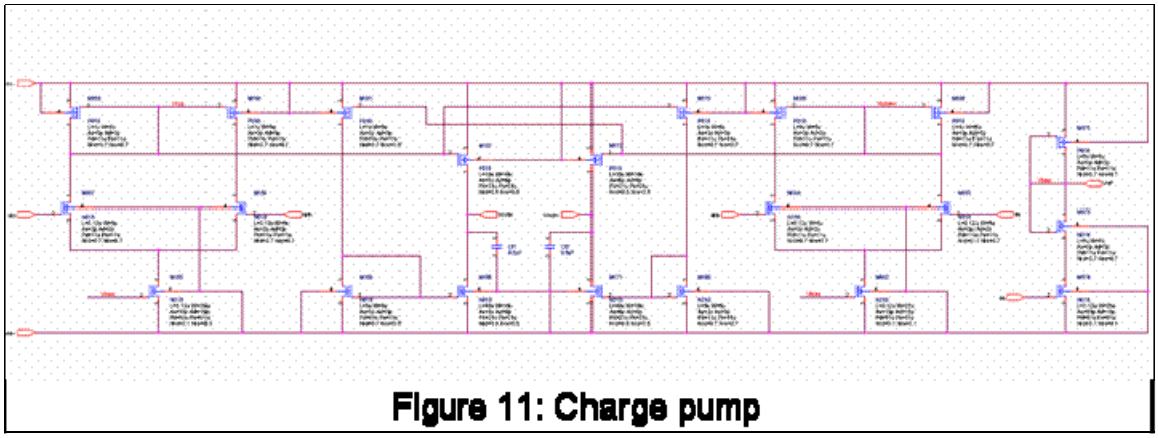

Figure 11: Charge pump

The filter capacitor ties into the differential input of the dual differential amplifier (DDA). The DDA is a rail-to-rail dual differential input and dual differential output operational amplifier capable of running at 1.5V (figure 12). The DDA uses a pair of differential amplifiers for each differential input pair. Each differential amplifier uses a quad input consisting of a two pairs each of matched NMOS and PMOS devices. The two differential amplifiers tie into a 10 transistor cascode stack of current mirror pairs. Each stack contains 4 each NMOS and PMOS devices in cascoded current mirrors. The cascoded current mirrors are separated by matched NMOS/PMOS pairs to provide bias levels in the current mirrors. Each current mirror draws about 9 µA of quiescent current, while each input device draws about 8 µA of current (at V_{cc} = 1.5V). The entire DDA consumes about 240 µA of quiescent current at V_{cc} = 1.5V. The entire block can be switched off via an enable line. This is a feature both to conserve power and to enable quiescent drain current (IDDQ) testing, a chip testing methodology for locating defective components within an IC.

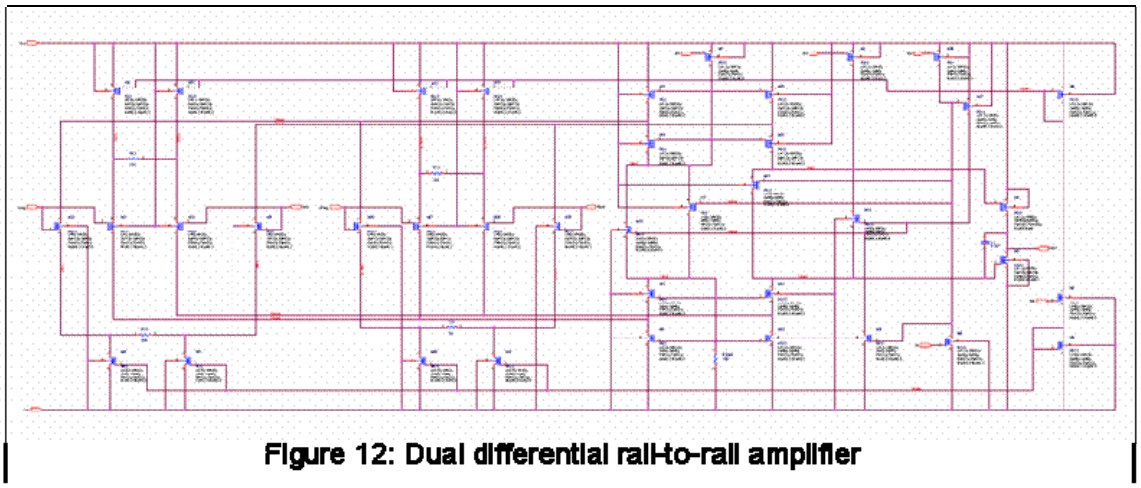

Figure 12: Dual differential rail-to-rail amplifier

The DDA converts the floating, differentially driven filter capacitor into a single-ended, ground referenced voltage for the loop delay time control. This voltage, VCNTL, needs to be able to extend to nearly the V_{cc} rail in order to pull the loop to its minimum response time.

The complete DLL test chip is shown in figure 13. Physical design for this chip used mostly custom cells created at Sandia National Laboratories. The pads were IBM intellectual property (IP) used under license from IBM. In addition, the standard cells used for the demultiplexer and PFD were IBM/Artisan IP. All other blocks were custom designed and drawn at Sandia National Laboratories and constitute Sandia IP.

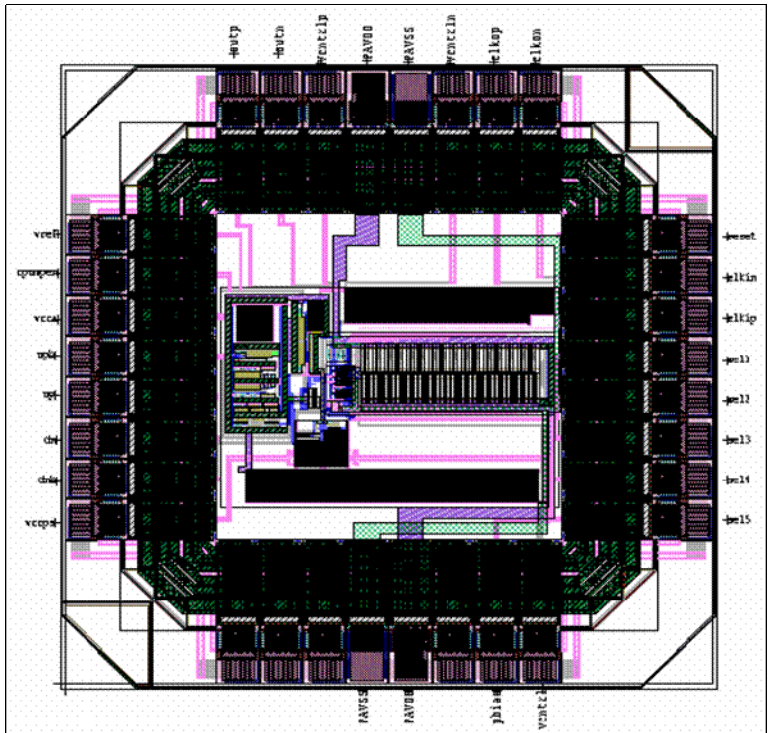

Figure 13: DLL test chip layout with ports

Testing: Probe Testing

Initially, the DLL test chip was tested as a packaged component on a custom printed circuit board (PCB) designed for that purpose. The test results were dominated by parasitic capacitances introduced by the PCB, so an attempt was made at probe testing the DLL directly. Probe testing attempts were hampered by the number of probes required and by the requirement to control impedances to 50 Ω to many of the ports on the part. The optimal approach to testing the DLL appeared to be a combination of printed circuit board technology for DC or low frequency signals, with either probes or short, low parasitic traces on the high speed lines.

A prototype for performing this type of testing of the DLL was made using the test configuration shown in figures 14 and 15. This was an effort to overcome previous probe-driven testing limitations. In previous testing, DLL performance was limited by both the need to input and measure differential signals and by the very limited output drive capability of the DLL. The DLL was created as a fully differential design in order to satisfy the power supply rejection and phase noise requirements. In previous testing, single-ended signals were used both to drive and to measure the DLL. Testing with single ended signals left unanswered questions about the input drive and phase requirements. In the configuration shown in figure 15, the DLL is assembled on a metal plate with 50Ω transmission lines cut from pre-fabricated forms and epoxied into place as differential lines. This enables probe testing using differential GSSG 200 micron probes.

This configuration gives better control over signals routed to and from the test board, since it preserves the differential nature of the DLL signals up to the board. However, it still leaves both the test chip input and output unbuffered. The DLL input is CMOS and does not present a 50Ω input impedance to the pulse generator. Also, the output of the DLL is unbuffered and is designed for driving a CMOS on-chip load. It is not capable of driving a typical 50Ω oscilloscope input, and most 1MΩ oscilloscope inputs have excessive input capacitance, typically 12-20pF. To overcome the output drive limitations, a FET probe (C_{in}=1.7pF) in conjunction with a Tektronix TDS540 oscilloscope was used. This helps to buffer the output but still results in some rolloff.

The output multiplexer stage of the DLL is shown in figure 16. The effective channel resistance of the output stage is given by

(11)
$$R_{chan} = \frac{1}{\mu \cdot C_{ox} \cdot W/L \cdot (V_{GS} - V_t)}$$

For a "short" format device in the IBM 8RF process, $V_{tN} = |V_{tP}| = 0.42V$, $\mu C_{oxN} = 550\mu A/V^2$, $\mu C_{oxP} = -100\mu A/V^2$. For the output stage in the process of transition, $V_{GS} = 0.75V$, $W_N/L_N = 154$, and $W_P/L_P = 385$. Using these values gives $R_N = 36\Omega$ and $R_P = 79\Omega$ in the center of the output transition band. Using an averaged value of output resistance indicates that the best case measurement bandwidth is 140MHz using a 20pF measurement system. Using a 3pF (1.7pF probe plus 1.3pF parasitic) measurement system gives a best case measurement bandwidth of 923MHz, but this is limited to a range of only a few hundred millivolts centered around 0.75v due to the highly nonlinear

nature of the channel resistance. The preferred solution is to buffer the output of the DLL before measurement or transmission.

A similar problem exists at the input to the DLL. The DLL has a standard CMOS input, while most high speed variable output level pulse generators are designed to interface to a 50Ω load. The result is that the input of the DLL test chip can be driven with an unknown voltage even though the pulse generator output has been measured by an oscilloscope. The DLL chip input is greater than 50Ω but less than 1MΩ. As a consequence, it is difficult to know what voltage the input to the DLL is actually seeing in the configuration shown in figures 14 and 15. The preferred solution is to shunt the input of the DLL with load resistors sized to render an effective 50Ω input impedance.

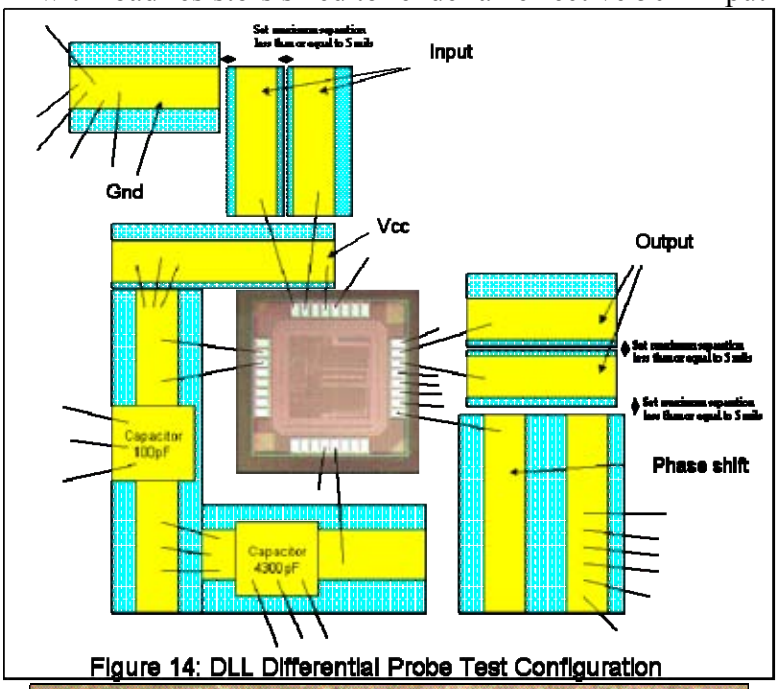

Figure 14: DLL Differential Probe Test Configuration

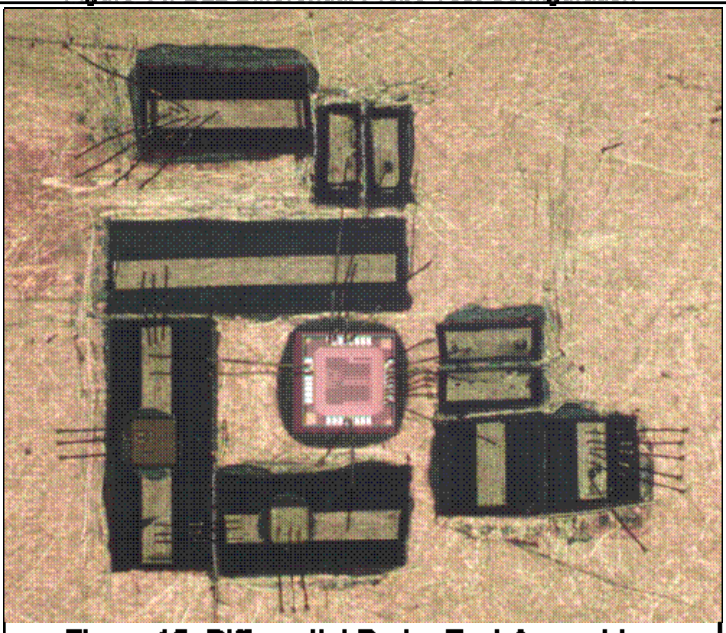

Figure 15: Differential Probe Test Assembly

Testing using this configuration resulted in interesting but incomplete results. The degree of phase shift of the DLL is a measure of the number of wave phases contained in its delay loop. The correct number of degrees is 360, indicating that the DLL has 32, 104 psec steps available at its output. Using the configuration in figures 14 and 15, the output exhibited switchable phase shifts, indicating that the device was operating correctly in 360^o mode at V_{cc} = 1.5V. In addition, it was possible to force the device into an incorrect 720^o mode by inducing a phase shift other than 180^o between the differential input signals. It was also possible to completely prevent the device from operating by applying an excessive differential phase shift to the inputs. Output voltage swings were limited to less than 300mV, as expected from the above analysis of the output loading effects. After a fairly brief test episode, the test article shown in figure 2 was damaged, apparently by an over-voltage condition at the input pins. This over-voltage condition arose from the inability to control or even measure the input signal amplitude as seen by the chip. During the test, the chip appeared at times to be receiving part of its DC power parasitically from the input signal rather than from the power supply. This was apparent from current fluctuations visible on the DC power supply.

In conclusion, the test results using the configuration of figures 14 and 15 indicated the possibility that the DLL could be brought into a correct 360^o operating state by applying the right input signal conditions. The results were inconclusive, because the DC operating voltage and the input signal amplitude both could not be reliably determined. It was possible, even likely, that the part was operating at a much higher voltage than 1.5V. In order to decisively answer these questions, a test board was needed with differential input and output, 50Ω input shunt loads to match to the pulse generator, and a differential on-board buffer to drive a 50Ω measurement instrument.

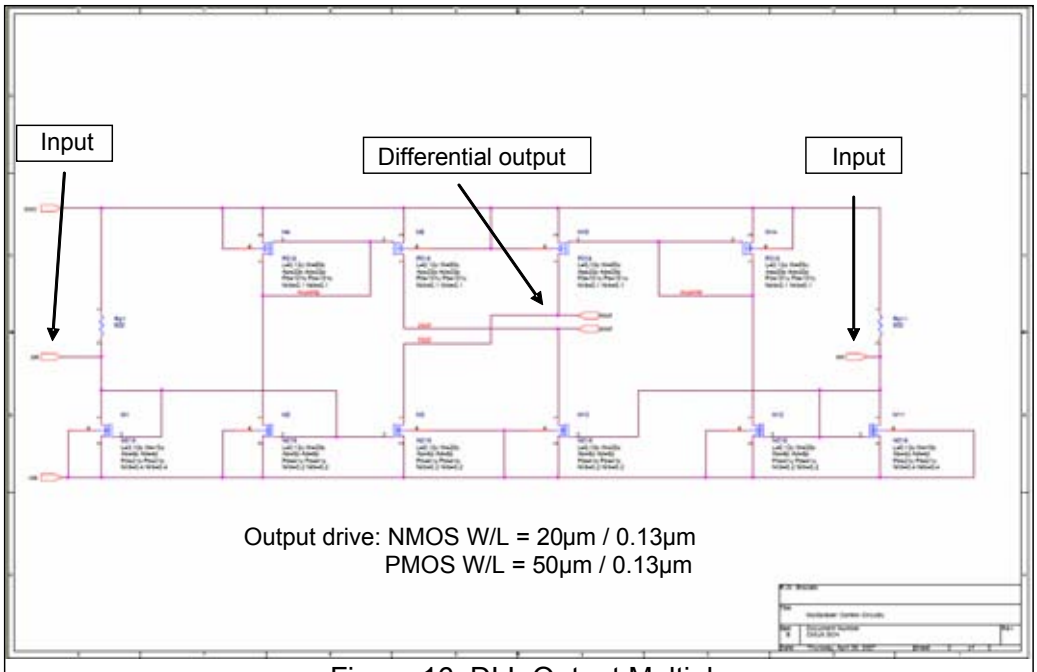

Figure 16: DLL Output Multiplexer

Testing: PCB Testing

The solve the problems of simultaneously making numerous connections to the DLL die, providing a differential buffer to the output, and controlling the impedance to the input, the test PCB in figure 17 was developed. It combines surface-mount packaged component mounting along with chip-and-wire mounting of the DLL die to eliminate package parasitics. All input/output (I/O) to and from the board are conducted by SMA connectors. The delay switch settings are controlled via an on-board switch block. The output signals are buffered by a 74AHC04 CMOS inverter block. Input and output signals are both available as differential signals. Test signals can be brought as controlled impedances to the board via coaxial cables (figure 18).

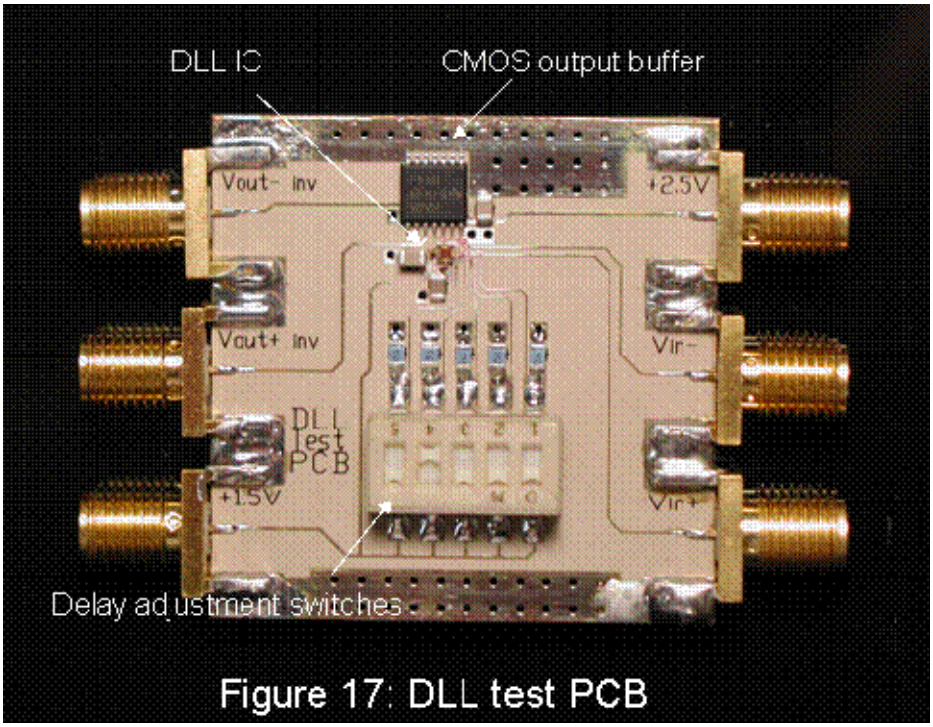

Figure 17: DLL test PCB

The DLL was tested with a variety of different signal and voltage conditions. Optimum operation of the chip was obtained for V_{cc} = 2.5V, the voltage that is used for I/O circuitry in the QDWS chip. At this power supply voltage and with V_{supply_AHC04} = 3.6V, the output voltage from the AHC04 buffers was measured to swing from 0 to 1.5V. The DLL was differentially driven from an HP8131A Pulse Generator. The input signal conditions and skew were adjusted and measured separately to guarantee 180^{o} of phase difference between the two input signals and an input signal that extended from ground to V_{cc}. The output signal from the AHC04 buffers was measured using a Tektronix TDS540 oscilloscope with 1.7 pF of input capacitance per channel. The DLL was tested from V_{cc} = 1.5V to V_{cc} = 2.9V. At V_{cc} = 2.5V, the DLL consumes 53.5 mA of current for a total power consumption of 134 mW.

The DLL was found to require a supply voltage level that is greater than the 1.5V core supply voltage to provide adequate output drive levels to ensure valid test results. Output

voltage swing at V_{cc} = 1.5V was only about 200 mV at the input to the oscilloscope. This is inadequate to guarantee proper operation of the DLL at that voltage. Recall that the output of the DLL drives a pair of short PCB traces and the input to the pair of AHC04 inverters. This load is estimated to include about 3 pF of parasitic capacitance. This load is considerably larger than any on-chip load that the DLL will see when embedded in the QDWS ASIC. So, while the DLL may function perfectly well at V_{cc} = 1.5V, it is not possible to verify this. The conclusion is that the DLL must be operated at V_{cc} = 2.5V to ensure proper operation.

A key question to consider in testing was whether the DLL operates with a single 360^o phase within its delay loop, or whether its loop contains a multiple of 360^o. If the loop locks to a multiple of 360^o, the loop will be operating in a slower mode than needed to properly track the input signal and each output step will consist of some multiple (2,3,4…) of 104 psec rather than the minimum step of 104 psec.

The photo sequence shown in figure 19 shows a sequence of tests conducted at V_{cc} = 2.5V with varying degrees of delay introduced between the input and the output. Each snapshot shows a test event in which the input signal is displayed on the top oscilloscope trace, and the DLL output signal is displayed on the bottom oscilloscope trace. The oscilloscope is triggered on the input waveform, so this provides the fiducial point to measure time delays against. The bottom image shows the input versus output signals with no time delay introduced into the DLL. The center image shows the input versus output signals with an 8 step time delay introduced. The 8 step delay should provide a retrograde time movement of the output of about 832 psec. If the DLL were operating at a higher order multiple of phase, the delay would be at least double this amount, 1660 psec. The top image shows the input versus the output signals with a 16 step time delay introduced. The 16 step time delay should provide a retrograde time movement of the output of about 1.66 nsec. Again, if the DLL were operating at a higher order multiple of phase, the delay would be at least double this amount, 3.32 nsec. Further tests, not shown, with a delay of 31 steps show the output brought within 104 psec of the original starting position. These tests verify the correct operation of the DLL when it is operated with the proper input signals and at an adequate supply voltage.

The series of tests shown in figure 19 were repeated at a variety of operating voltages and input frequencies. The DLL was successfully tested with supply voltages ranging from V_{cc} = 2.2V to V_{cc} = 2.9V. The DLL was also tested at lower operating voltages, but the limited size of the output voltage swing limits the reliability of those test data, as discussed above. The DLL was tested from 200 MHz to 500 MHz, with primary interest on the 300 MHz operating conditions of the requirements. Initial evaluation work with the DLL packaged and mounted on a low frequency qualified PCB demonstrated that the DLL could function as low as 1 MHz. However, these tests were not exhaustive, and if there is any subsequent interest in pursuing low frequency operation with the DLL, thorough testing should be undertaken using the test PCB shown in figure 17.

Startup and initial lock time measurements of the DLL were performed using the packaged version of the DLL. The power supply settling time was observed to be about

13 msec. The settling and initial lock times for the DLL were coincident with the power supply settling. The DLL appeared to become active and to settle within about a 3 msec time period, after the supply voltage rose above 1.0V. However, the DLL settling time measurement was limited by the speed with which the power supply would settle. It may be that the DLL settles in less than 3 msec, if the power supply were also to settle more quickly. Further testing will be required, if this settling time is deemed to be inadequate. Otherwise, one may safely conclude that the DLL startup time is not more than 3 msec after the supply voltage reaches at least 1.0V.

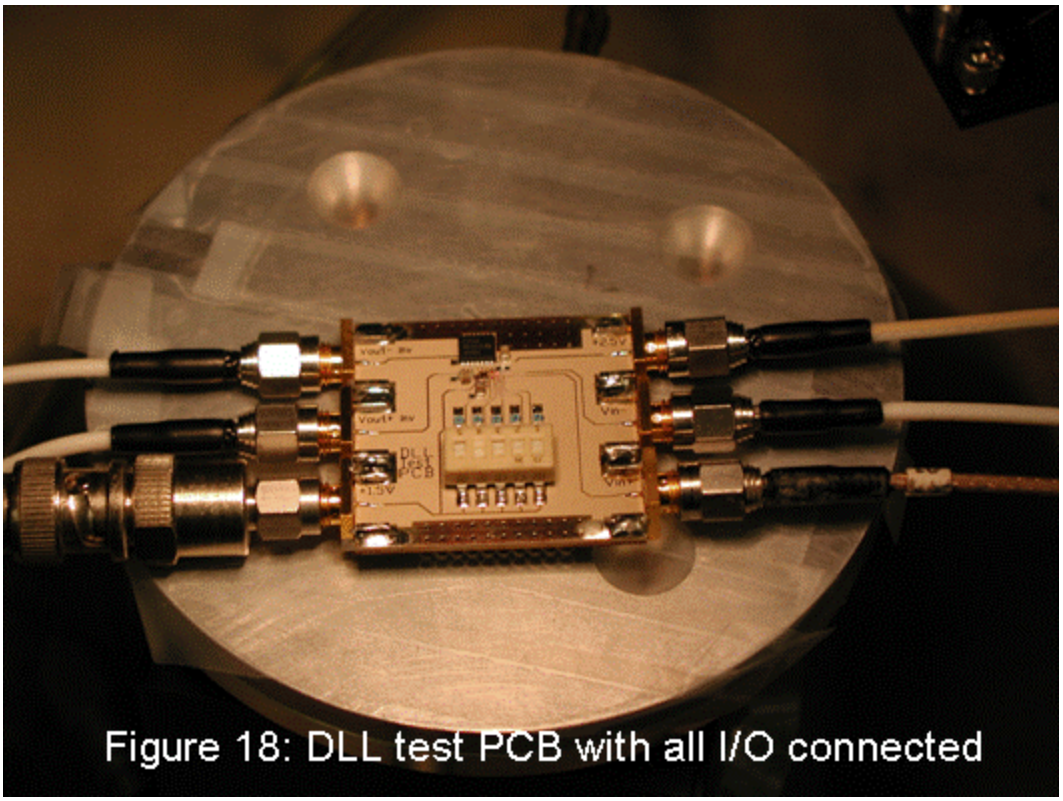

Figure 18: DLL test PCB with all I/O connected

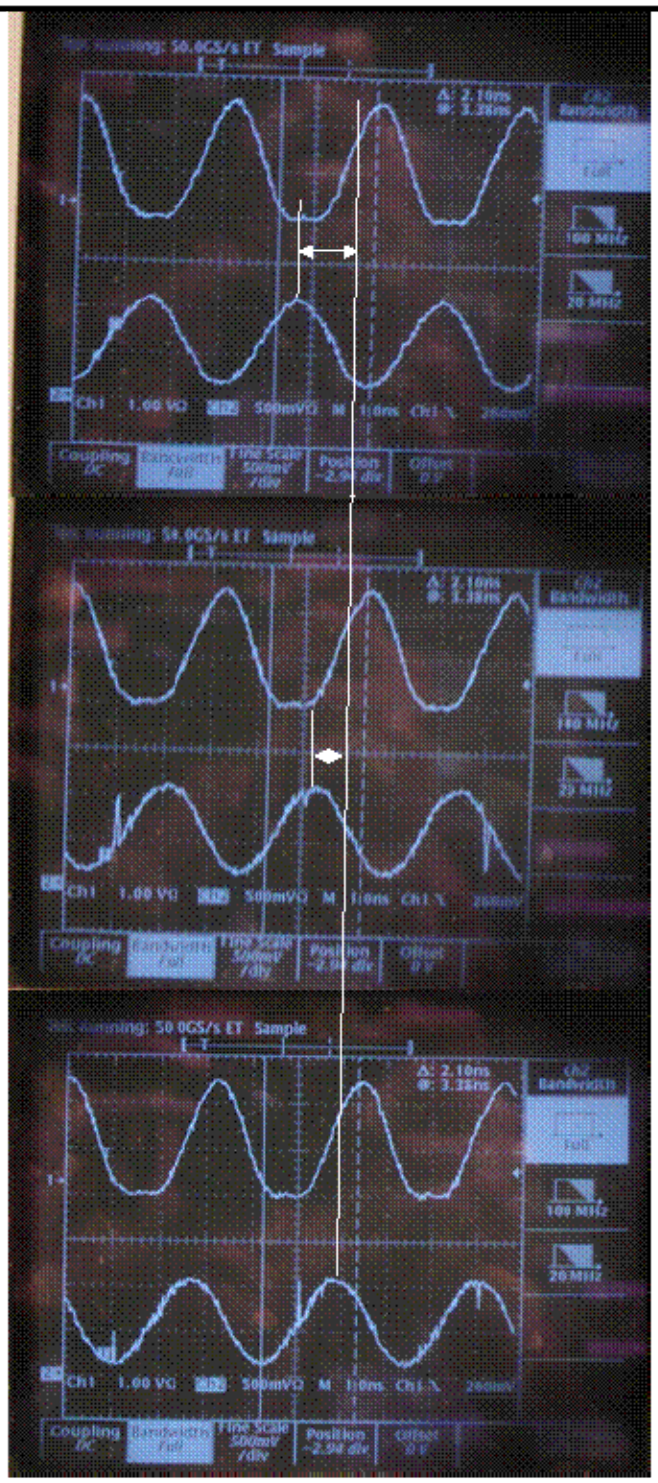

Figure 19: DLL test sequence of time delayed signals

Conclusion

A delay locked loop test chip, suitable for integration into a larger ASIC, was successfully designed, fabricated, and tested by the author, and test results were verified while in progress by a number of observers. The DLL test chip was fabricated in the IBM 8RF 0.13 µm CMOS process. The DLL provides a 32 step variable time delay that can track an input clock over a wide input range. The design could be easily ported to another process. The DLL was shown to be susceptible to improper test or usage conditions. However, when operated as a fully differential device with adequate supply voltage and output buffering, the DLL was shown to operate exactly as required.

References

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2) I.A. Young, J.K Greason, and K.L. Wong "A PLL Clock Generator with 5 to 110MHz of Lock Range for Microprocessors", *IEEE J. Solid State Circuits,* vol. 27, no. 11, pp1599-1607, Nov. 1992.

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