SANDIA REPORT

SAND2005-0052
Unlimited Release
Printed January, 2005

Si-Based RF MEMS Components

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Abstract

Radio frequency microelectromechanical systems (RF MEMS) are an enabling technology for next-generation communications and radar systems in both military and commercial sectors. RF MEMS-based reconfigurable circuits outperform solid-state circuits in terms of insertion loss, linearity, and static power consumption and are advantageous in applications where high signal power and nanosecond switching speeds are not required. We have demonstrated a number of RF MEMS switches on high-resistivity silicon (high-R Si) that were fabricated by leveraging the volume manufacturing processes available in the Microelectronics Development Laboratory (MDL), a Class-1, radiation-hardened CMOS manufacturing facility. We describe novel tungsten and aluminum-based processes, and present results of switches developed in each of these processes. Series and shunt ohmic switches and shunt capacitive switches were successfully demonstrated. The implications of fabricating on high-R Si and suggested future directions for developing low-loss RF MEMS-based circuits are also discussed.

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1.0 Introduction

Presently, there is a need for compact, high performance microwave switches with lower loss and lower static power dissipation than solid-state switches to enable miniaturization of high-performance microwave circuits. As systems move to higher operating frequencies and become more compact, the performance and power dissipation requirements become more stringent. High performance in the form of low signal loss circuits will be required to reduce the number of amplifiers and the noise figure in microwave circuits. Low static power dissipation microwave circuits will be required to minimize heat dissipation that becomes an increasing problem in smaller volume circuits. Solid-state switches are highly integrable and have switching speeds under 10ns, however they have higher static power dissipation and insertion loss, lower linearity, and are narrow band compared to RF MEMS switches [1-8]. The benefits of RF MEMS ohmic and capacitive switches in terms of static power dissipation, insertion loss, linearity, and bandwidth enable low-loss circuits such as phase shifters [9], tunable filters [10-14] and networks, and reconfigurable antennas for applications in miniaturized synthetic aperture radar, satellite communications, portable ground-based communications, miniaturized transceivers for autonomous sensor arrays, and RF tags. Switch insertion loss and isolation of 0.1 dB and 30 dB, respectively, from 0-40 GHz have been demonstrated [7]. W-band operation has also been demonstrated [15] and cycle lifetimes are presently approaching 100 billion cold switching cycles [16].

A large body of work in the field of RF MEMS is focused on low-temperature surface micromachining processing techniques of switches and switched circuits which is motivated by higher levels of electronics integration, the flexibility to perform substrate-independent processing, and by the limited materials set required to fabricate high-performance microwave circuits at high frequencies. Monolithic integration of RF MEMS devices with high-speed electronics has been demonstrated by combining RF MEMS ohmic switches with gallium arsenide (GaAs) active devices to make a switched amplifier [17]. The potential also exists to post-process RF MEMS devices on microwave circuits from monolithic microwave integrated circuit (MMIC) foundries. In another example, polysilicon (polySi) germanium microstructures were post-processed on CMOS electronics [18]. Substrate-independent processes are advantageous because only one process needs to be developed and optimized for a variety of applications. RF MEMS devices have been fabricated on semi-insulating (SI) and epitaxial GaAs, high-resistivity silicon (high-R Si), and quartz [7] substrates. Low-temperature processing is also driven by the materials constraint that is required for high-performance microwave circuits. High-conductivity metals and ideal insulators are preferred, which is readily compatible with low-temperature deposition processes such as metal sputtering and electroplating and insulator deposition by plasma enhanced chemical vapor deposition (PECVD). These films are also compatible with organic sacrificial layers.

In addition to low-temperature processing strategies, a number of references are available on the fabrication of RF MEMS components and circuits in Si CMOS or CMOS-like fabrication facilities. Examples include the fabrication of switches [19-21], micromachined passives [22], and mechanically resonating devices [23,24]. There are a number of compelling reasons that make fabrication in a CMOS or CMOS-like electronics facility advantageous. First, although the materials set in a CMOS facility is limited, high conductivity materials such as Al are available to develop low-loss transmission lines and mechanical structures. Equally as important is the availability of compatible sacrificial films that have a high degree of etch selectivity. Second, 6”

diameter high-R Si is readily available for processing low-loss microwave circuits in Si fabs. Third, although high-R Si is more expensive than starting materials for CMOS processing, the capability to volume manufacture reconfigurable circuits drives costs down. Fourth, there is motivation to fabricate certain micromachined structures on standard CMOS starting material for monolithic integration with CMOS circuitry for wireless applications. The fifth reason is Sandia-specific: the MDL has more than a decade of experience in processing polySi surface micromachining and the design infrastructure for complex MEMS devices that is directly transferable to the design of RF MEMS devices with novel processes.

In this work we demonstrate a variety of processes and switches for use in low-loss RF MEMS circuits. All processing is performed in the MDL; a radiation hardened CMOS facility at Sandia National Laboratories. New processes that use molded W are explored to fabricate transmission lines and switches. Novel Al surface micromachining processes are also used to develop switches. The devices, processes, and measurements are discussed in this work, and conclusions are drawn about the fabricated components and about future direction and needs for fabricating high-performance switches and circuits in the MDL.

2.0 Si as a Microwave Material

2.1 Planar Transmission Line Technology

Planar transmission lines have higher losses than waveguides, however for applications requiring high levels of integration such as with monolithic microwave integrated circuits, this is often the technology of choice. Planar technologies are compatible with integrated circuit processes because they require only planar signal and ground lines to define fixed-impedance transmission lines. Since one of the primary goals of many RF MEMS programs is the development of electronics-compatible processes in order to achieve the highest levels of microwave system miniaturization and functionality, this technology is an obvious choice. It is very difficult to effectively integrate RF MEMS devices with waveguides, due to the fact that they are non-planar, although such a scheme would result in unprecedented reconfigurability and performance.

Three important transmission line technologies are symmetric co-planar waveguides (CPW's), microstrip (MS) transmission lines, and stripline transmission lines, as shown in Figure 2.1. CPW transmission lines consist of a signal line surrounded on each side by two ground lines. Electromagnetic fields and currents are confined to the inside edges of the metal lines on either side of the two slots between the signal and ground lines. The proportion of electromagnetic field energy traveling above vs. below the metal lines depends on the relative values of the upper and lower dielectrics. In the case of RF MEMS, the upper dielectric is almost always air to allow for free-standing, movable mechanical structures. The transmission line inductance is varied by changing both the signal line width and the signal line-to-ground line gap, and the capacitance is changed by varying the signal line-to-ground line gap.

From our perspective, the primary advantage of CPW lines is that they are easy to fabricate. No vias are required and 50 transmission lines are easily fabricated on variable thickness substrates. This makes them very popular in RF MEMS academic research because the start-up time is minimal; a philosophy that we have also employed to more rapidly demonstrate a variety of switches and processes. Unfortunately, because most of the electromagnetic energy is confined to the inside edges of the metal lines, the effective resistance of CPW's is higher than

either MS or stripline transmission lines. Consequently, the attenuation per-unit-length is high and leads to low-Q microwave circuits such as filters. CPW transmission lines are also less well understood than microstrip transmission lines. Corners and bends are problematic in terms of unwanted modes and grounding bridges are required to reduce these affects. CPW's suffice for demonstration purposes but one of the other two technologies will ultimately be required to obtain high performance. Figure 2.2 shows the metal-loss attenuation for a reasonable geometry of 50 CPW transmission lines on an alumina substrate ($_r$ = 9.8).

MS transmission lines consist of a signal line on the topside of the substrate and a ground plane on the backside of the substrate (Figure 2.1, center image). Most electromagnetic energy is confined to the gap between the signal line and the ground plane, especially when there is a large difference in dielectric constants between the regions above and below the signal line. However, significant electromagnetic energy is contained in the air above the signal lines due to fringing and is responsible for dispersion. The transmission line inductance is determined by the signal line width and the capacitance is determined by both the signal line width and the thickness of the substrate between the signal line and the ground plane.

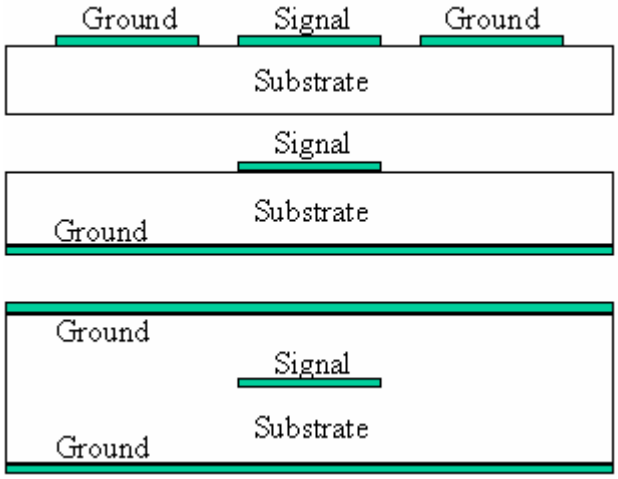


Figure 2.1: Co-planar waveguide, microstrip, and stripline transmission lines.

MS transmission lines have less loss than CPW transmission lines. The distribution of the EM energy under the signal line means that the associated current in the signal line is spread out over the length of its bottom side, effectively decreasing the series resistance over that of CPW lines. Corners and bends in MS lines are less problematic partly because they are better understood than CPW lines and grounding bridges are not required. MS crosstalk is greater than CPW crosstalk because MS transmission lines do not have shielding ground lines on either side of the signal line, however the primary disadvantages of MS transmission lines are that vias are required and that the characteristic impedance depends on the substrate thickness. This results in a significant process development cost. For example, the signal line width of a 50 MS transmission line on a standard thickness 25 mil 3" GaAs wafer is 500 m. This is undesirable for multiple reasons. Wide signal lines require more total area for a circuit layout, and thicker substrates increase radiation losses and decrease heat conduction away from circuit junctions. As a result, commercial MS processes use 8 mil or thinner substrates. Unfortunately, GaAs is

fragile and great care must be exercised in handling thin wafers to avoid yield losses. Through-wafer via etching and metal fill processes must also be developed. Figure 2.2 shows the metal-loss attenuation of 50 MS transmission lines on 10-mil alumina.

Stripline transmission lines have lower loss than either MS or CPW transmission lines. The stripline transmission line shown at the bottom of Figure 2.1 is essentially a MS transmission line with a second ground plane above the signal line and a homogeneous dielectric. Because the signal current is now distributed over both the bottom and top surface of the signal line, the effective series resistance is lowest of the three transmission lines discussed here. Similar to microstrip, the inductance and capacitance are varied by changing the signal line width that the signal-to-ground line gap, respectively. Stripline transmission lines are more difficult to integrate with MEMS structures, however they have several advantages over MS and CPW lines. If the dielectric is homogeneous TEM waves propagate in the stripline and there is no dispersion, unlike MS and CPW lines that both have air-dielectric interfaces. Dielectric loss is eliminated if air is used and there are also no radiation or surface wave losses. These advantages make stripline attractive for broadband, high frequency applications where dispersion and radiation loss are high. The integration of stripline transmission lines and RF MEMS structures is discussed in more detail in Sec. 2.4.

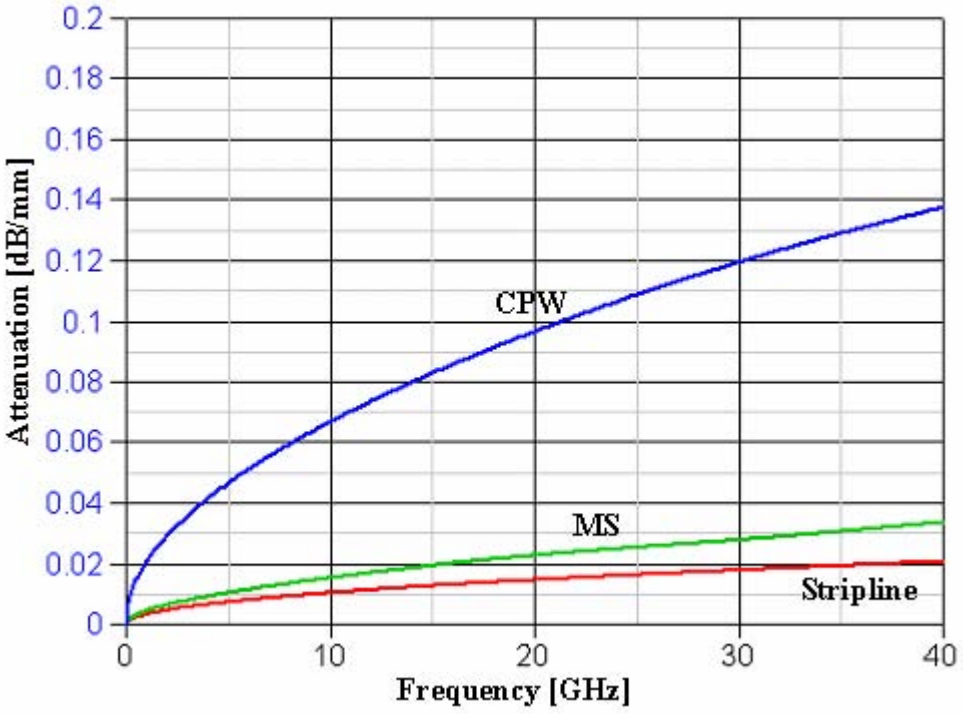


Figure 2.2: Attenuation of CPW, MS, and stripline transmission lines.

2.2 Dielectric Losses

Dielectric losses have two components: ohmic losses and relaxation losses. Losses in insulating microwave materials such as quartz, alumina, and sapphire are dominated by relaxation because they have very little free charge. Attenuation values are typically less than $5x10^{-4}$ dB/mm at 10 GHz (see Table 2.1) and planar transmission losses are dominated by

conductor losses at all RF and microwave signal frequencies. Semiconductors such as Si and gallium arsenide (GaAs) have a large component of free charge introducing a significant component of ohmic loss. The attenuation values of semi-insulating (SI) GaAs at 10^7 k cm, and Si at 1 k cm and 10 k cm are also listed in Table 1 and are significantly higher than the attenuation of the insulating substrates. Both ohmic and relaxation losses are significant in SI GaAs, however planar transmission line metal losses are still dominate at most RF and microwave frequencies. The loss of high-R Si is dominated by conductive losses, and depending on the substrate resistivity, there is a particular frequency over which metal losses dominate and under which ohmic dielectric losses dominate. To show this, Figure 3 contains plots of the dielectric losses in Si as a function of frequency for different values of bulk resistivity. Here the attenuation is frequency-independent because the assumption is made that losses are dominated by ohmic conduction in the substrate at all values of substrate resistivities. Also plotted for comparison are the metal losses of 50 MS and CPW transmission lines on 10 mil Si and 25 mil Si, respectively. For a CPW on a 25 mil high-R Si substrate with 1 k cm resistivity, this frequency is approximately 7 GHz. Above 7 GHz, CPW metal losses begin to dominate, and below 7 GHz, substrate ohmic losses begin to dominate. For substrate resistivities of >2 k cm, CPW metal losses exceed substrate losses above approximately 1 GHz. The high-R substrates used in this project were specified to >5 k cm so that CPW losses were dominant over the entire band. For MS transmission lines, the substrate resistivity should be >10 k cm so that metal losses dominate over the entire band.

Table 2.1: Dielectric Losses of Microwave Substrates

Substrate Material	**Attenuation at 10 GHz [dB/mm]**
Sapphire	3×10^{-4}
Quartz	1.5×10^{-4}
Alumina	5×10^{-4}
SI GaAs (10^7 k cm)	4×10^{-3}
High-R Si at 1 k cm	3.4×10^{-2}
High-R Si at 10 k cm	3.4×10^{-3}

As a note, standard 2 – 20 cm Si commonly used for manufacturing CMOS circuits has a dielectric loss of approximately 4 dB/mm. Over half of the propagating signal is attenuated over a distance of 1 mm. Clearly this substrate is inappropriate for implementation of passive components.

2.3 Processing and Characterization of High-R Si for RF MEMS Technology

2.3.1 Passivation

High-R Si requires the deposition of an insulating passivation layer prior to processing RF MEMS circuits in order to prevent conduction between metal features and breakdown of metal-semiconductor rectifying contacts. Passivation with Si oxide (oxide) by means of tetraethylorthosilane (TEOS), dry O_2, and steam oxidation were investigated. Silicon Nitride (SiN) on oxide was also investigated. A comparison between films was made by comparing the measurements of the insertion loss of various lengths of CPW transmission lines. Considerations in selecting the appropriate film or combination of films include electric field breakdown, trapped charge, process temperatures, and resistance to the release chemistries that are used in MEMS processes. Oxide on high-R Si was characterized first to determine the best surface passivation layer. Then SiN was deposited on the oxide and characterized. SiN is important as a means of preventing etching during the release process.

Three high-R Si wafers were used to characterize passivation with TEOS-deposited oxide. Each wafer had a different thickness of 0.1, 0.5, and 2.0 m of oxide deposited by TEOS at 750°C in the VTR. The wafers were subsequently annealed for 3 hours in N_2 at 1100°C. The wafers were cleaved into smaller samples in order to fit into the contact aligner at the Compound Semiconductor Research Laboratory (CSRL), and 1.7 m of Au was deposited by evaporation

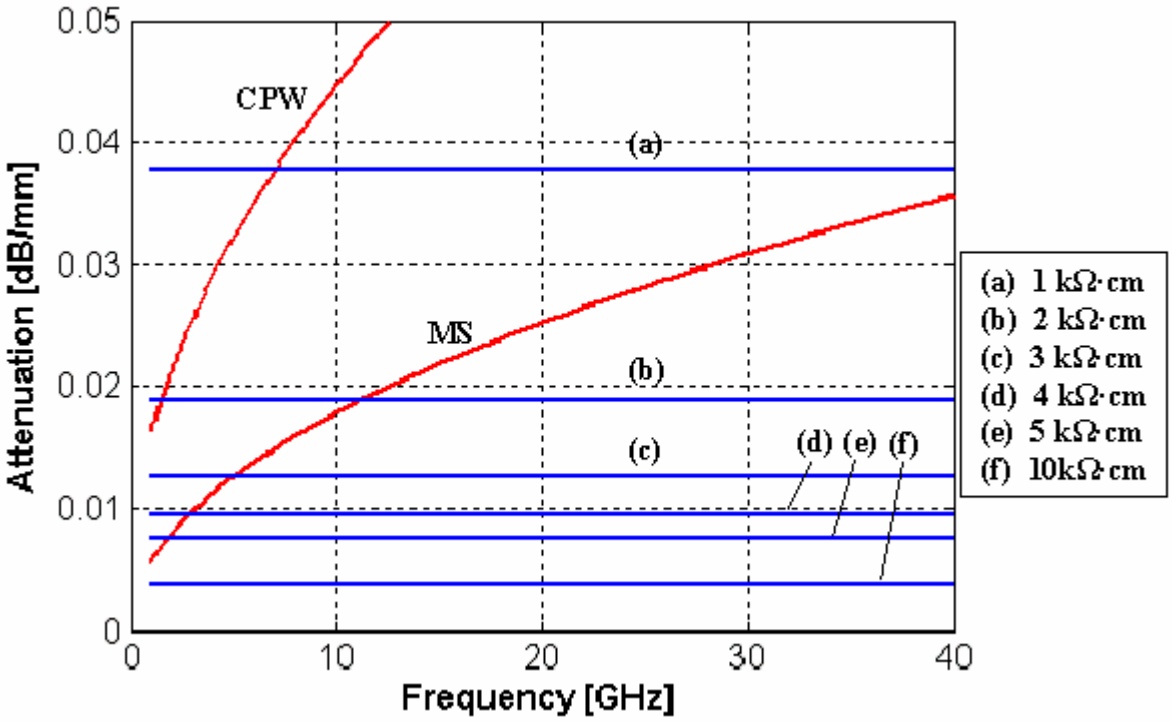


Figure 2.3: Si dielectric attenuation for various substrate resistivities plotted with 50 MS and CPW transmission line losses.

following patterning of negative photoresist. The resist was removed by lift-off to form CPW

test structures with lengths of 2.7, 5.5, and 11.3 m. S-parameters of the CPW's on each wafer were measured with a HP8510 vector network analyzer (VNA). The results are shown in Figures 2.4, 2.5, and 2.6 as the 'before anneal' curves. The insertion loss measurements have been normalized to their respective CPW lengths in order to obtain a loss per-unit-length measurement in dB/mm. Then, a 90 minute forming gas anneal (3% H_2, 97% N_2) at 400^{o}C was performed on all of the samples and S-parameter measurements were repeated. These results are plotted as the 'after anneal' curves in Figures 2.4, 2.5, and 2.6.

The insertion loss of CPW's on both the 0.1 m and 0.5 m thick oxide layers improved following annealing. Since the hydrogen in forming gas anneals is well known to tie up dangling Si bonds at the Si-oxide interface, this suggests a correlation between Si dangling bonds and an increase in CPW propagation loss. The interface states will affect the amount of free carriers in the underlying Si, which in turn will increase the dielectric attenuation. The measured attenuation values of the 0.1 m oxide sample after annealing (Figure 2.4) are close to the predicted attenuation values of a conductor-loss dominated CPW with a 1.7 m thick Au film on high-R Si. Therefore, it is reasonable to assume that the dielectric loss due to Si dangling bonds has become insignificant relative to the conductor loss following the anneal. However, the S_{21} curves of the 0.5 and 2.0 μm oxide samples after annealing (Figures 2.5 and 2,6) do not approach predicted values. They also have initially higher insertion loss levels prior to annealing in forming gas. In the case of the 2 m oxide sample, the loss before and after annealing is substantial, showing only a small improvement after annealing. This increase in loss as a function of thickness is possibly due to the presence of fixed oxide traps in the bulk of the oxide films. As the films get thicker, the amount of fixed oxide traps exceeds the amount of interface states, diminishing the improvement of the forming gas anneal. More experimentation is required to explain these observations, however we can conclude that TEOS deposited oxide films that are thicker than 0.1 μm are too lossy for microwave applications.

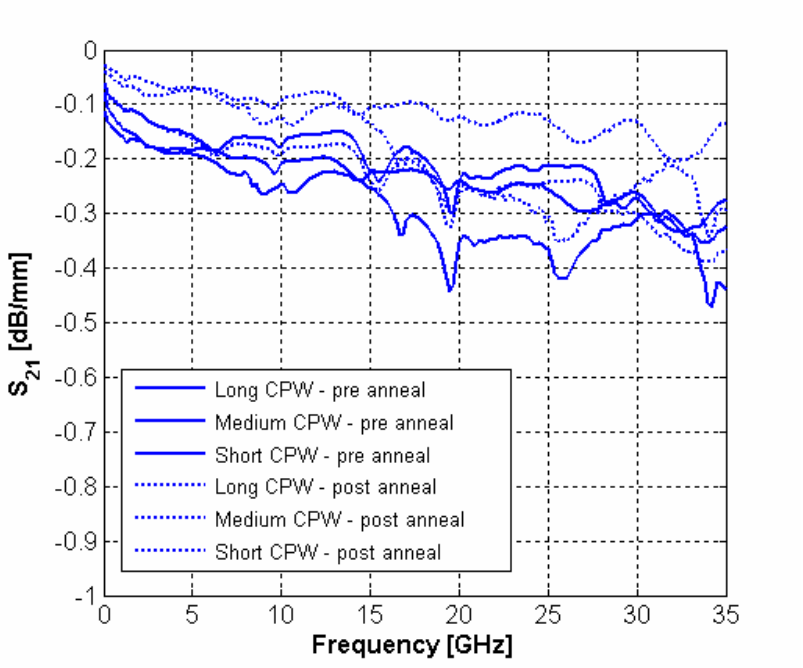


Figure 2.4: S_{21} measurements of Au CPW's on 0.1 m TEOS oxide on high-R Si before and after forming gas annealing.

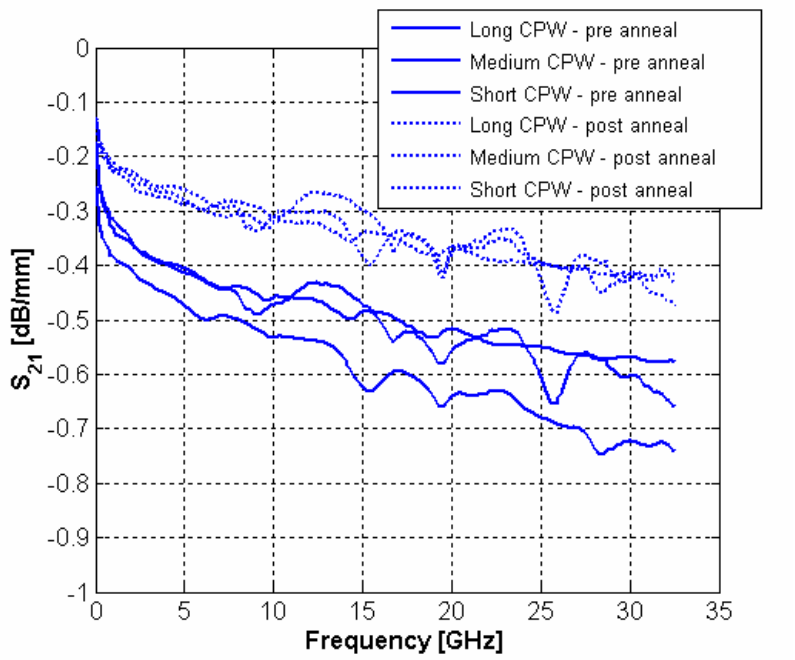


Figure 2.5: S_{21} measurements of Au CPW's on 0.5 m TEOS oxide on high-R Si before and after forming gas annealing.

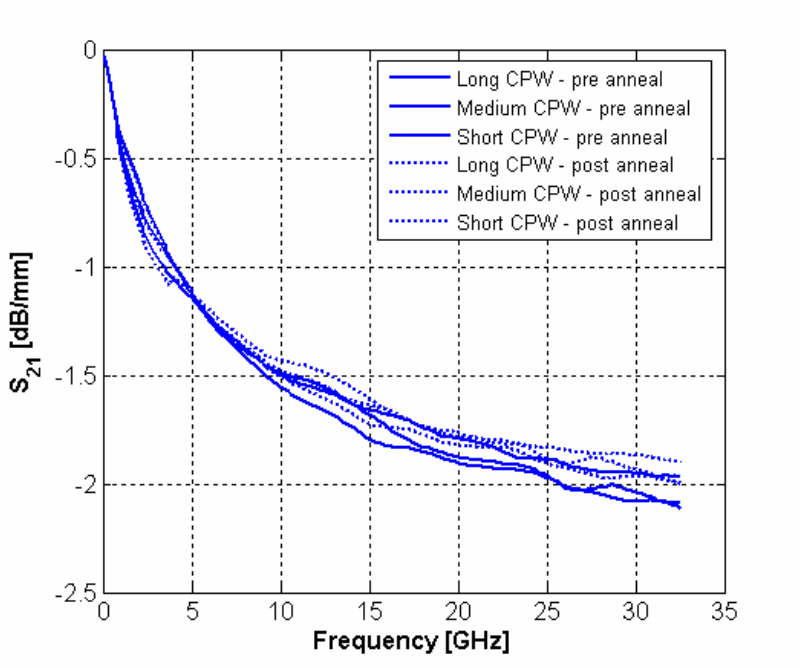


Figure 2.6: S_{21} measurements of Au CPW's on 2.0 m TEOS oxide on high-R Si before and after forming gas

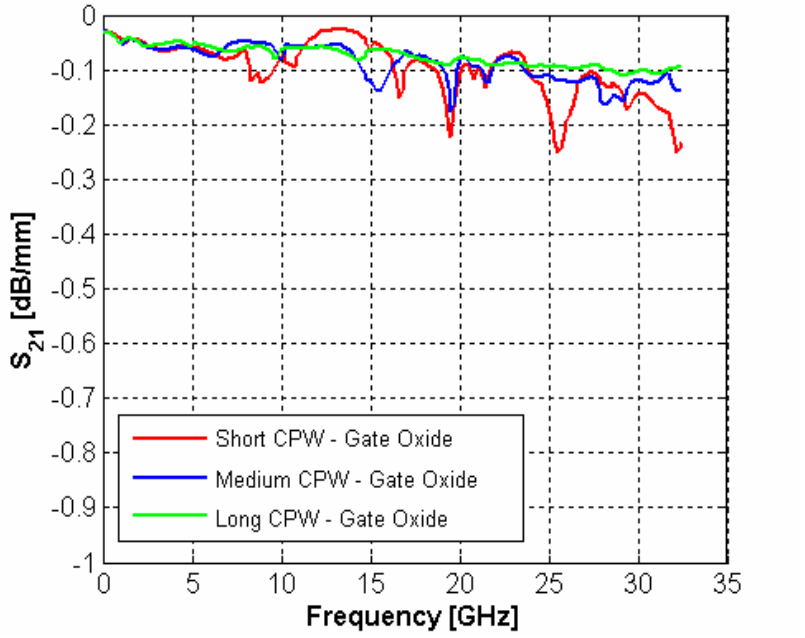


Figure 2.7: S_{21} measurements of Au CPW's on 120 gate oxide on high-R Si.

For the next experiment, a 120 gate oxide was deposited by dry O_2 onto high-R Si, followed by the evaporation deposition and lift-off patterning of Au CPW transmission lines at

the CSRL. The resulting S_{21} measurements are shown in Figure 2.7 and are close to the predicted values of conductor-loss dominated Au CPW's on high-R Si. Next, a 0.1 μm oxide layer was deposited by steam oxidation on high-R Si. S-parameter measurements of CPW transmission lines are shown in Figure 2.8. This loss is also close to predicted values of conductor-loss dominated Au CPW's on high-R Si. The final oxide layer that was investigated was a deposited by a 2-step process in the Epic and Integrity systems. The results are shown in Figure 2.9. The loss here is seen to be close to the values of the other CPW's on thin oxide layers and much lower than the thicker VTR TEOS deposited films. These results suggest that there are a lot fewer fixed oxide traps present in the films deposited by wet and dry oxidation and by the Epic and Integrity and than in the TEOS oxide films deposited in the VTR furnaces.

We then measured the propagation loss of a SiN-on-oxide stack by depositing a 0.7 μm thick layer of LPCVD Si-rich SiN on 0.1 μm of oxide deposited by steam oxidation. S_{21} plots are shown in Figure 2.10 for the 3 CPW line lengths and are indistinguishable from the S_{21} plots in Figure 2.8 indicating that the addition of SiN has no affect on the dielectric attenuation relative to the CPW conductor loss. This result is surprising given the amount of traps typically present in SiN films and at the SiN-oxide interface.

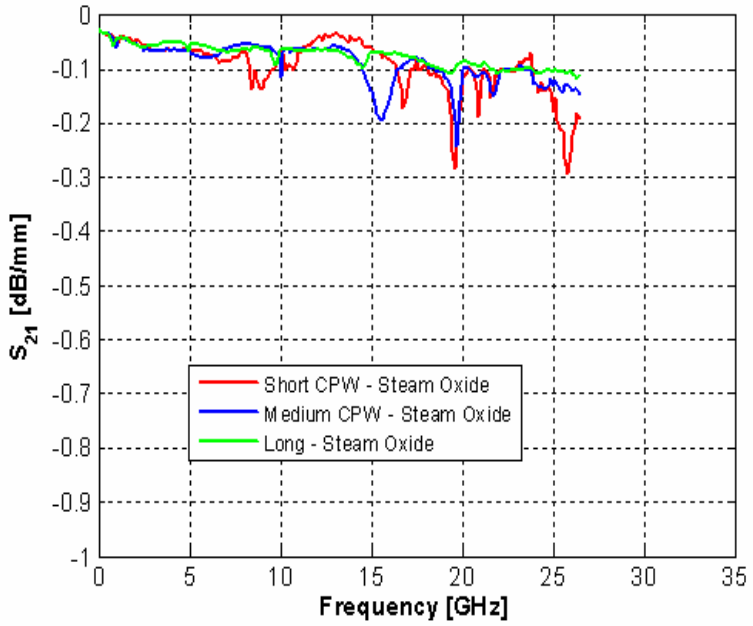


Figure 2.8: S_{21} of Au CPW's on steam oxide

When Au CPW's are deposited on passivation layers of thin TEOS-deposited oxide, dry-O_2 grown oxide, steam grown oxide, and thick oxide deposited by the Epic and Integrity, the transmission line losses are close to the predicted conductor-loss values and do not add significant additional loss. However, it is important to note that the evaluation of each of the oxide dielectrics by measuring CPW attenuation is less sensitive than by using MS transmission lines because the CPW conductor loss is much higher than the MS conductor loss (Figure 2.2). Any of the oxide deposition methods just described is adequate enough to passivate the high-R Si surface in order to evaluate RF MEMS components such as switches with CPW transmission lines. The HF-based solutions that are often used to etch sacrificial layers require an additional protective layer on the oxide passivation films to prevent them from etched during the release

process. We have examined Si-rich SiN films on steam oxidation and have found that CPW losses are not increased. Low-loss microwave circuits such as phase shifters and filters will require the development of a MS transmission line process, which means that the attenuation of the oxide films fabricated by each of these deposition methods would have to be re-examined.

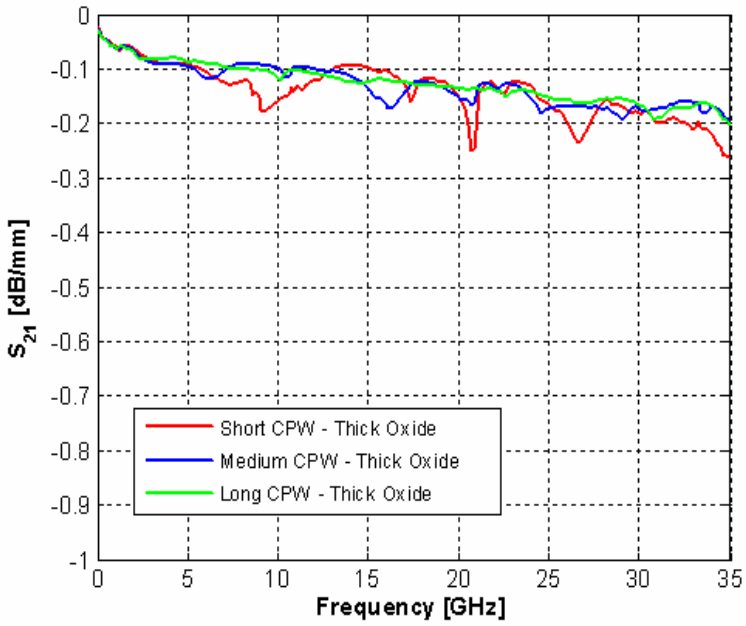


Fig. 2.9: S_{21} of Au CPW's on a thick oxide stack deposited by the Epic and the Integrity systems.

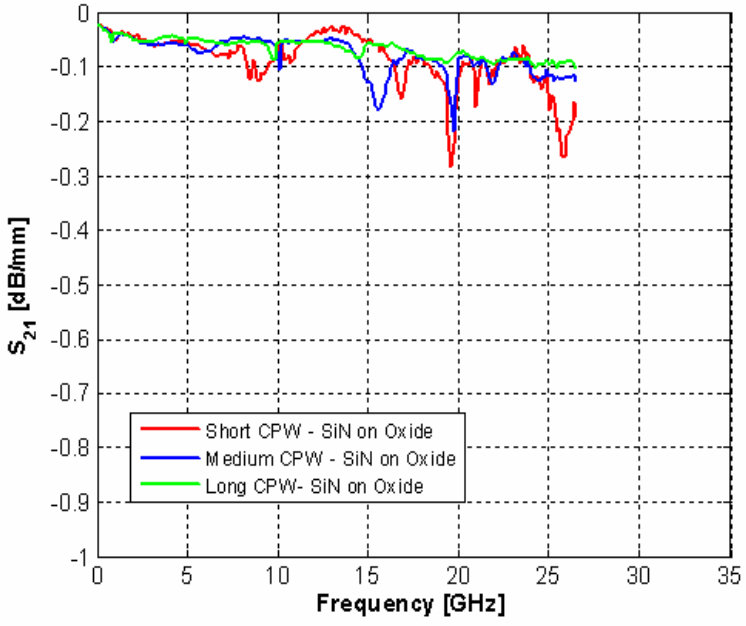


Fig. 2.10: S_{21} of Au CPW's on SiN on steam oxide.

2.3.2 Materials Limitations

CMOS processing facilities have a short list of elements that are allowed in the fabrication area to prevent contamination in the Si or gate oxide regions. This is particularly critical in the front end of the process where impurities cause a loss of control of MOS devices or the introduction of deep level traps in the Si bandgap. The allowed materials are Si, O, N, W, Al, B, P, Ti, and H. Advanced CMOS fabs also process Cu as interconnects and the wafers are exposed to KOH during polishing steps, however this occurs only in the backend of the process after proper diffusion barriers have been deposited on the wafers to protect them. Furthermore, any CMOS facility will be reluctant to introduce new elements into the process without a large body of data proving that these elements show a decisive advantage to circuit performance. In other words, without significant technological and economic drivers, the RF MEMS designer is limited to the aforementioned list of elements.

Sacrificial layers used in a micromachining process in a CMOS lab are often oxides and nitrides which are chosen for their etch selectively to metal and Si mechanical materials and for their thermal stability during the deposition of non-Si mechanical materials (300^o – 700^oC) and subsequent annealing processes, where necessary. Organic photoresists are generally not appropriate for processes requiring metal deposition temperatures above about 225^oC. Consequently, the release chemistry is typically HF-based and will attack any unprotected SiO_2 passivation layer on the surface of the high-R Si substrate. Low-stress silicon nitride (SiN), often called Si-rich SiN, is used to protect the passivating oxide layer during the release process. Alternatives to nitride and oxide sacrificial materials are available. One example might include W as a sacrificial material that is easily removed in H_2O_2 and is highly selective to most other materials in the fab. However, CVD-deposited W thickness is generally constrained to less than 1 μm due to stress.

2.3.3 Temperature limits

To prevent the blurring of junction profiles and the potential decrease in resistivity of the high-R Si, and thus a loss of it's microwave properties, a processing temperature limit of 800^oC was suggested by Rosen, et. al. [25]. Our substrates are not doped, however we were concerned about unintentional doping, activation, and subsequent diffusion of substitutional impurities introduced during high temperature processes such as annealing and oxidation steps. These impurities might exist as background impurities present in the fabrication equipment used in each of the processes and contaminate the high-R Si. Based on the results described in Section 2.3.1, we found no evidence that these processes increased the loss in our CPW transmission lines. Each of the samples that underwent either high-temperature post-deposition anneals or had steam or dry oxidation steps had signal loss measurements close to the predicted conductor-loss limited values for CPW transmission lines. In the case of the thinnest TEOS-deposited oxide, a forming gas anneal was required to reduce loss to the predicted values, and we believe that the high loss in the thicker oxides was due to fixed oxide charge and not to the process temperatures. As discussed earlier, a more sensitive set of measurements should involve microstrip or stripline transmission lines because metal losses in these lines are much lower than CPW losses.

2.4 Membrane Supported Stripline Technology

2.4.1 Introduction

In an effort to extend low-loss RF MEMS technology to broadband applications at frequency ranges much greater than Ka band, a paper study was performed on membrane supported stripline technology. As discussed in Section 2.1, planar MS and CPW technologies are commonly used because they are MMIC compatible, and in the case of MS, have low metal propagation losses. However, CPW and MS performance become limited at Ka band frequencies by radiation losses, surface wave propagation, and dispersion. Radiation loss is caused by circuit discontinuities and is worse for thick substrates with low dielectric constants. Increasing the substrate dielectric constant and thinning the substrate reduces radiation loss, such as in a 4-mil GaAs microstrip technology, however these substrates are difficult to handle and can result in high yield loss. Dispersion and surface wave propagation are caused by the substrate-air dielectric discontinuity. Dispersion affects high-frequency broadband performance and surface wave propagation contributes to signal loss.

Unlike MS and CPW transmission lines, striplines do not have radiation loss, dispersion, or surface wave propagation losses, and have the additional advantage of lower metal-loss attenuation. Furthermore, using air as the dielectric above and below the signal line eliminates dielectric losses. By fabricating microwave circuits on thin membranes and encapsulating them in a metal cavity formed out of bulk micromachined Si, low-loss, air-dielectric stripline circuits can be realized. A schematic of this technology, known as membrane-supported circuits, is shown in Figure 2.11. The signal lines are patterned on a thin Si-rich SiN membrane that is suspended after a portion of the substrate has been removed either by potassium hydroxide (KOH) wet etching or deep reactive ion etching (DRIE). The circuit size is limited by the mechanical integrity of the membrane. Three other wafers are then bulk micromachined to form the grounded cavity surrounding the membrane. The top wafer does not require any patterning and is blanket metallized to form the upper ground plane. The wafer located between the top wafer and membrane wafer is etched completely through its thickness to form the stand-off between the membrane-supported signal lines and the upper ground plane, and to provide electrical inputs and outputs. This wafer is also blanket metallized. The bottom wafer does not require patterning and is blanket metallized. All wafers are bonded together to form the cross-section shown in Figure 2.11.

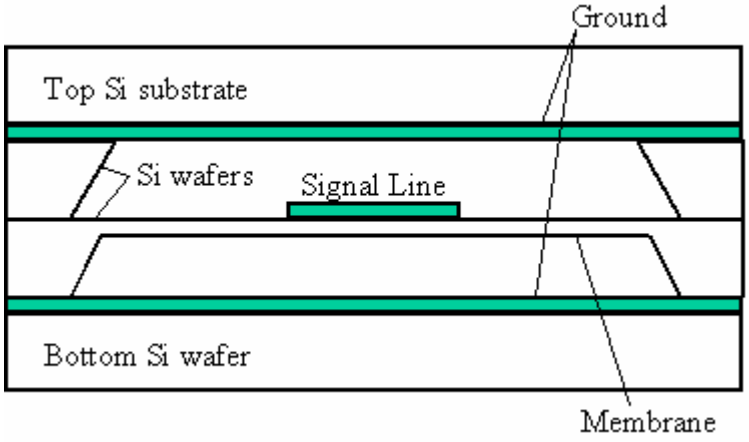


Figure 2.11: Membrane-supported stripline transmission lines. The signal line is supported by a thin SiN membrane and metallized wafers that are bonded above and below the signal line wafer form the ground lines.

A number of high-performance membrane-supported microwave circuits have been demonstrated [26]. Performance in these circuits is only limited by conductor losses and transition losses at the input output of the circuit, however, these circuits are not reconfigurable. The addition of low-loss RF MEMS components would add reconfigurability without compromising circuit performance. From our assessment, this technology appears to be MEMS-compatible and is readily hermetically sealed at the wafer level for high-reliability operation. The operational frequency of this technology is easily extended to greater than 100 GHz. A combination of bulk micromachining and wafer bonding can be used to obtain the upper and lower ground planes, as discussed earlier, and the MEMS structures can be fabricated on a thin suspended membrane made of Si-rich SiN deposited by low-pressure CVD methods. After reviewing process methods, it was concluded that this technology is more easily manufactured in a flexible lab, such as the CSRL or the new MESA flex lab, than in the MDL because the greater selection of available process materials makes it easier to fabricate switches. The next section describes the limits of MS transmission lines and the benefit of using striplines at high frequencies.

2.4.2 Microstrip Transmission Line Limits

This section describes the high-frequency performance limits of MS transmission lines. Since CPW lines have higher metal losses than MS lines, they are omitted from this discussion. As the signal frequency increases, the loss of MS lines increases due to conductor losses, radiation, surface wave generation, substrate mode generation, and dielectric loss. Dispersion is also a problem at higher frequencies. As the skin depth becomes significantly less than the conductor thickness, metal losses are determined by the conductivity and width of the conductor. Surface roughness is also significant, but is ignored in this discussion. Using a wide signal line made out of Au, Al, or Cu minimizes conductor losses. Substrate modes are generated in the signal line to ground line gap and surface waves are propagated outward from the signal line due to total internal reflection at the dielectric-air interface and reflection off of the backside metal-dielectric interface. Both substrate mode and surface wave generation is generally not a problem until at least W band frequencies [27] and will not be further discussed.

Radiation loss occurs at discontinuities in the circuit and is worse for thicker substrates with low dielectric constants. Radiation can be characterized by considering the radiation loss Q vs. frequency of half-wavelength (/2) resonators,

$$Q_r = \frac{3\varepsilon_r Z_o \lambda_o^2}{32\eta h^2} \tag{1}$$

where $_r$ is the substrate dielectric constant, Z_o is the characteristic impedance of the transmission line, $_o$ is the free-space wavelength of the signal, is the intrinsic impedance of free space (120), and h is the substrate thickness. Plots of Q_r as a function of h at 40 GHz and 100 GHz for quartz, alumina, and GaAs substrates are plotted in Figure 2.12. Table 2.2 lists the frequencies where the radiation loss and conductor loss Q's are equal, $Q_r = Q_c$, for 10 mil thick substrates of quartz, alumina, and GaAs. The conductor loss Q is given by

$$Q_c = \frac{\beta}{2\alpha_c} = \frac{\pi}{\alpha_c \lambda_o} \tag{2}$$

where is the propagation constant and $_c$ is the conductor attenuation. Z_o = 50 characteristic impedance is assumed for the Q_c calculations.

Both plots in Figure 2.12 show the strong dependence of substrate thickness on radiation loss resulting from the $1/h^2$ dependence in Eq. (1). For a 25-mil thick substrate, the Q is poor at both 40 GHz and 100 GHz regardless of the dielectric constant values. At 100 GHz, any microstrip substrate is going to suffer from low radiation Q's, making microstrip impractical for this frequency range. At 40 GHz, circuits on 10 mil GaAs have reasonable Q_r values, however when the conductor loss (Q_c) is factored in, the total circuit loss will have a Q well below 100. This is one reason for going to 8 mil and 4 mil GaAs processes. Table 2.2 shows the relative operation frequency limits of 10 mil substrates of quartz, alumina, and GaAs. 10 mil alumina has the best performance trade-off of bandwidth and loss.

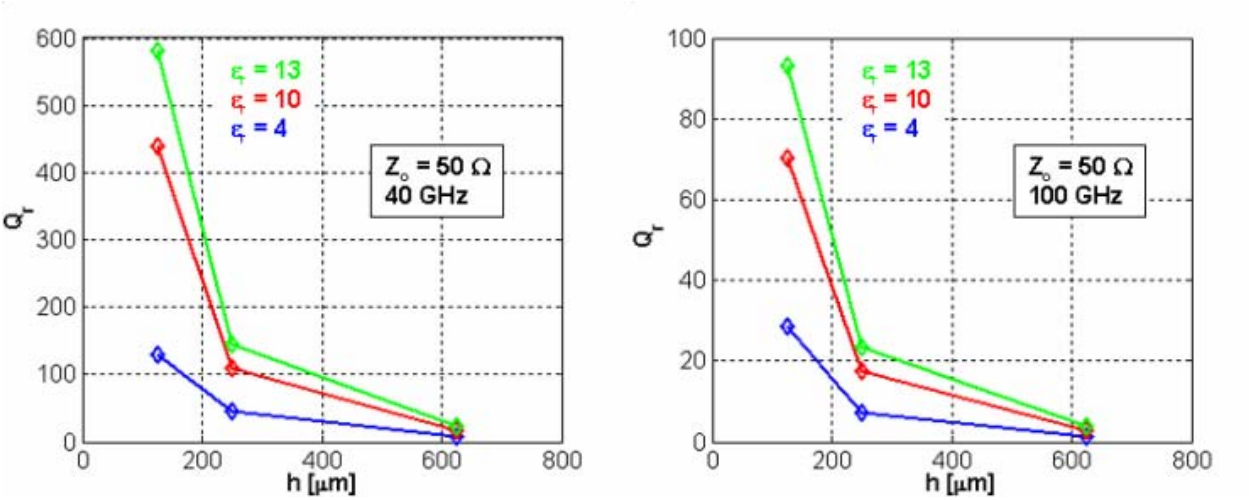


Figure 2.12: MS radiation loss Q vs. substrate thickness at 40 GHz and 100 GHz for quartz, alumina, and GaAs substrates.

Table 2.2: Frequency and Q values when $Q_c = Q_r$

Substrate (10 mil)	**Frequency when $Q_r = Q_c$**	**Q_r, Q_c Value**
Quartz	16 GHz	270
Alumina	26 GHz	260
GaAs	42 GHz	130

Dispersion is considered to be negligible below the following frequency [27],

$$f_D = 0.3\sqrt{\frac{Z_o}{h\sqrt{\varepsilon_r - 1}}} \quad (3)$$

where Z_o is the transmission line characteristic impedance, $_r$ is the substrate dielectric constant, and h is the substrate thickness. Decreasing $_r$ gradually increases the dispersion cut-off frequency, however this also increases the radiation loss as indicated by Eq. (1). Table 2.3 shows f_D for quartz, alumina, and GaAs substrates with 50 transmission lines. It is clear from this table that any broadband microstrip Ka band application will suffer from dispersion.

Table 2.3: Dispersion cut-off frequencies for quartz, alumina, and GaAs.

Substrate (10 mil)	f_D
Quartz	10 GHz
Alumina	7.8 GHz
GaAs	7.2 GHz

3.0 Molded W Processing and Circuits

3.1 W as a Mechanical Material

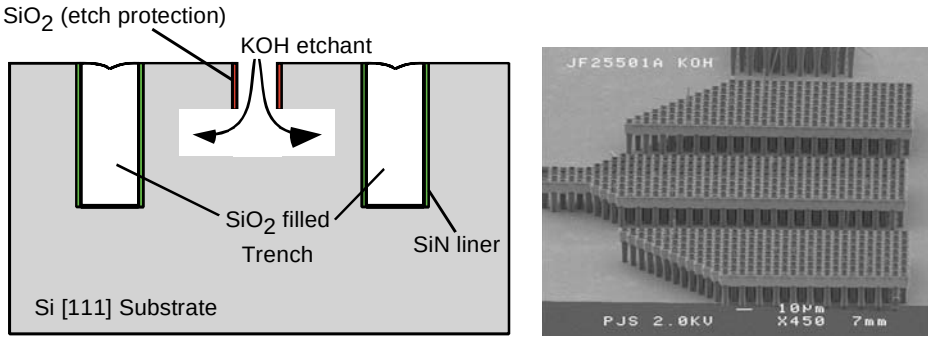
Most micromachining processes involve the use of Si because of its high quality mechanical properties and etch selectivity to readily available sacrificial materials. Surface micromachined polySi is popular because flat, low-stress films can be fabricated. However the use of W instead of Si as a mechanical material has some compelling advantages. W has a Young's modulus of 400 GPa compared to Si's 160 GPa and CVD W deposition temperatures are approximately 400^{o}C compared to polySi deposition temperatures of close to 600^{o}C (not including the high-temperature stress-relieving anneal). This makes the processing of W MEMS structures electronics compatible in either an interleaved or electronics-first approach. The main drawback to the use of blanket CVD W is the high built-in stress of the material. A high-temperature stress-relieving annealing step does not exist as it does with polySi surface micromachining. In fact, the stress of blanket deposited material is sufficiently high to prevent the use of many typical fabrication operations on the material, due to the low radius of curvature of the resulting wafers. This stress arises from two components. The first component is a combination of the compressive stress associated with the sputtered TiN adhesion layer required for CVD W deposition (~-1GPa) and a high level of built-in stress rising from the CVD W deposition process. The second component of stress arises as a result of the difference in thermal expansion coefficients between W and the Si substrate. The problem of built-in stress has been solved here by CVD depositing W into high aspect ratio trenches. Since the trench sidewalls are much higher than the trench base is wide, a thick W film that is largely stress compensated is formed. The following sections describe processes that are variations on this theme. The Si standoff approach is a bulk process that forms W molds in the Si substrate and the MOLTUN approach is a surface micromachining process that forms W molds in a sacrificial layer above the Si substrate.

3.2 Si Stand-off Approach

3.2.1 Introduction

The Si standoff approach is a Sandia patented technique used to elevate RF MEMS components above the Si substrate in order to minimize dielectric losses. Bulk <111> Si is removed in a lateral potassium hydroxide (KOH) wet etching process, resulting in a uniform air-gap isolation between mechanical structures and the Si substrate (Figure 3.1a). A modified Si standoff approach incorporating a tungsten (W) molding process is investigated that allows for thick, stress compensated, mechanical structures, as shown in Figure 3.1b. This process has a

couple of key advantages over other approaches. First, since the Si substrate is located further away from the RF signals, low-resistivity (low-R) Si substrates are possible. Low-R Si costs less than high-R Si, allowing performance and cost to be traded off for a given application. Second, the thick W mechanical material makes it possible to develop laterally actuated switches (as opposed most switch designs that are vertically actuated). Lateral actuation is more compatible with linear electrostatic actuation mechanisms such as the use of interdigitated comb fingers and larger actuator displacement is possible, as opposed to the 2 – 4 μm gaps that are practically obtainable with vertically actuated switches. Practical issues with laterally actuated switches involve deposition of contact materials on the switch sidewall and control of the sidewall roughness.



(a) (b)

Figure 3.1: Silicon standoff process: (a) the properties of <111> Si are used to create a uniform air gap between the mechanical layers and the substrate, and (b) a new W molding approach is used to fabricate thick, low residual stress, mechanical structures.

3.2.2 Switch Description

A diagram of the switch is shown in Figure 3.2. The switch is designed to laterally actuate by interdigitated W comb fingers and to open by the mechanical restoring force of the folded springs. The electrical contact is a block of W that is insulated from the actuator by a molded SiN mechanical linkage. An opening in one of the CPW ground lines allows the contact to reach the signal line (not shown in Figure 3.2). In order to decrease the contact resistance and attenuation of the CPW transmission lines, an additional series of process steps is added to deposit Au on the CPW transmission lines.

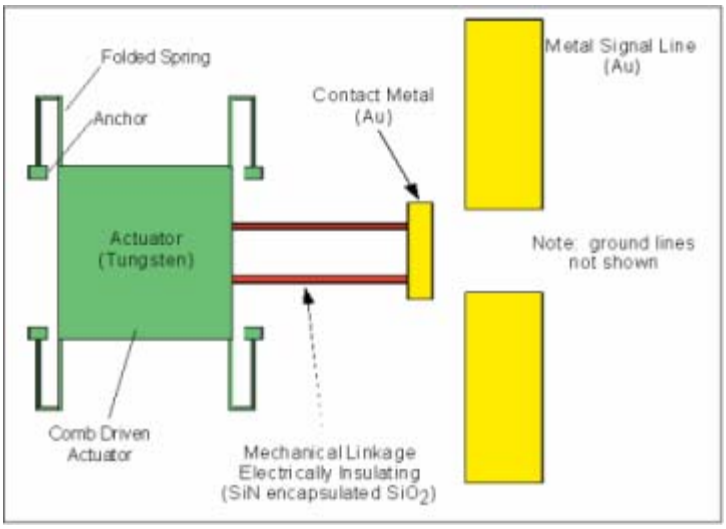


Figure 3.2: Diagram of the laterally actuating microswitch.

3.2.3 Processing method

Starting material consists of 2 – 20 cm, <111>, 6" Si substrates. The general process flow consists of a series of timed RIE etch steps to define narrow trenches of varying depths in the Si substrate. These trenches are filled and dry etched back to form planar filled trenches. Materials such as SiN, W, and oxidized polySi are used on different parts of the switch to form conducting paths, electrical insulation, and mechanical supports. The process flow used here is shown in Figure 3.3. The first trenches that are etched have the greatest depth in order to form the support connections to the substrate. These are lined with SiN and filled with polySi that is subsequently etched back for planarization and oxidized to form the electrically insulating supports (left side of Figure 3.3). Subsequent deposition and etch planarization steps result in shallower W and oxide-filled trenches. The oxide-filled trenches are used for electrical isolation and the W-filled trenches are used for the CPW's and actuator. The final step involves etching trenches into the substrate to allow access for the KOH release etch. The completed switch is shown in the SEM in Figure 3.4a and a close-up SEM of the comb drive actuator is shown in Figure 3.5.

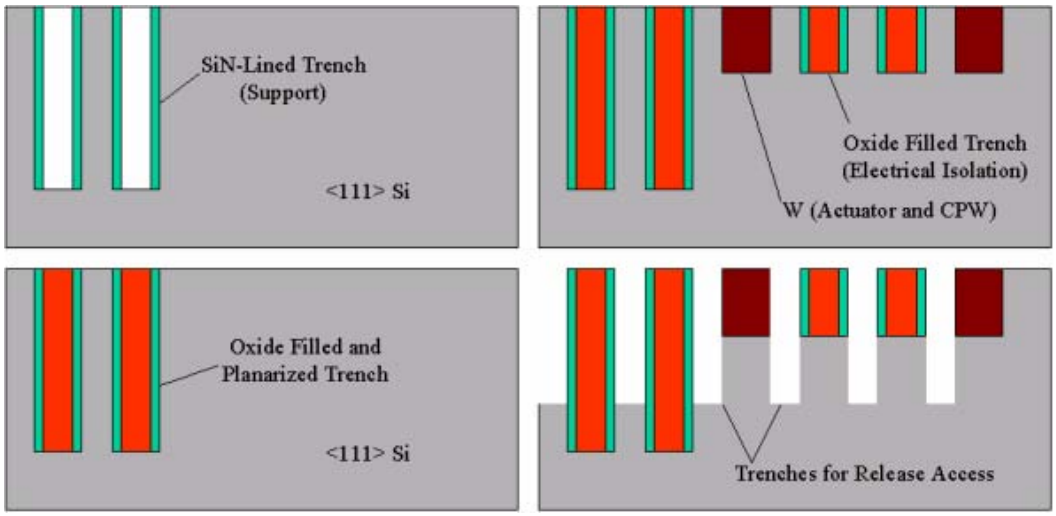
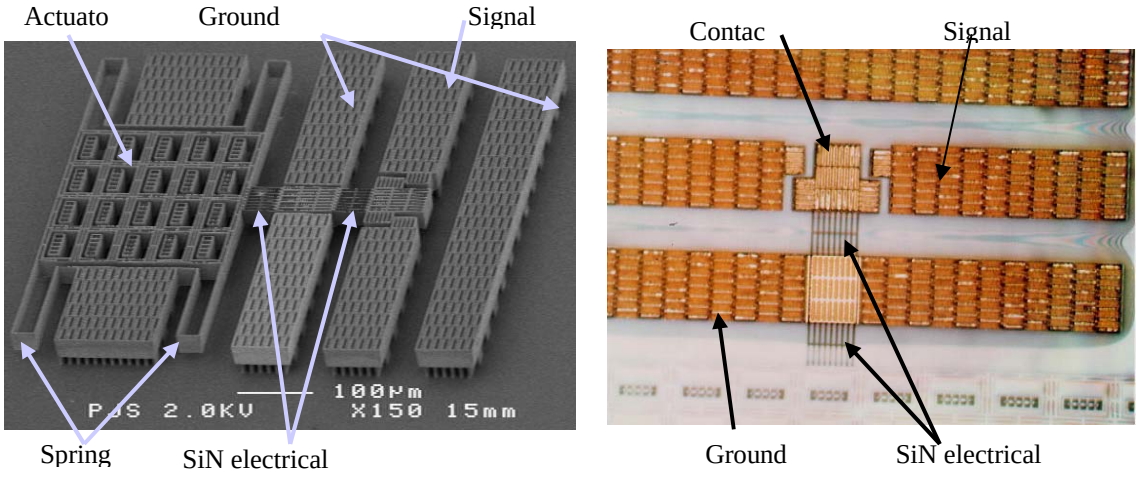


Figure 3.3: Si standoff approach process steps.

As it stands, the switch has a couple of performance disadvantages. First, the W has higher loss than high conductivity materials such as Au or Al, and second the switch has a break in the CPW ground line to accommodate the laterally actuating switch (Figure 3.4a). In order to solve this problem, an additional Au damascene process was added to the Si standoff process. Au is deposited into trenches above the W molded structures and ground back to form features. This part is released in a different chemistry prior to the KOH release step. Results of this process applied to a switch test structure are shown in Figure 3.4b. Au has been deposited and ground back to form a bridge over the lateral switch arm and to lower the CPW loss. A working device was not successfully completed with this process because we decided that the added complexity to the process made this process impractical for device fabrication.



(a) (b)

Figure 3.4: SEM photograph of the completed switch using the *Si standoff* process (a). The comb drive actuator is to the left. The dark areas of the device are SiN that was used to isolate the contact from the actuator. Results of grinding Au on Pt for the dual damascene process are shown in (b).

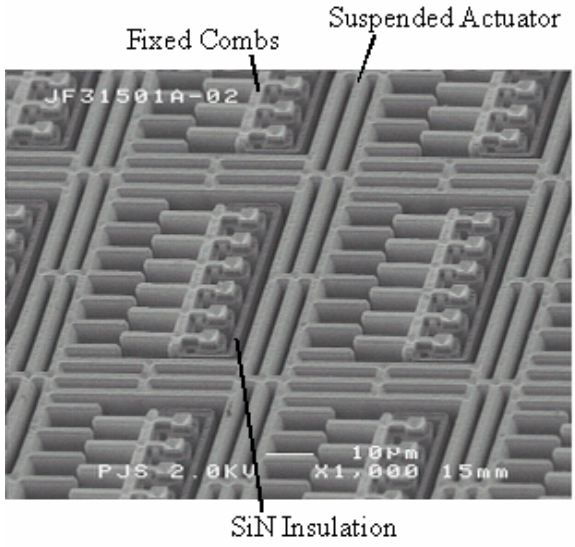


Figure 3.5: Close-up SEM image of the fixed combs and the suspended portion of the actuator.

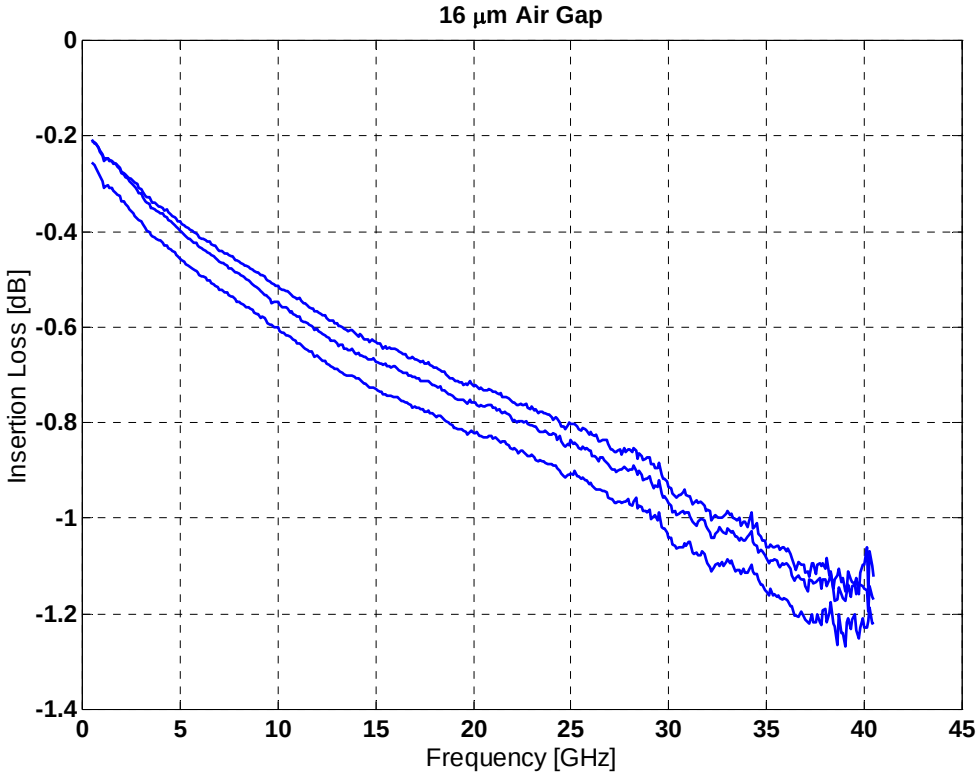


Figure 3.6: Molded W CPW insertion loss measurements. The CPW's are suspended 16 m above the Si substrate.

3.2.4 Results and Discussion

Insertion loss plots of 1-mm long W-molded CPW transmission lines are shown in Figure 3.6. These test structures were fabricated with a 16 m gap between the bottom of the molded W surface and the Si substrate. The insertion loss at 10 GHz is below 0.6 dB. This value is not unreasonable given the proximity of the Si substrate and the fact that W was used as the CPW metal. This result can be compared to the simulations shown in Appendix B of Au on varying thickness oxide layers on a low-R Si substrate. Losses for this structure are predicted to range from 0.5 dB to 0.8 dB at 10 GHz; similar to our measured values. The slight scatter in the three CPW measurements arises from the native oxide on the W CPW's. The probes required scrubbing down onto the CPW's to break through this layer and obtain a consistent measurement. The CPW attenuation measured here is too high for low-loss microwave circuits and will result in significant attenuation if any reasonable lengths of transmission lines are used.

The switch shown in Figure 3.4a was tested by applying a bias between the fixed combs and the moving actuator and monitored by applying a voltage across the signal line gap and monitoring current flow as the switch cycled open and shut. We observed that during test the structures moved in the opposite direction than was intended because the capacitance between the suspended part of the actuator and the fixed comb supports was larger than the capacitance of the interdigitated comb fingers. This caused the device to pull away from the contact and run

into the back portion of the interdigitated electrodes (The SiN insulator in Figure 3.5). Devices were allowed to run, since this still resulted in the collision of W – W contacts. A device from this lot achieved 1 billion cycles without sticking before the test was terminated.

As mentioned in the process section, the Au damascene process was abandoned due to the added process complexity. Unfortunately this limits the lateral switch process to what is shown in Figure 3.4. Although this switch was actuated to 10^9 cycles the contact was W-W and the CPW ground line was open. W-W contacts require high forces to break through the native films to form low resistance contacts and it is uncertain how an uncontrolled lab ambient will change the contact surface. There are competing processes between the breaking and forming of the native films during cycling. Evaporating metals such as Pt or Au onto the sidewalls of the switch can be done to lower the switch contact resistance and this has the additional advantage of simultaneously evaporating metal onto the CPW transmission lines to lower the attenuation. This could be accomplished by evaporating with a shadow mask. The presence of the open ground line will cause microwave performance problems in an actual circuit because of the floating ground lines and discontinuities that are formed.

This technology has an advantage that we did not exploit in this LDRD. By removing the proximity of the substrate from the transmission lines, the electromagnetic wave is propagating largely in a homogeneous medium: air. This not only lowers the dielectric losses, but also eliminates dispersion that is caused by a dielectric-air discontinuity, similar to what was discussed with a stripline transmission line in Section 2.4. With the application of a high-conductivity material to lower the propagation losses, this has potential for broadband, low-loss applications. The W mold can be made thick to reduce the losses inherent in thin CPW lines, as discussed in Section 2.1.

3.2.5 Conclusions

This process is advantageous because it is compatible with low-R Si substrates, however without a second mechanical level and high conductivity metals such as Au or Al, the attenuation remains high and the microwave properties are difficult to control. It is possible that at low frequencies where signal wave properties do not apply that this type of switch would be effective. One possibility of exploiting the strengths of this approach is to fabricate dispersionless transmission lines for broadband applications.

3.2 MOLTUN Process

3.2.1 Introduction

Unlike the bulk processing methods employed to fabricate structures in the Si Standoff process, the MOLTUN process is a CMOS back-end compatible surface micromachining process that patterns W free-standing structures above the Si substrate. The W films are thinner in this process, however greater mechanical complexity is possible by fabricating multiple process levels. Currently, up to 13 layers have been demonstrated with thicknesses varying between 2 and 25 m. A latching switch is demonstrated in this process.

3.2.3 Process Description

The MOLTUN process sequence is shown on the left side of Figure 3.7. W is used as the mechanical material and PECVD SiO_2 as the sacrificial layer. Trenches with a maximum width of 2 m and aspect ratios of up to 5:1 are etched into the sacrificial oxide and backfilled with W. The W is polished back and the oxide is etched in a HF solution to release the structures. Mechanical structures are formed by a grid of interconnected W beams formed by the filled trenches, as on the right side of Figure 3.7. Electrical isolation is accomplished by a PECVD SiN deposition and etch step prior to the sacrificial SiO_2 deposition.

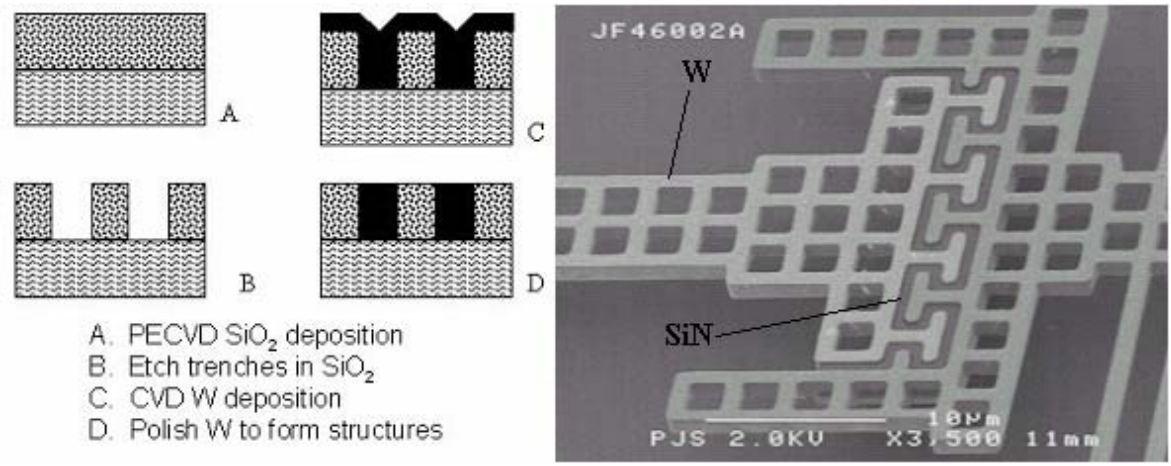


Figure 3.7: MOLTUN process description and a SEM micrograph showing how the interconnected W and SiN-filled trenches form free-standing mechanical structures.

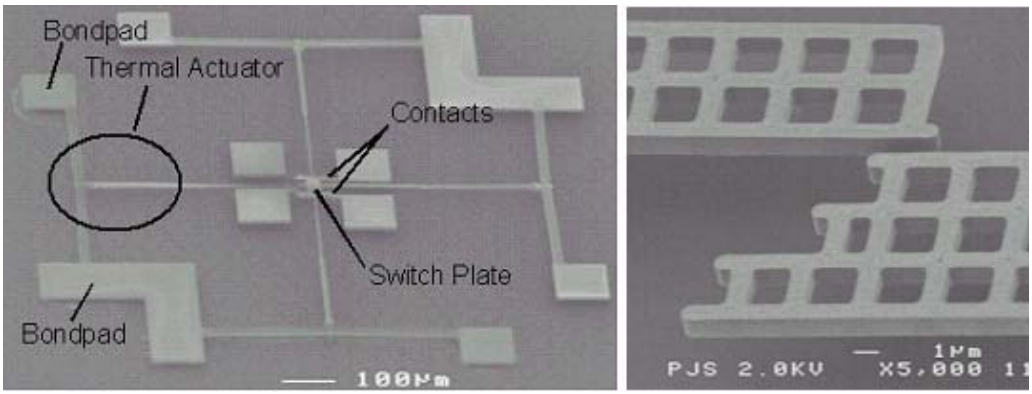


Figure 3.8: SEM micrographs of the latching switch and the latching mechanism fabricated in the MOLTUN process.

3.2.2 Latching Switch Demonstration

The latching switch shown in Figure 3.8 was fabricated using this process. The latching switch is formed out of a suspended W plate with two opposing thermal actuators. Each of the W suspending thermal actuator arms is in tension after the release process. This happens because the W is CVD deposited at 400°C and goes into tension as it cools due to the CTE mismatch between the W and the substrate (Si in this case). Applying a voltage between one or more combinations of bondpad pairs resistively heats and expands those springs. The springs that are opposite of the heated springs contract due to the built-in spring tension and pull the

plate in the direction of the unheated springs. The switch shown in Figure 3.8 has two pairs of opposing springs that allow it to have two degrees of freedom. The thermal actuation in combination with the built-in W stress results in plate displacements >10 microns and forces >10 mN. The switches and contacts can be patterned to accommodate mechanical stops for latching the switch plate (right side of Figure 3.8). The high built-in stress also has the advantage that latching contact forces are high without the need for applied signal power. Contact metals can be evaporated onto the switch sidewalls to lower the contact resistance. Angled evaporation and careful switch structural design prevents bond pads and contacts from shorting.

3.2.3 Conclusions

The MOLTUN process is a surface micromachining process with W and SiN mechanical and electrical layers that is back-end compatible with CMOS electronics and allows the fabrication of more complex mechanical structures than the Si Standoff Process. A thermally actuated latching switch capable of 10 mN of contact force was demonstrated in this technology for low frequency applications. Reliability of this device must still be determined.

4.0 Capacitive Switch Development

4.1 Capacitive Switch Technology

Capacitive switches are two-state capacitors. The typical capacitive switch, shown in Figure 4.1, is a metal bridge suspended above a CPW signal line with both ends of the bridge anchored to ground. The switch has a minimal loading effect on the signal line in this state (the passing state) and signals propagate with minimal reflection. The switch is snapped down when a voltage exceeding the electrostatic pull-in voltage is applied between the bridge and the signal line. In this state (the down-state) incident signals are reflected due to the formation of a low impedance path through the dielectric and the switch bridge to ground. The level of isolation depends on the relative value of the shunt impedance to the characteristic impedance of the transmission line, Z_o. The ratio of the blocking state (down-state) capacitance to the passing state (up-state) capacitance, C_{on}/C_{off}, is often used as a performance metric, with a typical value of 100 [6]. Generally, capacitive switches are used in this shunt configuration, as shown in Figure 4.1b, although a series configuration has been reported [20].

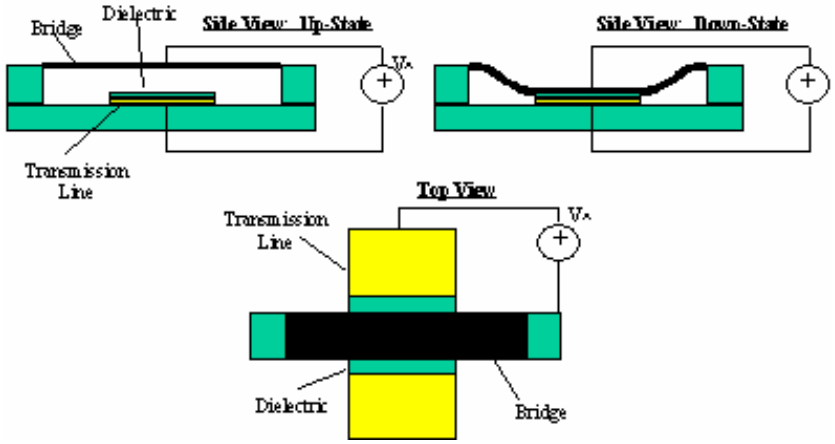


Figure 4.1: Diagram of a basic capacitive switch.

High down-state capacitance ensures high switch isolation. Increasing the bridge width and decreasing the bridge stiffness results in a large contact area in the down state, increasing the capacitance. However, the bridge width is limited by the up-state parasitic capacitance, which degrades the insertion loss of the switch. Reducing the dielectric film thickness also increases the capacitance, but the dielectric thickness is limited by the electrical breakdown strength of the insulator. One design caveat is that the signal line under the bridge and under the dielectric is thinner than the other sections of the transmission line to minimize the surface roughness of the metal and dielectric film stack under the bridge. Because films with roughness greater than a few nanometers will significantly reduce the downstate capacitance, the metal films are generally limited to a few thousand angstroms [6]. Finally, decreasing the bridge stiffness results in a larger down-state capacitance for a given actuation voltage, but it cannot be decreased indefinitely without risking stiction or adhesion failures.

Insertion loss and isolation of 0.28 dB and 35 dB, respectively, at 35 GHz have been reported [6] and capacitive switches are also capable of high-performance operation at W band (94 GHz) frequencies [9]. Capacitive switches have poor isolation at low frequencies (15 dB at 10 GHz) because the shunt impedance decreases as the signal frequency decreases. However, narrow band high isolation performance is possible at low frequencies by tuning the shunt resonance of the bridge inductance and the down-state capacitance [28]. Typical activation voltages are 30 to 50 volts, and are very sensitive to net residual strain in the clamped-clamped beam [6]. Switching speeds below 10 μs have been reported [4]. Capacitive switches are high-Q devices because they do not have any resistive loss due to a metal-metal contact, which makes well suited for tunable filter applications [4,10-13,14]. They have also been used in phase shifters [4,9]

The failure mechanism of capacitive switches is quite different than ohmic switches. Capacitive switches have larger area contacts than ohmic switches and do not have the contact degradation mechanisms associated with contact constriction resistance heating. The primary failure mechanism is charge build-up in the dielectric during operation [29,30]. Electric fields in the dielectric range from 1 – 4 MV/cm when the bridge is in the downstate, resulting in charge injection into the dielectric (typically SiN). This results in activation voltage shifts and unpredictable down-state contact behavior, depending on the magnitude and polarity of the stored charge. To date, there is no reported solution to this problem other than to use an air dielectric which limits the value of C_{on}/C_{off}.

4.2 Capacitive Switch with PECVD Oxide Dielectric

4.2.1 Switch Description

The first switch fabricated for this project consisted of an Al bridge and a PECVD deposited oxide dielectric. A diagram of this switch is shown in Figure 4.2. The switch consists of Al ground-signal-ground CPW's on an oxide passivation layer on high-R Si. The ground lines parts of the signal line are fixed to the substrate. The center section of the signal line is a suspended bridge which moves vertically. Below the signal line bridge there is a 0.2 μm thick oxide layer over a thin Al pad that is electrically connected by a shunt to the ground lines. In the as-fabricated (passing state), the capacitance between the shunt Al line and the Al signal line is small and the structure maintains an impedance close to 50 . Application of a bias between the

signal line and the ground line electrostatically attracts the signal line bridge downward. When the bias voltage exceeds the electrostatic pull-in voltage (V_{PI}) of the bridge-electrode system, the bridge is snapped down onto the thin oxide layer forming a low impedance shunt path to ground (blocking state).

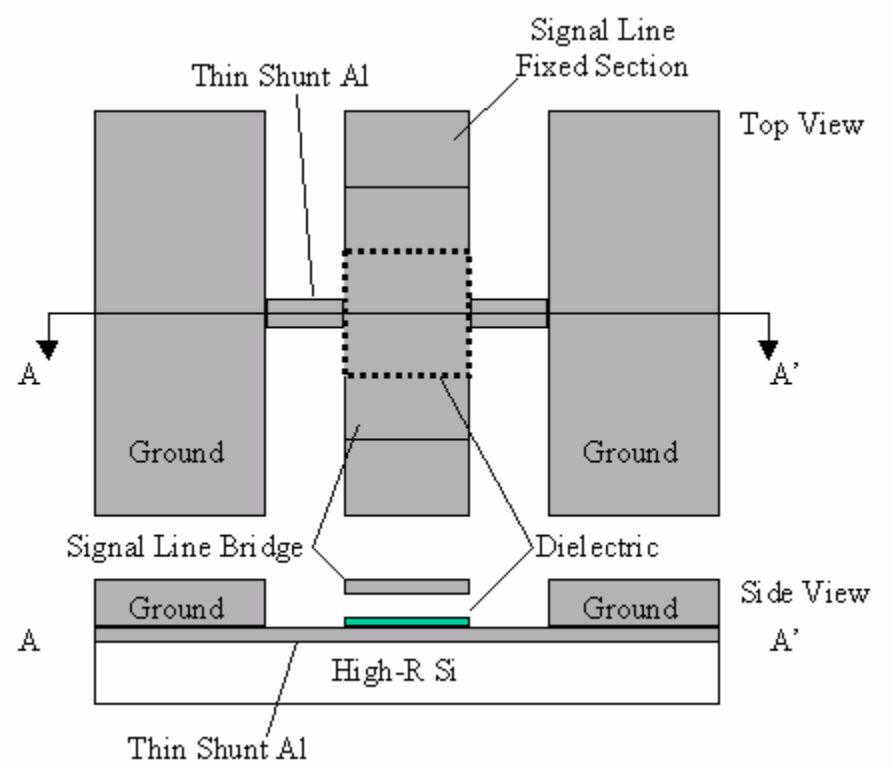


Figure. 4.2: Diagram of the capacitive switch fabricated with a PECVD oxide dielectric.

4.2.2 Fabrication Process

Process cross-sections are shown in Figure 4.3. The fabrication process begins with the growth of a 0.1 µm thick passivation oxide layer by steam oxidation on p-type 6 to 17 k ·cm Si substrates. This is followed by 0.5 µm of sputtered Al and a thin TiN capping layer. The Al layer was reactive ion etched (RIE) using a positive PR mask to form the thin metal layer under the switch dielectric. The Al layer is thin to minimize degradation of C_{on}/C_{off} due to roughness on the top surface of the metal. A 0.5 µm layer of TEOS oxide was deposited by PECVD (PETEOS) and polished back by 0.2 µm. This resulted in a planar surface and 0.3 µm of PETEOS oxide as the switch dielectric. A thin layer of TiN was sputtered over the top of the oxide in order to protect the switch dielectric from the HF-based release chemistry later in the process. Holes were patterned by RIE in the oxide/TiN layer stack in order to make electrical contact to the bottom Al layer. A 3 µm PETEOS sacrificial layer was deposited and holes were RIE etched to access the bottom thin Al layer. A 0.5 µm layer of Al was sputter deposited to make contact to the bottom Al layer and for form part of the mechanical layer. This was followed by another 2 µm oxide deposition. The oxide was blanket etched back for form a planar trench fill. Another 2 µm of sputtered Al was deposited to form the remainder of the

mechanical layer. After RIE etching with a PR mask, the PR was removed and the sacrificial oxide layer was removed with a HF-based solution. The TiN layer was designed to protect the switch dielectric during this process. After the sacrificial layer was removed, this layer was removed by H_2O_2. An optical micrograph of the completed switch is shown in the left side of Figure 4.4.

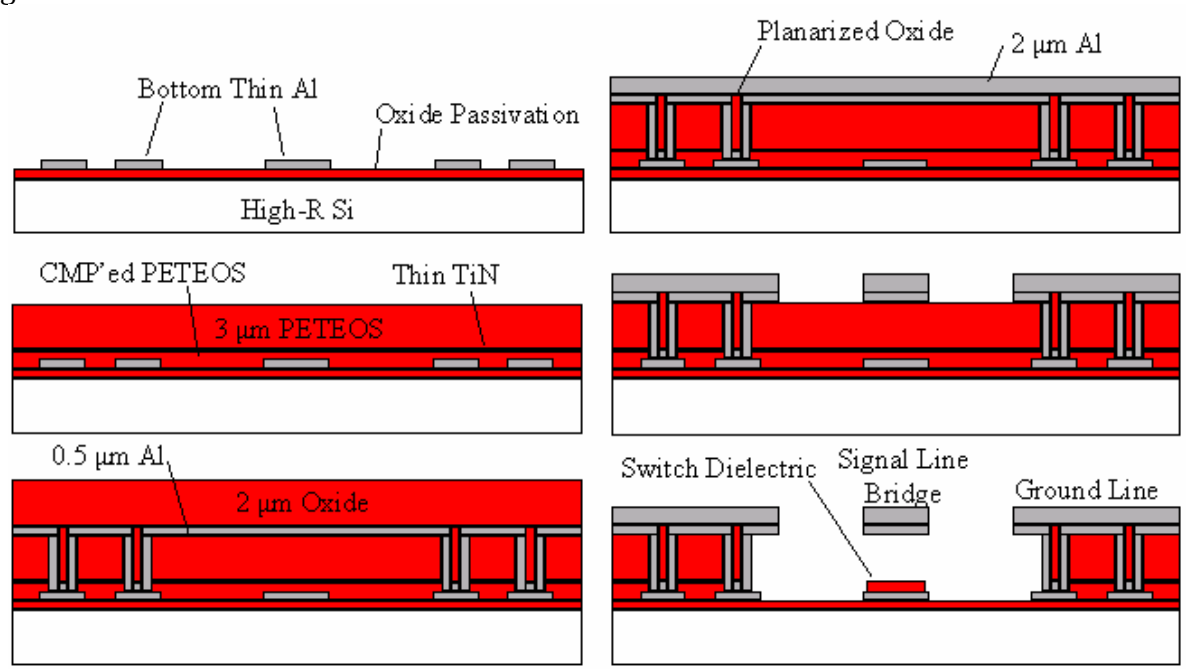


Figure 4.3: Capacitive switch process cross-sections

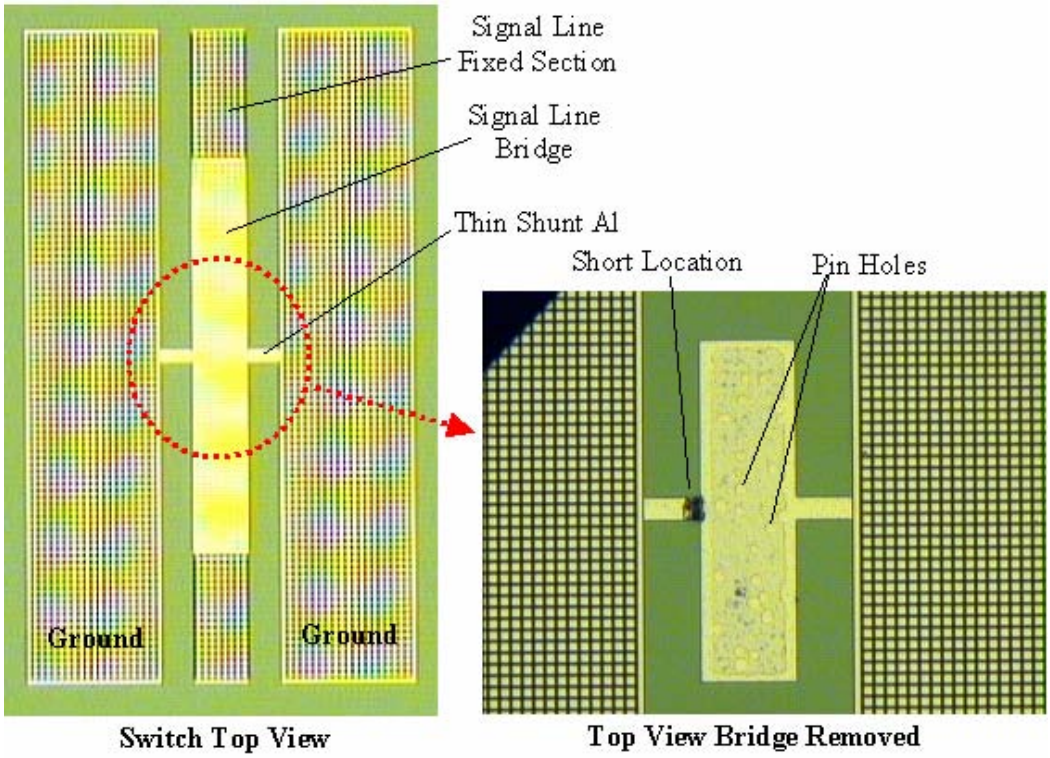


Figure 4.4: Optical micrographs of the completed switch (left) and a close up of a switch that has the switch bridge removed to reveal pinholes in the dielectric.

4.2.3 Results and Discussion

The switches were tested in bare wafer form on a Cascade Summit 9102 manual RF probe station with 150 µm ground-signal-ground (GSG) probes. An Advantest TR6143 0 – 110V DC Voltage Current Source/Monitor was used to actuation the switch. S-parameters were measured by a HP8510C Network Analyzer (VNA) with a 45 MHz to 26.5 GHz 8515A S-Parameter Test Set. 100 V bias T's were used as blocking capacitors to protect the VNA from the high activation voltages that could be applied to the VNA in the event that the switch dielectric shorts. The test setup was contained within a 8' x 12' class-100 soft-walled clean room. Movement of the switches was monitored by observing both the S-parameter data and the reflected signal from a pen laser mounted above the probe station. The change in reflected laser light was observed on a monitor that was connected to an AZoom2 microscope on the RF probe station.

The passing-state S-parameters measurements are shown in Figures 4.5 and 4.6, and the simulated results using commercially available method-of-moments (MOM) simulation software are shown in Appendix A1. The best-case S_{21} measurement is better than 0.5 dB to 22 GHz and the best case S_{11} is better than 30 dB to 26.5 GHz. The considerable device-to-device variability observed in S_{11} and S_{21} was traced to high impedance at the probe contacts. Since the device transmission lines are made of Al, consistent contact by the GSG probes was extremely difficult even when the probes were repeatedly "scrubbed" on the Al lines. This proved to be a persistent problem with all of our device measurements. The simulated passing-state S_{21} results of switches with three different electrode areas are significantly better than our measurements. Since the tested switches were observed to be mechanically in tact, we would expect the performance of the switches to closely match the simulation if it were not for the poor contact to the GSG probes.

When we attempted to snap the switches down to measure the blocking-state S-parameters, the bridges of several switches shorted to the thin Al shorting line and stuck down. This was traced to a process problem with the dielectric. The switch dielectric (oxide) appears to have been attacked by the HF solution during the release process due to pinholes present in the thin TiN protective layer. The right side of Figure 4.4 shows where the signal line of one of the switches has been removed in the lab by a dc probe. The dark spot in the figure shows where the Al signal line bridge was shorted to the bottom thin Al film on this particular switch by tipping slightly on its side. The blue spot is incompletely removed TiN that was left over after the H_2O_2 etch. This process could potentially be improved by substituting a thicker layer of W for the thin TiN protective layer to prevent the oxide from being attacked during the release process. This would not significantly impact the existing process because W could be removed in H_2O_2 following the sacrificial layer etch.

4.2.4 Conclusions

Capacitive switches were fabricated using Al as the transmission line metal and the mechanical metal, and PECVD deposited oxide was used as the switch dielectric. The switch performed well in the passing state, subject to observed measurement variability due to high resistance between the probes and the transmission lines that was caused by the Al native oxide on the transmission lines. The switches were mechanically functional when they were snapped down, however the switch bridge shorted to the shunt metal because of pin holes in the PECVD

oxide dielectric. One potential improvement to the process would be to substitute W for TiN as the protective layer for the oxide.

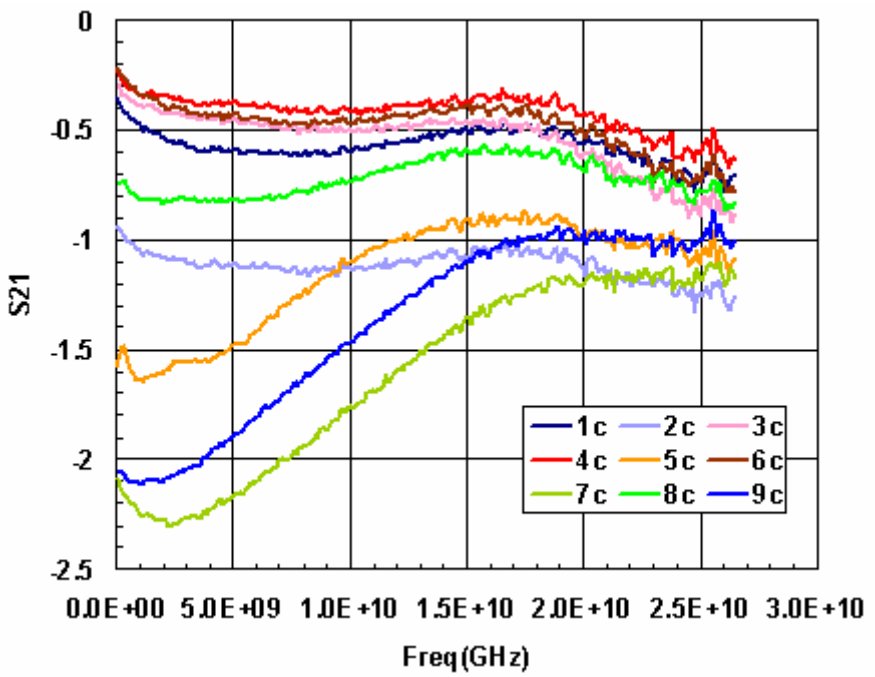


Figure 4.5: Measured S-parameters of the switch in the up-state

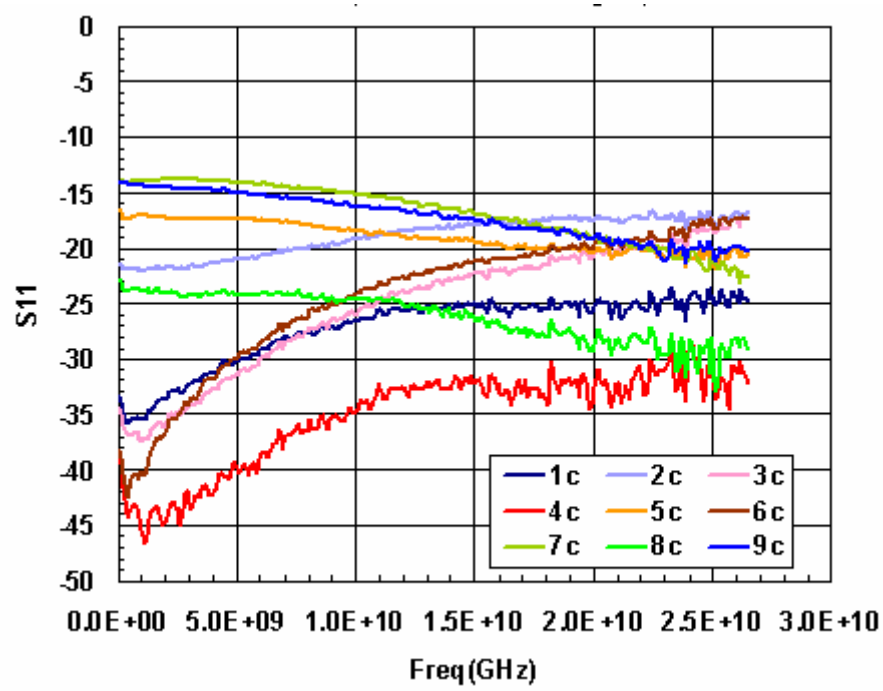


Figure 4.6: Return loss of upstate switches

4.3 Capacitive Switch with W-Al Dielectric

4.3.1 Switch Description

Capacitive switches are typically fabricated with a thin dielectric (0.1 – 0.3 μm thick) to increase C_{on}/C_{off}, as described in Section 4.1 and in the previous section. In order to increase the downstate capacitance, and thus to increase C_{on}/C_{off}, we recently fabricated a capacitive switch that uses the native oxides of W and Al as the switch dielectric when. The switch (Figure 4.7) consists of a suspended Al signal line bridge above a W shorting bar that connects the two CPW ground lines. Separate actuation electrodes pull the signal line down into contact with the shorting bar. The thin native oxides of Al and W create a low impedance path between the signal line and the ground lines through the shorting bar when the switch is in the downstate. The use of separate actuation electrodes prevents the thin native oxides of Al and W from breaking down when the switch is in the downstate. MOM simulations of the switch in the downstate are shown in Appendix A2.

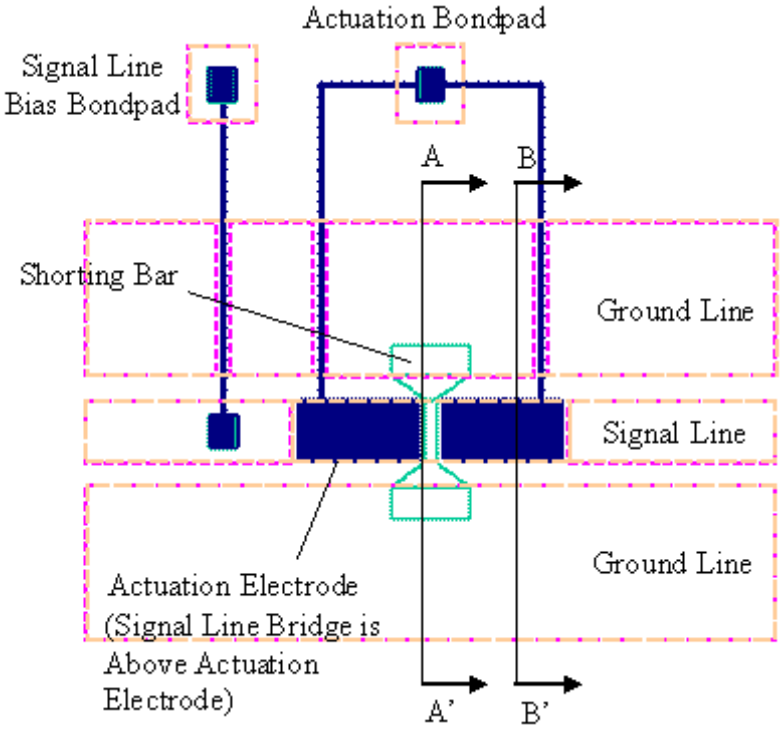


Figure 4.7: Diagram of the capacitive switch that uses native oxide layers of Al and W as the switch dielectric.

4.3.2 Fabrication Process

Process diagrams are shown in Figure 4.8 for cross-sections A-A' and B-B' in Figure 4.7. A 0.3 μm passivation layer of Si-rich SiN (LS SiN) is LPCVD deposited on 6 to 17 k ·cm high-R Si substrates. A thin TiN layer is then deposited and RIE etched to form the signal line bias and the actuation electrodes. This layer has an approximate resistance of 100 /square. 0.3 μm of PECVD SiN is deposited over the TiN. Then, TiN/W/TiN layer (25 nm/0.3 μm/25nm) is

deposited and RIE etched with a positive PR pattern to form the shorting bar. A sacrificial layer of 2 μm of PECVD TEOS oxide is deposited and CMP planarized to an approximate final thickness of 1.5 μm. 1.2 μm wide trenches are then etched into the PECVD oxide layer, followed by the deposition of 0.8 μm of CVD W on a TiN adhesion layer. The W layer is polished back to the sacrificial oxide layer resulting in the formation of W supports for the ground lines. Al is deposited to a thickness of 1.5 μm and etched back to form the signal and ground lines. The final release steps consist of a buffered oxide etch to remove the sacrificial PECVD oxide layer and subsequent dry etch to remove the thin TiN layer over the 0.3 μm W shorting bar. The completed switch is shown in Figure 4.9.

Some devices were functional after release process, however two process issues were responsible for a large number of failures. First, the trench etch through the sacrificial PECVD oxide layer was supposed to stop on the shorting bar, however the etch went through the 0.3 μm W layer and into the underlying PECVD SiN layer. This resulted in a small contact area between the TiN adhesion layer used for the W molded supports and the W shorting bar. This section was exposed during the dry etch portion of the release process that was used to remove the TiN layer above the W shorting bar, and was etched to form an open circuit between the molded supports and the shorting bar. The second process issue was delaminating of the upper PECVD SiN layer, as shown in Figure 4.10. This was traced to a residual organic film that was left over after etching the TiN actuation electrode layer. The result of this film was poor adhesion between the TiN layer and the overlying PECVD SiN layer.

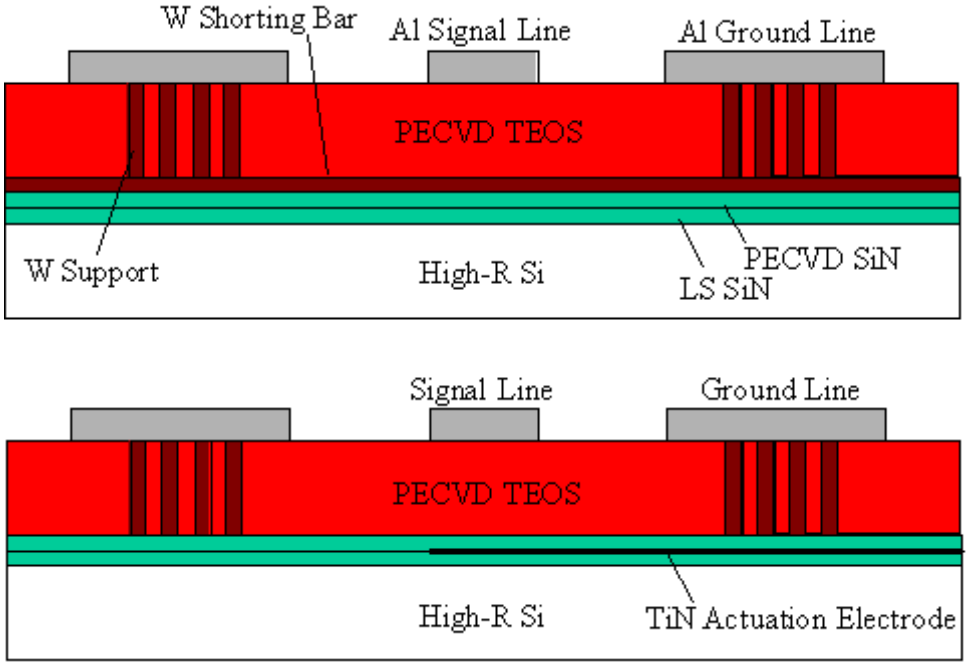


Figure 4.8: Cross-sections of the ohmic shunt switch process. The upper cross-section is for A-A' and the lower cross-section is for B-B' shown in Figure 4.7.

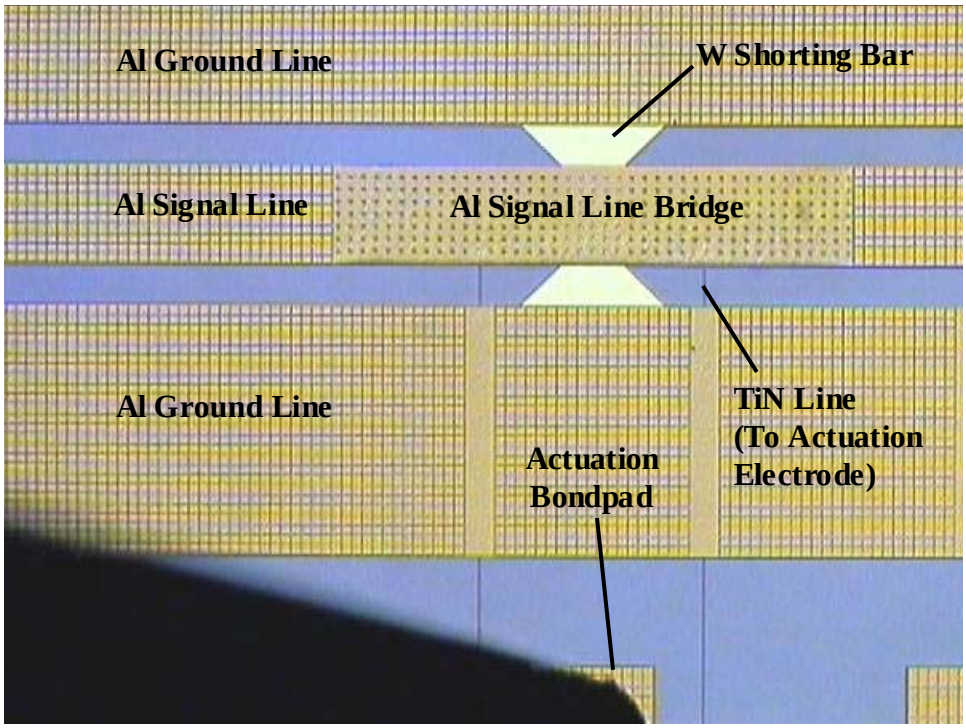


Figure 4.9: Optical micrograph of the completed capacitive switch that uses Al and W native oxides as the switch dielectric.

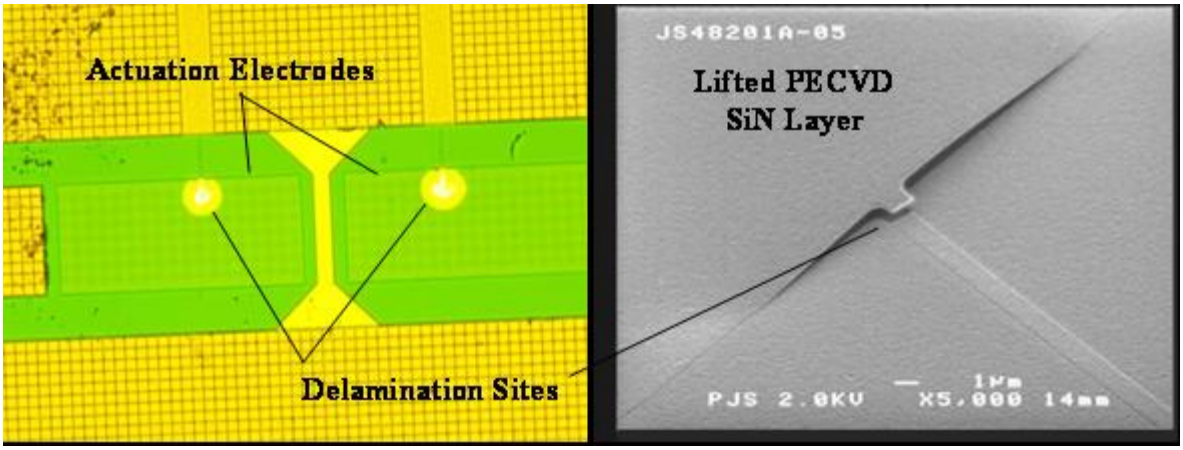


Figure 4.10: Images of the delamination failure points due to poor adhesion of the TiN biasing layer to the PECVD SiN layer.

4.3.3 Results and Discussion

The switches were tested in bare die form on the same test setup described in Section 4.2.3. A probe was placed on the actuation bondpad to actuate the switch, and the signal line of the GSG probes was set to dc ground. S-parameters were measured for both the up-state and down-state. A CPW transmission line test structure was measured first and this data shown in Figure 4.11. S_{11} is greater than 20 dB from 0 to 26.5 GHz indicating a reasonable match to 50 . S_{21} is 0.13 to 0.14 dB/mm at 10 GHz. This value is high is possibly caused by the presence of the W

molded supports under the Al in the ground lines which increases the series resistance of the transmission lines. It is also possible that some loss is contributed by the lack of a high-quality oxide passivation layer between the LS SiN and the high-R Si substrate, as discussed in Section 2.3.1. The use of W molded supports simplifies the process over that of the PECVD SiN capacitive switch process discussed in Section 4.2.2, however it adds to the switch loss and would be better if it were eliminated from the process.

Deformation of the signal line bridge was observed due to residual stress in the Al film. Scanning white light interferometry measurements showed that the Al signal line was 1.1 µm above the substrate, instead of the expected 1.5 µm separation after the release process. The bridge was also curved down along its length indicating the presence of tensile stress in the film. The film stress did not prevent the bridges from actuating, however this deflection was responsible for increased loading on the CPW line which in turn increased open-state insertion loss.

While testing the switches we noticed behavior indicative of dielectric charging in the PECVD TEOS oxide layer above the TiN actuation electrodes. This was seen in the S-parameter behavior after the switch bridge had been snapped down. As the S-parameters were swept from low frequency to high frequency, the switch isolation decreased (S_{21} decreased in magnitude) erratically. This behavior has been correlated in our lab with charge build-up in capacitive switches that screens the electric field between the actuation electrode and the switch bridge. We suspect that when the signal line bridge snaps down to the W shorting bar, part of the bridge snaps down over the region just above the TiN actuation electrodes. This creates a high electric field between the switch bridge and the TiN actuation electrodes and injects charge into the dielectric. As a result of this charge build-up, bipolar waveforms were used to actuate the switches. S-parameter measurements are shown in Figures 4.12 and 4.13.

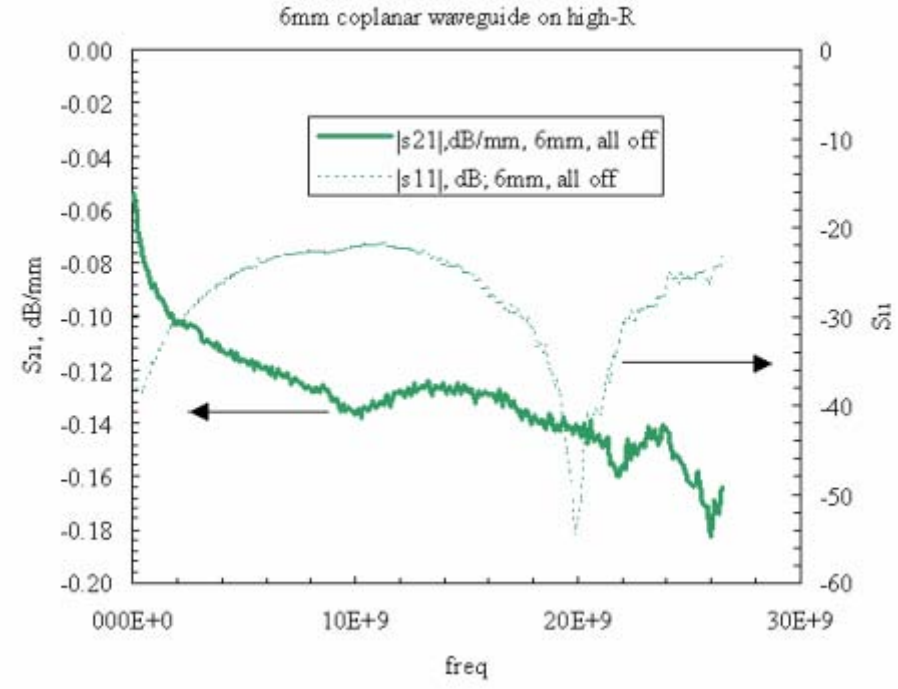


Figure 4.11: CPW through-line transmission line S-parameter measurements showing a good impedance match to 50 and higher-than-expected loss.

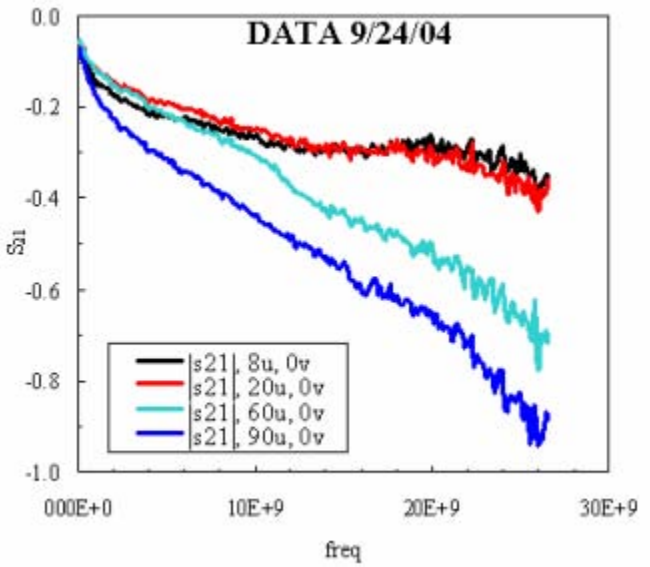


Figure 4.12: Up-state S-parameters of the capacitive switch that uses native oxide layers of Al and W as the switch dielectric.

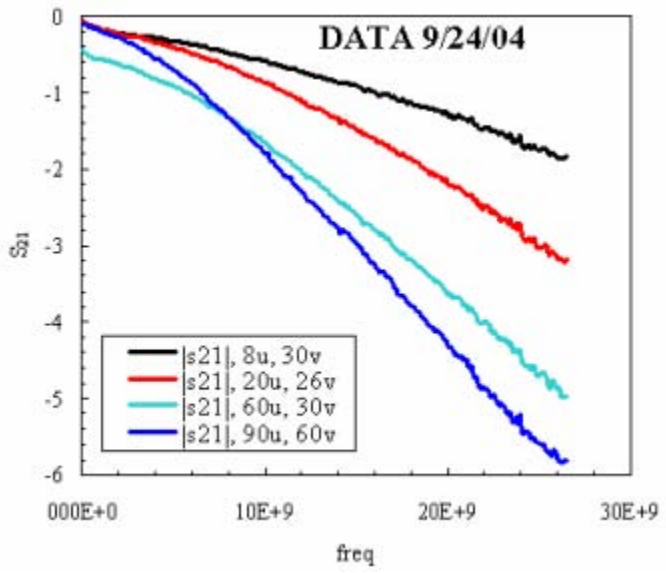


Figure 4.13: Down-state S-parameters of the capacitive switch that uses native oxide layers of Al and W as the switch dielectric.

The measured downstate isolation is not as high as the simulated values. We propose two possible explanations for the decreased performance. First, the actuation electrodes are separated from the capacitor electrodes which makes it very difficult to maintain an intimate contact between the bridge and the shorting bar (Al and W) when the switch is in the downstate. We believe this is why the downstate capacitances are lower than expected. Second, the expected resistances of the shorting bars are 0.2 to 4 based on bulk W values, however the measured values varied between 1 and 10 . It is well known that thin film resistances are higher than

bulk values and there is an additional uncertainty associated with measuring resistances through Al bondpads due to the native oxide layer, as discussed earlier in Section 4.2.3. This level of resistance will lower the downstate isolation because it increases the impedance to ground of the capacitive switch, however this alone does not account for the low measured isolation values.

We were unable to measure the resistance between the actuation electrodes and the actuation bondpad, however the bias line (see Figure 4.7) was measured to be 58 k . Based on this result and the similar geometries between the bias line and the actuation line, we would expect the resistance between the actuation bondpad and the actuation electrodes to be several 10's of k and not have any significant affect on the upstate RF performance.

4.3.4 Conclusions

A capacitive switch was designed and fabricated that relied on the native oxides of W and Al to form a low impedance path to ground in order to increase the isolation over capacitive switches with thin deposited dielectrics. The structures were successfully released and tested, however the downstate isolation was lower than expected due potentially to the lack of intimate contact between the Al and W native oxides and to the high shunt resistance of the W shorting bar. The reported process problems are surmountable, and with future runs we are confident that these problems would be solved. Dielectric charging is a persistent problem due to the presence of the PECVD SiN between the actuation electrodes and the switch bridge when it is in the down-state. Elimination of this dielectric would solve the problem.

5.0 Ohmic Switch Development

5.1 Ohmic Switch Technology

RF MEMS ohmic switches use an air gap for high isolation and a metal-to-metal contact to pass signals. A diagram of a generic ohmic switch is shown on the left side of Figure 4.14 that is similar to early work done by Yao, et. al. [31]. The switch is shown in the open (or blocking) state. It is a cantilevered structure consisting of two metal plates attached by an insulating layer. The metal plate over the ground plane serves as the top actuation electrode and the other plate is the contact region while the insulating layer electrically isolates the two. The contact region is suspended over a gap in a CPW signal line. Incident microwave signals are reflected by the parallel combination of the coupling capacitance between the contact region and the signal line and the coupling capacitance of the signal line gap. A low coupling capacitance results in high signal isolation. When a voltage exceeding the electrostatic pull-in limit is applied between the top electrode and the CPW ground line, the switch is snapped down. The contact region shorts the signal line gap and allows signals to propagate. Low contact resistance between the switch contacts and the CPW signal line results in low signal loss. Ohmic switches are used in either a series or shunt configuration [4], which blocks signals by forming a low-impedance path to ground when the switch is closed, as shown on the right side of Figure 4.14.

Important design parameters include isolation, insertion loss, return loss, switching speed, actuation voltage, and compactness [4,31]. High isolation is accomplished by minimizing the open-state coupling capacitances through the contacts and across the signal line gap. Increasing the signal line gap and narrowing the transmission lines by tapering them as they approach the switch contacts minimizes the capacitance across the signal line gap but also tends to degrade the

return loss. Additionally, small diameter contacts minimize contact coupling. To achieve low insertion loss, contact forces in the high 10's to 100's of N are necessary, requiring high activation voltages or high actuation capacitances [32-34]. There is a practical limit on the actuation capacitance that is dictated by space constraints of the circuit application. Larger switches can also degrade return loss at higher frequencies. High switching speeds are obtained with mechanically stiff springs, high activation voltages, and small gaps between the contacts and the signal line. A decrease in the latter will decrease isolation.

Outstanding switch performance has been demonstrated with less than 0.2 dB insertion loss and 27 to 30 dB of isolation from 0 to 40 GHz [5,7]. Typical DC contact resistance measurements are 1 [7], and open-state coupling capacitances as low as 2 fF have been reported [7]. Switching speeds ranging from 3 to 6 s have been reported [4,16]. Most switches are electrostatically actuated, which results in sub- W power dissipation levels, and cold switching cycle lifetimes are approaching 100 billion.

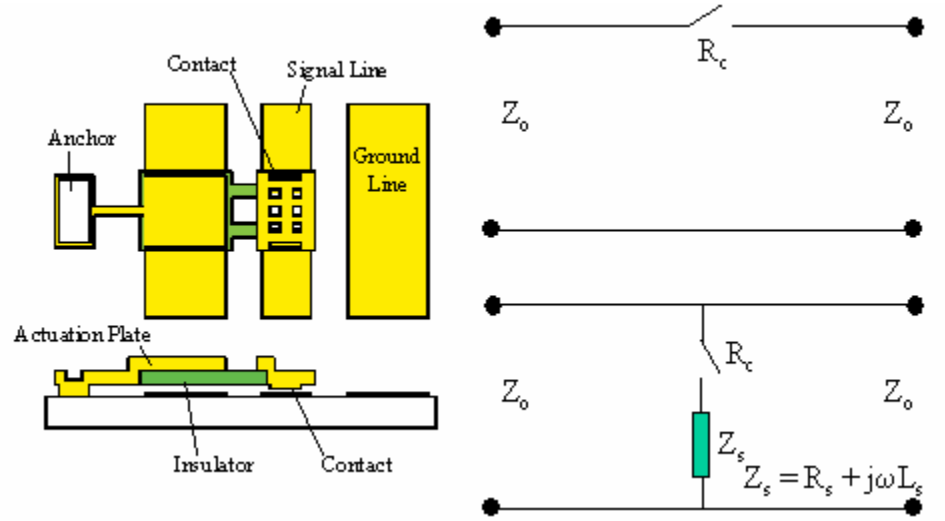


Figure 5.1: A diagram of a generic ohmic switch and series and shunt circuit configurations.

5.2 Ohmic Shunt Switch

5.2.1 Device Description

One of the fundamental issues associated with capacitive switches is charge storage in the capacitor dielectric due to the high electric fields across the dielectric that arise when the switch is in the downstate. One way to circumvent this, and still attain a capacitive shunt from the signal line to the ground line, is to fabricate a metal-metal contact that is connected in series to a capacitor to ground. To test this concept, a 'shorted' device was fabricated on high-R Si and tested. The device was fabricated with W bridges suspended above a CPW. The bridge anchors are capacitively coupled to the ground lines of the CPW by a 0.6 μm SiN film. The shorted test device was fabricated such that the W bridges were directly connected to the signal line. S-parameters for these devices were tested, resulting in >35 dB of isolation from 10 - 26.5 GHz for the best devices (Figure 5.2).

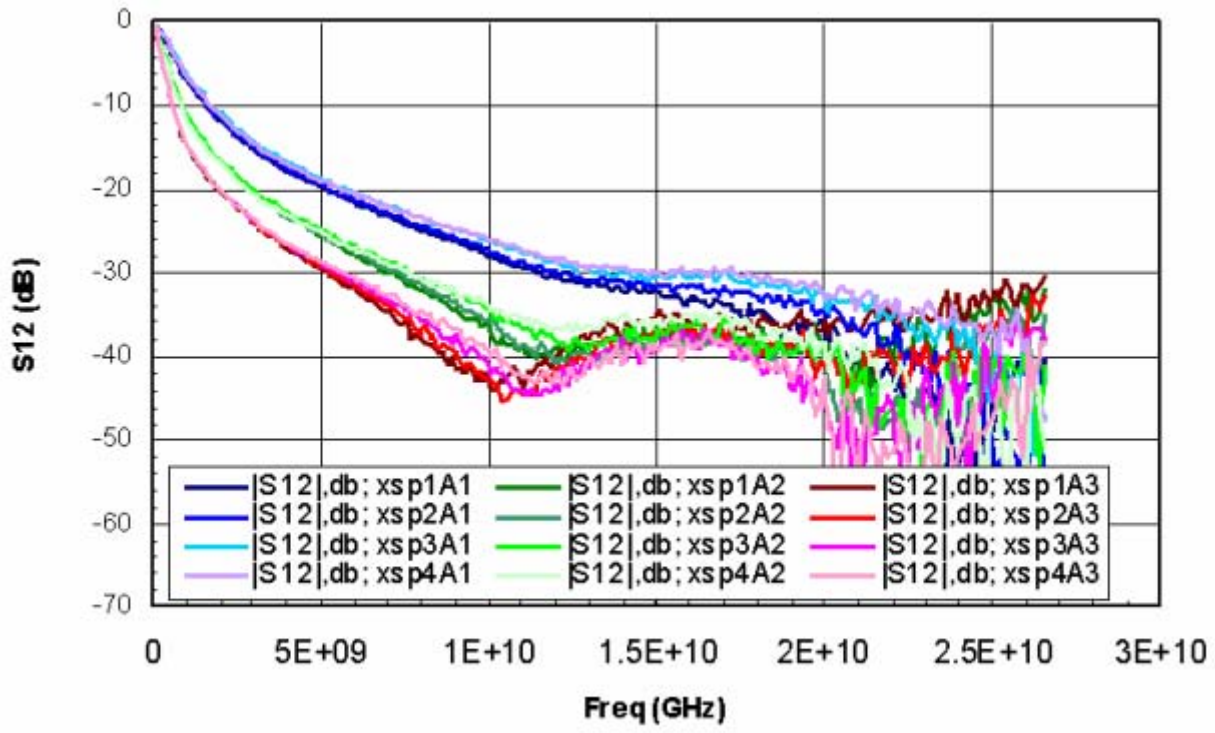


Figure 5.2: Shorted as-fabricated shunt ohmic switch measurements.

A diagram of the device is shown in Figure 5.3. The switch is an aluminum (Al) bridge that is suspended approximately 2 μm above a tungsten (W) bottom metal contact. The bottom contact is connected to a thin Al shunt metal that is connected to ground by a large capacitor under the CPW ground line. The bridge is also the signal line of a co-planar waveguide (CPW) transmission line. In the up-state (passing state), there is an air gap between the bridge and the contact metal. Incident microwave signals propagate through the switch with minimal reflection because there is a high impedance path to ground. When a bias voltage that exceeds the pull-in voltage is applied between the substrate and the signal line, the bridge is snapped down into contact with the underlying contact metal, forming a low impedance path to ground through the large capacitor, and reflecting incident signals. This is the downstate (blocking state). This switch differs from the capacitive switch described in Section 4.3 because is relies on a high enough contact force such that the Al-W contact is ohmic rather than capacitive.

5.2.2 Process Description

Process diagrams are shown in Figure 5.4. A passivation layer of 0.6 m of oxide grown by steam oxidation is deposited on 6", p-type, high-R Si wafers with a resistivity of 6 – 17 k cm. This is followed by 0.1 μm of LPCVD LS SiN and the sputter deposition and etch of 0.2 μm of Al to form the shorting electrical line. A layer of 0.5 μm of PECVD TEOS oxide is deposited and polished back to a thickness of 0.3 μm and another 0.6 μm of PECVD SiN is deposited over this. The combined stack of LS SiN and PECVD oxide forms the shunt dielectric under the ground lines of the switch. A 1 μm sacrificial layer of PECVD TEOS oxide is deposited over the LS SiN layer and narrow trenches are etched into the oxide down to the LS SiN. A 0.8 μm layer

of W is deposited and polished back to the sacrificial oxide to form W-fill trenches. These act as the bottom contact of the shunt switch. Another 1 μm layer of PECVD TEOS oxide is deposited to form the top layer of the sacrificial layer (2 μm total thickness). Another series of trenches are etch down to the PECVD SiN layer, filled with W, and polished back to form supports for the CPW ground lines. The devices are released by wet etching the PECVD oxide layers. A completed device is shown in Figure 5.5.

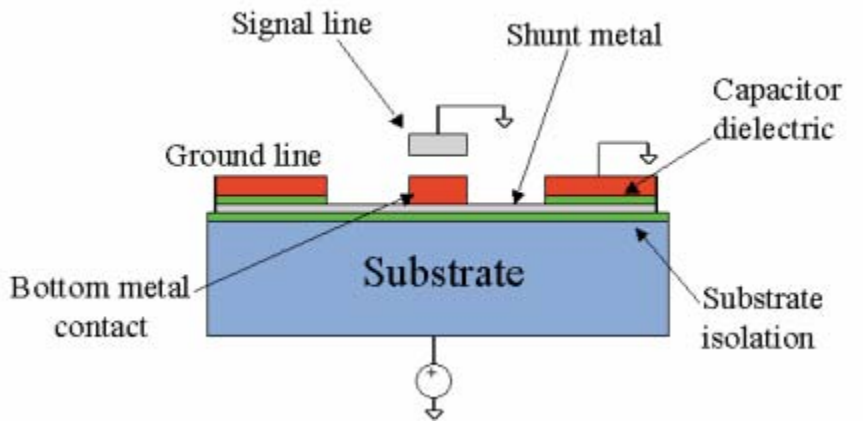


Figure 5.3: A diagram of a cross-section of the ohmic shunt switch.

5.2.3 Results and Discussion

S-parameters measurements for the switch in the up-state and the down-state are shown in Figure 5.6. The plot on the left shows the insertion loss and isolation of a typical switch. The upstate insertion loss is 2dB at 26.5 GHz. The insertion loss is substantial and is due to the large open-state capacitive coupling between the suspended bridge and ground. More insertion loss curves are shown in the plot on the right side of Figure 5.6. Insertion loss values range from 0.4 to 1.5 dB at 26.5 GHz. The upstate capacitive coupling will be reduced in future designs, as discussed later. The isolation curve in the plot on the left of Figure 5.6 is interesting, as it has a maximum value of 25 dB at 7.5 GHz and then decreases to 20 dB at 26.5 GHz. This is contrasted to the data of the switch test structures in Figure 5.2 which shows isolation values of 32 dB at 26.5 GHz. The switches and test structures have nominally the same geometry which suggests that the switch has a significant component of series inductance and resistance to ground on that is not present on the test structures. The increase series resistance can be accounted for by the contact resistance of the Al-W metal-metal contact, however we have not yet accounted for the source of inductance.

We observed that when the switches were actuated down, the switch isolation did not increase to the values shown in Figure 5.6 until a voltage that was much greater than the pull-in voltage was applied. This is shown in Figure 5.7 where an LCR meter was used to measure the shunt capacitance as a function of the applied actuation voltage. The left side of Figure 5.7 shows that the switches achieved very high shunt capacitance values, ranging from approximately 8-12 pF, at actuation voltages greater than 60V. However, most switches were observed under the microscope to snap down between 40V and 60V. This was also verified by observation under a scanning white light interferometer as the switches were actuated. The plot on the right of Figure 5.7 is the same C-V plot that has been rescaled to show smaller changes in capacitance. The arrows in the plot identify increases in the shunt capacitance where the

switches were observed to snap down. We suspect that this initial incremental change is due to native oxides in the W-Al metal-metal contact that prevent a metal-metal contact at the forces applied when the switches are initially pulled down. As the voltage is increased to 60 V, the contact becomes ohmic resulting in a sudden increase in the shunt capacitance to ground.

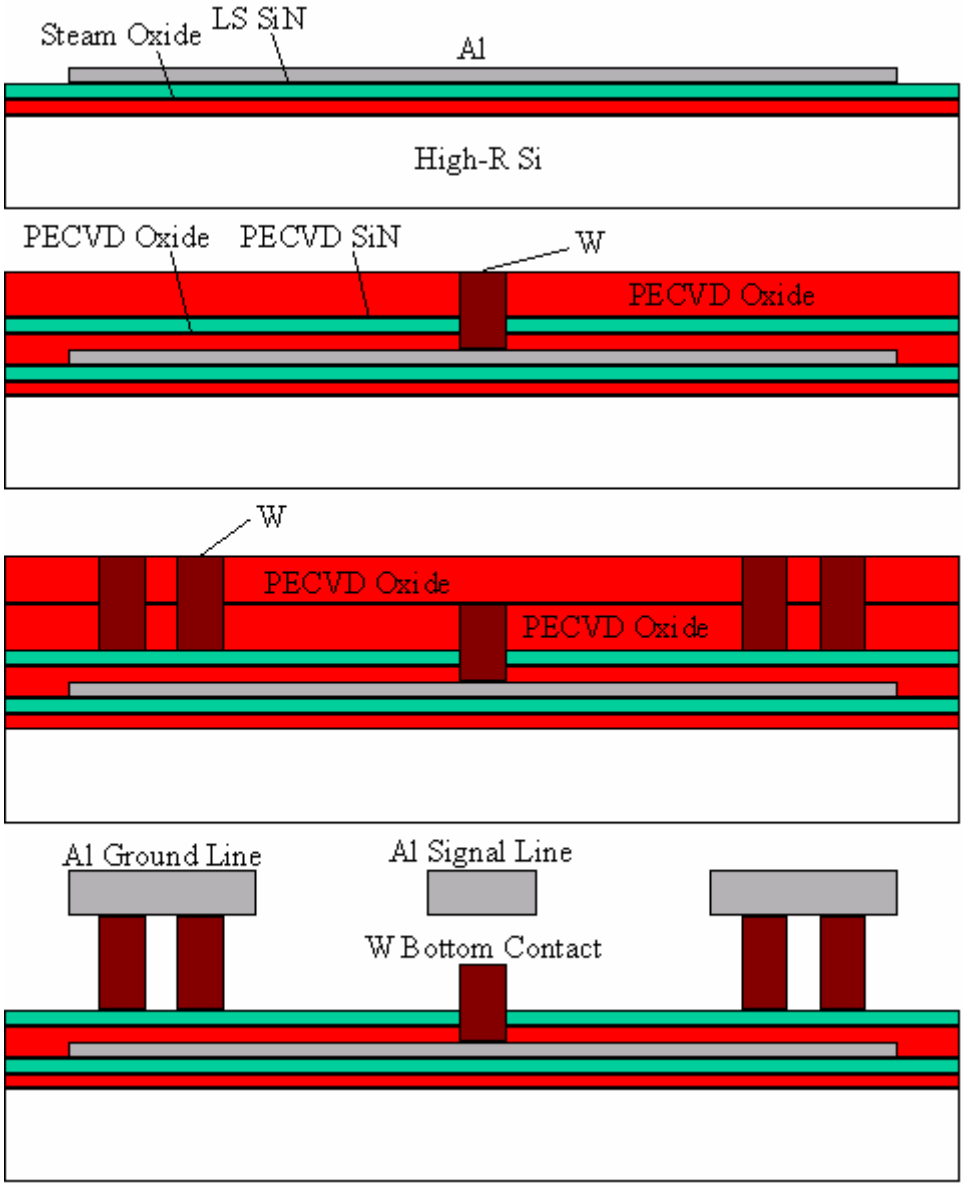


Figure 5.4: Ohmic shunt switch fabrication process.

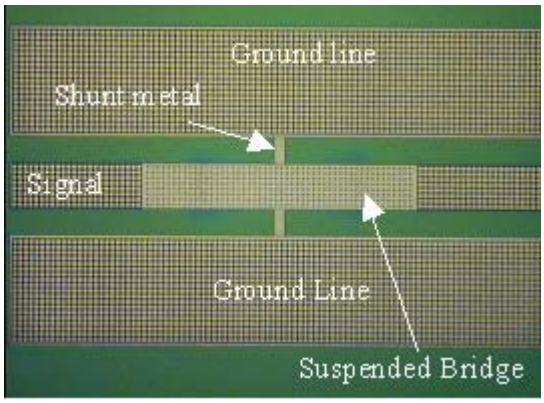


Figure 5.5: Completed ohmic shunt switch

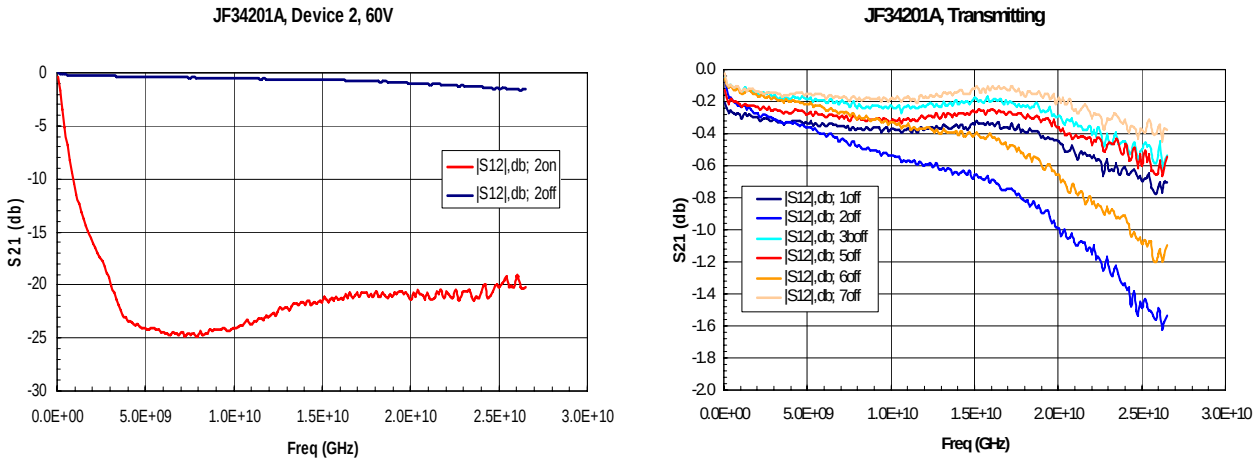


Figure 5.6: Measured upstate and downstate S-parameters of the ohmic shunt switch.

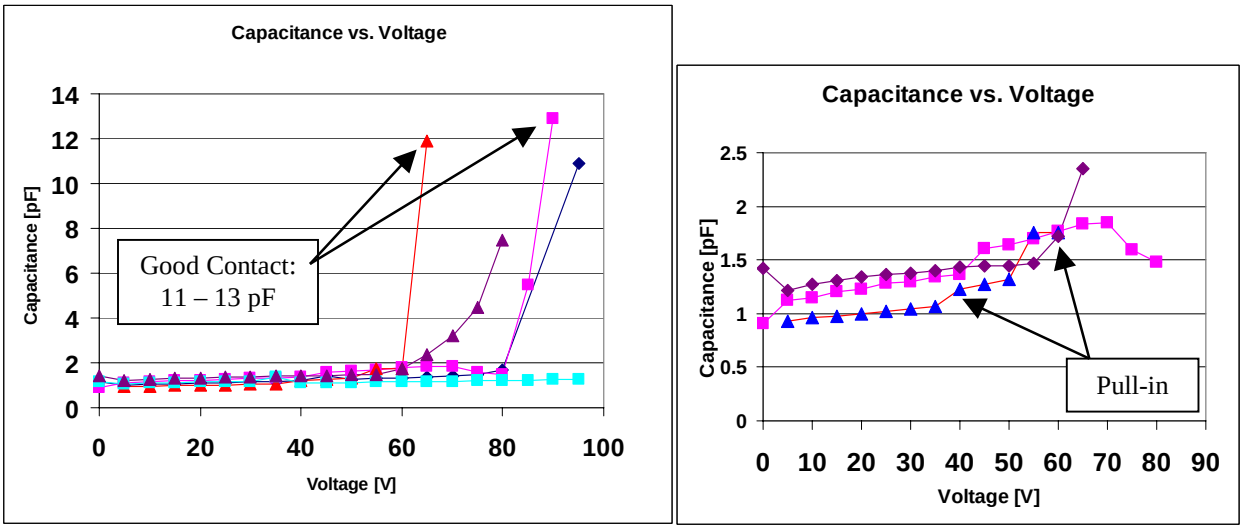


Figure 5.7: Measurements with an LCR meter of the shunt capacitance of the ohmic shunt switch.

5.2.4 Conclusions

A shunt ohmic switch with a Al-W metal-metal contact was fabricated and characterized. High isolation was achieved at low signal frequencies when the switch was in the downstate due to the large shunt capacitance in series with the metal-metal contact. Upstate performance was limited by the capacitive coupling of the bridge to the signal line which can be reduced in future designs. In order to achieve a high enough contact force to form an ohmic contact between the Al and W films, an applied voltage of approximately 20 volts above the pull-in voltage was required.

6.0 Conclusions

A variety of SiN and oxide passivation layers for high-R Si were explored by comparing measurements of the insertion loss of CPW transmission lines on these films. We found that the highest quality films resulted from the growth of native oxide films, deposited by either steam oxidation or dry O_2, and from the deposition of oxide films in the Epic and Integrity systems. These films resulted in low fixed charge and interface states that were found to increase the propagation attenuation of microwave signals by increasing the free charge concentration in the substrate of the high-R Si. TEOS deposited in the VTR systems was found to have the poorest performance because of the presence of high levels fixed charge and interface states.

We have successfully fabricated and demonstrated a number of RF MEMS switches and test structures on high-R Si substrates in the MDL; a radiation-hardened microelectronics facility at Sandia National Laboratories. Both capacitive and ohmic switches have been demonstrated and novel bulk and surface micromachined tungsten processes have been developed. By using the toolset available in a 6” CMOS line, we hope to drive the cost-per-device and circuit of this technology down without sacrificing microwave circuit performance given the constraints of the limited material set available to us.

The limited material set presents a formidable challenge to fabricating high performance RF MEMS devices. We found that it was easier to fabricate capacitive switches than ohmic switches in the MDL. The materials set makes it difficult to integrate the necessary contact metals that are needed to fabricate high performance, high reliability ohmic switches which generally require low resistance, noble metal-metal contacts. On the other hand, capacitive switches are easier to develop since PECVD and LPCVD films can be used as the switch dielectrics and are readily available in a CMOS facility. Post processing of contact metals in a facility outside of the MDL is possible, however this tends to have two problems. First, it is very difficult to deposit films on anything but the top surface and sidewalls of MEMS structures. This limits the types of ohmic switches to laterally actuating switches. Second, processing outside of the MDL negates the advantages of using the volume processing CMOS facility in the first place. We found that in either case, the use of aluminum was adequate to produce low-loss transmission lines, although wafer-level testing was difficult due to the aluminum oxide native layer that caused high contact resistance between the probes and the transmission lines.

The switches in this work were all fabricated with CPW transmission line technology that has significantly higher metal losses than microstrip technology. If high performance reconfigurable MEMS-based microwave circuits are to be developed in the future, a microstrip process will have to be developed. This will involve the thinning of Si wafers to achieve low-loss 50

transmission lines, and the development of a through-wafer via process. An alternative technology that was shown to be low loss was stripline technology. The fabrication of reconfigurable circuits in stripline technology has not been extensively explored, if at all. Although this technology could achieve unprecedented performance in terms of loss compared to CPW and MS technologies, the integration of MEMS and stripline transmission lines is challenging and begs the question of whether a CMOS facility is the right place to be fabricating this type of technology. However, three-dimensional micromachining as a general method of achieving compact, high-performance reconfigurable circuits is worth considering, and the machining of Si by wet and dry processes is attractive for this type of technology.

The use of chemical mechanical polishing in the fabrication of RF MEMS switches had a compelling advantage in terms of creating complex, multilevel mechanical devices by increasing the level of process precision without having to worry about topography. This could be very attractive in the development of air-gap capacitive switches; a topic that we did not explore. The capability to deposit uniform thin films combined with chemical mechanical polishing could result in the fabrication of an air-gap switch with a much higher downstate capacitance than is possible by other means. If such a switch could be developed, this would eliminate the reliability problems associated with dielectric charging of capacitive switches.

The molded tungsten processes developed in part by this LDRD present interesting methods of fabricating complex mechanical structures with a high quality mechanical film that is otherwise unusable due to its high levels of as-deposited stress. The structures fabricated for this project were useful for applications at low frequencies where the size and loss of the tungsten lines did not significantly detract from the switch performance. A novel latching switch was demonstrated in this LDRD.

7.0 References

[1] E. R. Brown, "RF-MEMS Switches for Reconfigurable Integrated Circuits," IEEE Trans. on Microwave Theory and Techniques, Vol. 46, No. 11, Nov. 1998, pp. 1868 – 1880.

[2] B. R. Norvell, R. J. Hancock, J. K. Smith, M. L. Pugh, S. W. Theis, and J. Kviatkofsky, "Micro Electro Mechanical Switch (MEMS) Technology Applied to Electronically Scanned Arrays for Space Based Radar," Proc. IEEE Aerospace Conf., March 6, 1999, pp. 239-247.

[3] J. J. Yao, "RF MEMS from a device perspective," J. Micromech. Microeng., 10 (2000), pp. R9-R38.

[4] G. M. Rebeiz, *RF MEMS Theory, Design, and Technology*, 2003, John Wiley & Sons.

[5] D. Hyman, A. Schmitz, B. Warneke, T. Y. Hsu, J. Lam, J. Brown, J. Schaffner, A. Walston, R. Y. Loo, G. L. Tangonan, M. Mehregany, and J. Lee, "GaAs-compatible surface micromachined RF MEMS switches," Elec. Lett., 4th Feb., 1999, Vol. 35, No. 3.

[6] Z. J. Yao, S. Chen, S. Eschelman, D. Denniston, and C. Goldsmith, "Micromachined Low-Loss Microwave Switches," Journal of Microelectromechanical Systems, Vol. 8, No. 2, June 1999, pp. 129-134.

[7] R. E. Mihailovich, M. Kim, J. B. Hacker, E. A. Sovero, J. Studer, J. A. Higgens, and J. F. DeNatale, "MEM Relay for Reconfigurable RF Circuits," IEEE Microwave and Wireless Components Letters, Vol. 11, No. 2, Feb., 2001, pp. 53-55.

[8] S. Pacheco, C. T. Nguyen, and L. P. B. Katehi, "Microelectromechanical Electrostatic K-Band Switches," 1998 IEEE MTT-S Digest, pp. 1569-1572.

[9] G. M. Rebiez, “RF MEMS Phase Shifters: Design and Applications,” IEEE Microwave Magazine, June, 2002, pp. 72-81.
[10] Y. Liu, A. Borgioli, A. S. Nagra, and R. A. York, “Distributed MEMS Transmission Lines for Tunable Filter Applications,” RF and Microwave Computer-Aided Engineering, Vol. 11, No. 5, 2001, pp. 255-260.
[11] R. D. Streeter, C. A. Hall, R. Wood, and R. Mahadevan, “VHF High-Power Tunable RF Bandpass Filter Using Microelectromechanical (MEM) Microrelays,” RF and Microwave Computer-Aided Engineering, Vol. 11, No. 5, 2001, pp. 261-275.
[12] J. Brank, Z. J. Yao, M. Eberly, A. Malczewski, K. Varian, and C. L. Goldsmith, “RF MEMS-Based Tunable Filters,” RF and Microwave Computer-Aided Engineering, Vol. 11, No. 5, 2001, pp. 276-284.
[13] A. A. –Tamijani, L. Dussopt, and G. M. Rebeiz, “Miniature and Tunable Filters Using MEMS Capacitors,” IEEE Trans. on Microwave Theory and Techniques, Vol. 51, No. 7, July 2003, pp. 1878-1884.
[14] R. M. Young, et. al., “Low-Loss Bandpass RF Filter Using MEMS Capacitance Switches To Achieve A One-Octave Tuning Range And Independently Variable Bandwidth,” 2003 IEEE MTT-S Digest, pp. 1781-1784.
[15] J. Rizk, G.-L. Tan, J. B. Muldavin, and G. M. Rebeiz, “High-Isolation W-Band MEMS Switches,” IEEE Microwave and Wireless Components Letters, Vol. 11, No. 1, Jan., 2001, pp. 10-12.
[16] S. Majumder, J. Lampen, R. Morrison, and J. Maciel, “A Packaged, High-Lifetime Ohmic MEMS RF Switch,” 2003 IEEE MTT-S Digest, pp. 1935-1938.
[17] E. A. Sovero, R. Mihailovich, D. S. Deakin, J. A. Higgins, J. J. Yao, J. F. DeNatale, and J. H. Hong, “Monolithic GaAs PHEMT MMICs Integrated with High Performance MEMS Microrelays,” SMBO/IEEE MTT-S IMOC’99 Proceedings, pp. 257-260.
[18] A. E. Franke, Y. Jiao, M. T. Wu, T. J. King, and R. T. Howe, “Post-CMOS Modular Integration of poly-SiGe Microstructures Using poly-Ge Sacrificial Layers,” Technical Digest, Solid-State Sensors and Actuators Workshop (Hilton Head), pp. 18-21, Hilton Head, SC, June, 2000.
[19] F. Plötz, S. Michaelis, R. Aigner, H. –J. Timme, J. Binder, and R. Noé, “A Low-Voltage Torsional Actuator for Application in RF-Microswitches,” Sensors and Actuators A, 92, pp. 312-317, 2001.
[20] J. Muldavin, R. Boisvert, C. Bozler, S. Rabe, and C. Keast, “Power Handling and Linearity of MEM Capacitive Series Switches,” 2003 IEEE MTT-S Digest, pp. 1915-1918.
[21] C. L. Goldsmith, Z. Yao, S. Eshelman, and D. Denniston, “Performance of Low-Loss RF MEMS Capacitive Switches,” IEEE Microwave and Guided Wave Letters, Vol. 8, No. 8, pp. 269-271, 1998.
[22] H. A. C. Tilmans, W. D. Raedt, and E. Beyne, “MEMS for Wireless Communications: ‘From RF-MEMS Components to RF-MEMS-SiP’,” J. Micromech. Microeng. 13, S139-S163, 2003.
[23] J. L. Lund, C. V. Jahnes, H. Deligianni, L. P. Buchwalter, J. M. Cotte, P. Andricacos, D. E. Seeger, and J. H. Magerlein, “A Low Temperature Bi-CMOS Compatible Process for MEMS RF Resonators and Filters,” Technical Digest, Solid-State Sensors and Actuators Workshop (Hilton Head), pp. 38-41, Hilton Head, SC, June, 2002.
[24] M. Hara, J. Kuypers, T. Abe, and M. Esashi, “MEMS Based Thin Film 2 GHz Resonator for CMOS Integration,” 2003 IEEE MTT-S Digest, pp. 1797-1800.

[25] A. Rosen, M. Caulton, P. Stabile, A. M. Gombar, W. M. Janton, C. P. Wu, J. F. Corboy, and C. W. Magee, "Silicon as a Millimeter-Wave Monolithically Integrated Substrate – A New Look," RCA Review, vol. 42, no. 4, pp. 633-660, Dec. 1981.
[26] G. M. Rebeiz, L. P. B. Katehi, T. M. Weller, C. -Y. Chi, and S. V. Robertson, "Micromachined Membrane Filters for Microwave and Millimeter-Wave Applications (Invited Article)," International Journal of Microwave and Millimeter-Wave Computer-Aided Engineering, vol. 7, no. 2, March, 1997, pp. 149-166.
[27] K. C. Gupta, *Microstrip Lines and Slotlines, 2nd ed.*, 1996, Artech House, Inc.
[28] J. B. Muldavin and G. M. Rebeiz, "High-Isolation CPW MEMS Shunt Switches – Part 1: Modeling," IEEE Trans. on Microwave Theory and Techniques, Vol. 48, No. 6, June 2000, pp. 1045-1052.
[29] C. Goldsmith, J. Ehmke, A. Malczewski, B. Pillans, S. Eshelman, Z. Yao, J. Brank, and M. Eberly, "Lifetime Characterization of Capacitive RF MEMS Switches," 2001 IEEE MTT-S Digest, pp. 227-230.
[30] J. R. Reid, "Capacitive Switch Reliability Issues," 2002 IEEE MTT-S Digest, pp. 48-51.
[31] J. J. Yao and M. F. Chang, "A Surface Micromachined Miniature Switch for Telecommunications Applications with Signal Frequencies from DC up to 4 GHz," 8th International Conf. on Solid State Sensors and Actuators (Transducers '95), pp. 384-387.
[32] D. Hyman and M. Mehregany, "Contact Physics of Gold Microcontacts for MEMS Switches," IEEE Trans. On Components and Packaging Technology, Vol. 22, No. 3, Sept. 1999, pp. 357-364.
[33] J. Schimkat, "Contact measurements providing basic design data for microrelay actuators," Sensors and Actuators A73 (1999), pp. 138-143.
[34] J. DeNatale, R. Mihailovich, and J. Waldrop, "Techniques for Reliability Analysis of MEMS RF Switch," 40th Annual IEEE International Reliability Symposium, 2002, pp. 116-117.

8.0 Appendices

Appendix A: Capacitive Switch Device Simulations

A1: PECVD Oxide Capacitive Switch Simulations

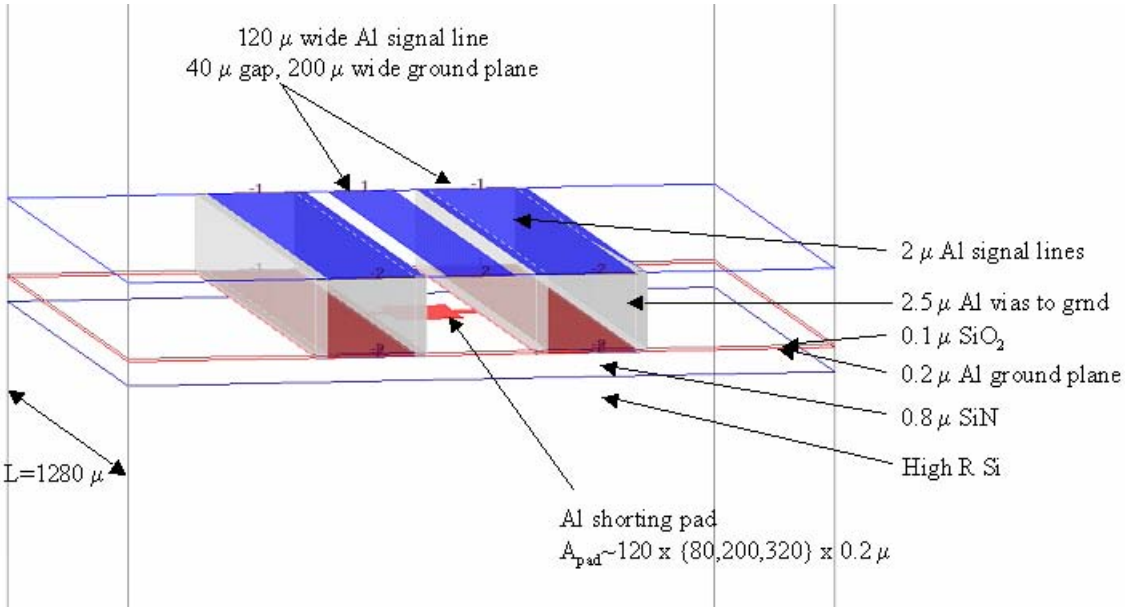


Figure A.1: Schematic used for the method of moments (MOM) simulation of the capacitive switch fabricated with PECVD oxide.

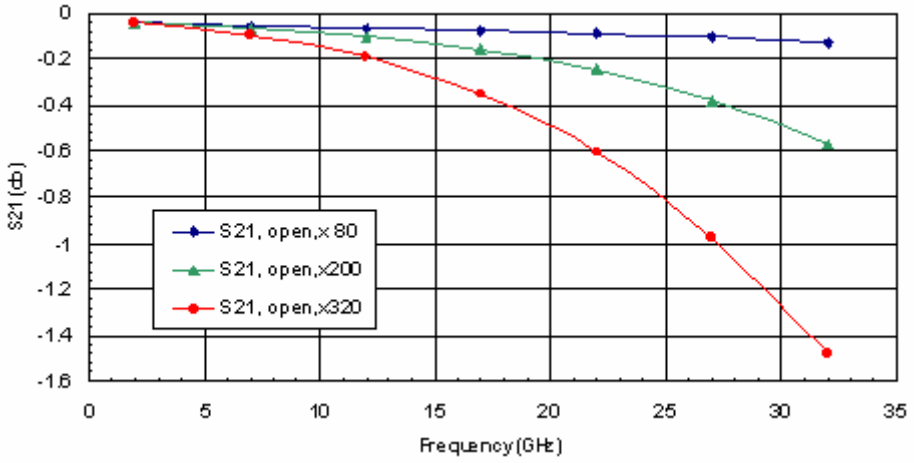


Figure A.2: S_{21} from the MOM simulation of the passing state of the capacitive switch shown in Figure A1.

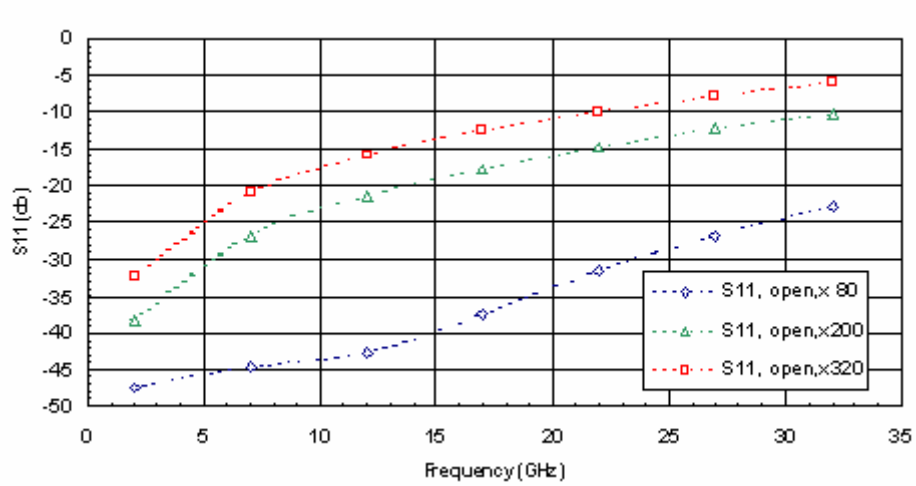


Figure A.3: S_{11} from the MOM simulation of the passing state of the capacitive switch shown in Figure A1.

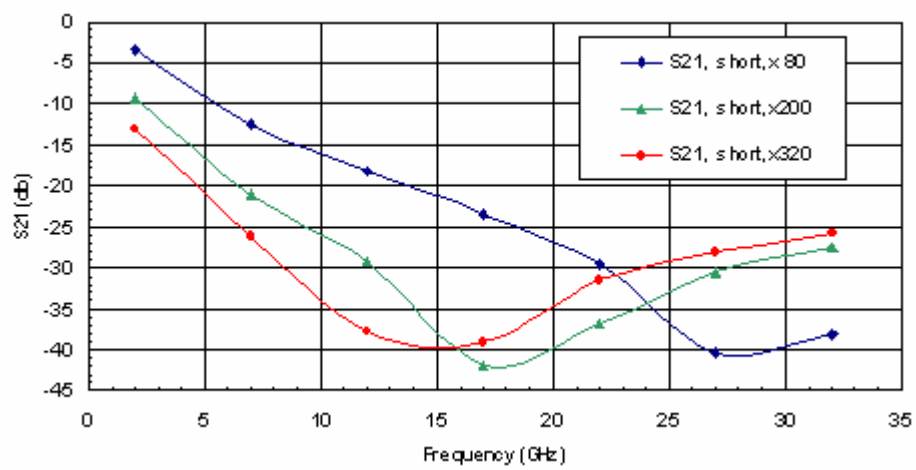


Figure A.4: S_{21} from the MOM simulation of the blocking state of the capacitive switch shown in Figure A1.

A2: Al-W Native Oxide Capacitive Switch Simulations

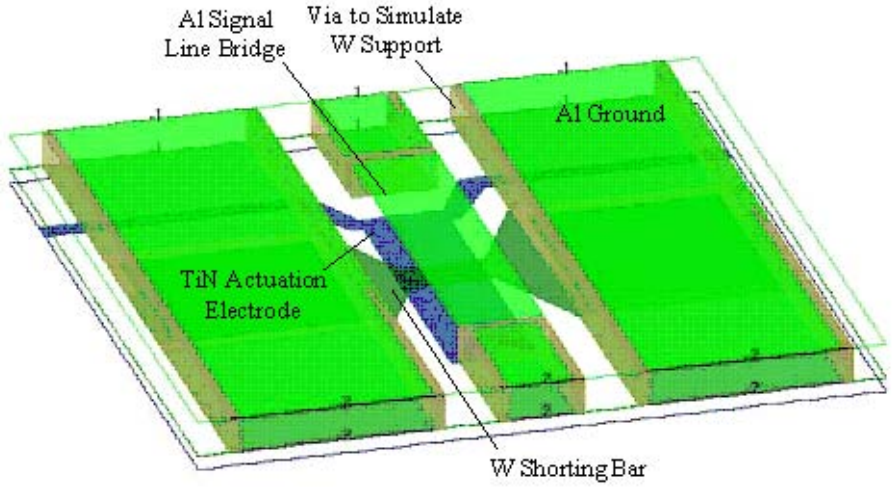


Figure A5: Schematic used for the method of moments (MOM) simulation of the capacitive switch fabricated with Al and W native oxides as the switch dielectric.

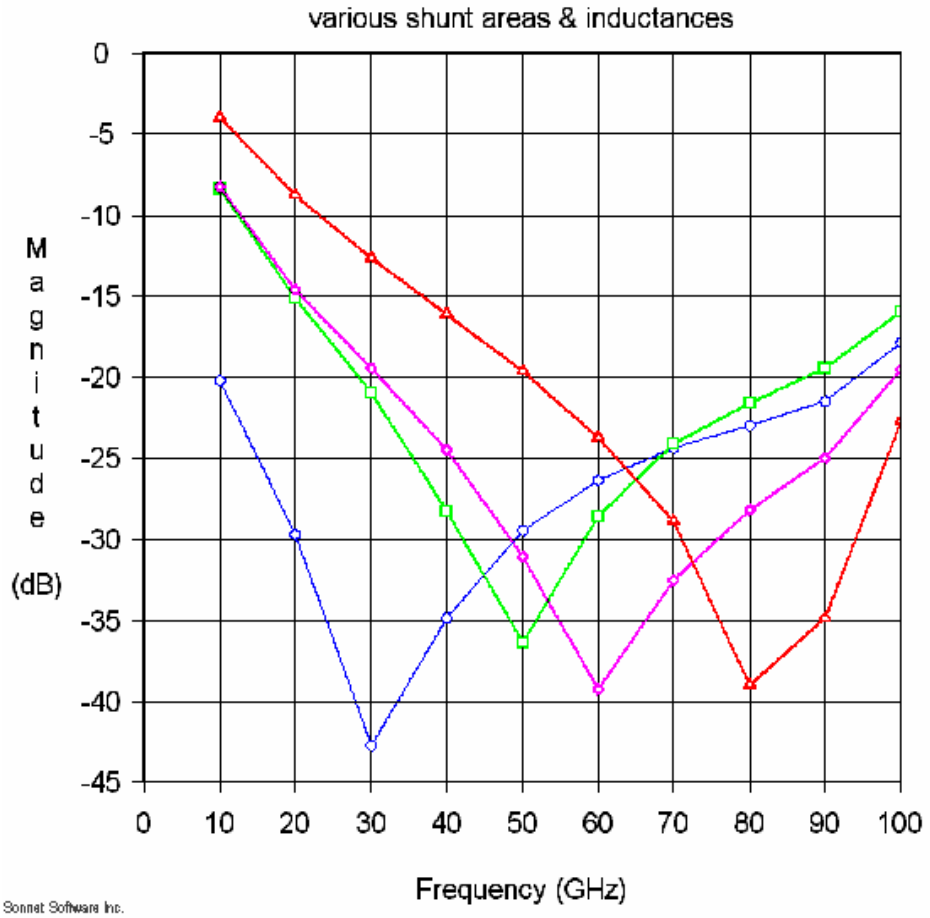
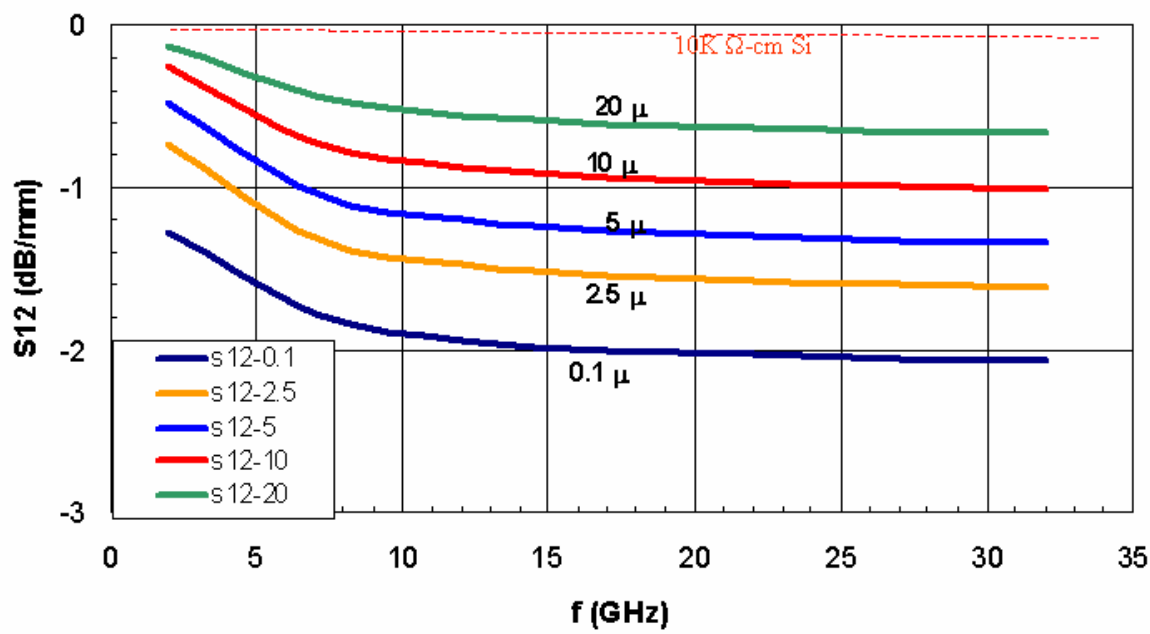


Figure A6: Downstate isolation as a function of frequency for varying shorting bar geometries.

Appendix B: Molded W Simulations of CPW T-lines as a function of distance from a standard low-R Si substrate.



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