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Integrated Superhard and Metallic Coatings for MEMS LDRD 57300 Final Report

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Integrated Superhard and Metallic Coatings for MEMS LDRD 57300 Final Report

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Abstract

Two major research areas pertinent to microelectromechanical systems (MEMS) materials and material surfaces were explored and developed in this 5-year PECASE LDRD project carried out by Professor Roya Maboudian and her collaborators at the University of California at Berkeley.

In the first research area, polycrystalline silicon carbide (poly-SiC) was developed as a structural material for MEMS. This material is potentially interesting for MEMS because compared to polycrystalline silicon (polysilicon), the structural material in Sandia National Laboratories' SUMMiTV^{TM} process, it may exhibit high wear resistance, high temperature operation and a high Young's modulus to density ratio. Each of these characteristics may extend the usefulness of MEMS in Sandia National Laboratories' applications. For example, using polycrystalline silicon, wear is an important issue in microengines, temperature degradation is of concern in thermal actuators and the characteristics of resonators can be extended with the same lithography technology.

Two methods of depositing poly-SiC from a 1,3-disilabutane source at 650˚C to 800˚C by low-pressure chemical vapor deposition (LPCVD) were demonstrated. These include a blanket method in which the material is made entirely out of poly-SiC and a method to coat previously released and fabricated polysilicon MEMS. This deposition method is much simpler to use than previous methods such as high temperature LPCVD and atmospheric CVD. Other major processing issues that were surmounted in this LDRD with the poly-SiC film include etching, doping, and residual strain control. SiC is inert and as such is notoriously difficult to etch. Here, an HBr-based chemistry was demonstrated for the first time to make highly selective etching of SiC at high etch rates. Nitrogen was incorporated from an NH_3 gas source, resulting in high conductivity films. Residual strain and strain gradient were shown to depend on deposition parameters, and can be made negative or positive. The tribology of poly-SiC was also

investigated. Much improved release stiction and in-use stiction performance relative to polysilicon MEMS was found. Furthermore, wear of poly-SiC-coated MEMS was much reduced relative to uncoated polysilicon MEMS. A prototype baseline process flow now exists to produce poly-SiC in the Berkeley Sensor and Actuator (BSAC) facility.

In the second project, galvanic deposition of metals onto polysilicon surfaces has been developed. The possible applications include reflective and optical coatings for optical MEMS, microswitches and microrelays for radio frequency MEMS and catalytic surfaces for microchemical reactors. In contrast to electroless deposition, galvanic displacement deposition requires no prior activation of the surface and is truly selective to silicon surfaces. This approach was used to deposit copper, gold and rhodium onto polysilicon MEMS. A method to study the adhesion of these metals to polysilicon was developed. It was also shown that the surfaces could be rendered hydrophobic by applying thiol-based self-assembled monolayers. This procedure also lowered their surface energy to ~3 $\mu J/m^2$, consistent with monolayer-coated polysilicon MEMS.

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Project 1

LDRD Summary Report
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<u>Project 1:</u> Integration of silicon carbide material as a coating as well as a structural material for MEMS

The wide energy band gap, high thermal conductivity, large break down field, and high saturation velocity of silicon carbide makes this material an ideal choice for high temperature, high power, and high voltage electronic devices. In addition, its chemical inertness, high melting point, extreme hardness, and high wear resistance make it possible to fabricate sensors and actuators capable of performing in harsh environments such Sandia's microengines, and hence the increasing interest in SiC in the microelectromechanical systems (MEMS) technology. Furthermore, SiC is an attractive material for micro and nanomechanical resonators due to the large ratio of its Young's modulus to density as compared to silicon.

A. Silicon Carbide Deposition

For heteroepitaxial growth of 3C-SiC on Si, the most common deposition method involves a two-step process (carbonization and crystal growth) using separate Si- and C-containing gases, such as SiH_4 and C_3H_8 with a carrier gas. This method produces relatively high-quality films but requires independent flow control of each source and high-growth temperatures (> 1200 ºC). These requirements in turn lead to elaborate and complicated gas control system to avoid departure from stoichiometry and cause serious problems such as high tensile stresses in the films. For these and other reasons, SiC technology remains technically demanding and non-standard in Si-based integrated circuit fabrication laboratories.

The deposition method we have pursued is based on CVD from a single precursor molecule. The precursor molecule we have used is 1,3-disilabutane (1,3-DSB, molecular structure CH_3-SiH_2-CH_2-SiH_3). The process has several key advantages over the conventional dual-source CVD SiC deposition method: 1) The precursor is a liquid at room temperature with vapor pressure of 400 Torr, and is rather benign. These characteristics make the handling aspects much simplified when compared to conventional dual-source CVD utilizing such gases as SiH_4. 2) The use of the single precursor insures stoichiometry, hence, it eliminates the need for elaborate gas handling system. 3) No pre-carbonization step is needed for deposition on Si and SiO_2.

In the first phase, an ultrahigh vacuum chamber was designed and assembled for the high-vacuum CVD (HVCVD) SiC deposition on 1cm x 1 cm sample size [**1-3**]. To transition the process into a conventional deposition scheme more compatible with microfabrication, more recently, we have assembled a low-pressure chemical vapor deposition (LPCVD) chamber for SiC deposition which is capable of processing 2" wafers [**4**]. The chemical, structural, and growth properties of the resulting films are investigated as functions of deposition temperature and flow rates. Based on X-ray photoelectron spectroscopy, the films deposited at temperatures as low as 650 ºC are indeed carbidic. X-ray diffraction analysis indicates the films to be amorphous up to 750 ºC, above which they become polycrystalline. The effect of process

parameters on film uniformity is also investigated. Highly uniform films are achieved at 750 ºC and lower, essentially independent of the flow rate (Fig. 1).

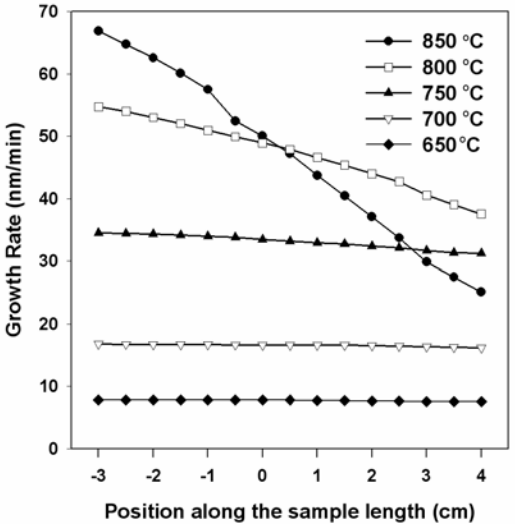
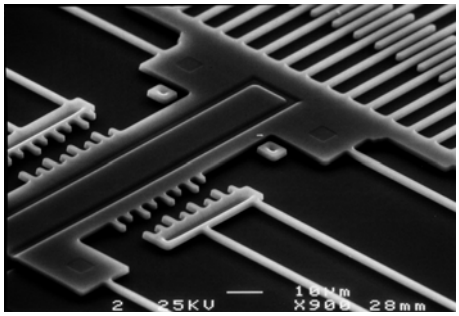


Fig. 1: SiC growth rate as a function of the sample length along the reactor axis. Position 0 corresponds to the center of the reactor tube.

The deposition of 3C-SiC films on Si(100) wafers from 1,3-DSB utilizing a conventional low pressure chemical vapor deposition system is studied theoretically [**5,6**]. The LPCVD reactor is modeled as a 1D system with axial dispersion. The reaction path of the 1,3-DSB decomposition is studied through quantum chemical methods due to the lack of kinetic information on this molecule. First the transition state for the decomposition reaction is calculated, then the fall-off regime of the reaction is determined using the RRKM theory. Information on the surface kinetics is taken mainly from literature data. The kinetic scheme obtained in this manner is first embedded into a 0D model to evaluate the most important kinetic processes, then a simplified kinetics is adopted in the 1D model. Finally, the calculated growth rates are compared with experimental data taken at different temperatures. The agreement between calculated and



(a)

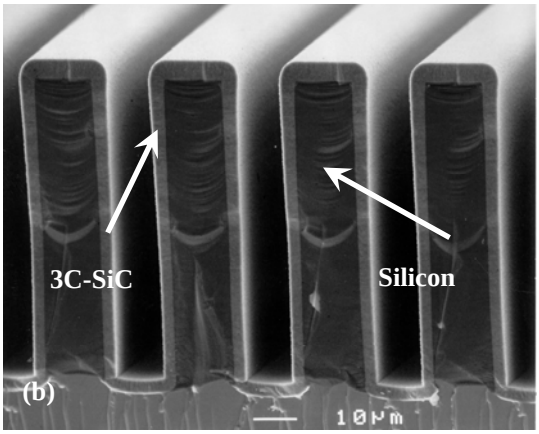


Fig. 2 (a) SEM image of a lateral resonator (fabricated in Sandia SUMMiT IV technology) following the deposition of a 35 nm thick SiC coating at 800°C. (b) Si microtrenches coated with SiC, yielding fairly conformal encapsulation

experimental data shows the importance of the gas phase decomposition reactions during the SiC deposition even in a low pressure process.

The DSB CVD process was used successfully to coat released polySi microstructures, due to our low deposition temperatures [**3**]. Figure 2a shows a SEM image of a lateral resonator (fabricated in Sandia SUMMiT IV technology) following the deposition of a 35 nm thick SiC coating at 800°C. The film thickness is estimated by carrying out the same deposition on a patterned Si(100) substrate and measuring the film thickness by profilometry. For thin SiC coatings, no deformation of the released structures is detected following deposition, as evidenced in the figure. This suggests that a fairly uniform film is deposited on all surfaces, including the bottom side. Furthermore, the SiC coating appears to be smooth, covering the microstructure's sidewalls. The microstructure is then immersed in hot KOH (an aggressive Si etchant) for 1 minute; no change is observed, suggesting that the film is dense and pin-hole free. In contrast, similar treatment on an uncoated microstructure led to complete dissolution of the device. Si microtrenches have also been coated with SiC, yielding fairly conformal encapsulation (Fig. 2.b). This is indirect evidence that the film is deposited on all sides. We have not yet performed systematic studies to look at coverage of the bottom side of very wide freestanding structures.

B. Silicon Carbide Doping

For both electronic and sensor applications, the electrical properties of polycrystalline SiC must be optimized. With the development and implementation of low-temperature growth processes for SiC, there is renewed interest in controlled doping while maintaining low deposition temperatures. This goal is particularly desirable for applications such as sensors and actuators, where tunable levels of conductivity are both highly desired and required. Nitrogen atoms are the predominant n-type dopant in all polytypes of SiC. Both N_2 and NH_3 have been successfully utilized as dopant precursors for the n-doping of SiC, although the decreased deposition temperatures used here necessarily require a precursor molecule such as NH_3 that needs less thermal energy for decomposition.

For these reasons, we investigated the growth and simultaneous doping of 3C-SiC films grown using 1,3-DSB and gaseous ammonia as the N dopant source using HVCVD system [**7**]. The chemical, structural, and electrical properties of n-doped cubic silicon carbide films grown from the precursors 1,3-disilabutane and NH_3 are investigated. Controlled nitrogen doping of 3C-SiC is demonstrated at 850 °C by by mixing the NH_3 with DSB and introducing the mixture to the reactor . Ammonia addition is shown to modify the growth rate, the chemical nature, and the crystalline quality of the deposited films. Undoped films exhibit a resistivity of 30 ohm-cm and are deposited at 220 nm/min. (The conductivity in the undoped film may be due to unintended background doping by the deposition system) N doping with 2% NH_3 in the feed gas, as measured by monitoring the pressure, at 850 ˚C markedly lowers the resistivity, reaching a minimum of 0.02 Ω·cm while only moderately decreasing the growth rate to 160 nm/min. For a 2 micron thick film, 0.02 Ω·cm corresponds to a resistance of 100 ohms/square.

The crystalline quality of the 3C-SiC thin films gradually changes from the 3C-SiC cubic polytype for an undoped film to an amorphous film at 5% NH_3 feed-gas content. However, at

2% NH_3, the film remains substantially polycrystalline . Likewise, morphology changes are significant at 5% NH_3, but subtle at 2% NH_3. Morphology changes, as indicated by surface roughness measurements, are shown in Table 1. Although N doping is definitely effective, XPS studies of the surface indicate that some of the N is also incorporated into the film in SiN_x form and also within an organic matrix. The SiNx content appears to increase with NH_3 content. More study is required to understand the quantitative contents, dispersion and the effect of these materials on the SiC properties.

Table 1. RMS roughness values obtained from AFM images over a 10 μm x 10 μm area and the growth rate on these samples

Temperature (°C)	RMS roughness (nm)	Growth rate (nm/min)
650	8.7	8
700	9.5	16
750	11.4	34
800	21.7	55
850	22.8	68

The doping investigation was then extended to the *in situ* nitrogen doping of SiC films in the commercial LPCVD reactor [**8**]. The major difference between the experiments described here and the doping experiments reported earlier [**7**] is that in contrast to the previous experiments, the current experiments are performed in a LPCVD reactor with a well-characterized hot zone with a uniform temperature profile, and well-controlled flow rates. In addition, the effect of deposition temperature, ammonia flow rate (as opposed to percent concentration in the feed gas) and post deposition annealing, not reported previously, are investigated. The chemical, structural, and electrical characteristics of in-*situ* doped SiC films grown from 1,3-disilabutane and NH_3 at various growth temperatures, 650-850 °C, are investigated by means of X-ray photoelectron spectroscopy, X-ray diffractometry, and four-point probe. The nitrogen is successfully incorporated throughout the SiC film (based on resistivity for different thicknesses). NH_3 appears to reduce the transition temperature from amorphous to polycrystalline by about 50 °C. The doped films exhibit approximately two orders of magnitude lower resistivity than the undoped films deposited at the same temperature, except for the films deposited at 650 °C, where doping does not occur. As the deposition temperature increases, the electrical resistivity is shown to increase and then decrease, peaking at 750 °C. The resistivity of the polycrystalline SiC films is further controlled by adjusting the NH_3 flow rate in the reactor. The lowest resistivity of 0.02 Ω·cm is achieved for the film deposited at 800 °C and the NH_3 flow rate of 5 sccm.

The post deposition annealing is shown to further lower the film resistivity. This decrease from 0.045 Ω·cm to 0.028 Ω·cm as annealing temperature increases from 900 °C to 1200 °C for a film deposited at 2 sccm 5% NH_3 in H_2. For a film deposited at 5 sccm 5% NH_3 in H_2, the decrease is from 0.028 Ω·cm to 0.020 Ω·cm.

C. Silicon Carbide Etching

Another major challenge in fabricating SiC devices is the selective etching of SiC films or bulk materials. Unlike Si, SiC is not etched significantly by most acids and bases at temperatures less than 600°C, which makes wet etching of SiC very difficult to accomplish. Non-standard techniques such as laser-assisted photoelectrochemical etching of SiC have been developed, but require special equipment and have poor control over the lateral dimensions. Reactive ion etching (RIE) is a standard technology for patterning semiconductor devices with precise line-width control, which is extremely important when the device features are in sub-micron scales. Therefore, RIE of SiC has been extensively studied utilizing various fluorinated gases such as CHF_3, CF_4, SF_6, and NF_3 in combination with O_2. Because of the strong bond between Si and C atoms, the etch rate of SiC is slower (less than 100 nm/min) than that of Si and SiO_2. Conventional etch masks for RIE such as hard-baked photoresist, SiO_2, and Si_3N_4 are etched at higher rate than SiC, which necessitates the employment of metals as etch masks. However, metal masks in RIE are known to cause micromasking phenomena, where metal atoms of the mask material are sputtered by the plasma and deposited in the etch field, producing grass-like structures. In addition, metal masks in RIE result in contamination in subsequent fabrication steps and the microfabrication tools, and hence, are commonly prohibited in integrated circuit (IC) processing. Thus, a high selectivity etching process using nonmetallic masks is highly desirable for SiC device fabrications.

The etching of polycrystalline 3C-SiC films is studied using oxygen-mixed sulfur hexafluoride transformer-coupled plasmas in a commercial LAM TCP 9400 etcher for MEMS applications [**9**]. Silicon dioxide is employed as etching masks, which avoids the micromasking phenomena and chamber contamination commonly involved when using metals as masks. The etch rate, selectivity and profile are characterized as functions of O_2 percentage in the etching gas. Etch rates of SiC remain almost unchanged at about 3600 Å/min up to 50% O_2, but decreases significantly when more than 50% O_2 is used. Etch selectivity of SiC over SiO_2 reaches a maximum of 2.6 when using 50% O_2. The chemical composition and the topography of the etched SiC films are also examined. The Si/C ratio is found not to significantly change after etching by different recipes, and no carbon fluoride polymer is formed on the SiC surface during the etch process. The etch process is found to actually smoothe the surface from 28 nm rms as-deposited to 22 nm rms after 1 minute of etching, and 12 nm rms after 4 minutes as etching proceeds (at approximately 0.3 μm/minute).

We have recently discovered high selectivity RIE of SiC using HBr-based chemistry in a commercial transformer/inductive coupled plasma (TCP) etcher [**10**]. Nonmetallic standard IC processing materials SiO_2 and Si_3N_4 are employed as etch masks. Etch rates of SiC and mask materials are measured as functions of chamber pressure at different TCP source power settings.

High etch rate ratios of SiC/SiO_2 and SiC/Si_3N_4 up to 20:1 and 22:1 are achieved, which are the highest reported to date. Most of the work reported in this section was carried out on small 1 cm x 1 cm dies placed at the center of the chuck, so cross-wafer uniformity data is not yet available.

Both the fluorine-based and the HBr-based chemistries have isotropic components and give sidewall slopes of about 60-80 degrees from horizontal.

D. Silicon Carbide Microfabrication

By combining the LPCVD (described in A) and dry etching processes (described in C) with conventional microfabrication technologies, a multi-user SiC MEMS process has been developed [**11-13**]. This is similar to the Si multi-user MEMS processes known as MUMPs in the MEMS research community, except that the structural material is poly-SiC instead of poly-Si. The deposition technology will become available by 2005 to outside users through a DARPA MEMS –Exchange Program. Such a multi-user SiC MEMS fabrication process provides us opportunities to fabricate almost any MEMS structures that have been demonstrated by Si MUMPs process. The process nominally allows up to three structural levels, and processing can be with doped or undoped poly-SiC. Currently. samples are limited to 2" in size, set by the LPCVD system. The etching tool is available in principle to all members of the Microlab including industrial members but needs to be characterized for full wafer.

A variety of microdevices have been realized. Figure 3(a) shows an SEM image of a complete SiC folded-flexure comb-drive resonator fabricated using the process. A schematic cross sectional view of this structure is shown in Fig. 3(b). Briefly, the fabrication process starts with the thermal oxidation of a Si(100) wafer, and then coating of Si_3N_4 films to isolated the conducting plane from the substrate. Highly doped 0.5 μm poly-Si films are deposited and patterned to serve as the conducting plane. Then, 2 μm LTO are deposited as the sacrificial and patterned to have anchors for the poly-SiC structural layers. Doped poly-SiC films are deposited to serve as the structural material and patterned by HBr/Cl_2 TCP dry etch using LTO as etch

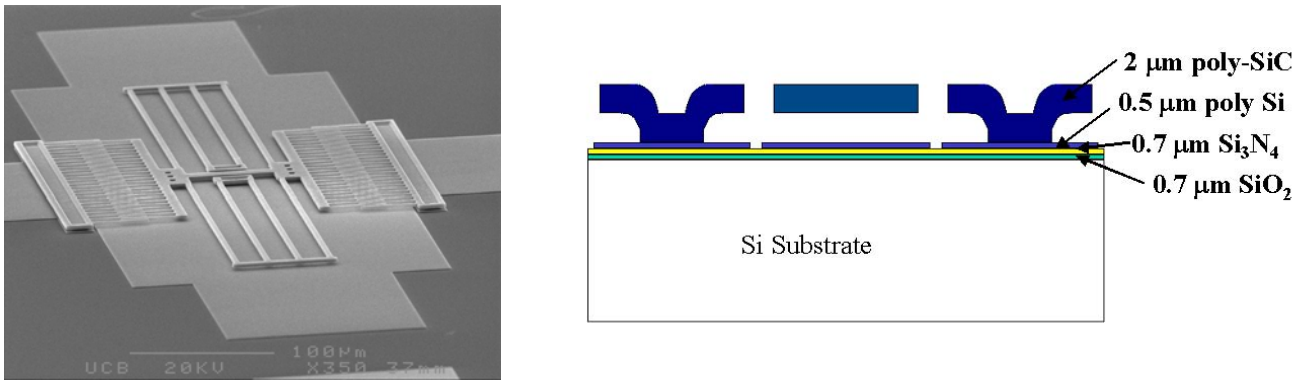


Fig. 3. (a) A SEM image of a SiC double-folded comb-drive resonator fabricated by combining the LPCVD and dry etching process for SiC with conventional microfabrication technology. (b) Schematic cross sectional view of the resonator.

masks. The structure is released by removing the LTO sacrificial layer in concentrated HF solutions.

At present, our baseline process poly SiC deposition temperature is 800 ˚C with 2% NH3 doping. The optimum temperatures for zero residual stress (at ~720 C) and strain gradient (800 C) are different (see below). However, we actually want the films to be slightly tensile. We are looking into the process pressure as a method to optimize both these properties at the same pressure.

E. Silicon Carbide Materials Characterization

In this section we characterize the materials and tribological properties of the SiC films.

E.i. Residual Strain

The residual strain of amorphous and polycrystalline SiC films deposited using 1,3-disilabutane single precursor is characterized as a function of deposition temperature ranging from 700 to 850°C [**11**]. SiC micro strain gauges and cantilever beam arrays fabricated by micromachining are employed to characterize directly the average residual strain and strain gradient. The residual strain of SiC films changes from compressive to tensile as the deposition temperature increases (Fig. 4a). The strain gradient is also found to depend on the deposition temperature, and can be adjusted between positive and negative values to fabricate flat, curling-up and curling-down micro-mechanical structures (Fig. 4b). The released cantilever beams curve up when the film is deposited at 750°C, but curve down for 800°C deposition temperatures. The lowest strain gradient of $3.6 \pm 1.6 \times 10^{-5}$ μm^{-1} is found for deposition temperature of 800°C.

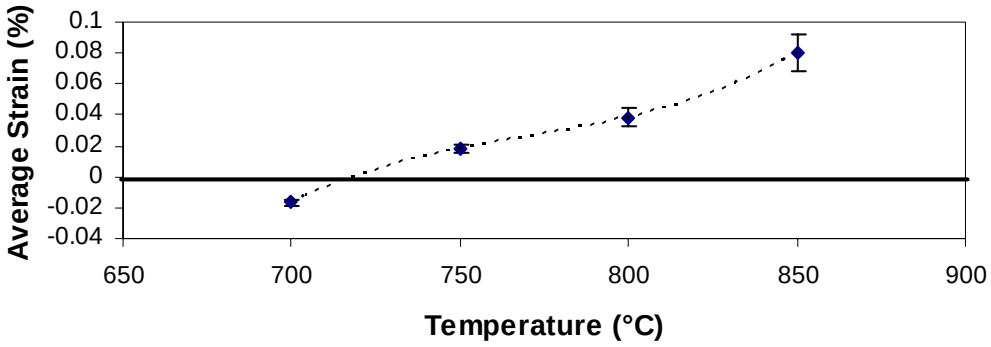


Fig. 4a. The residual strain of 1 μm thick SiC films measured by micromachined SiC strain gauges as a function of deposition temperatures**.** The dotted line is added as an aid to the eye.

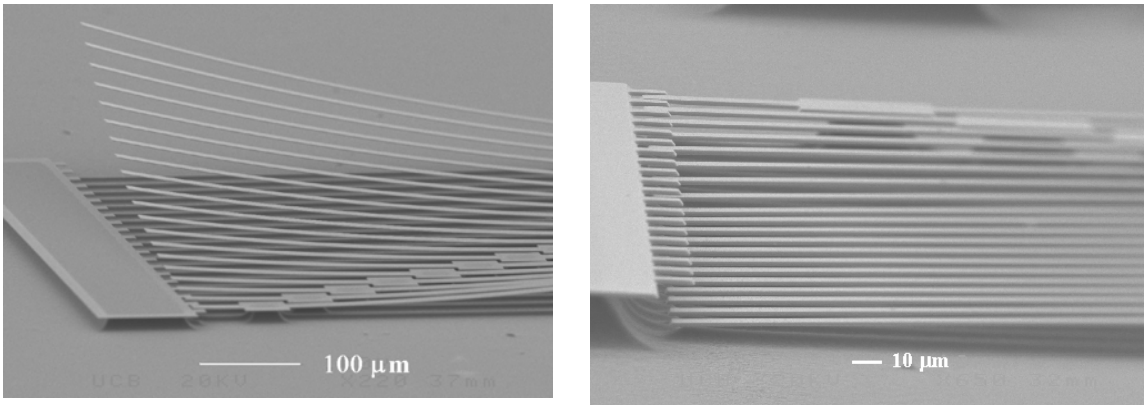


Fig. 4b. SEM images of SiC CBA after releasing from the substrates. The SiC films are deposited at (left) 750°C and (right) 800°C.

E.ii. Young's Modulus

By combining the LPCVD and RIE processes in conventional surface micromachining technology, SiC-based folded-flexure comb-drive resonators are fabricated [**12**]. The measured acoustic velocity of 15 km/s and Young's modulus of 710 GPa are the highest reported to date for poly-SiC films. Because the poly-SiC films are [111] textured, the folded-flexure is resonating in the (111) plane, where the Young's modulus is independent of the azimuthal angle. Using the elastic constants for 3C-SiC computed from semiempirical interatomic potential, the Young's modulus for single crystalline 3C-SiC in (111) plane is calculated to be 492 GPa, which is significantly lower than what is measured for our poly-SiC films. However, the Young's modulus of up to 700 GPa have also been reported for 3C-SiC films previously. In addition, it has been reported that doping with boron increases the Young's modulus of 3C-SiC bulk materials by a factor of about 2. We attribute the high Young's modulus to the effect of grain boundaries as well as the effect of nitrogen doping, but more detailed investigation is required to fully understand these results.

E.iii. Fracture

The fracture of polycrystalline SiC films is investigated using a micrometer-sized fracture tester fabricated by micromachining techniques [**13**]. A series of SiC cantilever beams varying in length are carried by a moving shuttle tethered to the substrate, and are bent in plane until fracture. The fracture strain of SiC films is calculated from the deflection of bending beams using non-linear beam theory and determined to be 3.3% ± 0.2%, which corresponds to a fracture stress of 23.4 ± 1.4 GPa using E=700 GPa. These values are significantly higher than those for polycrystalline silicon (2.6% and 4.2 GPa). In addition, the crack propagation in the polycrystalline SiC films is observed to be transgranular.

E.iv. Tribology

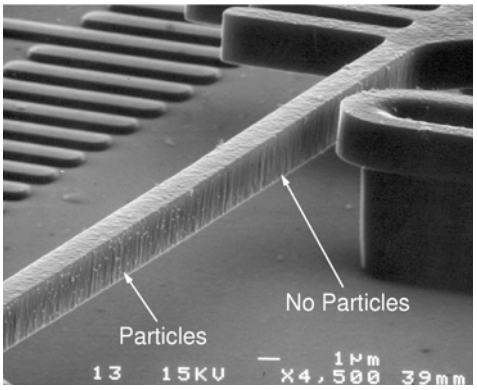
The tribological characteristics of SiC films, both as a structural material and as a thin passivating coating, are characterized using micromachined cantilever beam arrays, doubly clamped beams, and sidewall adhesion and friction testers [**14,15**]. Our results indicate that using SiC as the substrate or structural layer or thin film coating significantly reduces stiction of free-standing structures to the substrate, and virtually eliminates stiction and wear of sidewall MEMS structures.

The apparent work of adhesion of newly released poly-Si to SiC contacts (Table 2) is more than 4 orders of magnitude less than that of poly-Si to poly-Si contacts, which makes the detachment length of cantilever beams more than 1.5 mm long. All the test structures are released by time-etching the sacrificial silicon oxide in 49% HF aqueous solution, followed by rinsing with deionized water and isopropanol. They are dried in air of normal laboratory ambient (20 °C and 40% relative humidity). The detachment length only begins to decrease (and hence, the work of adhesion to increase) after the structure is exposed to room air (40% relative humidity) for two weeks. Even then, the replacement of poly-Si with SiC still significantly reduces the stiction of MEMS structures. We expect that under hermetic encapsulation, SiC will retain its extremely low stiction characteristics indefinitely. Clearly, to understand these results fully merits further investigation. The doubly clamped SiC beams up to 4 mm-long (the longest on the mask set) on both Si and SiC substrates are found to be free-standing after being released and dried in air without employing the critical point drying technique, and remain stiction-free after manually pushing into contact with the substrate. If adhesion is tested on poly-SiC/poly-Si interfaces that were first exposed to an O2 plasma clean, adhesion rises, but not to the level of poly-Si/poly-Si interfaces. It should be noted that the role of surface roughness of the poly-SiC (which tends to be rougher than poly-Si) cannot yet be differentiated from the role of poly-SiC surface chemistry in the adhesion results.

***Table 2**. In-use stiction results for contacts of poly-Si to Si and poly-Si to SiC surfaces. The apparent work of adhesion is calculated from the detachment length of cantilever beams.*

Structural Material	Substrate Material	Treatment	Cantilever Beams	
			Detachment Length (μm)	Apparent Work of Adhesion (mJ/m^2)
poly-Si	poly-Si	After release	200	20
poly-Si	SiC	After release	>1500	<0.006
		After exposed to room air for 1 week	>1500	<0.006
		After exposed to room air for 2 weeks	1000	0.034

Sidewall friction testers (Fig. 5) fabricated from poly-Si are tested with and without SiC coating. The SEM image of a rubbing beam of a SiC-coated side-wall friction tester after 1 million wear cycles is shown in Fig. 5(a). Another rubbing beam without any coating which has failed due to high friction and wear after about 11,000 cycles is shown in Fig. 5 (b). By comparing these two images, one can clearly see the wear debris and the worn surface of poly-Si without SiC coating, which are not obviously observed with SiC coating. Static friction coefficient as a function of rubbing cycle is reported in Fig. 6 and compared to the base line of Si-to-Si contact (i.e., without SiC coating). As is observed without any coating, the friction coefficient increases as the wear cycles increase and the device fails after 11,000 cycles. But with a thin SiC coating, the device still works after a million rubbing cycles, and the friction coefficient first decreases and then stabilizes as the number of wear cycles increases, indicative of the self-lubricating characteristics of SiC. Clearly, to understand this intriguing behavior fully merits further investigation. It is also interesting to note in Fig. 5(a) that particles on the surface are apparently worn away during the friction testing. Yet, as seen in Fig. 6, friction decreases with the number of cycles.



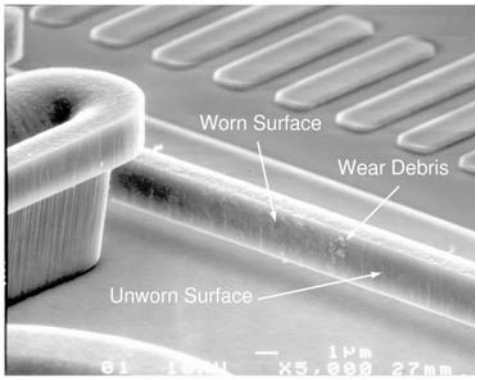


Fig. 5. SEM images of (a) the rubbing beam of a SiC-coated side-wall friction tester after 1 million wear cycles. (b) the tester without any coating which has failed due to high friction and wear after about 11,000 cycles.

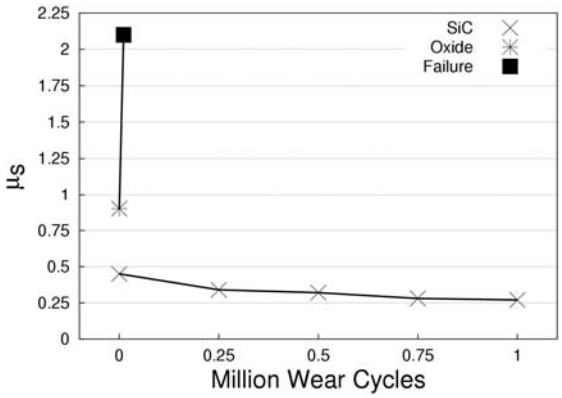


Fig. 6. Static friction coefficient as a function of rubbing cycle for sidewall friction testers with various surface treatments. In the case of oxide samples, the last data point represents failure of the device. The SiC device was not observed to fail by wear.

<u>Project 2:</u> Integration of noble metals as a coating for MEMS applications

Electrochemical processes at the core of IC technologies have been the subject of extensive investigations. In contrast, metallization of microelectromechanical systems (MEMS) by electrochemical processes remains a relatively unexplored subject. Potential applications of metals in MEMS technology range from reflective/conductive coatings for optical MEMS, microswitches and microrelays, to catalytically active coatings in microchemical reactors. Through the LDRD funds, we have reported recently on a new process for silicon metallization, which offers several attractive features for MEMS applications. The method is based on galvanic deposition from fluoride-containing solutions. In contrast to electroless deposition, galvanic displacement deposition requires no prior activation of the surface and is truly selective to silicon surfaces. Although the detailed mechanism by which metal ions are displaced from solution is still not well understood, the process can be described by the two half-cell reactions:

Anodic: $Si + 6\ HF \rightarrow SiF_6^{2-} + 6\ H^+ + 4\ e^-$
Cathodic: $Me^{n+} + n\ e^- \rightarrow Me$

where Me denotes any metal more noble than H (see Table).

Metal	**Redox Potential** (V vs. NHE)
Au	Au^{+3}/Au 1.42
Pt	Pt^{+2}/Pt 1.2
Ir	Ir^{+4}/Ir 0.93
Pd	Pd^{+2}/Pd 0.83
Ru	Ru^{+2}/Ru 0.8
Ag	Ag^{+}/Ag 0.78
Rh	Rh^{+3}/Rh 0.76
Cu	Cu^{+2}/Cu 0.34
Re	Re^{+3}/Re 0.3
Ni*	Ni^{+2}/Ni -0.23

We have used this approach to deposit copper on silicon surfaces [**16**]. Continuous copper films are obtained galvanically on p- or n-type, single- or poly-crystalline silicon. The films possess homogeneous structure, smooth surface and good adhesion to the substrate. The plating bath comprises an aqueous solution containing a copper compound, ascorbic acid, ammonium fluoride and an anti-stress agent. With this process, the use of seed layers to improve adhesion between metal and semiconductor is avoided. The coating process has been used to plate polycrystalline silicon micromachined devices after the release step. Excellent sidewall coverage is observed, indicating that the coating process is conformal and selective (e.g., it does not deposit on silicon nitride).

We have examined in detail several issues of concern in immersion plating MEMS, namely the conformality of the coating process and the surface energy of deposited copper films [**17,18**]. In particular, we have been able to Cu plate cantilever beam arrays. The copper film obtained by immersion plating is hydrophilic (as are the surfaces of bulk metallic Cu). This is an undesirable property in most MEMS devices, as it leads to microstructure adhesion caused by capillary forces. Fortunately, functionalization schemes for copper surfaces are available, and can be used to render the surfaces hydrophobic. Among these, we have chosen to employ alkanethiol self assembled monolayer passivation. We have been able, for the first time, to successfully integrate this functionalization scheme with a Cu plating and microstructure release process. The dodecanethiol-coated cantilever beam arrays are used to find the apparent work of adhesion of the film. Measurements on several different arrays yielded an average detachment length of about 1100 μm, or a work of adhesion of about 3 μJm^{-2}.

Adhesion of copper films on silicon is investigated by microindentation measurements [**19**]. Load-displacement tests with loads in the range of 1-1000 mN are performed on immersion plating copper films deposited on Si(100) from fluoride containing solutions, with or without adhesion-promoting additives. The results are analyzed with the aid of a composite hardness model for soft films on hard substrates. The composite Vickers microhardness is influenced by the adhesion of the copper film to the substrate: stronger adhesion corresponds to higher composite hardness and a more extended deformation zone at the film/substrate interface. Thus, it is shown that microhardness measurements provide a useful way to quantify the effect of solution additives (such as ascorbic acid or sodium sulfite) and heat treatment on copper film adhesion, and to rank additives accordingly.

Thin Au films were also grown on Si and Ge substrates by galvanic displacement from fluoride-containing solutions [**20,21**]. The physical and chemical properties of the metal-semiconductor interface were characterized by a variety of techniques, including X-ray photoelectron spectroscopy, atomic force microscopy and electron microscopy. Displaced gold films exhibit strong adhesion to germanium substrates, but not to silicon. This behavior is explained by the presence of a chemical bond at the Au-Ge interface, which is not observed in the Au-Si system.

We have also developed a process for galvanic displacement deposition of Rh. The process starts with etching of Si(100) substrate in concentrated HF to remove the native oxide. Then, the plating proceeds by placing the sample in a bath consisting of 20 mM $Rh(NO_3)_3$ with 8.5% v/v HF. After deposition, the samples are rinsed with DI water and dried using N_2. X-ray photoelectron spectroscopy indicates Rh^0 peaks only, with the strongest being Rh $3d_{5/2}$ and $3d_{3/2}$ at 307 and 312 eV binding energies, respectively. The films are thick enough (more than 10 nm) such that no photoelectron peaks from the underlying silicon are observed. X-ray diffraction analysis reveals (111), (200), (311) and (400) peaks, at 41, 48, 84 and 107º. The remaining peaks belong to Si(100) substrate. The catalytic activity of the deposited Rh films should be very interesting to examine.

Publications acknowledging Sandia support during this LDRD project:

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