

Conf -950728--1
SAN095-1374C

$\text{La}_{0.5}\text{Sr}_{0.5}\text{CoO}_3$ Electrode Technology for $\text{Pb}(\text{Zr},\text{Ti})\text{O}_3$ Thin Film Nonvolatile Memories

B.A. Tuttle, H.N. Al-Shareef, W.L. Warren, M.V. Raymond, T.J. Headley and J.A. Voigt

Sandia National Laboratories, Albuquerque, NM 87185, USA

Oxide electrode technology is investigated for optimization of $\text{Pb}(\text{Zr},\text{Ti})\text{O}_3$ (PZT) thin film capacitor properties for high density nonvolatile memory applications. PZT thin film capacitors with RF sputter deposited $\text{La}_{0.5}\text{Sr}_{0.5}\text{CoO}_3$ (LSCO) electrodes have been characterized with respect to the following parameters: initial dielectric hysteresis loop characteristics, fatigue performance, microstructure and imprint behavior. Our studies have determined that the fatigue of PZT capacitors with LSCO electrodes is less sensitive to B site cation ratio and underlying electrode stack technology than with RuO_2 electrodes. Doping PZT thin films with Nb (PNZT) improves imprint behavior of LSCO//PZT//LSCO capacitors considerably. We have demonstrated that PNZT 4/30/70 // LSCO capacitors thermally processed at either 550°C or 675°C have almost identical initial hysteresis properties and exhibit essentially no fatigue out to approximately 10^{10} cycles.

1. Introduction

Several important technological issues must be resolved before PZT thin film capacitors are viable for use in high density, nonvolatile semiconductor memories. A primary concern is having appropriate initial hysteresis loop behavior, such that, the capacitors function at low operating voltages, yet remain immune to disturb pulses. Further, these capacitors must exhibit superior fatigue performance, appropriate microstructure for process integration and minimal tendency to imprint. While carefully controlled Pt electrode technology may be marginally acceptable with respect to fatigue performance for certain nonvolatile memory applications [1,2], PZT thin films with oxide electrodes provide superior fatigue performance. PZT thin film capacitors deposited on RuO_2 or LSCO electrodes have exhibited essentially no loss in switched polarization up to 10^{13} cycles[3,4]. However, we have recently shown that the fatigue performance of PZT capacitors deposited on RuO_2 electrodes are more sensitive to underlying stack technology and changes in B site cation stoichiometry than similar PZT capacitors deposited on LSCO electrodes[5]. For these reasons, we have investigated PZT capacitors with RF sputter deposited LSCO electrodes with particular emphasis on lowering the processing temperatures. For high density memories, process temperatures of 625°C or less are essential to maintain plug integrity and to prevent degradation of underlying CMOS circuitry.

Imprint is a phenomenon that can seriously limit the functionality of high density ferroelectric thin film semiconductor memories. At the material level, recent work [6-8] has demonstrated that imprint is due to a rigid voltage shift caused by trapped electrons near the positive head of the polarization in the near interfacial regions of the ferroelectric thin film. Imprint, or voltage shifts in the dielectric hysteresis characteristic, can be induced by the following treatments: (1) poling a capacitor at ambient and then subjecting the capacitor to elevated temperature (P_r / Temp), (2) applying a dc bias and subjecting the capacitor to elevated temperature (V_s /Temp), (3) poling a capacitor at ambient and then

DISTRIBUTION OF THIS DOCUMENT IS UNLIMITED

MASTER

GT

DISCLAIMER

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency thereof, nor any of their employees, make any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

DISCLAIMER

**Portions of this document may be illegible
in electronic image products. Images are
produced from the best available original
document.**

illuminating with UV light (P_r /UV) and (4) applying dc bias and illuminating capacitors with UV radiation (V_s /UV). As discussed elsewhere [8] these techniques are also able to distinguish between electronic and ionic contributions to the voltage shift. We have used these techniques to evaluate the effect of processing conditions on the tendency for PZT//LSCO capacitors to imprint. Our elevated temperature treatment typically is 145°C for 45 min. On a device level, when the voltage shift is roughly equal to the coercive voltage, a bit error reading can occur in a memory [7]. The error occurs since the two remanent states (logic 1 or logic 0) are indistinguishable to the sense amplifier during memory read operations. Thus, capacitors having imprint of this magnitude are considered unacceptable for high density memories.

2. Experimental Procedure

The PZT and PNZT thin films discussed in this paper were fabricated by a solution deposition procedure termed the inverted mixing order process[8]. The 0.4 M solutions were synthesized by blending the Zr, Ti and Nb alkoxide precursors, adding acetic acid and methanol to the solution and then adding the lead (IV) acetate precursor. Additional acetic acid, methanol and distilled water were added to the solution to control viscosity and improve solution stability. Solutions were spin deposited at 3500 rpm for 30 s and then dried at 300°C for 5 min on a hot plate. Additional layers were deposited to achieve the desired film thickness. The films in this study consisted of either 3 or 4 layers and had a crystallized film thickness of approximately 0.3 μ m or 0.4 μ m, respectively. Crystallization temperatures ranged from 550°C to 675°C, and a heating rate of 50°C /min was used.

Both LSCO and RuO₂ electrodes were deposited by ambient RF magnetron sputter deposition. RuO₂ films were deposited by reactively sputtering a Ru metal target using a 50:50 oxygen to argon sputter gas ratio. LSCO films were deposited from a stoichiometric oxide target using argon sputter gas. A typical electrode stack was 60 nm LSCO or RuO₂//150 nm Pt//20 nm Ti//100 nm TiO₂//400 nm SiO₂//Si. Because of inferior fatigue performance of the RuO₂ electrodes for high Ti content films on this electrode stack, an electrode stack of 200 nm RuO₂ //80 nm Ti//400 nm TiO₂//400 nm SiO₂//Si was also investigated. For the LSCO electrodes, high temperature anneals were used to reduce the resistivity of the electrodes. While 675°C for 30 min was the baseline electrode annealing temperature, annealing temperatures as low as 550°C were shown to provide adequate resistivity for dielectric hysteresis and fatigue measurements. For our capacitors, the bottom electrode was annealed before the PZT film was deposited and the top electrode was annealed after the PZT film was crystallized, both electrodes were annealed at the same temperature. The top electrodes for the LSCO//PZT capacitors consisted of 60 nm LSCO//100 nm Pt to reduce the series resistance. Both the initial hysteresis measurements and the fatigue measurements were made with an RT66A ferroelectric tester. Microstructural characterization was performed using a Philips CM30 300 kV transmission electron microscope (TEM) and a JEOL 6400 scanning electron microscope.

3. Results

3.1. Initial hysteresis loops

Dielectric hysteresis loops for PZT 30/70 films deposited on LSCO and RuO_2 electrodes and crystallized at 675°C for 30 min are shown in Fig.1. The two capacitors have similar remanent polarization and saturation polarization values, approximately 19 $\mu\text{C}/\text{cm}^2$ and 42 $\mu\text{C}/\text{cm}^2$, respectively. However, the coercive voltage for the PZT film deposited on LSCO was less than that for the film deposited on RuO_2 (1.8 volts compared to 2.1 volts). There was also considerable asymmetry in the coercive voltage for the film deposited on RuO_2 with $+V_c = 2.87$ volts and $-V_c = -1.32$ volts. A high temperature post-anneal of the RuO_2 electrodes did not change the hysteresis loop. Both films were 0.3 μm thick and the Pt containing electrode stack described in the experimental procedure was used. The lower coercive voltage and more symmetric hysteresis loops make the LSCO technology more attractive than RuO_2 electrodes, at least for this stack technology.

3.2. Fatigue performance

The fatigue performance for PZT 30/70 capacitors deposited on RuO_2 and LSCO electrodes are shown in Fig.2. Limited polarization loss (16%) is observed for the PZT//LSCO capacitor; whereas, the polarization of the PZT// RuO_2 capacitor has a 80% decrease from its initial value after 10^{10} cycles. For these fatigue measurements, electrodes of 300 μm diameter and voltage cycles of ± 6 volts, 25 kHz, across the 0.4 μm thick capacitors were used. While the PZT//LSCO capacitor was deposited on the platinum containing stack, the PZT// RuO_2 capacitor was deposited on the electrode stack that did not contain Pt. A different underlying electrode technology was used to minimize the fatigue of the PZT 30/70// RuO_2 capacitor. Much worse fatigue behavior was measured for PZT 30/70// RuO_2 capacitors using the original Pt containing stack. Further, PZT 50/50 // RuO_2 films deposited on the stack that did not contain platinum, exhibited excellent fatigue behavior with the switched polarization decreasing by less than 10% after 10^{10} cycles[5]. A discussion of the effect of underlying electrode stack technology on PZT// RuO_2 capacitor fatigue behavior is outside the scope of this paper. Our fatigue measurements do show that LSCO electrodes are considerably less sensitive to B site cation stoichiometry and underlying substrate technology than RuO_2 electrodes.

3.3. Microstructure of PZT and PNZT films

High density memories require capacitors that have uniform microstructure and fine grain size. Microstructures of identically processed PZT 30/70 and PNZT4/30/70 films are shown in the SEM micrographs of Fig.3. Niobium additions (4 at%) decreased microstructural uniformity, decreased grain size and increased the volume fraction of second phase. Grain size for the PZT 30/70 film crystallized at 675°C and deposited on the LSCO electrodes was relatively uniform and equiaxed with grain sizes ranging from 0.1 to 0.25 μm . No evidence of second phase was observed. The majority of the PNZT film consisted of fine perovskite grains on the order of 0.1 μm . However, a small volume percent of large perovskite grains, on the order of 1 μm , having a pancake morphology are observed. Cross-Sectional TEM micrographs indicate that these large grains are perovskite

of high density and extend only approximately 100 nm into the film, in contrast with rosette structures commonly reported in the literature that extend through the entire thickness of the film. The cross-sectional TEM micrograph of the PNZT 4/30/70 film shown in Fig.4 indicates 0.1 μ m, columnar perovskite grain morphology with a fine grain (10 nm) second phase that is concentrated near the top of the film. This second phase has a fluorite structure and essentially forms a discontinuous layer in the top 20 nm of the film. Perovskite grains completely extend from the bottom electrode to the top electrode over roughly 50% of the film area, with the remaining 50% of the top surface consisting of the fluorite phase. While the microstructure of the PZT 30/70 film is superb for high density memory applications, there are presently some concerns regarding the PNZT 4/30/70 film microstructure for these applications.

3.4. PNZT//LSCO capacitor properties as a function of crystallization temperature

Lowering ferroelectric thin film capacitor processing temperatures below 625°C is essential for process integration of high density nonvolatile memories. For this reason, we have investigated the properties of PNZT // LSCO capacitors processed at the following temperatures: 675°C, 625°C, 600°C, 575°C and 550°C. These process temperatures are the temperatures at which both the LSCO electrode was annealed and the PNZT film was crystallized. All PZT films were 0.4 μ m thick. The initial dielectric hysteresis loops of the PNZT/LSCO capacitors processed at 675°C and 550°C are shown in Fig. 5 and are very similar. A remanent polarization of approximately 12 μ C/cm², a saturation polarization of approximately 34 μ C/cm² and a coercive voltage of approximately 1.3 volts were obtained for both films. Further, as shown in Fig.6. the fatigue behavior to approximately 10^{10} cycles was very similar for PNZT film capacitors processed at 550°C or 675°C. The increase in polarization with cycling may be attributed to a slight increase in leakage current of these capacitors or depinning of domain walls. The capacitor processed at lower temperature did exhibit more leakage under bias at 140°C than the capacitor processed at 675°C. Capacitors at intermediate process temperatures exhibited very similar initial hysteresis loop and fatigue behavior to that shown in Fig.5 and Fig.6.

3.5. Imprint behavior

Imprint data for three different PZT//LSCO capacitors are presented in Table 1. The effects of B-site cation stoichiometry and Nb doping [7] are illustrated by these three film compositions: PZT30/70, PNZT 4/30/70 and PZT 45/55. All of these capacitors were processed at 675°C for 30 min. For our data we have used two different techniques to simulate the tendency to imprint: (1) voltage bias and temperature and (2) remanent polarization and temperature. Voltage bias/temperature typically is a worst case condition for imprint due to enhanced polarization caused by alignment of defect-dipoles [8] and the increase in polarization at field compared to the remanent polarization state. The enhanced polarization can lead to additional electron trapping. Voltage bias/temperature imprint measurements were made by applying a positive 8 volt bias to the film, heating the film under bias to 140°C for 20 min, cooling the film to ambient and measuring the positive and negative coercive voltages. A negative 8 volt bias was applied to the film and the process repeated. The imprint voltage tabulated is the difference between the coercive voltages measured for +8 volt and - 8 volt biases, respectively. For remanent polarization/temperature imprint measurements, the films were poled at ambient and subjected to the 145°C/45 min thermal treatment with no bias applied. The imprint voltage

tabulated is the difference in coercive voltages measured at ambient for films subjected to the thermal treatment and poled to the +Pr and -Pr states, respectively. It is the remanent polarization, not the voltage bias, that is the driving force for imprint.

While the degree of imprint for PZT 30/70 films are unacceptable for nonvolatile memories with a 2.37 volt shift, Nb doping makes these capacitors highly resistant to imprint. The voltage imprint for the PNZT 4/30/70 film is an order of magnitude less than for the PZT 30/70 film. We postulate that Nb doping decreases the tendency for imprint by suppression of oxygen vacancies which in turn decreases the number of defect dipoles. A substantial reduction in imprint voltage is obtained by increasing the Zr content of the PZT film, as shown for a PZT 45/55 film. Compositions near the morphotropic phase boundary exhibit the largest concentration of Ti^{3+} centers[10]. These deep electron traps may diminish the number of carriers that can be trapped in the near interfacial ferroelectric thin film regions, thus decreasing the observed voltage shifts. Characterization of imprint for PZT//LSCO capacitors processed at lower temperatures is in progress.

Table 1. Imprint Behavior for PZT//LSCO Thin Film Capacitors

Film Composition	P_r / Temp	V_s / Temp
PZT 30/70	0.79	2.37
PNZT 4/30/70	0.06	0.21
PZT 45/55	0.28	<0.1

4. Summary

We have demonstrated that PZT //LSCO capacitor technology, with RF sputtered LSCO electrodes, is viable for high density nonvolatile memories with respect to fatigue, imprint and microstructure. While PZT 30/70 capacitors deposited on LSCO electrodes have excellent fatigue performance and microstructure, the imprint behavior is unacceptable. Doping the PZT films with niobium has substantially improved the resistance of the capacitors toward imprint, while maintaining excellent fatigue properties. However, the PNZT 4/30/70 film microstructure is not as uniform as for the PZT 30/70 films, as small amounts of a fluorite structure second phase and a few large perovskite grains of pancake morphology were obtained. Whether these microstructural nonuniformities are an insurmountable barrier to high density process integration is yet to be determined. PNZT//LSCO capacitor processed at 550°C were acceptable with regard to initial dielectric hysteresis and fatigue behavior for high density nonvolatile memories. Capacitor process temperatures of 625°C and below are required for high density nonvolatile memory technologies with restrictive architectures to maintain device functionality.

Acknowledgements

This work was performed at Sandia National Laboratories supported in part by the U.S. DOE under contract No. DE-AC04-94AL85000 and ARPA. The authors would

like to thank Gordon Pike, Duane Dimos, Walter Olson, Joe Evans, Celeste Drewien, Tom Chavez and Gary Zender for enlightening discussions and technical assistance.

References

- 1 M. Klee, D. Taylor, and P.K. Larsen, Proc. 7th Int. Symp. on Int. Ferroelectrics, 1995.
- 2 P.K. Larsen, M. Klee, Proc. 6th Int. Symp on Integrated Ferroelectrics, 1994.
- 3 R. Ramesh, H. Gilchrist, T. Sands, V.G. Keramidas, R. Haakenasen, and D.K. Fork, Appl.Phys.Lett, 63, 3592 (1993).
- 4 N. Abt, P. Misic, D. Zehngut, and E. Regan, Proc. 4th Int. Symp. on Int. Ferroelectrics 533-40 (1992).
- 5 H.N. Al-Shareef, B.A. Tuttle, W.L. Warren, T.J. Headley, J.A. Voigt and R. Nasby, Appl. Phys. Lett, Submitted (1995).
- 6 D. Dimos, W.L. Warren, M.B. Sinclair, B.A. Tuttle and R.W. Schwartz, J. Appl. Phys, 76 4305-15 (1994).
- 7 W. L. Warren, D. Dimos, G. Pike, B. Tuttle, M. Raymond, R. Ramesh and J. Evans, Appl Phys Lett, accepted for publication (1995).
- 8 G. Pike, W. Warren, D. Dimos, B. Tuttle, R. Ramesh, J. Lee, V. Keramidas and J. Evans, Appl Phys Lett (4) 23 484-6 (1995).
- 9 R.W. Schwartz, B. Bunker, D. Dimos, R. Assink, B. Tuttle, D. Tallant and I. Weinstock, Int. Ferroelectrics, Vol 2., 243-45 (1992)
- 10 J. Robertson, W.L. Warren and B. Tuttle, J. Appl. Phys., 77, 3975 (1995).

DISCLAIMER

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

Figures:

Fig.1. Dielectric hysteresis loops for PZT 30/70 films with LSCO and RuO₂ electrodes

Fig.2. Fatigue characteristics for PZT 30/70 films on LSCO and RuO₂ electrodes

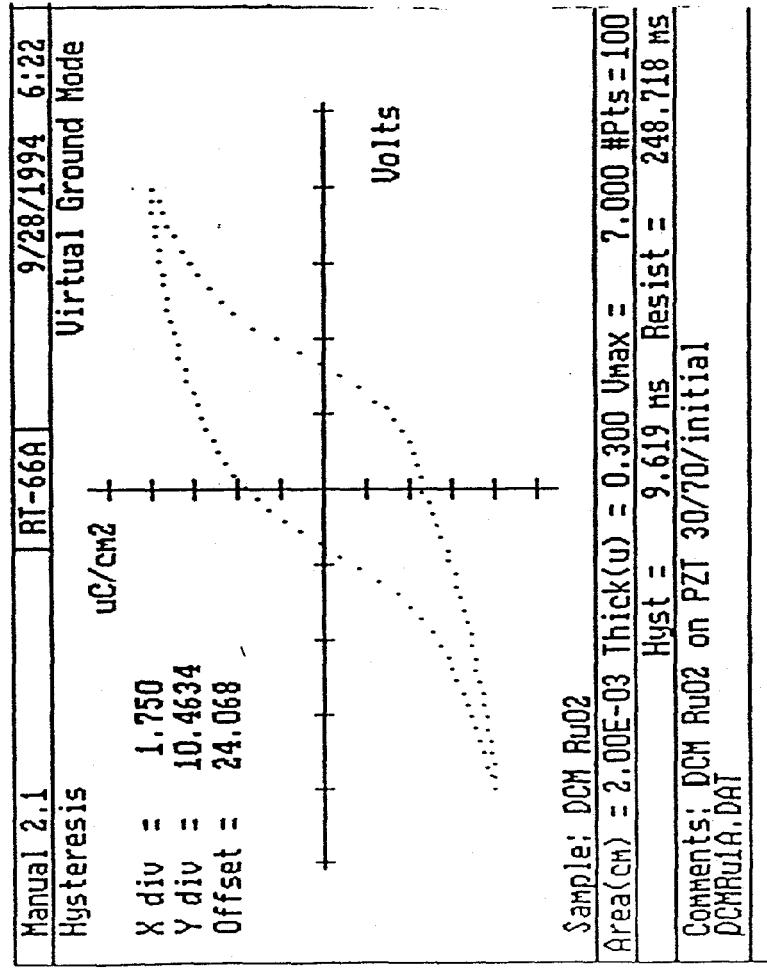
Fig. 3. SEM micrographs of identically processed PZT 30/70 and PNZT 4/30/70 films deposited on LSCO electrodes and crystallized at 675° for 30 min

Fig.4. Cross-Sectional TEM micrograph of PNZT 4/30/70 film deposited on LSCO stack

Fig. 5. Dielectric hysteresis characteristics for PNZT 4/30/70 films crystallized at 675°C and 550°C for 30 min, respectively

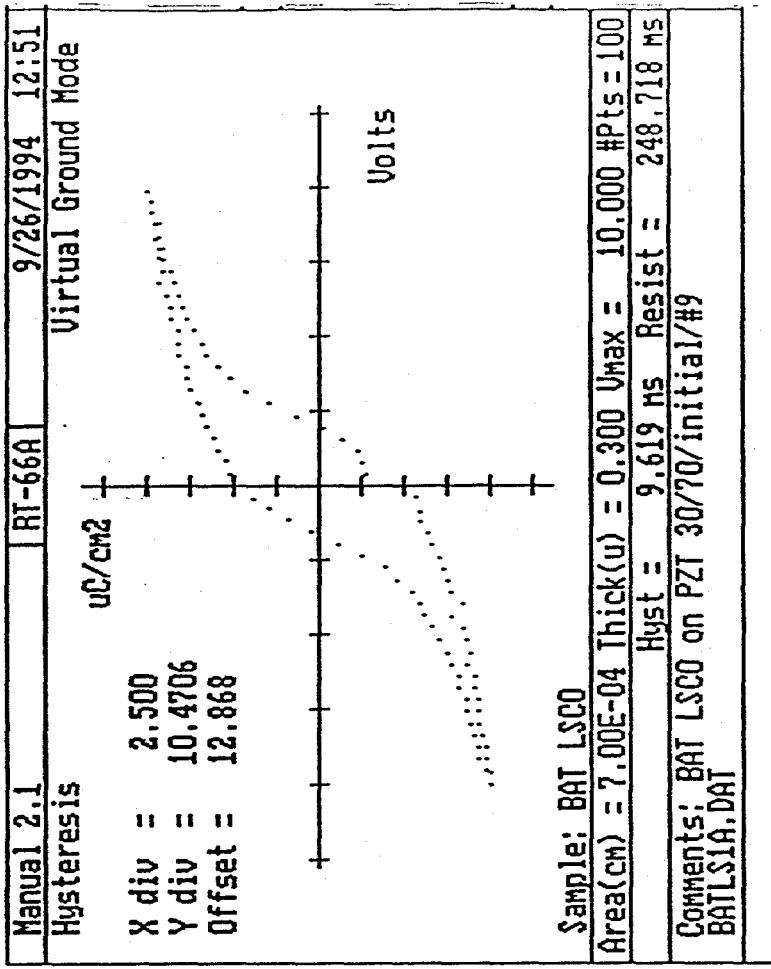
Fig. 6. Fatigue characteristics for PNZT 4/30/70 films crystallized at 550°C and 675°C, respectively

RuO₂ Electrodes



Sample: DCM Ru02
 $\text{Area(cm)} = 2.000E-03$ Thick(u) = 0.300 $\text{Um}ax = 7.000 \text{ #Pts} = 100$
 Hyst = 9.619 ms Resist = 248.718 ms
 Comments: DCM Ru02 on PZT 30/70/initial
 DCMRu1A.DAT

LSCO Electrodes



Sample: BAT LSCO
 $\text{Area(cm)} = 7.000E-04$ Thick(u) = 0.300 $\text{Um}ax = 10.000 \text{ #Pts} = 100$
 Hyst = 9.619 ms Resist = 248.718 ms
 Comments: BAT LSCO on PZT 30/70/initial/#9
 BATLs1A.DAT

Fig. 1.

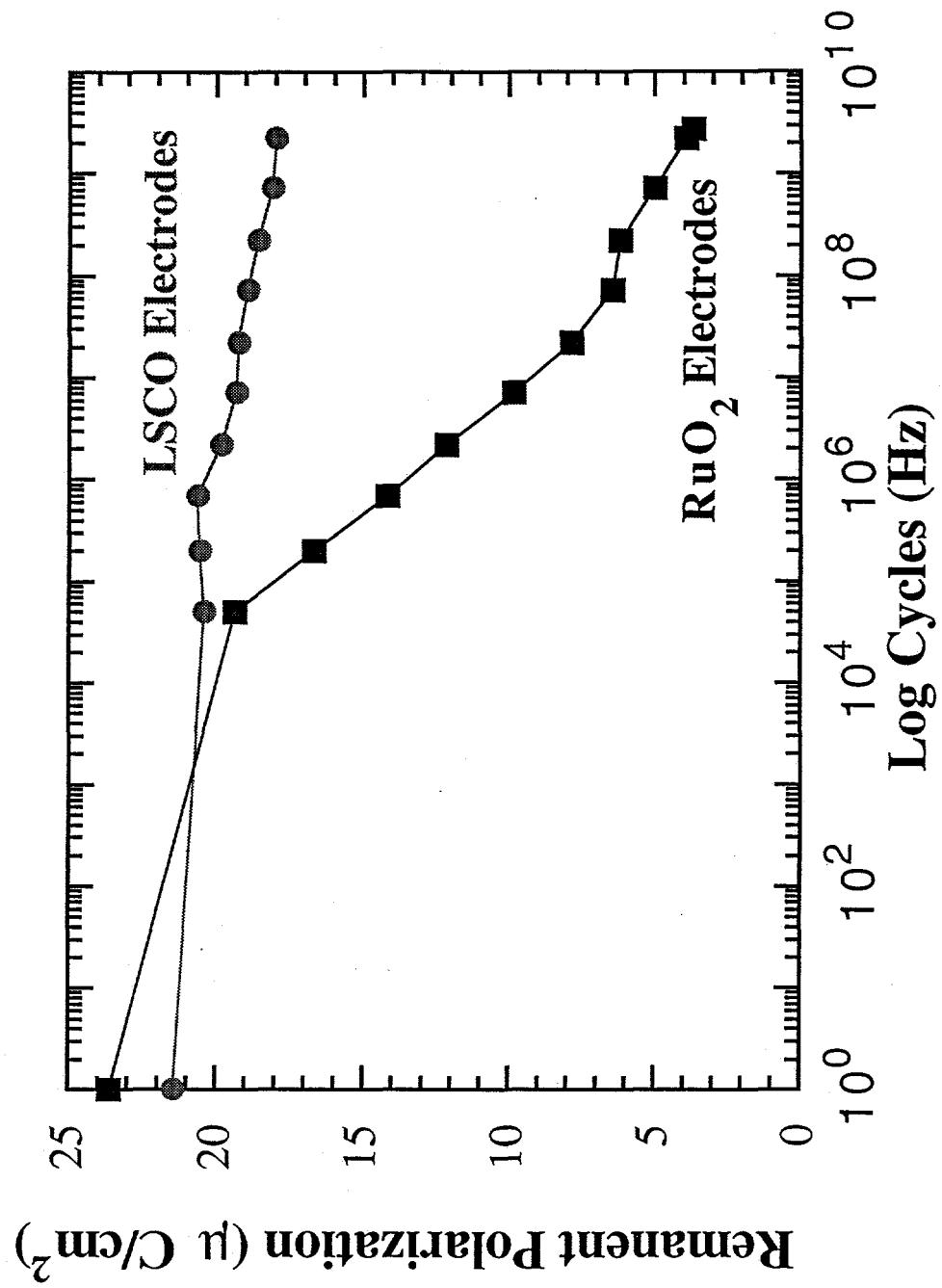
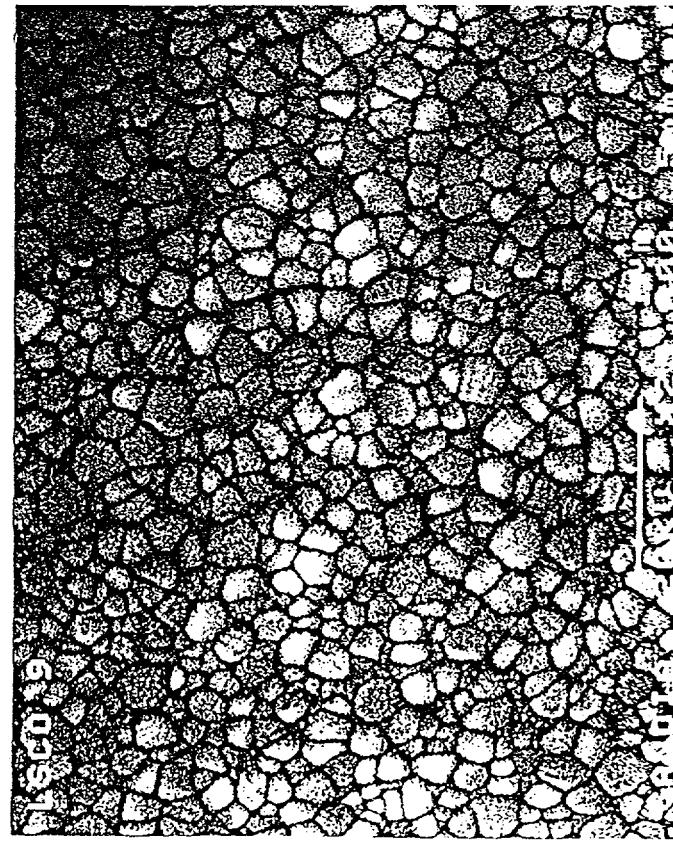


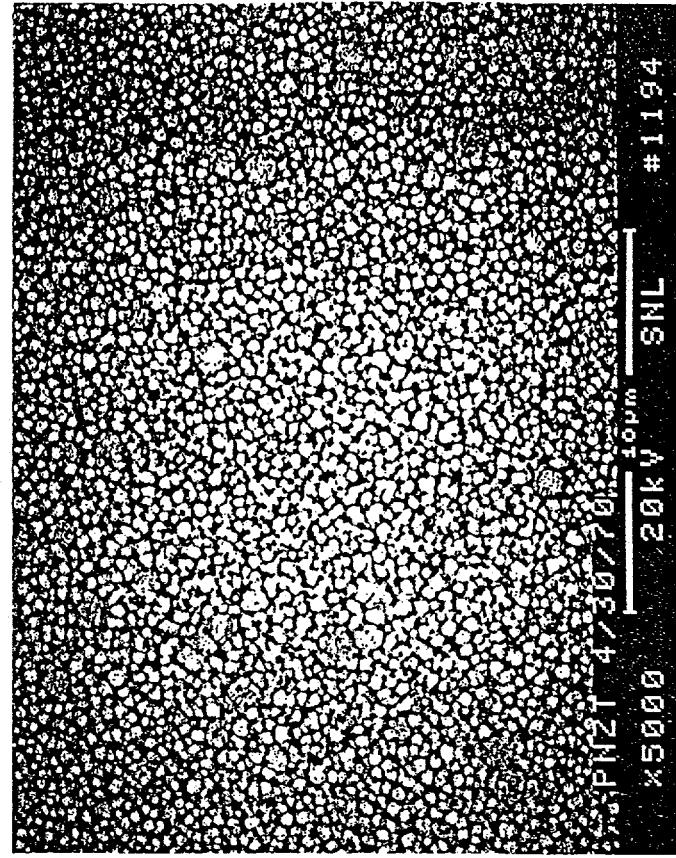
Fig. 2.

Niobium Doping Results In Less Uniform Microstructure

675°C/30min, LSCO//Pt//Ti, h = 300 nm
PZT 30/70



—
1 micron



—
1 micron

Fig. 3.

PNZT Film Has Columnar Perovskite
Grains and Fluorite Minor Phase

675° C/30min, LSCO//Pt//Ti, PNZT 4/30/70



0.1 micron

Fig. 4.

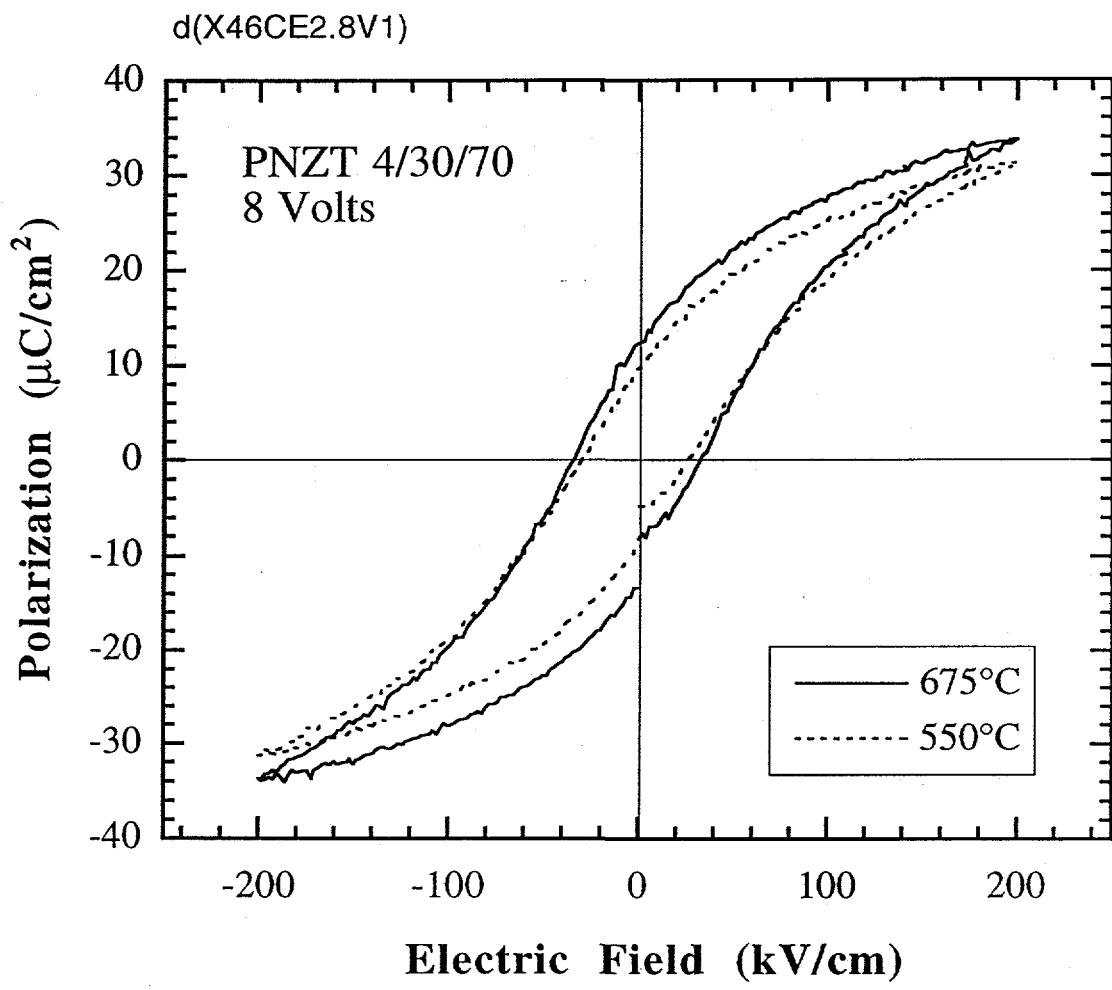


Fig. 5.

d(F46&34.pnzt)

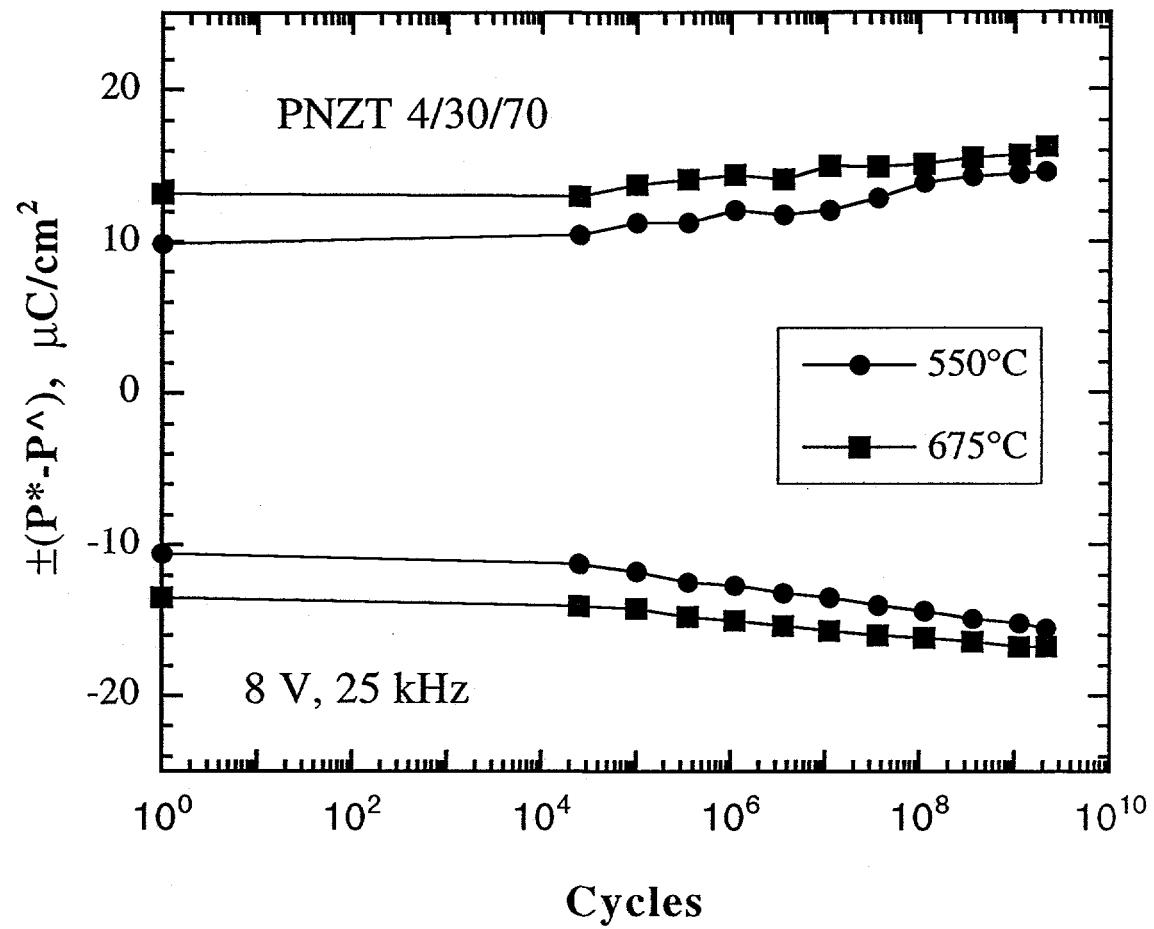


Fig. 4.