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Stable Local Oscillator Microcircuit

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Stable Local Oscillator Microcircuit

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Abstract:
This report gives a description of the development of a Stable Local Oscillator (StaLO) Microcircuit. The StaLO accepts a 100MHz input signal and produces output signals at 1.2, 3.3, and 3.6 GHz. The circuit is built as a multi-chip module (MCM), since it makes use of integrated circuit technologies in silicon and lithium niobate as well as discrete passive components. The StaLO uses a comb generator followed by surface acoustic wave (SAW) filters. The comb generator creates a set of harmonic components of the 100MHz input signal. The SAW filters are narrow bandpass filters that are used to select the desired component and reject all others. The resulting circuit has very low sideband power levels and low phase noise (both less than -40dBc) that is limited primarily by the phase noise level of the input signal.

Contents

Nomenclature

ADS	-	Agilent Corporation's Advanced Design System software
ASIC	-	Application Specific Integrated Circuit
CMOS	-	Complementary metal oxide semiconductor
CSRL	-	Compound Semiconductor Research Laboratory
dBm	-	Decibels relative to one milliwatt
DC	-	Direct current
FY	-	Fiscal Year
GSG	-	Ground-signal-ground probe type
GSSG	-	Ground-signal-signal-ground probe type
GHz	-	Giga Hertz (billion cycles/sec)
HP	-	Hewlett Packard Corporation
IBM	-	International Business Machines Corporation
IC	-	Integrated circuit
IDT	-	Interdigital Transducer
IF	-	Intermediate Frequency
IL	-	Insertion loss
ISM	-	Instrumentation, Scientific, and Medical frequency band
LDRD	-	Lab Directed Research and Development
LNA	-	Low Noise Amplifier
MATLAB	-	Simulation software available from MathWorks
MHz	-	Mega Hertz (million cycles/sec)
Mm	-	Milli-meters
NLTL	-	Non-linear transmission line
NPN	-	A type of bipolar transistor
PCB	-	Printed Circuit Board
PMMA	-	Polymethylmethacrylate
PTC	-	Positive temperature coefficient
RF	-	Radio Frequency
SAW	-	Surface Acoustic Wave
SiGe	-	Silicon germanium technology
SMA	-	Subminiature type 'A' connector
SPICE	-	Simulation Program with Integrated Circuit Emphasis
STALO	-	Stable local oscillator

Introduction

This report describes the development of the Stable Local Oscillator (StaLO) multi-chip module (MCM). The StaLO is a circuit that produces low phase-noise oscillator outputs at 1.2, 3.3, and 3.6GHz from a 100MHz reference oscillator. The StaLO module uses a combination of technologies, all of which had to be developed as completely custom elements.

The StaLO module is based on the concept of a comb generator. A comb generator uses a time periodic sequence of delta-function-like pulses to produce a frequency domain periodic sequence of delta-function-like components. The input reference oscillator is used to produce the time domain pulse train. A series of amplifiers and filters then successively amplify and select the desired frequency components. This is explained in more detail in the Overview section.

The StaLO is assembled using two different integrated circuit technologies and a multi-chip module packaging technology. The comb generator exists in the form of a custom silicon germanium (SiGe) integrated circuit (IC). The chip was designed by the author and produced at IBM using the 0.18μm 7WL SiGe process. The design details of this chip are discussed in the IC Design section. The filters to perform frequency component selection are custom surface acoustic wave (SAW) devices fabricated on lithium niobate or quartz. The details about the SAW filters are covered in the SAW Filters section. The amplifiers are also SiGe circuits designed and fabricated in the IBM 7WL process. The amplifier design and testing effort is discussed in the Amplifier section.

Overview

A block diagram of the complete StaLO is shown in figure 1. It consists of three mostly identical channels, referred to as "slices", to handle the three different frequency outputs of the StaLO. Each slice differs primarily in the center frequency of its SAW filters. It is possible to expand the StaLO to produce different frequency outputs merely by adding additional slices.

A block diagram of the 3.6GHz channel slice is shown in figure 2. It consists of a comb generator with an integrated differential amplifier, two SAW filters, and two amplifiers. The comb generator accepts a 100MHz signal with an arbitrary wave shape, here assumed to be a sinusoid. It then conditions the signal into a delta function pulse train with a 10nsec repetition rate. A delta function pulse train in the time domain transforms into a delta function train in the frequency domain when a Fourier transform is applied to the train. A comb function in the time domain can be described by the following equation

1) $$comb\left[t/T\right] = \sum_{n=-\infty}^{\infty} \delta(t - nT)$$

where each delta function is separated by a time interval, T. The Fourier transform of the comb function is

2) $$F\left\{comb\left[t/T\right]\right\} = T \cdot comb[T \cdot f]$$

indicating that the comb in the time domain produces a comb in the frequency domain with components separated by (1/T). This implies that an input pulse train, generated from a 100MHz wave, will have a spectrum with discrete components separated by 100MHz.

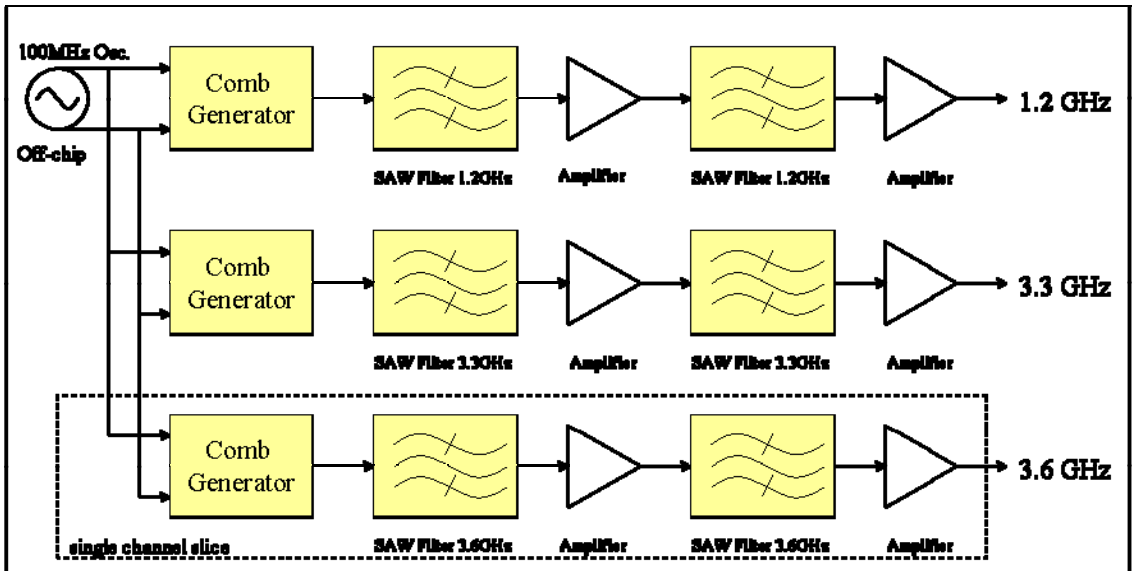

Figure 1: STALO multi-chip module block diagram overview

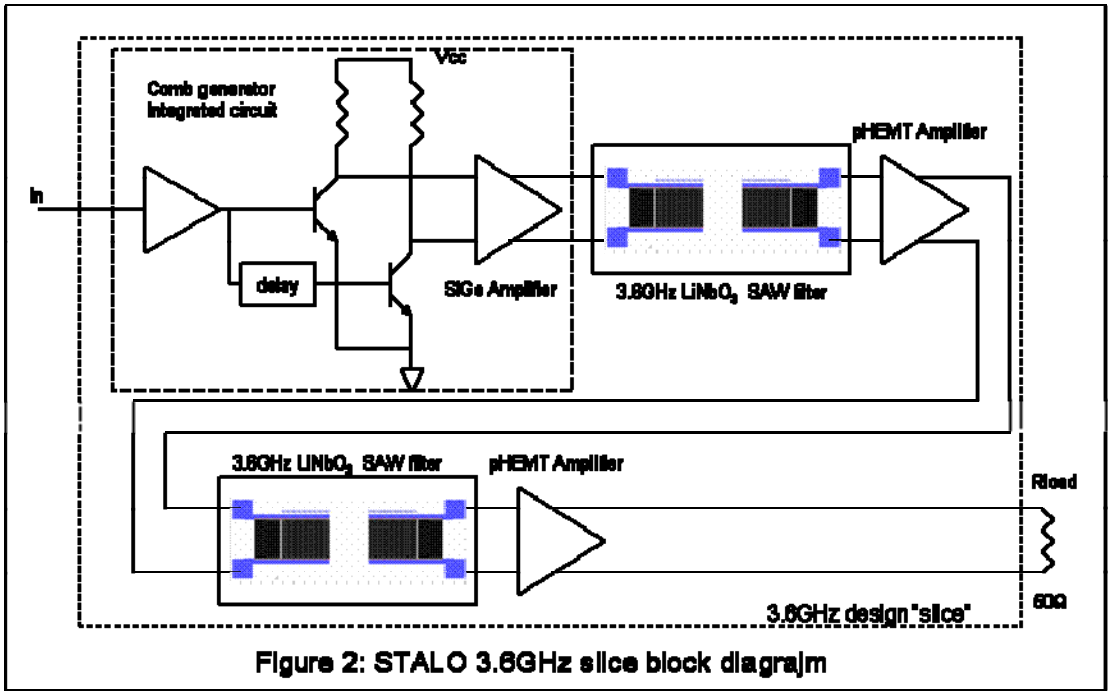

Figure 2: STALO 3.6GHz slice block diagram

These relations hold exactly for perfect delta functions. However, variations from a perfect delta function in the time domain lead to variations in the frequency domain. For example, if the time domain delta function has a finite rise-time, the maximum bandwidth of the comb function in the frequency domain will be limited.

For the transform operation from time to frequency domain Parseval's theorem apply. Parseval's theorem states that the energy contained in the signal in the time domain is equal to the energy contained in the signal in the frequency domain. It can be written as

3) $$\int_{-\infty}^{\infty} |x(t)|^2 \, dt = \frac{1}{2\pi} \int_{-\infty}^{\infty} |X(f)|^2 \, df$$

where x(t) is the time domain signal and X(f) is the Fourier transform of that signal. This theorem implies that amplitude limitations in the time domain will limit the amount of power in each spectral component in the frequency domain. For a circuit without inductors, the output amplitude is limited by the power supply voltage. To maximize StaLO output power, it is necessary to obtain output pulses from the comb generator circuit with voltage amplitudes that are as close as possible to the rail voltage.

Printed Circuit Board Version

A brassboard evaluation module of the 3.6GHz StaLO slice was built first in the form of a series of printed circuit boards (PCBs) joined together via SMA connectors. The circuit block diagram is shown in figure 2. The circuit uses a packaged SiGe transistor, the NESG2101. A view of the PCB version of part of the StaLO slice is shown in figure 3. This figure shows the portion of the StaLO leading up to the first SAW filter. The comb generator is built on a single PCB and SiGe differential amplifiers are built on following separate PCBs.

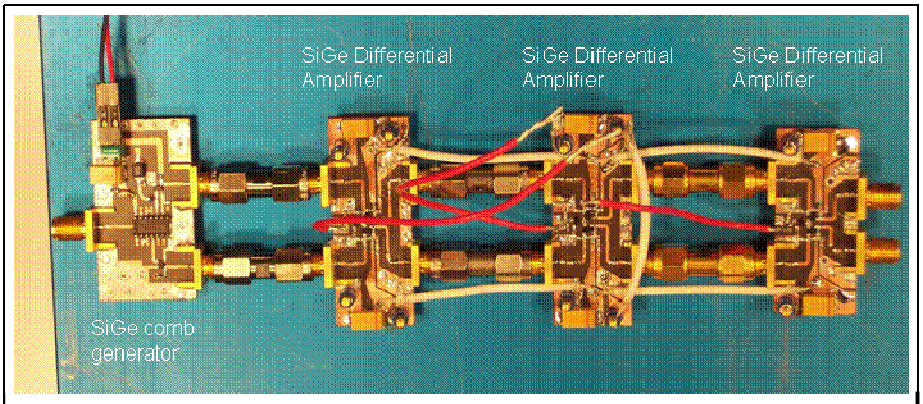

Figure 3: PC Board version of the 3.6GHz comb generator and amplifiers

The SiGe transistor used in the brassboard design, the NESG2101, is modeled using a Gummel-Poon model with additional passive parasitic capacitors and inductors added. The complete model is shown in figure 4. The NESG2101, purchased from California Eastern Laboratories, possesses stated performance that is very similar to the performance of the medium breakdown version of IBM's 0.48 x 20 μm SiGe NPN transistor in the 7WL process. The NESG2101 has V_{ceo} = 5V, f_t = 17 GHz (typical), and a maximum available gain (MAG) of 10dB at V_{ce} = 3V and I_c = 50mA. The IBM medium breakdown 0.48 x 20 μm NPN transistor has a stated V_{ceo} = 4V and f_t = 45 GHz (typical). MAG is not stated for the IBM transistor, and its bias conditions indicate that it peaks in gain at lower currents than the NESG2101. For the IBM transistor actual measured f_t = 17 GHz. In terms of measured performance, the two transistors are similar, with the IBM device achieving its peak performance at a lower collector current.

The brassboard simulator built using the NESG2101 and the 3.6GHz SAWs perform very much like simulation results predict. Each differential amplifier stage only exhibits a gain of about 3-5dB. This is why each amplifier block shown in figure 2 is a set of three differential amplifiers. The set of three amplifiers has a total gain of about 8-12dB at 3.6GHz, depending on bias conditions.

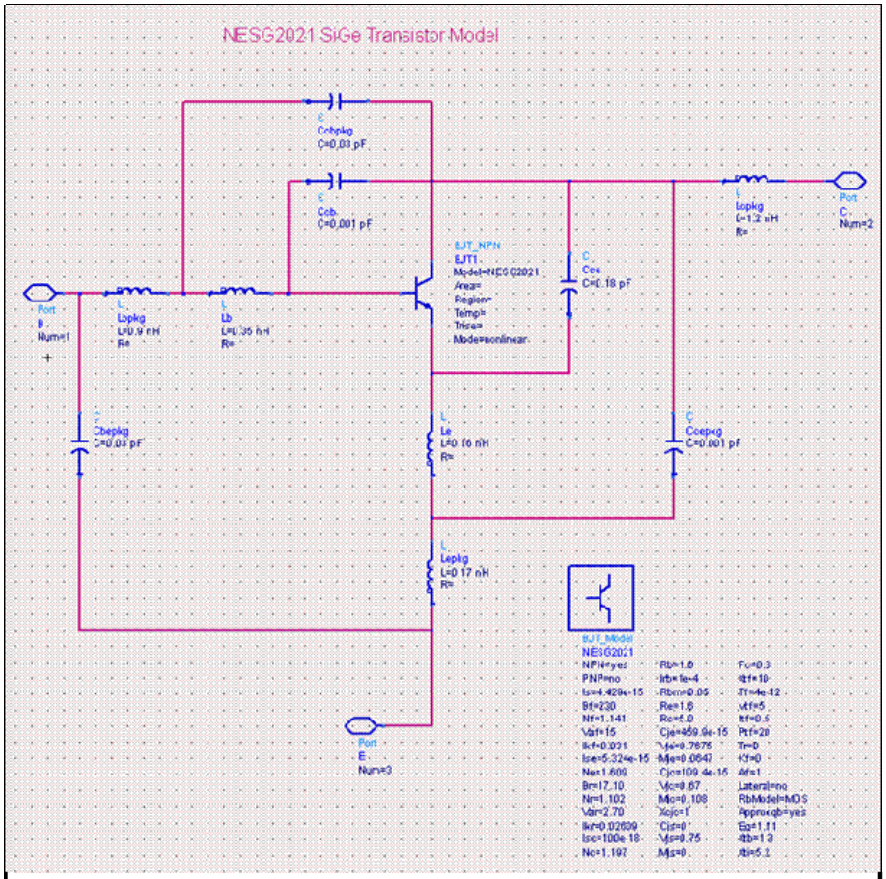

Figure 4: NESG2101 SiGe transistor simulation model

The output of the brassboard comb generator is shown in figure 5. The figure is from an Agilent E4446 Spectrum Analyzer connected directly to the output of the comb generator. One can see that the spectrum contains a broad distribution of components up to at least the 100th harmonic component. Small shifts in bias conditions can produce more of one component at the expense of others. The limits of harmonic generation are determined by the switching bandwidth of the device used to generate the delta functions. Use of a non-linear transmission line (NLTL) can enable the production of shock wave transitions with very wide bandwidths. Generation of signals up to 300GHz can be achieved using these techniques [1].

The output of the StaLO slice taken from the output of the first SAW filter is shown in figure 6. The center frequency is not at exactly 3.60 GHz, since the SAW filter used for development at this point had a center frequency of 3.57 GHz. The input driving frequency was also decreased slightly below 100MHz to compensate for this. The output power in the 36th harmonic, the component used to obtain the 3.6GHz output signal, is about -37.5 dBm or 178 nW. This represents a peak voltage signal of about 4.2 mV into

a 50Ω load. It is possible to increase this signal by preferentially pulling energy from the delta function generator into the harmonic component of choice. This is done by placing a resonant tank circuit at the output of the delta function generator [2]. This technique was not used in the first iteration of the StaLO IC but was added as an experimental comb generator in the second StaLO IC, named StaLO2.

The output signal from the PCB version delta function generator is shown in figure 7. The pulses are about 300 mV base-to-peak. The desired component has only about 1.4% of the amplitude of the original pulse. This represents about a 46 dB loss in power from the original pulse to the desired component. To a large extent, a significant power loss from the delta function to the desired component is inevitable, as it is only the power in the fastest transition of the delta function that can contribute to high frequency harmonic components. Still, such a loss indicates the presence of a good opportunity to improve output power performance and will be explored in subsequent investigations.

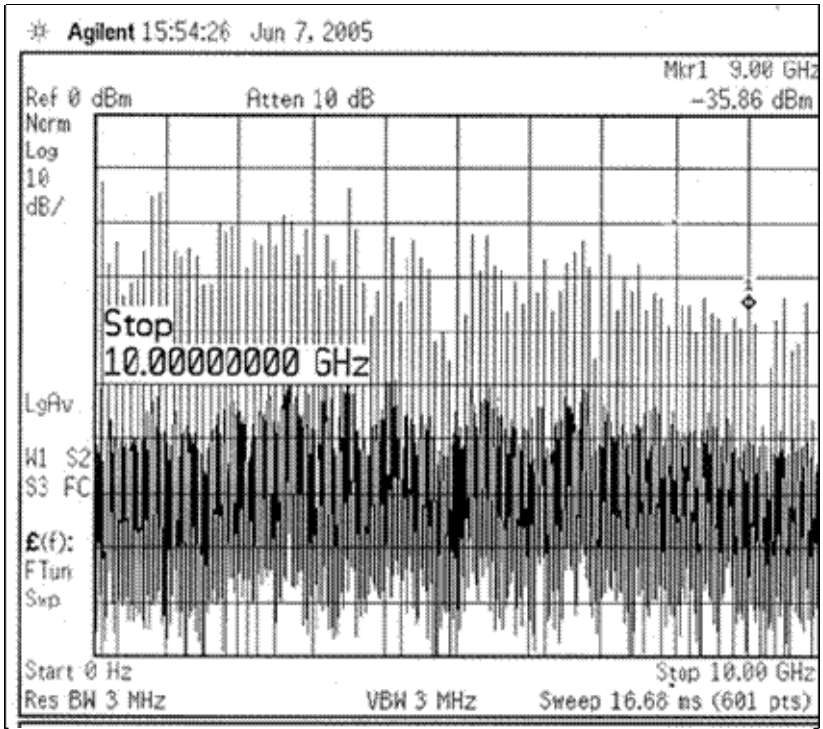

Figure 5 Breadboard comb generator spectrum output.

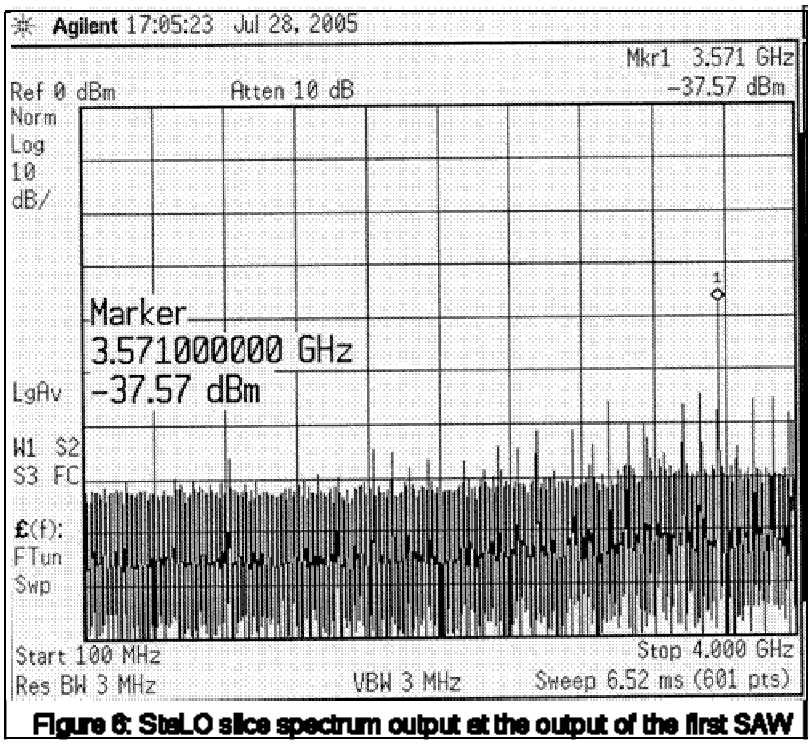

Figure 6: StaLO slice spectrum output at the output of the first SAW

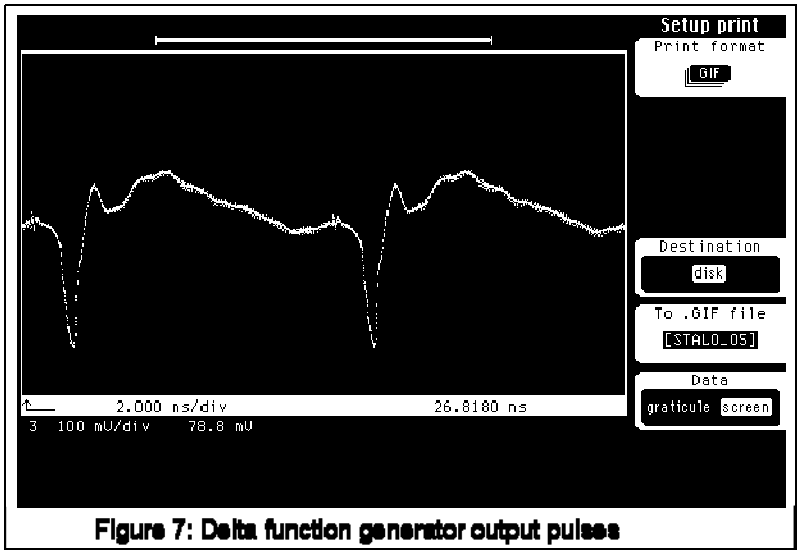

Figure 7: Delta function generator output pulses

Process Overview

Designing in an IBM SiGe process requires a significant amount of design support. The IBM design flow ideally requires a specific set of software tools, acquired at great cost. The toolset required at the time the StaLO was designed consisted of Cadence Analog Artist for schematic capture and simulation, Cadence Virtuoso for cell layout, and Cadence Assura for layout verification. Hspice, Columbus RF, and Agilent Advanced Design System (ADS) all received some degree of support from IBM. Also, certain contingents within IBM reportedly favored other design verification tools, and support for Cadence Assura was in some ways lacking. Since the complete toolset is very costly and not consistent for all processes, the design flow was custom adapted to a simulation and layout toolset that was available at Sandia.

The targeted SiGe process for the StaLO design shifted from the 5AM process to the 6HP process to the 7WL process. Originally, models were prepared for the 5AM process. This process was dropped from the Trusted Foundry program, and we had some concerns that it would not continue to be supported by IBM through Mosis. The targeted process was then shifted to 6HP with the consideration that the first prototype runs would be through Mosis. IBM/Mosis then changed the run format for the 6HP process from the conventional multi-project format to a "taxi-run" dedicated run format. This increased the cost of the prototype fabrication runs by about a factor of four and placed the 6HP process out of reach of the StaLO project. The 7WL process was then targeted for the design. The reason that the 7WL process was selected over the 7HP, 8HP, 9HP, or other processes was because it possessed SiGe transistors with sufficient bandwidth (f_t = 45 GHz) and breakdown (V_{beo} = 3.5V) to produce a 0 dBm output signal at 3.6 GHz.

For simulation, both ADS and Pspice were used. The models as provided by IBM were created by IBM for the Cadence Analog Artist and had to be adapted to operate in SPICE. In the course of the model adaptation, it was discovered that the original models had several parameter errors and even undefined parameters. Evidently, the errors were of such a nature that they did not cause catastrophic errors to the users of Analog Artist, however, performance of these models is suspect, at best. Models suitable for SPICE were created from MathCAD calculations of Gummel-Poon model parameters from the IBM parameter sets.

The measured performance of the transistors from the IBM model parameters was a disappointment, though not due to models themselves. Gummel-Poon bipolar transistor model parameters for SPICE were extracted from a test transistor after the first fabrication run. The circuits were then re-simulated using this model, and the results compared favorably with measured circuit performance. This model was then used to re-design and optimize the StaLO amplifiers for better gain performance.

SAW Filters

The design and processing procedures for producing the SAW filters are highly specialized. Sandia uses a process that is designed to give the highest performance possible in insertion loss and center frequency accuracy. This process is optimized for small scale production only, and the procedure described here is in all likelihood unique in the SAW fabrication business.

There are three SAW parameters that need to be simultaneously optimized during the design and fabrication of the filters used for the StaLO. These are insertion loss, sideband attenuations, and center frequency. The insertion loss is the S_{21} wave attenuation from input to output. It is minimized in order to maximize StaLO output power. It is a function of the substrate material coupling coefficient, the straightness and line-edge roughness of the transducer fingers, and the number of finger pairs in the electrical to acoustic transducers.

The center frequency of the SAW filter is a coarse function of the transducer finger spacing, or pitch. Because the minimum metal width of the 3.6GHz filters is only 80nm, a change of 1nm in metal width will change the frequency by 1.25%, or about 45MHz.

For our purposes, the StaLO needs to be tuned to within 3MHz of its design frequency, so mask design alone is unable to provide sufficient precision for the final filter center frequency. The goal of the design of the SAW filter mask is to put the SAW's center frequency as close as possible to but below the desired center frequency. The reason why the SAW filter is designed with a center frequency below its desired frequency is due to the effect of metal loading. The weight of the transducer metal on the surface of the SAW slows the surface wave slightly and lowers its output frequency below the design frequency. By removing some of the metal thickness through etching, the SAW output frequency can be raised to exactly its design frequency. The etching process is like a fine tune dial on a radio receiver. It doesn't give much range of control, but it does provide for a very fine selection of the final frequency.

The SAW lithography is created to generate one optical mask for gold pads and bus-bars and a series of data files for patterning the aluminum fingers. The SAWs are fabricated using a combination of electron beam (e-beam) machine and optical lithographic patterning. First, a 1 x 1 inch wafer of the desired substrate material in the correct crystallographic orientation is prepared with a coating of e-beam photoresist, polymethylmethacrylate or PMMA (fig. 8). The photoresist is then exposed in the e-beam machine using a series of carefully selected dosages geared to the different mask data types in the physical design. The exposed photoresist is processed by dissolving only the exposed portions of the wafer. After this step, a thin layer of aluminum (500Å) is deposited over the processed photoresist (fig. 9). The aluminum fingers and bus-bars sit directly on the piezoelectric substrate, while the remaining aluminum sits on top of the unexposed photoresist. The aluminum fingers and bus-bars are then removed using a lift-off process to dissolve the unexposed photoresist and remove the aluminum from the wafer field.

The pads and heavy bus-bars are formed next (fig. 10). First, a layer of silicon nitride is deposited over the entire wafer to protect the aluminum metallization from the optical photoresist to be applied next. A layer of optical photoresist is then deposited on top of the silicon nitride, patterned using an optical mask, and developed to expose holes for the pads and bus-bars. The silicon nitride exposed by the holes in the photoresist is etched down to the underlying material. Layers of chromium and then gold are next deposited and patterned using a lift-off procedure of the optical photoresist. The silicon nitride layer is finally removed, and the SAW is ready for initial frequency testing (fig. 11).

The results of the initial frequency testing are used to determine the amount of aluminum etching required in the last process step. The aluminum etchant used is a single step wet-chemical etch followed by a rinse. The etch time has been determined empirically.

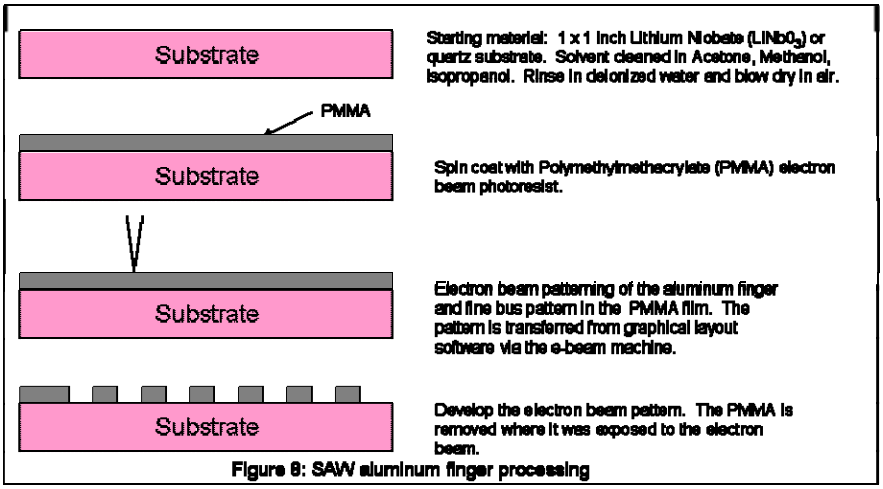

Figure 8: SAW aluminum finger processing

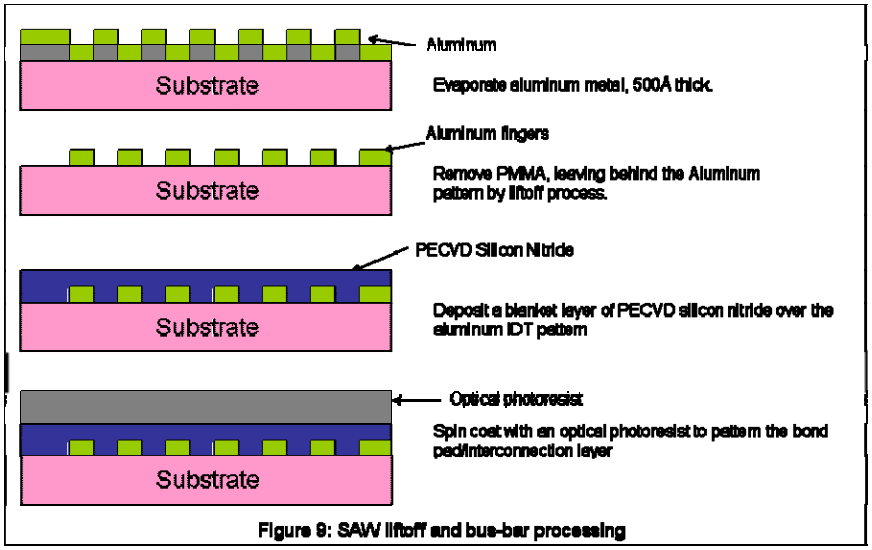

Figure 9: SAW liftoff and bus-bar processing

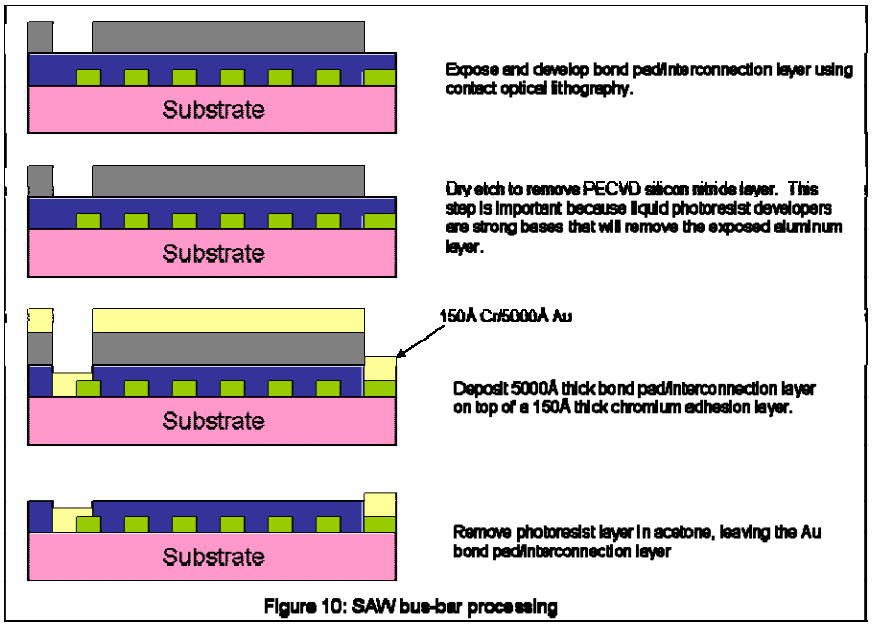

Figure 10: SAW bus-bar processing

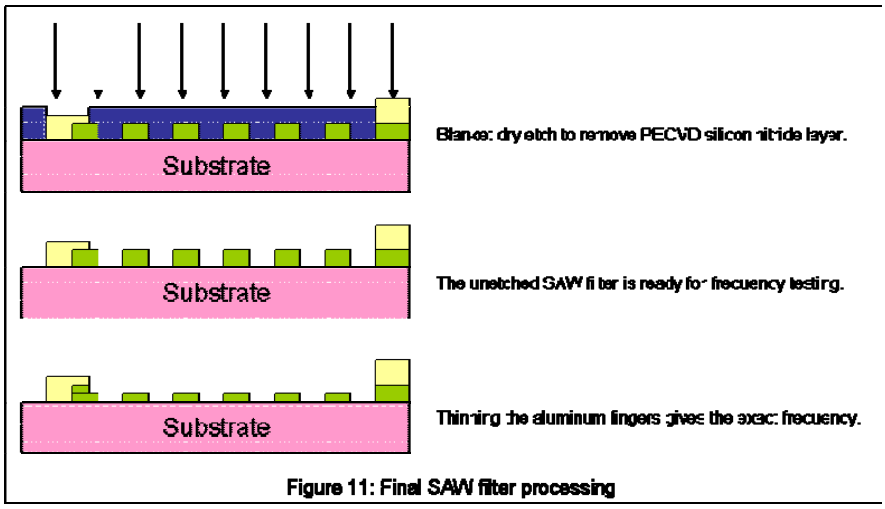

Figure 11: Final SAW filter processing

After the final etch, the SAW is ready for mounting and wire-bonding. The SAW is typically attached using a non-conductive epoxy with low out-gassing properties. This is required to prevent the surface of the SAW from being contaminated. Electrical connections are then made to the SAW using 3-mil gold ribbon wire that is thermo-sonically bonded.

Amplifiers

The amplifiers used in the StaLO slice are custom designed SiGe-based differential circuits. The amplifiers are differential rather than single-ended to take advantage of the 6dB increase in signal level obtained by using a differential signal over a single-ended one. This is made possible by the differential design of the SAW. All SAW filters are built on an insulating substrate and have no intrinsic ground point.

The StaLO amplifier uses an emitter-coupled pair with a simple input matching circuit (fig. 12). The complete amplifier consists of the emitter-coupled pair, dual input matching circuits, dual bias circuits, a tail-current source, and power supply bypassing filters. The amplifier is designed using a standard-sized SiGe bipolar NPN transistor. This standard sized transistor is a device that IBM gives detailed performance data for, and, more importantly, it is a device that we collected transistor model parameters for via direct measurements conducted at Sandia.

Multiple versions of this standard-sized transistor are used in the emitter-coupled pair to increase total collector current and transconductance (g_m). This is accomplished while still using a device with trusted model parameters. The input to the differential pair is matched using a series inductor-capacitor tank circuit. The tank provides a good match at both 3.3 and 3.6GHz. At 1.2GHz, the amplifier has excessive gain, and the gain detuning provided by the matching network lowers the gain and improves circuit stability. Amplifier gain versus frequency is shown in figure 13.

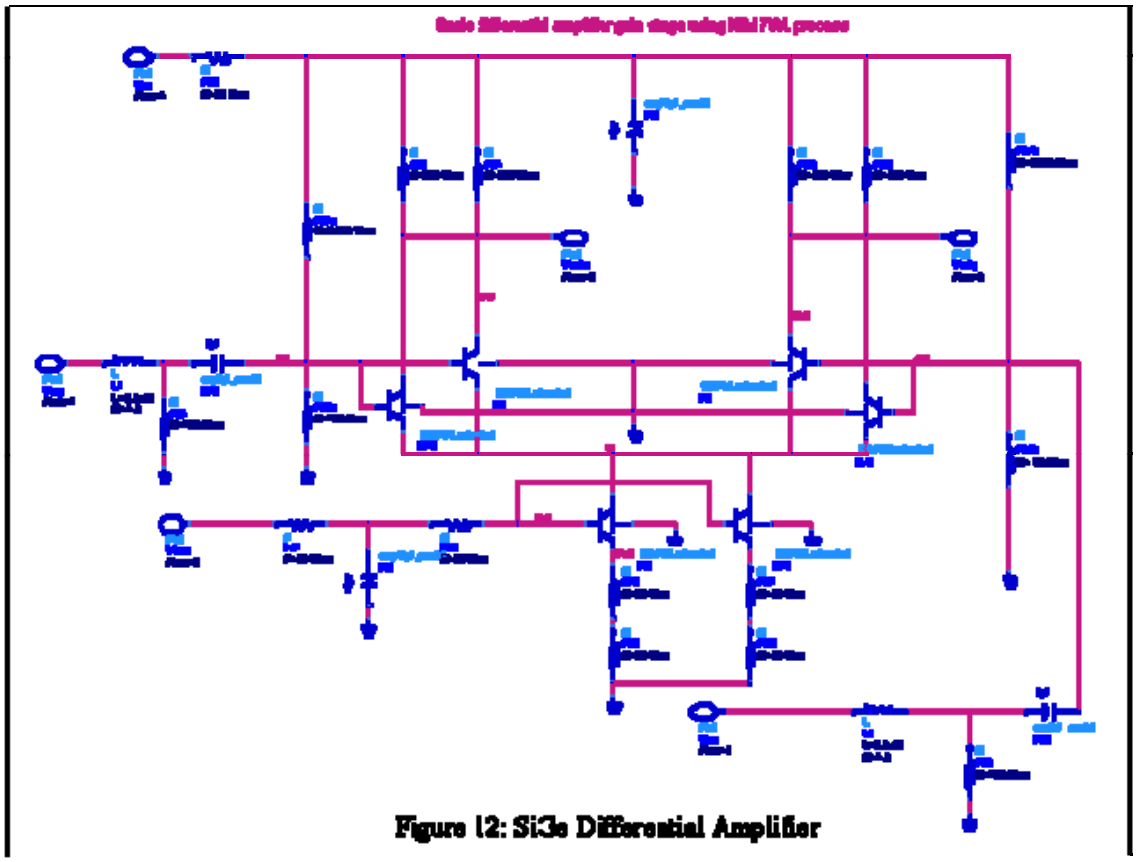

Figure 12: Si3e Differential Amplifier

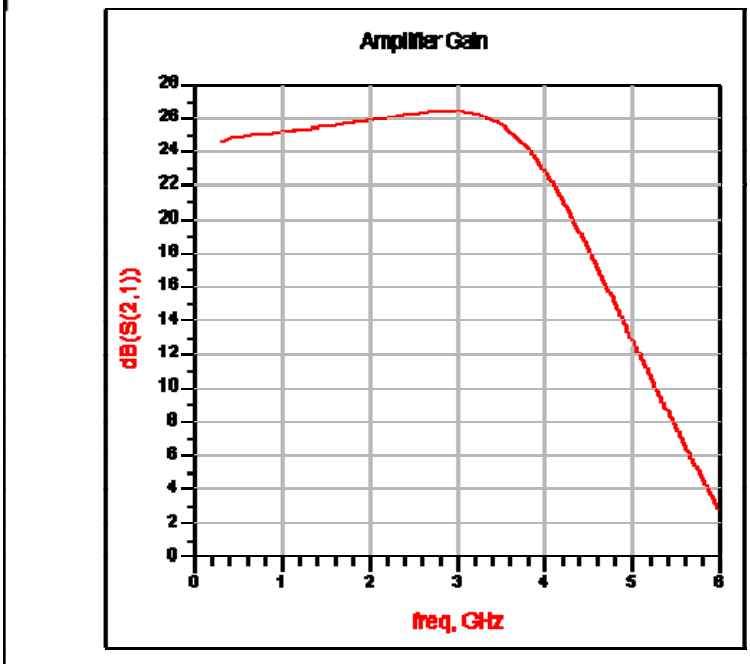

Figure 13: Gain versus frequency response for modified SiGe amplifier

The amplifier shown in figure 12 is a modification of an earlier design fabricated at IBM. As will be discussed in the Test Results section, the original amplifier design did not perform in accordance with simulation results, since IBM SiGe transistor performance was below advertised levels. The earlier amplifier version used single 0.48 x 20 µm transistors where doubled devices are shown in figure 12. It also used no input matching networks on the two inputs. As will be discussed in the Test Results section, the earlier amplifiers have adequate gain for the 1.2GHz StaLO channel, but not for the 3.3 or 3.6GHz channels.

In an attempt to overcome SiGe transistor underperformance, a commercial, single-ended amplifier manufactured by Triquint Semiconductor was tested in the 3.6GHz StaLO slice. There are few commercial amplifiers made for the 3-4GHz region, and the Triquint amplifier had the best overall performance of the candidates. The Triquint amplifier (TGA8061-SCC) has a stated gain of 16dB at 3.6GHz. However, since it is operating in single-ended, rather than differential mode, the gain of the first amplifier stage after the SAW filter can only be 10dB. This is because the conversion from the differential SAW to the single-ended Triquint amplifier cuts the voltage signal in half. The Triquint amplifier was found to have inadequate performance due to excessive power consumption. Details are provided in the Test Results section.

Test Results

The first portion of the StaLO that was thoroughly tested also proved to be the most impressive in its performance. A test circuit including a comb generator and SAW filter was created (fig. 14). The circuit was assembled on a gold-plated Kovar lid. The SiGe comb generator chip can directly accept a ground-signal-ground (GSG) probe, and the SAW chip can directly accept a ground-signal (GS) probe. As a result, there was no need to add separate probe launchers to the substrate.

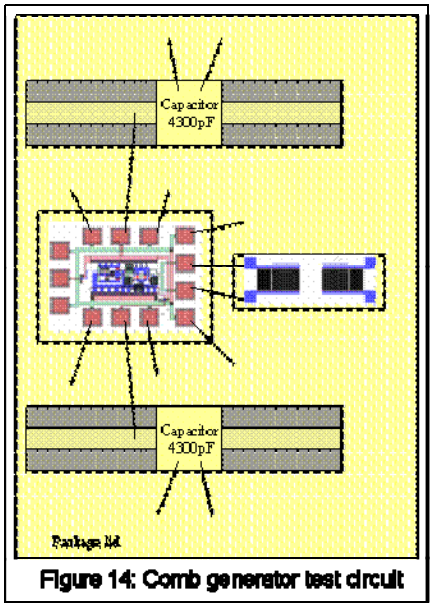

Figure 14: Comb generator test circuit

The top test rail of the comb generator test circuit ties to Vcc and was typically biased at 3.0V (@ 85mA). The bottom test rail of the comb generator ties to the amplifier bias line and was set at 2.2V (@ 2.2mA) to maximize power in the 3.3 and 3.6GHz spectral components. The input to the SiGe chip was driven with a 100MHz signal at $1.5V_{pp}$ though a bias tee with a 0.61V (@1.4mA) DC bias. The spectrum straight out of the SiGe chip, unfiltered by the SAW filter, is shown in figure 15. The 3MHz frequency error in the display is an artifact due to a limited number of frequency steps in the spectrum analyzer. Power is well distributed across the spectral region of interest. Furthermore, it is possible to change the relative power in any of the spectral components by adjusting the amplifier and input DC bias levels. This implies that there are optimal bias settings for specific spectral outputs. The bias and voltage levels stated above were found to be optimal, but a range of values produced similar results.

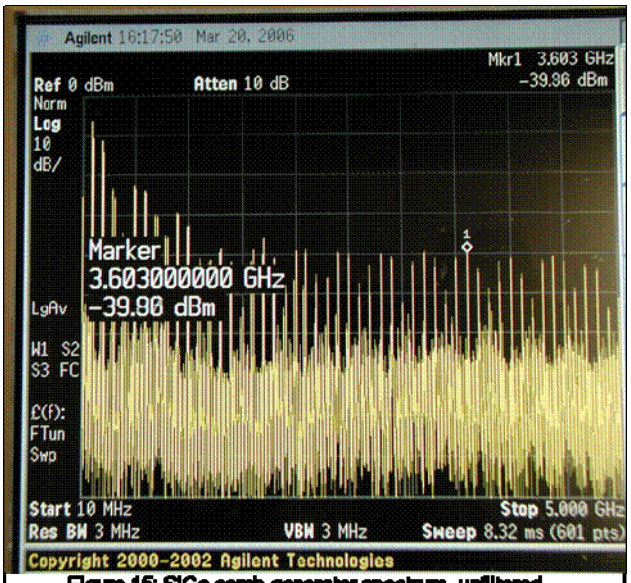

Figure 15: SiGe comb generator spectrum, unfiltered

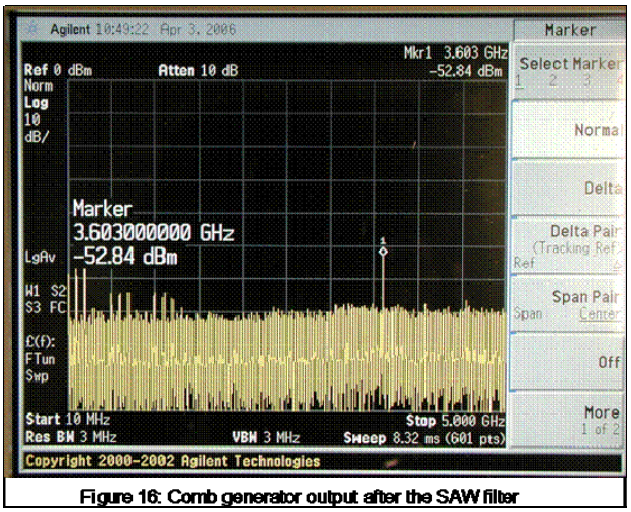

Figure 16: Comb generator output after the SAW filter

The output of the SAW filter following the comb generator is shown in figure 16. The bias conditions are the same as for figure 15. The low frequency spectral leakage is not coming through the SAW filter but is a limitation of the packaging. These components

can be eliminated by better packaging and/or by high pass filtering. Note that the output is what one should expect from the circuit. The output is a narrow bandpass filtered version of the raw comb generator output. The amplitude is reduced by about 13dB due to the insertion loss of the SAW filter. All other spectral components are greatly reduced, including the low frequency components, in spite of the package-induced coupling. The results are adequate, requiring only the addition of gain and elimination of the low frequency leakage.

To provide the additional gain, a test circuit including a SiGe amplifier following the SAW filter was built up (figure 17). As with the previous circuit, this circuit can be driven directly from a GSG probe and read directly from a GSSG probe. The bias and excitation configuration and voltages used were similar to those used for the previous arrangement shown in figure 16. The output signal from the output of the SiGe amplifier is shown in figure 18.

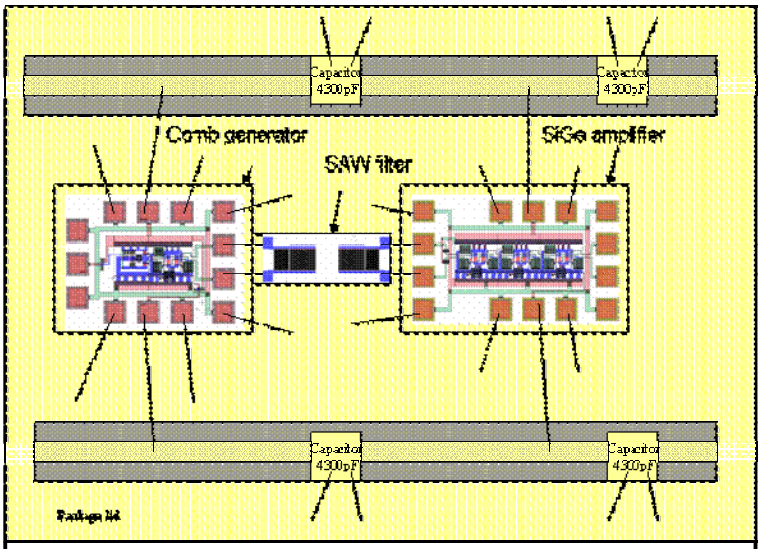

Figure 17: StsLO test circuit including comb generator, SAW filter, and SiGe amplifier

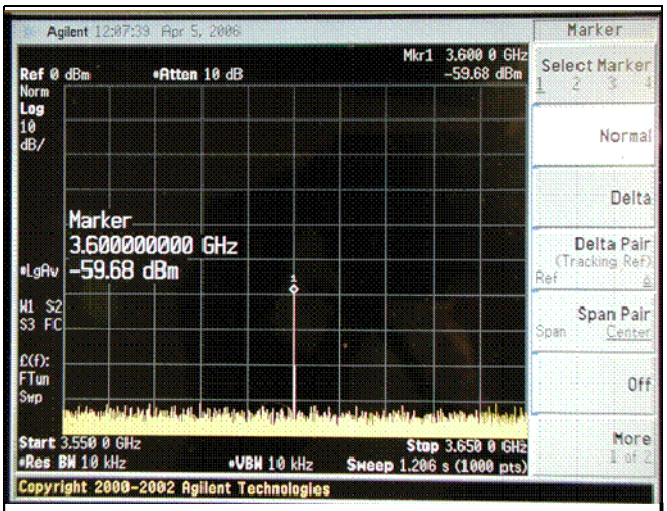

Figure 18: Output of comb generator, SAW, amplifier combination

As can be seen from the comparison between figures 16 and 18, the addition of the amplifier caused the output signal level to drop. The SiGe amplifier provided no gain to the signal. The gain (loss) from these figures can be inferred to be about -6.8dB for the particular amplifier used in the circuit.

To get a more accurate measure of amplifier performance, a separate test circuit was created (fig. 19). The amplifier was probed with a pair of GSSG probes to both the input and output. The amplifier had to be tested in a single-ended rather than differential mode. The resulting gain vs. frequency plot is shown in figure 20. The low frequency oscillations seen in the gain plot are the result of overdriving the network analyzer, an HP8510C. They are not the result of any instability in the amplifier. The plot shown in figure 20 was from the best amplifier tested. It has a net gain of about +2dB at 3.6GHz. The other devices tested exhibited even less gain. The conclusion is that the amplifier as designed using the IBM model possesses insufficient gain at 3.3 and 3.6GHz.

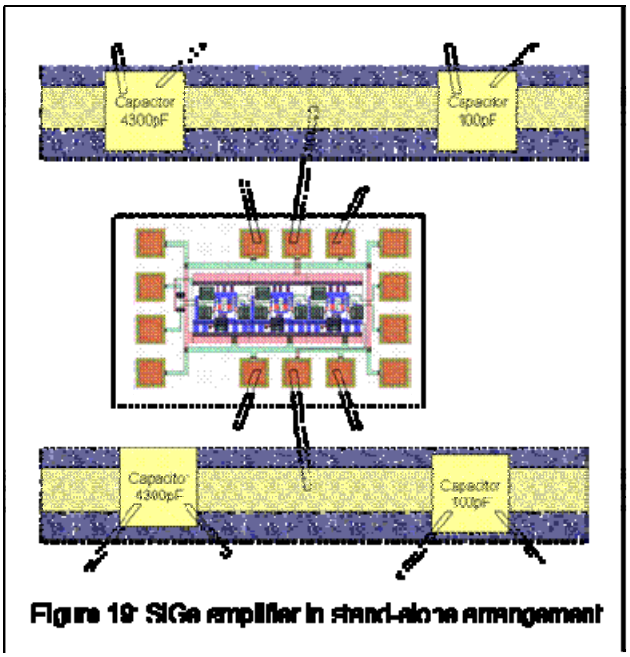

Figure 19: SiGe amplifier in stand-alone arrangement

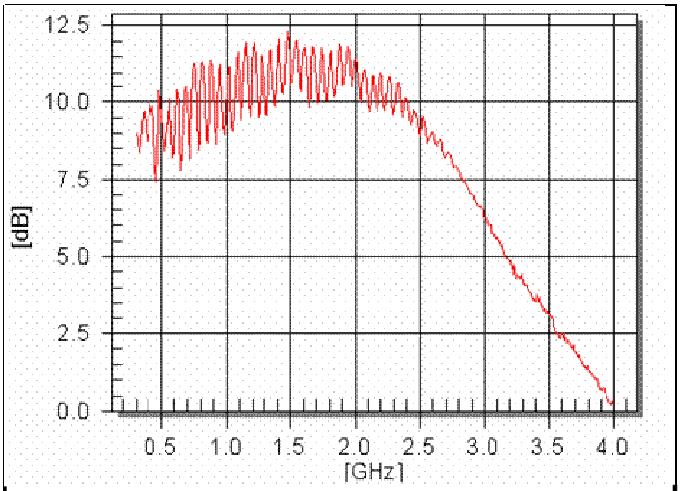

Figure 20: First SiGe amplifier response when tested stand-alone

In an effort to overcome the inadequate gain of the SiGe amplifier, a search was made for a suitable commercial amplifier. A Triquint TGA8061SCC low noise amplifier was one of the few amplifiers with adequate gain at 3.6GHz. It has a stated gain of 16dB at 3.6GHz. A simple test circuit consisting of a comb generator, 3.6GHz SAW filter, Triquint amplifier, and 50Ω probe launch point was constructed (fig. 21). The single ended output of the SAW filter was measured before the Triquint amplifier was added. The output signal strength was -53dBm. The Triquint amplifier and probe launch site were then added to the circuit, and the single ended output of the amplifier was measured. The signal strength was -40dBm, giving a gain of 13dB at 3.6GHz. Two problems were apparent with the circuit, however. First, the output of the Triquint amplifier had sidebands at up to -50dBm, only -10dB below the 3.6GHz harmonic and more than 30dB above the desired level. The change from a differential to a ground-referenced single-ended circuit likely had a significant impact on this undesirable increase in sideband level. The second problem with the circuit was the high power consumption of the Triquint amplifier. This was measured to be 156mA at +12v, or 1.87W for a single amplifier. A total of 4 amplifiers should be needed to obtain an output signal of 0dBm. The power budget for just the Triquint amplifiers would then be 7.5W per StaLO slice and 22.5W for the entire StaLO. This was deemed to be unacceptable.

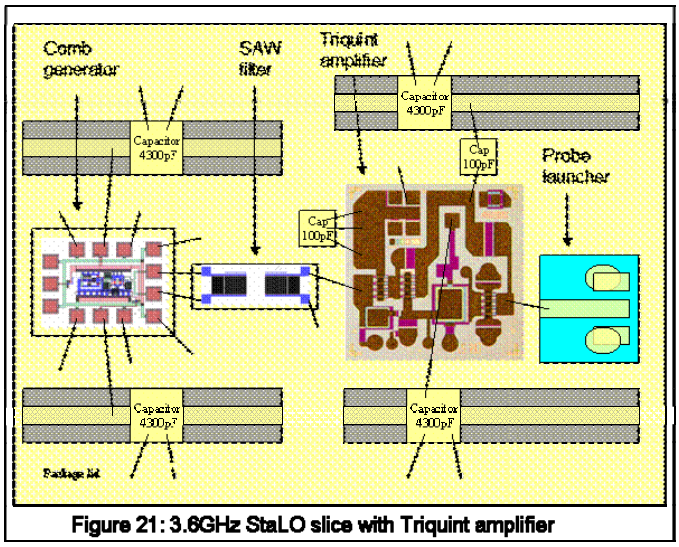

Figure 21: 3.6GHz StaLO slice with Triquint amplifier

The SiGe amplifier was re-designed (figure 12) using the extracted SiGe NPN Gummel-Poon model (figure 22). The transistor exhibited an f_t of only about 17GHz rather than the 45GHz claimed by IBM. The transistor S21 is shown under identical bias conditions to those reported by IBM (figure 23). This plot further confirms the sub-par performance. The extracted model created from the measured data was used to re-simulate the circuit, and the performance obtained was the same as measured by the actual amplifier (figure 24). All S-parameters are predicted very reliably by the extracted model. Note that measured gain saturation shown for S21 at low frequencies is due to exceeding the P_{1dB} for the part. The key point is that the simulations predict the low gain for the original amplifier (figure 25) design. Simulations performed on the re-designed circuit show a gain of about +25dB at 3.6GHz. An actual gain of +10dB at that frequency will be sufficient. The re-designed amplifier was re-fabricated at IBM and is now available for further testing.

```
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param LB = 0.000 '
param CC = 10.00f'
param Q1AREA = 1.000 '
param NPN.IS = 12.35a'
param NPN.BF = 114.7 '
param NPN.NF = 989.4m'
param NPN.VAF = 9.462 '
param NPN.IKF = 4.457 '
param NPN.ISE = 1.0000E-020'
param NPN.NE = 2.058 '
param NPN.BR = 11.70 '
param NPN.NR = 974.8m'
param NPN.VAR = 3.750 '
param NPN.IKR = 100.0 '
param NPN.ISC = 22.97a'
param NPN.NC = 1.147 '
param NPN.RB = 2.000 '
param NPN.IRB = 0.000 '
param NPN.RBM = 2.000 '
param NPN.RE = 16.41 '
param NPN.RC = 31.54 '
param NPN.XTB = 0.000 '
param NPN.EG = 1.000 '
param NPN.XTI = 3.000 '
param NPN.CJE = 148.0f'
param NPN.VJE = 855.0m'
param NPN.MJE = 01.95m'
param NPN.TF = 7.200p'
param NPN.XTF = 2.114 '
param NPN.VTF = 05.75m'
param NPN.ITF = 1.990m'
param NPN.PTF = 0.000 '
param NPN.CJC = 20.75f'
param NPN.VJC = 850.0m'
param NPN.MJC = 1.000 '
param NPN.XCJC = 700.0m'
param NPN.TR = 0.000 '
param NPN.FC = 500.0m'
```

F gure 22: Extracted SiGe transistor Gummel-Poon model

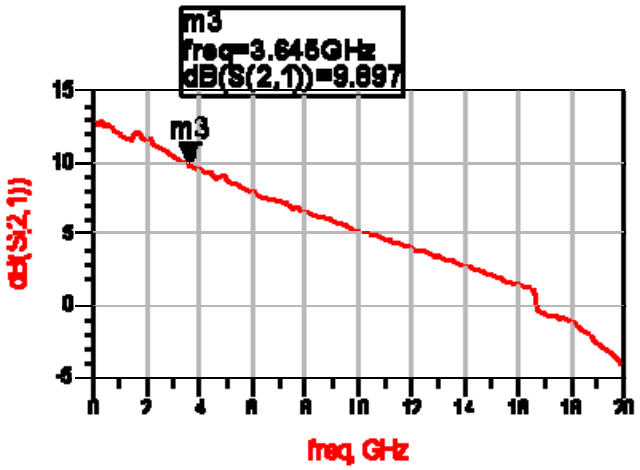

Figure 23: IBM 7WL 0.45 x 20um SiGe NPN S21.

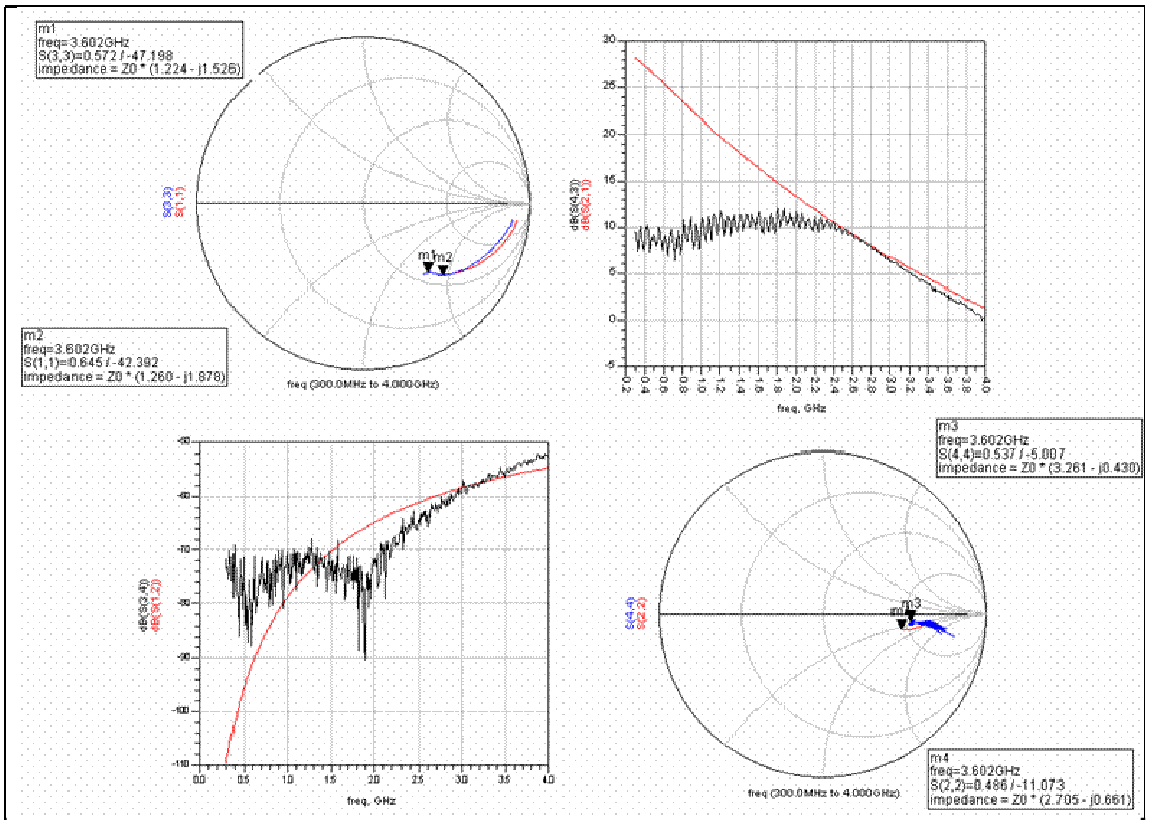

Figure 24: Comparison of SiGe amplifier measurements vs. simulation with extracted NPN model

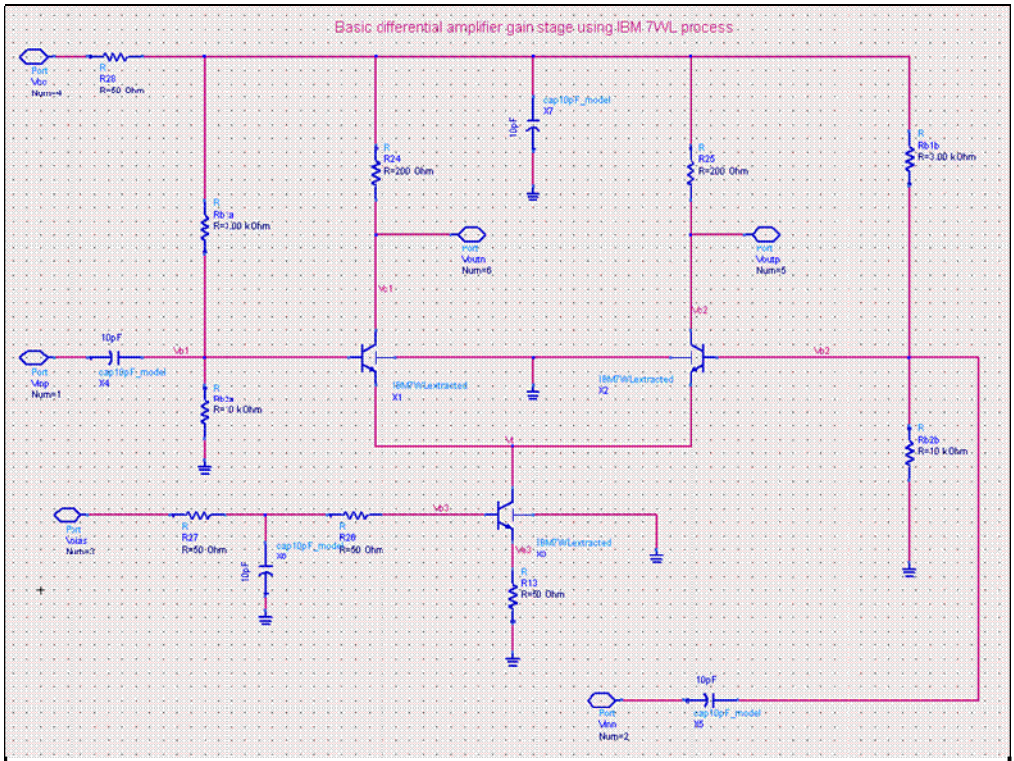

Figure 25: Original, poorly performing design of SiGe amplifier

Conclusion

The StaLO created by a comb generator-based architecture was demonstrated in a printed circuit board version and in integrated circuit form. Components to perform comb generation at all required frequencies, SAW filtering at all frequencies, and amplification at 1.2GHz have been demonstrated. The remaining component needed to complete the StaLO is the SiGe amplifier for 3.3 and 3.6GHz. As of press time, the SiGe amplifiers re-designed based on the Sandia transistor device model had been received but not tested. As a result, further work needs to be done to complete the StaLO assembly. Then, the final, completed StaLO can be fully tested using the completed components.

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1) M. J.W. Rodwell, M. Kamegawa, R. Yu, M. Case, E. Carman, K.S. Giboney, "GaAs Nonlinear Transmission Lines for Picosecond Pulse Generation and Millimeter-Wave Sampling," *IEEE Transactions on Microwave Theory and Techniques*, vol. 39, no. 7, July 1991, pp. 1194-1204.
2) "Harmonic Generation Using Step Recovery Diodes and SRD Modules," *Hewlett Packard Application Note920.*

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