DOE/R7/01314--T7

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May 15, 1995

RE: FEDERAL GRANT NO. DE-FG47-93R701314
COORDINATOR: FRED HART
TO: JAMES D. WELCH, SOLE PROPRIETOR
FROM: U.S. DEPARTMENT OF ENERGY, ENERGY RELATED INVENTIONS.
PROJECT: NOVEL METHOD FOR MAKING SEMICONDUCTOR CHIPS.

SEVENTH QUARTERLY AND FINAL REPORT

INVENTION NO.: 534
OERI NO.: 012693

FOR PERIOD BEGINNING: JANUARY 7, 1995
AND ENDING: MAY 7, 1995

FIRST, MATERIAL DISCLOSED HEREIN IS CONFIDENTIAL AND SUBJECT OF PENDING PATENT APPLICATIONS. PLEASE DO NOT RELEASE ANY OF THE INCLUDED INFORMATION.

DOCUMENTATION OF FABRICATION EFFORTS

Directly following in this Seventh Quarterly, and Final Report under the present funding, I have attempted to summarize the progress of the Research in the last two years, provide analysis of how I feel the Schottky Barrier MOSFET devices fabricated operate, and show some additional Results obtained in the last four months.

After serious consideration of what to provide as documentation of work performed and results achieved over the last two years in this Final Report, I have decided to simply include copies of relevant portions of the Six previous Quarterly Reports, as Attachment "A" hereto. After rereading the prior Quarterly Reports, I have concluded that all I would do is rewrite them were I to proceed otherwise, and that would involve leaving data out if anything. I have included as Attachments, said copies of relevant portions of prior Quarterly Reports, a copy of a presently pending Grant Application, and a copy of a presently pending Patent Application which resulted from the Research efforts supported by the DOE.

FOLLOWING THEN IS:

1. HISTORICAL ACCOUNTING OF SUPPORTED RESEARCH EFFORTS;

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2. ANALYSIS OF HOW FABRICATED DEVICES PROBABLY OPERATE WITH ACCOMPANYING VISUAL RESULTS WHICH DEMONSTRATE AND SUPPORT THE THEORETICAL CONSIDERATIONS;
3. ADDITIONAL FABRICATION EFFORT RESULTS ACHIEVED IN LAST FOUR MONTHS.

ATTACHMENTS

"A"---COPIES OF RELEVANT PORTIONS OF THE FIRST SIX QUARTERLY REPORTS SHOWING RESULTS ACHIEVED OVER THE LAST TWO YEARS;
"B"---COPY OF PENDING GRANT APPLICATION TO ALLOW INVESTIGATION OF NONINVERTING AND INVERTING SINGLE DEVICE EQUIVALENTS TO CMOS;
"C"---COPY OF PENDING U.S. PATENT APPLICATION.

HISTORICAL ACCOUNTING OF SUPPORTED RESEARCH EFFORTS

Work under DOE Grant No. DE-FG47-93R701314, to investigate a Novel Process for Fabricating MOSFET Devices, has progressed to a point where feasibility of producing MOSFETS using Chromium Disilicide Schottky barrier junctions at Source and Drain has been shown. Devices fabricated, however, show inconsistent operating characteristics from device to device, and further work is required to overcome the defects. Some fabrication procedures have produced a relatively high, (eg. ninety-five (95%) percent), yield of devices on a substrate which show at least some transistor action, while others have resulted in very low yield, (eg. five (5%) percent). Consistency of results from device to device is less than desired. However, considering that the University of Nebraska at Lincoln (UNL) Electrical Engineering Fabrication Lab is not what industry can provide, it is reasonable to project that essentially one-hundred (99.99+%) percent yield should be achievable in an industrial setting because of the simplicity in the fabrication procedure.

The Grant was initially provided to allow Research into applying the process of Patent No. 4,696,093 to the Principal Investigator Welch, to the end that MOSFET Devices would be fabricated. The goal of the work was to fabricate CMOS from seriesed N and P-Channel devices on a single substrate. While that goal was not achieved, very significant results have been achieved, and the identified goal is, with further funding, within grasp, as are additional goals identified during the work so far completed, (eg. Non-Inverting and Inverting Single Device Equivalents to CMOS, described supra herein).

The first Phase of the work involved obtaining supplies and then progressing to show that Chromium deposited onto N and P-type Silicon by a vacuum evaporation process, followed by an

anneal process, produced rectifying junctions on both the N and P-type Silicon. The first attempt at producing said rectifying junctions was successful when Chromium was deposited onto both N and P-Channel Silicon in an electron-beam evaporator, followed by a fifteen minute anneal at 350 Degrees Centigrade. The resulting Rectifying Junctions showed Current-Voltage characteristics with a few tenths of a volt forward conduction knee, and with 20 - 30 volts Reverse breakdown. Further work revealed that if the anneal temperature was raised to above 600 Degrees Centigrade, the Reverse Breakdown Voltage was increased to near 100 volts. This occurred on both the N and P-type Silicon. (Note that this verifies the results the Principal Investigator achieved on N-type Silicon in 1974 during his Masters Research, and extends said results to the case of P-Type Silicon). It was also determined that Rectifying Junctions resulted from the above procedure when as little as eight-hundred (800) Angstroms of Chromium was deposited atop the Silicon Substrates.

With the above results secured, attention was turned to fabricating MOSFET Devices. Masks were obtained which allowed forming MOSFET Drain-Source separated by a Gate patterns in substrates, by Photolithographic and Etching Techniques.

Three Thousand Angstroms of Silicon Dioxide was grown atop N and P-type Silicon substrates at the University of Nebraska at Lincoln, (UNL), in a wet steam atmosphere, and then Source and Drain openings were wet etched using Buffered Hydrofluoric acid to effect Drain and Source holes through the Silicon Dioxide to expose the Silicon. In some devices the Silicon was also etched, to depths of up to two (2) Microns. Note, that Silicon etched by wet acid techniques etches isotropically. That is, the Silicon Dioxide is laterally undercut, with respect to a Silicon Dioxide edge, by the wet acid etch, a distance approximately equal to the depth to which the Silicon is etched. Next, Chromium was deposited over the resulting substrates to a depth of eight-hundred (800) Angstroms. It was hoped that the Chromium would deposit atop the Silicon Dioxide and atop the opened Silicon such that a discontinuity would result therebetween, that the Chromium atop the Silicon would, during an anneal, form Source and Drain Rectifying Junctions, and that atop the Silicon Dioxide would act as Gate Metal. It was expected that this would occur, much as snow on stair-steps forms discontinuous vertical regions between successive steps if the snow is not too deep. It was particularly expected that this result would be achieved where the Silicon Dioxide was undercut laterally by a wet acid etch. That is, it was thought that deposited Chromium would not deposit under the edge of etched Silicon Dioxide. Many attempts at achieving this, however, were unsuccessful. When I ran into the identified problem I approached UNL Professor Ianno and inquired as to our ability to do dry plasma etching at UNL. He responded that he was an expert in the area. The reason for

Etching Silicon Dioxide by Dry Plasma Techniques is that it provides a very vertical anisotropically etched edge, as opposed to a tapered Silicon Dioxide edge result provided by wet acid techniques. The more vertical the etched edge, the more likely we could achieve a Chromium Deposition wherein the Silicon Dioxide edge was free of Chromium. Using the stair-step and snow analogy again, it will be appreciated that is easier to obtain discontinuity between vertically oriented successive steps than along a ramp. What we repeatably found, however, was that deposited Chromium was able to form a short between the Source and Drain. Somehow the deposited Chromium was able to adhere to the edges of the Silicon Dioxide, and even thereunder in laterally etched regions formed by a wet acid Silicon etch. We theorize that our Chromium Deposition technique was not sufficiently "Line-of-sight" to achieve the desired result. Deposited Chromium atoms must have been able to rebound after initial impact with Silicon and come to rest on the edges of the Silicon Dioxide, and even under laterally etched Silicon Dioxide. It is possible that the technique might still be workable, but we were not able to achieve results using it. I am maintaining my 093 Patent to the approach, as a testament to my belief that the technique can still work.

At this juncture I decided to etch the Chromium on the substrates we had produced a bit, in a wet acid etchant. I hoped that the Chromium on the edges of the Silicon Dioxide would be thinner than that atop thereof, and that I'd be able to remove just enough of it to achieve discontinuity between the Source and Drain regions and still have some present atop the Silicon Dioxide to act as a Gate. What occurred however, was that by the time I achieved discontinuity between the Source and Drain, all Gate metalization was etched away. At this point, with really no expectation of success, I decided to probe the resulting structures and apply electrical signals with the UNL Hewlett-Packard Curve-Tracer Test Set. As a bit of insight, the day I did this, (April 27, 1994), I had tickets to the Bob Dylan concert, said concert being scheduled for that day's evening. I had nothing else to do that afternoon, so decided to "play" a bit and kill time until the concert. About 2 P.M. Professor Soukup had come to the Lab to talk to his technician, and when preparing to leave looked over, saw me "playing" and commented with his dry sense of humor, (of which I am not being at all critical as it is actually similar to my own sense of humor!), "I see Jim is over there---that Jim, he has no idea what he's doing". While he was quite correct, I looked up and with a smile said "You're going to eat those words". Dan, the technician, then came over and asked me, "Don't you really know what your'e doing?". I smiled and responded "All I know is he gave me an "A" in Solar Cells". With that stage set I went on "playing", and about 20 minutes later, after placing the probes on a device such that the Gate probe simply rested atop the Silicon Dioxide and the Drain and Source probes contacted the Drain and Source regions, pushed the test set button, and "ALA---MOSFET Curves appeared!". I took a plot of them and walked into Professor Soukup's office and just

stood there with the print-out held out in from of me. He looked at them and said "It looks like you have it". I agreed. Then I went and had Chinese food for dinner, then went to the Dylan Concert and then came back to the Lab for a late night repeat of the earlier success. The next day, (April 28, 1994), I "typed" the substrate which had yielded curves, using a standard semiconductor typing "Hot-Point-Probe" technique, and found that the substrate I'd worked with the day before was P-type. I processed an N-type substrate in a similar manner and found similar curves, but they were in the first, rather than third quadrant. This showed we were seeing the effect of substrate type.

(I'll add, possibly inappropriately, that being a long time Bob Dylan fan---perhaps the magic of his being in town provided the atmosphere for the breakthrough. Perhaps not. The Scientific community, at least will never buy that analysis! However, as Scientology, (which I've studied for years), teaches, intangable aesthetics do play an ellusive role in success).

Continuing, while it had become apparent that the concept of using Chromium-DiSilicide as Source and Drain Junction material in MOSFETS was valid, it was obvious that we needed a procedure which would provide devices with a remaining Gate metal. This was so as it was difficult to set the Gate probe to achieve the curves I had stumbled onto, and once achieved, any bump of the probe stand caused them to vanish. As well, any potential industrial usage would require a gate metal be present. In consultation with Professor Ianno, the concept developed that we could add one step to the procedure and achieve the desired result. The added step was a deposition of Aluminum over the Silicon Dioxide prior to etching through the Silicon Dioxide, via the then present Aluminum, to expose the Silicon. We did this and found that we did achieve the desired structure. The reasons this worked is that the wet acid etchant for Chromium does not etch Aluminum to any noticeable extent, nor does it etch Chromium Disilicide. Hence our procedure became:

1. Provide an N or P-type Silicon Substrate.
2. Grow Silicon Dioxide atop thereof.
3. Deposit Aluminum atop the Silicon Dioxide.
4. Etch Source and Drain openings to the Silicon, through the Aluminum and Silicon Dioxide.
5. Deposit Chromium over the resulting system.
6. Anneal the System to form Chromium Disilicide in the Source and Drain Regions.
7. Etch remaining Chromium away by a wet acid technique.

As mentioned, said procedure did provide the structure we desired. That was observable using microscopes, including an

electron-microscope. However, since I had initially stumbled onto the Curves I had achieved, others had used the test set. When I had reconfigured the test set, I could no longer repeat my previous success. This, of course, led me to speculate to myself that the Curves I'd initially achieved were not valid. Perhaps I'd configured the test set wrongly the afternoon I'd first obtained the Curves etc. Finally, approaching anger, I contacted Hewlett-Packard and questioned them as to why what I was experiencing might be occurring. In telephone discussions with a Hewlett-Packard Engineer I learned that small 1 - 2 inch long Interface Adaptors which change three prong connectors on the test set to two prong connectors for interface to the probe stand, must be of the right type to work. That is, there are multiple possible lead interconnections inside an adaptor. What I discovered was that one of the Adaptors present was simply bad. It shorted out voltage applied between its inner terminal and the outer ground braid when the voltage reached 0.7 volts. This was not detectable with an ohm meter. I'd tested it, and the other Adaptors and leads with a ohm meter earlier and did not find the problem. The problem was a true "Gotcha" using the word the Hewlett-Packard Engineer used when clueing me into the scenario. Anyway, with that known, it became apparent that when I'd achieve the Curves I had stumbled onto the afternoon preceding the Dylan Concert, the faulty Adaptor had, by blind luck, been placed upon the Source lead. When present there, shorting problems did not matter as a short is present across said lead inside the Test Set anyway. However, when the Adaptor was placed at the Drain or Gate lead, it prevented voltage from actually appearing at the Devices under test, even though the Test Set showed application thereof.

With the Test Set then working, it was discovered that nearly every substrate upon which we had fabricated devices provided some devices which would demonstrate Curves when tested. The remaining problem, however, was that the reproduceability and consistency of results was not at all under control. This problem remains.

Next, upon achieving the first Curves, I prepared a Patent Application and submitted it to the U.S. Patent Office, for the purpose of obtaining a Patent Search. That Application (Serial No. 08/250,906, filed 05/31/94), served its purpose when a First Office Action provided Patents of which I had not previously been aware. None reported investigation of the use of Chromium in fabrication of MOSFETS, but some did identify the use of Schottky barrier junctions in MOSFETS. After receiving the Office Action I was in Washington D.C. regarding some Patent work for a Medical Doctor Client, and I stopped in and saw the Examiner, (Examiner Loke), for the Application. He provided me with an additional Patent, and I did some Searching myself.

Also, another concept which had been developing in my mind for quite some time, and for which we did some initial fabrication work, has shown promising results. The concept involves production of single devices which have operational characteristics similar to multiple device CMOS systems. I am including, as Attachment "B", a Grant Proposal submitted to the Air Force SBIR Program. A similar, Application has also been submitted to the DOE Energy Related Inventions Program.

I prepared a new Patent Application which is a CIP of the first, and submitted it. The Serial No. of which is 08/368,149. The focus therein is on the Single Device Equivalents, and on the use of a fabrication technique leading to a low leakage current, limited Schottky barrier cross sectional area geometry. Use of isotropic Silicon etching, and selective Silicon Dioxide growth provides a structure in which the Schottky barriers are present only at the ends of channel regions in MOSFETS, said Schottky barrier junctions being present under Gate Silicon Dioxide. A copy of the Patent Application is included in Attachment "C".

Directly following is an Analysis of how the Fabricated devices are probably operating.

ANALYSIS OF SCHOTTKY BARRIER MOSFET DEVICES

In view of the fact that Schottky barrier MOSFETS fabricated under the DOE support are essentially two Schottky barrier Junction Rectifying Diodes, oppositely directed, in the surface region of a Silicon substrate, which Diode Junctions are separated by a Channel Region, the Effective Doping Level in which can be controlled by application of a Voltage to an associated Gate, it might be predicted that certain Device operating characteristics should be expected. As the Junctions formed are Rectifying on either N or P-Type Silicon, application of a Drain to Source Voltage of either Plus or Minus Polarity to devices fabricated on either N or P-Type Silicon should be expected to cause one of the Diode Junctions to be Forward Biased, and one Reverse Biased on either type Silicon, (whether Metalurgical or Field Induced). Some Reverse Biased Tunneling Current, limited by the Diode which is Reverse Biased, would be expected to flow through the seriesed connection of Diode Junctions, but sufficient applied voltage across said seriesed connection of Diode Junctions should provide essentially symetrical Reverse Breakdown increased current flow. We do see such in the Devices fabricated on both N and P-Type Silicon, with Tunneling current prior to Reverse breakdown on the order of tens to hundreds of nanoamps, and with Reverse Breakdown typically occurring at between 15 and 30 volts, leading to the flow of microamp and above currents. (Note that the Reverse Breakdown Voltage of a formed Junction seems to be a function of the Temperature at which the Diode Junctions are formed by annealing Chromium to Doped Silicon. The 15 to 30 volt figure corresponds to formation at approximately 450 to 550 Degrees Centigrade, while we have seen Reverse Breakdown occur at approximately 80 to 100 volts where the formation temperature was on the order of 600 to 650 Degrees Centigrade). One might also expect that application of either polarity voltage to the Gate should lead to a result of increased current flowing between the Drain and Source as a result of Field induced Channel Region Effective Silicon Doping Levels, and the effect such has on Reverse Bias Tunneling Currents. That is, the higher the Effective Doping Level of the Channel Region, the more Reverse Tunneling Current should be observed through the Reverse Biased Junction. This is because the Channel Region is simply the Semiconductor portion of a Schottky Barrier Junction, and it is well known that the more highly doped a Semiconductor in a Schottky Barrier Junction, the more Reverse Tunneling Current will flow therethrough at a certain applied Reverse Voltage. This would be expected whether the increased Doping is Metalurgical or Field induced. In fact, at a high enough Schottky barrier Semiconductor Doping Level, the Junction will become essentially "Ohmic". At the practical levels of Gate Voltage investigated, (eg. -15 to +30), we do in fact see a Gate Voltage effect on the current flow when the Gate

Voltage is of a polarity so as to Invert the Channel Region Doping Type and the applied Drain to Source Voltage is of a Polarity so as to effect a reverse Bias at the Drain Junction with respect to the Inverted Channel Region, and a Forward Biased Source Junction. However, we do not see such occur where the Gate Voltage is of a polarity which should accumulate the Channel Region, or where the Drain to Source Voltage is of a polarity so as to cause the Source Junction to Reverse Bias, even where the Channel Region is Inverted. This, to some extent, was not what I expected to find, but it is what we have found in all operational Devices fabricated. As well, we see a fairly large Drain Current flow, (far greater than Reverse Bias Tunneling Current), when zero Gate Voltage is applied and the Drain to Source Voltage Polarity is such as to Reverse Bias the Drain Junction with respect to an inverted Channel Region, but the current flow level is very much less, (on the order of Reverse Bias Tunneling Current), when the Drain to Source Voltage Polarity is reversed. The relatively large Drain Current flow which occurs at zero applied Gate Volts when the Drain to Source Voltage Polarity is such as to Reverse Bias the Drain Junction with respect to an Inverted Channel Region is Decreased by application of a Gate Voltage of a polarity opposite to that required to invert the Channel Region, and is Increased by application of a Gate Voltage of a polarity appropriate to Invert said Channel Region. As plotted against a sweeping Drain to Source Voltage said Decreased Drain Current Curves appear similar to those of a current flowing through a diode-resistor, (ie. the Drain Schottky barrier Junction and the Oxide Resistance), combination beginning where said sweeping Drain to Source Voltage just overcomes an applied Gate Voltage and effects a Forward Bias thereto, as would occur if the Channel Region were not yet Inverted and the Drain Junction were actually Forward Biased for instance; and said Increased Drain Current Curves present with typical MOSFET-like Saturation Drain Current Characteristics. (It is noted that what would be expected is only a relatively small Reverse Bias Tunneling Current flow in either direction with zero Gate volts applied). To understand the outlined empirically achieved results requires a step by step analysis, but reasonable explanations for the observed results are available if we assume operation as a MOSFET. Said explanations are entirely consistent with MOSFET operation, but vary considerably from explanations appropriate to explain Diffused Junction MOSFET operation. Assumption of other modes of operation, (eg. Bipolar Transistor), have not been found appropriate or able to account for what we find by investigation of fabricated devices.

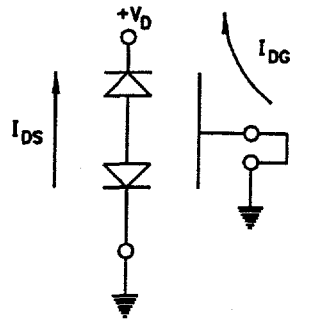
STEP BY STEP ANALYSIS OF FABRICATED SCHOTTKY BARRIER MOSFETS

Analysis of the fabricated Chromium-disilicide MOSFETS must be approached in stages depending upon what polarity voltages are

applied to the Drain and Gate with respect to the Source. Also, assumption of a Device Defect, namely the presence of Leaky Silicon Dioxide (Oxide), which is prone to "Breakdown" conduction, is necessary to make sense of the empirically obtained results.

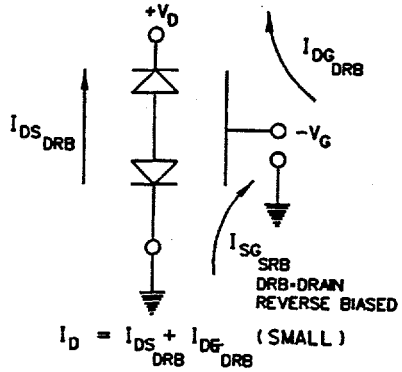
CONSIDER AN N-CHANNEL MOSFET FABRICATED ON P-TYPE SILICON. (AN ANALOGOUS ANALYSIS APPLIES TO A P-CHANNEL DEVICE WITH THE VOLTAGE POLARITIES APPLIED TO DRAIN AND GATE REVERSED).

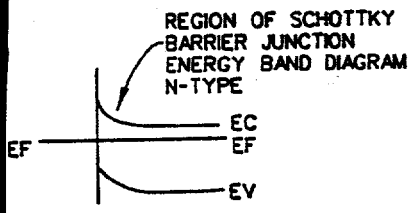
CASE 1. DRAIN TO SOURCE VOLTAGE POSITIVE (+) POLARITY

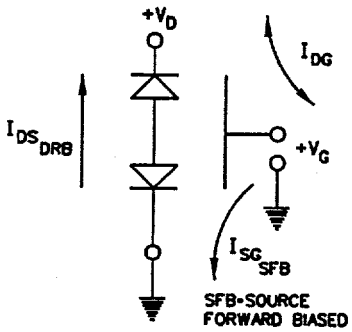


a. Application of Zero (0) Gate Volts, but gate circuit present. Current can flow through Reverse Biased Drain Junction and through parallel combination of two circuits, namely (1) a Channel Region in series with a Forward biased Source Junction, and (2) a Channel Region in series with a leaky Gate Oxide and Gate Circuit. However, note that the Gate Voltage is less Positive than the applied Drain Voltage and that the Gate sees a P-Type Silicon through a Leaky oxide, thereby effecting a Reverse Bias between the Drain and the Gate.

b. Application of Negative (-) Gate Volts. This will tend to accumulate the Channel Region and thereby effect a lower resistance Channel Region. Such can increase the tunneling current flow through the Reverse Biased Schottky barrier Drain Junction, (of which the Channel Region is the Semiconductor component), and in combination with the reduced Channel resistance increase current flow through the Forward Biased Source Junction. A negative Gate voltage will see a P-Type Silicon through a leaky Oxide, hence, a Reverse Bias situation with respect to the Drain, and Source Junctions, through leaky Oxide. This could serve to increase current flow through said Leaky Oxide and Gate Circuit, from the Drain Junction to a higher value that with Zero Gate Voltage present. The magnitudes of the currents are found to be on the order of relatively small Reverse Bias Tunneling Currents however. Said Currents are orders of magnitude less than those seen when the Drain has a Negative Polarity Voltage applied thereto and the Gate is provided a Positive, Channel Region inverting, Voltage,







BEFORE CHANNEL INVERSION

$V_D > V_G$

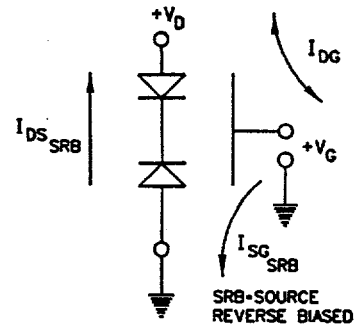
$I_D = I_{DS_{DRB}} + I_{DG_{DRB}}$ (SMALL)

$V_D < V_G$

$I_D = I_{DS_{DRB}} - I_{DG_{OFB}}$

I_{DG} COULD BE LARGE FORWARD BIAS CURRENT BUT WE DON'T SEE THIS OCCUR AS CHANNEL INVERTS AT LOW V_G

I_{SG} COULD BE LARGE FORWARD BIAS CURRENT IF CHANNEL DOESN'T INVERT



AFTER CHANNEL INVERSION

$V_D > V_G$

$I_D = I_{DS_{SRB}} + I_{DG_{DRB}}$ (SMALL)

$V_D < V_G$

$I_D = I_{DS_{SRB}} - I_{DG_{DRB}}$

PINCHOFF LIMITS GATE VOLTAGE MODULATION OF I_D AT REVERSE BIASED SOURCE

(see supra Case 2c). Apparently, Gate Voltage Modulation of Accumulation Effective Channel Doping has little effect on increasing Reverse Bias Drain Junction Tunneling Current by increasing effective non-Inverted Channel Region Doping Levels. Perhaps Conduction and Valance Energy Band Pinning, (as is known to occur in Schottky barrier Junctions), can not be significantly affected at the actual Schottky barrier Metal-Semiconductor Interface by an applied Gate Voltage in a Metalurigical Junction, whereas it can have a significant effect in Field Induced Schottky barrier Junctions. This interpretation is consistant with the Results we have obtained and I have found it a convenient thought aid to date. It might also be expected that at high Negative Gate Volts and High Positive Drain Volts the Reverse Biased Drain Junction might break down and allow Drain Current to flow. We do see a trend theretoward at times.

c. Application of Positive (+) Gate Volts. Positive Gate Voltage serves to immediately reduce the Reverse Bias present between the Gate and Drain which results from Applied Positive Drain Voltage, and if the Gate Voltage is increased enough to exceed the Applied Drain Voltage one might think that a Forward bias situation would develop at the Drain Junction, from the Gate through Leaky oxide. This, however, does not occur, as another effect apperantly dominates, that being MOSFET action Channel Region Inversion. This causes the Channel Region to become N-Type. Now, an N-type Channel with a Positive Drain Voltage applied means the Drain Junction will go Forward Biased and the Source Junction will become Reverse Biased as seen from the Drain. The Gate Circuit will see N-type Silicon through a leaky Oxide and could be part of a Forward Biased Drain to Gate Circuit where the Positive Applied Gate Voltage is less Positive than the Applied Positive Drain Voltage. This would be expected to cause a relatively high Forward Bias current flow through the Gate Circuit from the Drain. We do not see this occur however. Likewise one might expect to see a relatively high current flow through a Gate Voltage Modulated Silicon Doping Effect at the then Reverse Biased Source Junction. We do not see this occur either. (Note as will be

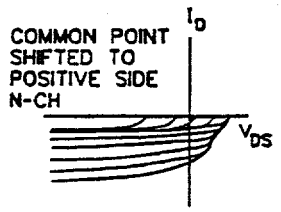
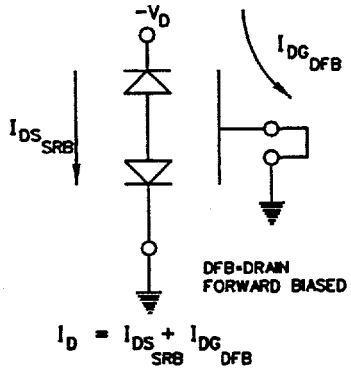


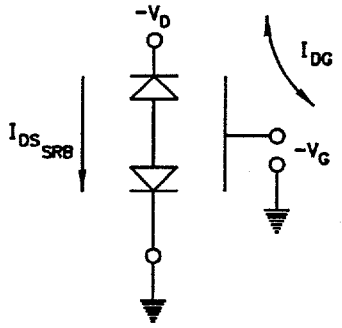
FIG. 20

described supra, in Case 2c, when an Inverted Channel Region exists and the Drain Junction is Reverse Biased, that is when applied Gate Voltage is Positive and applied Drain Voltage is Negative, we do see relatively high, applied Gate Voltage Modulated Drain Current flow, which Drain Current vs. Drain to Source Voltage Curves demonstrate "Saturation" Characteristics). What seems to occur when the Applied Drain and Gate Voltages are both Positve is that the Gate and Drain Voltages effect a Channel Region "Pinch-Off" such as that which causes Current Flow Saturation in Diffused Junction MOSFETS, and said "Pinch-Off" Region drops, (ie. "absorbs"), the Applied Drain Voltage. Said "Pinched-Off" Channel Region serves to shelter the Reverse Biased Source Junction so no Tunneling Current Flow Driving Force appears thereacross. This, at least, is a plausible explanation which seems to account for the results we achieved by empirical test of fabricated devices. (Note also that in some devices we see Drain Current Flow starting from a "Common Point" along the Drain to Source abscissa, on the Positive Drain Voltage side of Zero (0) Drain Volts, (eg. at approximately +2 Volts or less). Said Drain Current Flow merges into Saturation Drain Current Flow Characteristics as the applied Drain Voltage sweeps Negative, (see Case 2c supra). I think this occurs where a loss of Channel "Pinch Off" occurs, (as is expected to occur as the Positive Drain Voltage decreases, but which normally occurs at Zero (0) applied Drain to Source Volts), thereby presenting the difference in Voltage Applied to the Gate and that Applied to the Drain across the Oxide, which Oxide then apparently breaks down and allows Current to flow through a Forward biased Drain Junction, atop a Source Junction which remains Reverse Biased prior to Channel Region inversion.

CASE 2. DRAIN TO SOURCE VOLTAGE NEGATIVE (-) POLARITY



a. Application of Zero (0) Gate Volts, but Gate Circuit present. Current can flow through a Forward Biased Drain Junction and into a P-Type Channel Region, then through a parallel combination of 1. a Gate Circuit through Leaky Oxide, and 2. a Reverse Biased Source Junction. What we see is a relatively high Drain current flow which originates near the Drain to Source Zero (0) Voltage point and increase as the Drain Voltages is swept more negative. The shape of the Drain Current Curve is like that of a current flowing through a diode and a resistor in series.



$V_D > V_G$

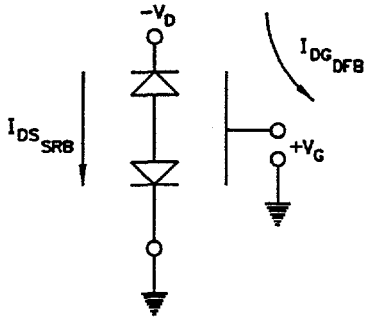
$I_D = I_{DS_{SRB}} + I_{DG_{DFB}}$

$V_D < V_G$

$I_D = I_{DS_{SRB}} - I_{DG_{DFB}}$

b. Application of Negative (-) Gate Volts causes the relatively high Drain Current which flows at Zero (0) applied Gate Volts to decrease, with each applied Negative Gate Voltage being associated with a different origin point at which Drain Current begins to flow. That is, if a Negative 2 Volts is applied to the Gate, the Drain Current flow is relatively low until the Drain to Source Voltage sweeps more negative 2 volts, and then said Drain Current flow increases, with the Curve thereof as the Drain Voltage sweeps being again like that of a diode in series with a resistor. To understand this one must recognize that said Gate Voltage will be applied to a P-Type Silicon through Leaky Oxide. Until the Drain Voltage sweeps more negative than the applied Negative Gate Voltage, the Gate to Drain Circuit will be a Reverse Biased Junction, with only Reverse Bias Tunneling Current flowing therethrough. When the Drain Voltage sweeps more Negative than the Applied Negative Gate Voltage, the Gate to Drain circuit becomes a Forward Biased Drain Junction with Oxide and P-Type Channel Region Silicon providing a seriesed Resistance. In view of this, it is felt that the reduction in Drain Current flowing at Zero (0) Applied Gate Voltage by the application of Negative Gate Voltage is proof that we do have Leaky Oxide, and said Leaky Oxide fully accounts for the Drain Current flow at Zero (0) Applied Gate Volts.

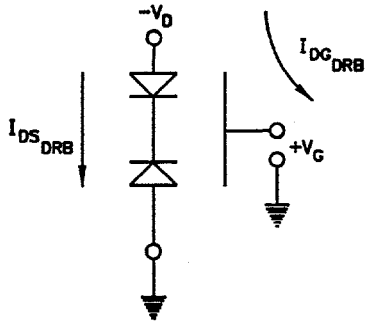
SEE OPERATIONAL SATURATION CHARACTERISTIC DRAIN CURRENT CURVES



BEFORE CHANNEL INVERSION

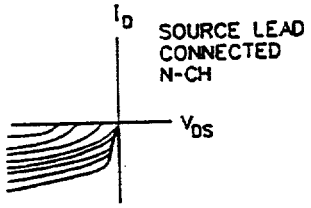
$I_D = I_{DS_{SRB}} + I_{DG_{DFB}}$

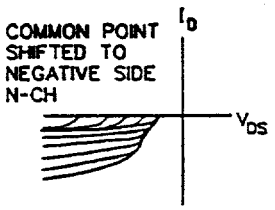
c. Application of Positive (+) Gate Volts provides the Operational Drain Current vs. Drain to Source Voltage Saturation Curves we find empirically. Said Saturation Characteristic Drain Current Curves develop from a Base Current Level corresponding to the Drain Current vs. Drain to Source Voltage Curve achieved at Zero (0) Applied Gate Voltage, and provide increased Drain Current Levels for increased Applied Positive Gate Volts. At low Applied Positive Gate Volts, before Channel Inversion, we see Forward Biased Drain Junction Current Flow through Leaky Oxide. Application of increased Positive Gate Volts, however, causes Inversion of the Channel Region to N-Type Silicon. The Applied Negative Drain Voltage then effects a Reverse Biased Drain Junction and a Forward Biased Source Junction with respect to said Inverted N-Type Channel Region. (Note, As the Polarities of the applied Drain and Gate Voltages are opposite, no "Pinch-Off" effect can develop and Deplete the Channel Region,



AFTER CHANNEL INVERSION

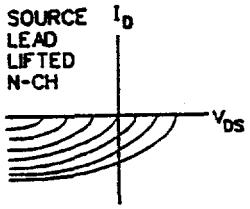
$I_D = I_{DS_{DRB}} + I_{DG_{DRB}}$





thereby lowering Channel Region conductivity). Essentially the full Applied Drain to Source Voltage drops across the Reverse Biased Drain Junction through the Forward Biased Source Junction, thereby providing a driving force for the production of a Reverse Bias Tunneling Current through said Reverse Biased Drain Junction. Said Drain Current will flow into said Inverted N-Type Channel Region and through said Forward Biased Source Junction to, in our test situation, ground. (Note the Source Lead could be connected to a Positive Voltage but it was not in our test situation). As the Positive Gate Voltage will see N-Type Silicon in the Channel Region, it sees a Reverse Biased Junction situation with respect to both the Drain Junction and the Source Junction. (Note, Gate Current Flowing has been observed to drop when Channel Inversion occurs). The Drain Junction has a Negative Voltage Applied thereto, and the Source, being at Ground is at a relatively more Positive Voltage. Hence, it is reasonable to assume that the majority of the Drain Current does flow from the Drain through the Inverted N-type Channel and then through the Forward Biased Source Junction. It is noted that the Drain Current Saturation Curves all start essentially at a "Common Point" on the Drain to Source Voltage abscissa, as the Drain Voltage is swept from Positive to negative through Zero (0) Volts. Now, normally we find that the "Common Point" is at Zero (0) Volts Applied to the Drain. However, now and then we find Devices in which the "Common Point" is shifted either Positive, (discussed infra), or Negative along the Drain to Source abscissa. I think this is the result of relatively high Source Contact Resistance, and the effect of forward biased current flowing through the Gate to Source pathway prior to the Inversion of the Channel Region. High Source Contact Resistance shifts the Drain Current Curves to the negative, (by dropping voltage), and Gate leakage Current flow to the positive, (by imposing a positive voltage in the Noninverted Channel, atop a then Forward Biased Source), prior to application of a Drain Current flow forcing Drain to Source Voltage.

It is also of interest to describe the sort of Curves which appear if we apply Positive Gate Voltages, and sweep the Drain to Source Voltage from Positive to Negative with the Source lead lifted from the Schottky barrier MOSFET Device Source Contact. In this case



the Drain Junction can become Forward Biased, with respect to the Gate, through leaky Oxide. That is the Drain and Gate Voltage Sources will be in a series circuit with the Drain Junction through leaky Oxide. What we see develop are a series of Curves, each similar to those which appear when Voltage is applied across a seriesed Diode and Resistor, (eg. the Leaky Oxide). Curves, one for each applied Gate Voltage, should start at locations along the Drain to Source abcsissa, where a swept Drain Voltage just decreases below the then applied Gate Voltage, effecting a Forward Bias on the Drain Junction. If the difference between applied Drain and Gate Voltages becomes large enough, however, Silicon Inversion can occur and the Drain Current Curves become Reverse Bias Tunneling in nature with Current flow through the Oxide.

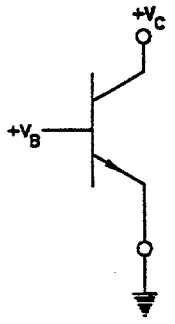
It is again note that a similar analysis to that presented infra for the N-Channel Schottky barrier MOSFET Devices can be performed for the P-Channel Schottky barier MOSFET Devices by simply reversing the recited Polarities of applied Gate and Drain Voltages.

Also, in the above analysis Bulk Effects were assumed negligible, which seems to be justified.

Generally, I feel that we must make but a few assumptions, in view of the above, to explain the results we have achieved. First, the Devices do operate in an Inverted Channel MOSFET Mode, but that Drain Current is the result of Tunneling Current through a Reverse Baised Schottky barrier Junction into the Inverted Channel. Second, we have a Leaky Oxide problem which causes Drain Current to flow when Drain Voltage is applied but no Gate Voltage is applied, and which causes Drain current to flow when Gate Voltage is applied and no Drain Voltage is applied. Third, in some devices we have seen evidence of relatively high Contact Resistance and Oxide Breakdown, in that the "Common Point" from which Saturation Drain Current Curves begin, shifts along the Drain to Source abscissa. Forth, the Devices only provide MOSFET Saturation Curves when an Inverted Type Channel Region is effected, and then only when the Drain Junction is Reverse Biased. This is felt to be because Metalurgical Junctions have different characteristics than do Field Induced Junctions, (with the later known to often demonstrate lower Reverse Breakdown Voltages and larger Tunneling Current flows at certain Voltages as compared to Metalurgically effected junctions). Fifth, we must assume that "Pinch-Off" Regions prevent Tunneling current driving force from dropping across a Reverse Biased Source Junction in an Inverted Channel Region Scenario, but have no effect on Voltage Dropped across a Reverse Biased Drain Junction to which the Drain Voltage is Applied directly, rather than through a length of "Pinched-Off" Channel Region.

ATTEMPT TO EXPLAIN DEVICE OPERATION AS A BIPOLAR TRANSISTOR

As we have seen, the present devices operate with the Drain Junction Reverse Biased and with the Source Junction Forward Biased. With that in mind, one can not help but think of Bipolar Transistors which operate with a Reverse Biased Collector and a Forward Biased Emitter Junction in analogically similar circuit positions to the present Device's Drain and Source. It must, however, be appreciated that the Bias arrangement alluded to is as seen from the Drain or, analogically, the Collector of respective MOSFET or Bipolar devices respectively, with respect to the Source, or analogically the Emitter of the respective devices. When one views from the Gate, or analogically the Base of the respective devices, with respect to the Source, or analogically the Emitter, the analogy to Bipolar devices breaks down. The present Schottky barrier MOSFET devices provide Saturation Drain Current vs. Drain Voltage Curves with the Applied Gate Voltage effecting a Reverse Bias with respect to both Drain and Source Junctions (assuming an Inverted Channel Region is present). If we do not assume an Inverted Channel Region is present the Gate Applied Voltage would effect a Forward Bias with respect to both the Drain and Source Junctions. This is because the Applied Gate Voltage, in the operational region of he present Schottky barrier MOSFET Devices, is of the opposite polarity to that applied to the Drain. (Note that in our test system the Source is held a ground, hence an applied Positive Gate Voltage is more positive with respect thereto, just as it is more positive with respect to an Applied Negative Drain Voltage. A Bipolar Transistor requires that the Voltage applied to the base be of the same polarity as that applied to the Collector, only of a lesser magnitude with respect to the Emitter thereof, emphasis added. As a result, I conclude that the Operation of the present Devices can not be explained by Bipolar Transistor Theory in view of the Test Set arrangement in which we obtained empirical results, (eg. the presence of a well defined Common Source, (Emitter), Terminal with respect to which the applied Gate and Drain Voltages were applied).

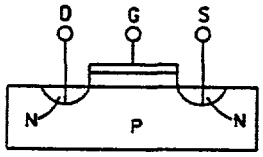


BOTH COLLECTOR AND BASE SAME POLARITY WHEN HAVE SATURATION CURVES

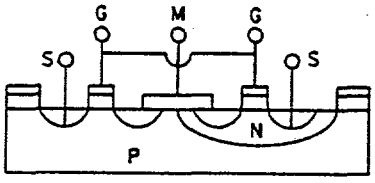
APPLICATION OF PRESENT DEVICES TO CMOS SYSTEMS

The reader might by now have noted that the present Schottky barrier MOSFETS operate with Drain Current flowing in a direction opposite to that which one finds in Diffused Junction MOSFETS. This is indeed the case. That is, in Conventional Diffused Junction MOSFES the Gate and Drain both have the same Polarity Voltage applied thereto and provide Saturation Drain Current vs. swept Drain to Source Voltage Curves via an Inverted Channel

"Pinch-Off" mechanism, whereas the present Schottky Barrier MOSFETS require Opposite Polaritiy Voltages be applied to the Gate and Drain to effect Saturation MOSFET Drain Current vs. swept Drain to Source Voltage Curves and effect said Curves via the limit of Reverse Bias Leakage Current which can flow through a Reverse Biased Drain Junction as a function of Field Induced Inverted Channel Doping Level. (It will be recalled that the Channel Region constitutes the Semiconductor component of a Schottky Barrier Junction, and that it is well known that a higher Doping Level of the Semiconductor component of a Schottky Barrier Junction is associated with a higher Reverse Bias Tunneling Currents at certian Applied Reverse Bias Voltages thereacross). In view of the above, it becomes a bit difficult to understand how Complimentary Metal Oxide Semiconductor (CMOS) Device Systems can be configured from the present Devices.



First, a conventional Diffused Junction MOSFET comprises Source and Drain Regions of one type of Semiconductor, (ie. N or P-Type), separated by a Channel Region of an opposite Type of Semiconductor. The Channel Regions have associated therewith a Gate, application of a Voltage of a proper polarity to which, can serve to Invert the Type of Semiconductor in the Channel Region, thereby providing an ohmic path between the Drain and Source. That is, no rectifying junction remains between the Drain and Source Contacts.



CONVENTIONAL DIFFUSED JUNCTION CIRCUIT

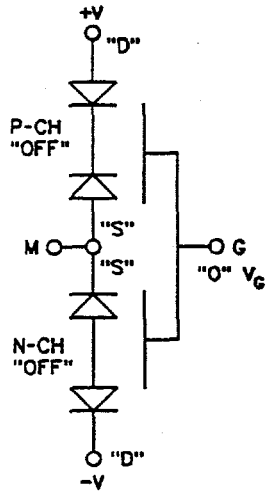
Conventional Diffused Junction CMOS systems comprise a seriesed combination of P and N-Channel Devices, in which the Drains of the respective devices are interconnected to form a Common Midpoint. If a Voltage is applied between the remaining noninterconnected Sources, and a voltage is applied to interconnected Gates of the P and N-Channel Devices with respect to one of said Sources, the end result is that one device is "On", (eg. conducting), when the other is "Off", (eg. nonconducting), and vice versa. The voltage at the interconnected Drains Midpoint will be an inverted version of the applied Gate voltage. For instance, assume the Source of a P-Channel Diffused Junction MOSFET is provided a Positive Polarity Voltage with respect to the Source of an N-Channel Diffused Junction MOSFET, which P and N-Channel Diffused Junction MOSFETS are configured in a CMOS configuration by interconnection of the Drains thereof, and by interconnection of the Gates thereof. If a Positive

Voltage, again with respect to the Source, of the N-Channel Diffused Junction MOSFET is applied to the interconnected Gates, the N-Channel Device will form an Inverted conducting Channel Region and be "On". the voltage at the Midpoint interconnection of the Drains will then be at Zero (0) volts. If the Gates are provided a Negative Voltage the P-Channel Device will form an Inverted conducting Channel and will be "On". The voltage at the Midpoint interconnection of the Drains will be at that applied to the Source of the P-Channel Device. In each case, the device not "on" will be "off" as there will not be an Inverted Channel region to ohmically connect the Drain and Source therein. These Inverter Circuit Systems are very energy efficient in use as the only time current flows is at the exact switch point. However, High and Low Voltages can be effected at the interconnected Drains, and remain until applied Gate voltage change effects the switch.

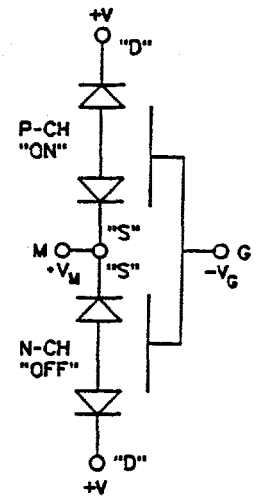
As one might expect the present N and P-Channel Schottky barrier MOSFETS can not simply be substituted for Conventional Diffused Junction N and P-Channel Devices in a CMOS system and the operation thereof in a CMOS configuration thereby understood. This is because the Applied Gate and Drain Voltages are of necessarily of opposite Polarity, as described infra. Also, a true Ohmic connection is not effected between a Drain and Source in the present Devices when they are "On". There are still Rectifying Junctions present with respect to the Channel Region, one of which is Reverse Biased. However, looking into the Drain of a present Device, one will see an effective lower resistance when it is "On" than when it is "Off". This seen to be the case as more current flows through an Applied Gate Voltage effected "On" device than through an "Off" Device at the same Drain to Source Voltage, (ie. Applied Drain Voltage divided by Current Flowing in said Drain provides an effective resistance between Drain and Source Contacts). Now, the Effective Resistance of the Reverse Biased Junction is a function of the Effective Doping of the Semiconductor component of the Schottky barrier Junction, not the amount of Current being force through it by Applied Voltage thereacross.

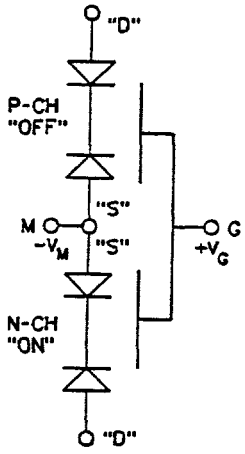
To understand how the present Schottky barrier MOSFETS can operate in a CMOS configuration it is necessary to understand that physically, the present Devices are symetrical. That is, the Rectifying Junctions which constitute the Drain and the Source thereof are identical. It is location in a circuit that defines them as Drain or Source, by the function performed thereby. One of the Junctions will be found to be a "Common" terminal to which Applied Drain and the Gate Voltages will refer. It will also be recalled that the present N-Channel Device, (which is fabricated in P-Type Semiconductor) operates, (ie. provides conduction as evidenced by Saturation Characteristic Drain Current vs. Drain to Source Voltage Curves), when the Drain

has a Negative Voltage applied thereto and the Gate has Positive Voltage applied thereto, again, both with respect to the Source thereof. A P-Channel, (which is formed in N-Type Semiconductor), operates (ie. provides conduction as evidenced by Saturation Characteristic Drain Current vs. Drain to Source Voltage Curves), when the Drain has a Positive Voltage applied thereto and the Gate has Negative Voltage applied thereto, both with respect to the Source thereof. In a circuit one must look for Voltage Polarities to define a Drain or Source.



Now, if we configure a present Schottky barrier P-Channel MOSFET and a present Schottky barrier N-Channel MOSFET so that one non-Gate terminal of each are interconnected, and such that the noninterconnected non-Gate Terminal of the P-Channel Device has a Positive Polarity Voltage Applied thereto, and such that the noninterconnected non-Gate Terminal of the N-Channel Device has a Negative Voltage applied thereto, and we interconnect the Gate Terminals, then we have an operable CMOS System wherein the Inverting Midpoint Voltage appears at the interconnected Terminals of the two Devices during use. To understand the operation, assume a Positive Voltage is Applied to the interconnected Gates, (eg. that Positive Voltage applied to the noninterconnected non-Gate Terminal of the P-Channel device). Also understand that the interconnected non-Gate Terminals Midpoint Voltage will be established between the Voltages Applied to the noninterconnected non-Gate Terminals by simple voltage division. Now a Positive Applied Gate Voltage, with respect to a "Source" Terminal is associated with turning "On" an N-Channel Device, the Drain of which is at a Negative Voltage with respect to a "Source" Terminal. If we think of the interconnected non-Gate Midpoint Terminals of the P and N-Channel Devices as the effective "Sources" of the Devices in the present CMOS System, then we see that the N-Channel device will have a Positive Gate Voltage with respect thereto, (eg. this is the result of a voltage drop across the effectively high Reverse Biased Schottky barrier Junction Resistance of the "Off" P-Channel Device), while the Effective "Drain", (ie. the noninterconnected non-Gate Terminal), of the N-Channel Deice has a Negative Voltage Applied thereto, again with





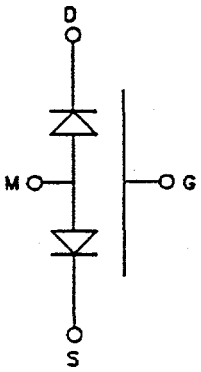
respect to the Effective "Source" thereof. In this circuit, the Effective "Sources" must be considered to be at the Midpoint interconnected non-Gate Terminals of the N and P-Channel Devices to understand how the required Voltage Polarities are present to make the circuit work. It will be recalled that when an N-Channel Drain has a Negative Voltage applied thereto, and a Positive Gate Voltage applied thereto, Saturation Drain Current vs. Drain to Source Voltage Curves appear. The appearance of such Curves is associated with an effectively lower Drain to Source Resistance therein. Now, again, it is to be understood that the P-Channel and N-Channel Devices form, in effect, a Voltage Divider Circuit. The Resistance of the P-Channel Device will remain relatively high when the Gate Voltage applied thereto is Positive with respect to the Effective Source thereof. Hence we expect to see a Low Midpoint interconnected non-Gate Terminal voltage. Now the lower the effective Resistance of the N-Channel Device becomes, the lower will be the Midpoint interconnected non-Gate Terminal Voltage by the voltage divider mechanism, hence the more Inverted the N-Channel Channel Region will become if the Gate Voltage is held constant, (which it typical is at that applied to the Effective "Drain" of the P-Channel Device), and the more Inverted the N-Channel Region, the lower will its Resistance become. A regenerative effect occur which serves to progressively turn the N-Channel Device more and more "On"! However, there will come a point where the Tunneling Current Flow Driving Voltage Dropped across the Reverse Biased Effective "Drain" in the N-Channel Device will not be sufficient to sustain Current Flow thereacross, even though the Reverse Biased Junction Resistance thereof will be low. At that point, both the N and P-Channel Devices will serve to limit Current Flow through the Series Chain in the Schottky barrier CMOS System described. As mentioned infra, however, the fact that little current is flowing through the Reverse Biased Effective "Drain" Junction in said N-Channel Schottky barrier MOSFET does not determine the Effective Resistance thereof, and the effect thereof in a Voltage Divider Circuit with the P-Channel Schottky barrier MOSFET Device.

That is, it is the effective Doping of the Inverted Channel Region Semiconductor component of the Schottky barrier Junction which determines the Effective Resistance thereof, and not the current forced therethrough at any point, as is the case with any resistor. (Also note that a "Pinch-Off" Region will add to the "Off" device resistance, thereby enhancing the effect).

A similar analysis applies to the case wherein a Negative Voltage is applied to the Gates of the present Schottky barrier MOSFET System, but the Midpoint Voltage, of course, will be "High" when said Negative Gate Voltage is Applied.

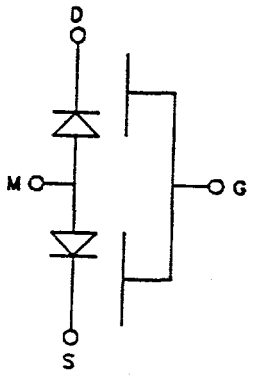
SINGLE DEVICE INVERTING AND NONINVERTING EQUIVALENTS TO CMOS

The work under the present support was expanded beyond that originally proposed to show feasibility of producing Schottky barrier Junction based Single Devices which provide Operating Characteristics similar to CMOS Systems, which as demonstrated above, comprise two devices. If successfully developed, such Single Device CMOS Equivalents will allow greatly increased Device Substrate Packing Density, (eg. more devices per area of Semiconductor).



NON-INVERTING
SINGLE DEVICE CMOS

The basic theory behind these Devices is relatively easily grasped. In the case of the Noninverting Single Device CMOS Equivalent, the physical structure is that of a Schottky barrier MOSFET with a Drain and Source separated by a Channel Region. Also present, however, is a Channel Region Contact which can sense Voltage present in the Channel Region under the Gate. Now, if a Voltage is applied across the Drain to Source, then one of the Schottky barrier Junctions, (ie. Drain or Source) is Forward Biased, and the other is Reverse Biased. The Voltage monitored by the Channel Region Contact should be essentially that applied to the Forward Biased Junction, and supported by the Reverse Biased Junction. Application of a Gate Voltage of a proper polarity will Invert the Semiconductor, and that will cause the location of the Forward and Reverse Biased Junctions to reverse. This will cause the Channel Region Contact Voltage to change to that applied to the then Forward Biased Junction. In this Device the direction of change of the Applied Gate Voltage and the direction of change of the Channel Region



INVERTING
SINGLE DEVICE CMOS

Contact Voltage are of the same, thus the Device is "Noninverting". (Note Conventional Diffused Junction CMOS requires four devices to fashion a Noninverting configuration.

Now, if the geometry of the Device is such that the Schottky barrier Junctions are Centrally located, with Semiconductor leading to an ohmic Source on one side thereof and Semiconductor leading to an ohmic Drain on the other side thereof, then we can achieve an Inverting Single Device Equivalent to CMOS. That is if a Voltage is applied across the Drain to Source, a Midpoint voltage will appear at the Schottky barriers. Now if interconnected Gates are associated with each lenght of Semiconductor, and a Gate Voltage of a Polarity proper to Invert said lengths of Semiconductor is applied, then we will see the Voltage at the Midpoint Schottky barriers change in a direction opposite to the direction of change of the Applied Gate Voltage.

(Note, these Single Device CMOS Equivalent Devices will probably have to be low Applied Gate Voltage Devices to prevent significant MOSFET Drain Current Flow, where an Inverted Channel Region is formed in use. We will want to achieve just sufficient Channel Region Inversion to shift the location of the Forward and Reverse Biased Junctions, but no more.)

The copy of the Pending Grant Application submitted to the Air Force included herewith, in Attachment "B", and the Patent Application in Attachment "C", better describes the geometry of these devices.

CONTINUED WORK

Continued Research is needed to provide better quality Schottky barrier Junction formation, (sputter clean silicon prior to depositing and annealing chromium), and upon obtaining better quality Oxide through which current can not flow. As well, Aluminum pads for mediate contact between Source and Drain Junctions and external testing equipment should be effected. This requires new photolithographic mask sets. Additional work should also investigate the use of other Schottky barrier forming metals, such as Molybdnium and Platinum.

There remains to be developed a Mathematical Model for the present Schottky barrier MOSFET Devices. However it is known that said Model will rely on the use of Reverse Bias Schottky barrier Junction Tunneling Current Equations, the Calculation of

Channel conductivity in both Non-Inverted and Inverted Modes and the effect that Applied Gate Voltage has thereon, as well as the effect that Effective Channel Region Doping Level has on Drain Current Flow via change in the Semiconductor Component of said Schottky barrier Junctions, and how such relates to Conduction, Valence and Fermi Levels in Energy Band Diagrams. Integration of the MOSFET Channel "Pinchoff" effect will be a necessary part of model, and Channel Region Geometry at the lateral edges of the Source and Drain Junctions, and how it affects current flow into and through the Channel should also be investigated.

ACTUAL EMPIRICALLY OBTAINED RESULTS

The following Series of Graphs show actual Empirically obtained Data achieved by investigation of Actual Fabricated Devices. Above discussed phenomona are demonstrated thereby.

The first Figures show Schottky barrier Junction Current vs. Applied Voltage. Fig. 1 shows said Curves for a P-Type Silicon Substrate and Fig. 2 for an N-Type Silicon Substrate upon which was deposited Chromium. Both Plots are for Schottky barrier Junctions formed by a fifteen minute 350 Degree Centigrade Vacuum Anneal. (Note, the polarities are not opposite on the Fig. 1 and 2 Plots as the monitoring probes were switched around when measuring the Device Curves. I changed this practice after initial efforts. Figs. 3 and 4 show Reverse Breakdown for N-Type and P-Type Silicon Schottky barrier Junctions formed by a 30 minute 450 Degree Centigrade Anneal. Figs. 5 and 6 show Reverse Breakdown for P-Type and n-Type Silicon Schottky Barrier Junctions formed by a 30 minute 650 Degree Centigrade Anneal. Note the Reverse Breakdown Voltage is greatly increased over that shown in Figs. 3 and 4. Fig. 8 shows an Optical Microscope Photograph of a Schottky Barrier MOSFET formed by the present invention procedure. The two Light Square Regions are the Source and Drain, with the thin Dark Region inbetween being the Gate. Fig. 7 shows typical back to back Schottky Barrier Reverse Breakdown Characteristics for Junctions formed by a 400 Degree Centigrade Anneal. Note the Reverse Breakdown is between approximately 15 and 30 Volts. This was a commonly achieved result. Figs. 9 and 10 show the Original N-Channel and P-Channel Curves I achieved on April 27 and 28th, 1994 as described in the Historical Accounting Section of this Report, infra. Note that the N-Channel Curves show Forward biased Junction Currents starting at 0, 2 4 Volts Drain to Source, when the Applied Gate Voltage was approximately 0, 2 and 4 Volts respectively. This is as thought to be explained by Cases 2a and 2b in the Analysis of Schottky Barrier MOSFETS Section of this Report, infra. Figs. 11 and 12 are interesting Plots which were rarely achieved. Obviously they are for P-Channel Devices, formed on N-Type

Silicon as the Curves are in the First Quadrant. These Figures seem to show definite transition from the Forward Bias Current Flow through the Drain Junction at Zero and Negative Applied Gate Voltages, to Saturation Current Characteristics at Positive Applied Gate Voltages. The Forward Bias Drain Junction Curves seem to begin at a bit low Drain to Source Voltage in Fig 12, but the general nature of the Curves in both Figs 11 and 12 is thought to be explained by Cases 2a and 2b in the Analysis of Schottky Barrier MOSFETS Section of this Report, infra, (Note said Sections 2a and 2b were written with respect to an N-Channel Device, so the Polarities in Figs. 11 and 12 are opposite to those discussed in said Sections 2a and 2b). Figs. 13 through 17 show Drain Current vs. Drain to Source Voltage for an N-Channel Device formed on P-Type Silicon. The Drain Voltge was swept from -5 to +5 Volts, and the Gate Voltage stepped from -10 Volts to + 18 Volts. Progressively lower Current Scales are applied to the same set of Curves. Again, note that for Gate Voltages of, in this case, Below 0 Volts, we see Drain Current flow as it would through a Forward Biased Drain Junction from the Gate, (eg. at Negative 2 Volts Applied to the Gate we see Drain Current begin at approximately Negative 2 Volts Applied to the Drain). At Positive Applied Gate Volts we see Saturation Drain Current Curves. Note in particular that at a Positive 4 Gate Volts the Current flow when a Positive 5 Volts is applied to the Drain, is approximately 8 x Ten-To-The-Minus-Ninth Amps, but that when a Positive 4 Gate Volts is applied with a Positive 5 Drain Volts present the Drain Current flow is approximately 4 x Ten-To-The-Minus-Seventh Amps, which is two orders of magnitude higher. This shows that the Inversion Channel is much more effected by Gate Voltage than is an Accumulated Channel. It is thought this is the result of a basic difference between Metalurgical and Field Induced Junctions as discussed in the Analysis of Schottky Barrier MOSFETS Section of this Report, infra. Figs. 18 through 20 show a similar sequence of Plots, for a P-Channel Device formed on N-Type Silicon. Figs. 21 through 24 show a sequence with the same set of Drain Current Curves obtained from another N-Channel Device, plotted with progressively lower Current Scales. Figs. 22, (and 27), show the Case 1b, (in the Analysis of Schottky Barrier MOSFETS Section of this Report, infra), effect of a trend toward a Reverse Drain Junction Breakdown as the difference between applied Drain Volts and Gate Volts increases. Figs. 25 and 26 show Curves for yet another P-Channel Device. Fig. 26 is plotted on a lower Current Scale, but the Curves are the same as in Fig. 25. Figs. 27 through 32 show additional Drain Current Curves obtained from yet other Fabricated Devices. Note that the P and N-Channel Devices represented by Figs. 29 and 30 respectively are fairly balanced and would probably make a good CMOS pair, were it possible to simultaneously identify, probe and interconnect them. Figs. 33 and 34 show Drain Current Curves obtained from P-Channel and N-Channel Devices which had no Gate Metal present. The Gate Probe was set atop the Oxide and acted as a Gate Metal. The Device which provided the Curves in Fig. 30 had the Silicon

etched approximately 2 microns. Both Figs. 33 and 34 show Drain Current Curves starting from a "Common Point" along the Drain to Source abscissa, but that "Common Point is offset from the Zero Drain to Source Voltage Point. This is thought to be explained by Case 2c in the Analysis of Schottky Barrier MOSFETS Section of this Report, infra, which discusses loss of "Pinch-Off" in an Inverted Channel Region, combined with Oxide Breakdown and accompanying Current flow therethrough. Figs. 35 and 36 show P-Channel device Curves obtained with and without the Source Lead in place, respectively. Note that with the Source lead in place, (Fig. 35 Curves), we find Saturation MOSFET-like Drain Current Curves starting from a "Common Point". Again, Case 2c in the Analysis of Schottky Barrier MOSFETS Section of this Report, infra, discusses why Drain Current Curves are thought to occur. With the Source lead lifted, Fig. 36 shows that a family of Drain Current Curves form, each of which initially appears as a Forward Bias Current flow through a Diode and the Silicon Dioxide. Note that each "Source lifted" Drain Current Curve starts at a point on the Drain Voltage Sweep where the Drain Junction would become Forward Biased, just overcomming a Reverse Bias set by the Applied Gate Voltage. As the difference between Gate and Drain Voltages increases, however, it can occur that the Silicon will invert and the Drain Current Curves will become Reverse Bias Tunneling in nature. Finally, Figs. 37 through 39 show MOS Capacitor Curves. These are included to show that we indeed do Invert silicon by applying Gate Voltage across leaky Oxide.

Another observation is that many of the Saturation Drain Current Curves seem to begin with an almost Forward Biased Diode Form, which then merges into a Saturation Current. It is felt, in view of the Case 2c explanation in the Analysis of Schottky Barrier MOSFETS Section of this Report, infra, that this should be expected where Positive Gate and Negative Drain Voltages are applied, and Drain Current initially flows through the Gate Oxide and a Forward Biased Drain Junction via a Non-Inverted Channel Region, (Figs. 28 & 31 are an exception to this as said Curves appear very MOSFET-like). When the Channel Inverts, the Drain Current Curves change to demonstrate Saturation Characteristics.

Let me add that I think the Gate Voltage supply continuously causes Minority Carrier production through "Avalanche" at the Source Junction, which Minority Carriers form an Inversion Channel Region, which Inversion Channel Region Minority Carriers then serve as the Carriers in Drain to Source Current Flow, under the driving influence of applied Drain to Source voltage. If that is the case one would then expect that limiting the Gate Current Flow to zero (0.0) Amps, would prevent formation of an Inverted Channel Region, and that no MOSFET Drain Current Curves would be effected. Indeed, it was observed that when the Gate Current Flow was limited to zero (0.0) Amps by a "Test Set Compliance" Setting, sweeping the Drain to Source Voltage from Negative to Positive caused no Drain Current to flow, regardless of applied Gate Voltage level. If, however, as little as one-hundred-nano-amps was allowed to flow in the Gate Circuit, in some cases some Drain Current Flow was effected by application of Gate Volts. I think what is occuring is that the Gate Circuit

feeds Source Junction located Gate Voltage controlled Avalanche Minority Carrier production, and the Gate Voltage Supply must be capable of supplying Minority Carriers thereto, for the devices to work. At the outset of the application of Channel Inverting Polarity Voltage to a Device Gate, I think current can flow from the Gate Voltage Supply through the leaky Silicon Dioxide through a Forward Biased Drain Junction and Drain Current can also flow at zero (0.0) applied Gate Volts when Drain Volts are applied. Once Channel Inversion occures, however, major Gate Voltage Supply-Silicon Dioxide Current Flow ends, as the Gate Voltage Supply then sees a Reverse Biased Drain, (and Source) Junction. Channel Region Inverting Avalanche Minority Carrier production at the Source Junction continues, under the control of the Applied Gate Voltage, and said Minority Carriers are caused to mediate a Drain Current Flow under the influence of applied Drain to Source Voltage. Some Minority Carriers are still lost through the leaky Oxide though, hence the requirement for Gate Current remains.

As stated elsewhere in this Report, we have shown feasibility, but not consistency and repeatability in the work completed. However, hopefully without sounding self serving, let me say that the results achieved, though not perfect, are acutally pretty good in view of how Research often goes, (and without much focused effort would have so gone in the present scenario)**. The results we have achieved are very definitely encouraging. Additional Research funding is definitely justified. The N and P-Channel MOSFETS results should be "Polished" and basic research investigation should be conducted regarding the Single Device Equivalents to CMOS.

** For instance, at the outset serious questions existed as to the ability of Chromium to form Rectifying Junctions with both N and P-Type SIlicon, when the Chromium is deposited as a thin film and then annealed thereto, and we did not know if a common Anneal Temperature would work for both Silicon Types if the Rectifying Junctions could be so formed. We had, and still have, no reference which teaches the result we achieved. Some references hint that such might occur, (said references provided the insight to initiate the present work), but none directly state that the result does occur. It was a relief when, the first time I tried it, I obtained positive results. We have since found that either Electron beam or Sputtering System can be used to deposit Chromium Thin Films and allow achieving Rectifying Junctions by way of an Anneal at approximately four-Hundred degrees Centigrade.

There was also, at the outset, question as to whether sufficient minority carriers would even be available to form an inverted channel region in both N and P-type Silicon. This point was a serious point of concern in the Second Round NIST Evaluation Report.

Another serious point of concern was whether when the Chromium formed Rectifying Junctions with N and P-Type Silicon,

the Junctions would be of sufficient quality to act as Rectifying Junctions in a MOSFET on both N and P-Type Silicon. That is, would their Reverse Breakdown be sufficiently high on both N and P-Type Silicon. In the same area of concern was the question as to whether when the Junction forming Anneal was carried out the resulting change in Silicon topology would be such to preclude self-delineation of devices. That is, would formed Chromium Disilicide cause an expansion of Silicon in the Source and Drain Regions such that a reasonable Oxide depth would be passed, thereby effecting a hoplessly shorted Source, Gate and Drain. As well, at the outset we had no idea how deep a layer of Chromium would have to be deposited to form usable Rectifying Junctions at a reasonable Anneal Temperature. We now know that the layer can be very thin indeed, (eg. 800 Angstroms), and the Silicide forming Anneal does not cause a Device prohibiting expansion of the Silicon.

In addition, had we, (Professor Ianno and I), not brainstormed and Conceived the added Aluminum Deposition Step to the Original Fabrication Procedure to provide a Gate Metal, when we could not make the initial Procedure work, we would probably never have achieved any Results Consistency with the equipment available to us. And even regarding the Aluminum Deposition, we have, at times, had problems making it succeed. That is, when Aluminum is deposited in the Electron-beam Evaporator, rather than the Sputtering System, and not Annealed, we have seen instances where it does not adher well. We think that the Sputtering System works better because it doesn't heat the Substrate during a Deposition Process, by Radiation.

We have also found that in some fabrication processes, even though all indications were that we had etched through the Oxide in the Source and Drain Regions, prior to depositing Chromium, we actually had not done so. This means that an Anneal will not form any Chromium Disilicide, hence, Rectifying Source and Drain Junctions, as it is not in contact with the Silicon thereduring. This was discovered when we achieved a particularly low yield of working devices on some processed substrates, but after we had found Operating Curves in prior Devices, (eg. The April 27, 1994 breakthrough). If that problem had occured early on we would have never known we should be achieving working devices at all, and eventually probably would have concluded that the entire idea was unworkable.

On a completely different note, the Test Set Faulty Interface Adaptor problem I ran into, which is recited in the Historical Accounting Of the Supported Efforts Section of this Report, infra, could have prevented us from knowing that we had achieved any results at all, even though we had.

In view of all the variables that had to "self-allign" for me at appropriate times, to find the initial Results I did, it was almost a Mirical that I ever found any results at all. The truth in that statement can not be over emphasised! However, I put forth the effort, had excellent fabrication support from Professor Ianno and others at UNL, and most importantly------

Luck was with me when I needed it!

ADDENDUM

After a lot of analysis assuming we have an Inverted Channel Region Scenario, (see infra), it has occurred to me, and I must point out, that there is a way that a family of Drain Current Curves could be achieved without the requirement that MOSFET Channel Inversion occur, if the Silicon Dioxide is leaky. I believe, however, that this case is most likely in Devices in which Drain Current Flow begins offset from the Drain to Source Voltage Zero (0.0) Volts point on a Drain Current vs. Drain to Source Voltage Curves abcsissa in a direction representing a Forward Biased Source Junction is effected by Current Flow through Silicon Dioxide by application of Gate Voltage prior to application of Drain Voltage. As is discussed supra herein, this, and a Depleted Channel Region Resistance increase effect are the only causes I see for two-slope "Saturation-type" Drain Curves to develop in a Non-Inverted Channel Scenario.

Proceeding, say we have an N-Channel Device formed on P-Type Silicon, and that it has leaky Silicon Dioxide. When in a test circuit, we will have a Gate Voltage Source looking through said leaky Silicon Dioxide into two Rectifying Junctions, (Source and Drain), the opposite side of which Source is connected to Common, and the opposite side of which Drain is connected to Common through a Drain Voltage Source. Let use look at various Gate and Drain Bias Voltage States again:

If a Negative Gate and Drain Voltages are applied we should expect to see Drain Current flow through the Silicon Dioxide beginning where the Drain Voltage is more negative than the Gate Voltage, thereby Forward Biasing the Drain Junction, just as we do see. This case is no different than that we have analyzed before.

If we apply Negative Gate Voltage and Positive Drain Voltage, both Source and Drain Junctions will be Reverse Biased, as viewed from the Gate Voltage Source. We should expect to see no Drain Current flow, (unless the Drain Junction Breaks down in Reverse Bias), as the Drain Junction will be Reverse Biased looking at it from the Drain Voltage Source. Again this is not different than previously analyzed.

Now, if we apply Positive Gate Voltage and Negative Drain Voltage, (where we see Drain Current Curves), prior to Channel Inversion, we could see Current flow from the Gate Voltage Supply through the Silicon Dioxide and Channel Regions into and through Forward Biased Source and Drain Junctions to Common, with the Current flow through the Forward Biased Drain Junction also flowing through a Drain Voltage Supply. However, the Forward

Biased Source Junction will greatly limit the amount of voltage presented to the Drain Junction in the Channel Region, (which Source Junction appears Reverse Biased to Sufficient Drain Voltage Source, said Drain Voltage being of an opposite Polarity to the Gate Voltage). That is, the Drain Circuit will be comprised of the Drain Voltage Source in series with the Forward Biased Drain Junction, (again assuming the Channel is not inverted), the Channel Region side of which Forward Biased Drain Junction is generally at a Voltage level set by voltage division of the applied Gate Voltage, said applied Channel Region Voltage resulting from a Voltage Division being between the resistance of the Forward Biased Drain Junction plus some Channel Region Resistance, and the Gate Silicon Dioxide Resistance plus some Channel Region Resistance. With Zero (0.0) Drain Voltage applied, however, the Voltage atop the Source Junction in the Channel Region will be at a Forward Biased drop across said Source Junction, perhaps in series with some Voltage drop effected by said Current flowing through the Silicon Dioxide as it flows through some Channel Region Resistance adjacent to said Source Junction. Now, as the applied Gate Voltage is increased, the Positive Voltage appearing atop the Source Junction in the Channel Region can increase by drop across the Channel Resistance between the Silicon Dioxide and the Source Junction. This could lead to increased Drain Current Flow, through the Gate Voltage Source, for a certain applied Drain Voltage as said Voltage is of an opposite Polarity to that applied to Non-Channel side of the Drain Junction. Thus a series of Drain Current Curves could develop as the Gate Voltage is increased. Said Drain Current flowing through the Gate Circuit. However, the "Origin" of said Drain Current Curves will not be a specific "Common Point", emphasis added. The Origin of the Drain Current Curves would shift to a more Positive point as the applied Gate Voltage is made more Positive. The shift will not be a drastic as is the case where the Source is lifted from the Common and the entire applied Gate Voltage appears at the top of the Source Junction, but will be reduced by the effect of the Voltage Division between the Silicon Dioxide, and the Channel Resistance and the Source Junction. (Note that if the Source is lifted from "Common" Forward Bias Drain Current Flow begins at the point where the Drain Voltage Source goes Positive with respect to the Gate Voltage Source, see Figs. 35 & 36). Now, while a Non-Inverted Channel Region family of Drain Current Curves could develop, it is difficult to see how they could occur where the Drain Current Curves all start at a true "Common Point" of zero (0.0) Volts, or thereabouts. That is, where the Source Junction voltage in the Channel does not change significantly with applied Gate Voltage as a result of the above described Voltage Division involving Channel Resistance atop the Source Junction, thereby causing the Drain Current initiation point to move Positive, there is not any added "Driving Force", (ie. increased Channel Region Voltage above the Source Junction as a function of applied Gate Voltage), to effect a Family of Drain Current Curves. If the Channel

Region Voltage above the Source Junction remains essentially the same for any applied Gate Voltage, then sweeping Drain Voltages will cause the same Drain Currents to flow regardless of applied Gate Voltage.

One could argue though that we have a Non-Inversion Channel Scenario in which the Gate Voltage Source appears through the Silicon Dioxide as a high impedance Current Source to the Channel, Current from which divides and goes part through the Forward Biased Source Junction and part of which goes through the Forward Biased Drain Junction, (said Source and Drain Junctions being referred to as seen by the Gate Voltage Source). Even though the Voltage in the Channel Region above the Forward Biased Source Junction, (as seen by the Gate Voltage Source), would stay relatively fixed at a Source Junction Forward Bias Drop Voltage level, increasing the Current flow from the Gate Voltage Source by increasing the Gate Voltage Source Voltage, would serve to increase the Drain Current Flow, via Current Division, as a function of Gate Voltage Source applied Voltage. Based upon results I have achieved, I can not rule this out, except that the Drain Current Curves obtained do not generally show a doubling of Drain Current Flow for a doubling of Applied Gate Voltage, as would be expected under this Scenario. (See for instance Fig. 27, where, at fifteen (15) Volts Drain to Source, a Gate Voltage of three (3) Volts causes a Drain Current of approximately twenty (20) microamps, but a Gate Voltage of six (6) Volts causes a Drain Current of only approximately twenty-five (25) microamps rather than forty (40) microamps. Also a Gate Voltage of twelve (12) Volts causes a Drain Current of only forty (40) microamps rather than fifty (50) microamps. Other Figures show similar results.)

Now, we still have the problem of explaining how a "Saturation-type" Drain Current vs. Drain to Source Voltage Curves could develop. if we assume a Non-Inverted Channel Scenario, the Drain Current "Saturation" characteristic could be the result of Gate Current initially flowing into a Forward Biased, (as caused by the Gate Voltage Source), Source Junction to Common. That would mean however, that any Drain Current Curves would have to begin from this Drain to Source offset point, emphasis added. When a Drain Voltage is applied, said flowing Gate Current might be diverted through the Drain Junction. Now, initially a low resistance path through the Source Junction might exist until said Source Junction is conducting essentially no Current, and appears Reverse Biased to the Drain Voltage Source. Another way to view this is that a Voltage Division could occur between the applied Gate and Drain Voltage Source Voltages between the Silicon Dioxide and the Channel Region Resistance adjacent to the Drain Junction. At the point where the Source Junction goes Reverse Biased the Drain Voltage Source would pull Current from the Gate Voltage Source only through a higher effective resistance Silicon Dioxide and

some Channel Resistance. This could form a two part "Saturation-like" Drain Current Curve. (Note that a Drain Current "Saturation" Characteristic indicates that a sudden increase in effective Resistance as seen by the Drain Voltage Source occurs). This could be the case, for instance, in Devices which provided the Drain Current vs. Drain to Source Voltage Curves in the Figures wherein Drain Current starts to flow at prior to zero (0.0) Drain to Source Voltage, (ie. most of the Figures). However, I do not think this explains the Figs. 9, 10, 28 and 31, (see supra), Drain Current results, where Drain Current Conduction begins at zero (0.0) or thereafter, rather than therebefore, again emphasis added. That is, if the Source Junction is never Forward Biased, it can't be caused to come out of Forward Bias and effect a major "Saturation" Drain Current Characteristic effecting Resistance change presented to the Drain Voltage Source. And, for the Source Junction to be Forward Biased requires that the Drain Current Curves begin atop that Forward Bias on the Drain to Source Voltage abcsissa. I say this as no current would be flowing in the Source Junction to be diverted into the Drain, hence, no low resistance pathway would initially exist through the Source Junction. Another way to say this is that the Source Junction would never be biased to a low Resistance point of its Current vs. applied Voltage Curve. I think to explain the Drain Current Curves in Figs. 9 and 10, 28 and 31 we must assume an Inversion Channel is formed, and that the analysis provided infra herein which assumes such, at least might be correct. This is because the Drain Current Curves do not start at a Common Point offset a Forward Biased Voltage drop above Common. Again for emphasis, without the presence of a Forward Biased Source Junction to bring out of Forward Bias, by Voltage Division of applied opposite Polarity Drain Voltage, it is difficult to account for the presence of sudden onset "Saturation-type" Characteristic shaped Drain Current Curves in a Non-Inverted Channel Scenario. However, there is an additional element in the parallel combination of the Gate Oxide and Voltage Source path to Common and the Source Junction to Common, that could change in effective resistance, which, again, is really what a "Saturation" Characteristic Drain Current Curve indicates. Said element is the Channel Region Resistance. Application of a Gate Voltage of a polarity intended to "Invert" the Channel Region will first "Deplete" it, thereby causing its effective Resistance to increase. In fact if we view Figs. 11 and 12 supra, we almost have to conclude that Channel Region "Depletion" is evidenced thereby. Note in said Figs. 11 and 12 are for P-Channel Devices formed on N-Type Silicon and that when Positive Polarity Voltage is applied to the Gate and the Drain to Source Voltage is swept negative to positive, we see Drain Current Flow Curves starting where the Drain Junction would become Forward Biased, which Drain Current Curves appear very much like a Diode Current vs. Voltage Characteristic in which very little series Resistance is present. This would indicate that the Silicon Dioxide Resistance must be relatively very low. (Compare the

Drain Current Flow Curves in other Figures under similar conditions). Now, if we apply Negative Polarity Voltage to the Gate and assume that a Forward Biased Source Junction comes out of Forward Bias and shifting all current flow through the Silicon Dioxide, then we should expect to see Drain Current Curves with a very large slope. That is, we have seen that the Silicon Dioxide is of a low Resistance by prior discussed observation. We see, however, low slope "Saturation-type" Drain Current Curves appear. This tells me that a Resistance which is other than the Silicon Dioxide Resistance, is in series with the Forward Biased Drain Junction, (again assuming no Channel Region Inversion). The only element left to provide this increased Resistance is the Channel Resistance, and it can only increase if it is depleted of carriers. Combined with the observation that I have made that Gate Current, in some tests decreases when Drain Current increases, I think Figs. 11 and 12 tell us that even in the presence of very leaky Silicon Dioxide, Channel Region Depletion can be effected. I know of no other explanation for the appearance of "Saturation-type" Drain Current Curves in Figs 11 and 12. Now, if Channel Region Depletion can be effected, it is likely that Channel Region Inversion can be as well, particularly in Devices with higher quality, (higher Resistance), Silicon Dioxide present. The fact that the Fig. 12 Drain Current Curves seem to proceed from "Saturation" to a high slope Characteristic as the Drain Voltage is increased, might be evidence that the Channel Region has inverted and that the Drain Current has become a function of Reverse Bias across the Drain Junction. Note, that the Channel Region might receive Inverting influence from the applied Drain Voltage, it being of opposite and proper polarity with respect to the applied Gate Voltage, even though major Inverting influence is typically caused by applied Gate Voltage with resepct to the Source. I think such insight might help to also explain why the Drain Current Curves in Fig. 35, for instance, show greater than a magnitude doubling between zero (0.0) and fifteen (15) applied Drain Volts, when the Gate Voltage increases from zero (0.0) to fifteen (15) applied Volts. If all that is occuring is that a doubling of Voltage is applied between Drain and Gate, with only Silicon Dioxide and a Forward Biased Drain Junction thereinbetween, then one must postulate that the Silicon Dioxide presents with a nonlinear resistance as a function of Voltage applied thereacross. I feel this is unrealistic, (though admittedly possible). I feel we are seeing the effect of Channel Rgion Depletion and Inversion.

Referring again to Fig. 12, for instance, I feel that a reasonable explanation for the Multi-Region Drain Current Curve Characteristics is that the Channel Region progreses from:

Non-Inverted for zero (0.0) applied Gate Volts and any applied Positive Drain Voltage;

to Depleted for applied Negative Gate Voltage and Positive Drain Voltage below approximately three (3) to six (6) Volts;

to Inverted for any applied Negative Gate Voltage and Drain Voltages above approximtely three (3) to six (6) Volts.

As a review, in an assumed Inverted Channel Scenario we have change in Drain Junction Reverse Bias Tunneling Current, as a function of Gate Voltage Effected Field Induced Effective "Inverted" Channel Region Silicon Doping Levels as an explanation to obtaining "Saturation-type" Drain Current Curves. In a Non-Inverted Channel Region Scenario the explanation is change in effective resistance of the Source Junction when coming out of Forward Bias, and/or increased Channel Region Resistance as a result of Depletion thereof. The Channel Region and/or Source Junction and/or the Silicon Dioxide Resistance, has to suddenly become higher to effect a sudden higher Resistance to the Drain Voltage Source. It would appear, in view of Figs. 11 and 12 that Depletion of the Channel Region is a most likely explanation for the presence of "Saturation-type" Drain Current Curves in a Non-Inverted Channel Region Scenario, with the change in Resistance of a Source Junction coming out of Forward Bias also being a possible contributing factor. Again Fig. 12 seems to also indicate that a Drain Current Characteristic slope increasing Channel Region Inversion occurs above an applied approximately three (3) to six (6) Positive Drain Volts, said applied Drain Volts serving to aid with Channel Inversion in addition to the influence of applied Gate Voltage with respect to the Source, (which Gate to Source Voltage is of a smaller magnitude, said Source being referenced to Common rather than held at a Positive Voltage as is the Drain Junction by the Drain Voltage Supply).

Now, I think we've seen both Inverted Channel and Non-Inverted Channel Device Operation without the ability to separate the effects. As regards Inverted Channel operation, we have shown that "Inversion" does occur in Silicon, (See Figs. 37 - 39), at applied Gate Voltage levels we have worked with, utilizing the same Silicon Dioxide as we used in fabricating our MOSFETS. This was shown by way of direct MOS Capacitor Tests and Figs. 11 and 12 are also strong evidence that at least Channel Region Depletion occurs in Devices, and Fig. 12 seems to suggest that Channel Region Inversion also occurs. Also, as I've stated elsewhere, I have seen Gate Current Flow decrease when Drain Current Flow increases, in tests of some Devices, utilizing an ampmeter in a Gate Circuit. Although I did not at all understand this effect when first discovering it as alluded to on page 7 of the Fifth Quarterly Report, (and also note that every Device test did not provide the result), I now believe it is firm evidence that the Channel Region does Deeply Deplete if not completely Invert, thereby converting Source and Drain Junctions toward a Reverse Bias, (with respect to applied Gate Voltage),

thereby greatly minimizing or outright blocking Forward Bias Current Flow from the Gate to the Drain, and simultaneously causing Tunneling Drain Current to flow from the then Reverse Biased Drain Junction, (with respect to the Drain Voltage Source), through the then Forward Biased Source, (again as seen by the Drain Voltage Source).

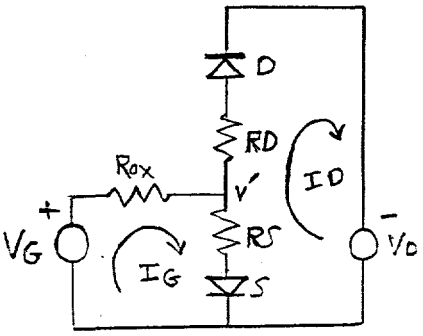
Being realistic, it should be noted that the Drain Current Curves we have seen might, in some cases, be a hybrid result, comprised of a merging of the many possible effects described in this Report. This conclusion would seem to be supported by reference to Figs. 35 and 36 where there are shown P-Channel Device Drain Current vs. Drain to Source Voltage Curves for Source Junction connected to Common, and Lifted therefrom respectively. First, the Fig. 35 Drain Current Curves start from a Common Point of approximately zero (0.0) Volts, rather than a Forward Bias Source Junction Voltage drop level, and Fig. 36 shows Gate Current flow through the Silicon Dioxide and Forward Biased Drain Junction can occur. Note the slopes of the respective Drain Current Curves for corresponding Gate Voltages are different in said Figures 35 and 36, indicating that the Drain Voltage Source sees somewhat different effective Resistances when the Source is connected to Common and when its lifted. That would seem to indicate that the Source Junction never becomes Reverse Biased, as viewed from the Drain Voltage Source. That would imply a Channel Inversion effect, at least at the more negative applied Gate Voltages. Such might also occur in the Fig. 36 lifted Source Drain Current Curves at a high difference between applied Drain and Gate Voltages even though Current would flow through the Gate Oxide. As well, note that projecting the slopes of the Drain Current Curves in Fig. 35 to the Negative Drain to Source Voltage Abscissa crossing point, does not show start of Drain Current Conduction at a point where the Drain Junction would go forward biased by overcoming the applied Gate Voltage, as is shown in the Fig. 36 lifted Source case. That is, the Drain Junction seems to remain nonconductive far after it should be Forward Biased by comparison of applied Gate and Drain Voltages, based upon Drain Current Curve slope.

The leaky Silicon Dioxide problem, it must be concluded, greatly complicates the situation, and analysis of the results is very difficult in view thereof. It remains my opinion, however, that at least some of the Drain Current Curves we have obtained are representative of true Inverted Channel Region MOSFET operation, via control of Tunneling Current through a Reverse Biased Schottky barrier Drain Junction and Forward Biased Source Junction, by way of Field Effected Inverted Channel Region Doping Levels. I will also add that the Drain Current flow levels we have seen are well within the ranges that both Silicon Dioxide leakage Currents, and Reverse Biased Schottky barrier Drain Junction Tunneling Currents would provide. We can not therefore use the levels of Drain Current flow to distinguish what is their

cause in various cases, nor do the shapes of the Drain Current Curves allow absolute determination of what effects combine, in what relative magnitudes, to provide the results achieved in any particular case. The only realistic way to sort things out is to do continued fabrication efforts until we achieve MOSFET Devices which demonstrate high quality Silicon Dioxide in separate Voltage Application thereacross tests, and then observe what Drain Current Curves appear in the absence of Silicon Dioxide leakage Currents, emphasis added.

It is also noted that Silicon Dioxide quality is a factor which consumes the full time focus of numerous Engineers in Industry. That we've apparently run into serious Silicon Dioxide quality based problems is, thus, not really surprising. Not only is the growth of Silicon Dioxide critical to its eventual quality, but as well, processing steps which might contaminate it, (liquid acid etching), or which require application of electric fields thereacross, (plasma etching or sputter deposition of Aluminum or Chromium metals for instance, can cause it to breakdown), are also critical. There are a "million +" reasons as to why we have run into Silicon Dioxide quality problems.

As I've stated elsewhere in this Report, what might be considered surprising is the fact that we've achieved so many favorable results from our efforts. The fact we have achieved so many significant results indicates that additional support of our work is justified beyond any question.



FOR DRAIN CURRENT "ID" TO DEMONSTRATE SATURATION CHARACTERISTICS IN A NON-INVERTED CHANNEL SCENARIO, THERE MUST BE A SUDDEN CHANGE IN THE EFFECTIVE RESISTANCE SEEN BY THE DRAIN VOLTAGE SOURCE "VD". IF A "VG" EFFECTED "IG" CURRENT FLOW CAUSES JUNCTION "S" TO BE FORWARD BIASED, AND "VD" BRINGS IT OUT OF FORWARD BIAS, THIS MIGHT CAUSE AN EFFECTIVE SUDDEN INCREASE IN THE RESISTANCE LOOKING FROM POINT "V'", AND EXPLAIN A SATURATION DRAIN CURRENT "ID" CHARACTERISTIC. AS WELL, DEPLETED CHANNEL REGION RESISTANCE (RD & RS) CAN PROVIDE INCREASED RESISTANCE AS SEEN BY A DRAIN VOLTAGE SUPPLY.

(As speculation it is offered that the applied Drain Voltage as well as the applied Gate Voltage both serve to cause the Channel Region to Deplete and Invert in the present Schottky barrier MOSFET devices. This operation is very different from Diffused Junction MOSFETS and Schottky barrier MOSFETS which operate with the same Polarity Voltage on both the Gate and Drain. Sweeping

the Drain Voltage in the present Schottky barrier MOSFET Devices, as well as increasing the Gate Voltage, then serves to Deplete and Invert the Channel Region as opposed to just application of Gate Voltage. Once Inverted, Gate Current flow is cut off, (as I've seen occur), as the Gate Voltage Source then sees Reverse Biased Source and Drain Junctions. AS A RESULT, THE PRESENT MOSFETS MIGHT BE MORE TOLLERABLE OF LOW QUALITY SILICON DIOXIDE THAN ARE CONVENTIONAL MOSFETS. THE PRESENT SCHOTTKY BARRIER MOSFETS MIGHT BE ABLE TO ROUTINELY UTILIZE LOWER QUALITY SILICON DIOXIDE. IF THIS IS THE CASE, INDUSTRY WOULD WELCOME THE RESULT. SILICON DIOXIDE QUALITY IS AN EXPENSIVE COMMODITY!!! IT VERY WELL MIGHT BE THAT IF THIS WERE NOT THE CASE, I'D NEVER FOUND ANY MOSFET DRAIN CURRENT CURVES AT ALL WITH THE LOW QUALITY SILICON DIOXIDE PRESNT, EMPHASIS ADDED.

CURVE TRACER CURRENT V. VOLTAGE (I-V) CHARACTERISTICS FOR RECTIFYING JUNCTIONS FORMED BETWEEN TEN-TO-THE-FORTEENTH PER CENTIMETER CUBED P-TYPE SILICON AND CHROMIUM DEPOSITED THEREON, WHILE SAID SILICON WAS HELD AT 200 DEGREES CENTIGRADE. A FIFTEEN MINUTE VACUUM ANNEAL AT THREE-HUNDREED-FIFTY (350) DEGREES CENTIGRADE WAS PERFORMED AFTER THE CHROMIUM DEPOSITION.

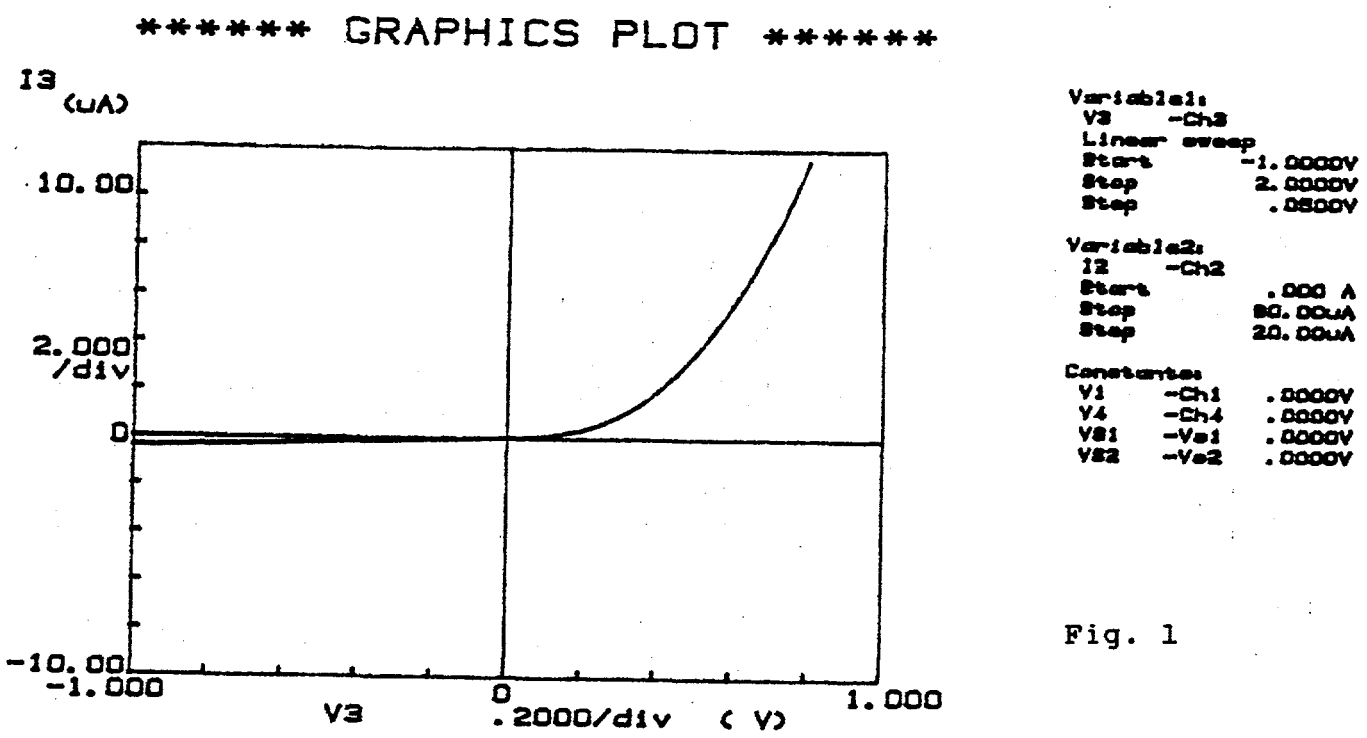


Fig. 1

CURVE TRACER CURRENT V. VOLTAGE (I-V) CHARACTERISTICS FOR RECTIFYING JUNCTIONS FORMED BETWEEN TEN-TO-THE-FIFTEENTH PER CENTIMETER CUBED N-TYPE SILICON AND CHROMIUM DEPOSITED THEREON, WHILE SAID SILICON WAS HELD AT 200 DEGREES CENTIGRADE. A FIFTEEN MINUTE VACUUM ANNEAL AT THREE-HUNDRED-FIFTY (350) DEGREES CENTIGRADE WAS PERFORMED AFTER THE CHROMIUM DEPOSITION.

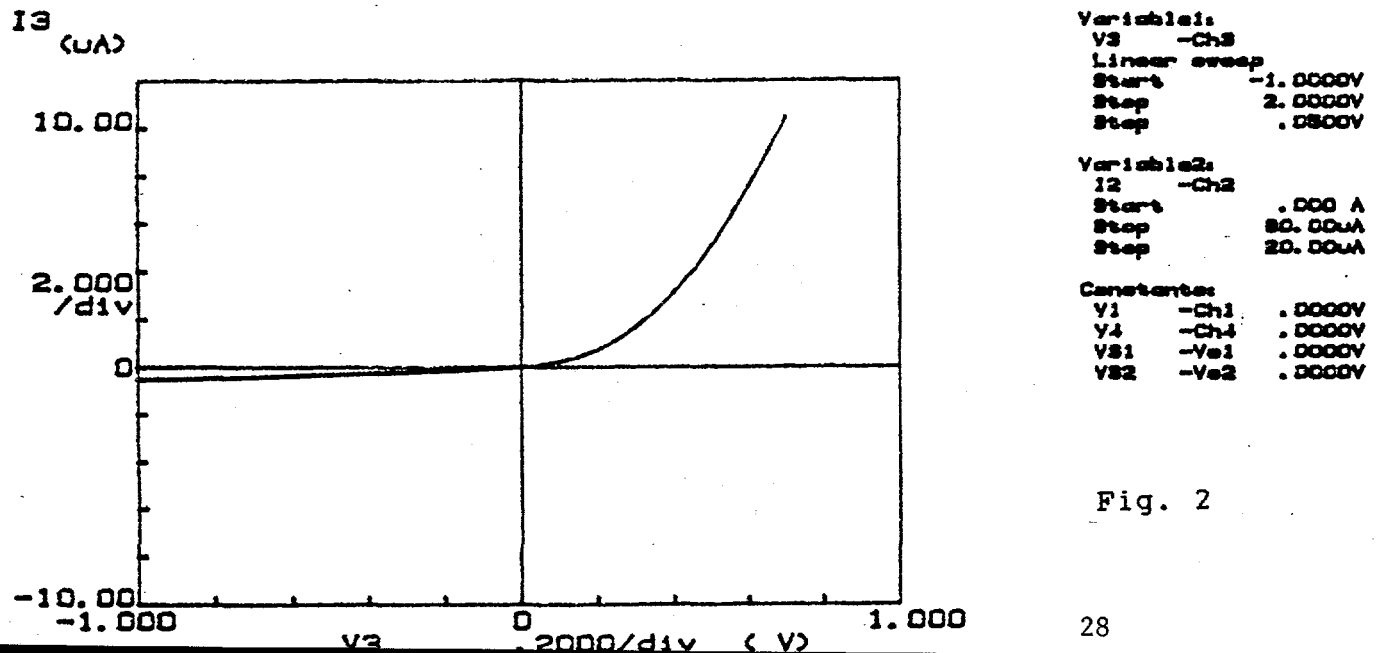


Fig. 2

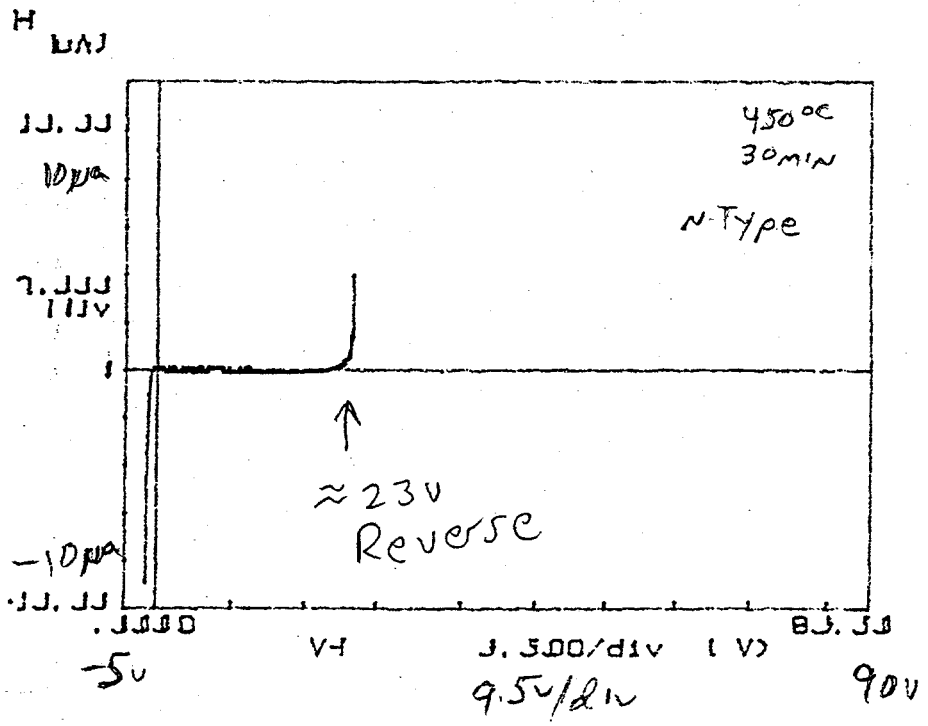

****** GRAPHICS PLOT ******
450°C
30min
N-Type
≈23V
Reverse
-5V
9.5V/div
90V

Fig. 3

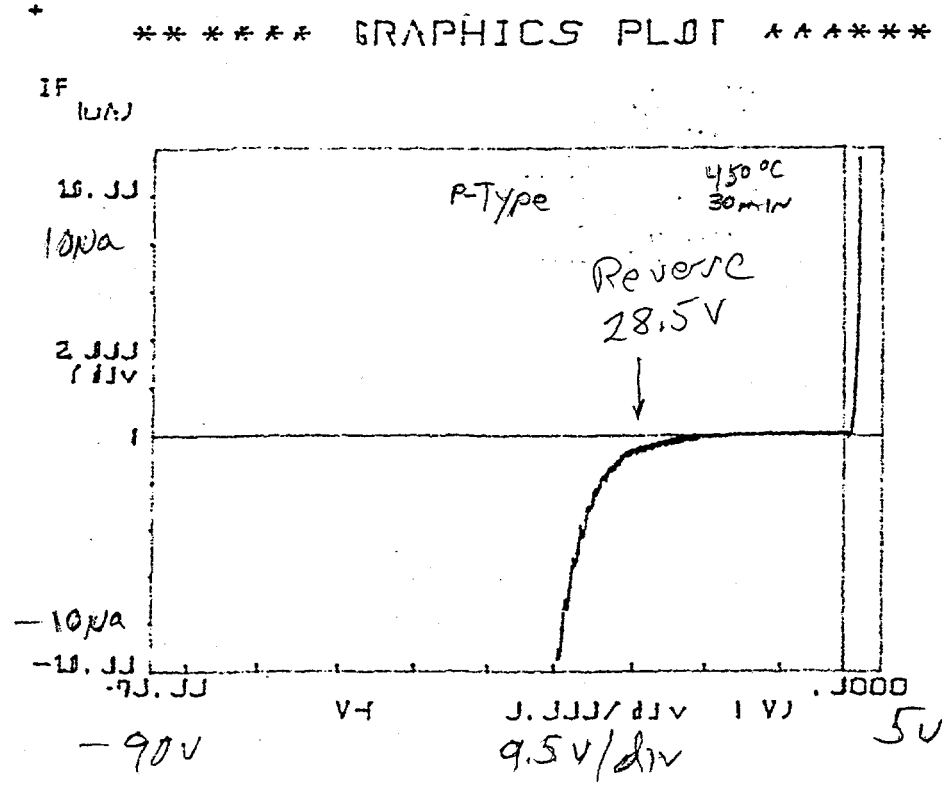

****** GRAPHICS PLOT ******
450°C
30min
P-Type
Reverse
28.5V
-90V
9.5V/div
5V

Fig. 4

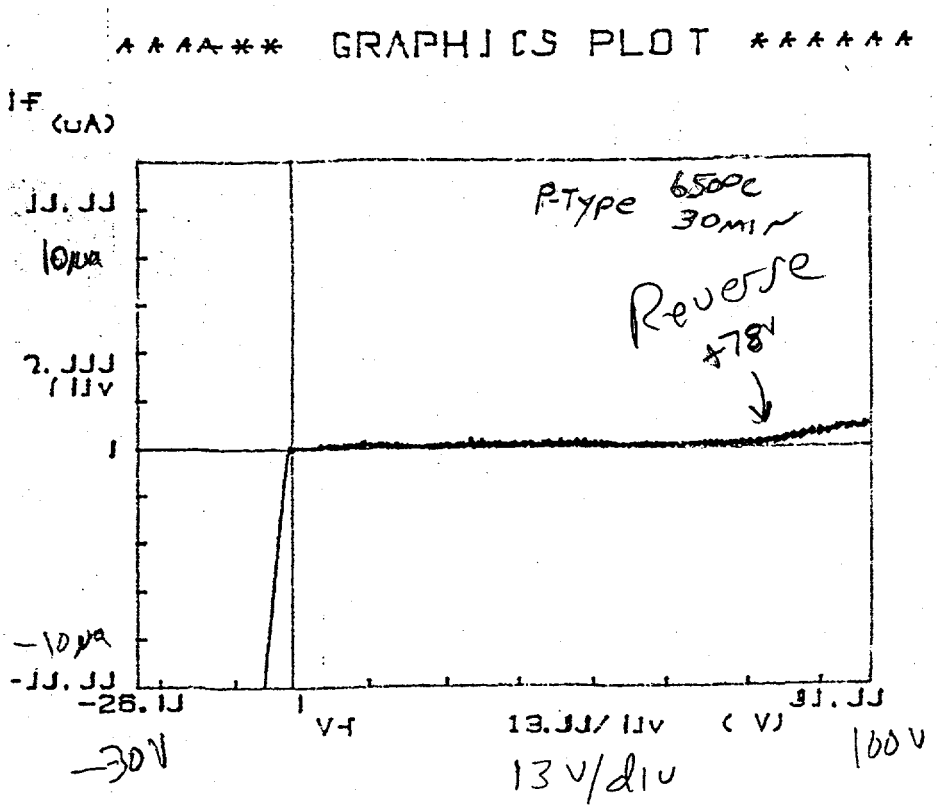

****** GRAPHICS PLOT ******
IF (uA)
10.00
10pA
2.000
1 V
-10pA
-10.00
-26.10
V-f
13.00/div (V)
30.00
-30V
13V/div
P-Type 650°C 30min
Reverse -78V
100V

Fig. 5

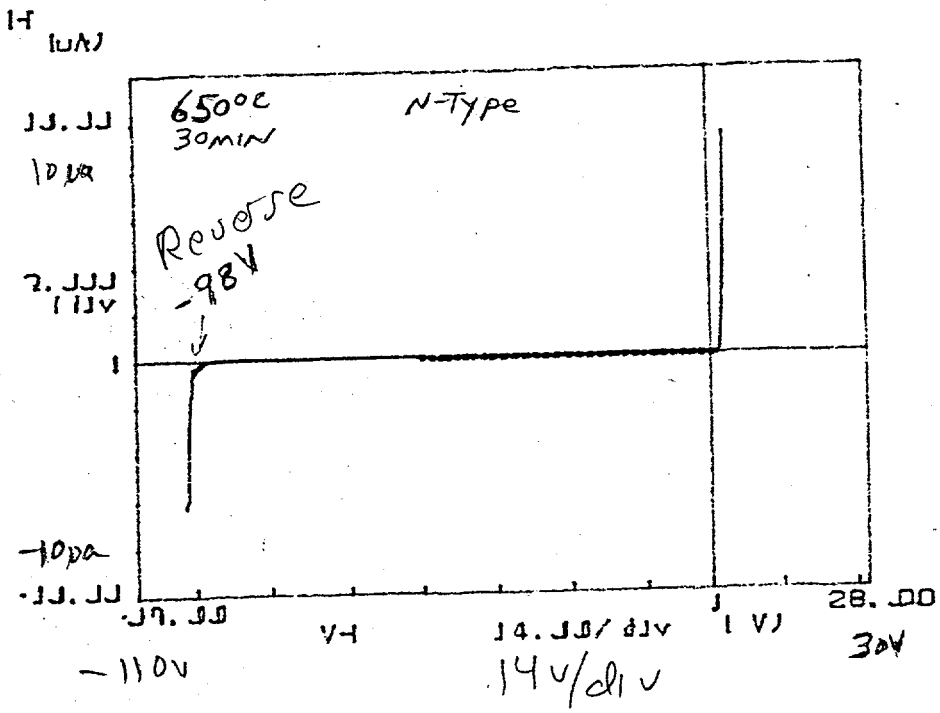
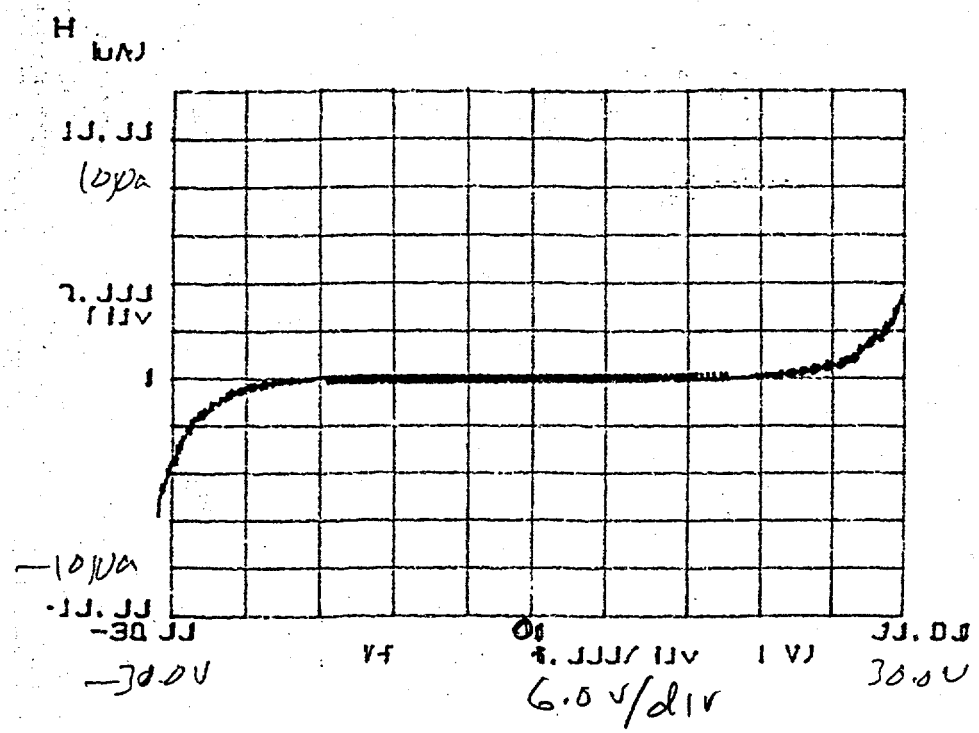

****** GRAPHICS PLOT ******
IF (uA)
10.00
10pA
2.000
1 V
-10pA
-10.00
-30.00
V-f
14.00/div (V)
28.00
-110V
14V/div
650°C 30min
N-Type
Reverse -98V
30V

Fig. 6



DRAIN TO SOURCE BACK TO BACK DIODE REVERSE BREAKDOWN

Fig. 7

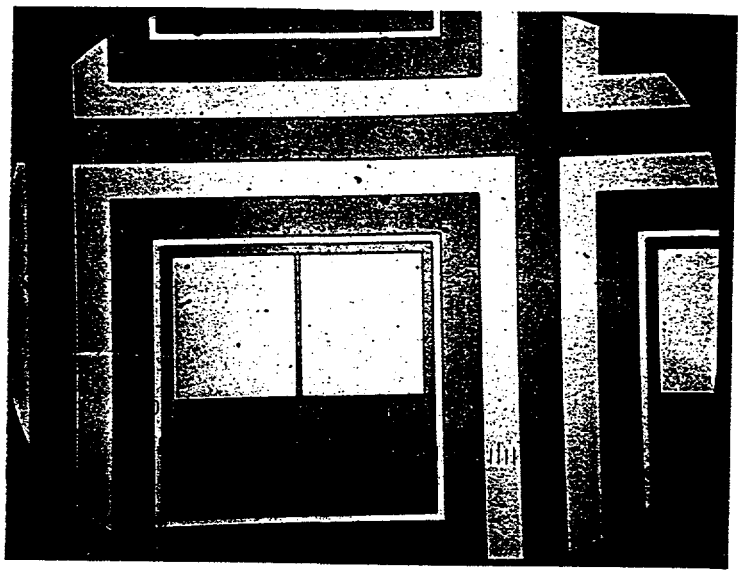
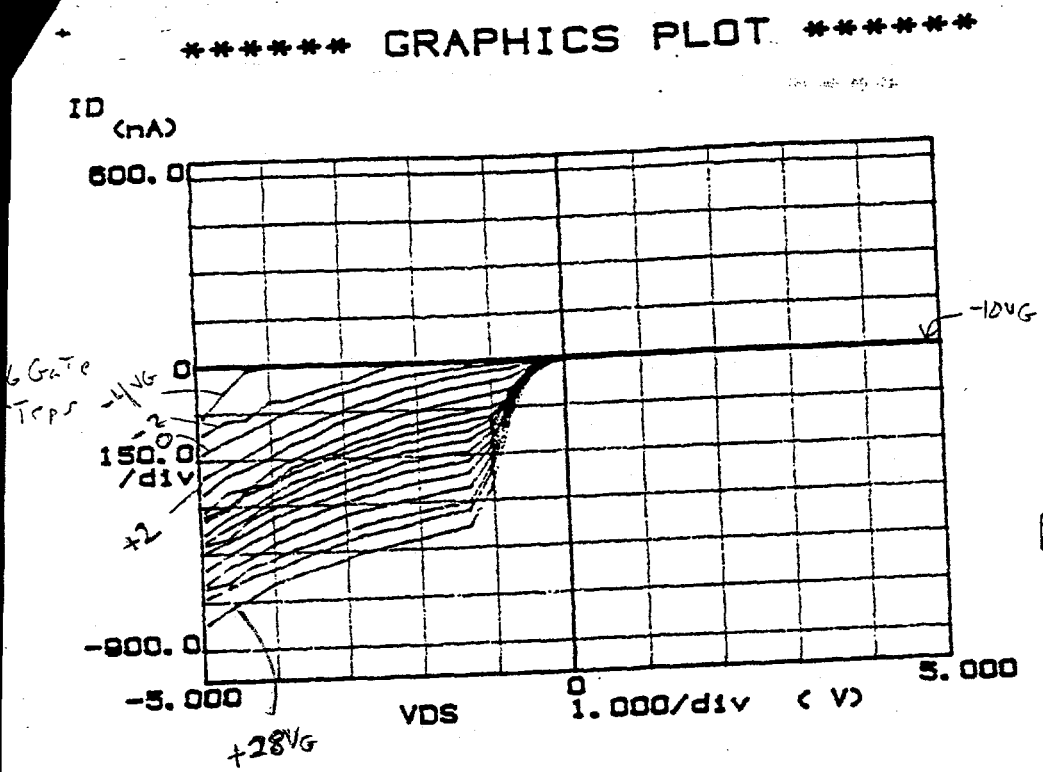


Fig. 8



Variable1:
VDS -Ch2
Linear sweep
Start -10.000V
Stop 5.0000V
Step .3000V

Variable2:
VG -Ch3
Start -10.000V
Stop 28.000V
Step 2.0000V

Constants:
VS -Ch1 .0000V

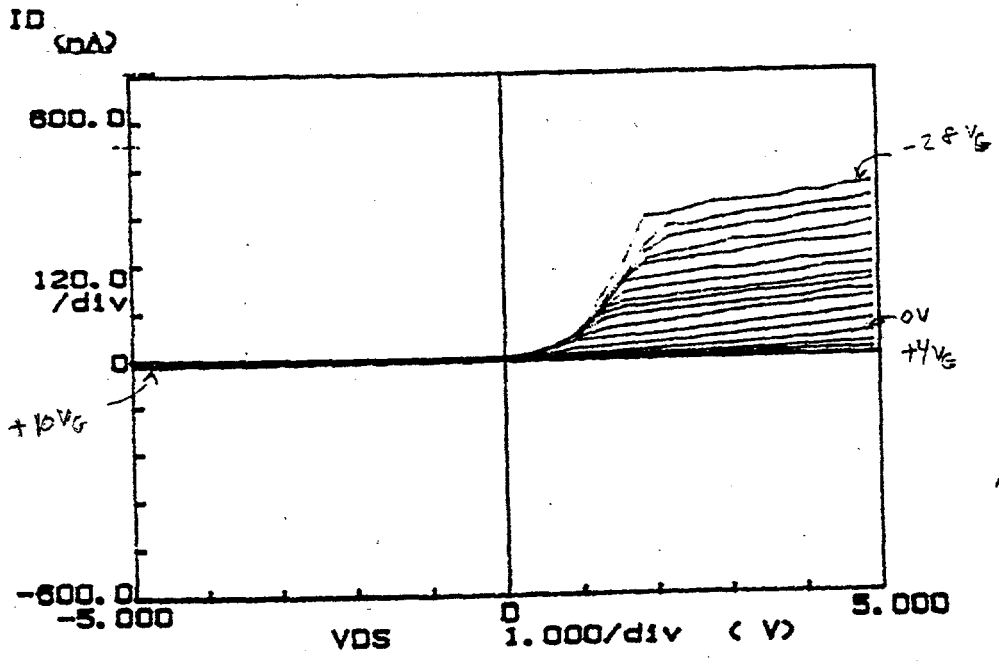
Curve Tracer Settings

P-Type

April 27, 1994

NO GATE METAL PRESENT, SEVENTY-FIVE MICRON DIAMETER GATE PROBE SETS ATOP GATE OXIDE AND SERVES AS GATE.

Fig. 9



Variable1:
VDS -Ch2
Linear sweep
Start -5.0000V
Stop 5.0000V
Step .3000V

Variable2:
VG -Ch3
Start 10.000V
Stop -28.000V
Step -2.0000V

Constants:
VS -Ch1 .0000V

Curve Tracer Settings

N-Type

April 28, 1994

NO GATE METAL PRESENT, SEVENTY-FIVE MICRON DIAMETER GATE PROBE SETS ATOP GATE OXIDE AND SERVES AS GATE.

Fig. 10

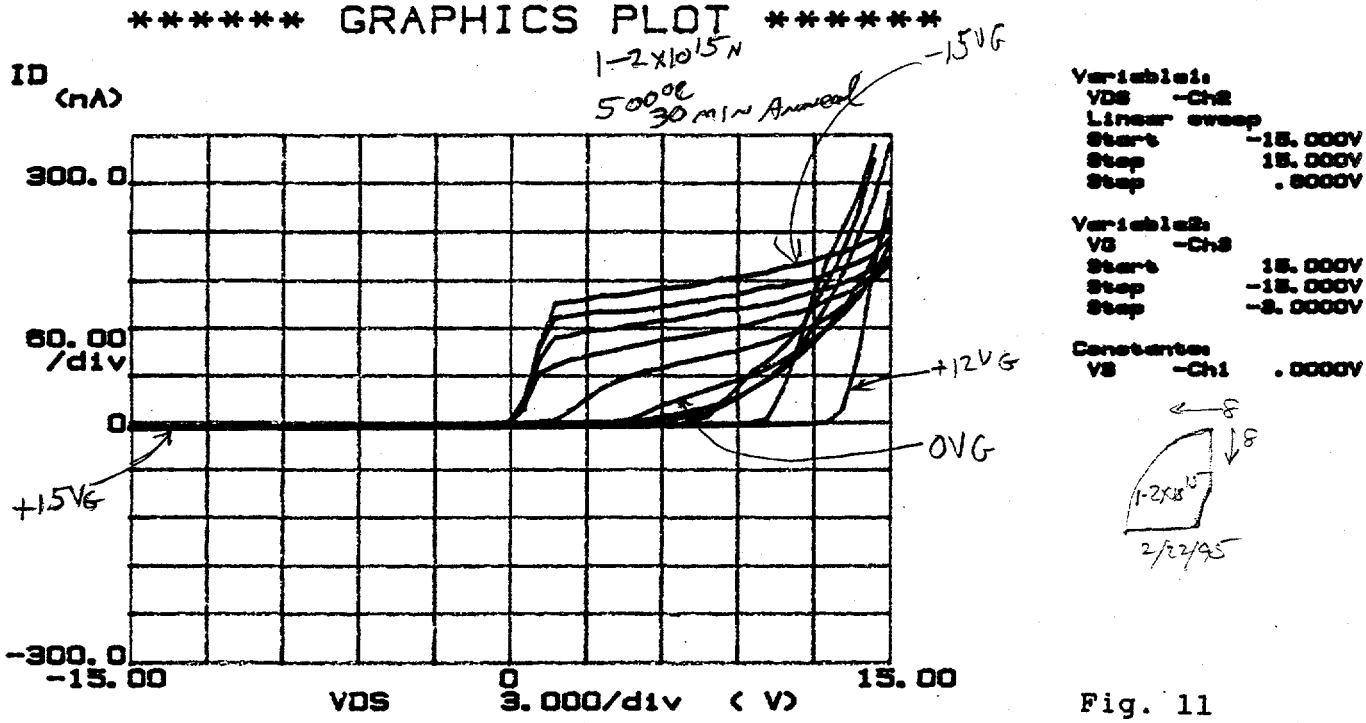


Fig. 11

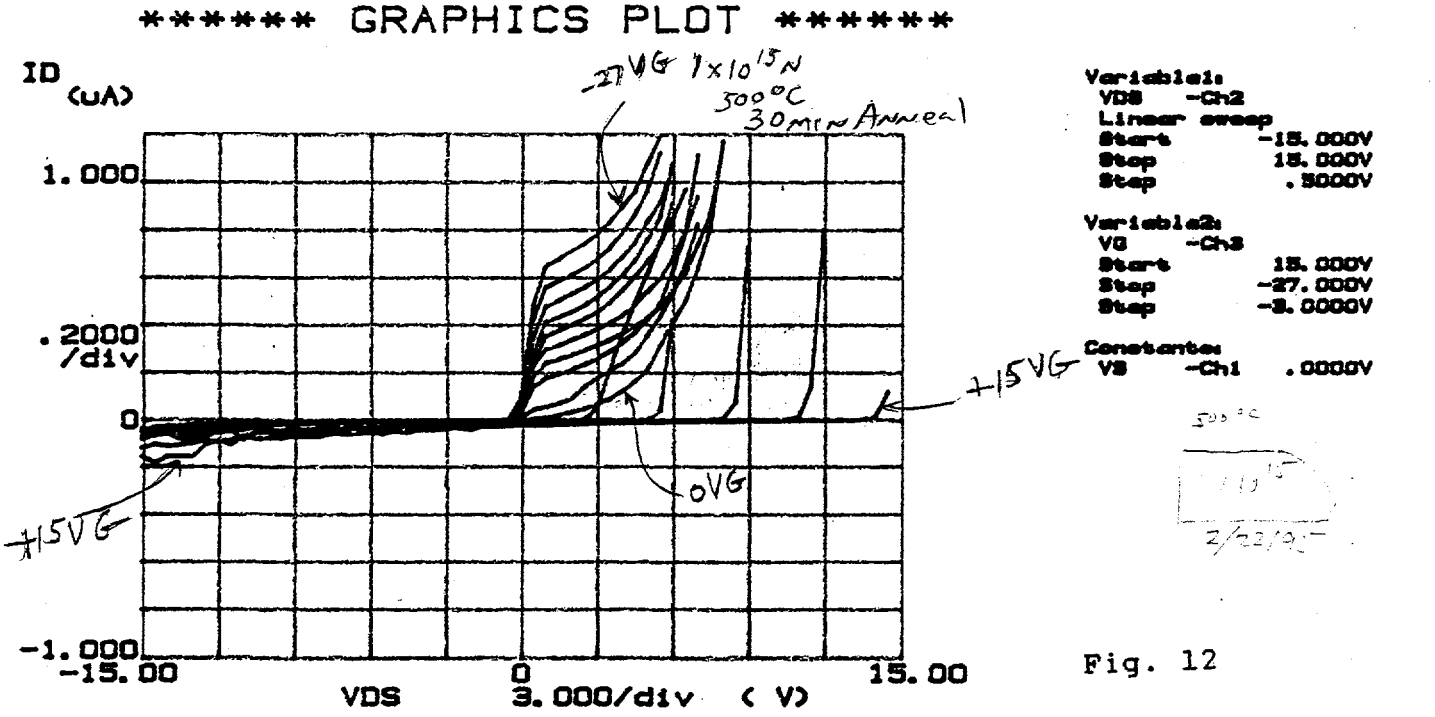


Fig. 12

WHEN (+) GATE VOLTAGE IS APPLIED SEE DRAIN JUNCTION GO FORWARD BIASED THROUGH THE SIO2. WHEN (-) GATE VOLTAGE IS APPLIED SEE SATURATION CURVES WITH GREATER THAN SIO2 RESISTANCE DEMONSTRATED. WE MUST BE SEEING CHANNEL REGION DEPLETION EFFECT.

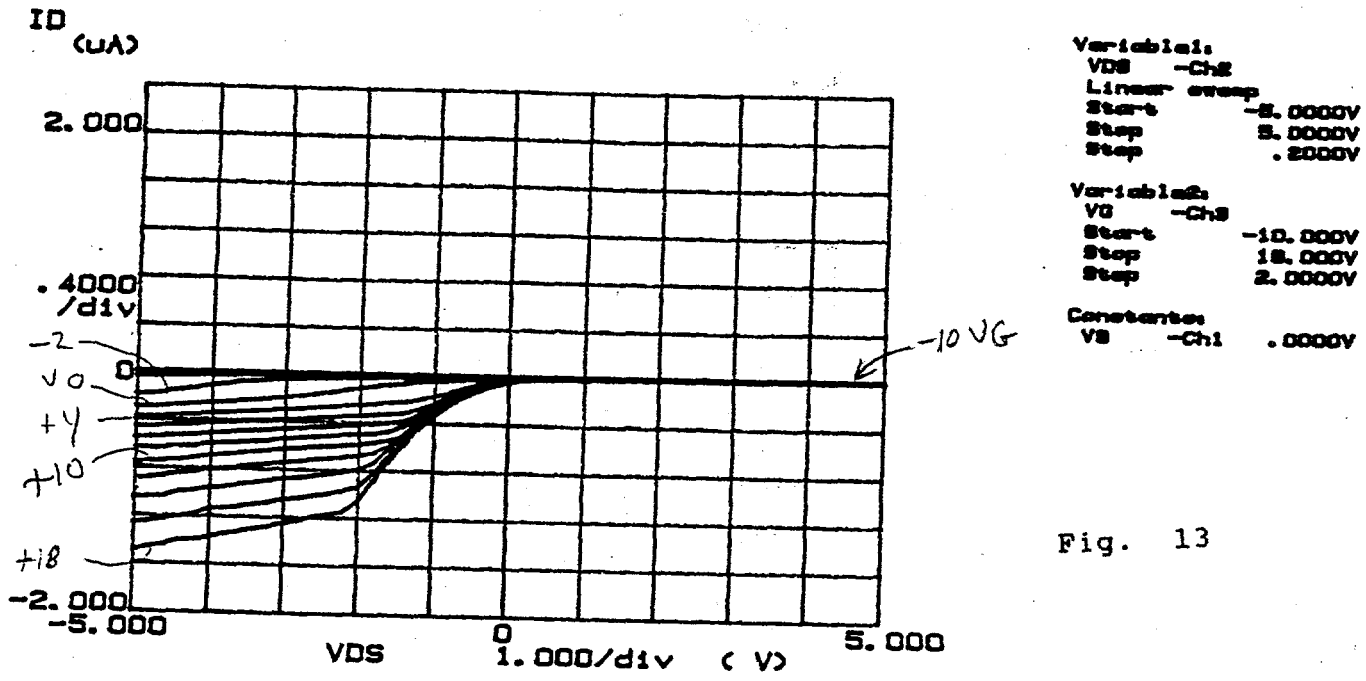

****** GRAPHICS PLOT ******
ID
(uA)
2.000
.4000
/div
-2
0
VO
+4
+10
+18
-10 VG
-2.000
-5.000
0
5.000
VDS
1.000/div (V)
Variable1:
VDS -Ch2
Linear sweep
Start -5.0000V
Stop 5.0000V
Step .2000V
Variable2:
VG -Ch3
Start -10.000V
Stop 18.000V
Step 2.0000V
Constants:
VB -Ch1 .0000V

Fig. 13

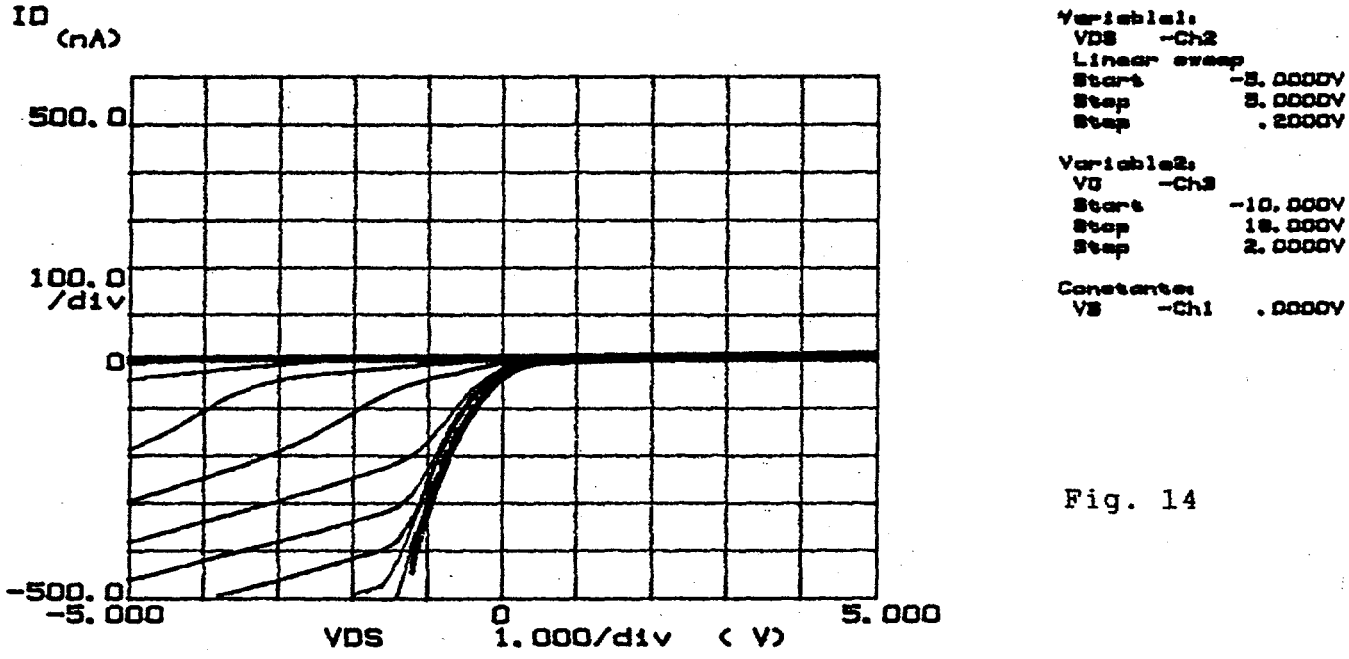

****** GRAPHICS PLOT ******
ID
(nA)
500.0
100.0
/div
0
-500.0
-5.000
0
5.000
VDS
1.000/div (V)
Variable1:
VDS -Ch2
Linear sweep
Start -5.0000V
Stop 5.0000V
Step .2000V
Variable2:
VG -Ch3
Start -10.000V
Stop 18.000V
Step 2.0000V
Constants:
VB -Ch1 .0000V

Fig. 14

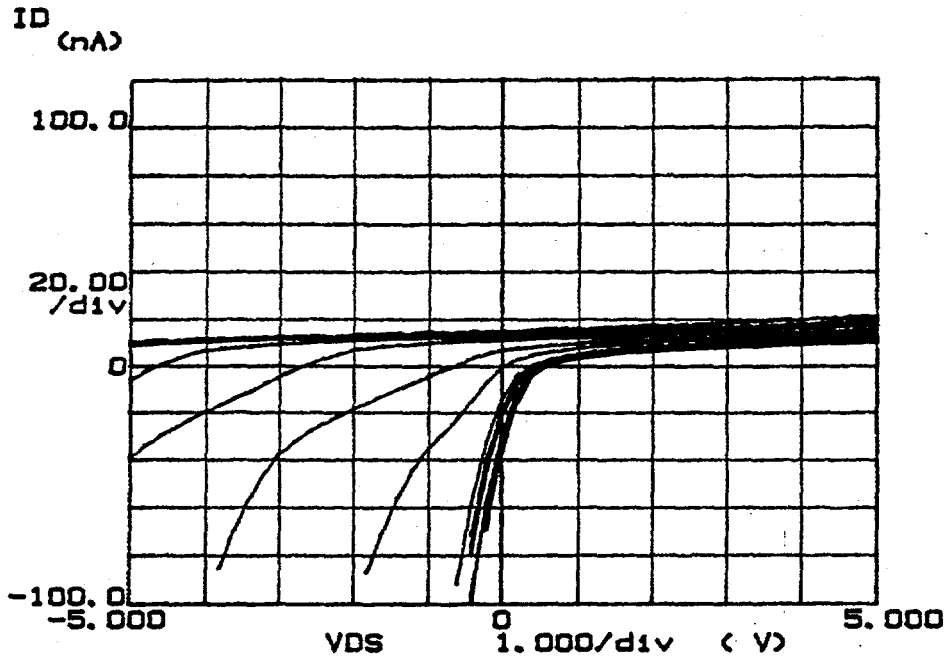

****** GRAPHICS PLOT ******
ID
(nA)
100.0
20.00
/div
0
-100.0
-5.000
0
5.000
VDS
1.000/div
(V)
Variable1:
VDS -Ch2
Linear sweep
Start -5.0000V
Stop 5.0000V
Step .2000V
Variable2:
VG -Ch3
Start -10.000V
Stop 10.000V
Step 2.0000V
Constants:
VS -Ch1 .0000V

Fig. 15

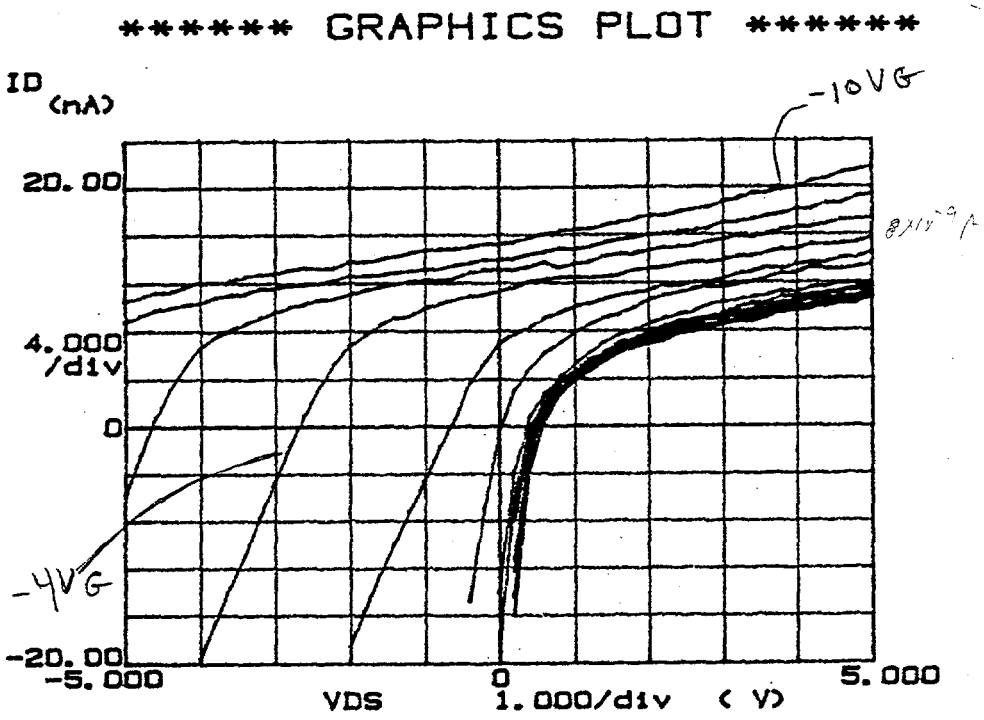

****** GRAPHICS PLOT ******
ID
(nA)
-10VG
20.00
4.000
/div
0
-4VG
-20.00
-5.000
0
5.000
VDS
1.000/div
(V)
Variable1:
VDS -Ch2
Linear sweep
Start -5.0000V
Stop 5.0000V
Step .2000V
Variable2:
VG -Ch3
Start -10.000V
Stop 10.000V
Step 2.0000V
Constants:
VS -Ch1 .0000V

Fig. 16

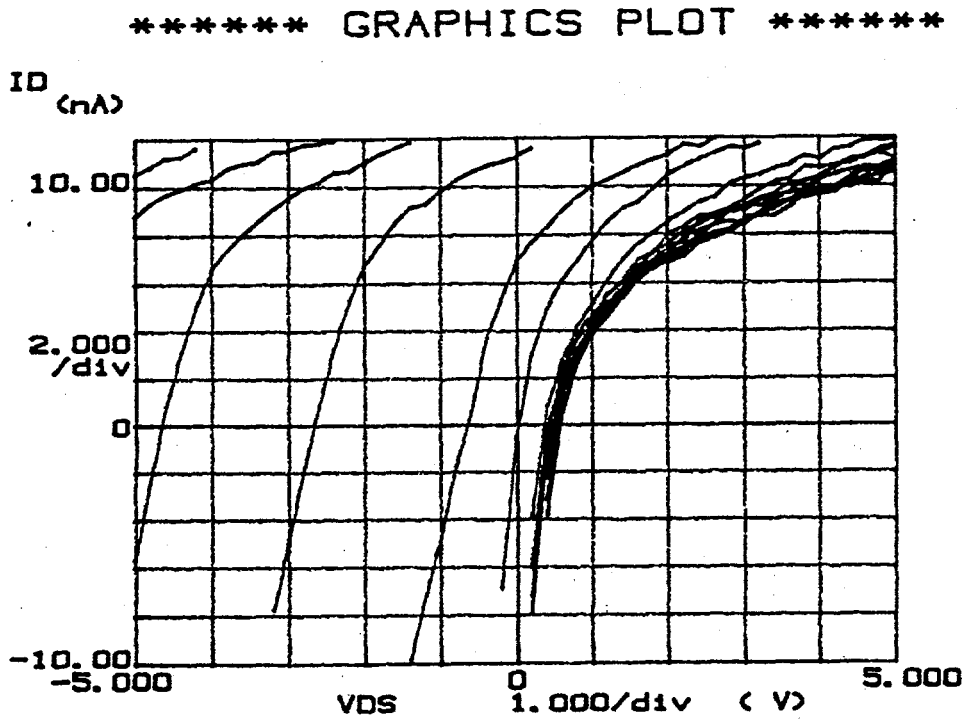

****** GRAPHICS PLOT ******
ID
(nA)
10.00
2.000
/div
0
-10.00
-5.000
0
5.000
VDS
1.000/div
(V)
Variable1:
VDS -Ch2
Linear sweep
Start -5.0000V
Stop 5.0000V
Step .2000V
Variable2:
VG -Ch3
Start -10.000V
Stop 18.000V
Step 2.0000V
Constants:
VS -Ch1 .0000V

Fig. 17

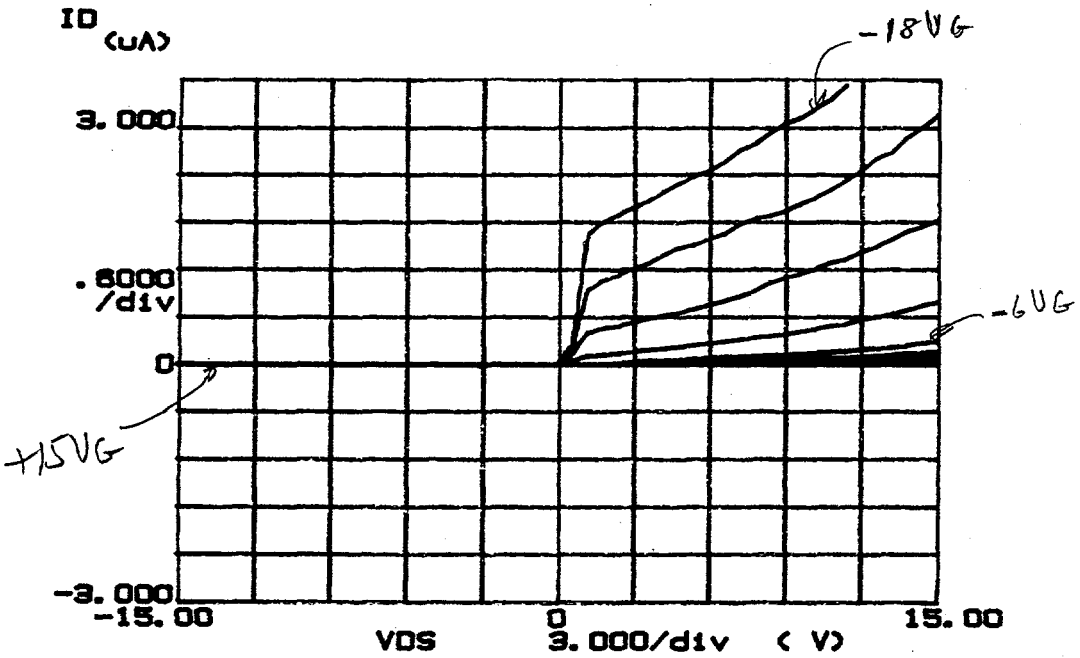

****** GRAPHICS PLOT ******
ID
(uA)
-18VG
3.000
.6000
/div
0
-6VG
+15VG
-3.000
-15.00
0
15.00
VDS
3.000/div
(V)
Variable1:
VDS -Ch2
Linear sweep
Start -15.000V
Stop 15.000V
Step .6000V
Variable2:
VG -Ch3
Start 15.000V
Stop -15.000V
Step -3.0000V
Constants:
VS -Ch1 .0000V

Fig. 18

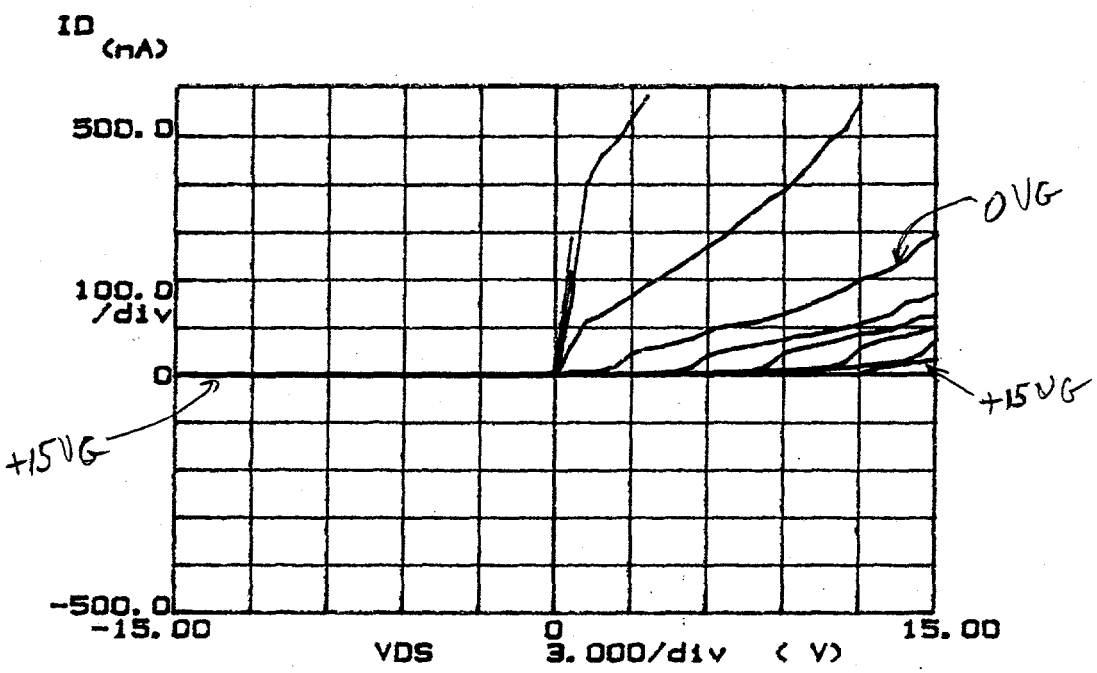

****** GRAPHICS PLOT ******
ID (nA)
500.0
100.0 /div
0
-500.0
-15.00
0
15.00
VDS
3.000/div (V)
0VG
+15VG
+15VG
Variable1:
VDS -Ch2
Linear sweep
Start -15.000V
Step 15.000V
Step .6000V
Variable2:
VG -Ch3
Start 15.000V
Step -15.000V
Step -3.0000V
Constants:
VS -Ch1 .0000V

Fig. 19

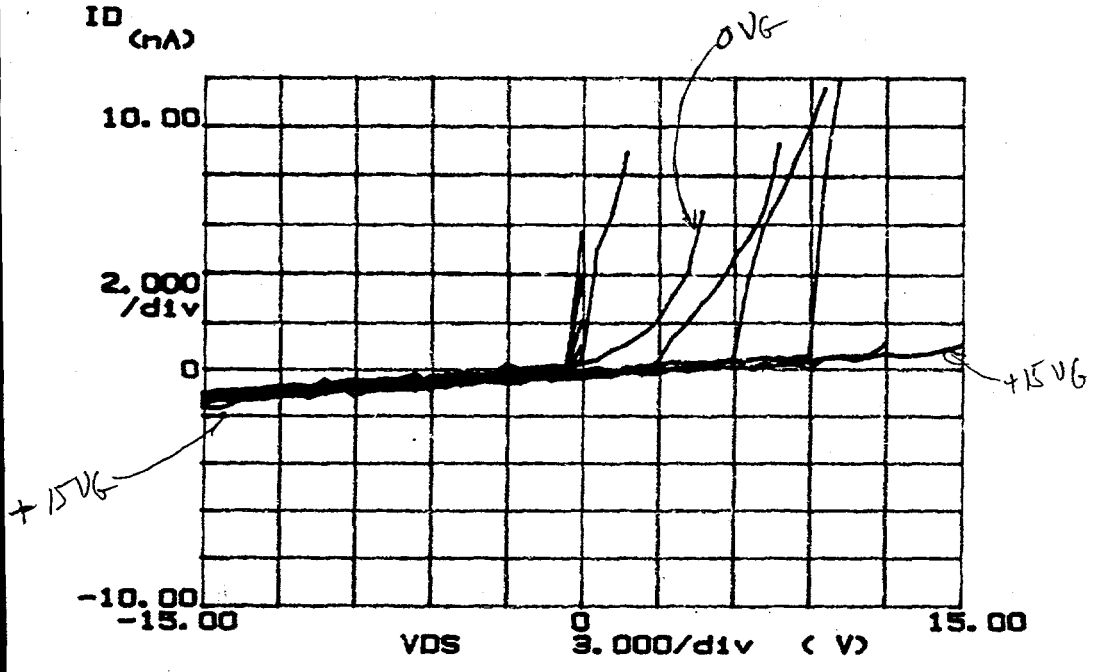

****** GRAPHICS PLOT ******
ID (nA)
10.00
2.000 /div
0
-10.00
-15.00
0
15.00
VDS
3.000/div (V)
0VG
+15VG
+15VG
Variable1:
VDS -Ch2
Linear sweep
Start -15.000V
Step 15.000V
Step .6000V
Variable2:
VG -Ch3
Start 15.000V
Step -15.000V
Step -3.0000V
Constants:
VS -Ch1 .0000V

Fig. 20

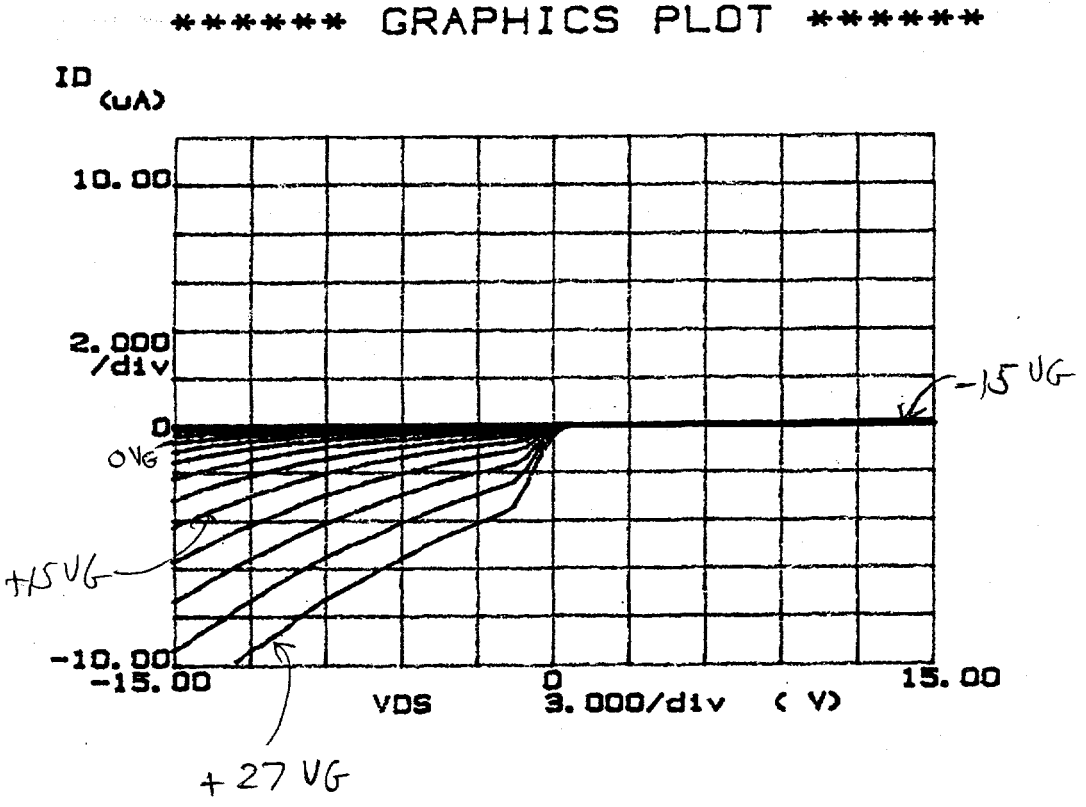

****** GRAPHICS PLOT ******
ID (uA)
10.00
2.000 /div
0
-10.00
-15.00
0
15.00
VDS
3.000/div (V)
-15 VG
0VG
+5VG
+27 VG
Variable1:
VDS -Ch2
Linear sweep
Start -15.000V
Stop 15.000V
Step .5000V
Variable2:
VG -Ch3
Start -15.000V
Stop 27.000V
Step 3.0000V
Constants:
VS -Ch1 .0000V

Fig. 21

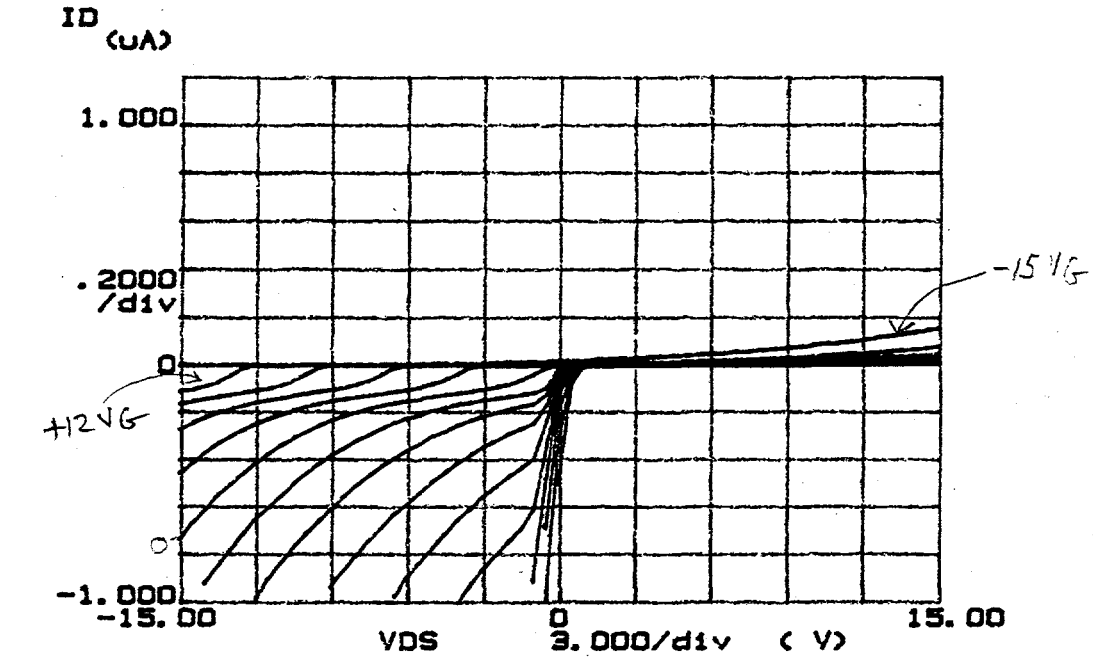

****** GRAPHICS PLOT ******
ID (uA)
1.000
.2000 /div
0
-1.000
-15.00
0
15.00
VDS
3.000/div (V)
-15 VG
+12VG
Variable1:
VDS -Ch2
Linear sweep
Start -15.000V
Stop 15.000V
Step .5000V
Variable2:
VG -Ch3
Start -15.000V
Stop 27.000V
Step 3.0000V
Constants:
VS -Ch1 .0000V

Fig. 22

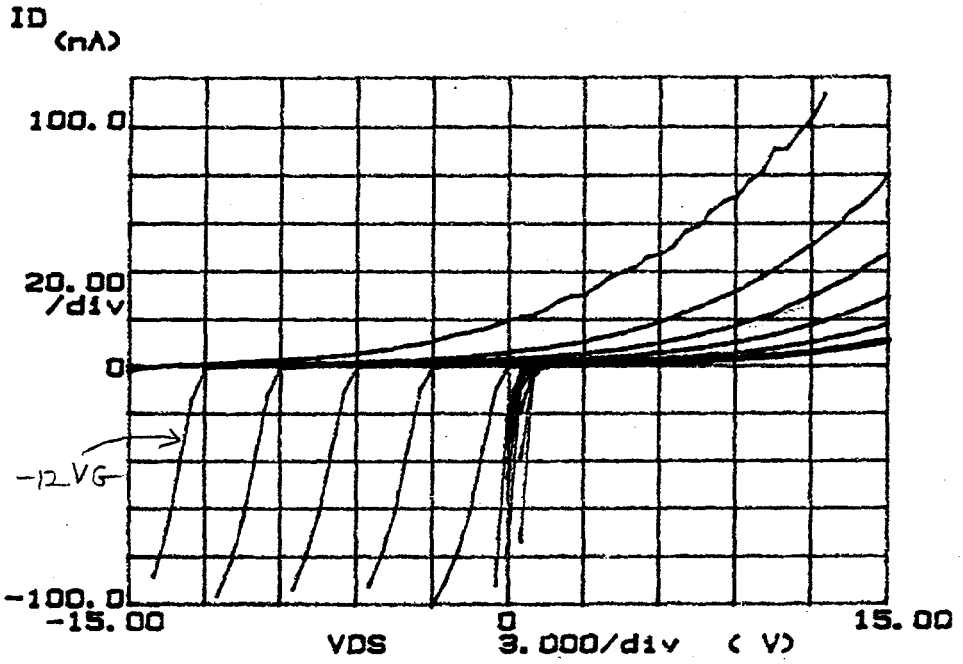

****** GRAPHICS PLOT ******
ID
(nA)
100.0
20.00
/div
0
-100.0
-12VG
-15.00
0
15.00
VDS
3.000/div
(V)
Variable1:
VDS -Ch2
Linear sweep
Start -15.000V
Step 15.000V
Step .5000V
Variable2:
VG -Ch3
Start -15.000V
Step 27.000V
Step 3.0000V
Constants:
VS -Ch1 .0000V

Fig. 23

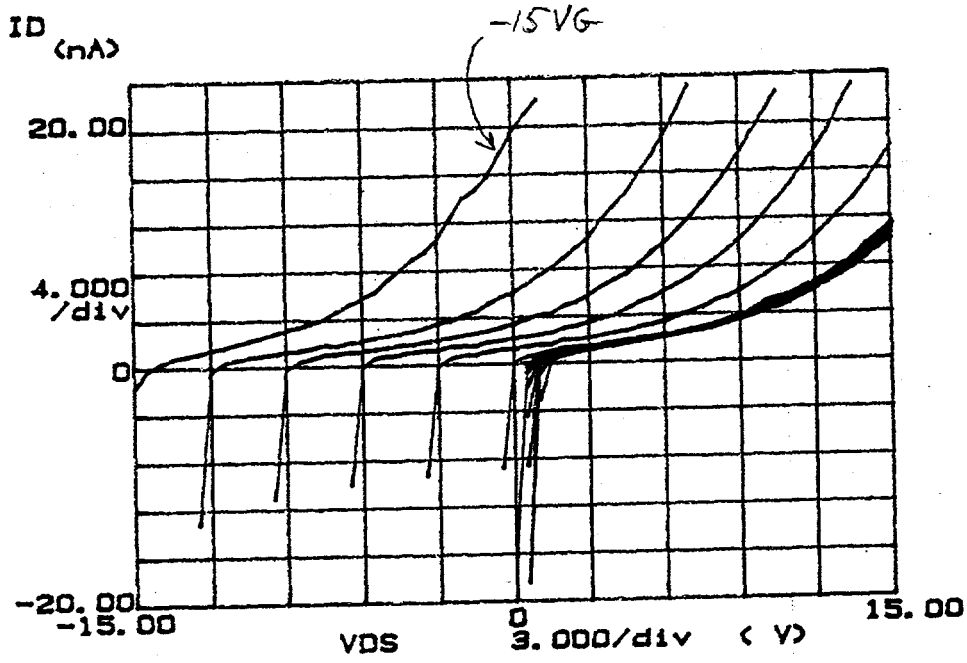

****** GRAPHICS PLOT ******
ID
(nA)
-15VG
20.00
4.000
/div
0
-20.00
-15.00
0
15.00
VDS
3.000/div
(V)
Variable1:
VDS -Ch2
Linear sweep
Start -15.000V
Step 15.000V
Step .5000V
Variable2:
VG -Ch3
Start -15.000V
Step 27.000V
Step 3.0000V
Constants:
VS -Ch1 .0000V

Fig. 24

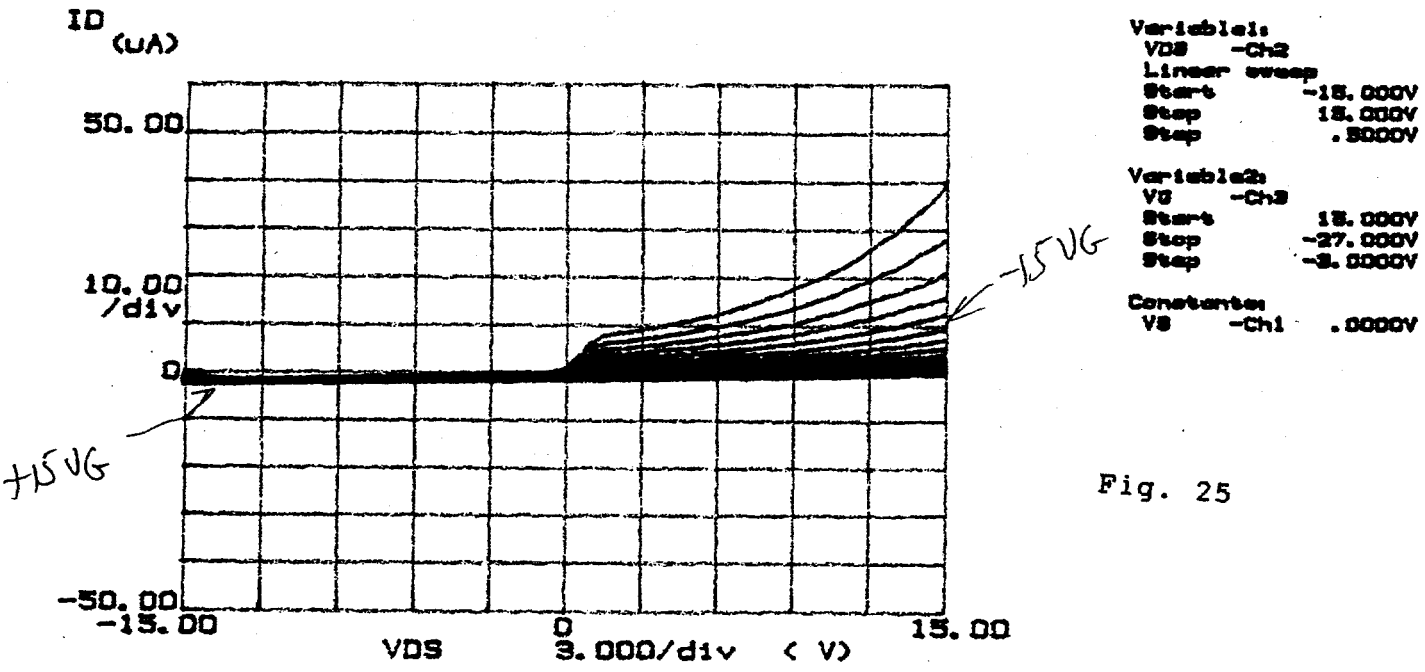

****** GRAPHICS PLOT ******
ID (uA)
50.00
10.00 /div
0
-50.00
-15.00
0
15.00
VDS 3.000/div (V)
-15VG
+15VG
Variable1:
VDS -Ch2
Linear sweep
Start -15.000V
Stop 15.000V
Step .5000V
Variable2:
VG -Ch3
Start 15.000V
Stop -27.000V
Step -3.0000V
Constants:
VB -Ch1 .0000V

Fig. 25

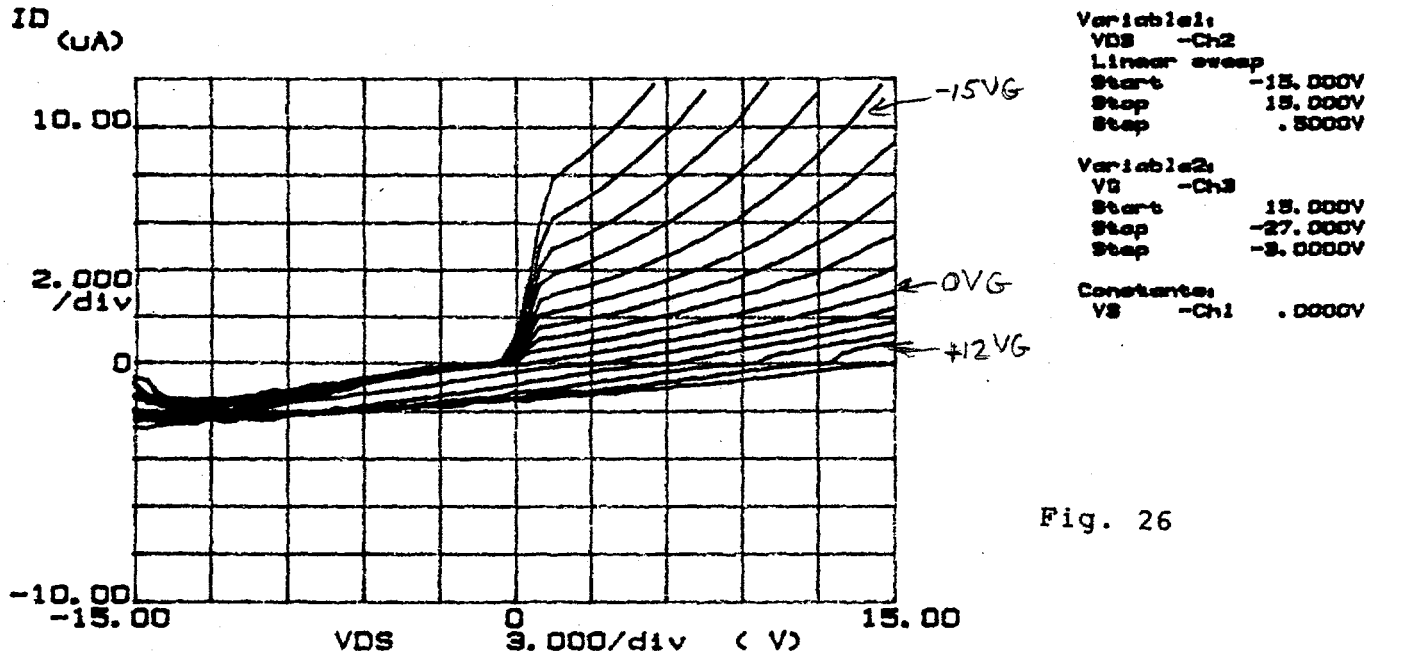

****** GRAPHICS PLOT ******
ID (uA)
10.00
2.000 /div
0
-10.00
-15.00
0
15.00
VDS 3.000/div (V)
-15VG
0VG
+12VG
Variable1:
VDS -Ch2
Linear sweep
Start -15.000V
Stop 15.000V
Step .5000V
Variable2:
VG -Ch3
Start 15.000V
Stop -27.000V
Step -3.0000V
Constants:
VB -Ch1 .0000V

Fig. 26

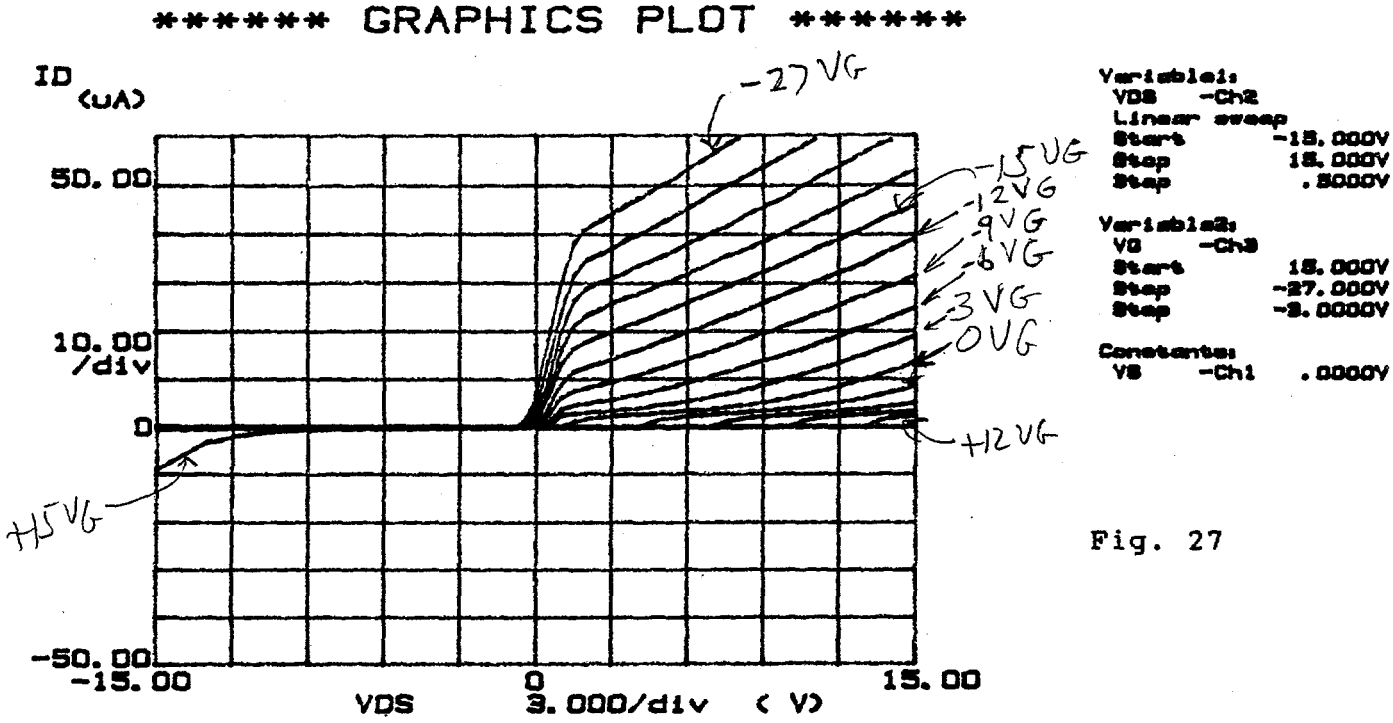

****** GRAPHICS PLOT ******
ID (uA)
50.00
10.00 /div
0
-50.00
-15.00
0
15.00
VDS 3.000/div (V)
-27VG
-15VG
-12VG
-9VG
-6VG
-3VG
0VG
+12VG
+15VG
Variable1:
VDS -Ch2
Linear sweep
Start -15.000V
Stop 15.000V
Step .5000V
Variable2:
VG -Ch3
Start 15.000V
Stop -27.000V
Step -3.0000V
Constants:
VB -Ch1 .0000V

Fig. 27

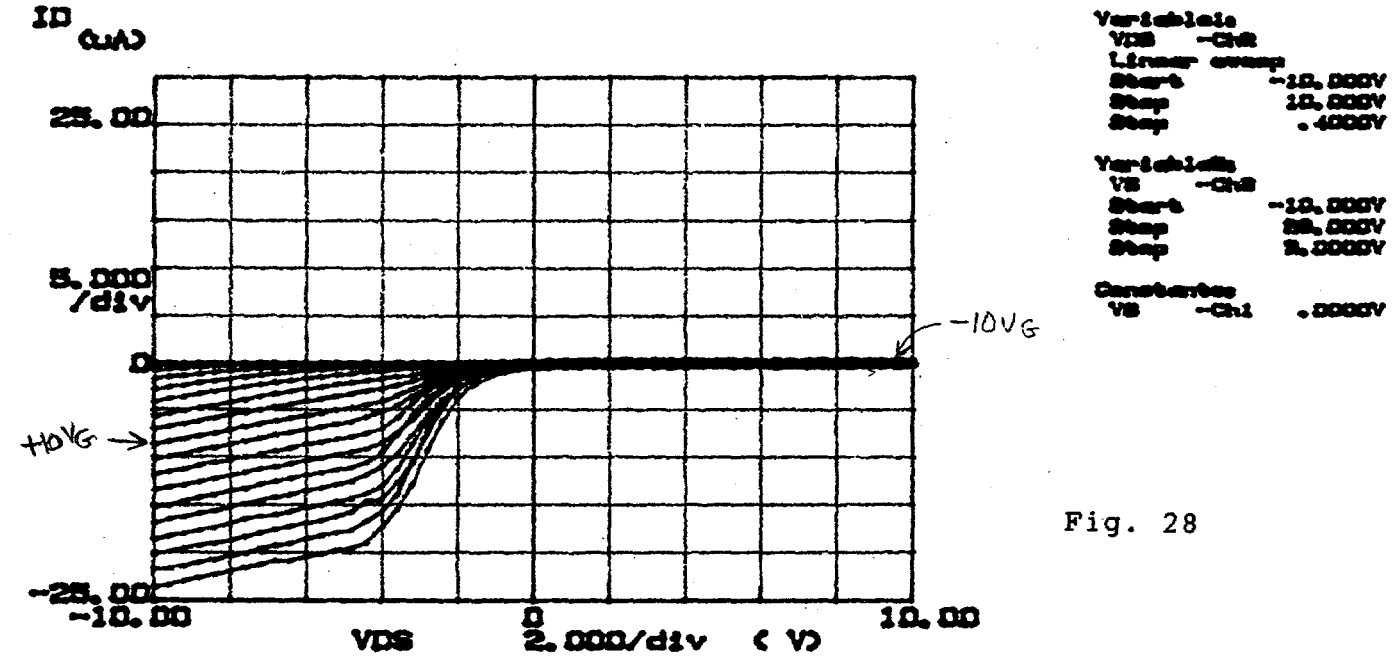

****** GRAPHICS PLOT ******
ID (uA)
25.00
5.000 /div
0
-25.00
-10.00
0
10.00
VDS 2.000/div (V)
-10VG
+10VG
Variable1:
VDS -Ch2
Linear sweep
Start -10.000V
Stop 10.000V
Step .4000V
Variable2:
VG -Ch3
Start -10.000V
Stop 25.000V
Step 5.0000V
Constants:
VB -Ch1 .0000V

Fig. 28

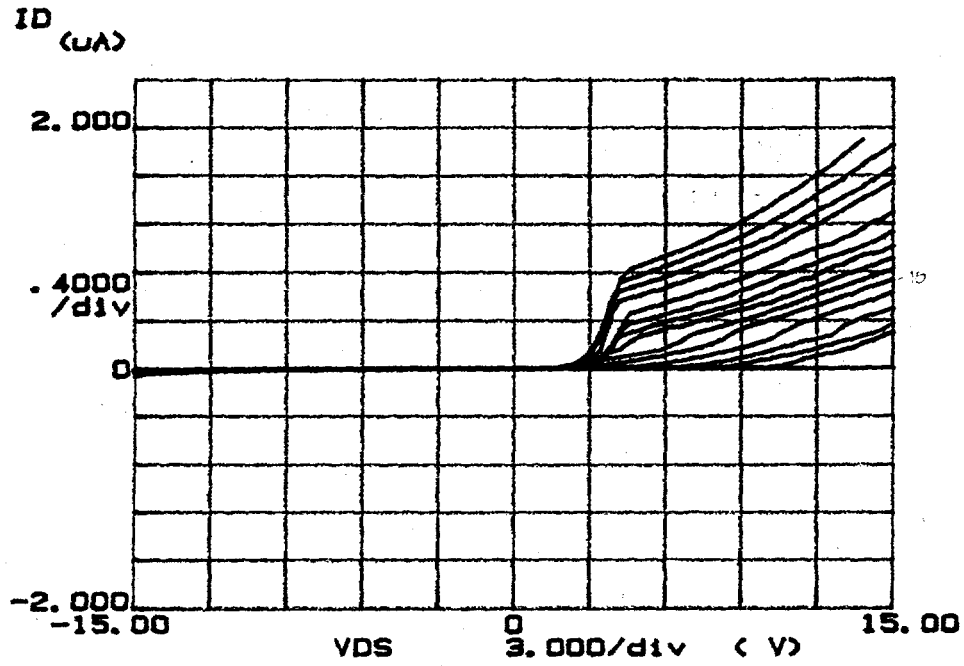

****** GRAPHICS PLOT ******
ID
(uA)
2.000
.4000
/div
0
-2.000
-15.00
0
15.00
VDS
3.000/div
(V)
Variable1:
VDS -Ch2
Linear sweep
Start -15.000V
Step 15.000V
Step .4000V
Variable2:
VG -Ch3
Start 10.000V
Step -25.000V
Step -2.0000V
Constants:
VS -Ch1 .0000V

Fig. 29

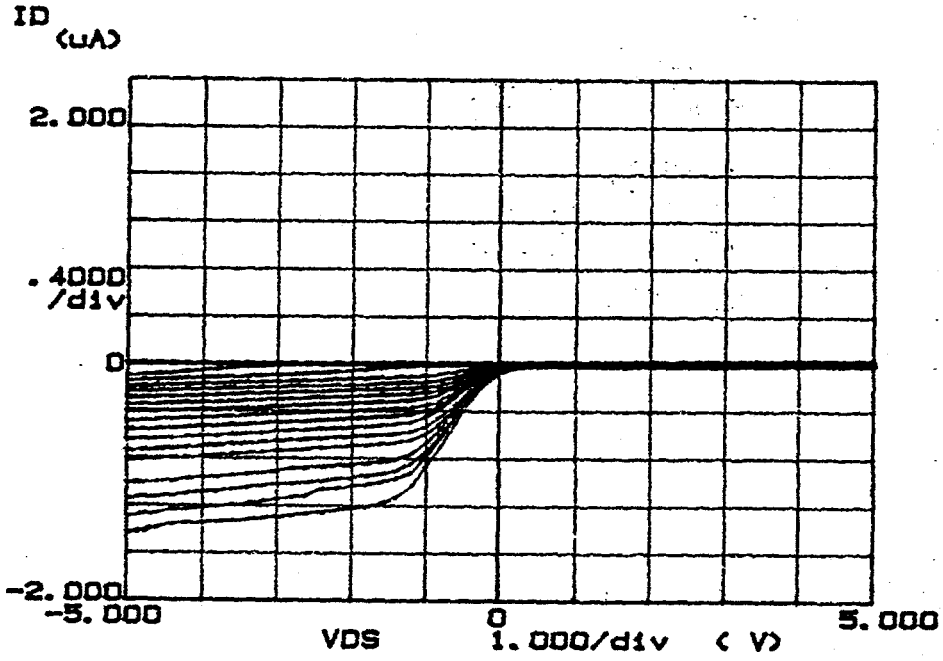

****** GRAPHICS PLOT ******
ID
(uA)
2.000
.4000
/div
0
-2.000
-5.000
0
5.000
VDS
1.000/div
(V)
Variable1:
VDS -Ch2
Linear sweep
Start -5.0000V
Step 5.0000V
Step .2000V
Variable2:
VG -Ch3
Start -10.000V
Step 25.000V
Step 2.0000V
Constants:
VS -Ch1 .0000V

Fig. 30

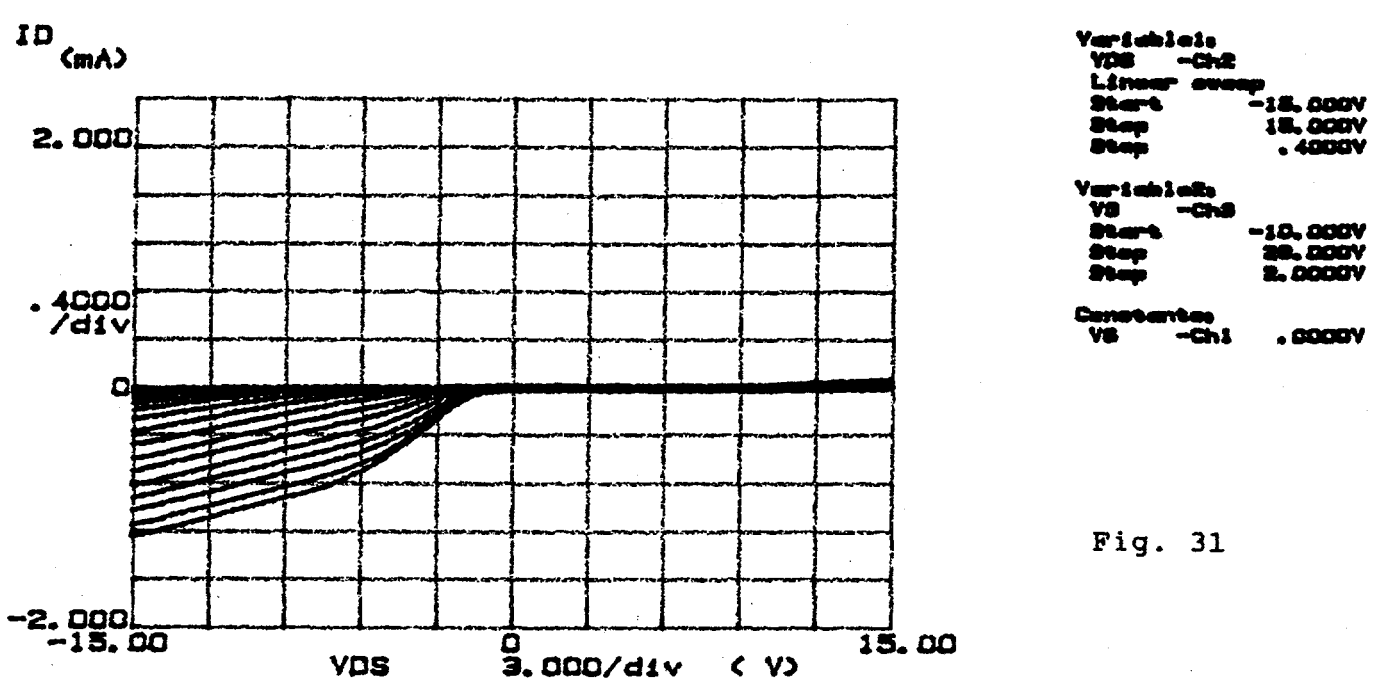

****** GRAPHICS PLOT ******
ID
(mA)
2.000
.4000
/div
0
-2.000
-15.00
0
15.00
VDS
3.000/div
(V)
Variable1:
VDS -Ch2
Linear sweep
Start -15.000V
Stop 15.000V
Step .4000V
Variable2:
VG -Ch3
Start -10.000V
Stop 20.000V
Step 2.0000V
Constants:
VG -Ch1 .0000V

Fig. 31

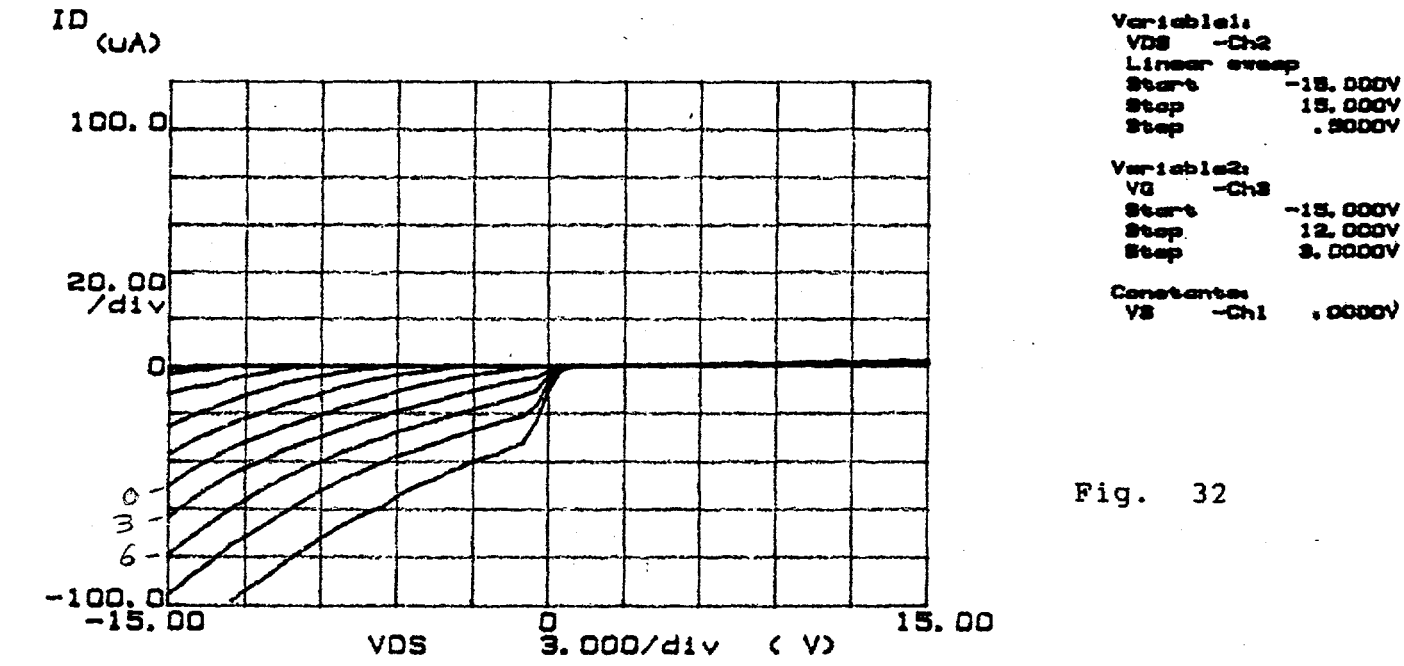
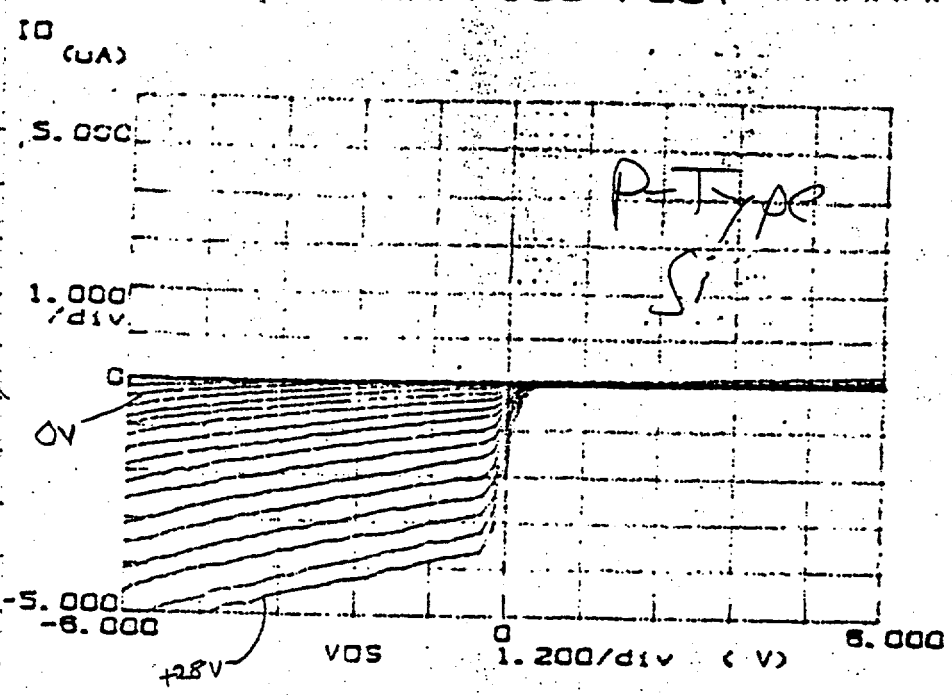

****** GRAPHICS PLOT ******
ID
(uA)
100.0
20.00
/div
0
0
3
6
-100.0
-15.00
0
15.00
VDS
3.000/div
(V)
Variable1:
VDS -Ch2
Linear sweep
Start -15.000V
Stop 15.000V
Step .3000V
Variable2:
VG -Ch3
Start -15.000V
Stop 12.000V
Step 3.0000V
Constants:
VG -Ch1 .0000V

Fig. 32



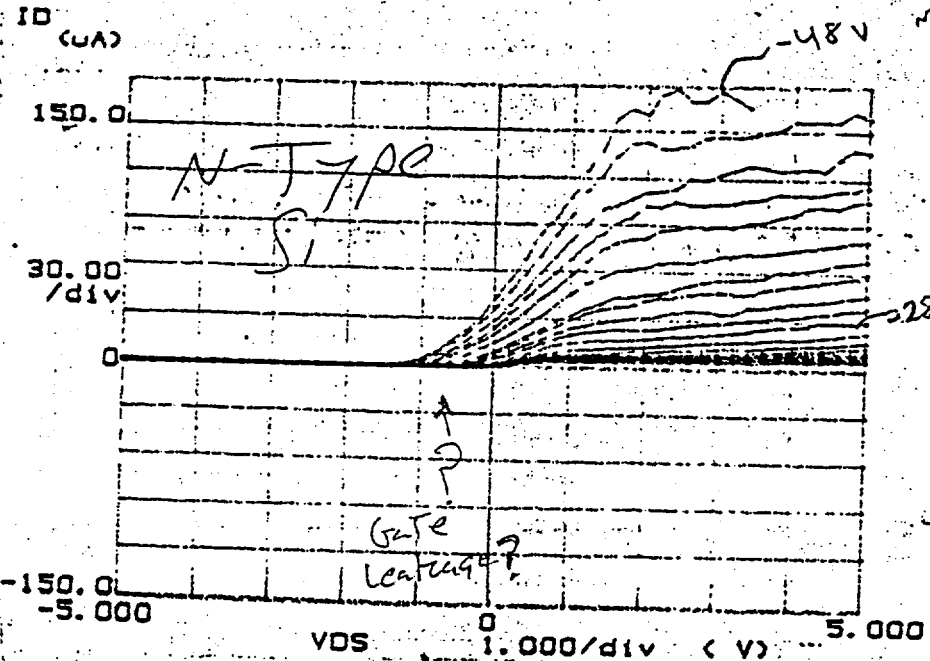
-4V threshold

P-Type
Original Substrate
Got April 27, 1994
Curves from
Why "0" volts off?
No Gate Metal

Fig. 33

Have Faulty Adapter on Source Lead

High VG Threshold

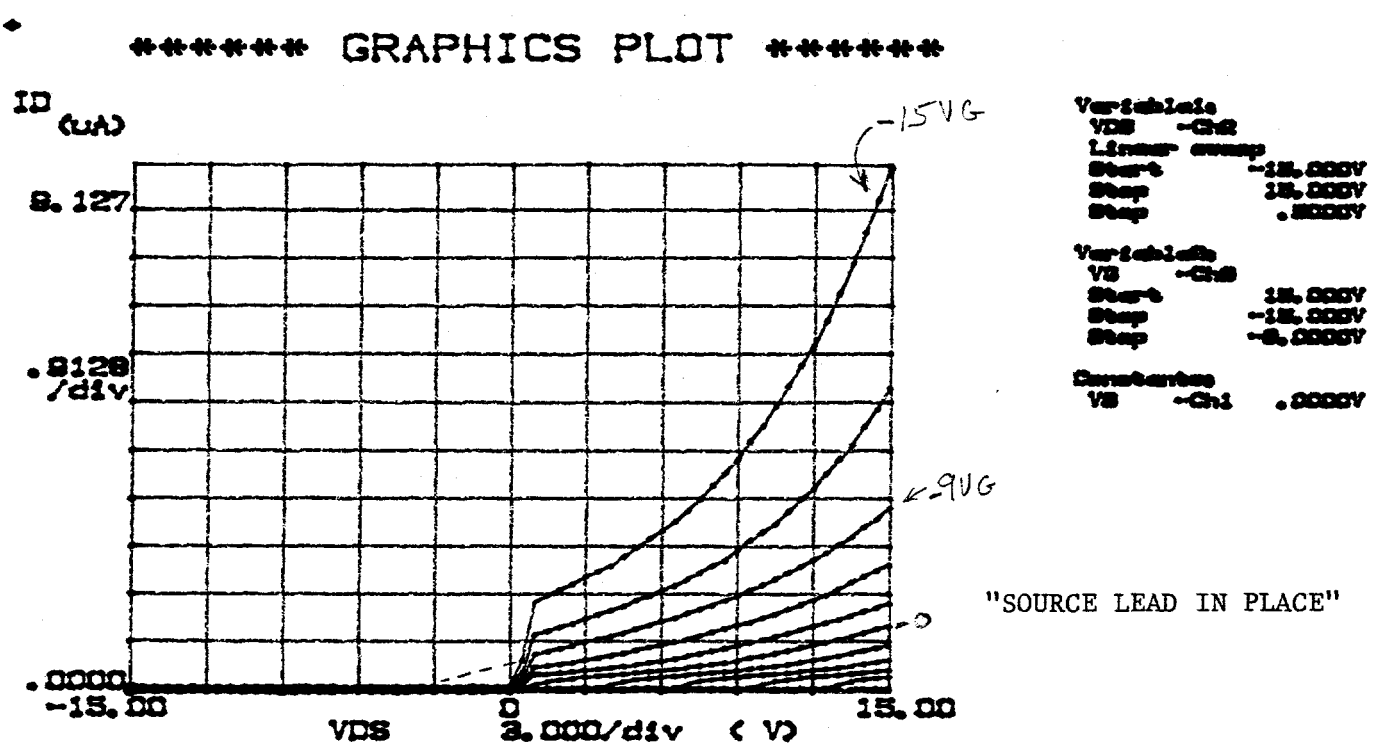


N-Type Si
2μm etch into Si

No Gate Metal

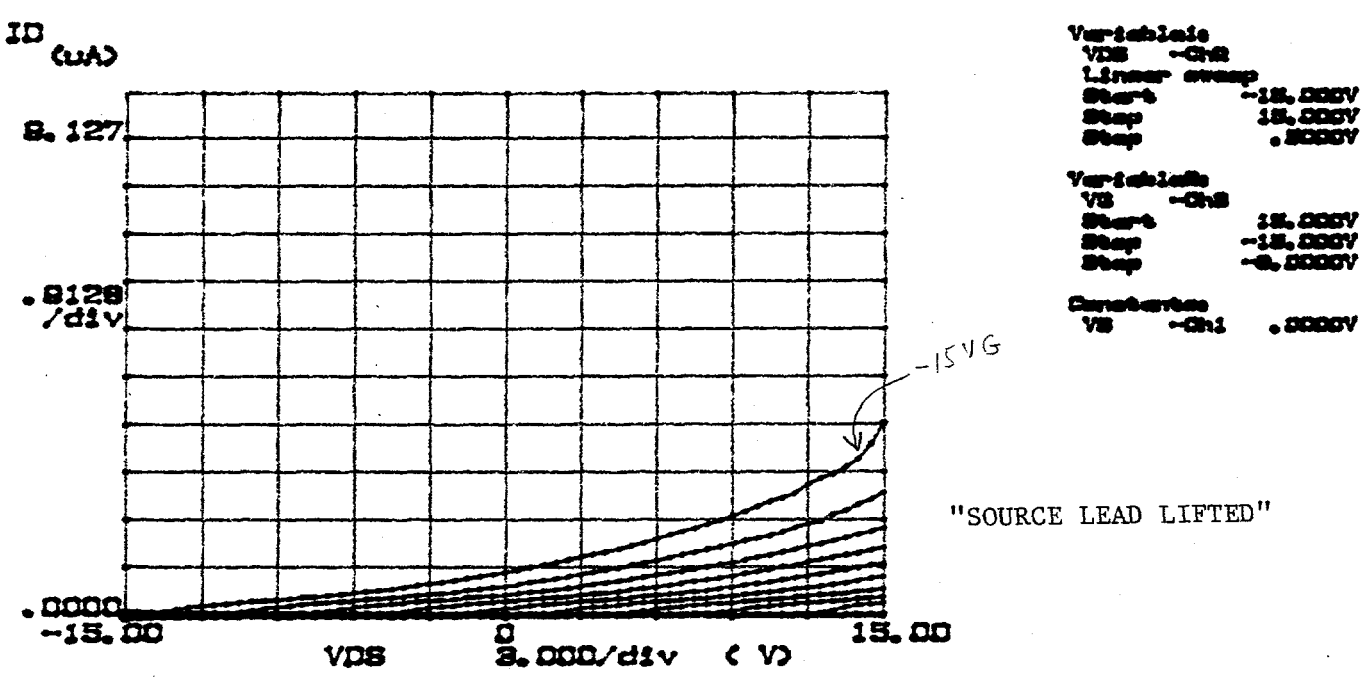
Fig. 34

Have Faulty Adapter on Source Lead



"SOURCE LEAD IN PLACE"

Fig. 35



"SOURCE LEAD LIFTED"

Fig. 36

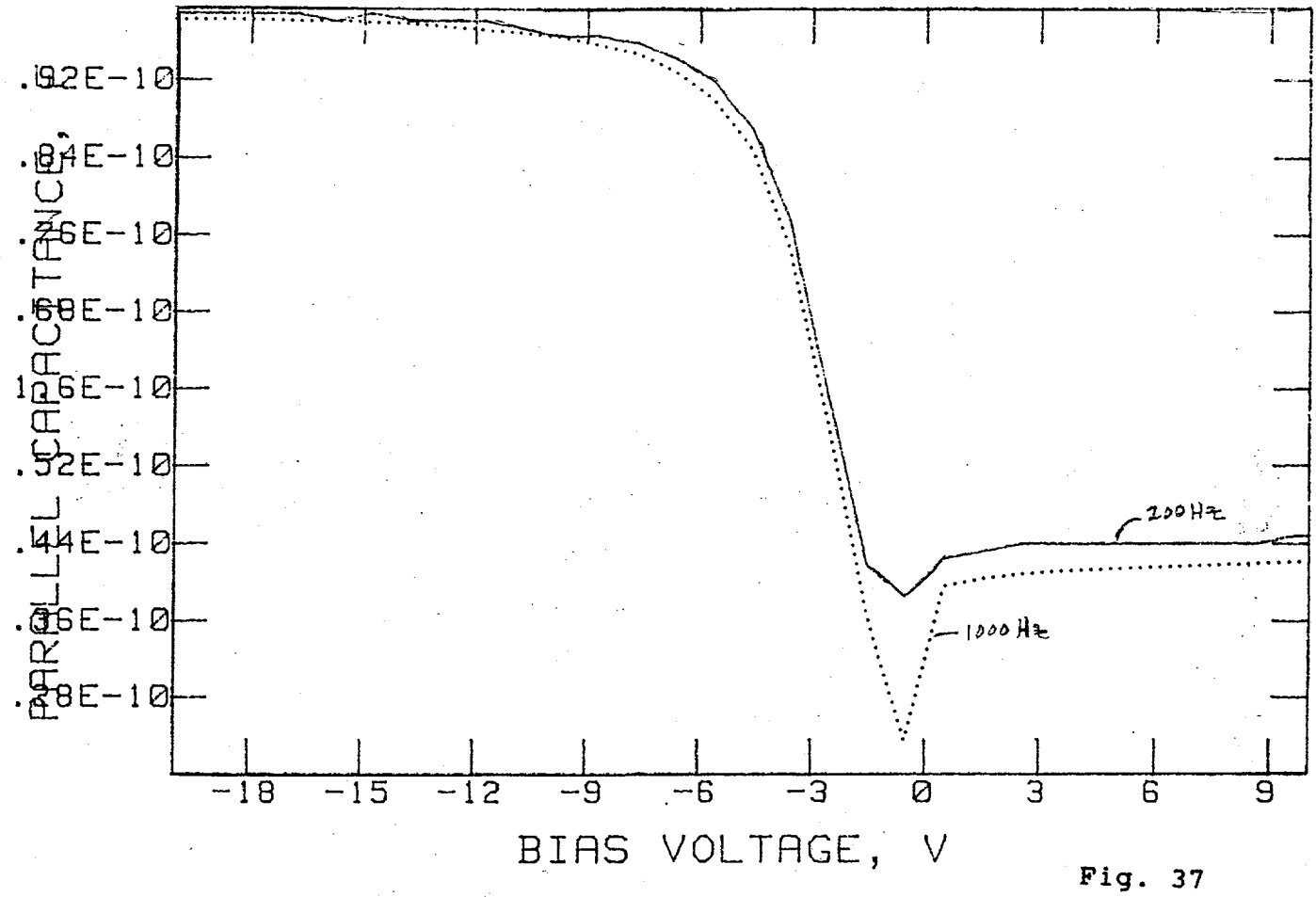

.92E-10
.84E-10
.76E-10
.68E-10
.6E-10
.52E-10
.44E-10
.36E-10
.28E-10
PARALLEL CAPACITANCE
200 Hz
1000 Hz
-18 -15 -12 -9 -6 -3 0 3 6 9
BIAS VOLTAGE, V

Fig. 37

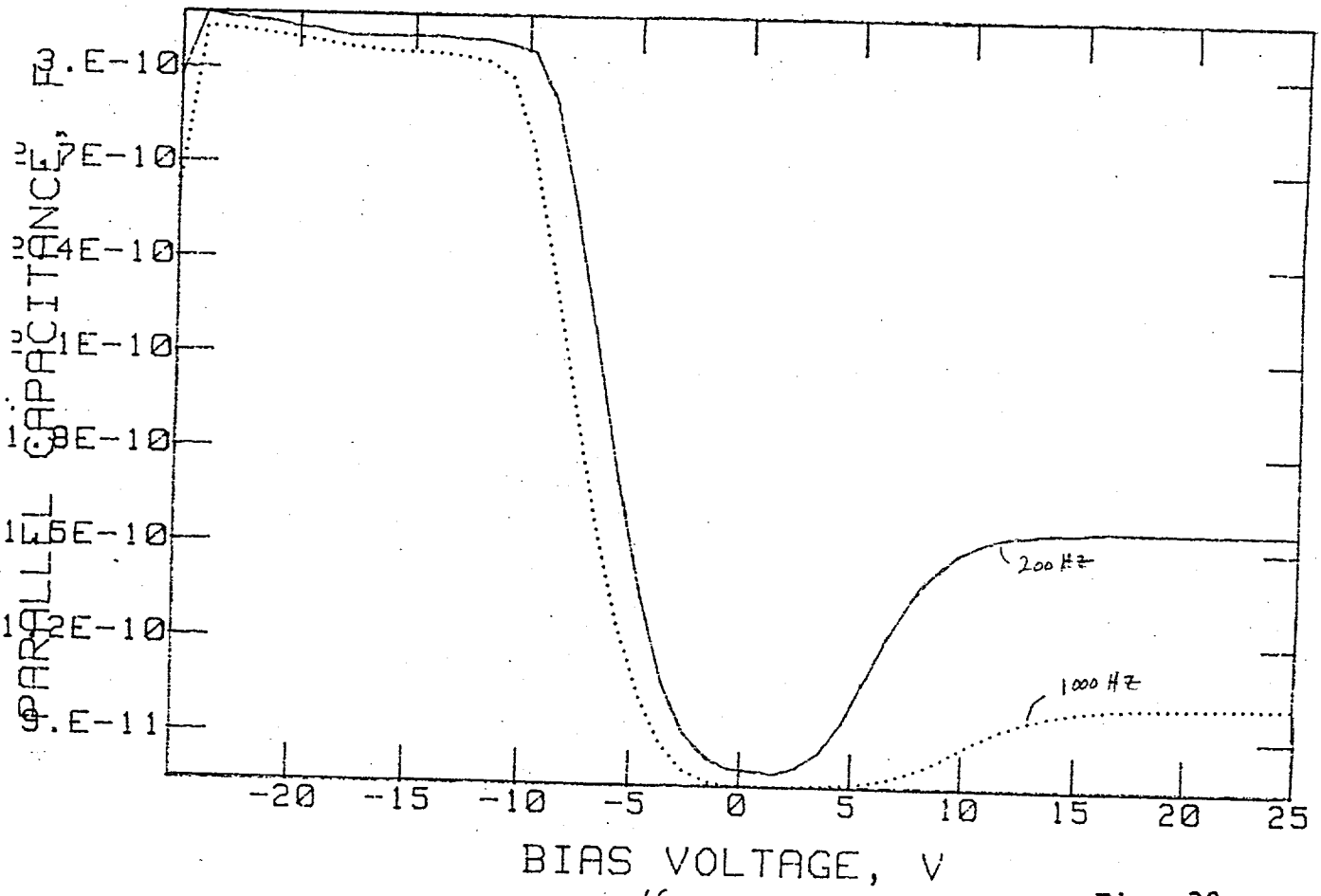

3.E-10
2.7E-10
2.4E-10
2.1E-10
1.8E-10
1.5E-10
1.2E-10
9.E-11
PARALLEL CAPACITANCE
200 Hz
1000 Hz
-20 -15 -10 -5 0 5 10 15 20 25
BIAS VOLTAGE, V

Fig. 38

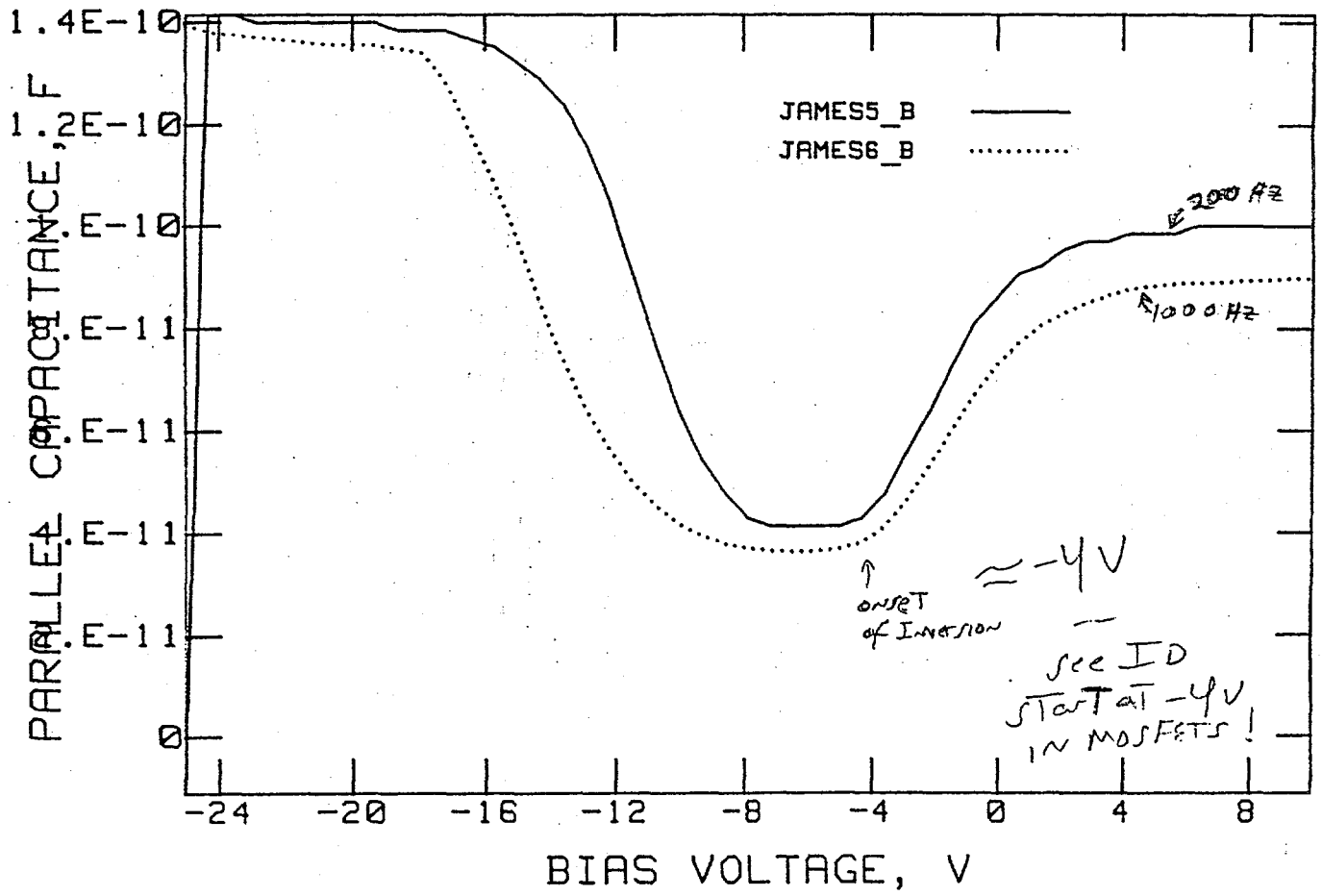

1.4E-10
1.2E-10
1.E-10
1.E-11
1.E-11
1.E-11
1.E-11
0
PARALLEL CAPACITANCE, F
JAMES5_B
JAMES6_B
200 Hz
1000 Hz
ONSET of INVERSION
≃-4V
See ID
START at -4V
IN MOSFETS!
-24
-20
-16
-12
-8
-4
0
4
8
BIAS VOLTAGE, V

Fig. 39

ADDITIONAL FABRICATION EFFORTS IN THE LAST FOUR MONTHS

In addition to producing the HISTORICAL ACCOUNTING and the ANALYSIS OF HOW FABRICATED DEVICES PROBABLY OPERATE Sections of this Final Report, in the last four months I have prepared and submitted an Office Action Response for the First Patent Application, Serial No. 08/250,906. This was sent to the Patent Office on March 27, 1995 in response to an Office Action Dated October 21, 1994. I had, until March 25, 1995 fully intended to abandon said First Patent Application and had advised the DOE Legal Department of that intention, (notice of my change of approach has been sent to the DOE Legal Department along with a copy of the submitted Office Action). The reason for this change in approach was that the Patent Examiner had found and cited Patents in his Office Action which describe Schottky barrier MOSFETS and their use in CMOS. However, in preparing the ANALYSIS OF HOW FABRICATED DEVICES PROBABLY OPERATE Section of this Final Report, (see infra), I became aware that the Chromium Disilicide MOSFET Devices fabricated under the DOE support seem to Operate with a different Gate and Drain Applied Voltage Polarity arrangement than do any other reported MOSFETS of which I am aware. I am attempting to base Patentability of the Chromium Disilicide Schottky barrier MOSFETS I, with the help of Professor Ianno, fabricated, on that Operational Voltage Polarity arrangement. I am including a copy of the Office Action response herewith to show what I am attempting to do.

ADDITIONAL DEVICE FABRICATION EFFORTS

Now, while we did undertake a lot of additional Device Fabrication efforts in the last four months, we were plagued with problems. First a flooded basement at the UNL EE Building prevented any fabrication work throughout the month of January. The Positive Pressure Ventilation System was out of order and we were not allowed to use any Fume Hoods, (hence do any acid etching), until it was back in order. As well, we have had one problem after another with the equipment. Vacuum leaks, in-situ heaters breaking etc. One series of problems involved a new Sputter System which was acquired by UNL, which we want to dedicate to Aluminum Deposition, so that Target, (material to be deposited), changing in the primary Sputtering System can be avoided, (changing targets is not an easy thing to do in said Primary Sputter System). The new Sputtering System worked fine the first time it was used, and then it developed problems, (Aluminum deposited thereby became black in color and did not adhere to the substrate well).

Even in view of the many problems we were able to produce a P-type substrate with N-Channel Schottky barrier MOSFETS thereon present, in which the Yield was almost one-hundred (100%)

percent. That is, nearly every device on the Substrate showed some degree of MOSFET Operation, though many devices had defects otherwise, (eg. relatively high leakage current etc.)

We also tried some new procedures in the area of depositing Chromium. Professor Ianno "Sputter Cleaned" the Silicon in the Source and Drain Regions prior to said Chromium Deposition. In some cases he also applied a Voltage Bias to the substrate during the Chromium Deposition. While some of the devices on the so-processed substrates provided excellent operating characteristics, many showed increased leakage current and a decreased junction reverse breakdown voltage level. We still think that the use of "Sputter Cleaning" is a viable approach however, and additional research into that is required. Use of the Bias is a bit more suspect. The Devices fabricated utilizing such seemed to have increased Gate leakage current. Such could be caused by a Applied Voltage induced Pin Holes caused by "Punch-through" of the Silicon Dioxide. I remember this was a concern, which we overcame, in the work I did years ago which utilized Ion Implantation around Chromium Masks atop of Silicon Dioxide.

I am including some print-outs of Drain Current vs. Drain to Source Voltage as a function of Gate Voltage Curves herein which were achieve from certain of the devices processed as described above. See Figs. FR 1 - FR 12. Note that I used the "Auto-Scale" function of the Curve Tracer, so only one major quadrant of Curves are present. However, it is to be noted that the other Quadrants were essentially without Drain Current flow. While not presented, it is to be noted that a majority of the devices which showed MOSFET action demonstrated leakage current as demonstrated in Fig. FR-10 through FR-12. (Note, Said Curves were obtained using a non-rigid thin wire probe. This approach, rather than use of rigid needle probes to access the Source and Drain Regions, leads to a lesser amount of leakage current being induced in other than the quadrant in which the curves appear).

Continuing, we were also able to fabricate a First Inverting Single Device Equivalent to CMOS on Intrinsic Silicon. The new Sputtering System was used to deposit the Aluminum in this effort and it worked fine. Although the devices did not operate, we did achieve the desired Structure, (eg. our photolithographic Masks are in order to allow fabrication although even in that category we had some initial problems).

It is of great interest to note that when I applied Voltage from the Drain to the Source, without any Gate Voltage applied, I saw Voltage appear at the "Midpoint" which was approximately a few Volts less than that applied to the Drain. Now, in the Noninverting Structure reported in the Sixth Quarterly Report, I did <u>not</u> see any Voltage appear at the "Midpoint" until a Gate Voltage was applied. I think this tells us that a Barrier forms

at the Chromium-Disilicide-Intrinsic Silicon Junction, which barrier blocks access of Voltage applied to the Chromium Disilicide side of said Barrier, but not Voltage applied to the Silicon Side thereof, to the Midpoint. This might be very significant. It is indeed the effect I hoped to see.

I think the reason said first run Inverting Single Device Equivalents to CMOS did not operate is, again, leaky Silicon Dioxide. Rather than seeing the "Midpoint" Voltage present, prior to application of Gate Voltage, reduce to zero (0.0) when a Gate Voltage was applied, I saw said "Midpoint" Voltage increase with applied Gate Voltage. (It was supposed to decrease to provide an Inverter action). This failure is probably because current is flowing through the Silicon Oxide. Additional fabrication efforts are definitely indicated and required and will be undertaken if the presently pending Grant Application to the DOE is awarded. Note, I have received notice from the NIST, (Dr. Bartholomew is the Chief Evaluator for the proposal), that my new proposal is now in Second Round Evaluation. That status was achieved after I had called Dr. Bartholomew and enquired as to how the evaluation was going. In that conversation he asked if I was preparing a Final DOE Report for the present Grant and I responded that I was. He asked that I send him a copy of it as it was, (eg. essentially the materials infra in this Report in a rougher state), and I immediately did. Shortly thereafter I received notice that my New Application was forwarded for Second Round evaluation.

I am including, in Fig. FR-0, an optical photo of the fabricated Inverting Single Device equivalent to CMOS herein, (Note, I've marked thereon an electrical interconnection between the identified Effective Gates associated with the Source and Drain, which interconnection I effect with probes). Also, present is an optical photo of the NonInverting Single Device Equivalent to CMOS which was fabricated earlier, and which provided promising experimental operational results. I also refer the reader to the accompanying SBIR Grant proposal which is pending before the Air Force for a more in-depth explanation of said Single Device Equivalents to CMOS Devices. (Note, the Grant proposal presently before the NIST is meant to support the same work as described therein).

CMOS WITH EXISTING N AND P-CHANNEL SCHOTTKY BARRIER MOSFETS

Finally, even though we have not progressed to the stage where fabrication of N and P-Channel MOSFETS on a Single Substrate in a CMOS configuration is feasible, I did configure working N and P-Channel MOSFETS form Separate Substrates into a CMOS circuit. (Probing two MOSFETS simultaneously, I might mention, is not easy with our Probe Stand arrangement!). I did achieve inverting CMOS Switching action from said configured

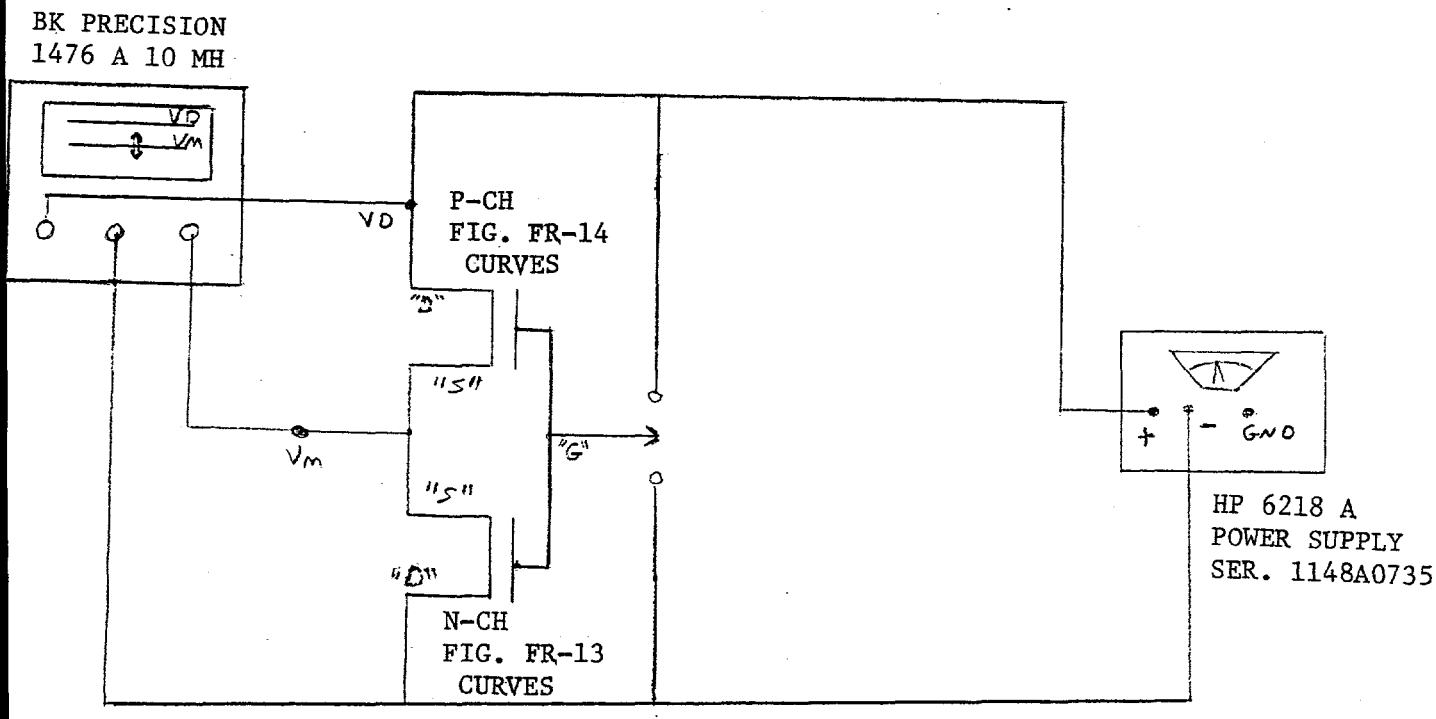
circuit. The results of said experiment were as follows:

First, I probed a number of Devices on both N and P-type Silicon. After a few hours of searching I choose devices which provided Drain Current vs. Drain to Source Voltage curves as shown in Figs. FR-13 and FR-14 for N-Channel and P-Channel. It is noted that the devices were not particularly well balanced as regards Gate induced Conduction Drain Currents, but both devices did demonstrate low curent flow where the Gate Voltage Polarity was opposite to that which causes Drain Current to flow in a MOSFET Mode, (ie. Positive Gate Voltage in N-Channel Devices formed on P-type Silicon effects Drain Current Flow, and Negative Gate Voltage for P-Channel Devices formed on N-type Silicon effects Drain Current Flow, but Positive Gate Voltage in P-Channel Devices and Negative Gate Voltage in N-Channel Devices did not cause significant Drain Current Flow). I would have liked to used Devices, Drain Current Curves from which are shown in Figs. FR-13 (N-CH), and Figs. FR-4, 5 & 6, (P-CH), but I ran into a problem probing the device indicated by Figs. FR-4, 5 & 6. I found that to probe two devices at once I had to use rigid needles in the probers. I could not use the non-rigid thin wires I used to probe the Devices when I obtained the Curves shown in Figs. FR-13, 14, 4, 5, & 6 as so many said wires were present in so small an area they constantly would short together. I could not control so many non-rigid thin wire to Source, Drain and Gate locations at once. I was, with a lot of effort to so control rigid needles contact to the multiple Source, Drain and Gate regions, however. Continuing, I could not get the devices represented in Figs. FR-4, 5 & 6 to operate when probed with rigid needles. (Note that Fig. FR-13b shows Drain Curent Curves obtained when probing a Device with rigid needles, as compared to a Device probed with non-rigid thin wires, as represented in Fig. FR-13, provides very different Drain Curent Curves).

Continuing, I probed the Gates of the P and N-Channel Devices with a common probe to which I affixed two Probe Needles. I next interconnected the "Effective Sources" of the N and P-Channel Devices represented by the Curves shown in Figs FR-13 and FR-14, to configure a Midpoint, then I applied a Positive voltage to the "Effective Drain" of the P-Channel Device, with respect to zero Volts applied to the "Effective Drain" of the N-Channel Device. I simultaneously monitored the applied Positive Voltage at the "Effective Drain" of the P-Channel Device and the Voltage at the interconnected "Effective Sources" of the N and P-Channel Devices, with respect to the "Effective Drain of the N-Channel Device, using my dual channel Oscilloscope. With Positive Twenty (20) Volts so applied, I saw approximately fifteen (15) Volts appear at said interconnected "Effective Sources" Midpoint. I then applied the Positive Twenty (20) volts to the Common Gates, and saw the Voltage at the interconnected "Effective Sources" drop by approximately three (3) Volts. I then connected the Common Gates to Zero (0.0) volts to the and

saw the Voltage at the interconnected "Effective Sources" rise by approximately three (3) Volts. That is, I witnessed an "Inversion" effect. Granted, it was not a very good "Switch", but the direction of the Voltage change with respect to applied Gate Voltage was proper for a CMOS arrangement.

From the above described experiment results I conclude that I did witness a CMOS Inverter Switching Action. However, I express extreme caution as I make that statement. It was extremely difficult to simultaneously probe two MOSFET Devices, and I had to use rigid needles to probe the Source and Drain at all. As explained above, probing Source and Drain Regions of the Schottky Barrier MOSFETS with rigid needles changes the Drain Current vs. Drain to Source Voltage as a function of Gate Voltage Curves over those obtained when probing with non-rigid thin wires. Said effect, and any number of other things could have occured, which I have no way to know. However, I do think that the fact that I observed an Inversion effect, indicates the CMOS circuit I configured was demonstrating CMOS Inverter Action. If the situation was otherwise, I think I would have seen an increase in Midpoint Voltage with applied Gate Voltage. That is, the Midpoint Voltage would have followed the Polarity of the Applied Gate Voltage. The result I observed is encouraging, but a lot remains to be done.

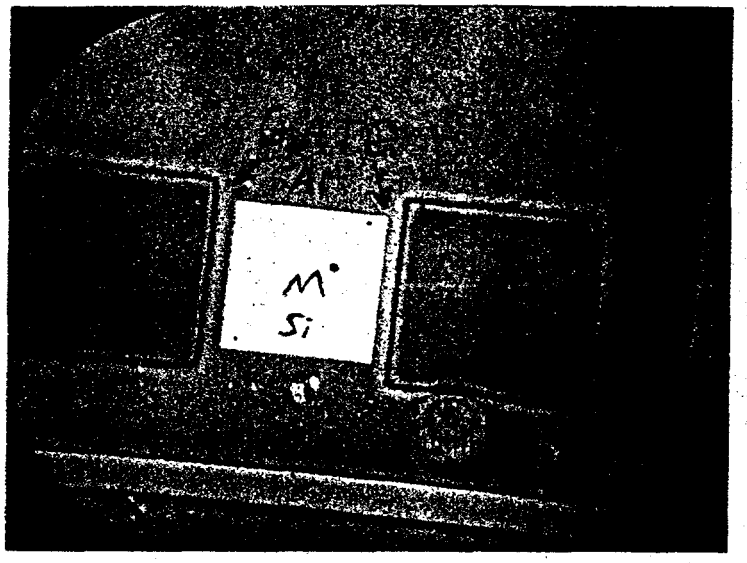


CMOS TEST SET-UP

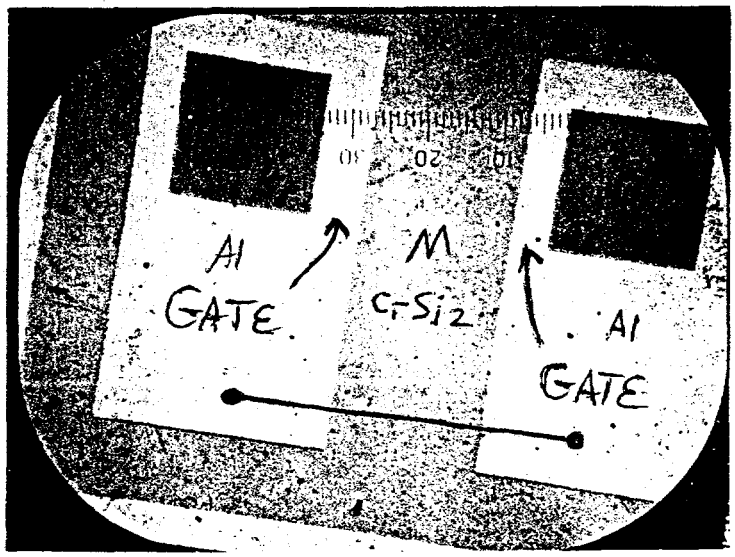
In conclusion, at the present stage of development we can not show Consistency and Repeatability in our fabricated Devices. Until we can do so it is premature to attempt to fabricate CMOS on a single substrate. However, we have shown the Feasibility of fabricating MOSFETS utilizing Chromium-Disilicide as Source and Drain, I've proposed an explanation as to why said Devices work as they do, and I've prepared and submitted Two Patent Applications focusing on the results achieved.

Also, it is appropriate to mention that Professor Ianno is continuing to do investigation of the efficiency of the various steps of the Fabrication Processs to see if we can determine where we are experiencing yield loss. He has a student helping. Proposed efforts include use of a very sensitive Profilometer called an Atomic microscope to investigate the Silicon Dioxide etching efficiency. We are also discussing how to best avoid contamination effects. One primary source of contamination may be the Asher system we use to remove Photoresist. We might use liquid organic Photoresist removal as an alternative to see if it improves our results.

Finally, I have informed the DOE Legal Office that I will pursue U.S. Patent Rights, but can not afford to pursue Foreign Patents. I recently submitted Applications to the European Patent Office (EPO) and to Japan for a Client. Each required in excess of $10,000.00 to simply gain entry. I personally simply can't afford that.



OPTICAL PHOTO OF FABRICATED NONINVERTING CMOS EQUIVALENT

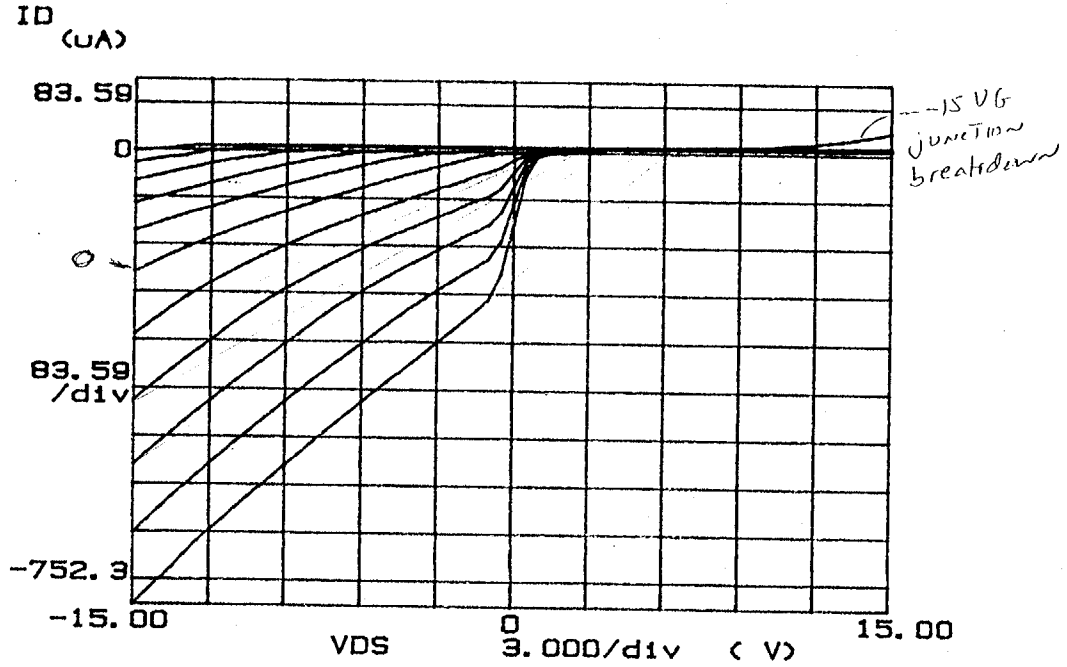


OPTICAL PHOTO OF FABRICATED INVERTING CMOS EQUIVALENT

Fig. FR-0

sputter clean
no bias

****** GRAPHICS PLOT ******



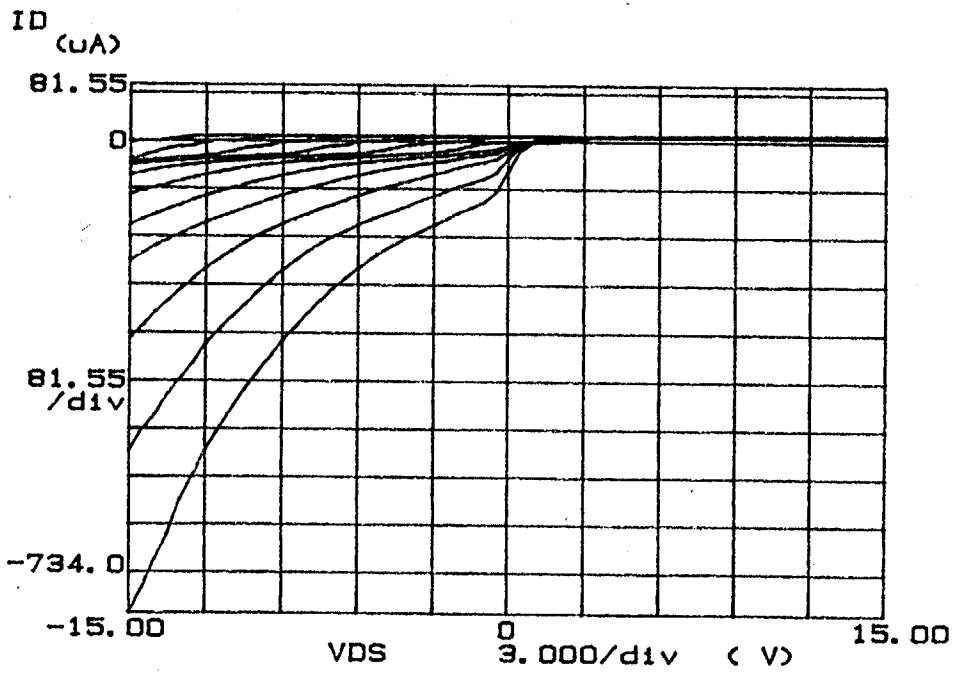
Variable1:
VDS -Ch2
Linear sweep
Start -15.000V
Stop 15.000V
Step .5000V

Variable2:
VG -Ch3
Start -15.000V
Stop 15.000V
Step 3.0000V

Constants:
VS -Ch1 .0000V

Fig. FR-1

sputter clean
no bias

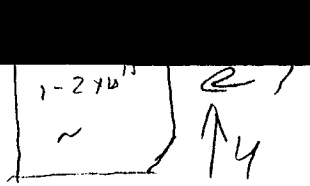


Variable1:
VDS -Ch2
Linear sweep
Start -15.000V
Stop 15.000V
Step .5000V

Variable2:
VG -Ch3
Start -15.000V
Stop 15.000V
Step 3.0000V

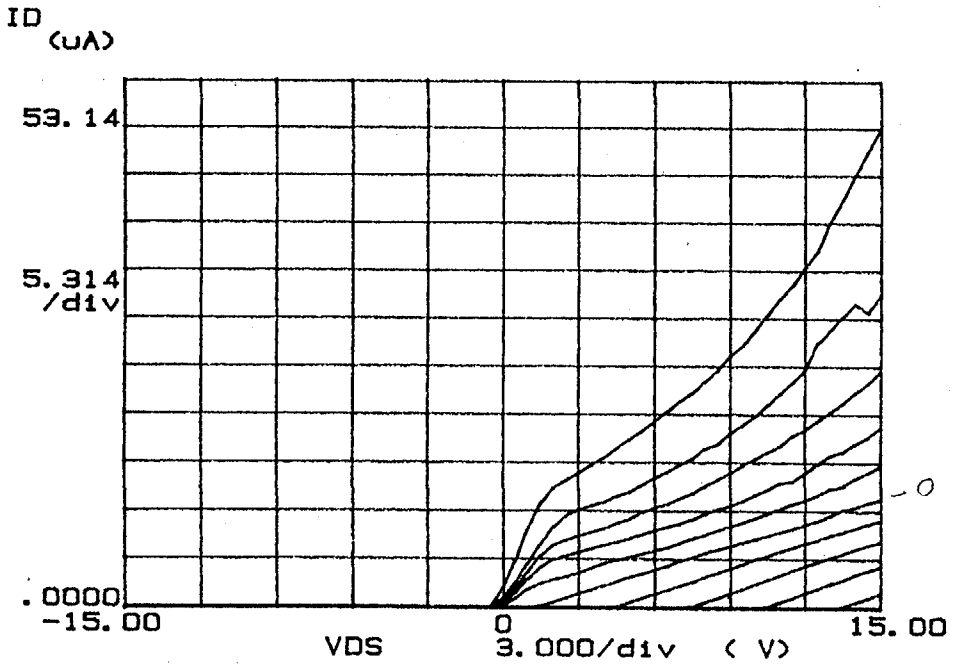
Constants:
VS -Ch1 .0000V

Fig. FR-2



sputter clean
no bias

****** GRAPHICS PLOT ******



Variable1:
VDS -Ch2
Linear sweep
Start -15.000V
Stop 15.000V
Step .5000V

Variable2:
VG -Ch3
Start 15.000V
Stop -15.000V
Step -3.0000V

Constants:
VS -Ch1 .0000V

Fig. FR-3

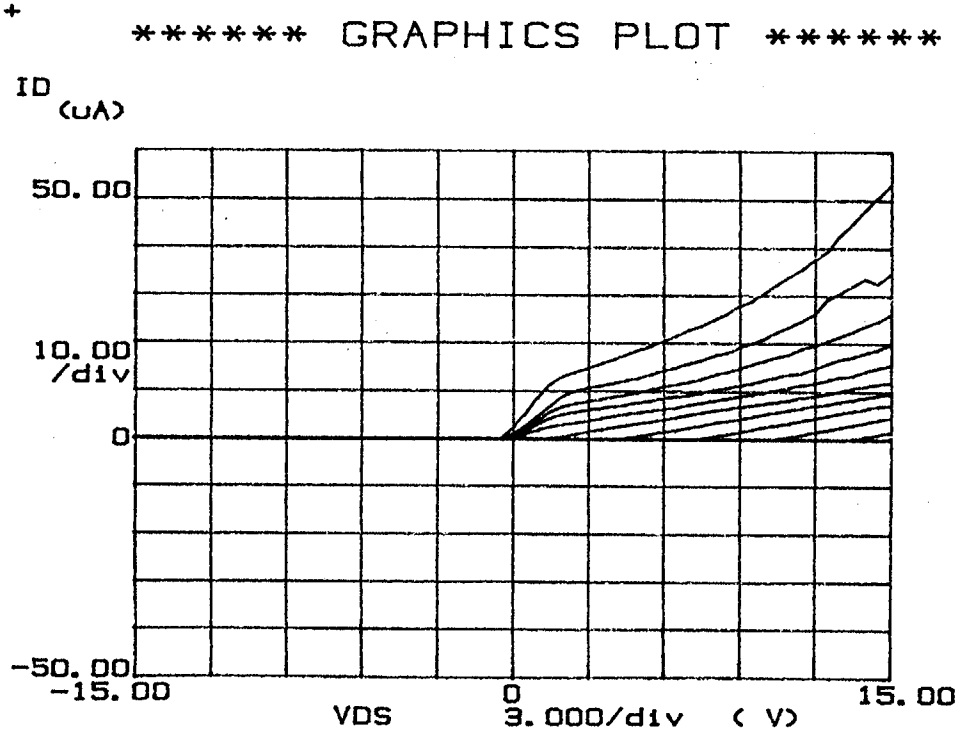
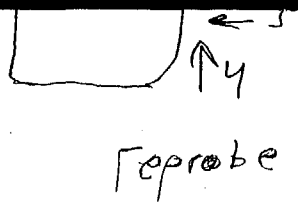
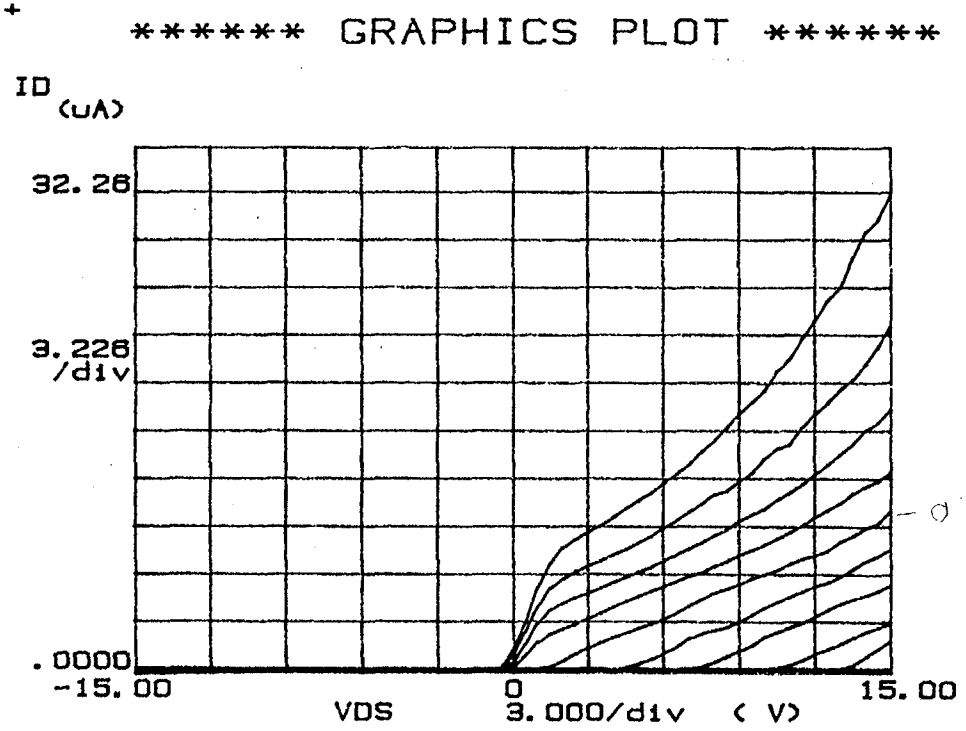

****** GRAPHICS PLOT ******
ID
(uA)
50.00
10.00
/div
0
-50.00
-15.00
0
15.00
VDS
3.000/div
(V)
Variable1:
VDS -Ch2
Linear sweep
Start -15.000V
Stop 15.000V
Step .5000V
Variable2:
VG -Ch3
Start 15.000V
Stop -15.000V
Step -3.0000V
Constants:
VS -Ch1 .0000V

Fig. FR-4





Variable1:
VDS -Ch2
Linear sweep
Start -15.000V
Stop 15.000V
Step .5000V

Variable2:
VG -Ch3
Start 15.000V
Stop -12.000V ← NIT 15
Step -3.0000V

Constants:
VS -Ch1 .0000V

Fig. FR-5

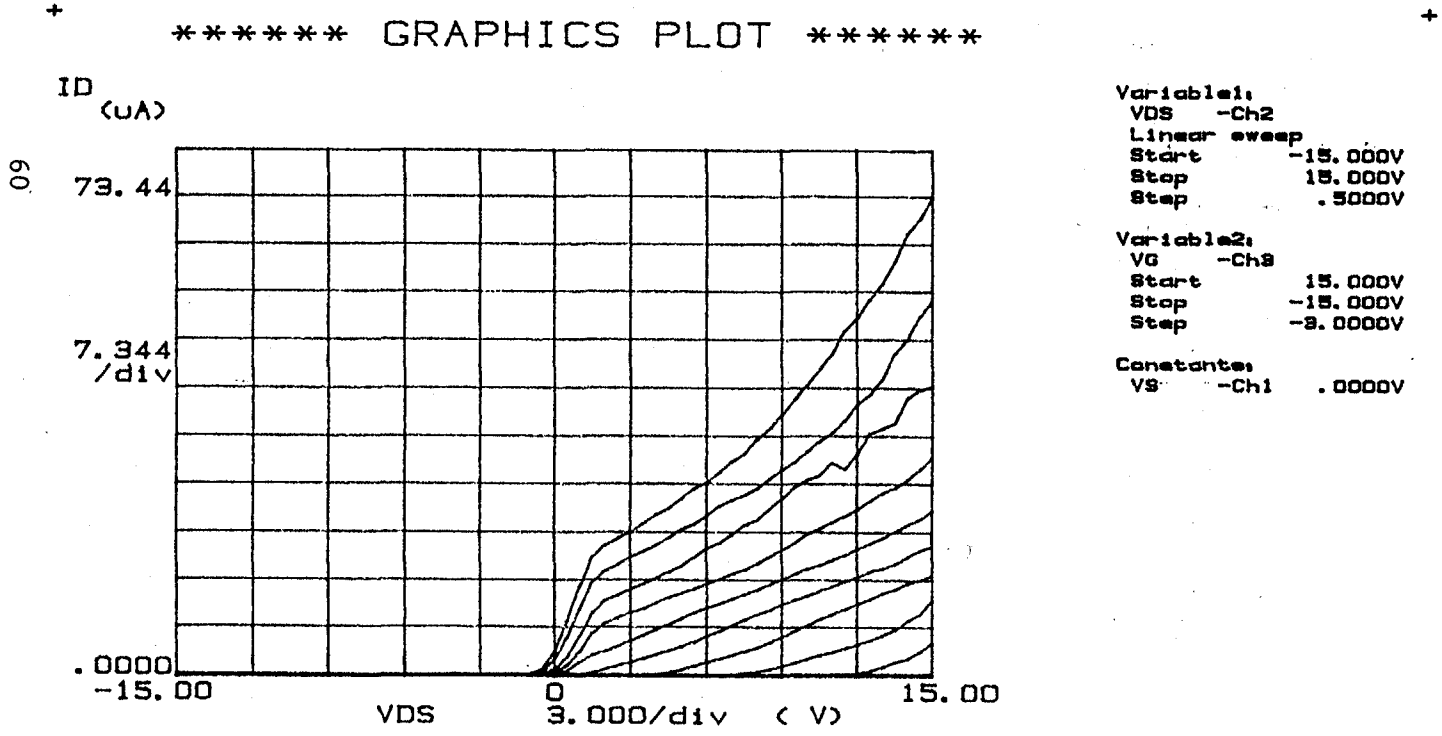
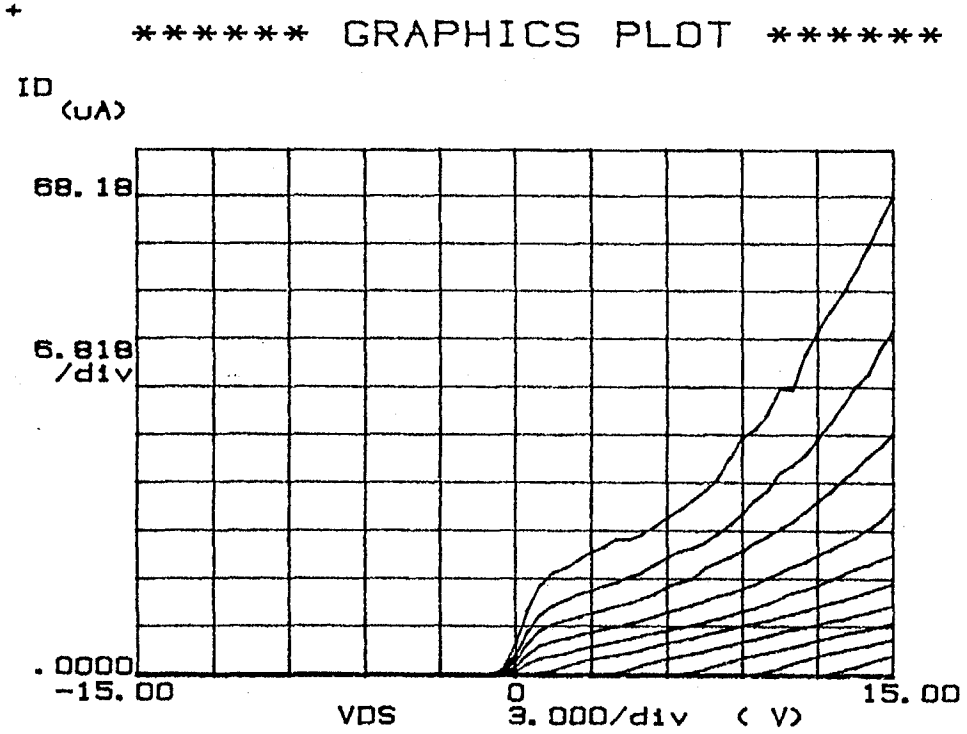

****** GRAPHICS PLOT ******
ID
(uA)
73.44
7.344
/div
.0000
-15.00
0
15.00
VDS
3.000/div
(V)
Variable1:
VDS -Ch2
Linear sweep
Start -15.000V
Stop 15.000V
Step .5000V
Variable2:
VG -Ch3
Start 15.000V
Stop -15.000V
Step -3.0000V
Constante:
VS -Ch1 .0000V

Fig. FR-6

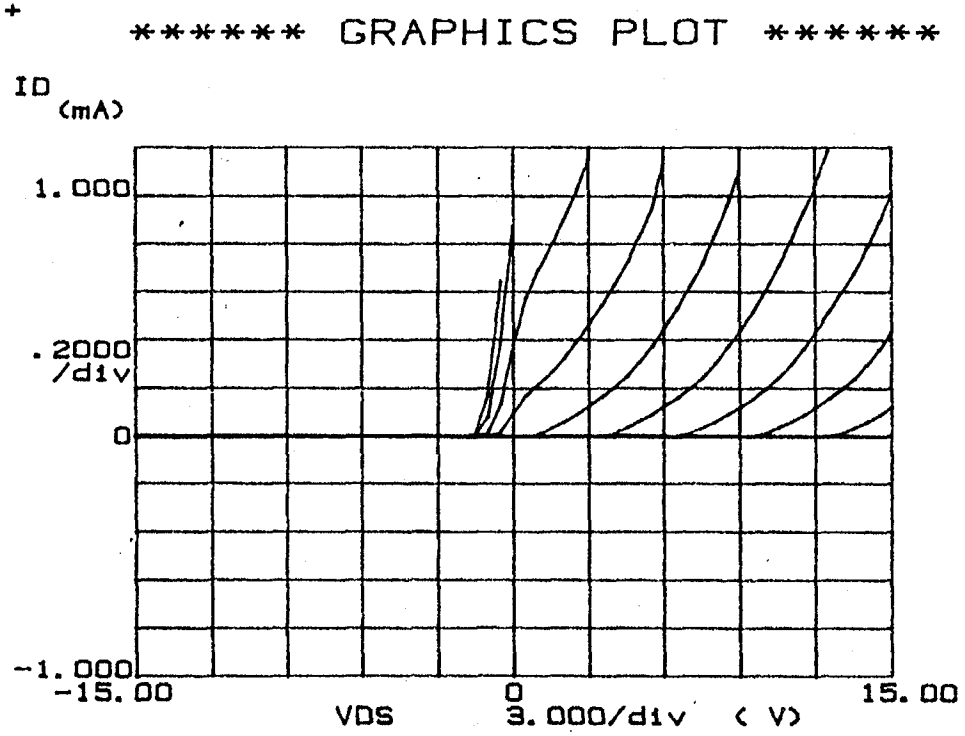


Variable1:
VDS -Ch2
Linear sweep
Start -15.000V
Stop 15.000V
Step .5000V

Variable2:
VG -Ch3
Start 15.000V
Stop -15.000V
Step -3.0000V

Conetante:
VS -Ch1 .0000V

Fig. FR-7



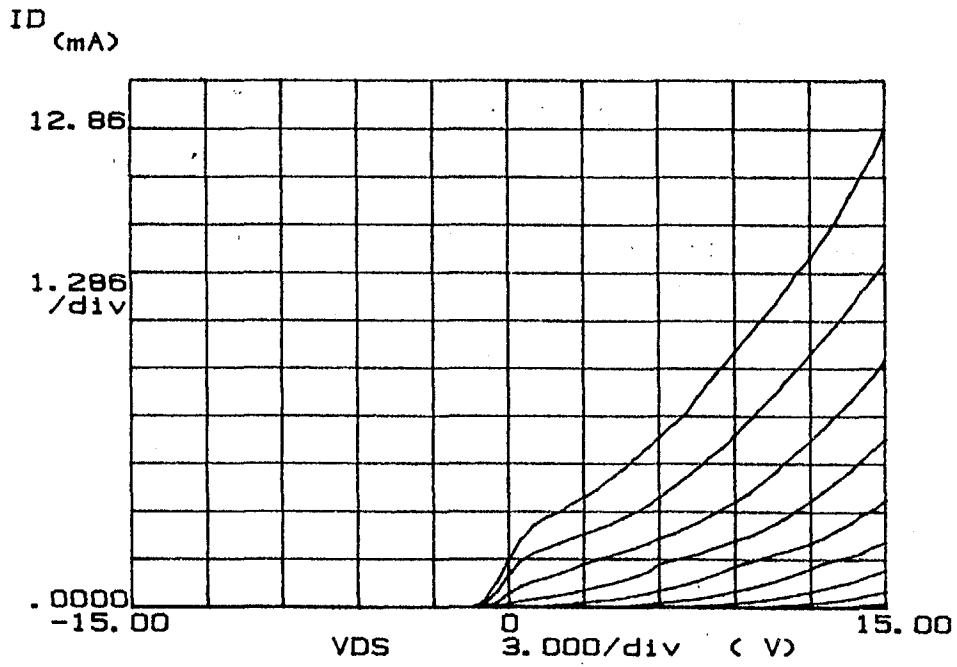
Variable1:
VDS -Ch2
Linear sweep
Start -15.000V
Stop 15.000V
Step .5000V

Variable2:
VG -Ch3
Start 15.000V
Stop -12.000V
Step -9.0000V

Constants:
VS -Ch1 .0000V

Fig. FR-8

Sputter clean
no bias



Variable1:
VDS -Ch2
Linear sweep
Start -15.000V
Stop 15.000V
Step .5000V

Variable2:
VG -Ch3
Start 15.000V
Stop -12.000V
Step -3.0000V

Constants:
VS -Ch1 .0000V

Fig. FR-9

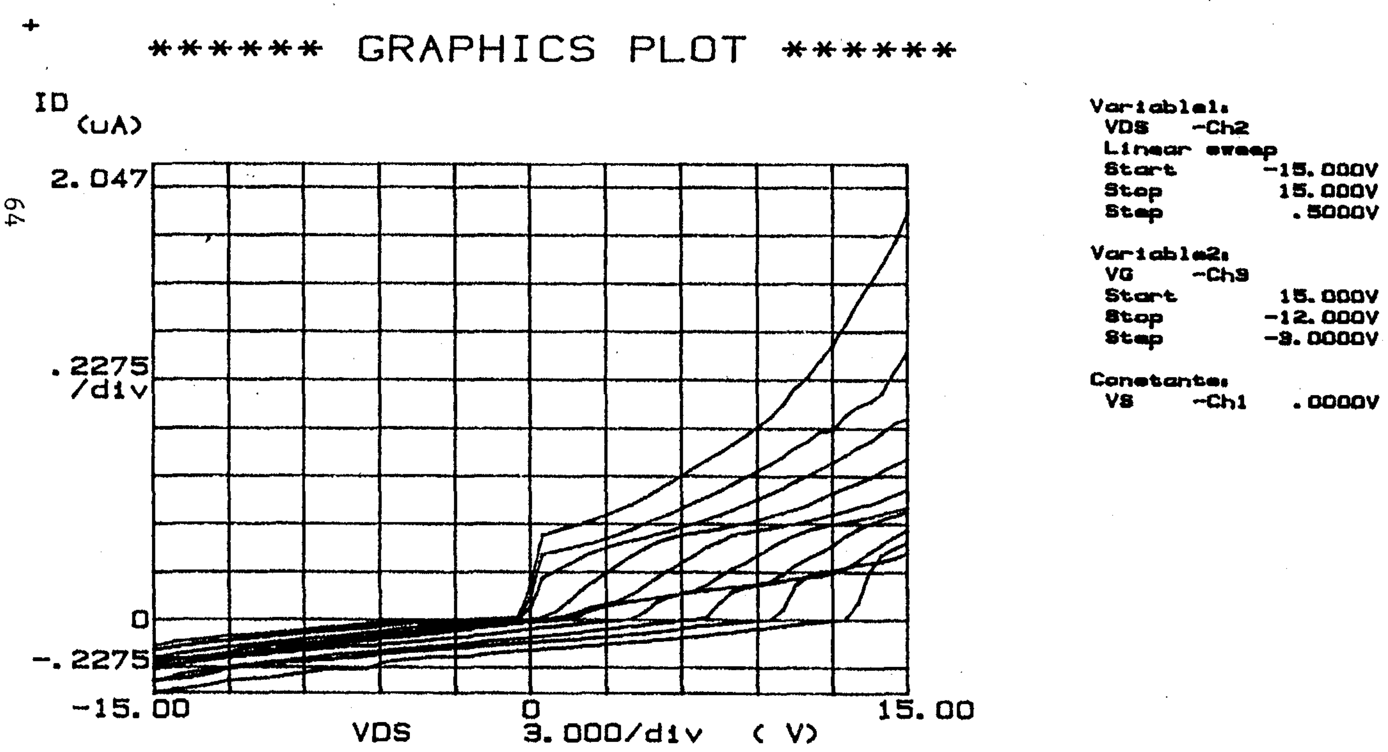
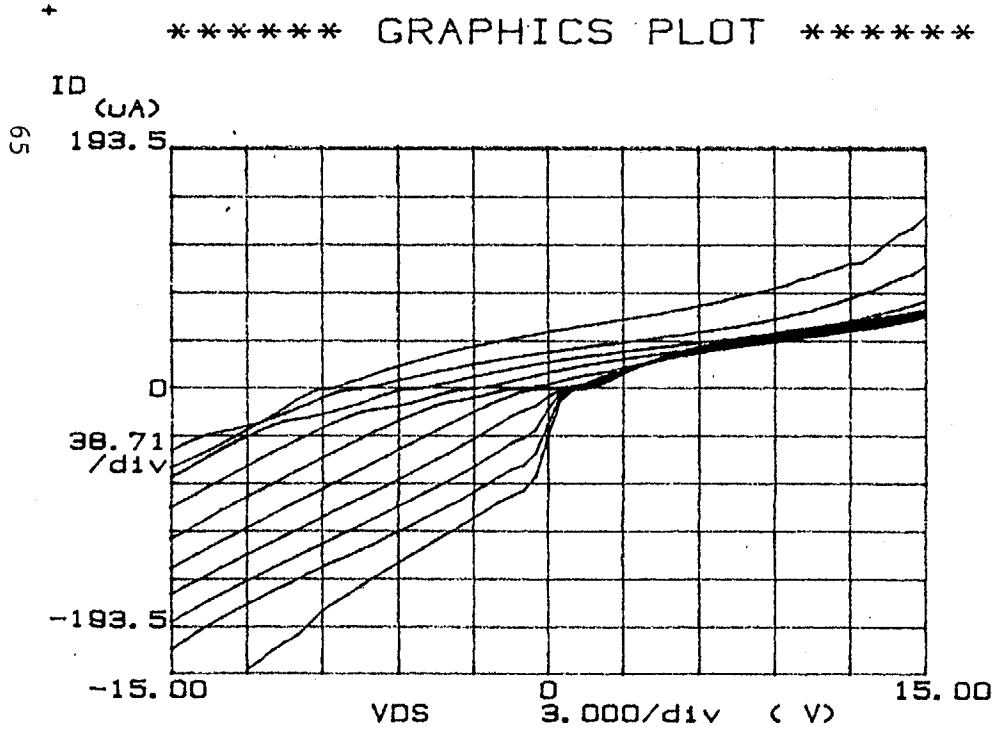

****** GRAPHICS PLOT ******
ID (uA)
2.047
.2275 /div
0
-.2275
-15.00
0
15.00
VDS
3.000/div (V)
Variable1:
VDS -Ch2
Linear sweep
Start -15.000V
Stop 15.000V
Step .5000V
Variable2:
VG -Ch3
Start 15.000V
Stop -12.000V
Step -3.0000V
Constants:
VS -Ch1 .0000V

Fig. FR-10



Variable1:
VDS -Ch2
Linear sweep
Start -15.000V
Stop 15.000V
Step .5000V

Variable2:
VG -Ch3
Start -15.000V
Stop 12.000V
Step 3.0000V

Constants:
VS -Ch1 .0000V

Fig. FR-11

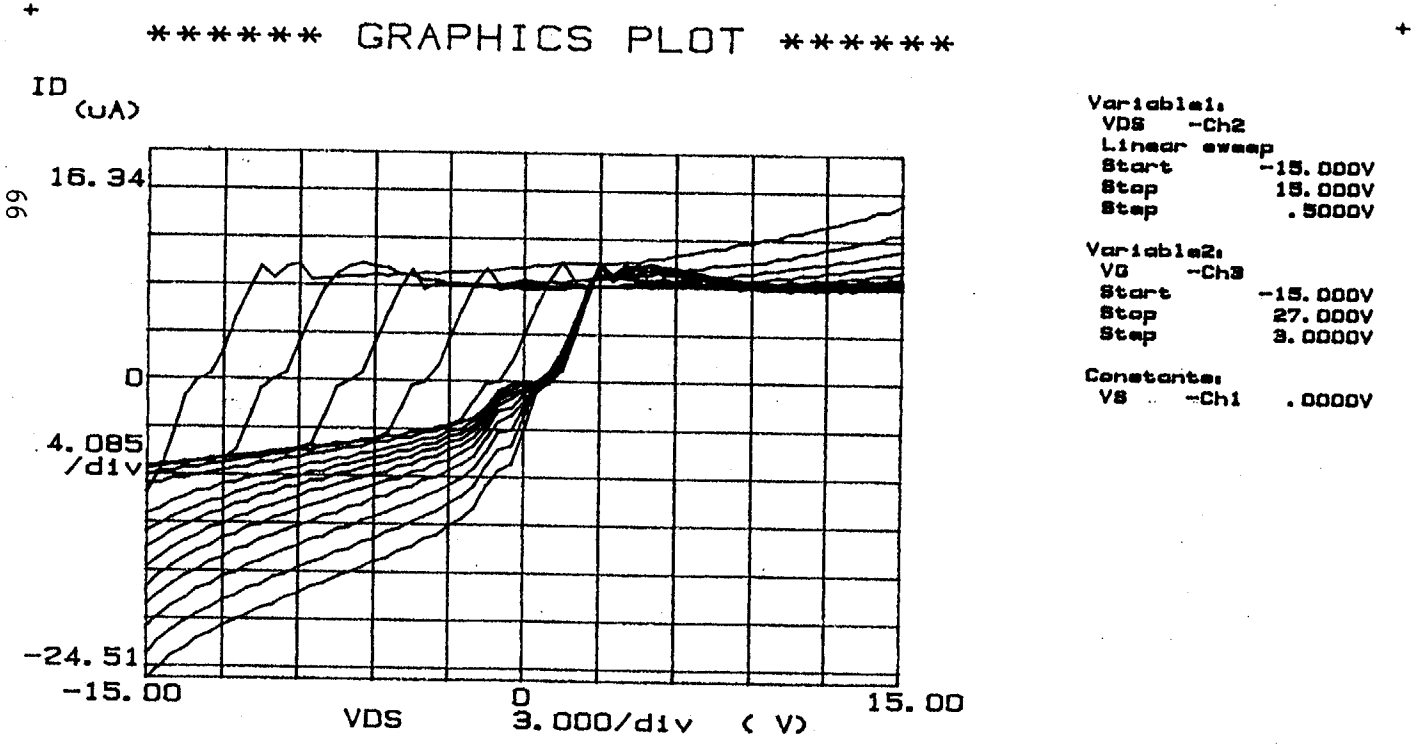
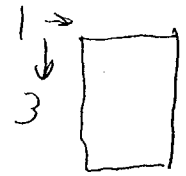
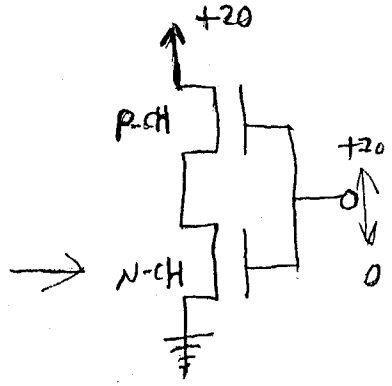

****** GRAPHICS PLOT ******
ID (uA)
16.34
0
4.085 /div
-24.51
-15.00
0
15.00
VDS
3.000/div (V)
99
Variable1:
VDS -Ch2
Linear sweep
Start -15.000V
Stop 15.000V
Step .5000V
Variable2:
VG -Ch3
Start -15.000V
Stop 27.000V
Step 3.0000V
Constants:
VS -Ch1 .0000V

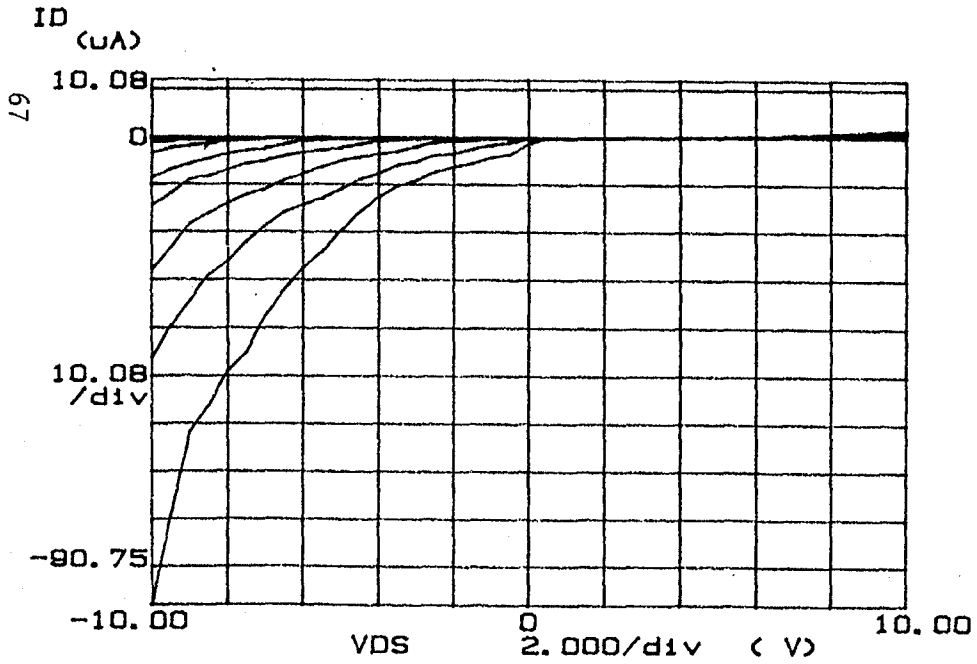
Fig. FR-12



CMOS
N-CH

Probed with wire





Variable1:
VDS -Ch2
Linear sweep
Start -10.000V
Stop 10.000V
Step .5000V

Variable2:
VG -Ch3
Start 10.000V
Stop -0.0000V
Step -2.0000V

Constants:
VS -Ch1 .0000V

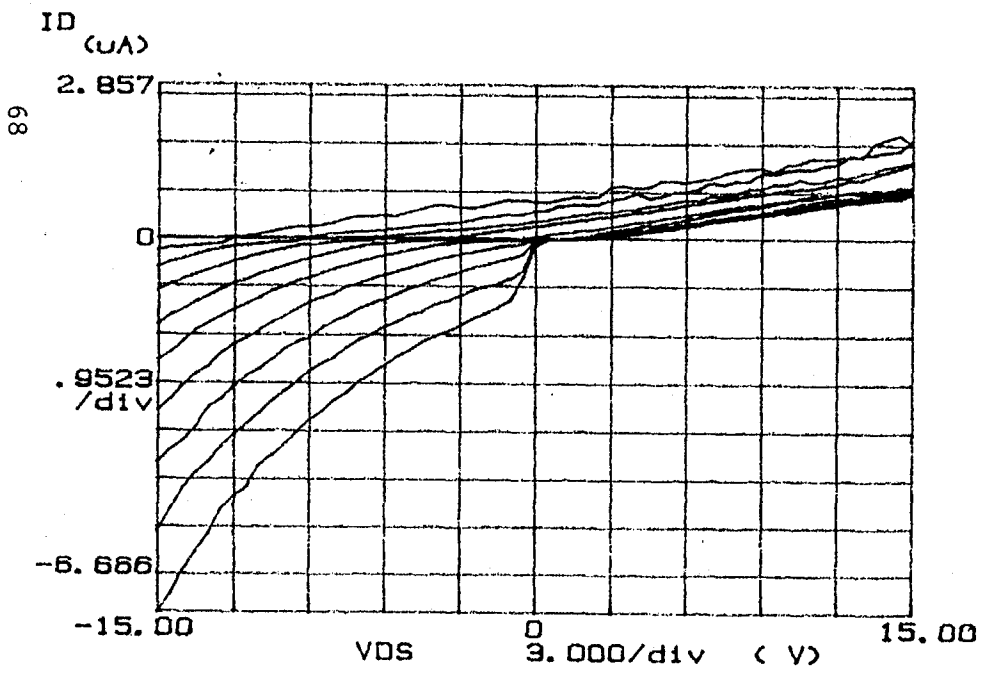
10^{-4}A @ 10V

$\frac{10}{10^{-4}} \approx 10^5 \Omega$

Fig. FR-13

Fig 13b
probe with needle

****** GRAPHICS PLOT ******



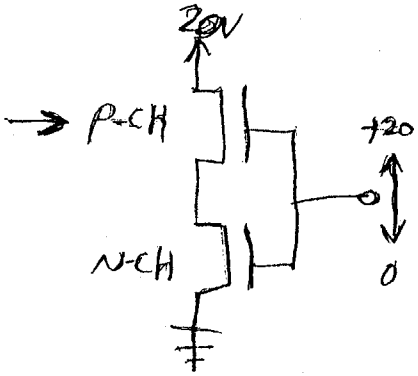
Variable1:
VDS -Ch2
Linear sweep
Start -15.000V
Stop 15.000V
Step .5000V

Variable2:
VG -Ch3
Start -15.000V
Stop 12.000V
Step 3.0000V

Constants:
VS -Ch1 .0000V

Fig. FR-13b

CMOS
P-CH



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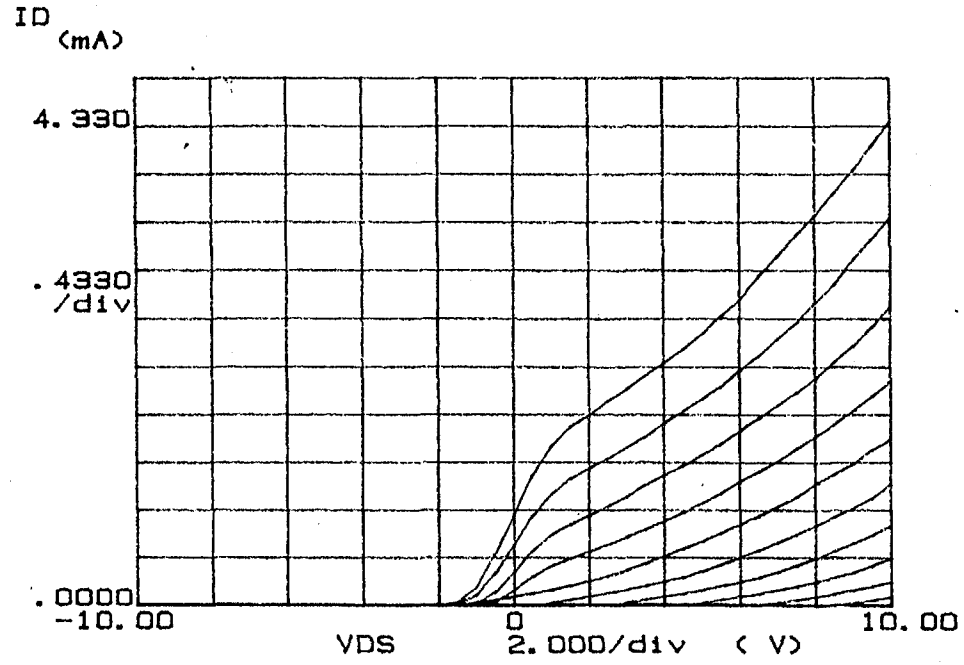


Variable1:
VDS -Ch2
Linear sweep
Start -10.000V
Stop 10.000V
Step .5000V

Variable2:
VG -Ch3
Start 10.000V
Stop -0.9990V
Step -2.0000V

Constants:
VS -Ch1 .0000V

$\approx 2\times10^{3}\Omega$

Fig. FR-14

JAMES D. WELCH
ATTORNEY AT LAW
PROFESSIONAL ENGINEER

INTELLECTUAL PROPERTY
402-391-4448

10328 PINEHURST AVE.
OMAHA, NEBRASKA 68124

March 25, 1995

Commissioner
Patent & Trademark Office
Washington, D.C. 20231

RE: APPLICATION OF WELCH TITLED " MOSFET SYSTEMS AND FABRICATION PROCEDURE"
SERIAL NO. : 08/250,906
FILE DATE 05/31/94
ART UNIT: 2508
EXAMINER: LOKE

Dear Sir;

I am in receipt of an Office Action dated 10/21/94 regarding the identified Application.

First, please find enclosed a check for $435.00 to allow response within the third extension month after the Office Action as per 37 C.F.R. 17(c).

The Examiner has required a New Title for the Application. In response, please cancel the Original Title and replace it with:

SCHOTTKY BARRIER MOSFETS AND SYSTEMS

The Applicant will be receptive to suggestions by the Examiner as to further change in the title, should such be necessary.

Next, the Examiner has required a New Abstract. In response please cancel the Original Abstract and replace it with a New Abstract, provided in Attachment 1 hereto.

Next, the Examiner requires that the Drawings be modified such that Legends stating that Figures 1a, 1b, 2a and 2b are Prior Art. Please find enclosed Drawings Marked-up in Red. The Examiner is respectfully requested to approve the proposed changes indicated.

Next, the Examiner has properly noted that the word "SCHOTTKY" is misspelled as "SCHOTTKEY" throughout the Disclosure of the present Application. In response please delete the word [Schottkey] or [schottky] as the case might be, and in its place enter the word <u>Schottky</u> in the following locations:

Page 4, Line 20;
Page 4, Line 21;
Page 4, Line 26;
Page 4, Line 29;
Page 4, Line 30;
Page 4, Line 32;
Page 5, Line 2;
Page 5, Line 11;
Page 5, Line 16;
Page 5, Line 19;
Page 6, Line 4;
Page 6, Line 6;
Page 6, Line 8;
Page 6, Line 14;

Page 6, Line 30;
Page 7, Line 3;
Page 9, Line 1;
Page 10, Line 27;
Page 12, Line 33;
Page 13, Line 15;
Page 13, Line 20;
Page 13, Line 34;
Page 14, Line 12;
Page 16, Line 12;
Page 16, Line 13;
Page 16, Line 16;
Page 16, Line 20;
Page 17, Line 35;
Page 18, Line 13;
Page 21, Line 7;
Page 25, Line 12;
Page

Also, on Page 9, in Line 25, please delete [(3)] and enter (3000).

Continuing, as Examiner Loke will recall, I dropped in on, and visited with him when I was in Washington last fall on unrelated business, which visit was after I had received the Office Action to which this paper is a Response. At that time, Examiner Loke provided me with a Patent in addition to Honma et al. cited in said Office Action. The additional Patent was to Koeneke et al., No. 4,485,550. In the later Patent the use of Schottky Barriers in the Source and Drain Regions of MOSFETS is disclosed, as well as the use of Schottky Barrier MOSFETS in CMOS Systems. In addition, while at the Patent Office I did some searching myself. Please find enclosed a continued Information

Disclosure to provide additional References which I found.

Now, to set the stage for this response it is necessary to add that I have recently been doing a rather in-depth analysis of how the N and P-Channel Schottky barrier MOSFET Devices which I have fabricated operate, (ie. how the Drain Current vs. Drain to Source Voltage as a function of Gate Voltage Curves, of which examples are shown in Figs. 6 & 7 of the Original Disclosure of the present Application, are achieved). I have been doing this to prepare a Final Report to the U.S Department of Energy, which funded my work to date. Prior to conducting said Analysis I had actually considered abandoning the present Application and continue my efforts only via a CIP Application. I mentioned this to Examiner Loke. However, in view of the results of my recent Analysis, I have decided to further prosecute the present Application. A copy of the results of said Analysis, in their present state, is included in Attachment 2 hereto. A close study thereof will reveal a consistent explanation of how the fabricated devices are thought to operate. In doing said Analysis it has become very much apparent to me that <u>while I have appreciated that my devices operate, (ie. provide Operating Drain Current vs. Drain to Source Voltage as a function of applied Gate Voltage Curves), only with Opposite Polarity voltages applied to the Drain and Gate, as referred to the Source, I have not appreciated, until just recently, that not only do diffused junction based MOSFETS operate with the same polarity voltages applied to the Drain and Gate, (which I knew), but so do all reported Schottky barrier MOSFETS, EMPHASIS ADDED.</u> That is, my fabricated N <u>and</u> P-Channel Devices provide Drain Current vs. Drain to Source Voltage, as a function of applied Gate voltage Curves, <u>only</u> when opposite polarity voltages are applied to the Drain and Gate thereof, and then, only where the Drain Voltage polarity is Negative and the Gate Voltage polarity is Positive in N-Channel Devices fabricated on P-type Silicon;

and only where the Drain Voltage polarity is Positive and the Gate Voltage polarity is Negative in P-Channel Devices fabricated on N-type Silicon. See Fig. 6 in the Original Disclosure for a graphical representation of the present invention N-Channel MOSFET Device operating Curves, and Fig. 7 in the Original Disclosure for a graphical representation of the present invention P-Channel MOSFET operating Curves. Note the N and P-Channel Schottky barrier MOSFETS I fabricated have operating Curves in Opposite Quadrants, emphasis added. This shows the effect of the doping type of the starting Semiconductor. (Attachment 2 provides empirically derived results from additional fabricated Schottky barrier MOSFETS which show Drain Current vs. Drain to Source Voltage as a function of Gate Voltage Curves of the same general nature. Such results have been repeated many times, although our fabrication facilities have so far limited our success in providing consistency in Current levels etc from Device to Device).

Now, papers and Patent of which I have become aware, which consider Schottky barrier MOSFETS, do not in any case, teach such a Drain Current vs Drain to Source Voltage as a function of Gate Voltage Operating Curve scenario as I have achieved from my Chromium/Chromium Disilicide Source and Drain based Schottky barrier MOSFETS. That is, all references of which I am now aware, teach Schottky barrier MOSFETS with operating characteristics similar to diffused junction MOSFETS, wherein the Polarity of the Voltages applied to the Drain and Gate must be the same.

For instance, the 550 Patent to Koeneke et al. teaches that the Platinum Silicide Schottky barrier MOSFETS described can be substituted directly in CMOS systems for Diffused Junction MOSFETS. My Chromium Disilicide Schottky barrier MOSFETS <u>can not</u> be so substituted because current flows through them in a

direction opposite to current in Diffused Junction MOSFETS, (ie. the Drain Voltage is required to be of an Opposite Polarity in my Devices as compared to Diffused Junction MOSFETS to obtain Operating Drain Current vs. Drain to Source Voltage as a function of Gate Voltage, Curves). The Koeneke et al. 550 Patent teaches that substituting a Schottky barrier MOSFET for at least one Diffused Junction MOSFET in a CMOS system will prevent "Latch-up" problems. That this is a valid interpretation of the Koeneke et al. teachings, it should be noted that a Patent to Lepselter, No. 4,300,152 is referenced in Line 19 of Column 1 in the Koeneke et al. 550 Patent, as the Patent which describes the Schottky barrier MOSFETS considered by Koeneke et al. Also, a paper by Lepselter and Sze, published in the Proceedings of the IEEE, August 1968, pages 1400-1402 goes further in describing the Schottky barrier MOSFETS considered by Koeneke et al. A copy of this Article is also included with this response. On page 1401 of said Lepselter et al. paper, there are shown graphed operating Drain Current vs. Drain to Source Voltage as a function of Gate Voltage Curves for the P-Channel Devices described by Lepselter and Sze, and Koeneke et al. Note that while said Lepselter and Sze Article graphs, at first glance, seem to indicate that the polarity of Voltages applied to the Drain and to the Gate are of opposite polarity, the Fig. 4 Energy Band diagrams make it clear that the Gate Voltage is greater than the Threshold Voltage of Channel Inversion, while the "Absolute Value" of the Drain Voltage is greater than zero. Description on page 1401 makes it clear that the Source Junction of the Lepselter et al. described Platinum Silicide Schottky barrier devices is Reverse Biased during operation. (See Second Column on page 1401 near the bottom thereof). Note, it is very definitely the Drain Junctions of my Chromium Disilicide Schottky Barrier MOSFETS which reverse biased during Operation. (See Lines 1 and 2 on page 22 of the present Patent Application where this was noted in the Original Disclosure). Also note near the top of the page 1401 of the Lepselter and Sze Article, in the second column thereof, that it

states that the Saturation Curves of the Drain Current are the result of Channel Region "Pinch-Off". Channel Region Pinch-off only occurs in Diffused Junction MOSFETS because the same polarity Voltage is applied to the Drain and Gate, EMPHASIS ADDED. That is, the Lepselter Schottky barrier MOSFETS provide Saturation Drain Current Characteristics by a mechanism which is identical to that which causes Saturation Drain Current Curves in Diffused Junction MOSFETS.

Now, in both the P and N-Channel Chromium Disilicide Schottky Barrier MOSFET Devices I have fabricated, Channel Region "Pinch-off" can not occur where we find Operating Characteristics because the Drain and Gate Voltages are of opposite polarity, EMPHASIS ADDED. "Pinch-off" can occur in my Schottky barrier MOSFETS only when they are not conducting current. The Saturation of the Drain Current in my Schottky barrier MOSFETS seems to be the result of limited Tunneling Current based upon the effective doping of the Inverted Channel Region and not the result of formation of a "Pinch-off" Region caused by the same Polarity Voltage being applied to the Drain and Gate. Drain Current flow can not be saturated in my Schottky barrier MOSFETS by a "Pinch-off" effect. That means my Chromium Disilicide Schottky barrier Devices operate inherently different from the Schottky barrier MOSFETS described by Lepselter and Sze, and by Koeneke et al. I have been unable to find any reference which discloses Schottky barrier MOSFETS which have Drain Current vs. Drain to Source Voltage as a function of Gate Voltage Operating Curves present only where the Drain and Gate Voltage Polarities are opposite, in both N and P-Channel Schottky barrier MOSFETS. In fact, my Patent Application, and a CIP thereof which has been submitted to Claim Single Device Equivalents to CMOS, are the only references I know of, after a focused Search, which teach such MOSFET Operation Curves in either a N or P-Channel Schottky barrier MOSFET, such as I have

achieved. In addition, I believe I now understand why basic nature of the operating Curves I have repeatably obtained in numerous fabricated Chromium Disilicide Schottky barrier Devices, are achieved. As mentioned, I have included, in Attachment 2, an analysis to which the Examiner is referred for the explanation. I do not know why previous researchers have not reported such results. I can only guess that the Schottky barriers they investigated were formed from metals and/or silicides etc. which acted essentially as P-Type dopants in N-type Silicon, thereby providing essentially P-type doped Source and Drain Regions in the MOSFETS achieved, rather than true Schottky barrier Junctions. For instance, Aluminum on N-type Silicon is known to form such a P-type doping junction with N-type Silicon. I am including a Paper by Hogeboom and Cobbold herewith found in Electronics Letters, March 1971, Vol. 7, Nos. 5/6 which describes such Aluminum on N-type Silicon Schottky barrier MOSFETS. Again, a graph on page 134 thereof shows that the Voltage Polarities applied to the Drain and Gate are the same where Drain Current vs. Drain to Source Voltage as a function of Gate Voltage are found Considering that previous Schottky barrier MOSFETS reported have actually been essentially equivalent to Diffused Junction MOSFETS, in that the Metal or Silicide etc. involved in forming the Schottky barrier acts essentially as a P-type Dopant, would explain the difference in results I have achieved and the results others have reported. My Schottky barrier MOSFET Devices operate as a result of the presence of "actual" Schottky barrier Source and Drain junctions, on both N and P-type Silicon, rather than as the result of an essentially Silicon doping effect caused by the metal or metal silicide etc. involved in contact with N-type Silicon. In addition, I will mention that I found no reported Drain Current vs. Drain to Source Volts as a function of Gate Volts Curves for Schottky Barrier MOSFETS fabricated on P-Type Silicon in any reference. In that light I find no reference which would enable Claims such as I provide herein

directly. I do find mention of Schottky barriers formed on P-type Silicon, but again, I find no reported empirical data to prove such works in a MOSFET setting. Rather any such mention is speculative in nature. I have provided such data in the original Disclosure, in Figs. 6 and 7. In fact, I firmly believe that the results reported by Lepselter et al. and Hogeboom show that the Schottky barrier forming metals used in the work said authors reported acted as P-type dopants in N-type Silicon. Neither paper reports actual fabricated Schottky barrier MOSFETS on P-type Silicon. The Hogeboom et al. article seems to report such at first glance, but a careful reading thereof will show that a N-type diffusion was carried out when P-type Silicon was utilized.

In view of the above, I feel that I should be able to Claim Schottky barrier MOSFETS in which the operating Drain Current vs. Drain to Source Voltage as a function of Gate Voltage Curves, are present only where the Applied Drain and Gate Voltages have opposite Polarities, such being valid for both the N and P-Channel MOSFETS I have fabricated. As far as I know, no other MOSFETS with such Drain Current vs. Drain to Source Voltage as a function of Gate Voltage Operating Curves have ever been reported, EMPHASIS ADDED.

It is also to be noted that the accompanying Attachment 2 provides an analysis of how my Chromium Disilicide MOSFETS operate in a CMOS System. Said Operation is very different from that of Diffused Junction, and other reported Schottky barrier CMOS Systems. Said operation involves a regenerative switching mechanism, with the effective Sources, (as defined by placement in a circuit and Voltage Polarities applied thereby), being the interconnected Junctions rather than Drains as is the case in Conventional Diffused Junction, and other reported Schottky barrier MOSFETS.

Now, in view of the Examiner's position with respect to the Original Claims, the Examiner is respectfully requested to please cancel all Original Claims and Examine the following New Claims.

NEW CLAIMS

39. A P-Channel Schottky barrier Metal Oxide Semiconductor Field Effect Transistor (MOSFET) device formed in the surface region of an N-type Semiconductor, comprising two Schottky barrier junctions, termed Source and Drain, which Source and Drain Schottky barrier Junctions are separated by an N-type Semiconductor Channel Region, in which (MOSFET) a Gate is present and offset from said N-type Semiconductor Channel Region by an insulator material, such that during use Drain Current vs. Drain to Source Voltage as a function of Gate Voltage Operating Curves appear only when the Voltage applied to the Drain is of a Positive Polarity, and the Voltage applied to the Gate is of a Negative Polarity so as to induce an inverted P-type Channel Region, both said Drain and Gate Voltages being referenced to the Source.

40. A P-Channel Schottky Metal Oxide Semiconductor Field Effect Transistor (MOSFET) as in Claim 39 in which the Semiconductor is Silicon and the Source and Drain Schottky barrier Junctions are formed between said Silicon and at least one member of the group consisting of Chromium and Chromium Disilicide.

41. An N-Channel Schottky barrier Metal Oxide Semiconductor Field Effect Transistor (MOSFET) device formed in the surface region of an P-type Semiconductor, comprising two Schottky barrier junctions, termed Source and Drain, which Source and Drain Schottky barrier Junctions are separated by a P-type Semiconductor Channel region, in which (MOSFET) a Gate is present

and offset from said P-type Semiconductor Channel Region by an insulator material, such that during use Drain Current vs. Drain to Source Voltage as a function of Gate Voltage Operating Curves appear only when the Voltage applied to the Drain is of a Negative Polarity, and the Voltage applied to the Gate is of a Positive Polarity so as to induce an inverted N-type Channel Region, both said Drain and Gate Voltages being referenced to the Source.

42. A P-Channel Schottky barrier Metal Oxide Semiconductor Field Effect Transistor (MOSFET) as in Claim 41 in which the Semiconductor is Silicon and the Source and Drain Schottky barrier Junctions are formed between said Silicon and at least one member of the group consisting of Chromium and Chromium Disilicide.

43. A Complimentary Metal Oxide Semiconductor (CMOS) System comprising an N-Channel Schottky barrier Metal Oxide Semiconductor Field Effect Transistor (MOSFET) and a P-Channel Schottky barrier (MOSFET), one Schottky barrier of said N-Channel Schottky barrier (MOSFET) and one Schottky barrier of said P-Channel Schottky barrier (MOSFET) being electrically interconnected to one another, and said Gates of said N and P-Channel (MOSFETS) being electrically interconnected to one another; which P-Channel Schottky barrier (MOSFET) comprises a (MOSFET) device formed in the surface region of an N-type Semiconductor, said P-Channel (MOSFET) comprising two Schottky barrier junctions, termed Source and Drain, which Source and Drain Schottky barrier Junctions are separated by an N-type Semiconductor Channel region, in which P-Channel Schottky barrier (MOSFET) a Gate is present and offset from said N-type Semiconductor Channel Region by an insulator material, such that during use Drain Current vs. Drain to Source Voltage as a function of Gate Voltage Operating Curves appear only when the Voltage applied to the Drain is of a Positive Polarity, and the Voltage applied to the Gate is of a Negative Polarity, so as to

induce an inverted P-type Channel Region, both said Drain and Gate Voltages being referenced to the Source; and which N-Channel Schottky barrier comprises a (MOSFET) device formed in the surface region of a P-type Semiconductor, said N-Channel (MOSFET) comprising two Schottky barrier junctions, termed Source and Drain, which Source and Drain Schottky barrier Junctions are separated by a P-type Semiconductor Channel region, in which N-Channel Schottky barrier (MOSFET) a Gate is present and offset from said P-type Semiconductor Channel Region by an insulator material, such that during use Drain Current vs. Drain to Source Voltage as a function of Gate Voltage Operating Curves appear only when the Voltage applied to the Drain is of a Negative Polarity, and the Voltage applied to the Gate is of a Positive Polarity, so as to induce an inverted N-type Channel Region, both said Drain and Gate Voltages being referenced to the Source; such that when a Negative Polarity Voltage is applied to the electrically noninterconnected Schottky barrier of the N-Channel Schottky barrier (MOSFET), said Negative Polarity being with respect to the Voltage applied to the electrically noninterconnected Schottky barrier of the P-Channel Schottky barrier (MOSFET), and the Gate Voltage is set to essentially that applied to the electrically noninterconnected Schottky barrier of the N-channel Schottky barrier (MOSFET), the voltage at the electrically interconnected Schottky barriers of the N and P-Channel Schottky barrier (MOSFETS) switches to essentially that applied to the electrically noninterconnected Schottky barrier of the P-Channel Schottky barrier (MOSFET); and when the Gate Voltage is set to essentially that applied to the electrically noninterconnected Schottky barrier of the P-Channel Schottky barrier (MOSFET), the voltage at the electrically interconnected Schottky barriers switches to essentially that applied to the electrically noninterconnected Schottky barrier of the N-Channel Schottky barrier (MOSFET).

44. A Schottky Metal Oxide Semiconductor Field Effect Transistor (MOSFET) as in Claim 43 in which the Semiconductor is Silicon and

the Source and Drain Schottky barrier Junctions of both the N and P-Channel (MOSFETS) are formed between said Silicon and at least one member of the group consisting of Chromium and Chromium Disilicide.

45. A Balanced Differential Pair Metal Oxide Semiconductor Field Effect Transistor (MOSFET) System comprising a first N-Channel Schottky barrier (MOSFET) and a second N-Channel Schottky barrier (MOSFET), which first and second N-Channel Schottky barrier (MOSFETS) each comprise two Schottky barrier junctions, termed Source and Drain, which Source and Drain Schottky barrier Junctions are separated by a P-type Semiconductor Channel region, in each of which said first and second N-Channel (MOSFETS) a Gate is present and separated from said P-type Semiconductor Channel Region by an insulator material, said Sources of each said first and second N-Channel (MOSFET) being electrically interconnected to one another such that during use Drain Current vs. Drain to Source Voltage as a function of Gate Voltage Operating Curves appear only in each N-Channel (MOSFET) when the Voltage applied to the Drain is of a Negative Polarity, and the Voltage applied to the Gate is of a Positive Polarity, both said Drain and Gate Voltages being referenced to the Source; such that in use Negative Polarity Voltage is applied to both of the electrically noninterconnected Drain Schottky barrier Junctions of the two N-Channel Schottky barrier (MOSFETS), said Negative Polarity being with respect to the Voltage applied to the electrically interconnected Source Schottky barrier junctions of said first and second N-Channel Schottky barrier (MOSFETS), and such that a Voltage is applied between the Gates of said first and second N-Channel (MOSFETS), the effect being that current flow through each of the N-Channel (MOSFETS) is controlled in a complimentary manner by said applied Voltage between said Gates.

46. A Balanced Differential Pair Metal Oxide Semiconductor Field Effect Transistor (MOSFET) System as in Claim 45 in which the Semiconductor is Silicon and the Source and Drain Schottky

barrier Junctions in both N-Channel Schottky barrier (MOSFETS) are formed between said Silicon and at least one member of the group consisting of Chromium and Chromium Disilicide.

47. A Balanced Differential Pair Metal Oxide Semiconductor Field Effect Transistor (MOSFET) System comprising a first P-Channel Schottky barrier (MOSFET) and a second P-Channel Schottky barrier (MOSFET), which first and second P-Channel Schottky barrier (MOSFETS) each comprise two Schottky barrier junctions, termed Source and Drain, which Source and Drain Schottky barrier Junctions are separated by a N-type Semiconductor Channel region, in each of which said first and second P-Channel (MOSFETS) a Gate is present and separated from said N-type Semiconductor Channel Region by an insulator material, said Sources of each said first and second P-Channel (MOSFET) being electrically interconnected to one another such that during use Drain Current vs. Drain to Source Voltage as a function of Gate Voltage Operating Curves appear only in each P-Channel (MOSFET) when the Voltage applied to the Drain is of a Positive Polarity, and the Voltage applied to the Gate is of a Negative Polarity, both said Drain and Gate Voltages being referenced to the Source; such that in use Positive Polarity Voltage is applied to both of the electrically noninterconnected Drain Schottky barrier Junctions of the two P-Channel Schottky barrier (MOSFETS), said Positive Polarity being with respect to the Voltage applied to the electrically interconnected Source Schottky barrier Junctions of said first and second P-Channel Schottky barrier (MOSFETS), and such that a Voltage is applied between the Gates of said first and second P-Channel (MOSFETS), the effect being that current flow through each of the P-Channel (MOSFETS) is controlled in a complimentary manner by said applied Voltage between said Gates.

48. A Balanced Differential Pair Metal Oxide Semiconductor Field Effect Transistor (MOSFET) System as in Claim 47 in which the Semiconductor is Silicon and the Source and Drain Schottky

barrier Junctions in both P-Channel Schottky barrier (MOSFETS) are formed between said Silicon and at least one member of the group consisting of Chromium and Chromium Disilicide.

49. A Complimentary Metal Oxide Semiconductor (CMOS) System comprising an N-Channel Schottky barrier Metal Oxide Semiconductor Field Effect Transistor (MOSFET) and a P-Channel Schottky barrier (MOSFET) as in Claim 43, in which both the N and P-Channel (MOSFETS) are simultaneously formed on a single Semiconductor substrate in which are present alternating regions of P and N-type doping present, by a common fabrication procedure.

50. A Balanced Differential Pair Metal Oxide Semiconductor Field Effect Transistor (MOSFET) System as in Claim 45 in which both said first and second N-Channel Schottky barier (MOSFETS) are formed on a single substrate.

51. A Balanced Differential Pair Metal Oxide Semiconductor Field Effect Transistor (MOSFET) System as in Claim 47 in which both said first and second P-Channel Schottky barier (MOSFETS) are formed on a single substrate.

52. A P-Channel Schottky barrier Metal Oxide Semiconductor Field Effect Transistor (MOSFET) device formed in the surface region of an N-type Semiconductor, comprising two Schottky barrier junctions, termed Source and Drain as in Claim 39, which Source and Drain are formed in regions of said N-type Semiconductor which have been etched.

53. An N-Channel Schottky barrier Metal Oxide Semiconductor Field Effect Transistor (MOSFET) device formed in the surface region of a P-type Semiconductor, comprising two Schottky barrier junctions, termed Source and Drain as in Claim 41, which Source and Drain are formed in regions of said P-type Semiconductor which have been etched.

Continuing, as all Claims to other than N and P-Channel Schottky barrier MOSFETS, Schottky barrier CMOS systems and Balanced Differential MOSFET pairs are dropped, the Examiner objections pertaining to uncertainty regarding Single Device Equivalents to CMOS should now be moot. Said Single Device Equivalents are subject of a presently submitted CIP Application.

It is believed that all points raised by the Examiner in the Office Action have been handled.

As well, in view of the foregoing, it is believed that with the Operational Voltage Polarities included as limitations to the Schottky barrier Devices Claimed in the New Claims, said New Claims should be Allowable in view of all known Prior Art. That is, unless the Examiner has references which obviate N and P-Channel MOSFETS which each provide operational characteristics only when the polarities applied to the respective Drains and Gates thereof are opposite, both referenced to the Source, as is the proven case with my Schottky barrier MOSFETS, the New Claims should be Allowable.

In closing, the Examiner is respectfully requested to, in view of all prior art, carefully consider the Analysis of Operation Report I have recently prepared for inclusion in the Final Report to the Department of Energy, which Agency funded my work, (which Analysis of Operation Report I've included herewith as Attachment 2). It is my belief that I have fabricated Schottky barrier MOSFETS which operate differently from any MOSFETS reported to data, and that the Analysis of Operation Report in Attachment 2 provides an explanation of the how the Schottky barrier Devices I have fabricated operate. Again, the basis and focus of Patentability of the New Claims presented infra herein, is believed found in the presence of Opposite Polarity Voltages applied to the Drain and Gate when Operational Drain Current vs. Drain to Source Voltage as a function of Gate Volts, Curves are found. Both my N and P-Channel Schottky

barrier MOSFETS demonstrate Operational Curves only when the applied Drain and Gate Voltages are of Opposite Polarities, as said voltages are referenced to the Source. No prior art of which I am aware describes MOSFETS which demonstrate such Drain Current vs. Drain to Source Voltage as a function of Gate Voltage Operating Curves in both N and P-Channel Schottky barrier MOSFETS fabricated by a common process. It is noted that the type of Schottky barrier Junctions formed on both the N and P-type Silicon, in my work, are of a similar type. That is, the Junction on one type of Silicon is a True Schottky barrier, while the Junction on the other type of Silicon is the result, (or equivalent to), of a Doping effect, (which doping type junctions seem to account for the Lepselter et al. and Hogeboom et al. results discused infra herein, so that said Lepselter et al. and Hogeboom et al. described Schottky barrier MOSFET devices are interchangable with Diffused Junction MOSFETS, as regards their Operational Drain and Gate Voltage Polarities being the same---as contrasted to my Schottky barrier MOSFET devices which can not be substituted for Diffused Junction MOSFETS because Opposite Polarity Voltages must be applied to the Drain and Gate to achieve Operational Drain Current vs. Drain to Source Voltage as a function of Gate Voltage. That is, the Drain Current in both the N and P-Channel Schottky barrier MOSFETS I have fabricated flows in a direction opposite to that in all known prior reported MOSFETS, in use, because the Voltage Polarity applied to the Drain must be opposite to that applied in all known prior art MOSFETS.)

Finally, the Homna et al. Patent cited by the Examiner is to MOS devices with one ohmic junction. The Schottky Barrier MOSFETS Claimed herein avoid such in that rectifying junctions are present at both Source and Drain. More importantly, as I read the Homna et al. Patent, the Devices described therein operate in an Accumulated Channel Mode. My Devices operate in an

Inverted Channel Mode and do not operate in an Accumulate Channel Mode at all.

The Examiner is, thus, respectfully requested to allow all pending New Claims 39 - 53.

Please contact Applicant Welch with any questions.

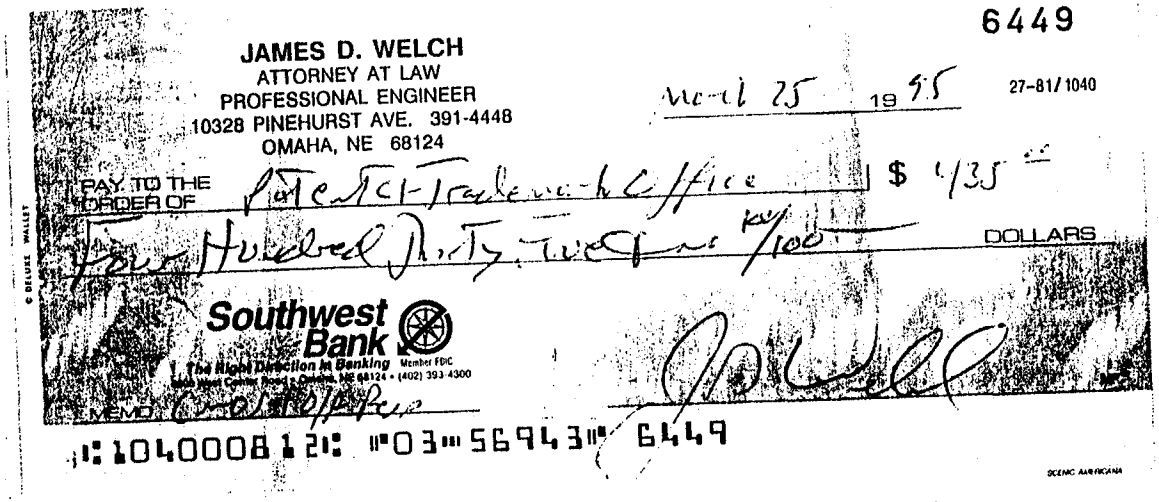
Sincerely,

JAMES D. WELCH
Reg. No. 31,216
JW/hs
ENC.

ATTACHMENT 1

ABSTRACT

N and P-Channel Metal Oxide Semiconductor Field Effect Transistors (MOSFETS), and (MOSFET) device systems, which have Schottky barrier source and drain to channel region junctions, are disclosed. Both the N and P-Channel Schottky barrier (MOSFET) devices are unique in that they provide operational drain current vs. drain to source voltage as a function of gate voltage only where the polarities of the drain voltage and gate voltage are opposite, as reference to the source. Complimentary Metal Oxide Semiconductor (CMOS) Field Effect Transistor systems which are a seriesed combination of the N and P-Channel (MOSFET) are also disclosed as are Balanced Differential MOSFET pairs which consist of electrically interconnected Schottky barrier MOSFETS of similar Channel type. Experimentally derived results which demonstrate operation of fabricated N and P-Channel Schottky barrier (MOSFETS) are also provided.



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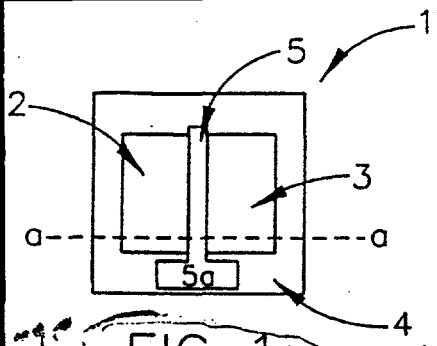

FIG. 1a
PRIOR ART

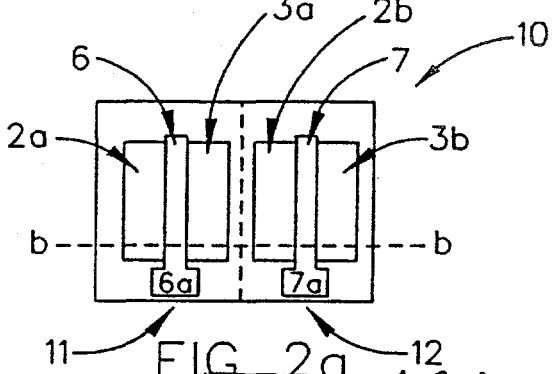

FIG. 2a
PRIOR ART

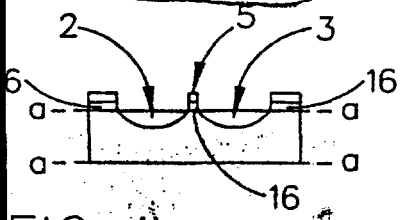

FIG. 1b
PRIOR ART

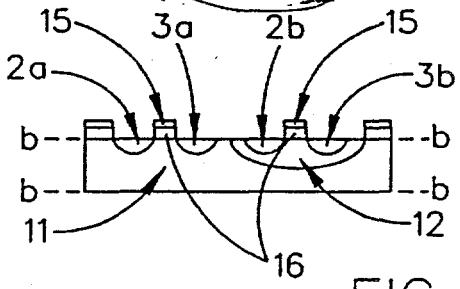

FIG. 2b
PRIOR ART

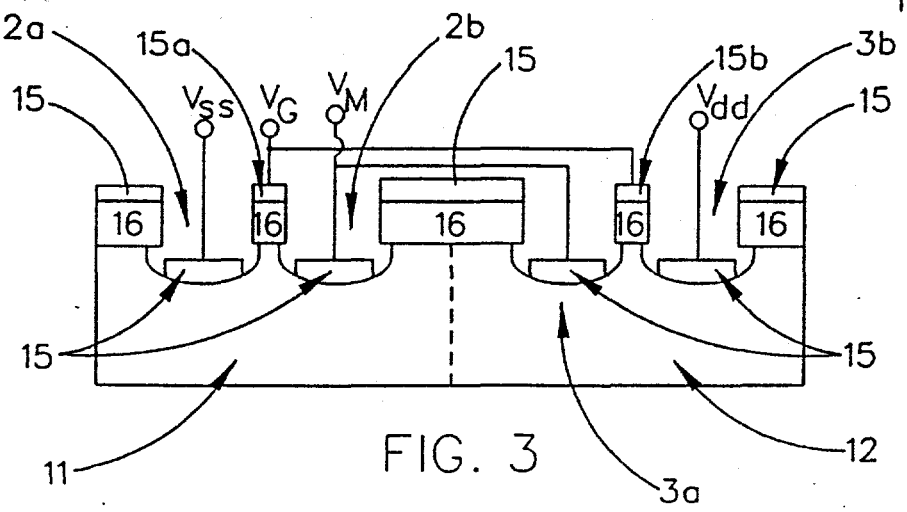

FIG. 3

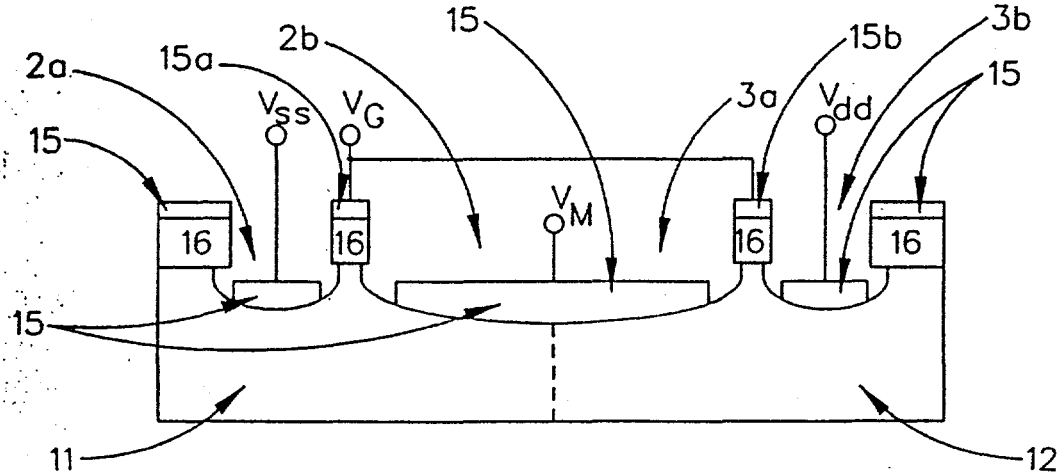

FIG. 4

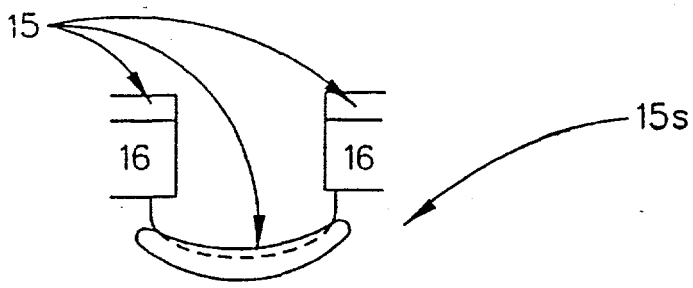

FIG. 5

United States Patent [19]

Welch

[11] **Patent Number: 4,696,093**

[45] **Date of Patent: Sep. 29, 1987**

[54] **FABRICATION OF SCHOTTKY BARRIER MOSFETS**

[76] Inventor: **James D. Welch**, 10328 Pinehurst Ave., Omaha, Nebr. 68124

[21] Appl. No.: **872,147**

[22] Filed: **Jun. 9, 1986**

[51] **Int. Cl.**[4] **H01L 21/441**

[52] **U.S. Cl.** **437/176**; 437/228; 437/247; 437/913

[58] **Field of Search** 29/571, 578, 589, 590, 29/591

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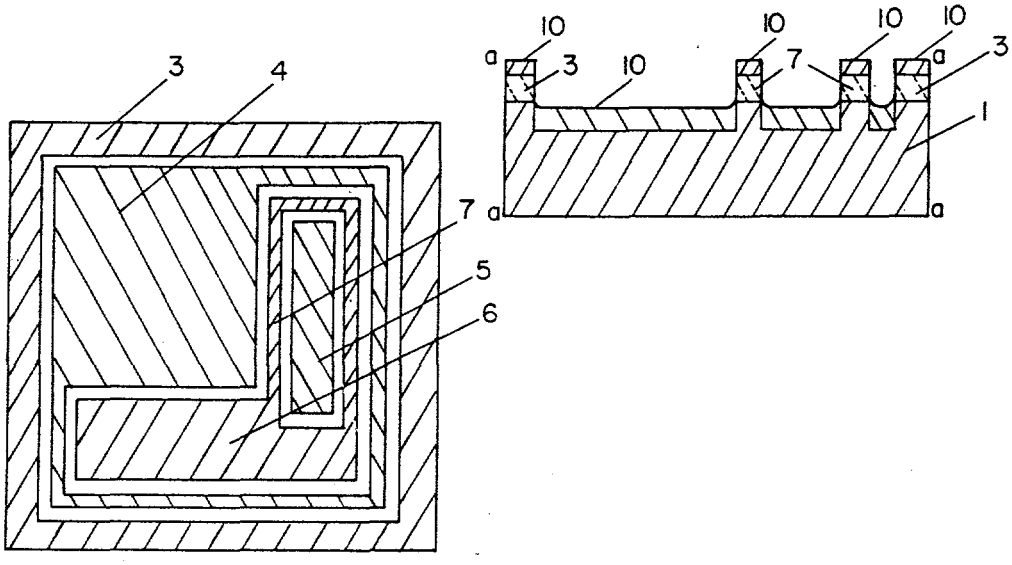
Primary Examiner—George T. Ozaki

Attorney, Agent, or Firm—James D. Welch

[57] **ABSTRACT**

A method for fabricating MOSFET devices by a one mask, one etch process utilizing vacuum deposited chromium, silicon upon which is grown SiO_2 and an anneal process. An optional optimizing ion implantation and activating anneal step is also disclosed, as are two, and three, mask and etch procedures.

4 Claims, 6 Drawing Figures



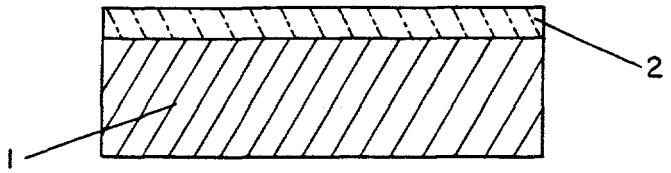


FIG. 1

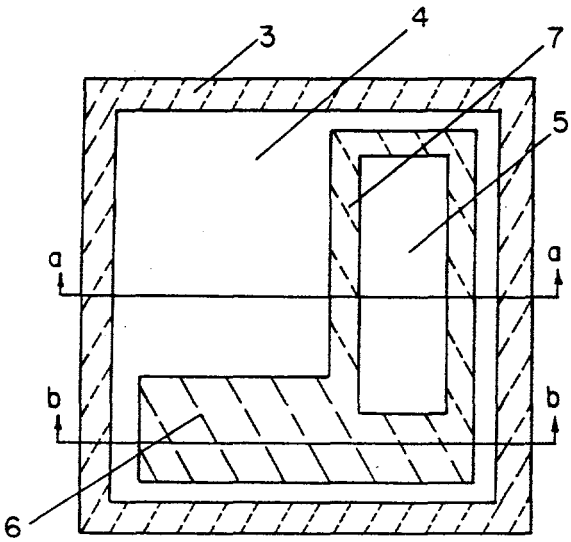


FIG. 2A

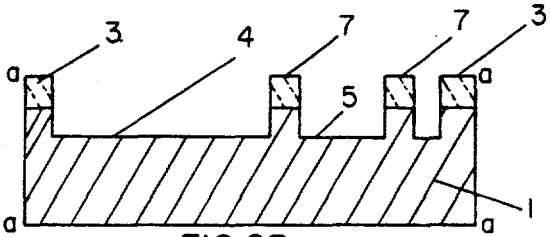


FIG. 2B

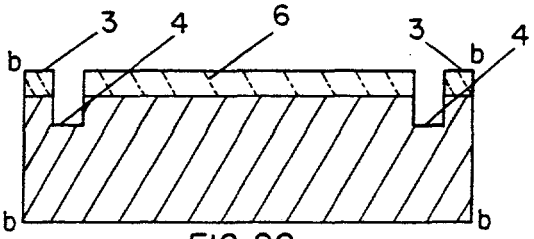


FIG. 2C

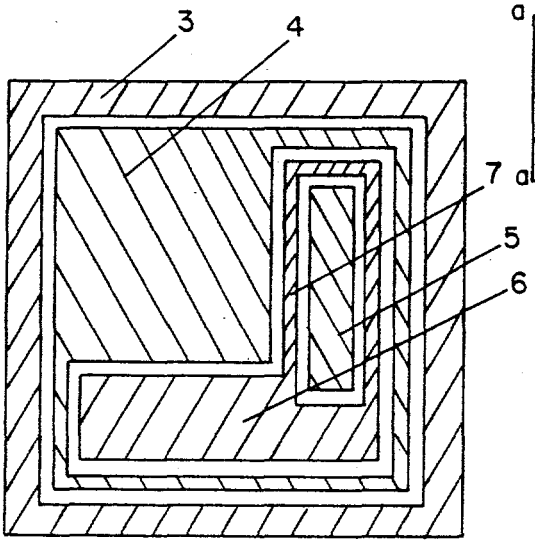


FIG. 3

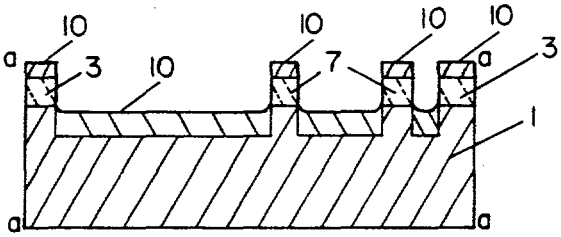


FIG. 2D

FABRICATION OF SCHOTTKY BARRIER MOSFETS

TECHNICAL FIELD

This invention relates to fabrication of transistors, and more particularly to a method for fabrication of MOSFETs which requires a single mask and etch step, in conjunction with chromium deposition and an anneal, with optional ion implantation allowed for to optimize the resulting device. Two, and three mask and etch procedures are also disclosed.

BACKGROUND ART

Typical processes for fabrication of MOSFETs require that numerous steps be performed. A silicon substrate must have silicon dioxide SiO_2 grown upon its surface. The oxide must then be etched to open source and drain regions through which dopants are entered and driven in via high temperature diffusions. Next, further oxide etches must be performed to remove all but the gate and gate pad oxide, then a layer of metal, which is typically aluminum must be deposited and etched. An additional sinter anneal is normally performed to cause good electrical contact between the metal and the underlying silicon.

Methods which reduce the number of steps, or the complexity of fabrication,or the energy required to fabricate MOSFETs are always of interest. A method for fabrication of MOSFETs which could reduce the number of steps required to the growing of, and etching of silicon dioxide, the deposition of a metal, and the annealing of the result, would be of great utility.

In 1974 a thesis titled "DESIGN AND FABRICATION OF SUB-MICRON CHANNEL MOS. TRANSISTORS BY DOUBLE ION IMPLANTATION" was submitted by James D. Welch to the Electrical Engineering Department of Toronto University. Disclosed in that work was the procedure Mr. Welch developed for fabricating MOSFET devices via the implantation of Boron ions around deposited and etched chromium patterns atop of N type silicon upon which had been grown 1000Å of SiO_2. During his work, Mr. Welch investigated an MOS capacitor to determine how chromium interacts with SiO_2 during an anneal at 650° C. That temperature was of particular significance in the fabrication procedure. While investigating the MOS capacitor Mr. Welch discovered that chromium deposited on the back, unpolished side of the silicon substrate, when annealed at 650° C. formed a very good rectifying junction. Recently Mr. Welch had a computer search run for authority on the use of chromium and silicon as a system. No patents were discovered but two articles were turned up. The articles, "COMPOUND FORMATION BETWEEN SILICON AND CHROMIUM" by Yacobi, Szadkowski and Zukotynski, J. App. Phys., Dec., 1980; and "METALLURGICAL AND ELECTRICAL PROPERTIES OF CHROMIUM SILICON INTERFACES", by Martinez and Esteve, Solid State Electronics, 1980; document that the effect which Mr. Welch noted in his earlier work exists and is due to the formation of chromium disilicide $CrSi_2$. It is the benefit afforded by the diode junctions formed from $CrSi_2$, in conjunction with a facilitating device geometry, which the present method utilizes to produce MOSFETs in an economical and simple way. The minimal number of steps in the process also provides for enhanced yield of devices per substrate processed.

DISCLOSURE OF THE INVENTION

A single mask and etch procedure for fabrication of MOSFETs is achieved by taking advantage of the diode properties of $CrSi_2$ formed when chromium is annealed in contact with silicon at temperatures between 300° C. and 900° C. The preferred method of putting chromium and silicon in contact with each other is vacuum deposition. The method involves the growth of SiO_2 on a silicon substrate to a depth of approximately 2000Å (range 500Å to 6000Å), etching a pattern into the SiO_2 and depositing chromium on the surface thereof. If the chromium depth is limited to about 600Å, (e.g. approximately 0.33 times the depth of the SiO_2), then the chromium layer will be discontinuous. That is, the chromium deposited on top of the SiO_2 will not be in contact with that directly on the silicon. Annealing the resultant system results in the formation of diode junctions in the regions where the chromium contacts the silicon, but not in the regions where SiO_2 separates the chromium from the silicon.

The invention herein utilizes the above disclosed facts in conjunction with a clever device geometry, which is formed by etching SiO_2, to form MOSFET transistors. Additional steps can include the use of ion implantation to adjust threshold voltages, or to adjust source and drain junction geometry. If such ion implantation step(s) are performed, then ion activating anneal step(s) are also added. In the case of boron implantation the activating anneal temperature is approximately 900° C. Thus, it is preferable to perform any ion implant and activating anneal prior to the deposition of chromium, although it is possible to do one combined ion activating, $CrSi_2$ forming anneal.

The starting substrates can be N or P type (typically N type), doped at between $10^{13}/cm^3$ to $10^{18}/cm^3$, of any crystal orientation, but typically <100>, or possibly amorphous.

A variation of the basic method includes an etch into the silicon directly following the SiO_2 etch. This serves to deepen the surface topology depth change, between the top of the SiO_2 and the new surface of the silicon. The result makes it possible to increase the depth of the chromium deposited while still achieving discontinuity of the metal layer.

Other embodiments allow for a second oxide etch, the purpose being to allow production of a lower capacitance gate pad region, and/or a chromium etch which will serve to delineate device regions if the metal depth becomes too great to allow discontinuity.

The primary objective of the present invention is to provide a means for the fabrication of MOSFETs by an economical easy to practice process. The method relies on the properties of chromium when annealed in contact with silicon, and the fact that a discontinuous metal layer can be achieved when chromium is vacuum deposited onto a substrate, the surface of which has had SiO_2 grown thereon, and etched. The process also relies on the geometry of the SiO_2 etch. Said geometry providing for automatic delineation of the source and drain regions, and for the location of a gate between the drain and source regions, as well as pads for contacting the source, drain and gate.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a side elevational view of a silicon substrate with SiO_2 shown on top thereof.

FIG. 2A shows a top view of a MOSFET prior to deposition of chromium but after an SiO_2 etch.

FIG. 2B shows a side elevational view of a MOSFET prior to chromium deposition but after a SiO_2 and Si etch, which side view is taken at the location a—a on FIG. 2A.

FIG. 2C shows a side elevational view of a MOSFET prior to chromium deposition but after an SiO_2 and Si etch, which side view is taken at the point b—b on FIG. 2A.

FIG. 2D shows a side elevational view of a MOSFET after chromium is deposited to a depth of approximately 0.33 times the distance from the top of the SiO_2 to the Si. Note that the chromium on the SiO_2 is not continuous with that on the Si.

FIG. 3 shows a top view of a MOSFET upon which chromium has been deposited to a depth such that it is continuous but then has been subjected to an anneal and a source, drain and gate delineation etch.

BEST MODES FOR CARRYING OUT THE INVENTION

Referring now to FIG. 1, a silicon substrate (1) is shown in side view, upon which has been grown approximately 2000Å of SiO_2 (2), (range 500Å to 6000Å). The substrate can be doped between $10^{13}/cm^3$ to $10^{18}/cm^3$, but typically $10^{15}/cm^3$, and can be of any crystal orientation, but typically <100>. Amorphous silicon might also be used.

After the SiO_2 is grown, masks developed by standard photolithographic techniques are used in conjunction with standard photo resists and etchants, to etch a pattern in the SiO_2, as indicated in FIGS. 2A, 2B and 2C. Note that after the SiO_2 is etched, the silicon can also be etched to deepen the topology depth change, (e.g. see FIGS. 2B and 2C). After the etch, oxide remains only in the gate pad (6), channel (7), and device separation (3) areas. FIGS. 2A and 2B also show the pad regions, but no oxide remains in said areas.

At this point in the process ion implantation can be performed to set the eventual device's gate threshold voltage point, or to adjust the substrate bulk region junction geometries. Prior to the vacuum deposition of chromium to a depth of approximately 0.33 times the topology depth change distance of the etched SiO_2, (or the combined depth of the etched SiO_2 and the etched silicon), an anneal can be performed to place the implanted ions onto substitutional sites.

The next step is to vacuum deposit chromium (10) on the surface of the silicon substrate to a depth no more than that which causes the metal upon the remaining SiO_2, to be discontinuous with the chromium on the silicon in the source and drain regions, which were opened during the prior etching, (e.g. see FIG. 2D). An anneal at between 300° C. and 900° C., (typically 550° C.), is then performed to cause formation of $CrSi_2$ in the source (5) and drain (4) regions and the resultant diode junctions.

An educated observation of FIGS. 2A, 2B, 2C and 2D will show that, an operable MOSFET transistor will exist, and can be probed in the pad regions (4), (5), and (6), and tested or used.

A second embodiment involves a process similar to that already described, but provides for the presence of a deeper gate oxide. The deeper oxide serves to reduce gate capacitance. In the above process, at the point where the oxide is grown, approximately 5000Å of oxide (range of 1000Å to 6000Å), is grown, rather than the typically 2000Å. An etch is then performed to remove all of the SiO_2, except that in the gate-pad-to-be region (6), and in the device seperation (3) region. Next, an oxide growth is effected to a depth of approximately 800Å, (range 500Å to 2000Å), and then the process is continued as described above.

A third embodiment involves an additional step which can be added to either of the above two embodiments. FIG. 3 demonstrates the extra step, which is the performance of a chromium etch, to delineate the final device metalization, if the metal was deposited to a depth too great, and it is present in a continuous fashion over the entire surface of the substrate. The chromium etch then, serves to delineate the source (5), drain (4) and gate pad (6), and gate (7) regions, and to delineate the devices (3).

It is to be understood that this disclosure describes steps which are presented in a definite order. This is not to be taken to mean that some variation in the order of the steps is beyond the scope of the invention. The optional ion implantation might be carried out after the metal deposition, for instance. The focus of the invention is in the use of the self defining device source, drain and gate regions, and in the use of the discontinuous metalization, and in the use of chromium as the metal. The later is the primary factor which makes the process workable. It is only because $CrSi_2$ forms when annealed in contact with silicon, and because $CrSi_2$ forms a usable diode junction with silicon that the present method is possible. The use of aluminum, for instance, which is the typical transistor metalization metal, leads to the formation of a eutectic combination of the aluminum and the silicon when annealed, and does not provide a probable metal in contact with a diode junction in the bulk of the substrate, if it is used in the present invention method. It is the surprising formation of a probeable metalized junction, in the above disclosed method which is the focus of the present invention.

The devices formed by the one mask and etch process will have channel lengths as short as photolithographic techniques will allow. Also, the resultant drain-source voltage curves will be flat as a result of the step nature of the diode junction formed, and because the silicon will be effectively more highly doped than will be the chromium, hence, the space charge region will extend primarily into the chromium as the drain-source voltage is increased.

It must be pointed out the the Figures present representative geometry. Any pattern which surrounds a source region with a gate oxide, and provides self arranged source, drain and gate regions, is to be considered equivalent.

Having hereby disclosed the subject matter of this invention, it should be obvious that many modifications, substitutions, and variations of the present invention are possible in light of the teachings. It is therefore to be understood that the invention may be practiced other than as specifically described, and should be limited in breadth and scope only by the claims.

I claim:

1. A single mask/etch method for fabricating MOSFETs comprising:

selecting a silicon substrate;

growing SiO_2 on top of the silicon substrate to a depth appropriate for use as channel oxide under a gate;

etching the SiO_2 to the silicon to form a pattern comprising a source region surrounded by channel and gate SiO_2, which channel and gate SiO_2 is surrounded by a drain region, which drain region is surrounded by a device delineating SiO_2;

depositing chromium to a depth just under that which would cause the chromium on the SiO_2 to be continuous with that on the silicon in the etched source and drain regions so that the resulting metalization is discontinuous; and

annealing the resulting system so that junctions form in the source and drain regions between the deposited chromium and the silicon in the source and drain regions.

2. A single mask etch method for fabricating MOSFETs as in claim 1, in which an additional silicon etch is performed directly following the SiO_2 etch, the same pattern being etched into the silicon as was etched into the SiO_2 so that the depth between the top of the SiO_2 and the silicon is increased.

3. A two mask/etch method for fabricating MOSFETs comprising:

selecting a silicon substrate;

growing SiO_2 on top of the silicon substrate to a depth appropriate for use as channel oxide under a gate;

etching the SiO_2 to form a pattern comprising a source region surrounded by channel and gate SiO_2, which channel and gate SiO_2 is surrounded by a drain region, which drain region is surrounded by a device delineating SiO_2;

depositing chromium to a depth sufficient to form a continuous metalization over the entire surface of the etched silicon substrate;

annealing the resulting system so that junctions form in the source and drain regions between the deposited chromium and the silicon; and

etching the resulting system to delineate the source, gate-channel and drain regions.

4. A two mask/etch method of fabricating MOSFETs as in claim 3 in which an additional silicon etch is performed directly following the SiO_2 etch, the same pattern being etched into the silicon as was etched into the SiO_2 so that the depth between the top of the SiO_2 and the silicon is increased.

* * * * *

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Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D. C. 20231

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OMAHA, NE 68124

DATE MAILED
01/23/91

127786

MAINTENANCE FEE STATEMENT

The data shown below is from the records of the Patent and Trademark Office. If the maintenance fees and any necessary surcharges have been timely paid for the patents listed below, the notation "PAID" will appear in column 10, "status" below.

If a maintenance fee payment is defective, the reason is indicated by code in column 10, "status" below. An explanation of the codes appears on the reverse of the Maintenance Fee Statement. TIMELY CORRECTION IS REQUIRED IN ORDER TO AVOID EXPIRATION OF THE PATENT. NOTE 37 CFR 1.377. THE PAYMENT(S) WILL BE ENTERED UPON RECEIPT OF ACCEPTABLE CORRECTION. IF PAYMENT OR CORRECTION IS SUBMITTED DURING THE GRACE PERIOD, A SURCHARGE IS ALSO REQUIRED. NOTE 37 CFR 1.20(k) and (l).

If the statement of small entity status is defective the reason is indicated below in column 10 for the related patent number. THE STATEMENT OF SMALL ENTITY STATUS WILL BE ENTERED UPON RECEIPT OF ACCEPTABLE CORRECTION.

M R	PATENT NUMBER	FEE CDE	FEE AMOUNT	SUR CHARGE	SERIAL NUMBER	PATENT DATE	FILE DATE	PAY YR	SML ENT	STAT
	4,696,093	273	415	----	06/872,147	09/29/87	06/09/86	04	YES	PAID

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
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75N4/0331

JAMES D. WELCH
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ITM NBR	PATENT NUMBER	FEE CDE	FEE AMOUNT	SUR CHARGE	SERIAL NUMBER	PATENT DATE	FILE DATE	PAY YR	SML ENT	STAT
1	4,696,093	284	965	----	06/872,147	09/29/87	06/09/86	08	YES	PAID

JAMES D. WELCH
ATTORNEY AT LAW
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402-391-4448

10328 PINEHURST AVE.
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October 15, 1993

Administered for DOE
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DOE Project Officer
Anne Scheer
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911 Walnut, 14th Floor
Kansas City, MO 64106

U.S. Department of Energy
Department of the Controller
Payments Management Branch
P.O. Box 500
Germantown, MD 20784

RE: QUARTERLY AND FEDERAL CASH TRANSACTIONS REPORT.
FEDERAL GRANT NO.: DE-FG47-93R701314.

Dear Sirs;

Please find enclosed the identified documents.

Sincerely,

JAMES D. WELCH
JW/hs
ENC.

QUARTERLY REPORT

RE: FEDERAL GRANT NO. DE-FG47-93R701314.
COORDINATOR: JACK AELLEN.
TO: JAMES D. WELCH, SOLE PROPRIETOR.
FROM: U.S. DEPARTMENT OF ENERGY, ENERGY RELATED INVENTIONS.
PROJECT: NOVEL METHOD FOR MAKING SEMICONDUCTOR CHIPS.

INVENTION NO: 534
OERI NO: 012693

FOR PERIOD BEGINNING: JULY 7, 1993
AND ENDING: OCTOBER 7, 1993

TASK 1. PRELIMINARY

AS PER THE WORK PLAN, THE FIRST THREE MONTHS WERE USED TO OBTAIN ACCESS TO THE UNIVERSITY, ORDER SUPPLIES AND BECOME FAMILIAR WITH EQUIPMENTS, PROFESSORS AND OTHER RESOURCES AT THE UNIVERSITY ETC. THIS TASK HAS BEEN ESSENTIALLY COMPLETED.

UNIVERSITY ACCESS WAS EASILY ACHIEVED UNDER THE PRE-EXISTING CONTRACT. THE ONLY PROBLEM WHICH DEVELOPED WAS THAT THE UNIVERSITY REQUIRED LIABILITY INSURANCE TO COVER MY USE OF THEIR EQUIPMENTS. SAID INSURANCE COST $1081.00. THIS WAS PAID BY SHIFTING FUNDS FROM MY SALARY TO UNIVERSITY ACCESS. A NOTICE OF THIS WAS SENT TO KANSAS CITY FOR ENTRY INTO MY FILE. I HAVE BEEN PROVIDED A DESK IN THE ELECTRICAL ENGINEERING DEPARTMENT CHAIRMAN'S LAB AS A LOCATION FROM WHICH TO WORK.

INITIAL SUPPLIES WERE ORDERED AND RECEIVED WITHOUT ANY REAL DIFFICULTY.

ONE PROBLEM IS THAT A SUITABLE GRADUATE STUDENT ASSISTANT WHO WANTED TO WORK ON THE PROJECT WAS NOT IDENTIFIED.

IN ADDITION, THE ELECTRON BEAM EVAPORATOR WHICH I WAS TO USE TO PERSONALLY, WITH A GRADUATE STUDENT, DEPOSIT CHROMIUM AND ALUMINUM ON TO SILICON, HAS PROVEN TO BE IN NEED OF SOME REPAIR. IT PRESENTLY WILL NOT PROVIDE THE REQUIRED LEVEL OF VACUUM. IT WILL PROBABLY BE USABLE SOON, BUT IS NOT AS OF THIS DATE.

AS A RESULT OF THE ABOVE, I HAVE ARRANGED TO PAY FOR ACCESS TO A UNIVERSITY OF NEBRASKA ASSOCIATE RESEARCH PROFESSOR WHO DOES METAL DEPOSITIONS AS A FULL TIME OCCUPATION, AND WHO WORKS ON A SUPERIOR EVAPORATOR SYSTEM AT THE UNIVERSITY, (WHICH SYSTEM I AM NOT ALLOWED TO PERSONALLY OPERATE), TO DO MY CHROMIUM AND ALUMINUM DEPOSITIONS. THE RESEARCH PROFESSOR'S TIME WILL BE BILLED AT $30.00 PER HOUR. THE FUNDS EARMARKED FOR THE GRADUATE

STUDENT IN THE WORK PLAN WILL BE REDIRECTED TO THAT END USE. IT IS EMPHASIZED THAT THE RESEARCH PROFESSOR WILL BE DOING THE SAME WORK WHICH WAS EARMARKED FOR A GRADUATE STUDENT TO PERFORM, BUT BY GOING THE NEW ROUTE, I WILL BE ACCESSING SUPERIOR TALENT AND EQUIPMENT. IT IS MENTIONED THAT THE AVAILABILITY OF THE SUPERIOR EQUIPMENTS HAS LED TO IDENTIFICATION OF AN INNOVATION POSSIBILITY WHICH WAS COMMUNICATED TO THE INTELLECTUAL PROPERTY COUNCIL OF THE DOE IN CHICAGO RECENTLY, WHEN A DISCLOSURE DOCUMENT DISCLOSING SAME WAS SENT TO THE PATENT OFFICE.

I AM NOW READY TO BEGIN TASK 2, WHICH WILL INVOLVE INITIAL RESEARCH WORK IN THE FORM OF ATTEMPTING TO PRODUCE RECTIFYING JUNCTIONS BETWEEN BOTH N AND P-TYPE SILICON AND CHROMIUM. THE NEXT QUARTERLY REPORT, IF ALL GOES WELL, WILL CONTAIN CURVE TRACER RESULTS WHICH PRESENT THE RECTIFYING PROPERTIES OF JUNCTIONS DEVELOPED. THE FIRST CHROMIUM AND ALUMINUM DEPOSITIONS ARE SCHEDULED TO BE CARRIED OUT IN THE NEAR FUTURE.

I WILL ALSO MENTION THAT I AM TAKING A COURSE IN SOLAR CELLS UNDER DEPARTMENT CHAIRMAN, PROFESSOR SOUKUP. THIS IS SERVING TO REFRESH MY KNOWLEDGE OF SOLID STATE DEVICES AND SO FAR THIS EFFORT IS GOING VERY WELL. AFTER THE YEARS OF BEING AWAY FROM FORMAL EDUCATION IN ELECTRICAL ENGINEERING I FIND I AM STILL ABLE TO SUCCESSFULLY COMPETE IN THAT ARENA.

I AM AT THE UNIVERSITY MONDAYS, WEDNESDAYS AND FRIDAYS.

A QUARTERLY CASH TRANSACTIONS REPORT IS ENCLOSED WITH THIS QUARTERLY REPORT. UNUSED FUNDS FOR ADDITIONAL SUPPLIES AND FOR A GRADUATE STUDENT HAVE BEEN DEPOSITED IN UNIVERSITY ACCOUNTS FOR DISBURSMENT AS REQUIRED, (I MUST PROCURE THROUGH THE UNIVERSITY AS SUPPLY SOURCES WILL NOT SELL DIRECTLY TO ME AND THE RESEARCH PROFESSOR IS PAID THROUGH A UNIVERSITY ACCOUNT). ALSO, APPROXIMATELY $1000.00 EARMARKED FOR PROFESSOR CONSULTATION, WHICH WAS RECENTLY RECEIVED, WAS NOT DISBURSED BY THE END OF THE QUARTER. ALL OTHER FUNDS RECEIVED HAVE BEEN EXPENSED AS INDICATED IN THE WORK PLAN. FUNDS IN THE UNIVERSITY ACCOUNTS WILL BE EXPENSED SHORTLY AS INDICATED THEY WOULD BE IN THE WORK PLAN. IN PARTICULAR, UNUSED FUNDS IDENTIFIED IN THE WORK PLAN FOR A GRADUATE STUDENT WHICH ARE PRESENTLY IN A UNIVERSITY ACCOUNT, AND WHICH WILL BE USED TO OBTAIN CHROMIUM AND ALUMINUM DEPOSITIONS AS DESCRIBED ABOVE, WILL BE USED VERY SHORTLY.

IN SUMMARY, INITIAL SUPPLIES ARE ON SITE AND WORK IS PROCEEDING ON SCHEDULE. THE MINOR CHANGES FROM THE ORIGINAL WORK PLAN HAVE BEEN DICTATED BY FACILITY, PERSONNEL AND EQUIPMENTS AVAILABILITY, AND BY A DESIRE TO ACCESS THE BEST POSSIBLE EXPERTISE AND CAPABILITY AVAILABLE.

SINCERELY,

JAMES D. WELCH

JW/hs
ENC.

JAMES D. WELCH
ATTORNEY AT LAW
PROFESSIONAL ENGINEER

NTELLECTUAL PROPERTY
402-391-4448

10328 PINEHURST AVE.
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January 30, 1994

Administered for DOE
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DOE Project Officer
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U.S. Department of Energy
Department of the Controller
Payments Management Branch
P.O. Box 500
Germantown, MD 20784

RE: QUARTERLY AND FEDERAL CASH TRANSACTIONS REPORT.
FEDERAL GRANT NO.: DE-FG47-93R701314.

Dear Sirs;

Please find enclosed the identified documents.

Sincerely,

JAMES D. WELCH
JW/hs
ENC.

JAMES D. WELCH
ATTORNEY AT LAW
PROFESSIONAL ENGINEER

INTELLECTUAL PROPERTY
402-391-4448

10328 PINEHURST AVE.
OMAHA, NEBRASKA 68124

JANUARY 30, 1994

QUARTERLY REPORT 2

RE: FEDERAL GRANT NO. DE-FG47-93R701314.
COORDINATOR: JACK AELLEN.
TO: JAMES D. WELCH, SOLE PROPRIETOR.
FROM: U.S. DEPARTMENT OF ENERGY, ENERGY RELATED INVENTIONS.
PROJECT: NOVEL METHOD FOR MAKING SEMICONDUCTOR CHIPS.

INVENTION NO: 534
OERI NO: 012693

FOR PERIOD BEGINNING: OCTOBER 7, 1993
AND ENDING: JANUARY 7, 1994

TASK 1. PRELIMINARY

AS PER THE WORK PLAN, THE FIRST THREE MONTHS WERE USED TO OBTAIN ACCESS TO THE UNIVERSITY, ORDER SUPPLIES AND BECOME FAMILIAR WITH EQUIPMENTS, PROFESSORS AND OTHER RESOURCES AT THE UNIVERSITY ETC. THIS TASK HAS BEEN COMPLETED AS REPORTED IN THE FIRST QUARTERLY REPORT.

TASK 2. INITIAL WORK, DIODE FABRICATION.

AS MENTIONED IN THE FIRST QUARTERLY REPORT I WAS, AT THE TIME OF ITS PREPARATION, READY TO BEGIN TASK 2. TASK 2 INVOLVED INITIAL RESEARCH WORK IN THE FORM OF ATTEMPTING TO PRODUCE RECTIFYING JUNCTIONS BETWEEN BOTH N AND P-TYPE SILICON AND CHROMIUM. THE QUESTION TO BE ANSWERED IN TASK 2 WAS WHETHER RECTIFYING JUNCTIONS COULD BE FORMED ON BOTH "N"-TYPE AND "P"-TYPE SILICON BY A SIMULTANEOUS SINGLE TEMPERATURE ANNEAL TO CHROMIUM. THIS QUESTIONED IS NOW ANSWERED IN THE AFFIRMATIVE, FOR THE CASES OF SILICON DOPED TO THE-TO-THE-FORTEENTH AND TEN-TO-THE FIFTEENTH PER CENTIMETER CUBED. THIS QUARTERLY REPORT CONTAINS CURVE TRACER RESULTS OF RECTIFYING JUNCTIONS WHICH HAVE BEEN FABRICATED. FIGURES 1 AND 2 SHOW RESULTS FOR JUNCTIONS FABRICATED ON BOTH "N"-TYPE AND "P"-TYPE SILICON RESPECTIVELY. FIGURES 3 AND 4 SHOW "PROFILOMETER" INDICATIONS OF THE DEPTH OF CHROMIUM DEPOSITED ON THE RESPECTIVE SILICON SUBSTRATES. IT IS TO BE NOTED THAT WE ACHIEVED DEPOSITION OF APPROXIMATELY 2200 ANGSTROMS OF CHROMIUM ON THE "N"-TYPE SILICON SUBSTRATE AND APPROXIMATELY 700 ANGSTROMS ON THE "P"-TYPE SUBSTRATE. WE HAD INTENDED TO APPLY 3000 ANGSTROMS TO BOTH, BUT EQUIPMENT

CALIBRATION, AND CHROMIUM "BURN-OUT" (IE. WE USED THE CHROMIUM UP BEFORE FINISHING THE DEPOSITION---THIS WILL BE AVOIDED IN THE FUTURE BY PROVIDING A BACK-UP SUPPLY IN THE EVAPORATOR), LED TO THE ACTUAL RESULTS ACHIEVED. ACTUALLY, BECUASE RECTIFYING JUNCTIONS WERE ACHIEVED, THE DIFFICULTIES ENCOUNTERED IN THE METAL DEPOSITION PROCEDURE SERVED TO PROVIDE MORE INFORMATION THAN WE WOULD HAVE ACHIEVED HAD THINGS GONE AS PLANNED. WE KNOW THAT 700 ANGSTROMS OF CHROMIUM, (WHICH IS VERY THIN), IS SUFFICIENT TO FORM A RECTIFYING JUNCTION ON "P"-TYPE SILICON. THIS IS SIGNIFICANT BECAUSE AS I MOVE ON INTO TASK THREE THE THINNER THE CHROMIUM WHICH CAN BE UTILIZED THE EASIER IT WILL BE TO FORM THE MOSFETS BY THE DISCONTINUOUS METAL DEPOSITION TECHNIQUE DESCRIBED IN THE WORK PLAN.

IT IS MENTIONED THAT WE HELD THE SILICON SUBSTRATES AT 200 DEGREES CENTIGRADE WHILE DOING THE METAL DEPOSITION, AND PERFORMED A VACUUM ANNEAL AT 350 DEGREES CENTIGRADE FOR FIFTEEN MINUTES PRIOR TO REMOVING THE SUBSTRATES FROM THE EVAPORATOR TO ARRIVE AT THE RECTIFYING JUNCTIONS. I WAS ABLE TO DO THIS IN SUPERIOR EQUIPMENT AVAILABLE TO ME AT SCHEDULED TIMES BY AGREEMENT, WHICH EQUIPMENT IS OPERATED BY A RESEARCH PROFESSOR. THE REASON I AM ACCESSING THIS EQUIPEMENT WAS DESCRIBED IN THE FIRST QUARTERLY REPORT.

THE ONE QUESTION I SEE STILL TO BE RESOLVED REGARDING TASK 2 IS WHAT ANNEAL TEMPERATURE MIGHT BE OPTIMUM TO ACHIEVE OPTIMUM JUNCTION CHARACTERISTICS, (IE. REVERSE BREAKDOWN, LEAKAGE CURRENT AND MINIMUM FORWARD CONDUCTION VOLTAGE). THE REVERSE BREAKDOWN, FOR INSTANCE, OF THE JUNCTIONS RECENTLY FABRICATED WAS A MAXIMUM OF APPROXIMATELY 40 VOLTS. IN WORK I DID AT TORONTO UNIVERSITY IN 1972-74, IN WHICH I USED A 650 DEGREE CENTIGRADE ANNEAL, I OBTAINED AN 80 VOLT REVERESE BREAKDOWN VOLTAGE. AS A RESULT A HIGHER ANNEAL TEMPERATURE APPEARS TO PROVIDE BENEFITS, BUT CAN ALSO SERVE TO DEGRADE CHROMIUM, PARTICULARLY IF NOT PERFORMED IN A VACUUM AMBIENT. METAL DEGRADATION COULD MAKE UTILIZATION THEREOF AS DEVICE GATE DIFFICULT. THE METAL DEPOSITION EQUIPMENT CAN NOT PROVIDE SUCH HIGH ANNEALING TEMPERATURES, BUT A VACUUM SYSTEM WILL BE AVAILABLE SOON WHICH CAN. DETERMINATION OF AN OPTIMUM ANNEALING TEMPERATURE WILL THEREFORE BE INVESTIGATED WHILE PURSUING TASK THREE.

TASK 3. NMOS AND PMOS PRODUCTION.

WITH THE ABOVE IN MIND I HAVE OBTAINED MY FIRST PHOTOLITHOGRAPHIC MASK, AND HAVE DEVELOPED THE ABILITY TO GROW SILICON DIOXIDE AND PERFORM THE PHOTORESIST PROCEDURE I REQUIRE UTILIZING EQUIPMENTS AVAILABLE AT NEBRASKA UNIVERSITY. IN TASK THREE I HOPE TO DEMONSTRATE THE ABILITY TO FABRICATE MOSFETS AS DESCRIBED IN THE WORK PLAN. IT IS MENTIONED THAT I RAN INTO SOME INITIAL TROUBLE ATTEMPTING TO USE PHOTORESIST ALREADY ON SITE. IT STILL WORKS IN RESEARCH OTHERS ARE DOING, BUT HAS AN EXPIRED DATE THEREON. I FOUND IT WOULD NOT WORK WITH THE

RELATIVELY STRONGER HYDROFLUORIC ACID, WHICH IS REQUIRED TO ETCH SILICON DIOXIDE. AS A RESULT I'VE UTILIZED APPROXIMATELY $500.00 OF THE REMAINING SUPPLIES FUNDS TO PURCHASE NEW PHOTORESIST, DEVELOPER, XYLENES, ISOPROPYL ALCOHOL AND A SURFACE ADHESION INCREASING FACTOR AS WELL AS SOME BUFFRED HYDROFLUORIC ACID. THE NEW MATERIALS WORK WELL.

ALSO, I HAVE BEEN ABLE TO SHOW THAT POTASIUM PERMAGNATE (2 PARTS) IN COMBINATION WITH 48% HYDROFLUORIC ACID (1 PART) MIXED IN 5 PARTS DEIONIZED WATER WILL ETCH SILICON ISOTROPICALLY AT A RATE OF APPROXIMATELY 1000 ANGSTROMS IN SEVEN SECONDS. THIS RESULT IS ENCOURAGING FOR APPLICATION TO THE CASES WHEREIN I WILL ETCH INTO THE SILICON IN THE SOURCE AND DRAIN REGIONS AS DESCRIBED IN THE WORK PLAN.

I HAVE ALSO SPOKE WITH PROFESSOR IANNO IN THE ELECTRICAL ENGINEERING DEPARTMENT REGARDING THE POSSIBILITY OF UTILIZING "DRY ETCHING" FACILITIES IN HIS LAB, AS WELL AS USE OF A HIGH TEMPERATURE VACUUM ANNEALING SYSTEM HE IS ASSEMBLING. HE IS AGREEABLE TO WORKING WITH ME. (NOTE THAT PROFESSOR IANNO IS A RECOGNIZED EXPERT IN THE FIELD OF DRY ETCHING, WITH NUMEROUS PAPERS PUBLISHED IN THE AREA). DRY ETCHING USES PLASMA ACTIVATED IONS TO ETCH SILICON DIOXIDE AND SILICON. THE RESULTS ACHIEVABLE BY DRY ETCHING ARE SUPERIOR TO WHAT CAN BE ACHIEVED BY WET ACID ETCHING. THE WALLS OF A DRY ETCHED AREA ARE ESSENTIALLY VERTICAL, (IE. THE ETCH IS ANISOTROPIC), AS COMPARED TO A TAPERED RESULT WHEN WET ACIDS ARE USED. THE STRAIGHT WALLS WOULD BE VERY BENEFICIAL TO MY WORK. I PLAN TO UTILIZE SOME OF THE FUNDS ORIGINALLY EARMARKED FOR A GRADUATE STUDENT TO GAIN ACCESS TO SAID DRY ETCHING FACILITIES AND HIGH TEMPERATURE VACUUM ANNEALING FACILITIES, MUCH AS I HAVE DONE TO GAIN ACCESS TO THE SUPERIOR METAL DEPOSITION EQUIPMENT. IT IS TURNING OUT TO BE A BLESSING THAT I DID NOT FIND A SUITABLE GRADUATE STUDENT TO WORK WITH ME ON THIS PROJECT AS THE EARMARKED FUNDS HAVE BEEN REQUIRED TO GAIN ACCESS TO EQUIPMENTS.

----------RECENT DEVELOPMENT----------

JANUARY 28, 1994

JANUARY 1994 WORK INVOLVING WET ACID ETCHING OF SILICON DIOXIDE AND SILICON, WITH METALIZATION THEN APPLIED AND ANNEALED TO THE RESULTING STRUCTURE, DID NOT PROVIDE A DISCONTINUOUS CHROMIUM METALIZATION AS REQUIRED. CHROMIUM WAS FOUND TO BE PRESENT ON THE EDGES OF THE SILICON DIOXIDE LEADING TO A SHORT BETWEEN SOURCE AND DRAIN REGIONS. A CHROMIUM ETCH WAS ATTEMPTED TO SEE IF THAT WOULD "CLEAN-UP" THE RESULTS, BUT IT DID NOT. MY HOPE WAS THAT THE CHROMIUM ON THE WALLS OF THE SILICON DIOXIDE WAS NOT BE AS DEEP AS CHROMIUM IN THE SOURCE AND DRAIN REGIONS AND ATOP THE SILICON DIOXIDE, THEREBY ALLOWING ITS REMOVAL WHILE LEAVING SUFFICIENT CHROMIUM WHERE REQUIRED. WHAT OCCURED WAS

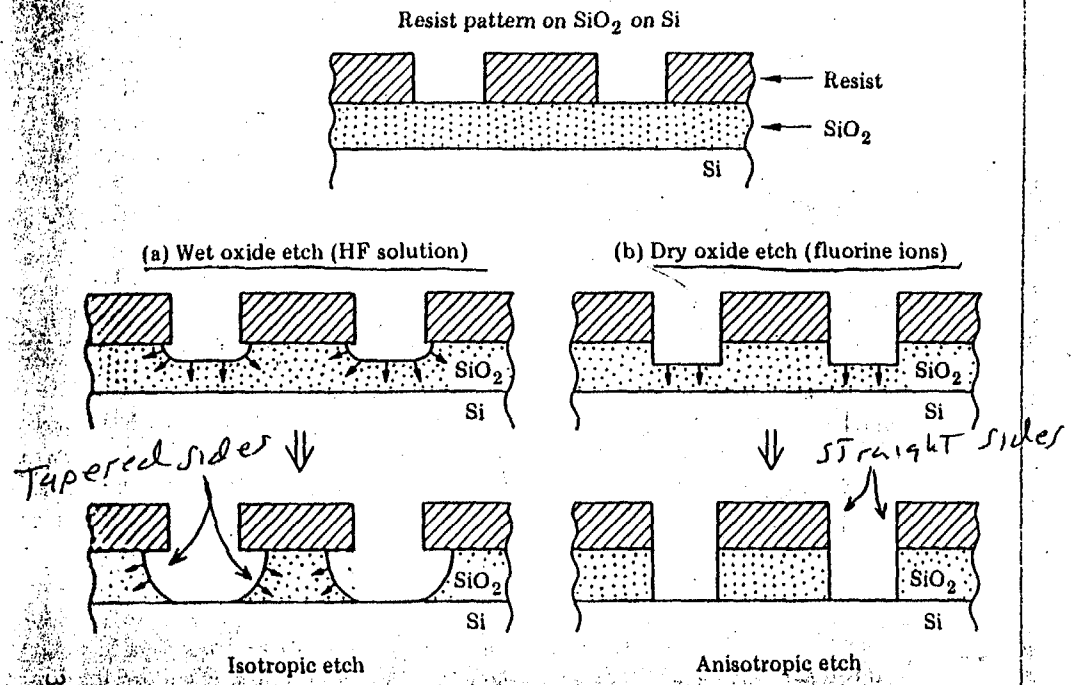


FIGURE 1.11 Formation of grooves in SiO_2 by use of resist patterns and (a) isotropic, wet-etch (HF) solutions or (b) anisotropic, dry-etch (fluorine ion) plasmas.

plasma etching uses fluorine or chlorine ions, which attack SiO_2. Reactive-ion beam etching (RIBE) uses reactive ions, which are accelerated through a potential before bombarding the surface. These dry-etching processes are widely used in integrated-circuit processing. Highly directional, highly anisotropic, etching profiles can be achieved as shown in Fig. 1.11. Straight-wall cuts can be made in oxides or deep grooves formed in the semiconductor as shown for the trench capacitor in Fig. 1.5. Finally, the resist can be removed in a dry process, *resist ashing*, by oxidizing (burning) the resist in an oxygen plasma system.

Lithography, from masks to etches, is a major part of the fabrication of integrated circuits. A complete integrated circuit generally requires between 10 and 20 lithography processing steps. It is a specialized topic, with conferences and books devoted to it, so we will not cover the topic further here except where properties of the electronic materials are directly involved.

1.6 Ingots and Wafers

Integrated circuits originate with the growth of single crystals of silicon and gallium arsenide. The crystals are grown from the melt with the melting temperatures

$$T_m(\text{Si}) = 1414^\circ\text{C} \quad 1430^\circ\text{C}\ ? \qquad (1.12)$$

This is a page from a book titled "Electronic Materials Science" by Mayer & Lau, Macmillan Publishing, 1990; demonstrating the superior results achievable by dry etching of SiO_2.

Dry Etching will be pursued in near term efforts.

First Run Device Fabrication attempt using wet acid (HF) solution was not successful. The oxide edges were very tapered & Chromium accumulated there during deposition. This shorted the Drain & Source.

I Tried wet etching as I could do it myself relatively easily.

$$N_{Si} = \frac{6.022 \times 10^{23} \times 2.33}{28.086} = 4.996 \times 10^{22} \text{ atoms/cm}^3$$

$$= 5 \times 10^{22} \text{ atoms/cm}^3.$$

Therefore, the number of atoms in a device

$$N_{device} = N_{Si} \times \text{volume} \simeq 5 \times 10^{22} \times 10^{-10} = 5 \times 10^{10} \text{ atoms}$$

or

$$\frac{N_{device}}{N_A} \simeq \frac{5 \times 10^{10}}{6 \times 10^{23}} \simeq 10^{-13} \text{ mole (mol) of Si.}$$

The sizes and active volumes of electronic devices in integrated circuits are small. The recurrent goals in the electronic circuit industry are the further reduction in size to increase the packing density and the improvement in the control of process steps to increase the yield of devices. Both the size reduction and process control require knowledge of the properties of electronic materials—the topic of this book. For example, to achieve 1 million bits (1 Mb) in an array, not only is the length between source and drain reduced to less than 1 μm, but the capacitor can be folded into a trench as shown in Fig. 1.5 for a 4-Mb DRAM. Clearly, the fabrication of such devices requires exceptional control.

Such control is achieved by use of vacuum technologies and controlled ambients at various stages in the processing of integrated circuits. In vacuum technology, the basic relation is the ideal gas law:

$$PV = \bar{\nu}RT = N_m kT \qquad (1.3)$$

where P, V = pressure [newtons (N)/m^2] and volume (m^3)
T = absolute temperature, Kelvin (K) (K = °C + 273.16)

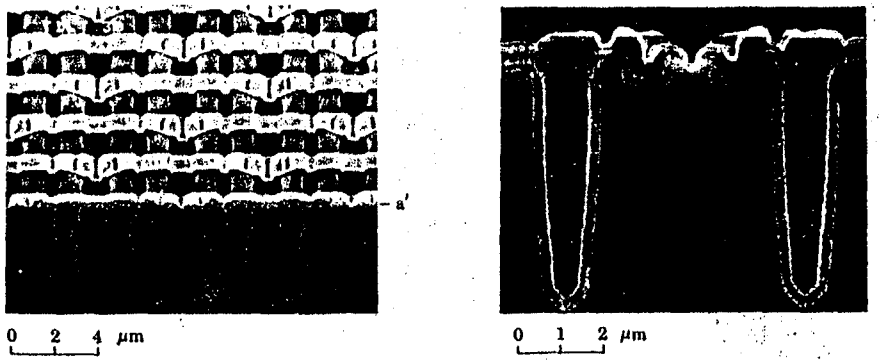


FIGURE 1.5 Scanning electron micrograph of the memory array of a 4-Mb DRAM with 10-μm^2 cell size made with capacitors formed in trenches etched in the silicon. (From K. Nakamura, Nippon Electric Co., Japan.)

From Mayer & Lau

R = gas constant = 8.31 joules (J)/K · mol
k = Boltzmann's constant = R/N_A = 1.38 × 10^{-23}

The Standard International (SI) unit of pressure is N/m^2 (see Table 1.1), also 1 pascal (Pa). The torr is the unit of pressure based on the height of a colu of liquid:

$$1 \text{ torr} = 1 \text{ mm Hg} = 133.3 \text{ N/m}^2$$

and

$$1 \text{ atmosphere (atm)} = 760 \text{ torr} = 1.013 \times 10^5 \text{ N/m}^2.$$

The number of molecules per unit volume at 1 atm and 25°C is

$$\frac{N_m}{V} = \frac{P}{kT} = \frac{1.013 \times 10^5}{1.38 \times 10^{-23} \times 298.16} = \frac{2.46 \times 10^{25}}{\text{m}^3} = 2.46 \times \frac{10^{19}}{\text{cm}^3}$$

In vacuum process technology, vacuums of 10^{-4} Pa (7.5×10^{-7} torr) common, with the number of molecules per unit volume:

$$\frac{N_m}{V} = \frac{P}{kT} = \frac{10^{-4}}{1.38 \times 10^{-23} \times 298.16} = 2.43 \times \frac{10^{16}}{\text{m}^3} = 2.43 \times \frac{10^{10}}{\text{cm}^3}.$$

The average kinetic energy $\bar{E}_k$ of the molecules is

$$\bar{E}_k = \frac{3}{2}\frac{R}{N_A}T = \frac{3}{2}kT = \frac{1}{2}m_m v_a^2$$

where m_m is the mass of the molecular and v_a is the average velocity, and the r_c of molecular collisions per unit area per second is

$$r_c = \frac{N_m}{V}\frac{v_a}{4}.$$

where the factor of 4 is a geometrical correction. At a pressure of 10^{-4} I nitrogen gas (M = molecular weight = 28 g/mol = 28 × 10^{-3} kg/mol) at 2

TABLE 1.1 Common Units and Conversions Used in Pressures and Gases

1 newton · meter (N · m) = 1 joule (J) = 10^7 dyne (dyn) · cm = 10^7 ergs
$1 \frac{\text{N}}{\text{m}^2}$ = 1 pascal (Pa) = 7.5×10^{-3} torr
10^6 N/m^2 = 10.2 kg/cm^2 = 146 lb/in^2 = 146 psi
1 torr = 133.3 N/m^2 = 133.3 Pa
1 atm = 760 torr = 1.013×10^5 N/m^2
1 bar = 10^5 N/m^2 = 750 torr
1 dyn/cm^2 = 0.1 N/m^2

THAT THE CHROMIUM ON THE SILICON "CRACKED" AND LIFTED OFF THE SUBSTRATE, (THIS INDICATES THAT CHROMIUM DISILICIDE HAD NOT FORMED THERE DURING WHAT WE INTENDED TO BE A 415 DEGREE CENTIGRADE VACUUM ANNEAL PERFORMED IN THE METAL DEPOSITION EQUIPMENT), AND CHROMIUM ON THE SILICON DIOXIDE GRADUALLY ETCHED AWAY. OBSERVATION OF THE PRESENTLY FABRICATED STRUCTURES WITH AN OPTICAL MICROSCOPE INDICATED THAT CHROMIUM PRESENT ON THE EDGES OF THE SILICON DIOXIDE IS VERY UNIFORM. ALSO, THE WALLS OF THE SILICON DIOXIDE WERE OBSERVED TO BE VERY TAPERED. A 4300 ANGSTROM, (IE. 3000 ANGSTROM SILICON DIOXIDE PLUS 1400 ANGSTROM ETCH INTO SILICON), VERTICAL DROP CORRESPONDED TO APPROXIMATELY 2.5 MICRONS HORIZONTALLY. THE WET ETCHING APPROACH THUS DOES NOT APPEAR TO PROVIDE SUFFICIENTLY STRAIGHT WALL ETCHING FOR USE IN THE PRESENT WORK. SEE FIGURE 5 FOR A TOP VIEW PHOTO OF A FIRST RUN DEVICE STRUCTURE TAKEN THROUGH AN OPTICAL MICROSCOPE. THE RECTANGULAR SOURCE AND DRAIN REGIONS APPEAR WHITE, WHILE THE OXIDE REGIONS APPEAR DARKER WITH A LIGHTER BORDER THEREAROUND. SAID LIGHTER BORDER IDENTIFIES THE TAPERED EDGE REFERRED TO ABOVE. APPROXIMATELY 1000 ANGSTROMS OF CHROMIUM WAS DEPOSITED AND IS PRESENT ATOP ALL AREAS.

IN VIEW OF THESE RESULTS I WILL, BY NECESSITY, PURSUE THE DRY ETCHING PROCESS IN COORIDINATION WITH PROFESSOR IANNO'S FACILITES.

I AM PROCEEDING WITH THE INTENTION OF SHOWING THAT THE BASIC EFFECTS I REQUIRE TO BE SUCCESSFUL IN THE END GOALS OF MY RESEARCH, ARE ACHIEVABLE. ONCE SHOWN, I WILL STRUCTURE MY EFFORTS TO "FILL-IN" ANY DATA REQUIRED TO BETTER DOCUMENT AND OPTIMIZE THE WORK. THIS REVISED APPROACH IS NECESSARY IN VIEW OF METAL DEPOSITION EQUIPMENT SCHEDULING AND ACCESS, AS WELL AS SCHEDULING AND ACCESS TO THE DRY ETCHING FACILITIES AND HIGH TEMPERATURE (EG. 650 DEGREES CENTIGRADE), VACUUM ANNEALING FACILITIES.

I WILL ALSO MENTION THAT MY COURSE IN SOLAR CELLS UNDER DEPARTMENT CHAIRMAN, PROFESSOR SOUKUP, WENT VERY WELL. I RECEIVED A GRADE OF "--A--". THIS COURSE WAS HEAVY INTO SECOND ORDER DIFFERENTIAL EQUATIONS WITH BESSEL AND ERROR FUNCTION, FOR INSTANCE, SOLUTIONS. I SURPRIZED EVEN MYSELF AT MY ABILITY REGARDING THE MATERIAL AFTER A TWENTY YEAR PERIOD AWAY THEREFROM. WE ALSO USED THE "MAPLE" PROGRAM A GOOD BIT. WHILE I AM NOT EXPERT IN ITS USE, I AM NOW SOMEWHAT "PROFICIENT". AS WELL, WE DID A PROJECT FOR THIS COURSE INVOLVING OPERATION OF THE SCANNING ELECTRON MIOCROSCOPE AND APPLICATION THEREOF TO DETERMINING MINORITY CARRIER DIFFUSION LENGTHS BY THE ELECTRON BEAM INDUCED CURRENT (EBIC) APPROACH. AS A RESULT I AM NOW ABLE TO UTILIZE THE SCANNING ELECTROM MICROSCOPE AND INTEND TO DO SO DURING MY CONTINUING RESEARCH EFFORTS, TO VIEW THE CHROMIUM-SILICON JUNCTIONS GREATLY MAGNIFIED. THIS IS SOMETHING I WOULD NOT HAVE

BEEN ABLE TO DO BUT FOR TAKING THE SOLAR CELL COURSE.

I HAVE ALSO BEEN ABLE TO CARRY-ON WITH THE MORE IMPORTANT ASPECTS OF MY PATENT PRACTICE.

I AM AT THE UNIVERSITY TUESDAYS AND THURSDAYS THIS SEMESTER, AND AT OTHER TIMES WHEN REQUIRED BY SCHEDULING.

A QUARTERLY CASH TRANSACTIONS REPORT IS ENCLOSED WITH THIS QUARTERLY REPORT. IN THE INTEREST OF AVOIDING ADVERSE YEAR END TAX CONSEQUENCES, AND IN VIEW OF THE MINIMIZED EXPENDITURES I HAVE MADE, I DID NOT REQUEST ADVANCES FOR TWO MONTHS RUNNING. I HAVE KEPT JO ANN TIMM IN THE KANSAS CITY FIELD OFFICE ADVISED OF MY APPROACH. I HAVE NOW RESUMED ADVANCE REQUESTS.

IN SUMMARY THERE IS A LOT LEFT TO BE DONE, BUT TO DATE NO ABSOLUTE BLOCKADES TO ACHIEVING THE INTENDED GOALS HAVE DEVELOPED WHICH I COULD NOT, BY ALTERNATIVE APPROACH AND DISCUSSION AND AGREEMENT WITH APPROPRIATE PERSONS, PROPOSE AND PURSUE AVENUES TO OVERCOME. HOPEFULLY THE NEXT QUARTERLY REPORT WILL INCLUDE CURVE TRACER RESULTS ACHIEVED FROM INVESTIGATION OF FABRICATED MOSFETS.

SINCERELY,

JAMES D. WELCH

JW/hs
ENC.

P.S. I AM ENCLOSING SOME PHOTOGRAPHS OF VARIOUS FACILITIES AND EQUIPMENTS I AM UTILIZING. THE PHOTOS OF VARIOUS FACILITES WERE TAKEN BY MY MOM WHEN I TOOK HER ON A TOUR THEREOF DURING THE HOLIDAYS.

I AM ALSO ENCLOSING A COPY OF A RECENT MEMO TO PROFESSOR IANNO WHICH OUTLINES THE PROPOSED NEXT STEPS OF MY RESEARCH IN VIEW OF THE RESULTS OF THE FIRST EFFORTS TO FABRICATE SCHOTTKY BARRIER MOSFETS, WHICH FIRST EFFORTS INVOLVED USE OF WET ACID ETCHANTS TO ETCH SILICON DIOXIDE AND SILICON.

CURVE TRACER CURRENT V. VOLTAGE (I-V) CHARACTERISTICS FOR RECTIFYING JUNCTIONS FORMED BETWEEN TEN-TO-THE-FORTEENTH PER CENTIMETER CUBED P-TYPE SILICON AND CHROMIUM DEPOSITED THEREON, WHILE SAID SILICON WAS HELD AT 200 DEGREES CENTIGRADE. A FIFTEEN MINUTE VACUUM ANNEAL AT THREE-HUNDREED-FIFTY (350) DEGREES CENTIGRADE WAS PERFORMED AFTER THE CHROMIUM DEPOSITION.

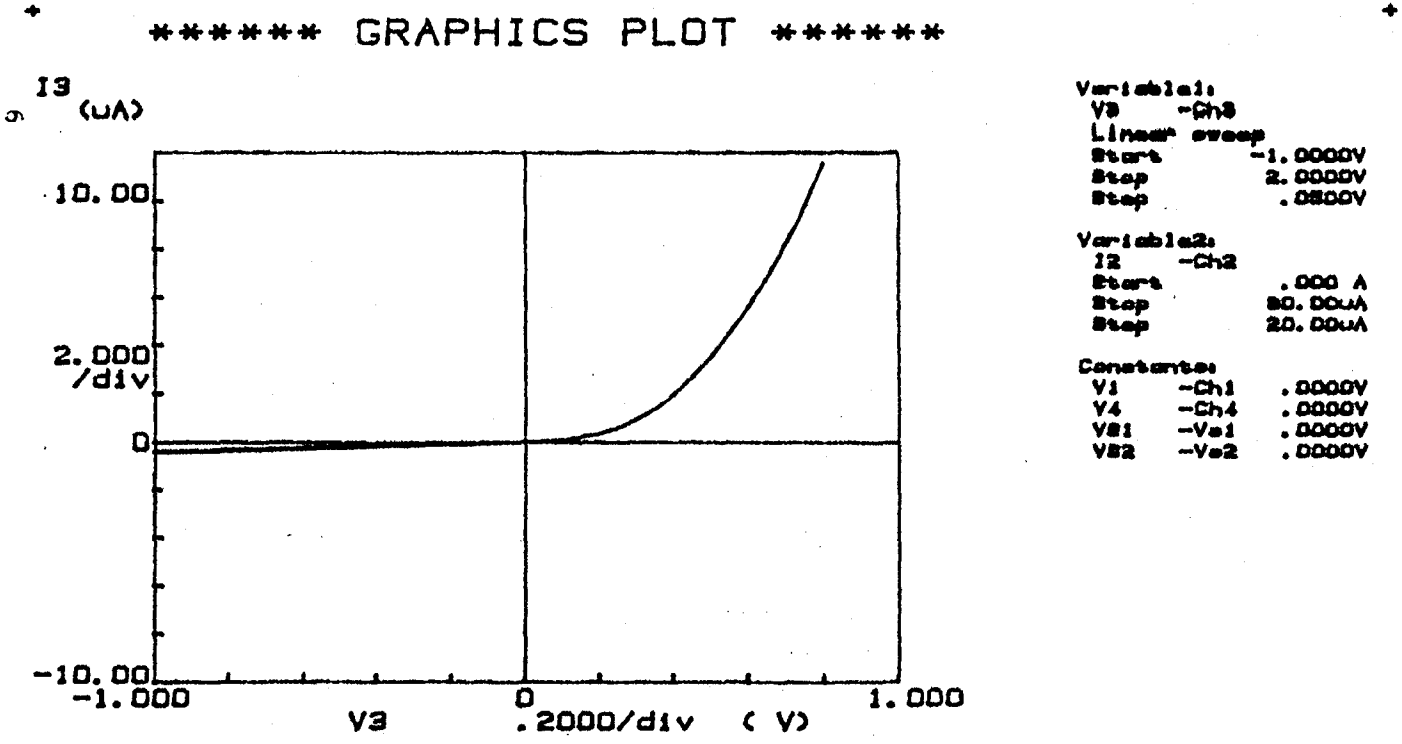


FIG. 1

CURVE TRACER CURRENT V. VOLTAGE (I-V) CHARACTERISTICS FOR RECTIFYING JUNCTIONS FORMED BETWEEN TEN-TO-THE-FIFTEENTH PER CENTIMETER CUBED N-TYPE SILICON AND CHROMIUM DEPOSITED THEREON, WHILE SAID SILICON WAS HELD AT 200 DEGREES CENTIGRADE. A FIFTEEN MINUTE VACUUM ANNEAL AT THREE-HUNDRED-FIFTY (350) DEGREES CENTIGRADE WAS PERFORMED AFTER THE CHROMIUM DEPOSITION.

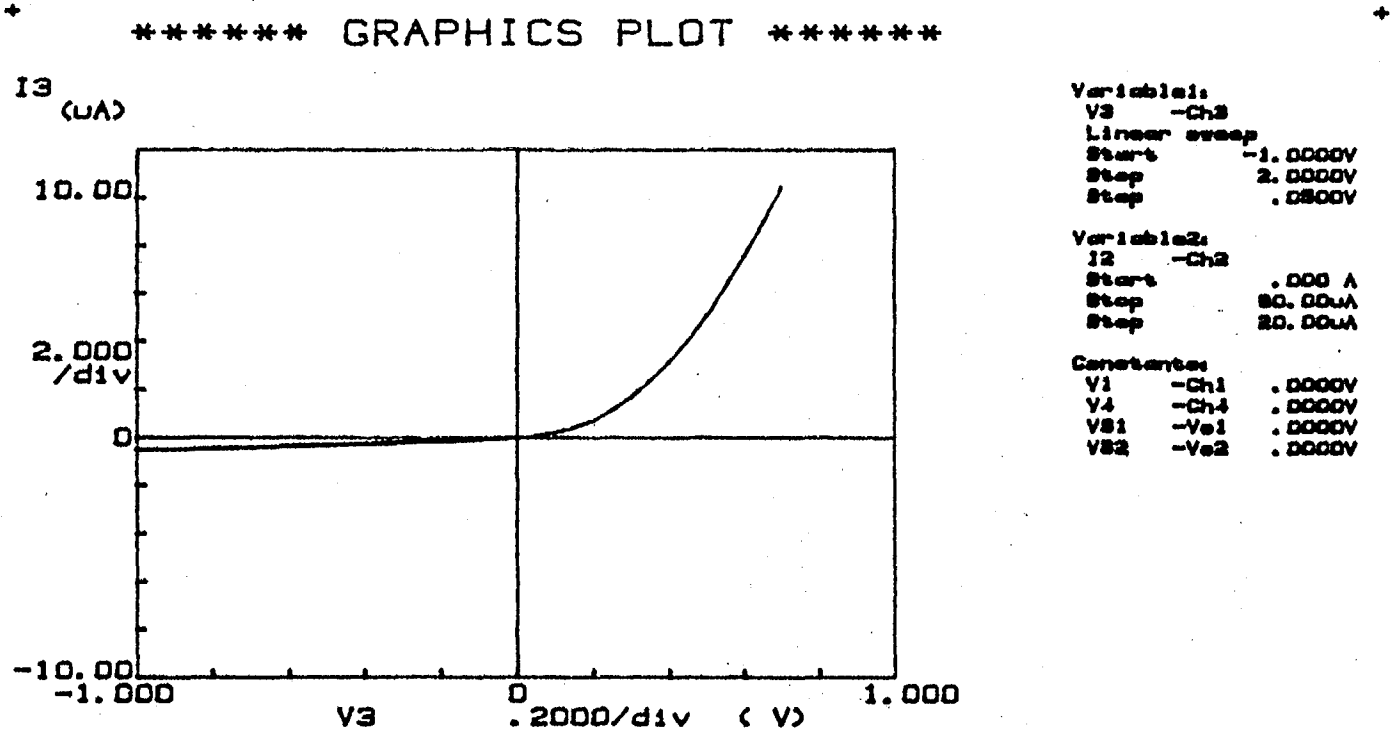
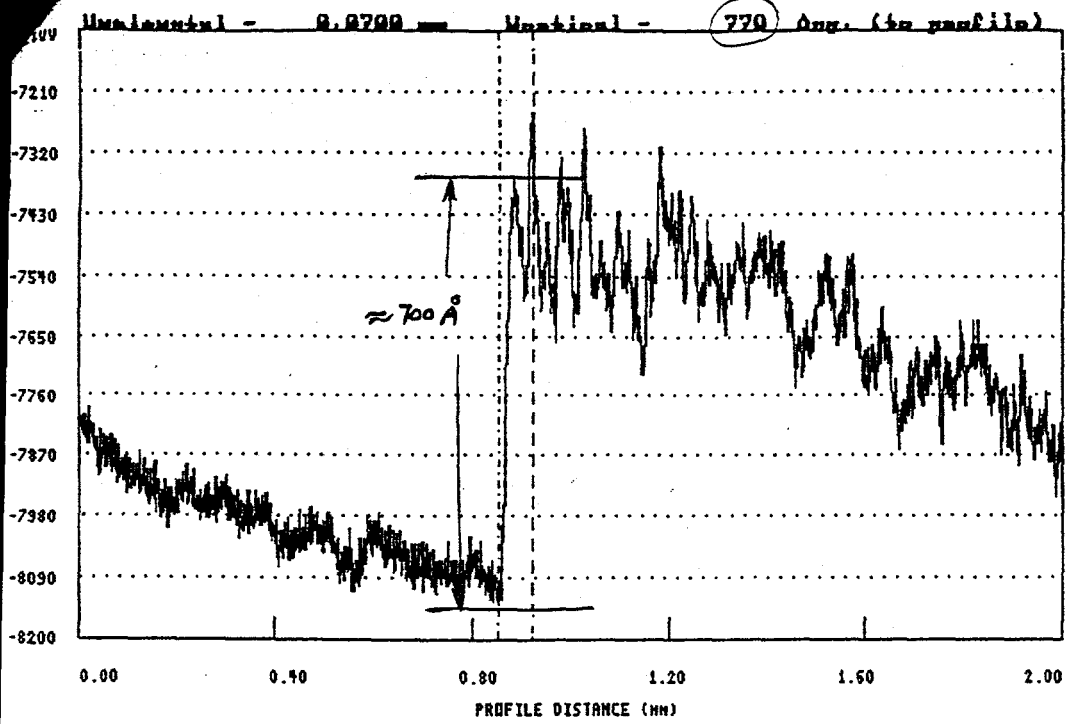
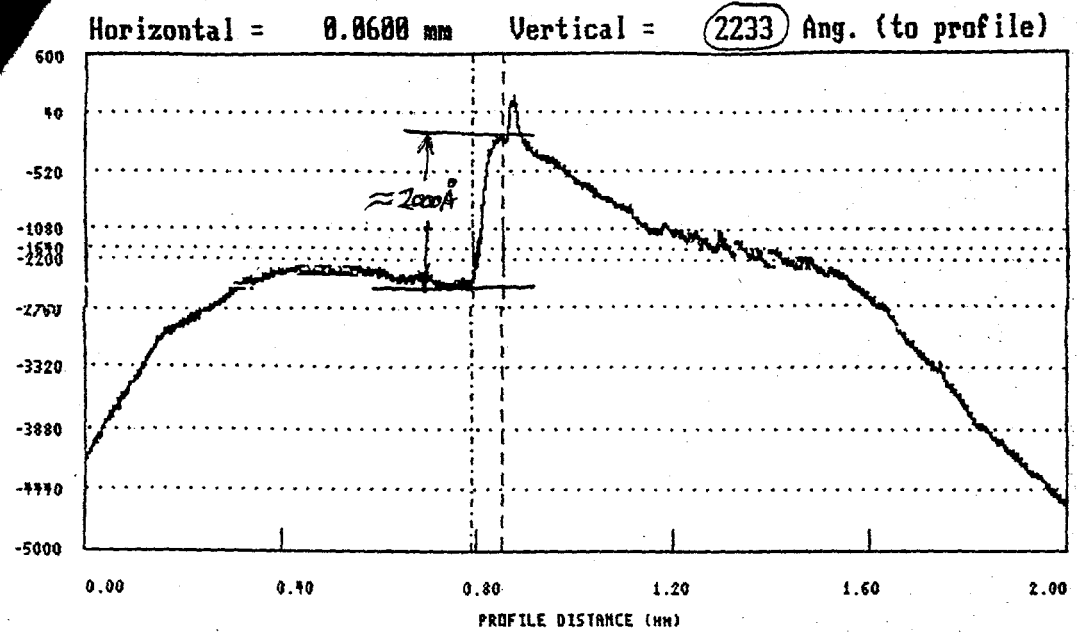


FIG. 2



ROFILOMETER RESULTS SHOWING APPROXIMATELY SEVEN-HUNDRED (700) NGSTROMS OF CHROMIUM WAS DEPOSITED ON THE P-TYPE SUBSTRATE. OTE, THE PROFILOMETER READS ABOUT 5% HIGH.

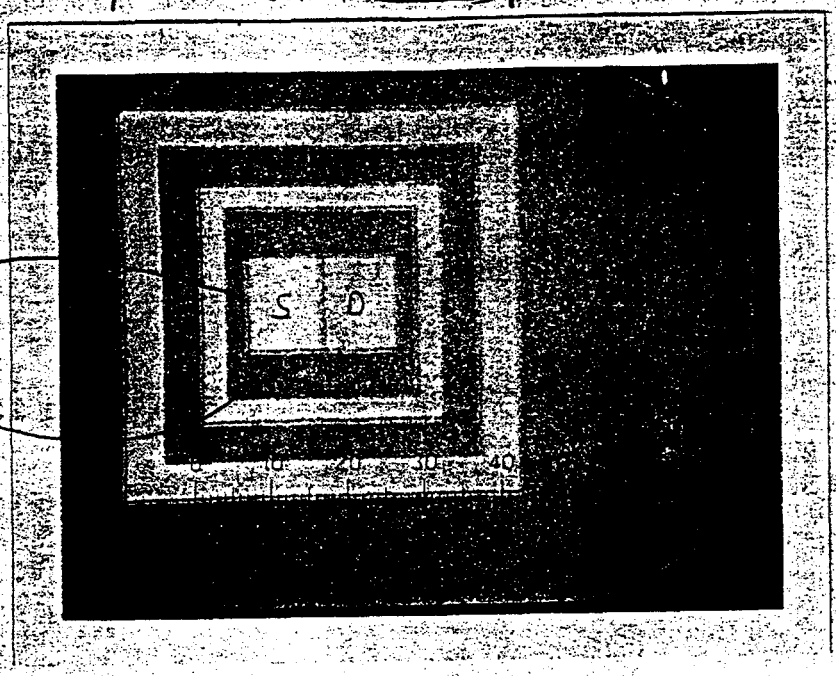
FIG. 3



10^{15} N-Type

PROFILOMETER RESULTS SHOWING APPROXIMATELY TWO-THOUSAND-PLUS (2000+) ANGSTROMS OF CHROMIUM WAS DEPOSITED ON THE N-TYPE SUBSTRATE. NOTE, THE PROFILOMETER READS ABOUT 5% HIGH.

FIG. 4



OPTICAL MICROSCOPE PHOTO OF FIRST RUN DEVICES SHOWING DELINEATION OF SOURCE, DRAIN AND GATE REGIONS. NOTE LIGHTER BORDER AROUND EDGES OF SILICON DIOXIDE INDICATING TAPERED EDGES.

FIG. 5

ATTACHMENTS

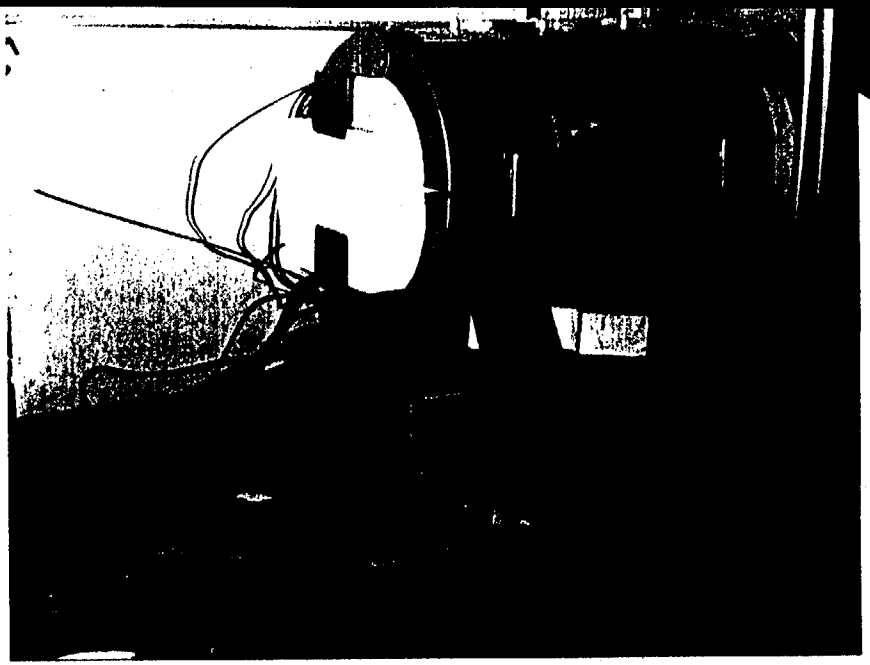
1. SERIES OF PHOTOS SHOWING FACILITIES.

2. MEMO TO PROFESSOR IANNO REGARDING ACCESS TO HIS DRY ETCHING AND HIGH TEMPERATURE VACUUM ANNEALING FACILITIES.

3. COPY OF GRADE REPORT FOR SOLAR CELLS CLASS.

Me entering University

(3)



Furnace
(Oxide Growth)

(2)

Me at my Desk

(4)

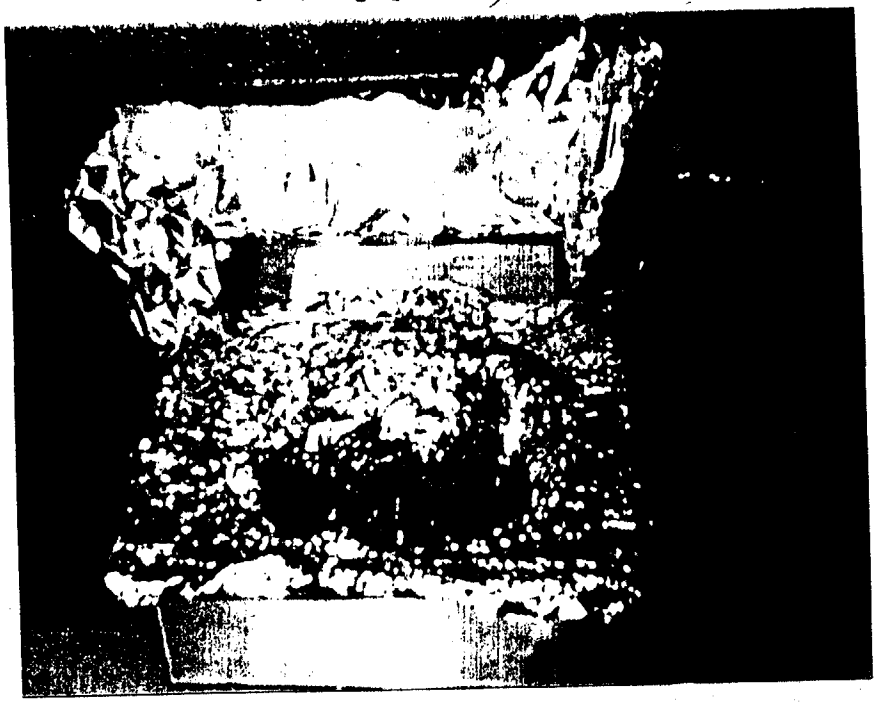
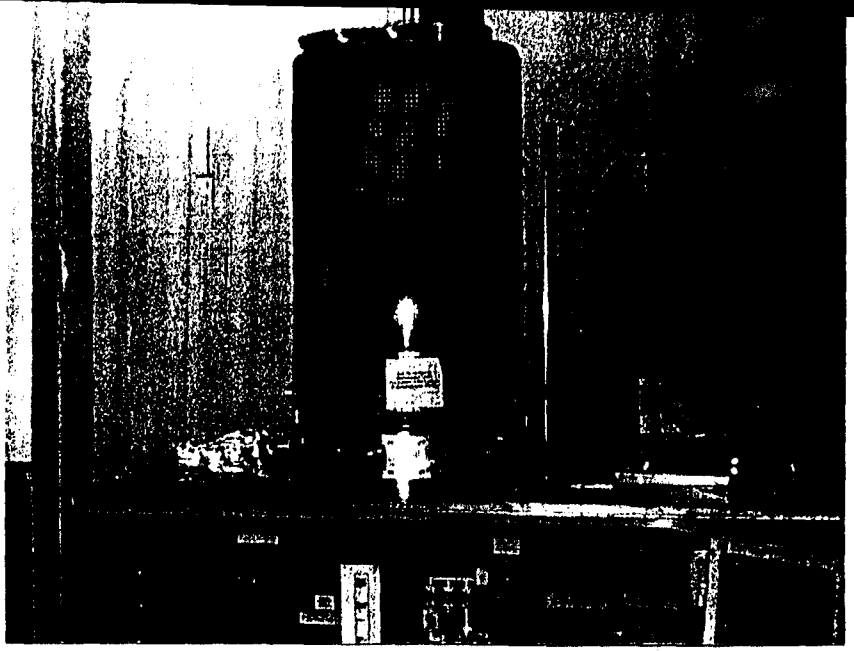


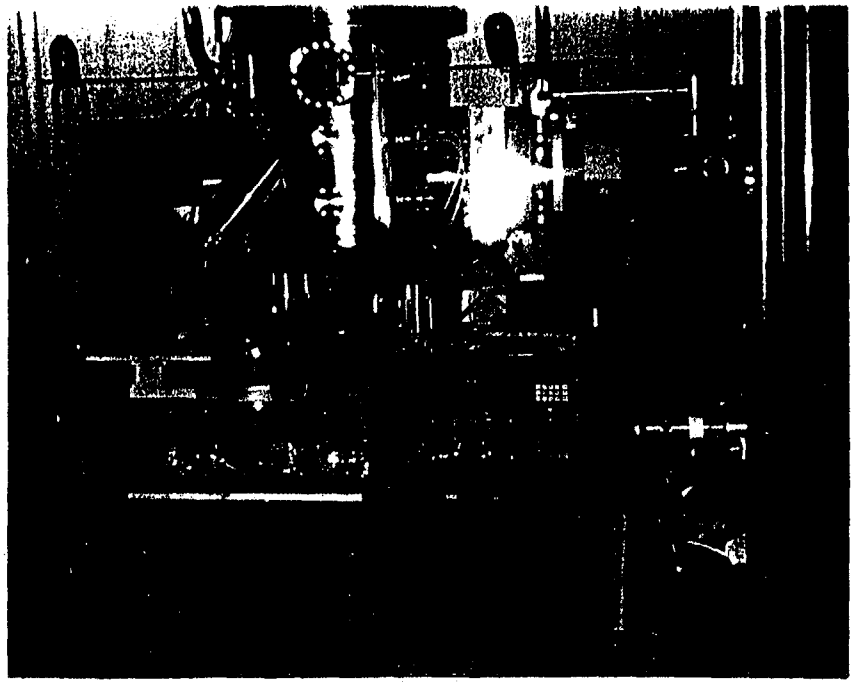
Photo Resist Application



Electron Beam Evaporator

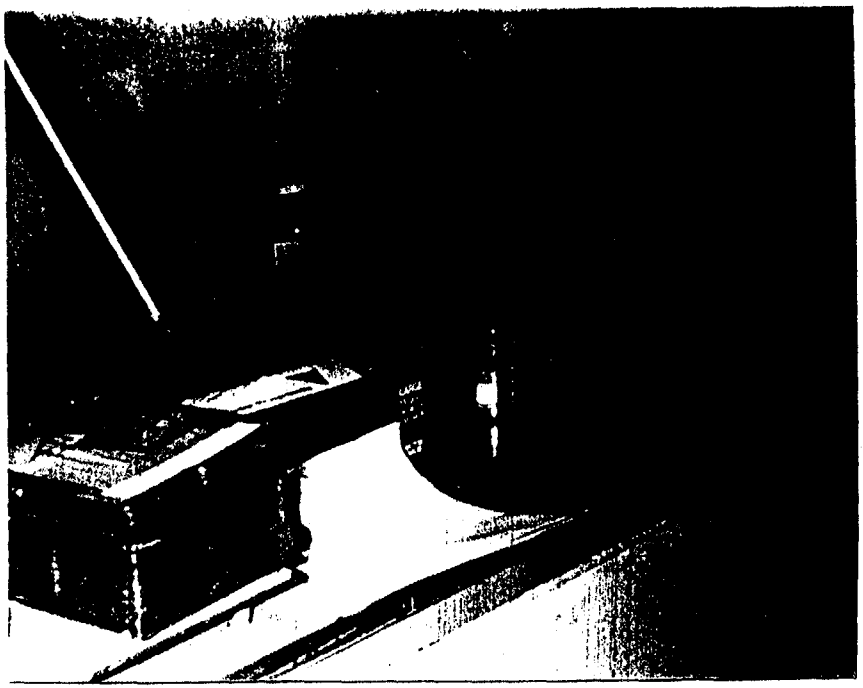
MASK ALLIGNMENT AND PHOTO RESIST EXPOSURE SYSTEM

(6)



Better Electron Beam Evaporator

(8)



Acid Etching Hood

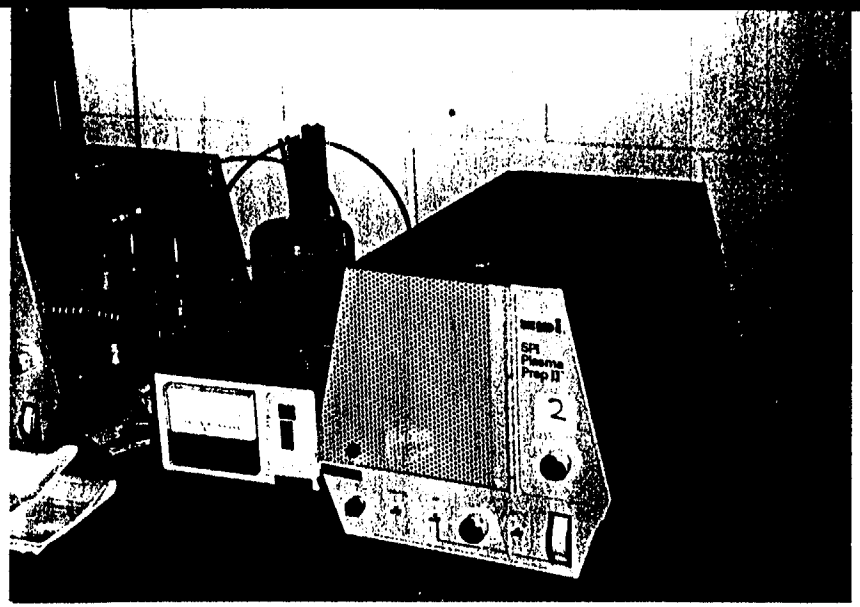
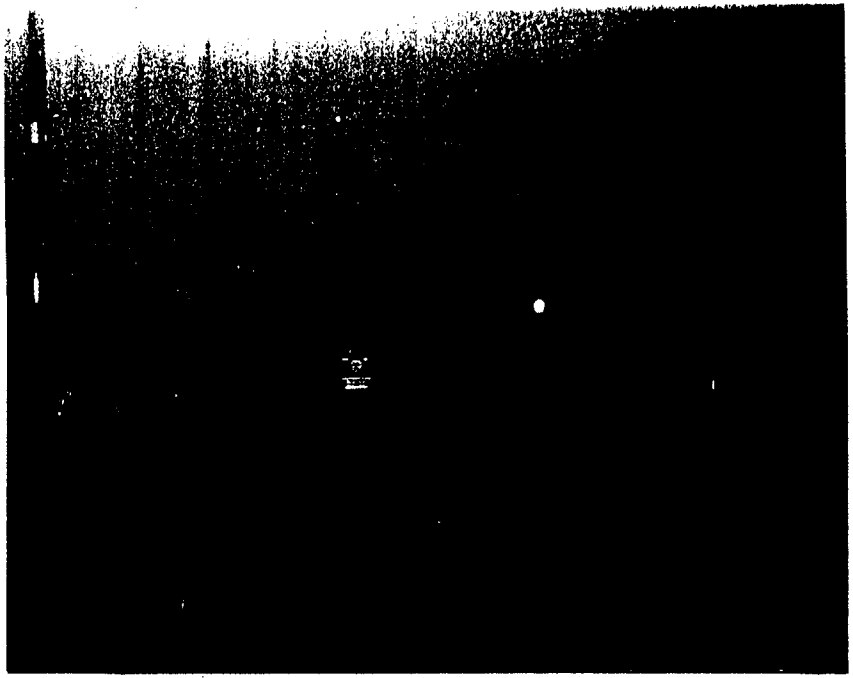


Photo Resist Removing, Asher

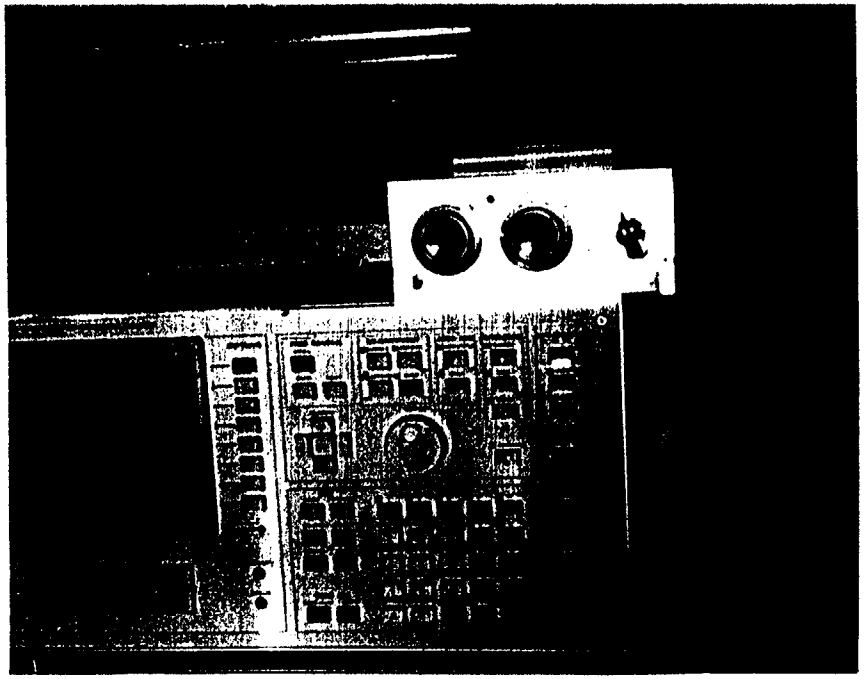
Device Probe Stand

(10)



Profilometer

(12)



Curve Tracer

JAMES D. WELCH
ATTORNEY AT LAW
PROFESSIONAL ENGINEER

TELLECTUAL PROPERTY
402-391-4448

10328 PINEHURST AVE.
OMAHA, NEBRASKA 68124

April 15, 1994

Administered for DOE
Kansas City Support Office
U.S. Department of Energy
911 Walnut, 14th Floor
Kansas City, MO 64106

DOE Project Officer
Anne Scheer
U.S. Department of Energy
911 Walnut, 14th Floor
Kansas City, MO 64106

U.S. Department of Energy
Department of the Controller
Payments Management Branch
P.O. Box 500
Germantown, MD 20784

RE: QUARTERLY AND FEDERAL CASH TRANSACTIONS REPORT.
FEDERAL GRANT NO.: DE-FG47-93R701314.

Dear Sirs;

Please find enclosed the identified documents.

Sincerely,

JAMES D. WELCH
JW/hs
ENC.

JAMES D. WELCH
ATTORNEY AT LAW
PROFESSIONAL ENGINEER

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OMAHA, NEBRASKA 68124

APRIL 15, 1994

QUARTERLY REPORT 3

RE: FEDERAL GRANT NO. DE-FG47-93R701314.
COORDINATOR: JACK AELLEN.
TO: JAMES D. WELCH, SOLE PROPRIETOR.
FROM: U.S. DEPARTMENT OF ENERGY, ENERGY RELATED INVENTIONS.
PROJECT: NOVEL METHOD FOR MAKING SEMICONDUCTOR CHIPS.

INVENTION NO: 534
OERI NO: 012693

FOR PERIOD BEGINNING: JANUARY 7, 1993
AND ENDING: APRIL 7, 1994

TASK 1. PRELIMINARY

AS PER THE WORK PLAN, THE FIRST THREE MONTHS WERE USED TO OBTAIN ACCESS TO THE UNIVERSITY, ORDER SUPPLIES AND BECOME FAMILIAR WITH EQUIPMENTS, PROFESSORS AND OTHER RESOURCES AT THE UNIVERSITY ETC. THIS TASK HAS BEEN COMPLETED AS REPORTED IN THE FIRST QUARTERLY REPORT.

TASK 2. INITIAL WORK, DIODE FABRICATION.

AS MENTIONED IN THE FIRST QUARTERLY REPORT I WAS, AT THE TIME OF ITS PREPARATION, READY TO BEGIN TASK 2. TASK 2 INVOLVED INITIAL RESEARCH WORK IN THE FORM OF ATTEMPTING TO PRODUCE RECTIFYING JUNCTIONS BETWEEN BOTH N AND P-TYPE SILICON AND CHROMIUM. THE QUESTION TO BE ANSWERED IN TASK 2 WAS WHETHER RECTIFYING JUNCTIONS COULD BE FORMED ON BOTH "N"-TYPE AND "P"-TYPE SILICON BY A SIMULTANEOUS SINGLE TEMPERATURE ANNEAL TO CHROMIUM. THIS QUESTIONED IS NOW ANSWERED IN THE AFFIRMATIVE, FOR THE CASES OF SILICON DOPED TO THE-TO-THE-FORTEENTH AND TEN-TO-THE-FIFTEENTH PER CENTIMETER CUBED.

THE ONE QUESTION STILL TO BE RESOLVED REGARDING TASK 2 IS WHAT ANNEAL TEMPERATURE MIGHT BE OPTIMUM TO ACHIEVE OPTIMUM JUNCTION CHARACTERISTICS, (IE. REVERSE BREAKDOWN, LEAKAGE CURRENT AND MINIMUM FORWARD CONDUCTION VOLTAGE). THE REVERSE BREAKDOWN, FOR INSTANCE, OF THE JUNCTIONS RECENTLY FABRICATED WAS A MAXIMUM OF APPROXIMATELY 40 VOLTS. IN WORK I DID AT TORONTO UNIVERSITY

IN 1972-74, IN WHICH I USED A 650 DEGREE CENTIGRADE ANNEAL, I OBTAINED AN 80 VOLT REVERSE BREAKDOWN VOLTAGE. AS A RESULT A HIGHER ANNEAL TEMPERATURE APPEARS TO PROVIDE BENEFITS, BUT CAN ALSO SERVE TO DEGRADE CHROMIUM, PARTICULARLY IF NOT PERFORMED IN A VACUUM AMBIENT. METAL DEGRADATION COULD MAKE UTILIZATION THEREOF AS DEVICE GATE DIFFICULT. THE METAL DEPOSITION EQUIPMENT CAN NOT PROVIDE SUCH HIGH ANNEALING TEMPERATURES, BUT A VACUUM SYSTEM WILL BE AVAILABLE SOON WHICH CAN. DETERMINATION OF AN OPTIMUM ANNEALING TEMPERATURE WILL THEREFORE BE INVESTIGATED WHILE PURSUING TASK THREE.

TASK 3. NMOS AND PMOS PRODUCTION.

AS MENTIONED IN THE SECOND QUARTERLY REPORT, JANUARY 1994 WORK INVOLVING WET ACID ETCHING OF SILICON DIOXIDE AND SILICON, WITH CHROMIUM METALIZATION THEN APPLIED AND ANNEALED TO THE RESULTING STRUCTURE, DID NOT PROVIDE A DISCONTINUOUS CHROMIUM METALIZATION BETWEEN CHROMIUM ATOP THE SILICON DIOXIDE AND THAT IN ETCHED REGIONS WHEREAT SILICON IS UNCOVERED, AS REQUIRED FOR MY RESEARCH TO BE SUCCESSFUL. CHROMIUM WAS FOUND TO BE PRESENT ON THE EDGES OF THE SILICON DIOXIDE LEADING TO A SHORT BETWEEN SOURCE AND DRAIN REGIONS. THE REASON FOR THIS WAS THAT THE SILICON DIOXIDE WALLS WERE SIGNIFICANTLY TAPERED. AS INDICATED IN THE SECOND QUARTERLY REPORT I, AS A RESULT, SPOKE WITH PROFESSOR IANNO IN THE UNL ELECTRICAL ENGINEERING DEPARTMENT REGARDING THE POSSIBILITY OF UTILIZING "DRY ETCHING" FACILITIES IN HIS LAB, AS WELL AS USE OF A HIGH TEMPERATURE VACUUM ANNEALING SYSTEM HE IS ASSEMBLING. DRY ETCHING USES PLASMA ACTIVATED IONS TO ETCH SILICON DIOXIDE AND SILICON. THE WALLS OF A DRY ETCHED AREA CAN BE ESSENTIALLY VERTICAL, (IE. THE ETCH IS ANISOTROPIC), AS COMPARED TO A TAPERED RESULT WHEN WET ACIDS ARE USED. THE STRAIGHT WALLS ARE APPARENTLY NECESSARY TO THE SUCCESS OF MY WORK. SOME OF THE FUNDS ORIGINALLY EARMARKED FOR A GRADUATE STUDENT ARE BEING USED TO GAIN ACCESS TO SAID DRY ETCHING FACILITIES AND HIGH TEMPERATURE VACUUM ANNEALING FACILITIES, MUCH AS I HAVE DONE TO GAIN ACCESS TO THE SUPERIOR METAL DEPOSITION EQUIPMENT.

THE WORK WITH PROFESSOR IANNO IS MOVING ALONG BUT HAS REQUIRED A GREAT DEAL OF PRELIMINARY EFFORT. PROFESSOR IANNO HAS BEEN ABLE TO DO SUFFICIENT TEST RUNS TO GAIN CONFIDENCE REGARDING ETCH RATE OF SILICON DIOXIDE IN HIS DRY ETCHING SYSTEM UTILIZING CF4 ETCHING GAS, WHICH I PURCHASED WITH REMAINING SUPPLY PROCUREMENT FUNDS. TO DATE I HAVE PROVIDED PROFESSOR IANNO WITH FOUR SUBSTRATES UPON WHICH I PERFORMED PHOTORESIST PROCEDURES TO PROVIDE PATTERNS THEREON UTILIZING A NEW MASK. SAID NEW MASK PROVIDES LARGER AREAS FOR ELECTRICAL PROBING THAN DID THE FIRST MASK OBTAINED, (SEE FIG. 1 FOR AN OPTICAL PHOTOGRAPH SHOWING THE PATTERN EFFECTED BY USE OF THE NEW MASK). PROFESSOR IANNO HAS DRY ETCHED THE SILICON DIOXIDE IN THE AREAS NOT PROTECTED BY PHOTORESIST ON THREE OF THE SUBSTRATES, (TWO P-TYPE AND ONE N-TYPE). INVESTIGATION OF THE RESULTS WITH THE SCANNING

ELECTRON MICROSCOPE (SEM) PRIOR TO DEPOSITION OF METAL, (SEE FIG. 2 HEREIN--I AM ABLE TO UTILIZE THE SEM AS A RESULT OF A PROJECT WE DID IN THE SOLAR CELL COURSE I TOOK FIRST SEMESTER), SHOW THAT THE WALLS OF THE ETCHED SILICON DIOXIDE ARE VERY STRAIGHT AT THE LOWER ASPECT OF THE SILICON DIOXIDE, WHERE IT MEETS THE SILICON. THIS IS WHAT IS REQUIRED. FIG. 3 IS INCLUDED TO SHOW A SEM PHOTO OF SILICON DIOXIDE ETCHED WITH HYDROFLUORIC ACID. NOTE THE VERY TAPERED EDGES.

CHROMIUM WAS DEPOSITED UPON EACH OF THREE SILICON SUBSTRATES TO A DEPTH OF APPROXIMATELY 800 ANGSTROMS WHILE EACH WAS HELD AT 200 DEGREES CENTIGRADE, AND EACH SUBSTRATE WAS SUBSEQUENTLY VACUUM ANNEALED AT APPROXIMATELY 400 DEGREES CENTIGRADE FOR 30 MINUTES. DEVICE TESTING REVEALED THAT DISCONTINUITY OF METALIZATION WAS NOT ACHIEVED IN THAT PROBES TO SOURCE AND DRAIN REGIONS INDICATED ELECTRICAL CONTINUITY. HOWEVER, RECTIFYING JUNCTIONS WERE ACHIEVED IN THE SOURCE AND DRAIN REGIONS. IT IS SPECULATED THAT THE WALLS OF THE DRY-ETCHED SILICON DIOXIDE ARE NOT AS STRAIGHT AS THEY COULD BE, AND/OR THAT THE CHROMIUM DEPOSITION SYSTEM IS NOT PROVIDING CHROMIUM TO THE SUBSTRATES ALONG A NORMAL TRAJECTORY. BOTH COULD CAUSE THE NONDISCONTINUITY WE ARE FINDING.

IN VIEW OF THE ABOVE, TO ATTEMPT TO REMOVE THE CHROMIUM FROM THE SILICON DIOXIDE EDGES, AN ADDITIONAL PHOTORESIST PROCEDURE WAS PERFORMED IN WHICH THE SAME MASK AS USED TO DELINEATE THE SOURCE AND DRAIN REGIONS WAS AGAIN USED. PHOTORESIST WAS APPLIED TO A SUBSTRATE WITH CONTINUOUS CHROMIUM THEREON AS JUST DESCRIBED AND EXPOSED THROUGH SAID MASK, WHEN IT WAS ALIGNED WITH THE PATTERN ON THE SUBSTRATE. PHOTORESIST THEN SERVED TO PROTECT THE CHROMIUM ATOP THE SILICON DIOXIDE, BUT LEAVE OPEN THE SOURCE AND DRAIN REGIONS IN WHICH RECTIFYING JUNCTION CAUSING CHROMIUM-DISILICIDE FORMED DURING THE 400 DEGREE CENTIGRADE ANNEAL MENTIONED ABOVE IS PRESENT. A 30 SECOND ETCH IN A MIXTURE OF (8 GRAMS OF CERRIC AMMONIUM NITRATE, 3 MILILITERS OF PERCHLORIC ACID AND 40 MILILITERS OF WATER) PROVED TO GREATLY IMPROVE THE ISOLATION BETWEEN SOURCE AND DRAIN REGIONS---SEE FIG 4. IN FACT BACK TO BACK DIODES WERE OBSERVED, WITH A CURVE TRACER, BETWEEN SOURCE AND DRAIN REGIONS, WITH THE CURRENT SCALE SET TO 10 MICROAMPS. (NOTE THAT THE CHROMIUM-DISILICIDE IS NOT REMOVED BY THE CHROMIUM ETCHANT, HENCE THE RECTIFYING JUNCTIONS IN THE SOURCE AND DRAIN REGIONS REMAIN). THIS APPARENT ISOLATION IS WHAT WE WANT TO SEE, AND UPON OBSERVING IT THE PHOTORESIST WAS ASHED OFF THE CHROMIUM ATOP THE SILICON DIOXIDE, THEREBY PROVIDING AN OPEN GATE METAL FOR PROBING. WE DID NOT HOWEVER, SEE MOSFET ACTION AS HOPED FOR WHEN THE OPEN WAS GATE PROBED AND PROVIDED VOLTAGE STEPS. UPON REALIZING THIS IT WAS OBSERVED THAT CURRENT DOES FLOW DRAIN TO SOURCE AT THE NANONOAMP LEVEL. GATE VOLTAGE HAS NO EFFECT UPON THE MAGNITUDE THEREOF HOWEVER. IN VIEW OF THIS, IT IS SPECULTATED THAT NANOAMP OR LOWER CURRENT LEVELS STILL MIGHT STILL BE FLOWING FROM THE GATE

TO THE DRAIN. THAT WOULD CORRELATE TO APPROXIMATELY (TEN-TO-THE-NINTH OHMS) GATE OXIDE RESISTANCE. THE VALUE SHOULD BE 5 ORDERS OF MAGNITUDE BETTER THAN THAT. THIS INDICATES THAT ALL THE CHROMIUM MIGHT NOT HAVE BEEN REMOVED FROM THE SILICON DIOXIDE EDGES BY THE DESCRIBED 30 SECOND CHROMIUM ETCH. FURTHER WORK IS IN PROGRESS UTILIZING LONGER CHROMIUM ETCHES WITH THE HOPE THAT WE WILL ARRIVE AT SILICON DIOXIDE LEVELS OF ISOLATION. IT WOULD STAND TO REASON THAT IF ANY CURRENTS CAN FLOW FROM THE SOURCE AND/OR DRAIN TO THE GATE, THEN ANY GATE INDUCED CHARGE IN THE CHANNELS REGION WOULD BE DRAINED OFF THEREBY PREVENTING MOSFET ACTION.

IT IS ALSO POSSIBLE THAT THE SILICON DIOXIDE WHICH I GREW ON THE SUBJECT SUBSTRATES, BEING GROWN IN A WET OXYGEN ATMOSPHERE TO SAVE TIME, HAS LED TO SILICON DIOXIDE-SILICON INTERFACE STATES BEING PRESENT WHICH ARE PINNING THE FERMI LEVEL AND PREVENTING SURFACE INVERSION, THEREFORE MOSFET ACTION. IN THE NEXT FABRICATION RUN I AM PLANNING TO GROW SILICON DIOXIDE IN A DRY OXYGEN ENVIRONMENT. IT WILL TAKE 11 HOURS RATHER THAN 48 MINUTES, BUT DOING THIS WILL ELIMINATE A POSSIBLE SOURCE OF PROBLEMS. A FINAL 30 MINUTE ANNEAL IN A NITROGEN AMBIENT WILL ALSO BE PERFORMED AS SUCH IS KNOWN TO REDUCE SURFACE STATES. (IT IS NOTED THAT EARLY WORK TO DEVELOP CONVENTIONAL MOSFETS RAN INTO PROBLEMS BECAUSE THE SILICON DIOXIDE QUALITY WAS POOR). AS WELL, THE NEXT FABRICATION RUN WILL UTILIZE (100) ORIENTED CRYSTALINE SILICON RATHER THAN THE (111) USED TO DATE BECAUSE OF AVAILABILITY AND SIZE. (100) SILICON HAS FEWER SURFACE STATES ASSOCIATED THEREWITH BUT THAT AVAILABLE TO ME MUST BE CUT TO A SIZE WHICH WILL FIT IN THE EQUIPMENT BEING USED. IN CONJUNCTION WITH THIS CAPACITANCE-VOLTAGE (C-V) PLOTS WILL BE OBTAINED IN THE NEAR FUTURE TO DETERMINE IF THE CHANNEL REGION SURFACE UNDER THE GATE IS INVERTING WHEN GATE VOLTAGE IS APPLIED. IF THIS IS THE CASE THEN THE PROBLEM WOULD MOST PROBABLY BE CAUSED BY LACK OF CONTINUITY OF THE CHANNEL WITH THE SOURCE AND DRAIN CHROMIUM AT THE EDGES OF THE GATE. IF THIS IS THE CASE IT COULD BE OVERCOME BY A SILICON ETCH PRIOR TO CHROMIUM DEPOSITION. THIS WILL BE TRIED.

I WILL ALSO MENTION THAT MY FIRST ATTEMPTS AT THE SECOND PHOTORESIST PROCEDURE WERE NOT SUCCESSFUL. IT TOOK SOME TIME TO REALIZE THAT THE HIGHLY REFLECTIVE CHROMIUM GREATLY CHANGES THE PHOTORESIST ULTRAVIOLET LIGHT EXPOSURE REQUIREMENTS. WHEREAS IT IS TYPICAL TO DO A 2 MINUTE EXPOSURE, ANYTIME LONGER THAN APPROXIMATELY 30 SECONDS IN THE SECOND PROCEDURE LEADS TO THE PHOTORESIST BEING HARDENED OVER NEARLY THE ENTIRE SUBSTRATE RATHER THAN ONLY BENEATH THE CLEAR AREAS ON THE MASK. AS WELL, IT IS VERY DIFFICULT TO PERFECTLY ALLIGN THE MASK WITH AN EXISTING PATTERN WITH THE AVAILABLE EQUIPMENT.

CONTINUING, IN ADDITION, A TASK 2 RELATED SEQUENCE OF ANNEALING PROCEDURES WAS PERFORMED ON CHROMIUM-SILICON SYSTEMS,

AND THE ELECTRICAL CHARACTERISTICS OF THE RESULTING RECTIFYING JUNCTIONS OBTAINED. BOTH N AND P-TYPE SILICON WAS INVESTIGATED AND ANNEALING WAS PERFORMED AT 350, 450, 550 AND 650 DEGREES CENTIGRADE FOR 30 MINUTE TIME PERIODS IN A NITROGEN AMBIENT. NOTE, CHROMIUM WAS DEPOSITED TO A DEPTH OF APPROXIMATELY 300 ANGSTROMS ON EACH SUBSTRATE THROUGH A MASK WHICH PROVIDED CIRCULAR HOLES THERETHROUGH. THE RESULTS OF THIS EFFORT REVEALED THAT ANNEAL AT TEMPERATURES OF 450 DEGREES CENTIGRADE AND LOWER PROVIDED VERY REPEATABLE RESULTS ON BOTH N AND P-TYPE SILICON IN WHICH THE REVERSE BREAKDOWN VOLTAGE AVERAGES AROUND 20 VOLTS AND IN WHICH THE FORWARD CONDUCTION KNEE IS AT APPROXIMATELY 0.2 TO 0.5 VOLTS. ANNEAL AT 650 DEGREES CENTIGRADE PROVIDED DIODES WHICH PROVIDE A REVERSE BREAKDOWN VOLTAGE OF 90 TO 100 VOLTS. HOWEVER THE RESULTS ARE NOT REPRODUCIBLE AT WILL. THAT IS, NUMEROUS PROBING ATTEMPTS ARE REQUIRED TO LOCATE SAID DIODES. THE REASON APPEARS TO BE THAT THE CHROMIUM HAS REACTED WITH THE SILICON WITH THE RESULT BEING THAT SAID CHROMIUM IS NOT UNIFORM ACROSS EACH DOT, (RECALL THAT ONLY APPROXIMATELY 300 ANGSTROMS OF CHROMIUM WAS DEPOSITED--A VERY THIN LAYER). IN THE LOWER TEMPERATURE ANNEAL CASES THE CHROMIUM STILL APPEARED TO BE VERY UNIFORM. ADDITIONAL WORK IN THIS AREA WILL BE CONTINUED. FIGS. 5 AND 6 SHOW TYPICAL I-V CHARACTERISTICS FOR DIODES FORMED BY ANNEAL AT 450 DEGREES CENTIGRADE OR LOWER, FOR N AND P-TYPE SILICON RESPECTIVELY. FIGS. 7 AND 8 SHOW SIMILAR CHARACTERISTICS ACHIEVED WHEN THE ANNEAL TEMPERATURE WAS 650 DEGREES CENTIGRADE. IT WOULD APPEAR THAT THE HIGHER ANNEALING TEMPERATURE IS HAVING A SIGNIFICANT EFFECT ON THE REVERSE BREAKDOWN VOLTAGE ACHIEVABLE. THIS DUPLICATES MY WORK AT TORONTO UNIVERSITY YEARS AGO REGARDING N-TYPE SILICON AND EXTENDS IT TO P-TYPE SILICON.

FINALLY, I HAVE, SO FAR, RECEIVED SEVEN ADVANCES OUT OF EIGHTEEN, HAVING LET TWO MONTHS SLIDE AS A RESULT OF HAVING NOT EXPENDED FUNDS RECEIVED IN THE FIRST FOUR MONTHS OF THE GRANT DURING THE FIRST FOUR MONTHS, LEAVING SUFFICIENT FUNDS TO CARRY THROUGH THE FIFTH AND SIXTH MONTHS. WHILE THE WORK IS NOT PRESENTLY AS FAR ADVANCED AS I WOULD LIKE, IT IS PRETTY FAR ALONG WHEN VIEWED AGAINST THE NUMBER OF ADVANCES TAKEN TO DATE. I HAD HOPED TO HAVE BETTER RESULTS AT THIS TIME, BUT MUST AT THIS TIME ONLY REPORT THAT I AM WORKING TO OBTAIN THEM AS BEST I CAN.

I WANT TO ALSO RELATE MY VERY POSITIVE OPINION REGARDING THE AID PROVIDED TO ME BY THE STAFF OF THE UNL EE DEPARTMENT. THINGS DO NOT ALWAYS MOVE AS FAST AS I'D LIKE, BUT THE PROFESSORS AND OTHERS ARE ALL TO BE COMMENDED FOR THEIR VERY POSITIVE ATTITUDES AND HELP.

SINCERELY,

JAMES D. WELCH

JW/hs
ENC.

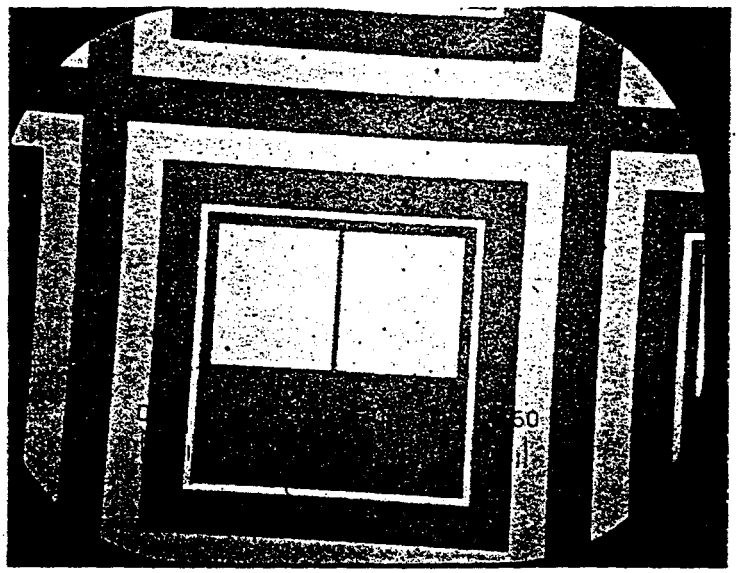


Fig. 1A

optical microscope of New Mask Pattern Dry Etched SiO_2

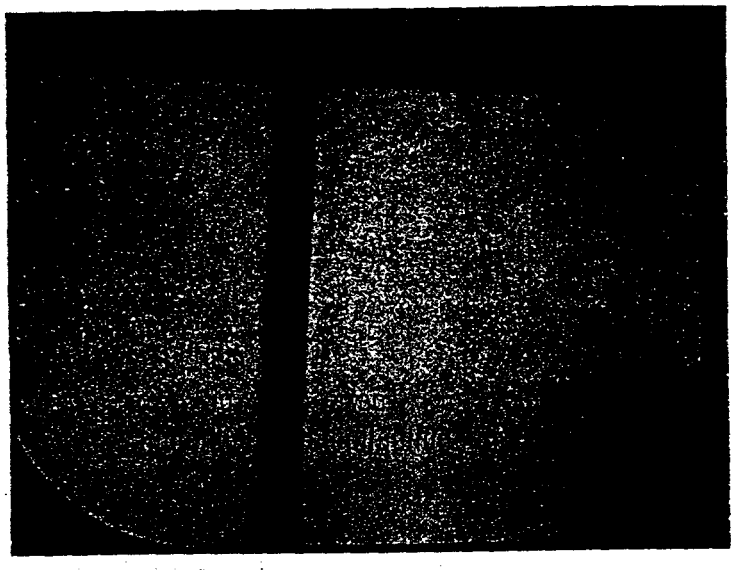
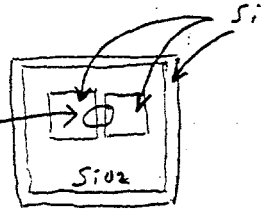


Fig 1B

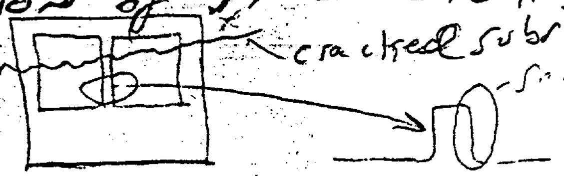
Close-up of Gate

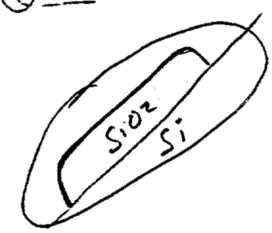


?/7/94
Called Air Products - Tom will call Tank of N_2
Delivered

?/8/94
Called Air Products — Gary says he delivered N_2
end of February to Rm 218. -- will bring another Tank tomorrow.
When get N_2 & Sergio puts 1000Å Cr onto NaP
substrate - divide each into Quarters & do 10, 20, 30 min
anneals on each at 350, 450 550 & 650°C.
Take diode I-V curves after each time period.

?/10/94
Did SEM investigation of dry SiO_2 etch
on edge of substrate





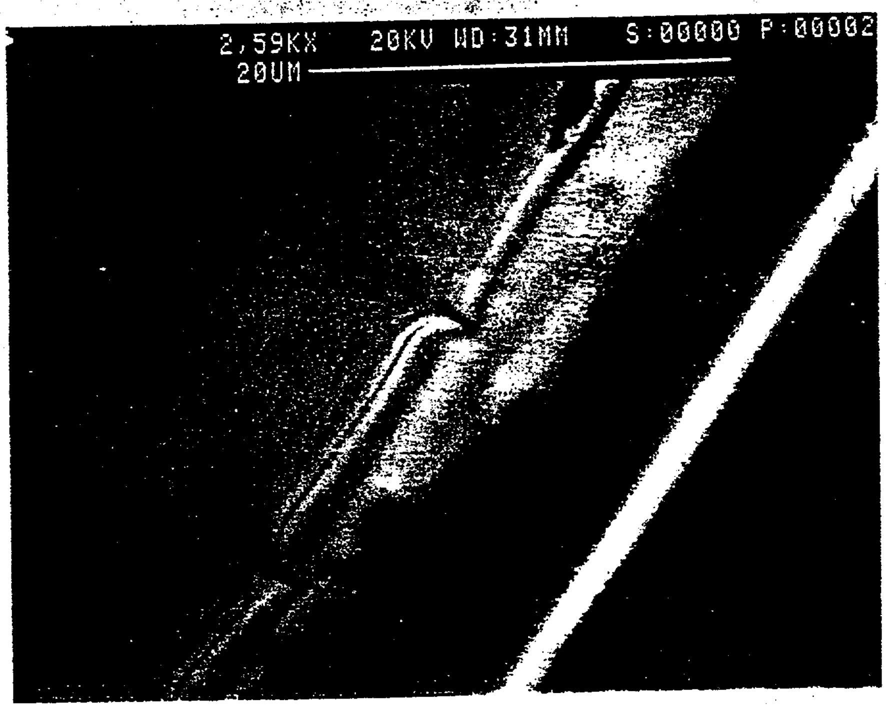


Fig 2

* See p. 11 for optical image of fill flow with P.R. [illegible]

See page 12 for [illegible]

HF wet
d SEM Photo of Acid etched SiO_2

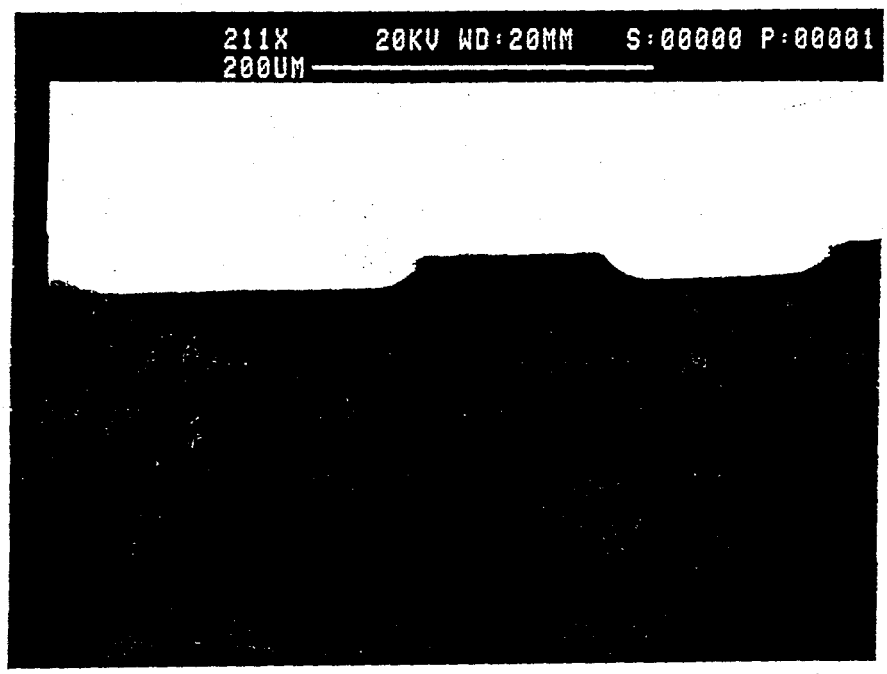
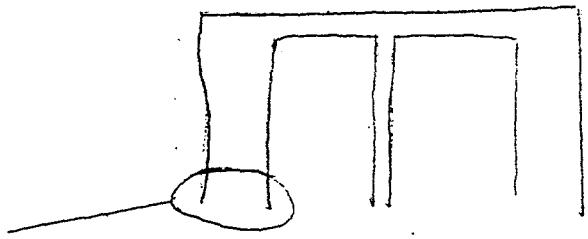


Fig. 3



show Taper wet etch profile

looking directly onto SiO_2 etch

See page 12 for dry etch SEM profile.

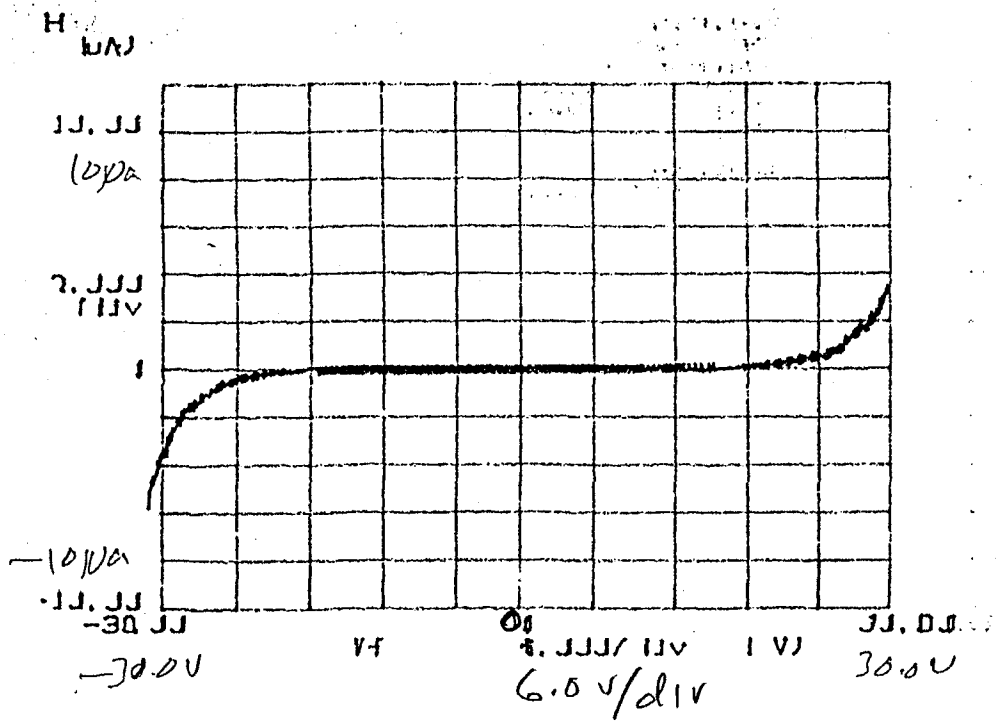


Fig. 4

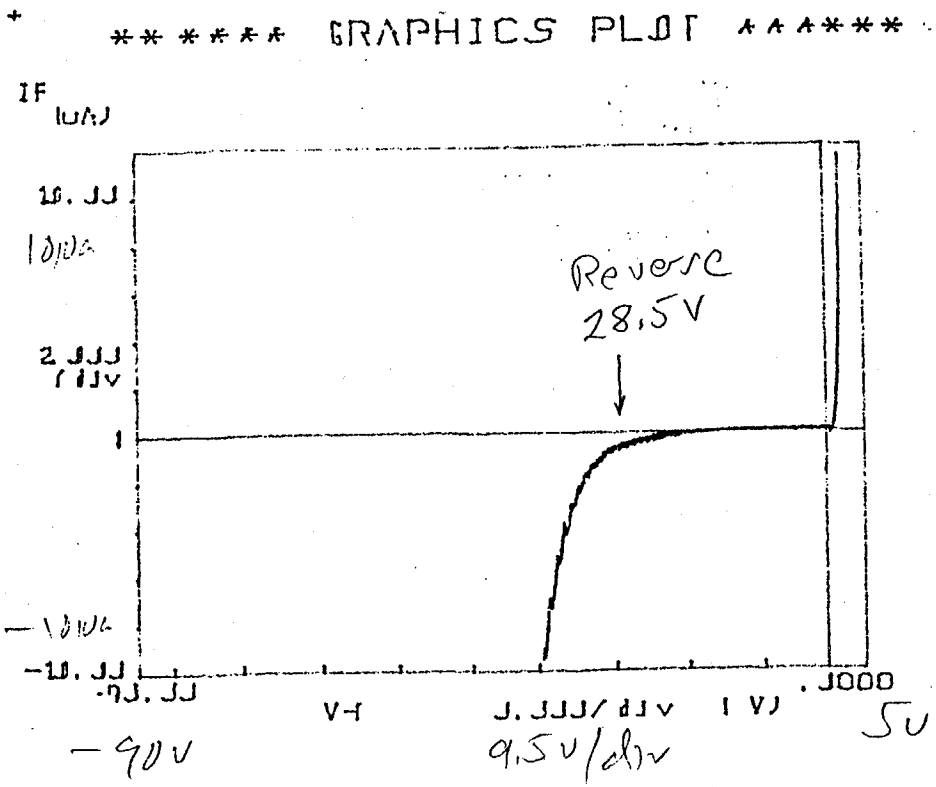
Back To Back Diodes Source To Drain, on 10μa scale.

400 °C
30 minute Anneal

≈ 500 Å Cr present initially

Cr etched 30 sec

N-Type
450°C
30 min



-90V

Fig 5

450°C
30 minute
Anneal
N-Type
≈ 300 Å Cr present
in DoT
very repeatable

P-Type
450°C
30 min
very repeatable
with some Vp being
a bit lower

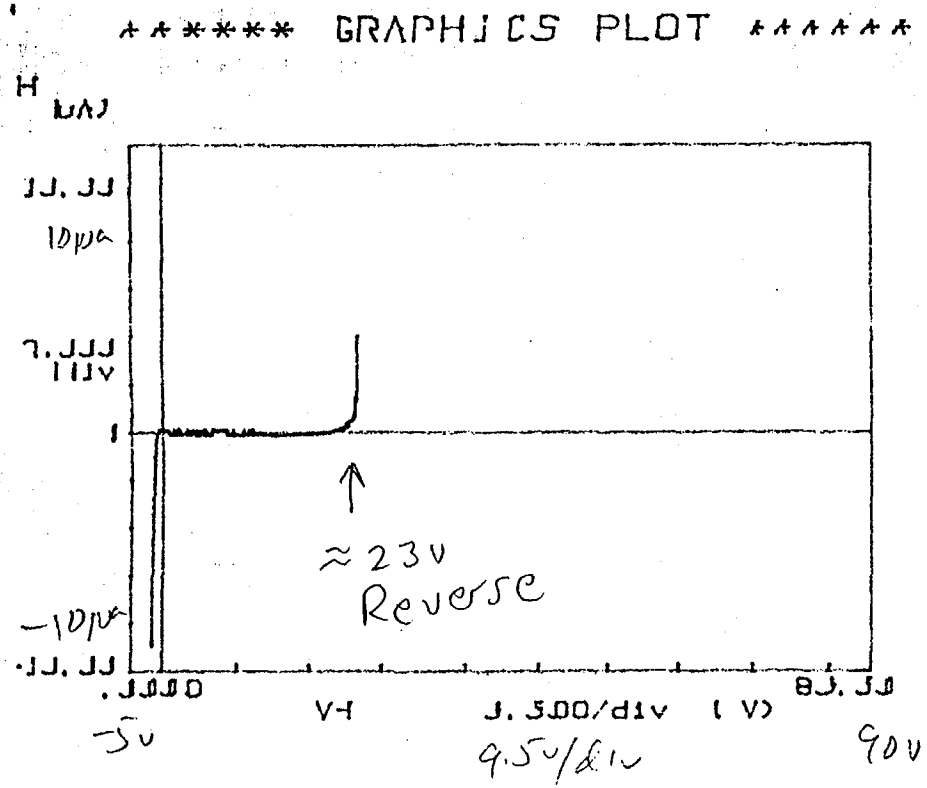


Fig 6

450°C
30 minute
Anneal
P-Type
≈ 300Å Cr present
in DoT
very repeatable

3/22/94

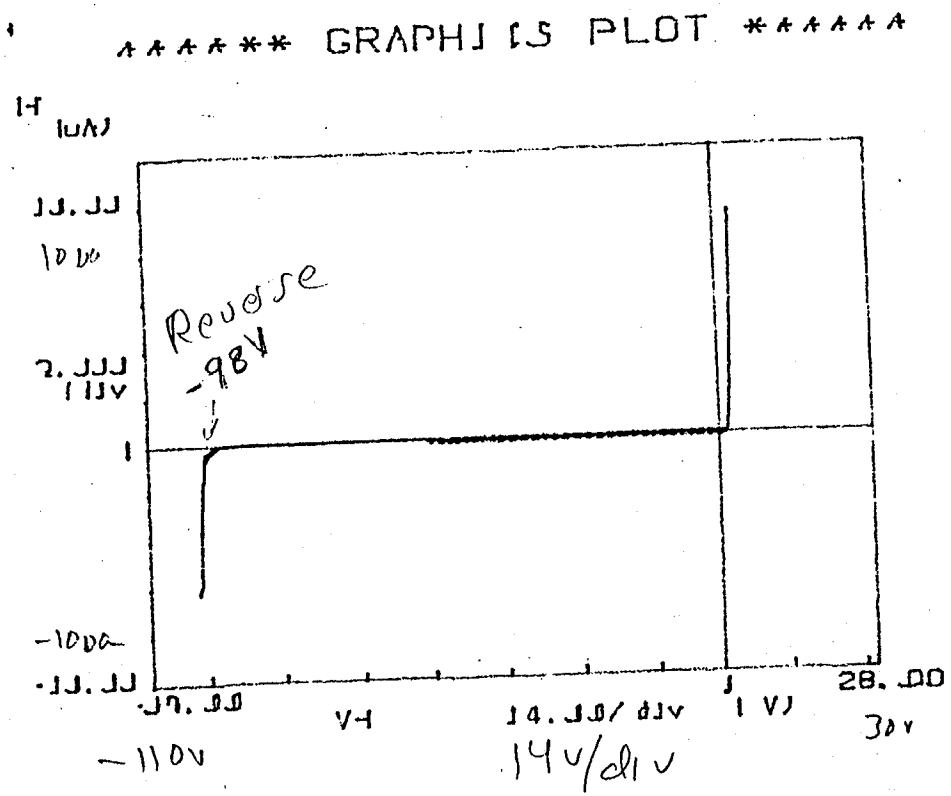


Fig. 7

650°C
30 minute
Anneal
N-Type
≈ 300 Å Cr present
in DOT

****** GRAPHICS PLOT ******

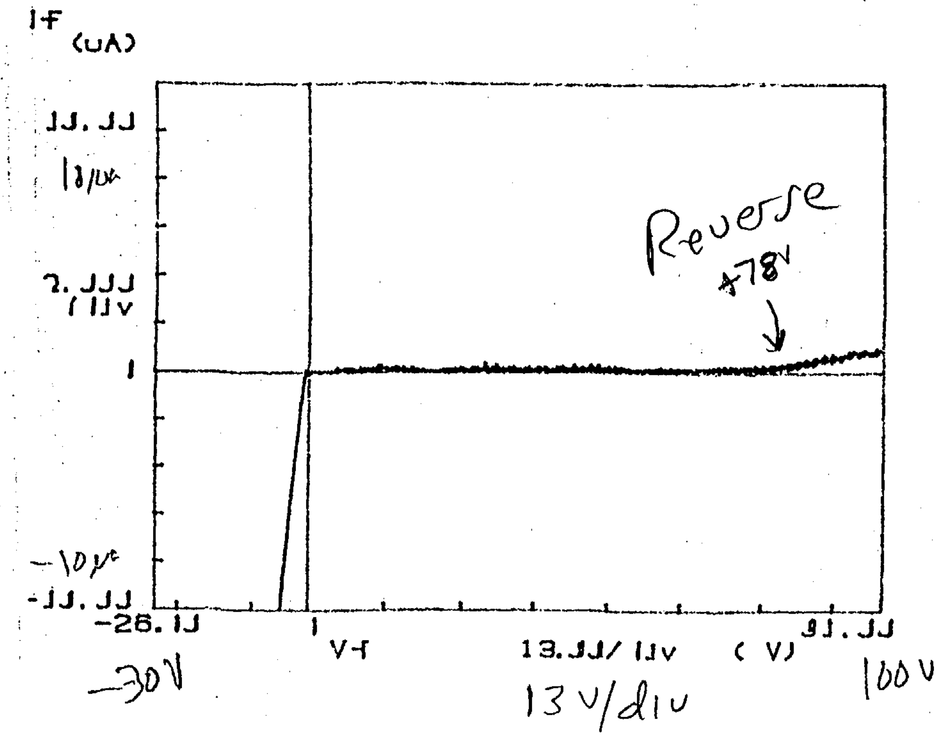


Fig 8

650°C
30 minute
Anneal
P-Type
≈ 300 Å Cr present in DOT

JAMES D. WELCH
ATTORNEY AT LAW
PROFESSIONAL ENGINEER

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July 15, 1994

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U.S. Department of Energy
911 Walnut, 14th Floor
Kansas City, MO 64106

DOE Project Officer
Anne Scheer
U.S. Department of Energy
911 Walnut, 14th Floor
Kansas City, MO 64106

U.S. Department of Energy
Department of the Controller
Payments Management Branch
P.O. Box 500
Germantown, MD 20784

RE: QUARTERLY AND FEDERAL CASH TRANSACTIONS REPORT.
FEDERAL GRANT NO.: DE-FG47-93R701314.

Dear Sirs;

Please find enclosed the identified documents.

Sincerely,

JAMES D. WELCH
JW/hs
ENC.

JAMES D. WELCH
ATTORNEY AT LAW
PROFESSIONAL ENGINEER

TELLECTUAL PROPERTY
402-391-4448

10328 PINEHURST AVE.
OMAHA, NEBRASKA 68124

JULY 10, 1994

QUARTERLY REPORT 4

RE: FEDERAL GRANT NO. DE-FG47-93R701314.
COORDINATOR: JACK AELLEN.
TO: JAMES D. WELCH, SOLE PROPRIETOR.
FROM: U.S. DEPARTMENT OF ENERGY, ENERGY RELATED INVENTIONS.
PROJECT: NOVEL METHOD FOR MAKING SEMICONDUCTOR CHIPS.

INVENTION NO: 534
OERI NO: 012693

FOR PERIOD BEGINNING: APRIL 7, 1994
AND ENDING: JULY 7, 1994

TASK 3. NMOS AND PMOS PRODUCTION.

THERE HAVE BEEN SOME VERY INTERESTING, ENCOURAGING AND "CONFUSING", DEVELOPMENTS AND RESULTS DURING THE LAST QUARTER.

WE CONTINUED TO ATTEMPT TO ARRIVE AT SELF DELINEATED GATE, SOURCE AND DRAIN PATTERNS USING THE PROCEDURE OF MY 4,696,093 PATENT---WITHOUT SUCCESS. WHILE WE ARE ABLE TO NOW STANDARDLY PLASMA ETCH THE MOSFET PATTERN INTO SILICON DIOXIDE, (WE ARE USING THREE-THOUSAND (3000) ANGSTROMS OF SILICON DIOXIDE AND CF4 GAS IN PLASMA TO ETCH THEREINTO), AND INTO SILICON, (EFFECTED BY ADDING SOME OXYGEN TO THE CF4 GAS), WE HAVE BEEN UNABLE TO ACHIEVE DISCONTINUOUS METALIZATION WHEN EIGHT-HUNDRED (800) ANGSTROMS OF CHROMIUM IS DEPOSITED OVER THE SUBSTRATE IN THE ELECTRON BEAM EVAPORATOR. THAT IS, WHEN WE CHECK BETWEEN THE SOURCE AND DRAIN IMMEDIATELY AFTER METAL DEPOSITION AND ANNEAL, WE FIND A SHORT CIRCUIT. THIS IS THE CASE EVEN WHERE WE ETCHED INTO THE SILICON TO DEPTHS OF TWO (2) MICRONS BY A WET ACID APPROACH.

AS PART OF THE PLANNED PROCEDURE WE HAVE BEEN ANNEALING THE SUBSTRATES AFTER THE CHROMIUM IS DEPOSITED, AT A NOMINAL FOUR-HUNDRED (400+) DEGREES CENTIGRADE FOR THIRTY (30) MINUTES. THIS IS BEING DONE IN A VACUUM ENVIRONMENT AND SERVES TO FORM CHROMIUM-DISILICIDE WHERE THE CHROMIUM IS IN CONTACT WITH THE SILICON, BUT IT DOES NOT NOTICEABLY AFFECT THE CHROMIUM ATOP THE

SILICON DIOXIDE. WE KNOW WE ARE FORMING RECTIFYING JUNCTIONS BECAUSE WE SEE BACK TO BACK REVERSE BREAKDOWN VOLTAGE CURVES, (AFTER WE REMOVE DRAIN TO SOURCE CHROMIUM WHICH INITIALLY EFFECTS A SHORT THEREBETWEEN), WHEN WE APPLY SUFFICIENTLY HIGH VOLTAGES (EG. PLUS/MINUS 20 TO 30 VOLTS), BETWEEN THE SOURCE AND DRAIN OF A DEVICE WITH THE CURVE TRACER.

HERE IS WHERE IT GETS INTERESTING. AS ONE AVENUE OF INVESTIGATION TO OBTAIN A DISCONTINUOUS METALIZATION PATTERN, I DID A TIME LIMITED ETCH OF CHROMIUM WITHOUT USING ANY PHOTOLITHOGRAPHIC MASKING TO PROTECT THE CHROMIUM ATOP THE SILICON DIOXIDE GATE. (NOTE THAT I'VE FOUND THAT ALIGNMENT MUST BE PERFECT IF SUCH PHOTOLITHOGRAPHIC MASKING IS UTILIZED, AND PERFECT MASK ALIGNMENT IS ESSENTIALLY IMPOSSIBLE TO OBTAIN AT WILL). MY HOPE WAS THAT I COULD ETCH THE LAYER OF CHROMIUM OFF THE SILICON DIOXIDE WALLS, (IT BEING THEORETICALLY THINNER THAN THAT ATOP THE SILICON DIOXIDE GATE), BUT STILL HAVE CHROMIUM REMAINING ATOP THE SILICON DIOXIDE GATE. WHAT OCCURRED WAS THAT AFTER TEN (10) SECONDS OF CHROMIUM ETCH, THE SOURCE AND DRAIN WERE STILL SHORTED. AFTER TWENTY (20) SECONDS ALL CHROMIUM WAS ETCHED. (THAT IS, SUCH AN ETCH IS HARD TO CONTROL AND WOULD NOT LIKELY BE APPROPRIATE FOR PRODUCTION). DO NOTE, HOWEVER, THAT THE CHROMIUM DISILICIDE IS NOT ETCHED BY THE CHROMIUM ETCH AND THAT RECTIFYING JUNCTIONS REMAIN IN THE SOURCE AND DRAIN REGIONS AFTER SAID ETCH.

CONTINUING, I DECIDED TO PROBE DEVICES IN WHICH THERE WAS NO GATE METAL REMAINING TO SEE IF I COULD OBSERVE ANYTHING AT ALL. FIGURES 1 AND 2 HEREIN SHOW THAT I HAPPENED ON WHAT APPEAR TO BE MOSFET-LIKE CURVES. THE CURVES IN FIG. 1 WERE OBTAINED FROM DEVICES ON P-TYPE SILICON, AND THOSE IN FIG. 2 WERE OBTAINED FROM DEVICES ON N-TYPE SILICON ON APRIL 27, 1994 AND APRIL 28, 1994 REPSECTIVELY . NOTE THAT THE DRAIN AND GATE VOLTAGES ARE REVERSED, COMPARING THE RESULTS SHOWN IN FIG. 1 AND FIG. 2. THIS INDICATES THAT THE SUBSTRATE TYPE WAS HAVING AN EFFECT. ALSO NOTE THAT THE PROBE NEEDLE APPARENTLY SERVED AS THE GATE METALIZATION. IT IS APPROXIMATELY SEVENTY-FIVE (75) MICRONS WIDE AT THE TIP.

WHILE THESE CURVES ARE ENCOURAGING IN THAT GATE APPLIED VOLTAGE AFFECTED THE DRAIN CURRENT, WE DO NOT FULLY UNDERSTAND WHAT WE ARE SEEING, (CONFUSION). AS WELL, THE CURVES HAVE PROVEN TO BE VERY ELLUSIVE. THE PROBE NEEDLE MUST BE SET BY TRIAL AND ERROR AND ONCE THE CURVES ARE FOUND, THE SLIGHTEST BUMP OF THE PROBE STAND CAUSES THEM TO BE LOST. MUCH TRIAL AND ERROR EFFORT IS THEN REQUIRED TO AGAIN FIND THEM. IT WAS <u>EXTREMELY LUCKY</u> THAT I FOUND THEM AT ALL. IF THE CURVE TRACER CURRENT LEVEL HAD NOT BEEN SET TO THE NANOAMP LEVEL (AND THERE WAS NOTHING IDENTIFIABLE GUIDING ME TO SET IT THERE), I WOULD HAVE NEVER KNOWN THE CURVES WERE THERE EVEN IF I HAD OBTAINED THEM. THEY SIMPLY WOULD NOT HAVE BEEN DISTIGNUISHABLE. IT IS ALSO MENTIONED THAT IT WAS

IMPOSSIBLE TO REPEAT THE RESULTS ONCE ACHIEVED FOR WEEKS THEREAFTER. FOR A WHILE THE CURVE TRACER WAS USED BY OTHERS AT THE UNIVERSITY, AND MY USE OF IT WAS CURTAILED FOR A FEW WEEKS. WHEN I AGAIN GAINED ACCESS TO THE CURVE TRACER, I FOUND I COULD NOT AGAIN ACHIEVE THE CURVES. AS MENTIONED ABOVE, I WAS ABLE TO OBTAIN CURVES A NUMBER OF TIMES IN A TWO DAY PERIOD, (APRIL 27 AND 28TH), BUT WAS NOT ABLE TO OBTAIN ANYTHING SIMILAR AGAIN, EVEN USING THE SUBSTRATES WHICH PROVIDED THE CURVES SHOWN IN FIGS. 1 & 2, UNTIL JUNE 30, 1994, AND THAT WAS AFTER I RINSED THE SAME SUBSTRATES WITH WATER AND BLEW THEM DRY WITH COMPRESSED CLEAN GAS. AFTER WEEKS OF WONDERING WHAT MIGHT BE DIFFERENT, ONE THING I REALIZED WAS THAT JUST BEFORE PROBING, I HAD JUST FINISHED ETCHING CHROMIUM AND RISING THE SUBSTRATES WITH WATER THE FIRST TIME I FOUND CURVES. I SPECULATED THAT LATENT REMAINING WATER ATOP THE OXIDE MIGHT HAVE BEEN SERVING AS A GATE "METAL" ATOP THE SILICON DIOXIDE. (RECALL THAT THE DEVICES HAVE NO GATE METAL PRESENT). WHEN I TESTED THAT THEORY, I OBTAINED CURVES ON THE P-TYPE SUBSTRATE FAIRLY QUICKLY, ALTHOUGH THEY WERE A BIT DIFFERENT THAN THOSE I ACHIEVED IN APRIL. SEE FIGS. 3 AND 4. FIG. 3 SHOWS THE CURVES I ACHIEVED ON JUNE 30, 1994 WHEN GATE VOLTAGE WAS STEPPED FROM -10 TO +28 VOLTS AND DRAIN TO SOURCE VOLTAGE WAS SWEPT FROM -5 TO +5. THE CURVES ARE GENERALLY SIMILAR TO THOSE SHOWN IN FIG 1, BUT THE THRESHOLD OF CONDUCTION IS ABOUT -10 VOLTS RATHER THAN -4 VOLTS AS IN FIG. 1. THIS COULD BE BECAUSE POSITIVE IONS HAD SOMEHOW CONTAMINATED THE SUBSTRATE OXIDE SINCE THE FIG. 1 CURVES WERE ACHIEVED, THEREBY CAUSING THE CHANNEL REGION OF THE DEVICE TESTED TO BE INVERTED WITH NO GATE VOLTAGE PRESENT. THAT WOULD EXPLAIN THE HIGHER "0" GATE VOLTAGE DRAIN CURRENT AS WELL. NOW, WHILE I HAD THE ABILITY TO OBTAIN THE FIG. 3 CURVES I TOOK THE GATE LEAD LOOSE AND AGAIN RAN THE VOLTAGES. FIG. 4 SHOWS THAT ONLY A SINGLE TRACE WAS PRESENT. THIS IS WHAT ONE WOULD EXPECT IF THE CURVES ARE MOSFET IN NATURE. I ALSO LIMITED THE GATE CURRENT COMPLIANCE TO ESSENTIALLY "0" AMPS, (IE. THE CURVE TRACER PROVIDES 50 PICO AMPS WHEN "0" AMPS IS REQUESTED), AND THE CURVES REMAINED ESSENTIALLY AS SHOWN IN FIG. 3. THIS IS ALSO CONSISTANT WITH OPERATION AS A MOSFET WITH AN INVERTED CHANNEL AND A REVERSE BIASED DRAIN JUNCTION AND WITH A NON- LEAKING OXIDE.

IN EARLY JUNE I CONSULTED WITH PROFESSOR IANNO REGARDING THE STATE OF AFFAIRS AND WE DEVISED AN APPROACH WHICH WILL RESULT IN GATE METAL BEING PRESENT IN A RELATIVELY EASILY FABRICATED MOSFET. WE FELT THAT WHAT WE HAD SEEN TO DATE WAS VERY ENCOURAGING, BUT THAT UNTIL WE COULD PRODUCE A DEVICE WITH STABLE GATE METALIZATION, WE WOULD BE UNABLE TO REALLY GET A GRIP ON THE SOURCE OF THE CURVES ACHIEVED. THE MODIFIED FABRICATION APPROACH IS NOT AS SIMPLE AS THE ORIGINAL, (IT REQUIRES AN ADDITIONAL METAL DEPOSITION), BUT IT SHOULD LEAD TO RELIABLE FABRICATION OF STABLE DEVICES, AND THE NUMBER OF STEPS REQUIRED TO OBTAIN THEM WILL STILL BE LESS THAN CONVENTIONAL DIFFUSED JUNCTION MOSFETS REQUIRE. THE NEW APPROACH, FOR WHICH I HAVE

SUBMITTED A DISCLOSURE DOCUMENT TO THE PATENT OFFICE IS:

1. SELECT SILICON SUBSTRATE.
2. GROW SILICON DIOXIDE ATOP THEREOF.
3. DEPOSIT ALUMINUM TO A DEPTH OF APPROXIMATELY 5000 ANGSTROMS.
4. APPLY PHOTORESIST AND EXPOSE THROUGH EXISTING MASK.
5. ETCH ALUMINUM WITH PHOSPHORIC ACID.
6. ETCH SILICON DIOXIDE WITH PLASMA CF4 GAS.
7. APPLY 1000 ANGSTROMS OF CHROMIUM OVER THE RESULTING SUBSTRATE PATTERN.
8. ANNEAL THE SUBSTRATE AT 400+ DEGREES CENTIGRADE.
9. ETCH OFF CHROMIUM, NOT REACTED WITH SILICON TO FORM RECTIFYING CHROMIUM DISILICIDE JUNCTIONS IN SOURCE AND DRAIN REGIONS.
10. TEST DEVICES.

WE HAVE PERFORMED ONE RUN USING THIS PROCEDURE AND HAVE FOUND THAT THE VARIOUS STEPS DO PROVIDE THE STRUCTURE WE WANT, BUT WE DID NOT FIND STABLE MOSFET CURVES UPON REACHING STEP 10 ABOVE. IT APPEARS THAT THE OXIDE IS LEAKING SIGNIFICANT CURRENT TO THE DRAIN CIRCUIT IN THESE DEVICES. IN PARTICULAR THOUGH, THE CHROMIUM ETCHANT, (CERRIC AMMONIUM NITRATE IN PERCHLORIC ACID AND WATER), DOES NOT QUICKLY AFFECT THE ALUMINUM, THEREBY ALLOWING SAID CHROMIUM ETCHANT TO BE USED TO REMOVE UNREACTED CHROMIUM, (THAT NOT CONVERTED TO SILICIDE DURING AN ANNEAL), WITHOUT DESTROYING THE GATE METAL. WE HAVE CONFIDENCE THAT THE ABOVE PROCEDURE WILL PROVIDE OPERATIONAL MOSFETS WHEN WE HAVE BETTER CONTROL OVER THE GATE CIRCUIT LEAKAGE CURRENT. WE MAY PURCHASE SOME SILICON SUBSTRATES WITH PROFESSIONALLY GROWN SILICON DIOXIDE ATOP THEREOF.

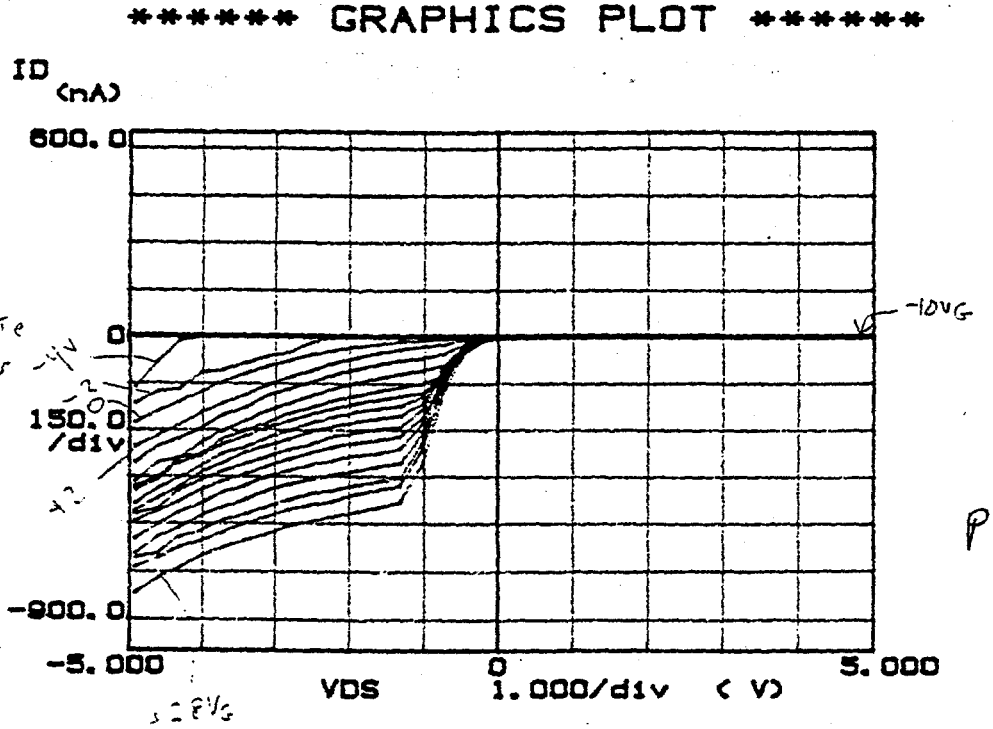
I WANT TO ALSO MENTION THAT I HAVE SUBMITTED AN ADDITIONAL PATENT APPLICATION TO THE PATENT OFFICE. WHILE THE PATENT APPLICATION WILL CERTAINLY HAVE TO BE RESUBMITTED AS A CONTINUATION SOMETIME DOWN THE ROAD BASED UPON CONTINUED NEW FINDINGS, (THAT IS, THE PRESENTLY SUBMITTED NEW PATENT APPLICATION IS VERY UNLIKELY TO EVER BE TAKEN TO ISSUE AS A PATENT), I FEEL IT DOES NOT HURT TO BEGIN PATENT SUCH EFFORTS NOW. THIS IS PRIMARILY IN VIEW OF THE FACT I CAN DO THE APPLICATION MYSELF, WEARING MY PATENT ATTORNEY, RATHER THAN MY RESEARCHER, HAT. BY SO PROCEEDING I WILL GAIN INSIGHT TO ANY PATENT ACTIVITY IN THE AREA OF WHICH I AM NOT NOW AWARE. THE PRESENTLY SUBMITTED PATENT APPLICATION, WILL SERVE TO PROVIDE A PATENT EXAMINER'S SEARCH OF THE CURRENT STATE OF THE ART, WHICH WILL BE VALUABLE WHEN PREPARING A CONTINUATION APPLICATION DOWN THE ROAD. (NOTE IT WOULD COST AS MUCH TO HAVE A PATENT SEARCH PERFORMED AS IT DOES FOR ME TO SUBMIT AN APPLICATION AND OBTAIN A PATENT EXAMINER PERFORMED SEARCH). I HAVE ADVISED THE DOE ATTORNEY OF THIS EFFORT AND PROVIDED HIM AN ABSTRACT OF THE APPLICATION.

WE ARE CONTINUING TO STRIVE TO ACHIEVE THE GOAL.

SINCERELY,

JAMES D. WELCH

JW/hs
ENC.



Variable1:
VDS -Ch2
Linear sweep
Start -10.000V
Step 5.0000V
Step .3000V

Variable2:
VG -Ch3
Start -10.000V
Step 28.000V
Step 2.0000V

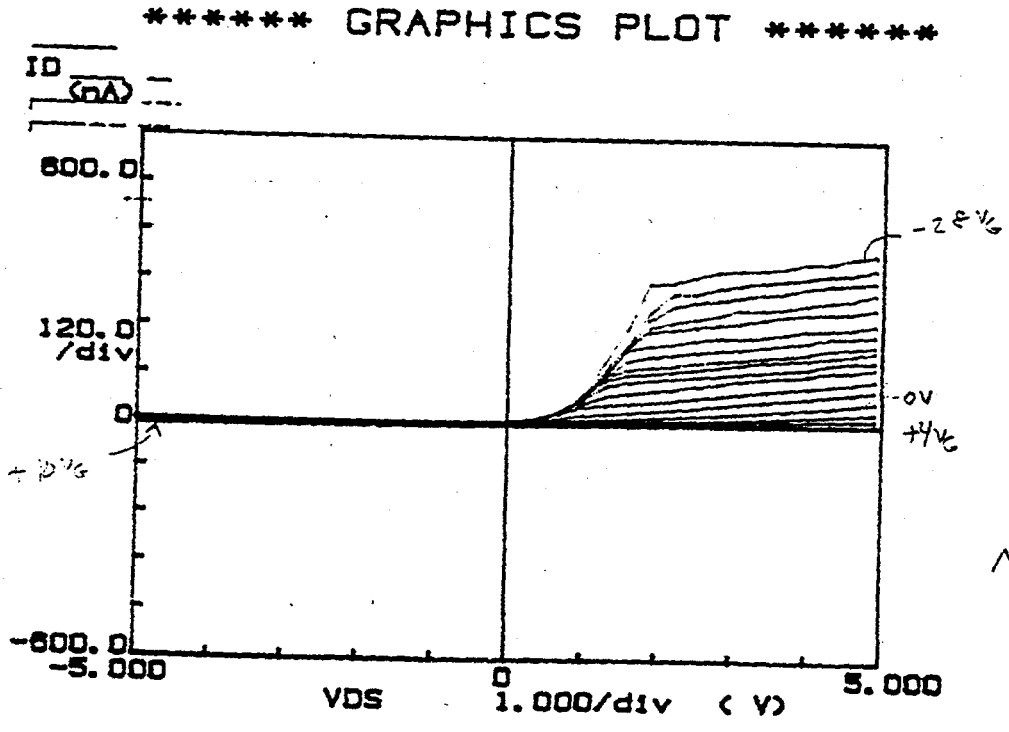
Constants:
VS -Ch1 .0000V

Curve Tracer Settings

P-Type

April 27, 1994

Fig. 1



Variable1:
VDS -Ch2
Linear sweep
Start -5.0000V
Step 5.0000V
Step .3000V

Variable2:
VG -Ch3
Start 10.000V
Step -28.000V
Step -2.0000V

Constants:
VS -Ch1 .0000V

Curve Tracer Settings

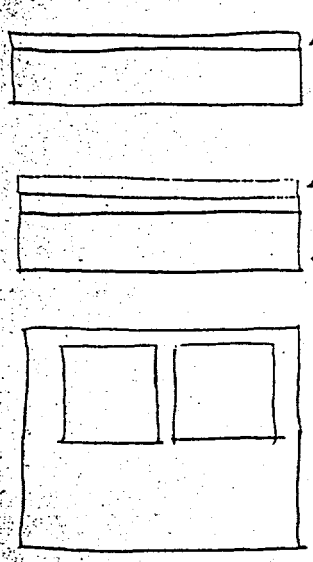
N-Type

April 28, 1994

Fig. 2

6/12/97

Neil: Let's Try This:
We can sputter the metal.



(Start w/ P <111> with SiO_2 Thermal)

PR & Expose 30 sec.

Then Etch Thru (Cr or Al) & SiO_2 & perhaps Si

(Can we dry etch Cr? Al?)

Then deposit Cr Ti ≈ 800 Å

Then Anneal 400°C 30 minutes

Then remove unreacted Cr

- Should have Device with Gate metal & $CrSi_2$ Source & Drain

Then put Al on back

Then Test

This is the same process as in my Patent

JAMES D. WELCH
ATTORNEY AT LAW
PROFESSIONAL ENGINEER

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10328 PINEHURST AVE.
OMAHA, NEBRASKA 68124

October 15, 1994

Administered for DOE
Kansas City Support Office
U.S. Department of Energy
911 Walnut, 14th Floor
Kansas City, MO 64106

DOE Project Officer
Anne Scheer
U.S. Department of Energy
911 Walnut, 14th Floor
Kansas City, MO 64106

U.S. Department of Energy
Department of the Controller
Payments Management Branch
P.O. Box 500
Germantown, MD 20784

Dear Sirs;

Please find enclosed the Fifth Quarterly Report.

Sincerely,

JAMES D. WELCH
JW/hs
ENC.

JAMES D. WELCH
ATTORNEY AT LAW
PROFESSIONAL ENGINEER

TELLECTUAL PROPERTY
402-391-4448

10328 PINEHURST AVE.
OMAHA, NEBRASKA 68124

OCTOBER 15, 1994

RE: FEDERAL GRANT NO. DE-FG47-93R701314
COORDINATOR: FRED HART
TO: JAMES D. WELCH, SOLE PROPRIETOR.
FROM: U.S. DEPARTMENT OF ENERGY, ENERGY RELATED INVENTIONS.
PROJECT: NOVEL METHOD FOR MAKING SEMICONDUCTOR CHIPS.

FIFTH QUARTERLY REPORT

INVENTION NO.: 534
OERI NO.: 012693

FOR PERIOD BEGINNING: JULY 7, 1994
AND ENDING: OCTOBER 7, 1994

THE FOLLOWING MATERIAL TYPED IN NONCAPITAL LETTERS WAS SUBMITTED AS AN UPDATE TO THE FORTH QUARTERLY REPORT AT THE REQUEST OF FRED HART, AFTER I TOLD HIM OF THE OVERCOMING OF A PROBLEM BASED IN TEST SET OPERATION WHICH HAD BEEN INTERMITTANTLY MASKING DETECTION OF SUCCESSFUL RESULTS.

July 25, 1994

Fred Hart
DOE-CE521
1000 Independence Avenue
Washington, D.C. 20585

Dear Fred;

As per your request in our telephone conversation this morning, I am providing this updated disclosure.

As the latest Quarterly Report I submitted stated, I have for quite some time been having trouble achieving repeatable MOSFET curves from the numerous devices we have been fabricating.

I literally stumbled onto curves from devices formed on P-type silicon, which devices had no gate metal remaining, back on April 27, 1994, and on the next day had similar luck finding curves from devices formed on N-type silicon. I found that by positioning the Gate probe atop the silicon dioxide, I could, at

times, effect MOSFET action. (I guess this is why I have some success in research. I try things which others would assume would not work). This result is recited in the latest Quarterly Report. However, the results were difficult to repeat. Said problem, however, provided encouragement and a shot of adrenalin to lead us to develop devices with a stable Gate metal remaining, and as I recited in the latest Quarterly Report we have achieved that. The procedure we used to achieve that is recited in the latest Quarterly Report. Briefly, we have added an aluminum deposition step to that end. The remaining problem was that we did not find MOSFET curves when we tested said devices. That was initially extremely discouraging. However, I was assuming that the test equipment I was using was working, and not believing that our devices with Gate metal would not work in view the initial, "stumbled onto", curves I set to work investigating the test equipment. I've recently discovered that assuming the test equipment was working was not a justified assumption. It does "basically" work, but there has been an almost impossible to detect intermittant problem right the way along. It is almost a miracle I ever found the initial curves I did in view thereof.

One of the three prong to two prong interface adaptors on the HP 4145B Curve Tracer seems to have oppositely directed diodes therein between the center lead and the outer braid. It breaks down at approximately 0.76 volts therebetween. Testing it and its attached cable with an ohm meter, which I did months ago, from the opposite end of the cable, does not show any problem to exist as its not a direct short. It is a true "Gotcha" type problem. Now, when that interface adaptor is present on the Source lead, its defect is shorted out by Curve Tracer internal circuitry. When I happened to have said interface adaptor at that location I would find curves. When it happened to be on the Gate or Drain lead, it served to short out the voltage I assumed was reaching the devices being tested.

In short, I can now repeatably obtain MOSFET curves from devices with a metal Gate remaining. I am also again able to repeatably obtain MOSFET curves from the devices without a Gate metal, from which I initially achieved success. As well, I have even achieved MOSFET curves from devices in which a two micron etch into the silicon was performed.

We are now in a position to move forward in a "bit higher gear".

I have ordered some high quality oxide substrates to use in our future work. We can grow oxide, but that we've produced to date is not of the quality we should be achieving. For instance, recent Capacitance Voltage curves show onset of N-Channel inversion on P-type silicon to be at approximately negative four (-4.0) volts which . This matches the onset of Drain Current in tested MOSFETS, which is a very encouraging correlation. This

strongly indicates we are seeing what we think we are seeing, (ie. MOSFET action) in tested devices.

Now, in view of these results, I've postulated a new device. A single device equivalent to CMOS. This device not only saves energy in fabrication in the steps after formation of a checkerboard in a silicon substrate---it eliminates the need to form the checkerboard! I have a new Patent Application already Pending which Claims this device along with additional material.

Please send me the Forms so that I can apply for another Grant to allow me to investigate the proposed single device equivalent to CMOS. It meets the guidelines of energy savings.

If you have questions, do call.

Do send the new Grant Application Forms ASAP---Thanks.

Sincerely,

JAMES D. WELCH
JW/hs

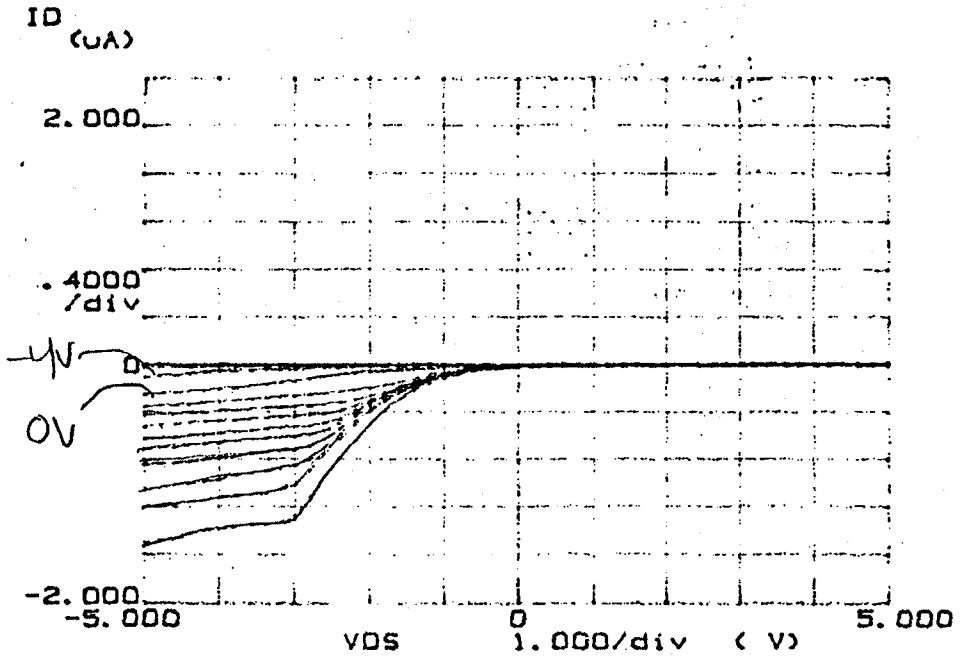
ENC. Copies of MOSFET Curves recently achieved from devices formed on P-type silicon, (which devices have Gate metal remaining, and curves from devices formed on N-type silicon in which a two micron silicon etch was performed prior to chromium deposition. The later devices have no Gate metal remaining, and the Gate probe serves as a Gate metalization.
The Drain to Source onset of current conduction variation is considered to be the result of leakage current through our present quality silicon dioxide, into the Gate circuitry. This defect should be eliminated by use of our ordered high quality oxide substrates in future fabrication efforts.
Also, copy of recently achieved Capacitance-Voltage curves form MOS Capacitors formed on P-type Silicon upon which we grew silicon oxide. Correlates with onset of Drains current in MOSFET devices. Indicates strong positive ion contamination.

ADDITIONAL MATERIAL

I HAVE RECENTLY PREPARED AND SUBMITTED AN ADDITIONAL GRANT APPLICATION TO THE NIST IN WHICH PROFESSORS SOUKUP AND IANNO ARE IDENTIFIED AS CONSULTANTS AND WHICH THE UNIVERSITY OF NEBRASKA IS NAMED AS THE RESEARCH FACILITY, (NOTE I PROVIDED A COPY TO FRED HART), THROUGH THE ENERGY RELATED INVENTION PROGRAM, WHICH APPLICATION REQUESTS ADDITIONAL FUNDS TO CONTINUE THE PRESENT WORK AFTER THE PRESENT GRANT EXPIRES, IN VIEW OF THE PRESENT

Al Gate

****** GRAPHICS PLOT ******



Variable1:
VDS -Ch2
Linear sweep
Start -5.0000V
Stop 5.0000V
Step .2000V

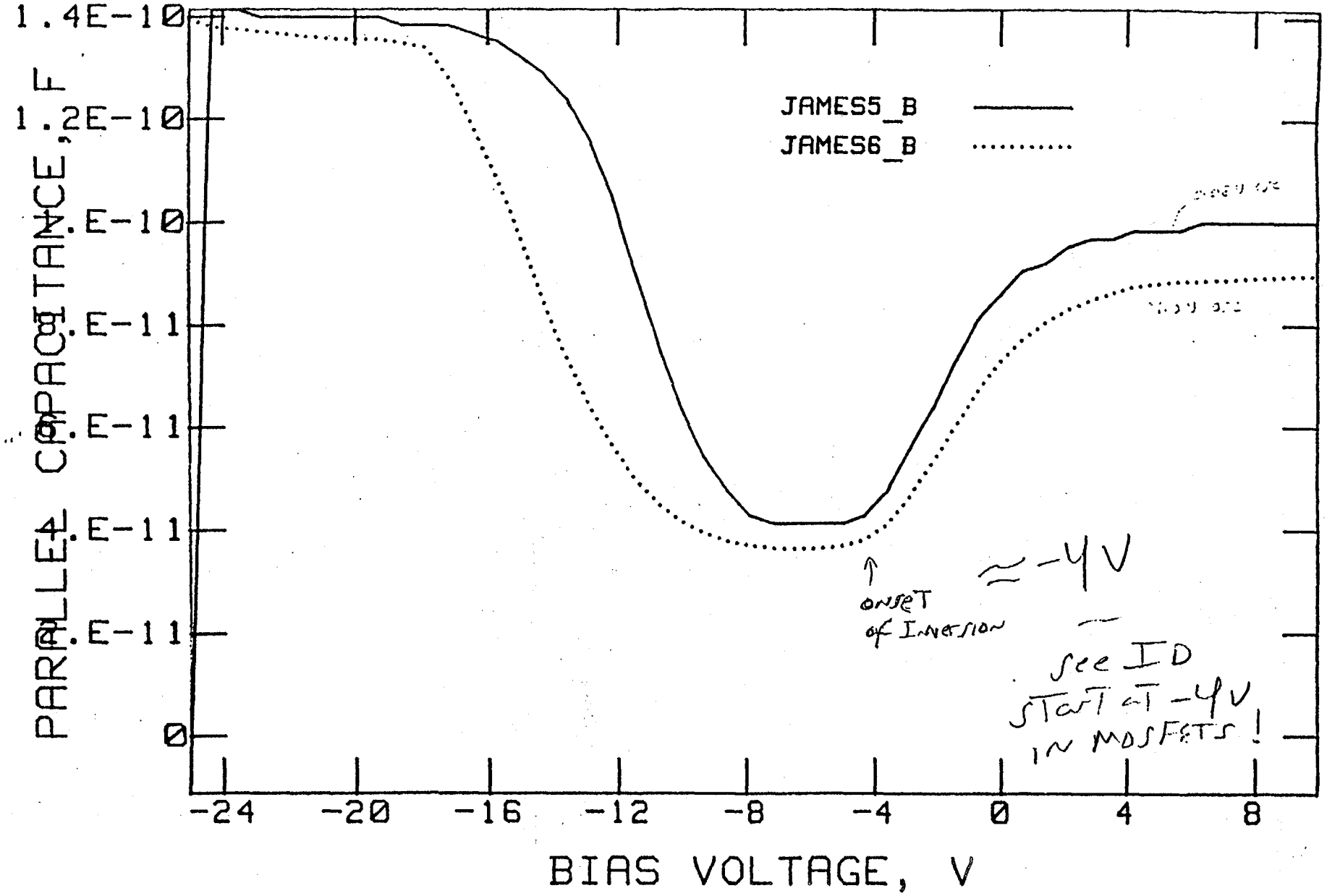
Variable2:
VG -Ch3
Start -10.000V
Stop 18.000V
Step 2.0000V

Constants:
VS -Ch1 .0000V

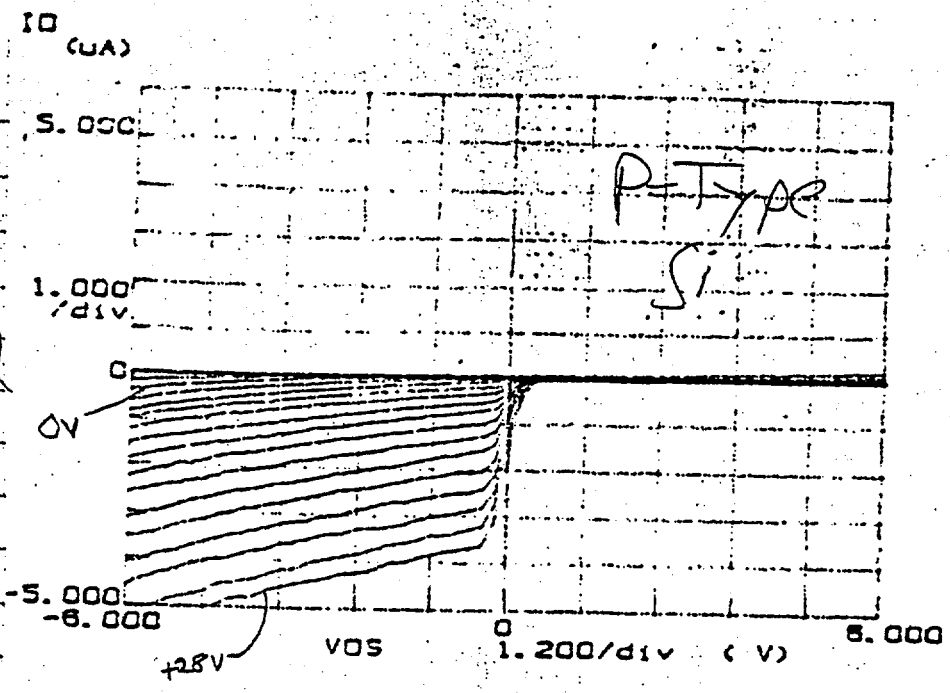
Gate Metal Present.

VGS Repeatable on Probe Stand

MOS CAPACITANCE-VOLTAGE



****** GRAPHICS PLOT ******



Variable1:
VDS -Ch2
Linear sweep
Start -6.000
Stop 6.000
Step .200

Variable2:
VG -Ch3
Start -10.00
Stop 28.00
Step 2.000

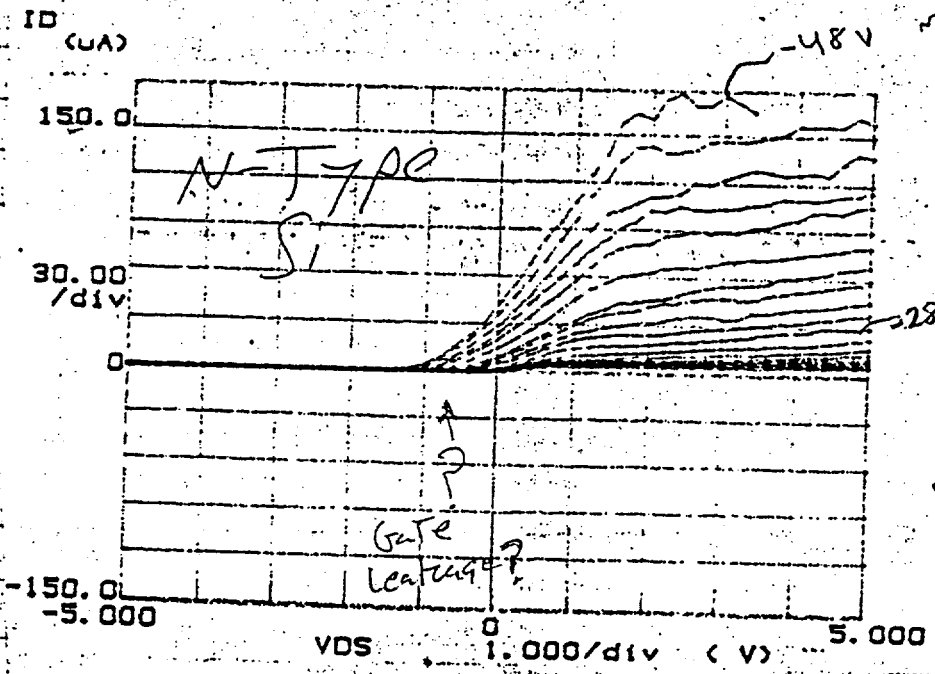
Constants:
VS -Ch1 .0000

-4V threshold

P-Type
Original substrate
Got April 27, 1994
Curves from
Why "0" volts off?
No Gate Metal

Have Faulty Adapter on Source Lead

****** GRAPHICS PLOT ******



no Gate Metal

Variable1:
VDS -Ch2
Linear sweep
Start -5.0000V
Stop 5.0000V
Step .2000V

Variable2:
VG -Ch3
Start -10.000V
Stop -48.000V
Step -2.0000V

Constants:
VS -Ch1 .0000V

N-Type
2μm etch into Si
See p 38 for
SEM —
No Gate
Metal

Have Faulty Adapter on Source Lead

SUCCESS. THE SCOPE OF INVESTIGATION IS EXPANDED TO INCLUDE FABRICATION OF SINGLE DEVICE EQUIVALENTS TO CMOS. THE APPLICATION HAS BEEN ACKNOWLEDGED BY GEORGE LEWETT AND PROVIDED AN IDENTIFICATION NUMBER IN A LETTER FROM THE NIST DATED SEPTEMBER 3, 1994.

REGARDING PRESENT EFFORTS, WE HAVE CONTINUED TO MOVE ALONG. THIS HAS INCLUDED FABRICATION AND TESTING OF NUMEROUS ADDITIONAL DEVICES. I OBTAINED 2000 ANGSTROMS OF HIGH QUALITY SILICON OXIDE GROWN ON BOTH N AND P-TYPE SUBSTRATES, OF VARIOUS DOPING LEVELS, AS FOLLOWS:

TYPE	DIAMETER	DOPING	QUANTITY
P	4 INCH	6×10^{15}	1
P	3 INCH	2×10^{15}	3
P	3 INCH	5×10^{14} - 1×10^{15}	2
N	3 INCH	1×10^{15} - 2×10^{15}	3
N	3 INCH	1×10^{15}	1

DEVICE FABRICATION ON P-TYPE SUBSTRATES DOPED 5×10^{14} TO 1×10^{15}, 2×10^{15} AND 6×10^{15} PER CENTIMETER CUBED PROVIDED WORKING DEVICES ON THE LOWER AND HIGHER DOPED SUBSTRATES. THE ALUMINUM ETCH, HOWEVER, WAS NOT SUCCESSFUL ON THE MID-RANGE DOPED SUBSTRATE HOWEVER AND DEVICES FORMED THEREON DID NOT OPERATE. IN ADDITION, THE ALUMINUM ETCH ON AN N-TYPE SUBSTRATE DOPED $1\text{-}2 \times 10^{15}$ WAS ALSO UNSUCCESSFUL. AN IMMEDIATE ATTEMPT TO REPEAT SAID UNSUCCESSFUL FABRICATION WAS UNSUCCESSFUL AS A GRADUATE ASSISTANT MISTAKENLY DEPOSITED CHROMIUM OXIDE, RATHER THAN CHROMIUM, IN THE FABRICATION PROCEDURE. THE CHROMIUM OXIDE TARGET HAD BEEN USED EARLIER IN ANOTHER RESEARCH PROJECT AND WAS MISTAKENLY ASSUMED TO BE A CHROMIUM TARGET. BRIEF INVESTIGATION OF DEVICES FORMED ON N-TYPE SILICON UPON WHICH CHROMIUM OXIDE WAS DEPOSITED WILL BE MENTIONED AGAIN SUPRA.

CONTINUING, CURVES OBTAINED FROM THE DEVICES FABRICATED ON THE LOWER AND HIGHER DOPED SUBSTRATES PROVIDED SOME INTERESTING INITIAL RESULTS. INITIAL MONITORING OF 'DRAIN CURRENT V. DRAIN TO SOURCE VOLTAGE' ON SAID DEVICES SHOW RELATIVELY GOOD DRAIN CURRENT SATURATION CHARACTERISTICS ON THE LOWER DOPED P-TYPE SUBSTRATE, WITH SATURATION TAKING PLACE IN THE MICROAMP RANGE, (SEE FIG. N-1). INITIAL TESTING OF DEVICES FABRICATED ON THE HIGHLY DOPED P-TYPE SUBSTRATE SHOW LITTLE DRAIN CURRENT SATURATION CHARACTERISTICS AND MUCH HIGHER DRAIN CURRENT, (ON THE

ORDER OF 50 MICROAMPS), BEING EFFECTED BY SIMILAR APPLIED GATE VOLTAGE, (SEE FIG. N-2).

ASSOCIATED MOSFET CAPACITANCE V. APPLIED VOLTAGE (C-V), CURVES WERE OBTAINED FOR THE HEAVILY DOPED P-TYPE SUBSTRATE. C-V PLOTS PRESENT CAPACITANCE V. APPLIED VOLTAGE WITH FREQUENCY BEING A VARIABLE PARAMETER. TO OBTAIN THE C-V CURVES ALUMINUM WAS APPLIED TO THE BACK OF A SUBSTRATE, (FROM WHICH THE SILICON DIOXIDE HAD BEEN REMOVED), AND DOTS OF ALUMINUM WERE APPLIED TO THE TOP OF THE REMAINING SILICON DIOXIDE ATOP THE SUBSTRATE. THIS RESULTED IN A MOS CAPACITOR WITH THE SILICON DIOXIDE SERVING AS THE DIELECTRIC.

THE TEST RESULT FOR THE P-TYPE SUBSTRATE DOPED 6×10^{15} INITIALLY PROVIDED C-V CURVES WHICH INDICATED NO INVERSION WAS OCCURRING AT THE SILICON DIOXIDE-SILICON INTERFACE FOR ANY APPLIED VOLTAGE, (SEE FIG N-3). AS A RESULT THE MOS CAPACITOR WAS SUBJECTED TO A FIFTEEN MINUTE 400 DEGREE CENTIGRADE ANNEAL PROCESS. PROFESSOR SOUKUP SUGGESTED THAT THIS MIGHT ELIMINATE ANY NON-OHMIC JUNCTION PRESENT AT THE BACK OF THE SUBSTRATE BETWEEN DEPOSITED ALUMINUM AND THE SILICON, WHICH NON-OHMIC JUNCTION MIGHT BE MASKING THE EFFECT WE WERE EXPECTING. AFTER SAID ANNEAL THE C-V CURVES SHOWED SOME INDICATION OF INVERSION, (SEE FIG. N-4). HOWEVER, AS SHOWN IN FIG. N-4 THE EFFECT WAS NOT STRONG AS MIGHT BE EXPECTED FROM REFERENCE TO CLASSICAL TEXTBOOK EXAMPLES, (SEE COPY OF GRAPH FROM A BOOK TITLED "PHYSICS AND TECHNOLOGY OF SEMICONDUCTOR DEVICES" BY GROVE, (SEE FIG. N-5). THIS LACK OF STRONG INVERSION MIGHT EXPLAIN WHY THE HEAVILY DOPED P-TYPE SUBSTRATE DID NOT SHOW GOOD DRAIN CURRENT SATURATION CHARACTERISTICS.

SIMILAR C-V PLOTS WERE OBTAINED FROM MOS CAPACITORS FABRICATED ON A P-TYPE SUBSTRATE DOPED 2×10^{15} AND ARE SHOWN IN FIG. N-6. THESE RESULTS ARE A BIT MORE LIKE WHAT IS EXPECTED, IN THAT A MORE PRONOUNCED DEFINITE INVERSION IS INDICATED. AS WELL, IT MUST BE REMEMBERED THAT DEVICES FABRICATED ON LOWER DOPED SUBSTRATES SHOW MUCH BETTER DRAIN CURRENT INVERSION CHARACTERISTICS.

AT THIS STAGE OF INVESTIGATION WE FEEL VERY STRONGLY THAT WE ARE SEEING MOSFET ACTION FROM THE DEVICES WE ARE FABRICATING ON BOTH N AND P-TYPE SILICON. WE ALSO FEEL THAT DOPING LEVEL OF A SUBSTRATE UPON WHICH DEVICES ARE FABRICATED HAS A PRONOUNCED EFFECT ON THE DRAIN CURRENT V. DRAIN TO SOURCE VOLTAGE CURVES OBTAINED. INITIAL DIRECT INVESTIGATION THEREOF WITH A CURVE TRACER, AND INVESTIGATION OF C-V PLOTS INDICATES THAT THIS IS THE CASE. IT MUST BE EMPHASISED HOWEVER, THAT MANY DIFFICULT TO CONTROL VARIABLES EXIST WHEN INVESTIGATING NEW ELECTRONIC DEVICES. WHILE WE FEEL WHAT IS PRESENTED HEREIN ARE VALID DATA AND PRELIMINARY INTERPRETATION THEREOF, A GREAT DEAL MORE

PRECISION AND INVESTIGATION IS REQUIRED TO DEVELOP CERTAINTY.

CONTINUING, IT WAS MENTIONED THAT AN IMMEDIATE ATTEMPT TO FABRICATE DEVICES ON A MID-DOPED P-TYPE AND ON AN N-TYPE SUBSTRATE, (TO REPLACE THE DEVICE FABRICATION WHICH WAS NOT SUCCESSFUL ON SAID SUBSTRATES), RAN INTO A PROBLEM WHEN AN ASSISTANT MISTAKENLY DEPOSITED CHROMIUM OXIDE RATHER THAN CHROMIUM AT THE APPLICABLE STEP IN THE FABRICATION PROCEDURE. I INVESTIGATED THE RESULTING DEVICES FABRICATED ON THE N-TYPE SUBSTRATE WITH THE CURVE TRACER AND FOUND THAT CURVES WERE OBTAINABLE. SEE FIG. N-7. THE INTERESTING ASPECT OF THE CURVES IS THE APPEARENT PRESENCE OF NEGATIVE RESISTANCE IN THE DRAIN CURRENT V. DRAIN TO SOURCE VOLTAGE, WHEN CERTAIN GATE VOLTAGES ARE APPLIED. THIS EFFECT MIGHT BE SOMETHING DESERVING ADDITIONAL INVESTIGATION, BUT NOTHING MORE IS STATED AT THIS TIME.

INCLUDED IN FIGS. N-8 THROUGH N-12 ARE DRAIN CURRENT V. DRAIN TO SOURCE VOLTAGE FOR A DEVICE FABRICATED ON P-TYPE SILICON. THE SAME CURVES ARE SHOWN ON VARIOUS CURRENT RANGE SCALES. SAID CURVES SHOW THAT APPLIED GATE VOLTAGE DEFINITELY AFFECTS DRAIN CURRENT. APPLIED NEGATIVE GATE VOLTS IN THE POSITIVE DRAIN TO SOURCE VOLTAGE RANGE LEADS, (AT -10 VOLTS), TO THE PRESENCE OF APPROXIMATELY 20 MICROAMPS. APPLICATION OF POSITIVE GATE VOLTS, (AT +10 VOLTS), TO THE FLOW OF APPROXIMATELY 0.8 MICROAMPS IN THE NEGATIVE DRAIN TO SOURCE VOLTAGE RANGE.

WE ARE CONTINUING TO FABRICATE OPERATING DEVICES AND DO INVESTIGATION THEREOF WITH AN EYE TO GATHERING AS MUCH DATA AS POSSIBLE. HOWEVER, WE ARE STILL AT THE INITIAL STAGES OF THAT EFFORT, AND WHILE IT IS EXPECTED THAT ADDITIONAL TESTING WILL SUPPORT THE RESULTS PRESENTED HEREIN, IT IS TO EXPECTED THAT AS VARIABLES ARE BETTER CONTROLLED, MODIFICATIONS IN THE DATA WILL RESULT AND THAT REPEATABILITY WILL IMPROVE.

IN THE NEXT QUARTER I HOPE TO CONFIGURE STABLE DEVICES FORMED ON BOTH N AND P-TYPE SILICON INTO A CMOS ARRANGEMENT AND DOCUMENT CMOS SWITCHING ACTION THEREFROM AS A FUNCTION OF APPLIED GATE VOLTAGE.

IT IS NOTED THAT AT THIS TIME IT IS NOT PLANNED TO FABRICATE CMOS ON A SINGLE SUBSTRATE WHICH REQUIRES FORMATION OF THE P AND N-TYPE CHECKERBOARD. FORMATION OF A CHECKERBOARD IS STANDARD TECHNOLOGY IN INDUSTRY AND OUR ABILITY TO DUPLICATE IT WOULD NOT PROVIDE ANY VALUABLE DATA. AT THIS TIME WE FEEL THAT OUR EFFORTS ARE BETTER APPLIED TO FABRICATION AND INVESTIGATION OF SCHOTTKEY BARRIER MOSFETS ON SEPARATE N AND P-TYPE SILICON SUBSTRATES. THERE IS A LOT LEFT TO BE DONE TO ARRIVE AT STABLE REPEATABLE RESULTS IN THE AREA. AS WELL, IN VIEW OF THE NEW PROPOSAL FOCUSING UPON A SINGLE DEVICE EQUIVALENT TO CMOS, FOR WHICH A GRANT APPLICATION IS NOW SUBMITTED FOR CONSIDERATION TO THE NIST AS DISCLOSED ABOVE, OUR ABILITY DUPLICATE A STANDARD FORMATION OF

A CHECKERBOARD IS FELT TO BE A NONOPTIMUM USE OF RESEARCH TIME AND EFFORT.

I MIGHT MENTION THAT A CONCERN AT THE PRESENT TIME IS THAT WHILE WE DO SEE GATE VOLTAGE INFLUENCE ON DRAIN CURRENT IN THE DEVICES RECENTLY FABRICATED, IN WHICH GATE METAL IS PRESENT, THE GATE VOLTAGES AT WHICH THE MOST SIGNIFICANT EFFECT IS SEEN, ARE IN EXCESS OF THE APPLIED DRAIN TO SOURCE VOLTAGE, (EG. GATE VOLTS GREATER THAN 10 VOLTS AND DRAIN TO SOURCE VOLTS 0 TO 5 VOLTS). THIS IS NOT SUITABLE FOR APPLICATION IN A CASCADED LOGIC SYSTEM. AS WELL, IN A FEW OF OUR PRESENTLY FABRICATED DEVICES, THE CHROMIUM-DISILICIDE-SILICON RECTIFYING JUNCTIONS HAVE A REVERSE BREAKDOWN VOLTAGE OF APPROXIMATELY 10 VOLTS, THEREBY PREVENTING APPLICATION OF HIGHER DRAIN TO SOURCE OPERATING VOLTAGES. IT WILL BE RECALLED THAT THE INITIALLY OBTAINED DRAIN CURRENT V DRAIN-TO-SOURCE VOLTAGE (ID V. VDS) CURVES, ON SUBSTRATES IN WHICH NO GATE METAL WAS PRESENT SHOWED A MORE REASONABLE DRAIN CURRENT CONTROL AS A FUNCTION OF APPLIED GATE VOLTAGE WITHIN A GATE VOLTAGE RANGE OF +/- 5 VOLTS. IN SAID CASES A MUCH SMALLER EFFECTIVE GATE WIDTH WAS PRESENT, BEING ON THE ORDER OF 3 MILLS, THE WIDTH OF A PROBE STAND PROBE. I AM BECOMING CONCERNED THAT SMALLER DIMENSION DEVICES THAN THOSE WE ARE NOW PRODUCING MIGHT BE REQUIRED TO ALLOW SUCCESSFUL APPLICATION TO PRODUCTION OF CMOS DEVICES BECAUSE LEAKAGE CURRENTS ARE LESS IN SMALL DIMENSION DEVICES, THEREBY ALLOWING APPLICATION AT LOWER FORWARD CURRENT LEVELS.

ANOTHER POINT WHICH IS NOW IN FOCUS IS THAT THE PROBE STAND APPLIED ELECTRICAL PROBE CONTACT PRESSURE HAS AN EFFECT ON THE CURVES ACHIEVED DURING TESTING. CHANGING PROBE PRESSURE CHANGES THE DRAIN (ID) CURRENT LEVELS AND ALSO SEEMS TO CHANGE EVEN THE SILICON DIOXIDE RESISTANCE LEVELS BETWEEN GATE AND SOURCE OR DRAIN. I HAVE OBSERVED OXIDE RESISTANCE LEVELS OF ESSENTIALLY SO HIGH AS TO BE OFF SCALE OF A METER, TO 35 MEGOHM TO AS LOW AS 2.5 MEGOHM. IN ADDITION, PUTTING A CURRENT METER IN SERIES WITH A GATE LEAD SHOWS THAT SOME CURRENT FLOWS IN THE GATE CIRCUIT WHEN THE DEVICES ARE "ON". THE CURRENT LEVEL IS ON THE ORDER OF 50 TIMES LESS THAT FLOWS IN THE DRAIN TO SOURCE PATH HOWEVER. THE CAUSE OF THIS CURRENT FLOW IS NOT PRESENTLY KNOWN. HOWEVER, IT SEEMS TO DECREASE TO ESSENTIALLY ZERO AT THE ONSET OF DRAIN TO SOURCE CURRENT FLOW. I AM INVESTIGATING THIS FURTHER.

AT THE PRESENT TIME WE HAVE A FABRICATION PROCEDURE WHICH REPEATABLY PROVIDES DEVICES WHICH WHEN TESTED SHOW EXPECTED (ID V. VDS) CURVES. MY EFFORTS PRESENTLY ARE FOCUSED UPON TESTING FABRICATED DEVICES FORMED ON SILICON OF VARIOUS DOPING LEVELS, AND ATTEMPTING TO COME TO SOME DECISION AS HOW TO OBTAIN DEVICES WITH LOW GATE THRESHOLD VOLTAGES AND INCREASED DRAIN CURRENT TO APPLIED GATE VOLTAGE SENSITIVITY. IT IS NOTED THAT RECENT TESTING OF DEVICES FABRICATED ON TWO-TIMES-TEN-

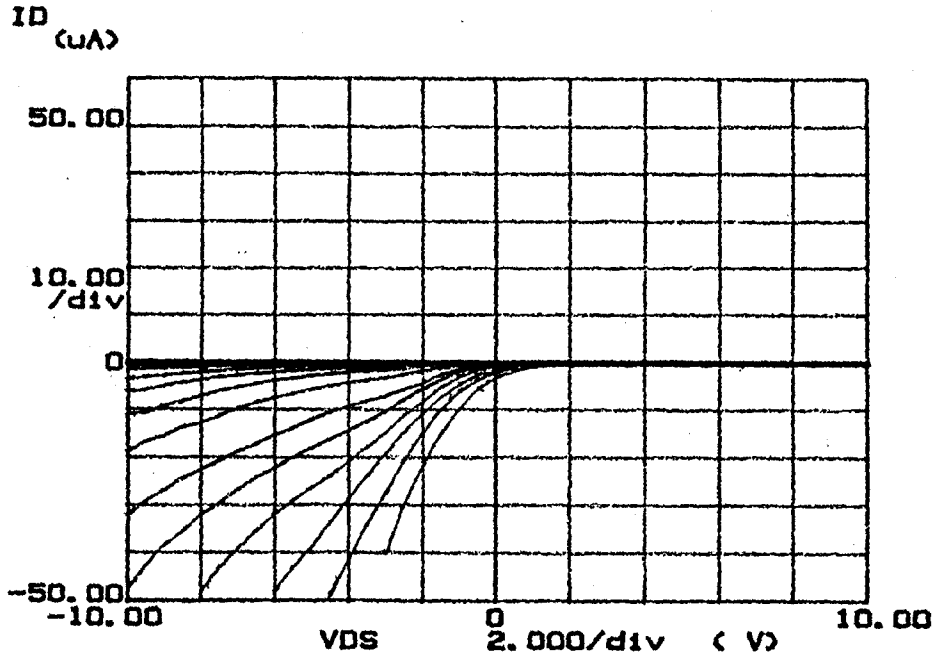
TO-THE-FIFTEENTH P-TYPE SHOWED THRESHOLD OF CONDUCTION AT LESS THAN ZERO VOLTS, MUCH AS DID THE ORIGINALLY TESTED DEVICES WITHOUT A GATE METAL, (SEE PREVIOUS QUARTERLY REPORTS). THIS IS ALSO NOT UNDERSTOOD AT THE PRESENT TIME.

I AM ALSO INCLUDING RECENTLY OBTAINED DRAIN CURRENT V. DRAIN TO SOURCE VOLTAGE CURVES FOR DEVICES FABRICATED ON BOTH P AND N-TYPE SILICON, (SEE FIGS. N-13 AND N-14). THESE FIGS. SHOW RELATIVELY BALANCED OPERATING CHARACTERISTICS AND JUNCTIONS WITH SUFFICIENTLY HIGH JUNCTION BREAKDOWN CHARACTERISTICS, (THAT IS THE CURVES SHOW THE JUNCTIONS DO NOT BREAK DOWN AT APPLIED VOLTAGES) TO BE USED IN A CMOS CONFIGURATION . I HOPE TO BE ABLE TO CONFIGURE THESE DEVICES INTO A FUNCTIONAL CMOS SERIES.

SINCERELY,

JAMES D. WELCH
JW/HS
ENC.

****** GRAPHICS PLOT ******



Variable1:
VDS -Ch2
Linear sweep
Start -10.000V
Stop 10.000V
Step .5000V

Variable2:
VG -Ch3
Start -10.000V
Stop 28.000V
Step 2.0000V

Constants:
VS -Ch1 .0000V

Fig. N-1

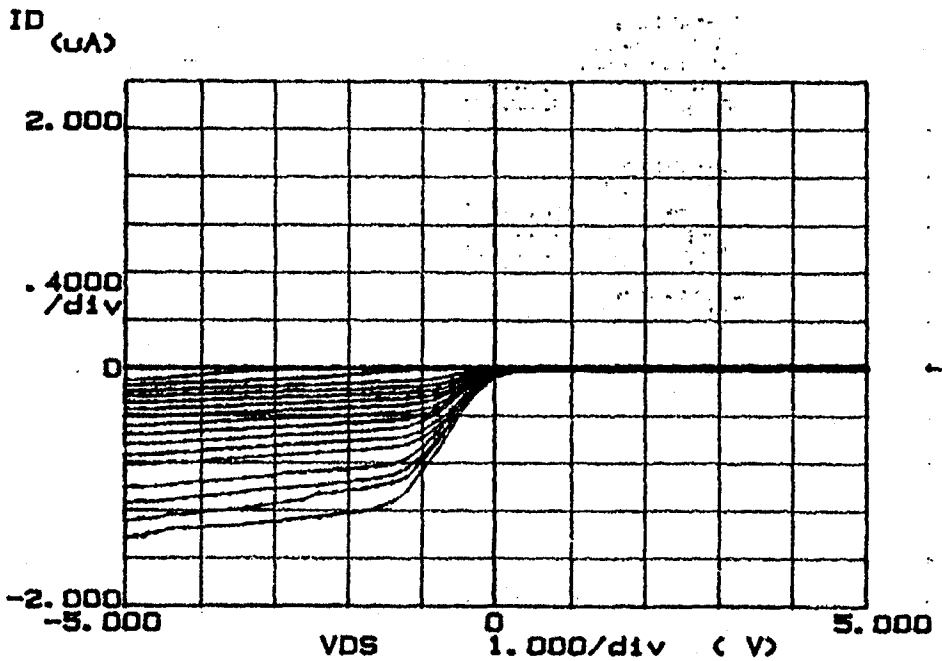

****** GRAPHICS PLOT ******
ID (uA)
2.000
.4000 /div
0
-2.000
-5.000
0
5.000
VDS
1.000/div (V)
Variable1:
VDS -Ch2
Linear sweep
Start -5.0000V
Stop 5.0000V
Step .2000V
Variable2:
VG -Ch3
Start -10.000V
Stop 25.000V
Step 2.0000V
Constants:
VB -Ch1 .0000V

Fig. IV-2

Jun 20

108 112

$6 \times 10^{15}/cm^3$

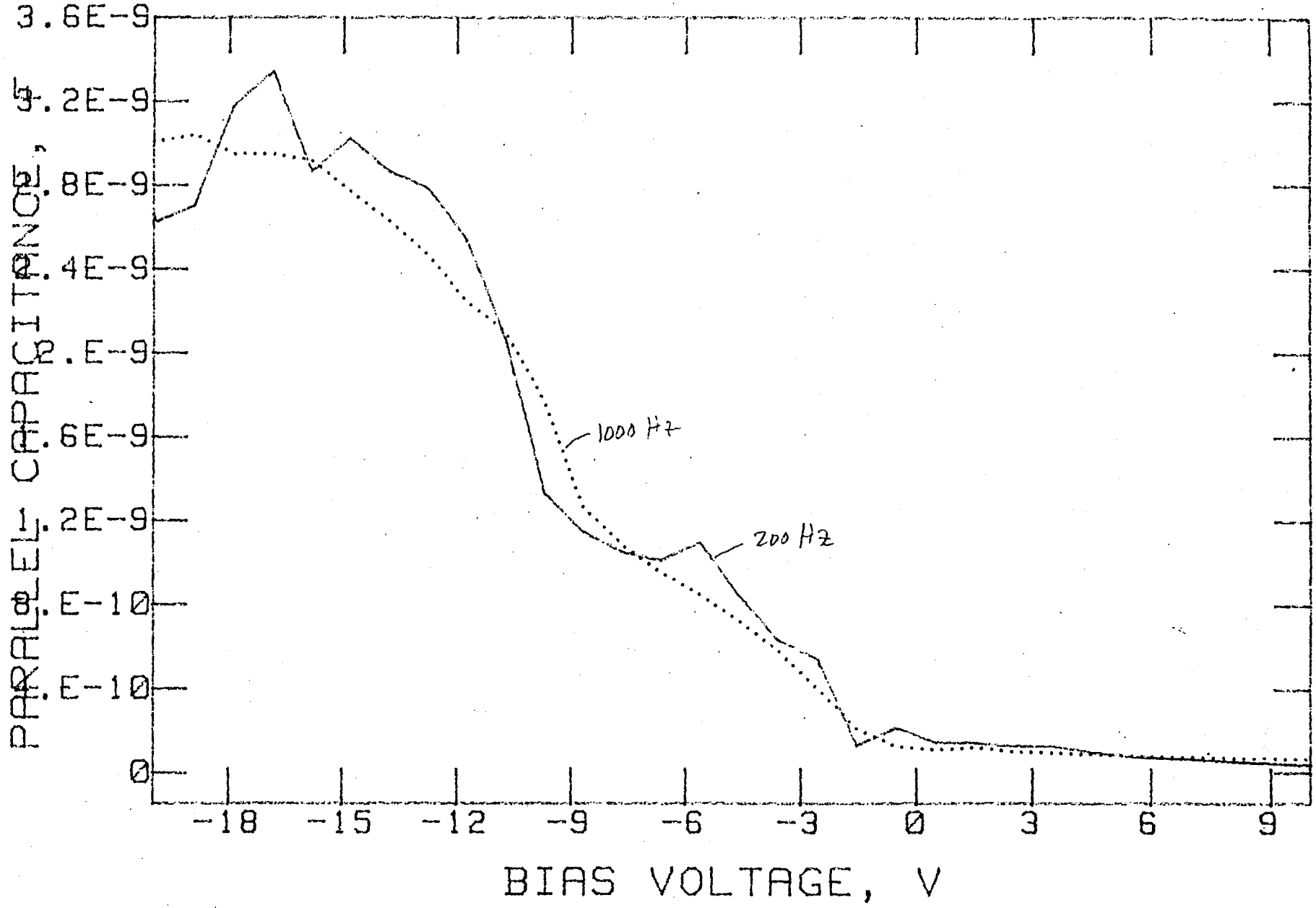


Fig V-3

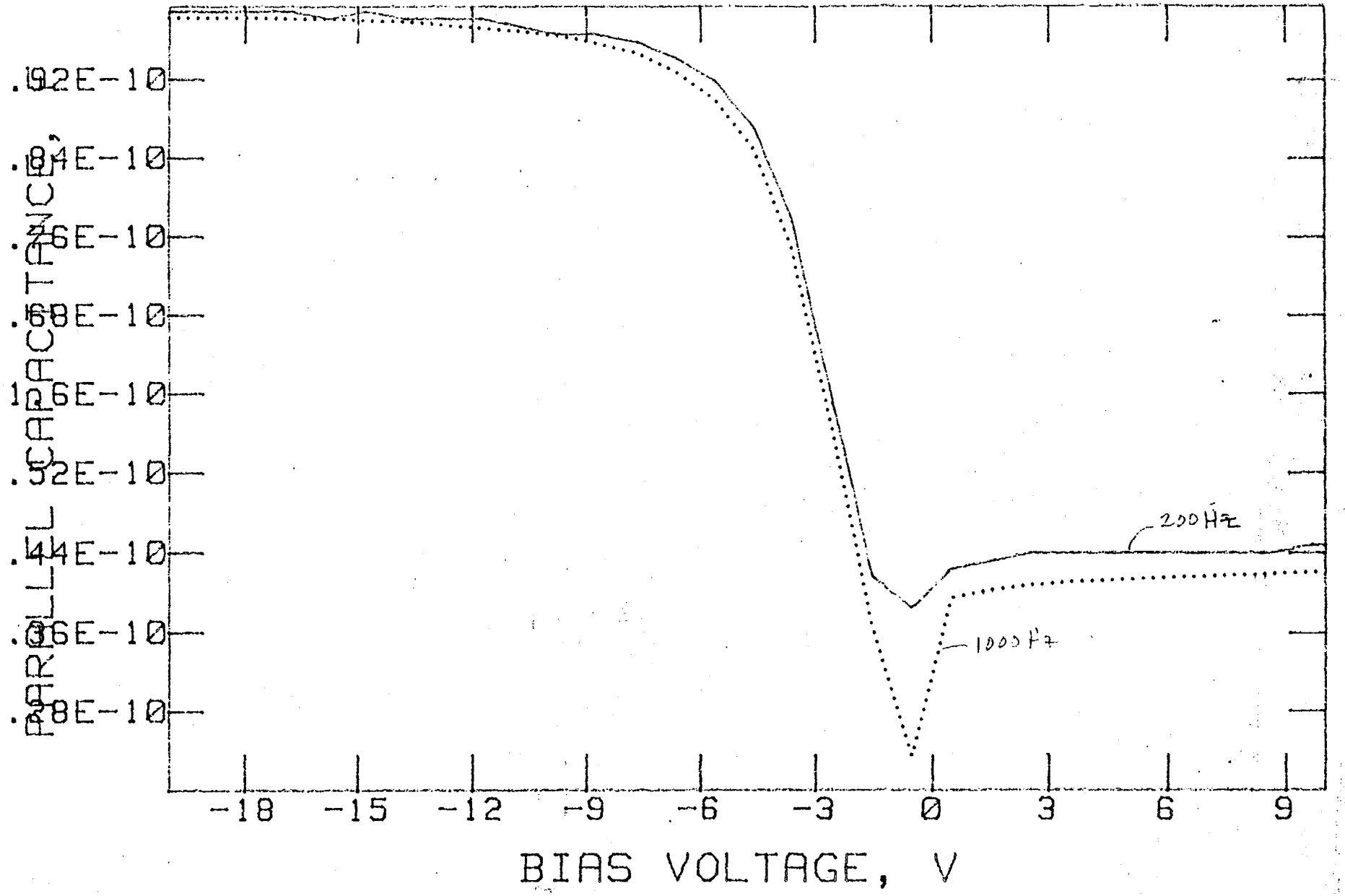

.92E-10
.84E-10
.76E-10
.68E-10
.6E-10
.52E-10
.44E-10
.36E-10
.28E-10
PARALLEL CAPACITANCE, C
-18
-15
-12
-9
-6
-3
0
3
6
9
BIAS VOLTAGE, V
200Hz
1000Hz

Fig. V-4

This is, in fact, what happens when the measurement frequency is high. If however the measurement frequency is low enough that recombination-generation rates can keep up with the small signal variation, then the recombination-generation mechanism will lead to charge exchange with the inversion layer in step with the measurement signal. In that case, the capacitance measured will approach that of the oxide layer alone.

To understand this better, let us consider what happens when a positive voltage applied to an MOS structure is increased by a small amount. Instantaneously, as the voltage is increased, more negative charge is induced in the silicon. At high frequencies, holes will be pulled out of the *p*-type semiconductor and the width of the depletion region will increase slightly, as shown in Figure 9.9a. If however electron-hole pairs can be generated fast enough, i.e., before the voltage is reduced again, the generated holes will replenish the holes pulled out from the edge of the depletion region and the extra electrons will appear in the inversion layer. Thus the incremental negative charge brought about by the incremental increase in gate voltage will appear at the oxide-silicon interface, as illustrated in Figure 9.9b. As a result, the capacitance measured will be that of the oxide layer alone, C_o.

As a consequence, the capacitance-voltage characteristics of metal-oxide-semiconductor structures are frequency dependent. Experimental measurements on an MOS structure corresponding to the computations given in Figure 9.8 are shown in Figure 9.10, for various measurement

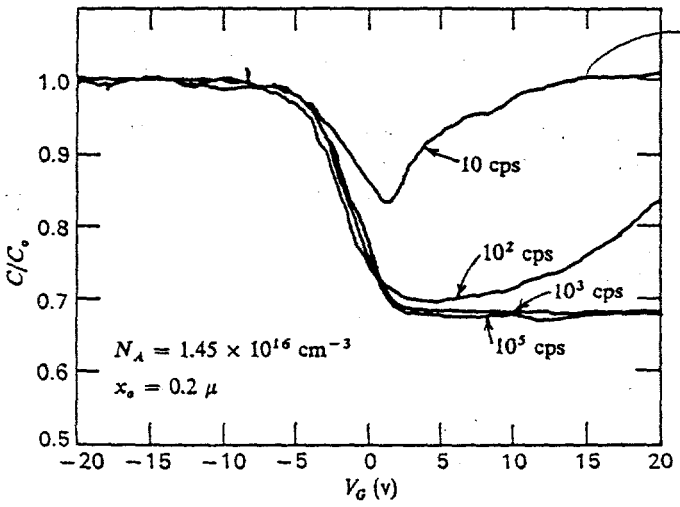


Fig. 9.10 The effect of measurement frequency on the capacitance-voltage characteristics of MOS structures.[5]

Jim 15
Jim 20

P-Type Si
$\approx 2 \times 10^{15}/cm^3$

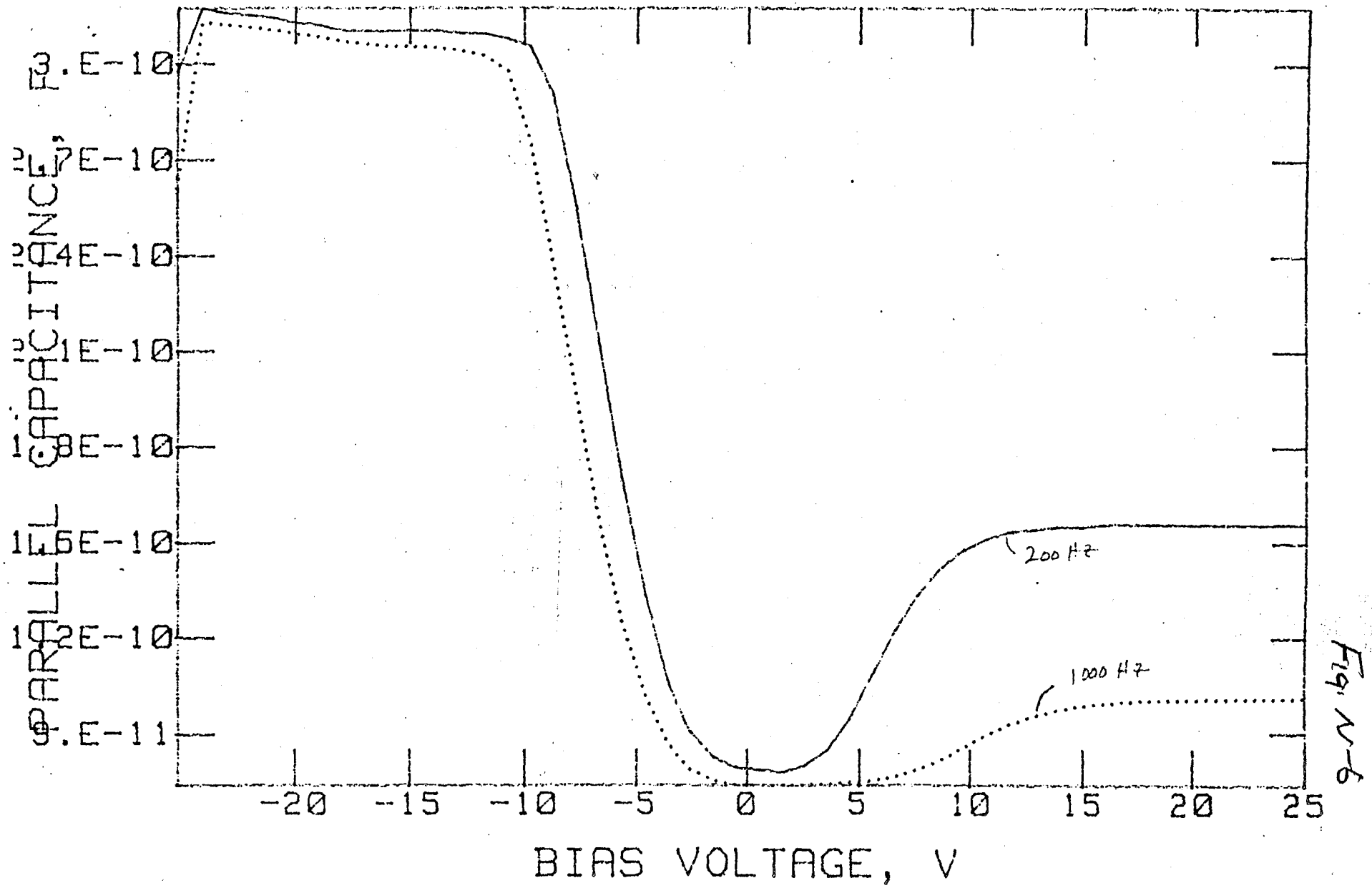
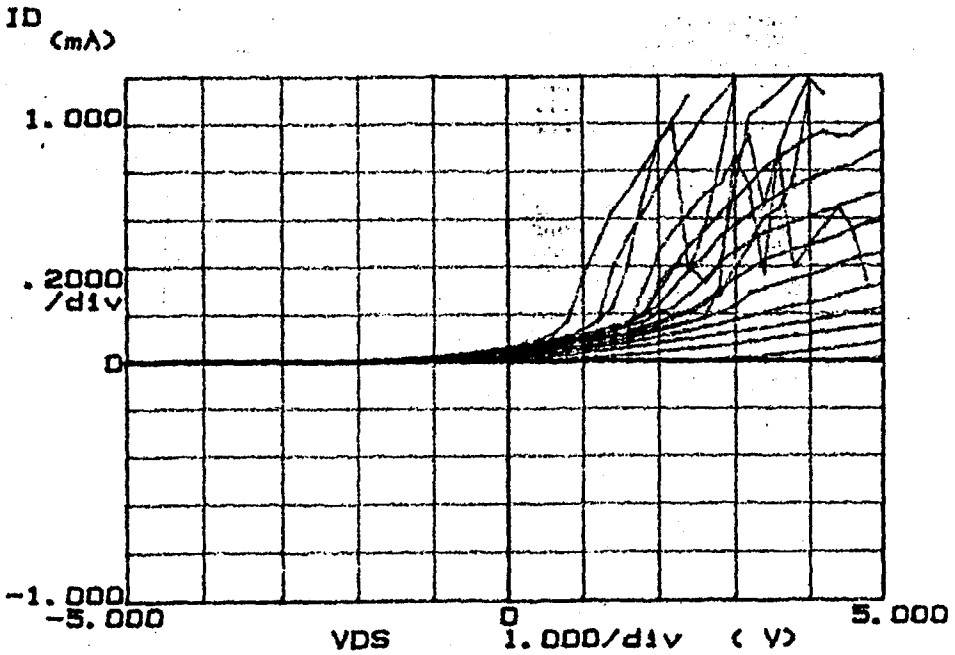


Fig. V-6

****** GRAPHICS PLOT ******



Variable1:
VDS -Ch2
Linear sweep
Start -5.0000V
Stop 5.0000V
Step .2000V

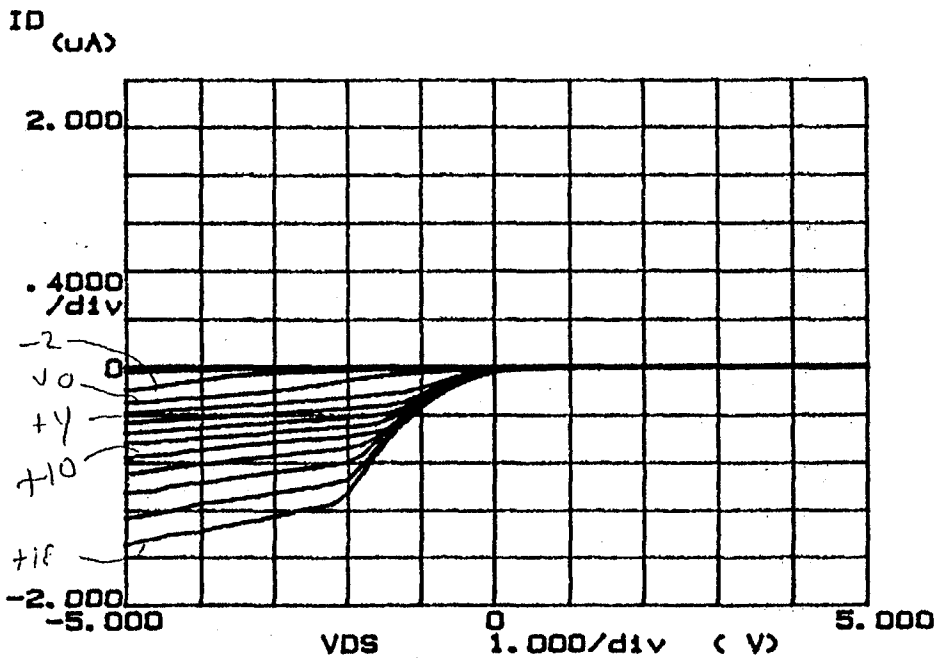
Variable2:
VG -Ch3
Start 10.000V
Step -20.000V
Step -2.0000V

Constants:
VB -Ch1 .0000V

Fig. N-7

Al gate

shutting



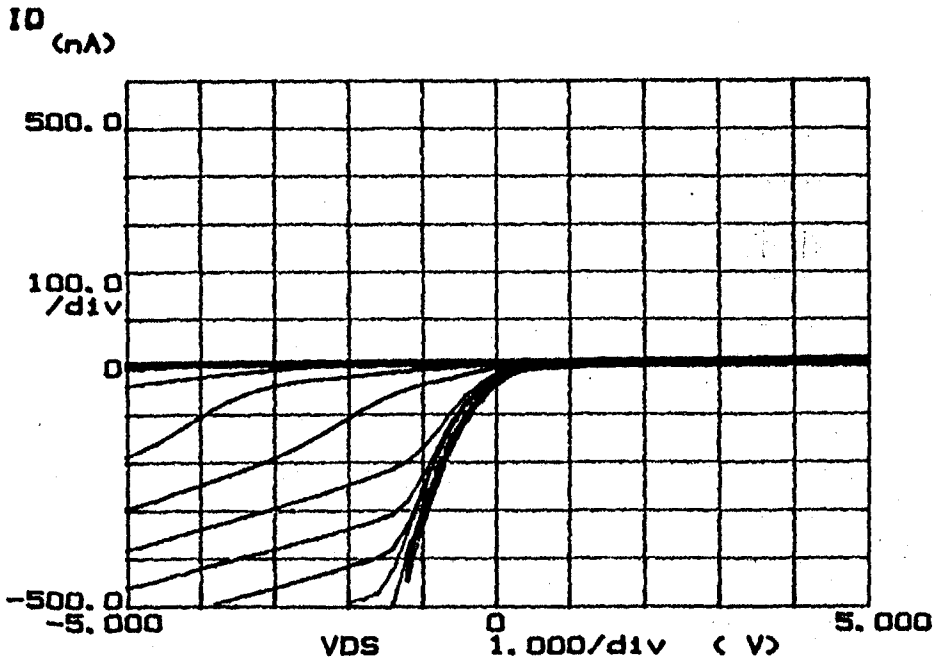
Variable1:
VDS -Ch2
Linear sweep
Start -5.0000V
Stop 5.0000V
Step .2000V

Variable2:
VG -Ch3
Start -10.000V
Stop 18.000V
Step 2.0000V

Constants:
VB -Ch1 .0000V

Fig. V-8

****** GRAPHICS PLOT ******



Variable1:
VDS -Ch2
Linear sweep
Start -5.0000V
Step 5.0000V
Step .2000V

Variable2:
VG -Ch3
Start -10.000V
Step 10.000V
Step 2.0000V

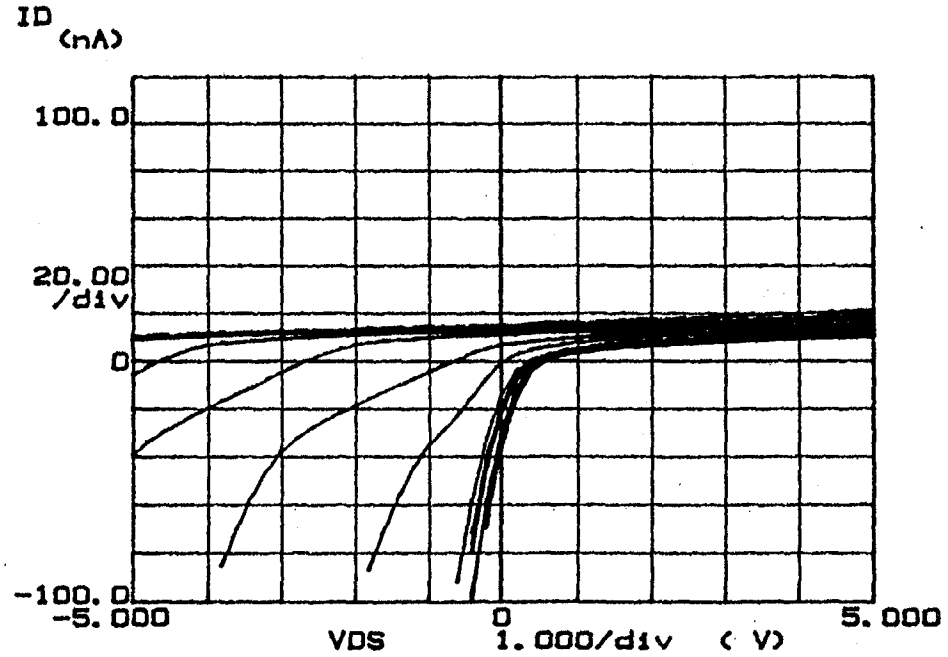
Constants:
VB -Ch1 .0000V

Fig. N-9

Al G.Te

+ IDUNA

****** GRAPHICS PLOT ******



Variable1:
VDS -Ch2
Linear sweep
Start -5.0000V
Stop 5.0000V
Step .2000V

Variable2:
VG -Ch3
Start -10.000V
Stop 10.000V
Step 2.0000V

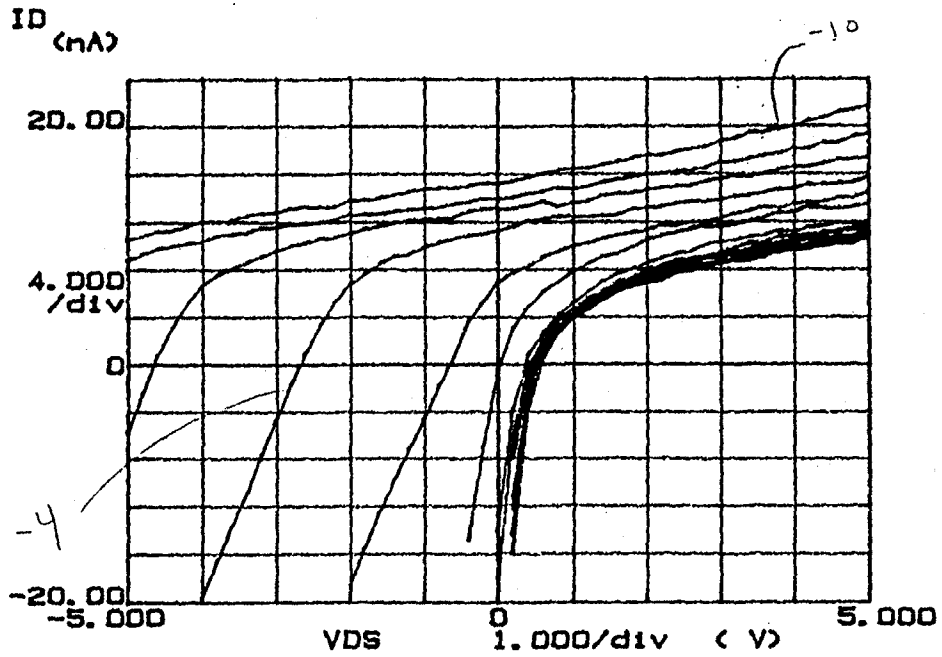
Constante:
VS -Ch1 .0000V

Fig N-10

P-Type
Al Gate

I 20nA

****** GRAPHICS PLOT ******



Variable1:
VDS -Ch2
Linear sweep
Start -5.0000V
Stop 5.0000V
Step .2000V

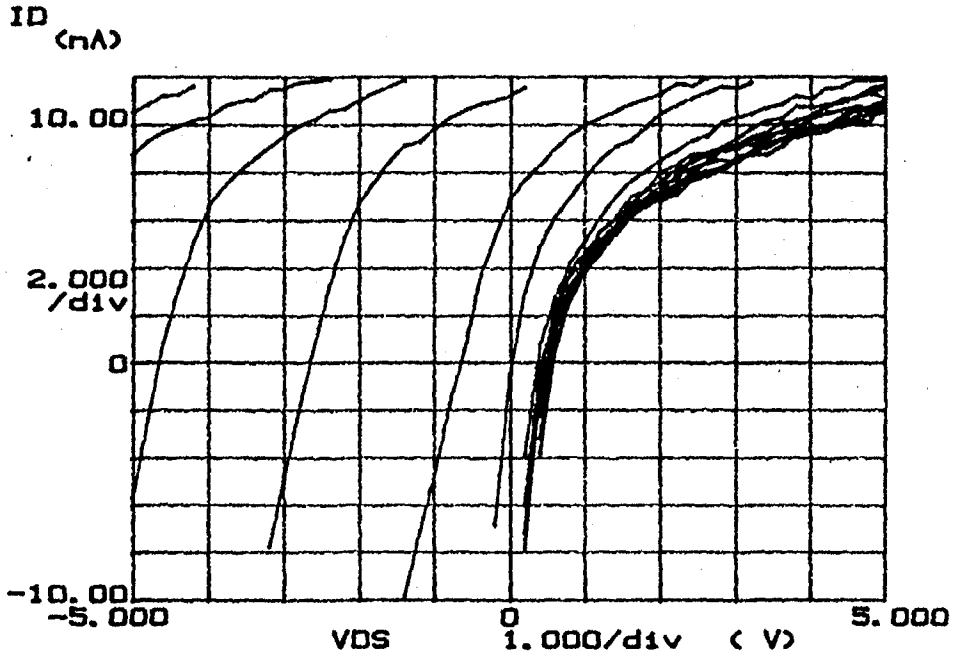
Variable2:
VG -Ch3
Start -10.000V
Stop 10.000V
Step 2.0000V

Constants:
VB -Ch1 .0000V

Fig. N-11

Al G
± 10 na

****** GRAPHICS PLOT ******



Variable1:
VDS -Ch2
Linear sweep
Start -5.0000V
Stop 5.0000V
Step .2000V

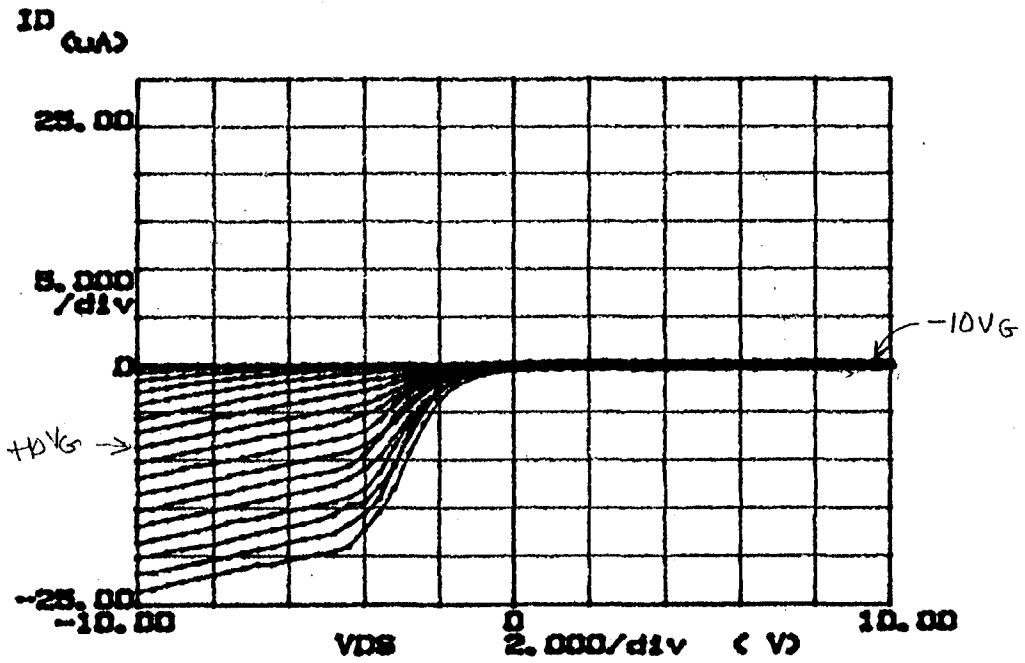
Variable2:
VG -Ch3
Start -10.000V
Stop 10.000V
Step 2.0000V

Constants:
VS -Ch1 .0000V

Fig. N-12

G-S GJ res

******* GRAPHICS PLOT *******

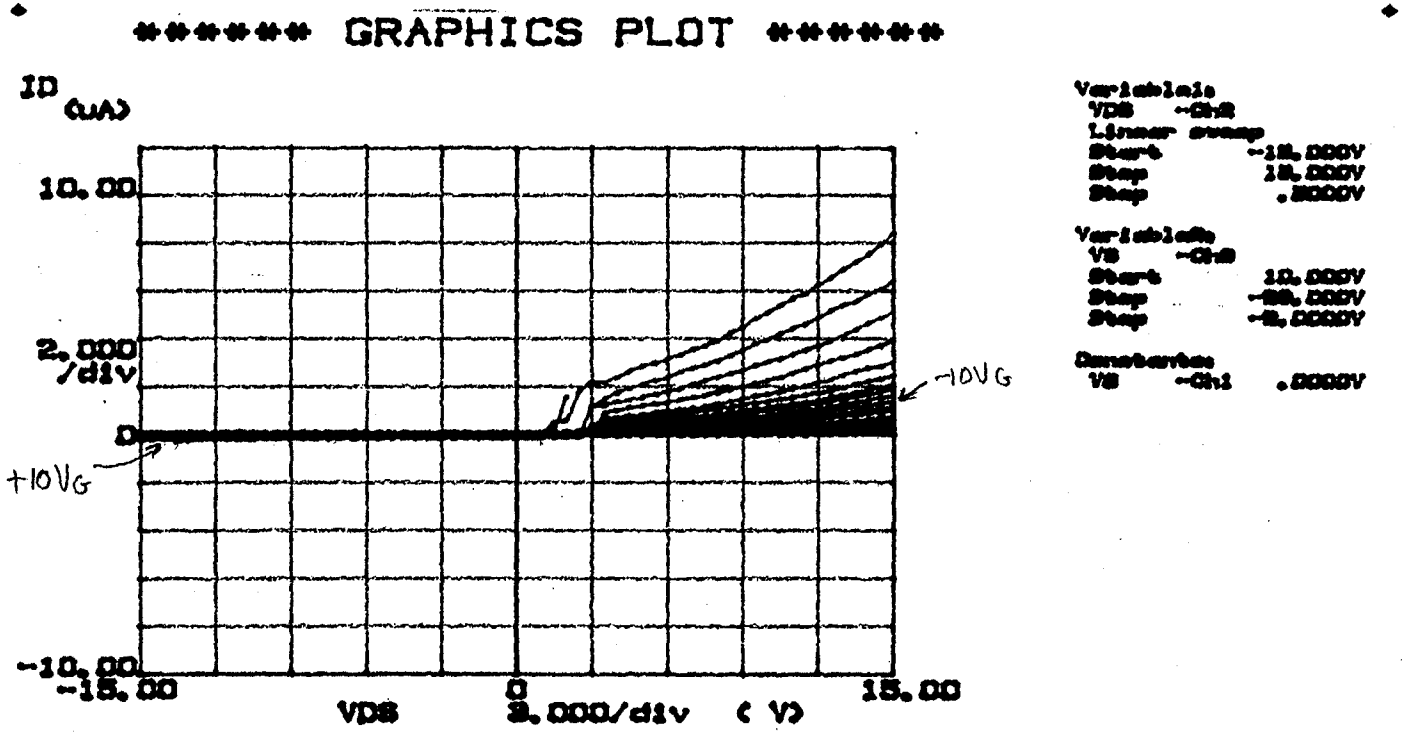


Variables
VDS -Ch2
Linear stepp
Start -10.000V
Stop 10.000V
Step .4000V

Variables
VG -Ch3
Start -10.000V
Stop 50.000V
Step 5.0000V

Constants
VG -Ch1 .0000V

N-13


******* GRAPHICS PLOT *******
ID (uA)
10.00
2.000 /div
0
-10.00
+10VG
-10VG
-15.00
0
15.00
VDS
2.000/div (V)
Variables
VDS -Ch2
Linear sweep
Start -15.000V
Stop 15.000V
Step .2000V
Variables
VG -Ch3
Start 10.000V
Step -2.0000V
Step -2.0000V
Parameters
VG -Ch1 .0000V

JAMES D. WELCH
ATTORNEY AT LAW
PROFESSIONAL ENGINEER

INTELLECTUAL PROPERTY
402-391-4448

10328 PINEHURST AVE.
OMAHA, NEBRASKA 68124

January 15, 1995

U.S. Department of Energy
Attn: Pat Simmons
Office of Scientific & Technical Information (OSTI)
P.O. Box 62
Oak Ridge, TN 37830

Administered for DOE
Kansas City Support Office
U.S. Department of Energy
911 Walnut, 14th Floor
Kansas City, MO 64106

DOE Project Officer
Anne Scheer
U.S. Department of Energy
911 Walnut, 14th Floor
Kansas City, MO 64106

U.S. Department of Energy
Department of the Controller
Payments Management Branch
P.O. Box 500
Germantown, MD 20784

RE: SIXTH QUARTERLY AND FEDERAL CASH TRANSACTIONS REPORT.
FEDERAL GRANT NO.: DE-FG47-93R701314.

Dear Sirs;

Please find enclosed the identified documents.

Sincerely,

JAMES D. WELCH
JW/hs
ENC.

JAMES D. WELCH
ATTORNEY AT LAW
PROFESSIONAL ENGINEER

NTELLECTUAL PROPERTY
402-391-4448

10328 PINEHURST AVE.
OMAHA, NEBRASKA 68124

JANUARY 15, 1995

RE: FEDERAL GRANT NO. DE-FG47-93R701314
COORDINATOR: FRED HART
TO: JAMES D. WELCH, SOLE PROPRIETOR.
FROM: U.S. DEPARTMENT OF ENERGY, ENERGY RELATED INVENTIONS.
PROJECT: NOVEL METHOD FOR MAKING SEMICONDUCTOR CHIPS.

SIXTH QUARTERLY REPORT

INVENTION NO.: 534
OERI NO.: 012693

FOR PERIOD BEGINNING: OCTOBER 7, 1994
AND ENDING: JANUARY 7, 1995

FIRST, MATERIAL DISCLOSED HEREIN IS CONFIDENTIAL AND SUBJECT OF PENDING PATENT APPLICATIONS. PLEASE DO NOT RELEASE ANY OF THE INCLUDED INFORMATION.

NOW, THIS HAS BEEN AN EVENTFUL QUARTER.

PATENT MATTERS

I RECEIVED AN OFFICE ACTION ON THE PENDING PATENT APPLICATION. THE EXAMINER FOUND SOME RELEVANT ART AND I HAVE SPENT A GOOD BIT OF TIME PREPARING A CONTINUATION-IN-PART PATENT APPLICATION IN RESPONSE THERETO. APPARENTLY AVAILABLE RIGHTS WILL NOT BE WHAT I'D EXPECTED, BUT STILL MIGHT BE VALUABLE.

THE EXAMINER CITED ONE PATENT, TO HONMA ET AL, NO. 5,177,568, IN THE OFFICE ACTION WHICH DESCRIBES A SCHOTTKY BARRIER MOSFET STRUCTURE IN WHICH THE DRAIN JUNCTION IS ESSENTIALLY OHMIC. AS I READ THAT PATENT IT SEEMS THAT THE DEVICES OPERATE IN AN ACCUMULATED CHANNEL REGION MODE. MENTION OF SCHOTTKY BARRIER CMOS IS PRESENT IN SAID PATENT.

AS I WAS IN WASHINGTON ON OTHER MATTERS (IE. A MEDICALLY ORIENTED PATENT APPLICATION EFFORT FOR A CLIENT), SHORTLY AFTER RECEIVING THE OFFICE ACTION ON MY FIRST SUBMITTED APPLICATION IN THE PRESENT RESEARCH AREA, I STOPPED IN AND SAW THE EXAMINER ON THE CASE, (EXAMINER LOKE) AT THE PATENT OFFICE. I ASKED HIM IF HE

KNEW OF ANY OTHER ART BESIDES THAT HE HAD CITED IN HIS OFFICE ACTION. HE TOLD ME HE HAD FOUND AN ADDITIONAL PATENT AND PROVIDED ME A COPY THEREOF, SAID PATENT BEING TO KOENEKE ET AL. NO. 4,485,550. THIS PATENT IS A BIT DAMAGING TO THE BROAD SCOPE OF MY EFFORTS. IT DESCRIBES SCHOTTKY BARRIER MOS AND CMOS. THE FOCUS IS ON THE USE OF AN ION IMPLANTATION AT THE SCHOTTKY BARRIER JUNCTIONS TO REDUCE LEAKAGE CURRENTS. I DO NOT FIND MENTION OF THE USE OF CHROMIUM WITH SILICON, BUT THE GENERAL CONCEPT OF CMOS FROM SCHOTTKY BARRIER MOSFETS IS PRESENT.

WHILE AT THE PATENT OFFICE I DID SOME SEARCHING MYSELF AND FOUND AN ADDITIONAL PATENT TO LEPSELTER, NO. 4,300,152. THIS PATENT DESCRIBES THE USE OF PLATINUM TO FORM SCHOTTKY BARRIER MOSFETS AND MENTIONS A CMOS STRUCTURE CONFIGURED THEREFROM. IT IS MENTIONED THAT THE USE OF AT LEAST ONE SCHOTTKY BARRIER MOSFET IN A CMOS CONFIGURATION PROVIDES IMMUNITY TO PARASITIC SILICON CONTROLLED RECTIFIER-LIKE "LATCH-UP" IN RESULTING CIRCUITS. THIS CAN OCCUR IN DIFFUSED JUNCTION CMOS SYSTEMS.

WHILE A SET-BACK, I STUDIED THE PROBLEMS IDENTIFIED BY THE NEWLY DISCOVERED ART. IT SEEMS THAT TWO PROBLEMS IDENTIFIED ARE THE RELATIVELY HIGHER LEAKAGE CURRENTS ASSOCIATED WITH SCHOTTKY BARRIER JUNCTIONS AS COMPARED TO DIFFUSED P-N JUNCTIONS AND THE "GAP" WHICH TYPICALLY EXISTS BETWEEN A SOURCE OR DRAIN AND A CHANNEL REGION IN A SCHOTTKY BARRIER MOSFET. SAID "GAP" IMPOSES HIGH RESISTANCE DRAIN TO SOURCE CURRENT FLOW LIMITING REGIONS BETWEEN SOURCE AND DRAIN JUNCTIONS AND A CHANNEL REGION.

IN RESPONSE I CONCEIVED A SIMPLY WAY TO OVERCOME THE PROBLEMS INVOLVING THE USE OF AN ISOTROPIC SILICON ETCH AFTER THE GROWING OF A GATE OXIDE ATOP A SILICON SUBSTRATE. SAID ISOTROPIC SILICON ETCH UNDERCUTS THE OXIDE. DEPOSITION OF CHROMIUM, OR OTHER SILICIDE FORMING METAL CAN THEN BE CAUSED TO PROVIDE SAID METAL UNDER SAID UNDERCUT OXIDE, WHICH ELIMINATES ANY HIGH RESISTANCE GAPS BETWEEN SOURCE AND DRAIN JUNCTIONS. IN ADDITION, THE RELATIVELY HIGH LEAKAGE CURRENTS OF SCHOTTKY BARRIER JUNCTIONS CAN BE MINIMIZED BY REDUCING THE CROSS SECTIONAL AREA OF SAID JUNCTIONS. NOW,THE ONLY LOCATION SAID SCHOTTKY BARRIER JUNCTIONS ARE REQUIRED ARE AT THE ENDS OF A CHANNEL REGION. I CONCEIVED THE USE OF AN ADDITIONAL OXIDE GROWTH AN ETCH STEP TO PROVIDE A MOSFET STRUCTURE IN WHICH THE SCHOTTKY BARRIER JUNCTIONS ARE PRESENT ONLY AT THE ENDS OF A CHANNEL REGION, AS WELL AS UNDER THE GATE OXIDE. MY APPROACH IS, I BELIEVE, SUPERIOR TO THE ION IMPLANTATION APPROACH OF KOENEKE ET AL.

I AM INCLUDING A COPY OF A RELEVANT PORTION, (EG. THE DETAILED DESCRIPTION AND DRAWINGS), OF A NEWLY SUBMITTED PATENT APPLICATION WHICH I PREPARED TO FURTHER DISCLOSE WHAT IS STATED ABOVE, IN ADDITION TO OTHER PRESENT INVENTION MATTERS. (SEE ATTACHMENT 1 HERETO).

ADDITIONAL DEVICE FABRICATION EFFORTS

AS WELL, IN VIEW OF THE RESULTS OBTAINED TO DATE, I CONCEIVED A

SINGLE DEVICE EQUIVALENT TO CMOS. WE KNOW CHROMIUM ANNEALED TO EITHER N OR P-TYPE SILICON FORMS A RECTIFYING JUNCTION THEREWITH. THIS IS THE CASE WHETHER THE SILICON IS METALURGICALLY DOPED OR SAID DOPING IS INDUCED BY APPLICATION OF A VOLTAGE TO A GATE. (SEE ATTACHMENT 2 FIG. 7 FOR AN OPTICAL PHOTOGRAPH OF THE FABRICATED DEVICE).

NOW, A MOSFET DEVICE SYSTEM COMPRISES A CHANNEL REGION WITH A SCHOTTKY BARRIER JUNCTION ON EACH END THEREOF. IF ONE APPLIES A CONSTANT POLARITY POTENTIAL ACROSS THE TWO JUNCTIONS, ONE SAID JUNCTION IS REVERSE AND THE OTHER FORWARD BIASED. IF THE CHANNEL REGION DOPING IS INVERTED BY APPLICATION OF A GATE VOLTAGE, THE SILICON TYPE IS EFFECTIVELY CHANGED AND THIS CAUSES THE REVERSE BIASED JUNCTION TO FORWARD BIAS AND THE FORWARD BIASED JUNCTION TO BECOMES REVERSE BIASED. NOW----IF WE CAN MONITOR THE VOLTAGE IN THE CHANNEL REGION VIA A CHANNEL ACCESSING REGION WE SHOULD SEE IT FOLLOW THE POTENTIAL APPLIED TO THE FORWARD BIASED JUNCTION. TO INVESTIGATE THIS POSSIBILITY WE FABRICATED SOME CRUDE DEVICES AND SAW SOME ENCOURAGING RESULTS WHEN THE RESULTING DEVICES WERE TESTED. WE DO SEE A GATE CONTROLLED DRAIN TO SOURCE APPLIED VOLTAGE PRESENT AT THE CHANNEL ACCESSING REGION WHEN THE GATE VOLTAGE IS APPLIED AND KEPT BELOW APPROXIMATELY 10 VOLTS. (SEE FIG. 8 IN ATTACHMENT 2 FOR GRAPHICALLY PRESENTED RESULTS). WITHOUT APPLIED GATE VOLTAGE NO CHANNEL ACCESS REGION VOLTAGE IS PRESENT. ABOVE ABOUT 10 VOLTS ON THE GATE, THE GATE VOLTAGE DOMINATES THE CHANNEL ACCESS MIDPOINT VOLTAGE. tHAT IS, REEUCING DRAIN TO SOURCE VOLTS TO ZERO (0) NO LONGER CAUSES LOSS OF MID POINT VOLTS. iF WE CAN OVERCOME THE BUGS, WHAT MIGHT BE POSSIBLE IS A SINGLE DEVICE EQUIVALENT TO MULTIPLE DEVICE CMOS, WHICH SINGLE DEVICE IS FORMED ON SINGLE DOPING TYPE SILICON, OR EVEN GALLIUM ARSENIDE. THE FABRICATION EASE IS EVIDENT. THIS DESERVES MORE INVESTIGATION AND WE HAVE SEVERAL ADDITIONAL GRANT APPLICATIONS IN THE WORKS, INCLUDING ANOTHER APPLICATION TO THE DOE ENERGY RELATED INVENTIONS GROUP.

THE PORTION OF THE PATENT APPLICATION INCLUDED HEREIN BETTER DESCRIBES THE SINGLE DEVICE EQUIVALENT TO CMOS DEVICES. NOTE THAT BOTH INVERTING AND NONINVERTING DEVICES ARE POSSIBLE. DIFFUSED JUNCTION CMOS PROVIDES ONLY INVERTING DEVICES. THIS COULD BE A SIGNIFICANT POINT.

AS WELL THE INCLUDED PORTION OF THE NEWLY SUBMITTED CONTINUATION-IN-PART PATENT APPLICATION PROVIDES INSIGHT TO THE SCOPE OF RIGHTS I AM ATTEMPTING TO ACQUIRE.

I HAVE PROVIDED A COPY OF THE FULL CONTINUATION-IN-PART PATENT APPLICATION TO THOMAS G. ANDERSON, DOE ASSISTANT CHIEF LEGAL COUNSEL AT THE 9800 SOUTH CASS AVENUE, ARGONNE, IL 60439 LOCATION.

I ALSO WANT TO MENTION THAT OVER THE CHRISTMAS HOLIDAY SEASON, (BETWEEN DECEMBER 16 AND 21, 1994), I WAS IN TORONTO. WHILE THERE I VISITED WITH PROFESSOR'S SALAMA AND COBBOLD AT TORONTO UNIVERSITY REGARDING MY RESEARCH. NEITHER HAD HEARD OF ANYONE

ELSE EVER ATTEMPTING TO FORM THE SINGLE DEVICE EQUIVALENT TO CMOS WHICH I'VE CONCEIVED AND FOR WHICH I'VE PURSUED FABRICATION AND PATENT RIGHTS. AS A RESULT I DO BELIEVE THAT SUCH IS NEW, NOVEL, NONOBVIOUS AND USEFUL, THEREFORE PATENTABLE AND POSSIBLY VERY VALUABLE. WE WILL SEE WHAT THE PATENT EXAMINER THINKS.

I INTEND TO ABANDON THE FIRST PATENT APPLICATION AS IT WAS, FROM THE OUTSET, VERY LOOSE. I SUBMITTED IT FOR THE PURPOSE OF OBTAINING A PATENT SEARCH. IT HAS SERVED ITS PURPOSE. (IT WOULD HAVE COST ME AS MUCH TO HAVE A PATENT SEARCH PERFORMED AS IT DID TO HAVE IT DONE BY A PATENT EXAMINER THE WAY I APPROACHED IT).

FINALLY IT IS NOTED THAT CONTINUED DEVICE FABRICATION AND TESTING EFFORTS HAVE SHOWN THAT WHILE WE CAN SHOW FEASIBILITY, WE HAVE A DIFFICULT TIME WITH REPEATABLITY AND CONSISTENCY. (SEE ATTACHMENT 2 FIGS. 1 - 7 FOR TYPICAL MOSFET CURVES NOW ROUTINELY ACHIEVED). WE ARE GOING TO ATTEMPT TO TIGHTEN-UP THE PROCEDURE DESCRIBED IN THE LAST QUARTERLY REPORT IN THE NEXT QUARTER AND SEE IF WE CAN ARRIVE AT MORE DEFINITIVE RESULTS. HOWEVER, IT IS BEGINNING TO APPEAR THAT AN ENTIRE NEW SET OF MASKS MIGHT BE NECESSARY, WHICH PROVIDE OFFSET ELECTRICAL CONTACT PADS ETC., TO PROVIDE DEVICES WHICH DEMONSTRATE CONSISTENT AND REPEATABLE RESULTS. THE MASKS I'VE BEEN USING PROVIDE FOR ELECTRICAL PROBING AT THE DRAIN, SOURCE, AND CHANNEL ACCESSING MIDPOINT REGION DIRECTLY AND IT HAS BEEN FOUND THAT PROBE PLACEMENT AND PRESSURE ETC. INFLUENCE THE ELECTRICAL CHARACTERISTICS ACHIEVED. ADDITIONAL GRANT FUNDS WILL BE, IT APPEARS, REQUIRED TO PURSUE BETTER REPEATABILITY AND CONSISTENCY IN ACHIEVED RESULTS. WE HAVE AGAIN APPLIED TO THE DOE ENERGY RELATED INVENTIONS PROGRAM FOR A SECOND GRANT, AS WELL AS TO NSF AND THE AIR FORCE UNDER SBIR PROGRAMS. IT IS MY HOPE THAT ADDITIONAL FUNDS WILL BE AVAILABLE WHEN THE PRESENT GRANT EXPIRES.

SINCERELY,

JAMES D. WELCH
JW/HS

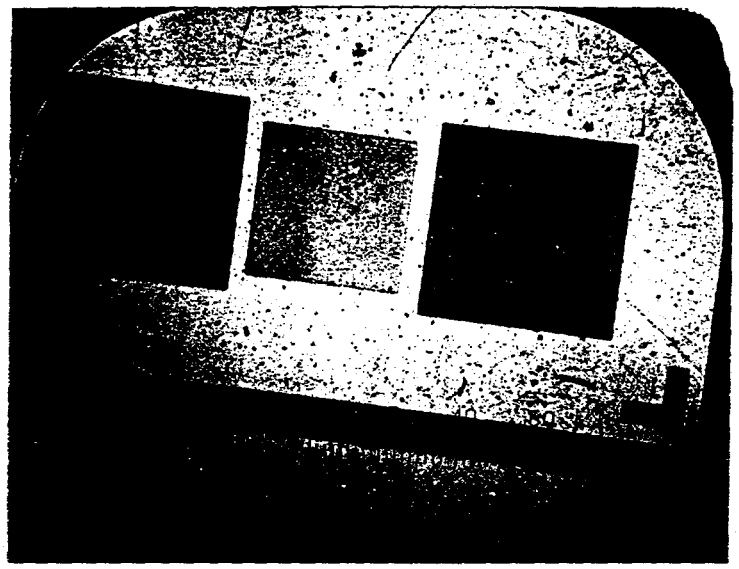
ENC. DETAILED DESCRIPTION AND DRAWINGS FROM CONTINUATION-IN-PART PATENT APPLICATION I RECENTLY PREPARED AND SUBMITTED TO THE PATENT OFFICE FOR EXAMINATION. PLEASE KEEP ALL MATERIALS CONFIDENTIAL!

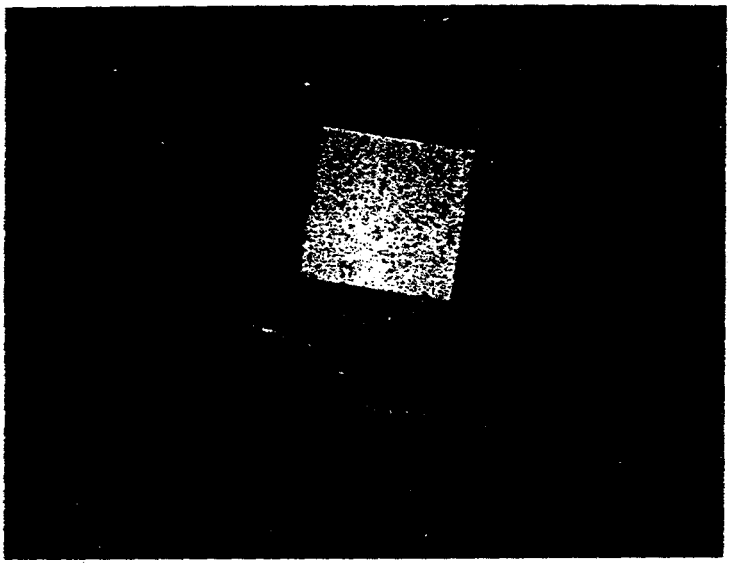
COPIES OF ADDITIONAL N-CHANNEL AND P-CHANNEL MOSFET CURVES, AND AN OPTICAL PHOTOGRAPH OF THE FABRICATED SINGLE DEVICE EQUIVALENT TO CMOS.

ALSO, I RECEIVED A "B" IN QUANTUM ELECTRONICS LAST SEMESTER.

Optical photo

NONINVERTING
Single Device Equiv To CMOS





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C. Identification and Significance of the Problem

Silicon based CMOS circuits command a substantial share of the world market for semiconductor device sales. The United States leads the world in microprocessor circuit manufacturing and sales, where the circuits are based on CMOS technology. Therefore, advances in CMOS devices and manufacturing technology will directly impact a large portion of the Unites States semiconductor industry, leading to increased competitiveness in the world market. Towards this end we are proposing to develop a new MOS technology that is based on Schottky barrier junctions, rather than p-n junctions, at the source and drain. The Principal Investigator, as described in US patent 4,696,093[1] has developed a method for the formation of Schottky barrier diodes on p and n-type silicon by depositing chromium on the silicon and annealing in an inert atmosphere or vacuum to form $CrSi_2$. Also described in the patent is a method for fabricating MOSFETs based on the Schottky barriers formed by the $CrSi_2$ in place of the p-n junctions. It should be pointed out that Lepselter and Sze[2] describe a similar device. However, their device is based on platinum silicide Schottky barriers and will only operate as an pMOS device. We are currently supported by DOE grant #DE-FG47-93R701414 (see Section L. Current and Pending Support) to study the fabrication of $CrSi_2$ devices. We have done so, with the resulting I_D vs V_D, V_G curves as seen in Figure 1. Clearly, these devices exhibit transistor action similar to that observed in MOSFETs. That is for a p-type substrate, a positive gate voltage is required to turn the device on, while for an n-type substrate a negative gate voltage is required to turn the device on. However, for the nMOS device I_D only flows when V_D is negative and for a pMOS device I_D flows only when V_D is positive. The polarities and current directions for V_{DS} are such that the devices operate in the "inverted" mode with respect to standard FETs, but do not operate in the standard forward mode. This result is not clearly understood, but it must be a direct result of the Schottky barrier junctions. A brief examination of Figure 1 shows that when an inversion region exists under the gate, one of the junctions must be reversed biased in order for current to flow since $CrSi_2$ forms barriers with respect to both n and p-type silicon. Based on the polarities of V_{DS} it appears that the drain junction is in reverse bias during operation. Further, it should be pointed out that devices fabricated on p and n-type substrates require opposite voltages to achieve transistor action. We believe that this indicates the devices are operating in a mode similar to standard MOSFETs.

Based on these results, we are proposing to place a voltage sensor at the center of the gate, as seen in Figure 2. We believe that for a fixed drain to source voltage, gate voltage induced changes in the channel carrier type can cause switching of which Schottky barrier junction is forward biased and which is reversed biased. Assuming the source to be ground, the gate center tap voltage with respect to the source should switch as the source to channel junction changes from one bias state to the other as the gate voltage is changed.

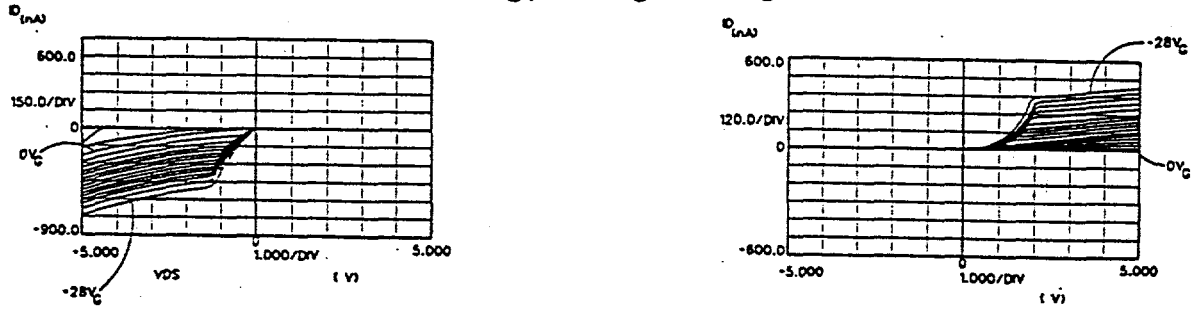


Figure 1. ID vs VDS as a function of VG, a) n-channel, b) p-channel

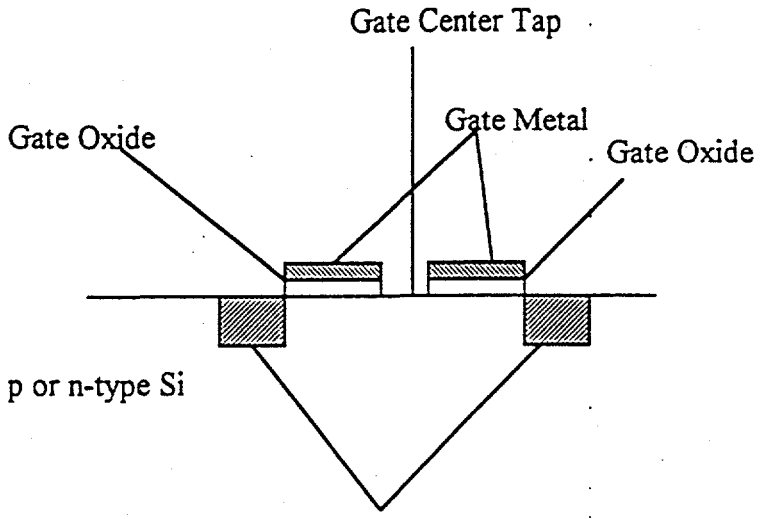


Figure 2. Schematic diagram of single device equivalent to a CMOS. The structure is a Schottky barrier based MOSFET with a gate center tap.

We have fabricated these devices on p-type, n-type, and nominally intrinsic, high resistivity silicon (ρ>10,000 Ω-cm). The best results were achieved with the intrinsic silicon, where Figure 3 is graph of the center tap gate voltage vs gate voltage when the source is grounded, for a fixed drain to source voltage.

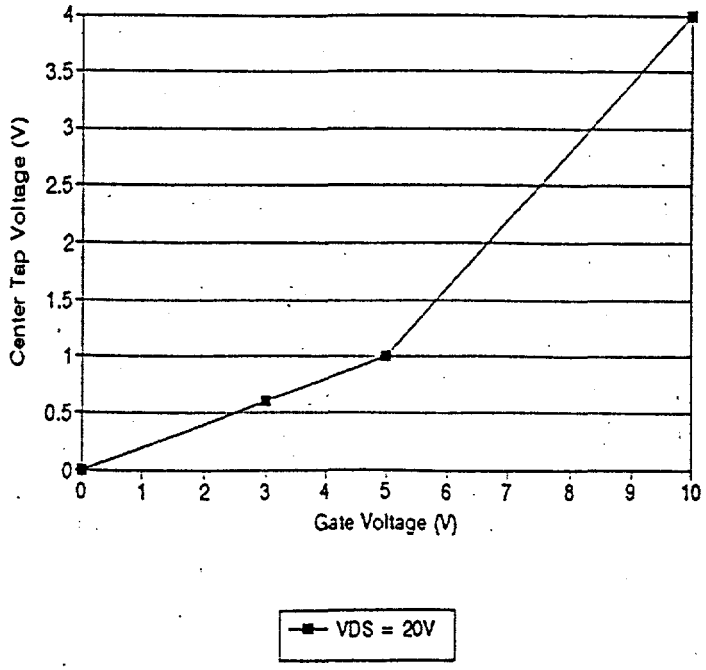
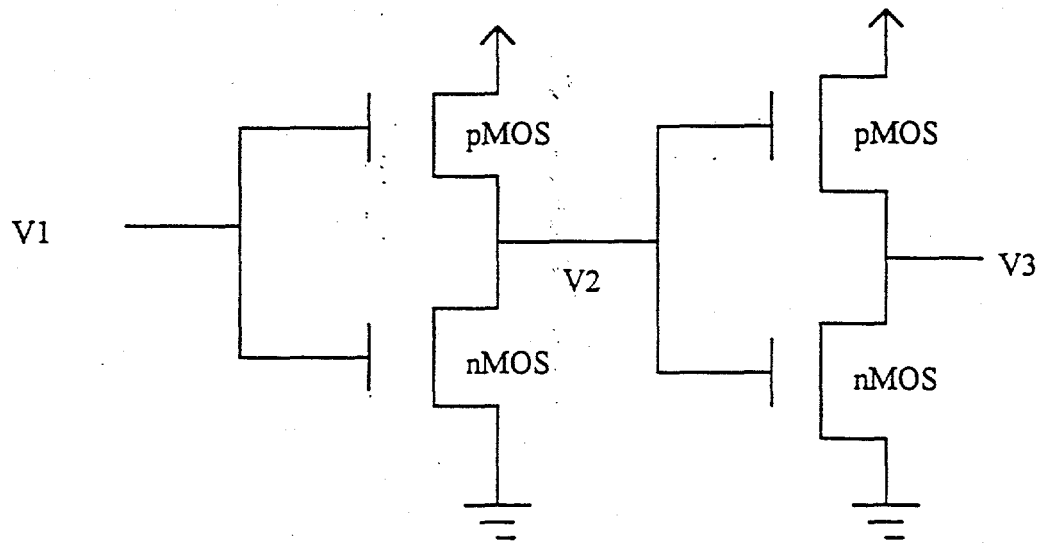
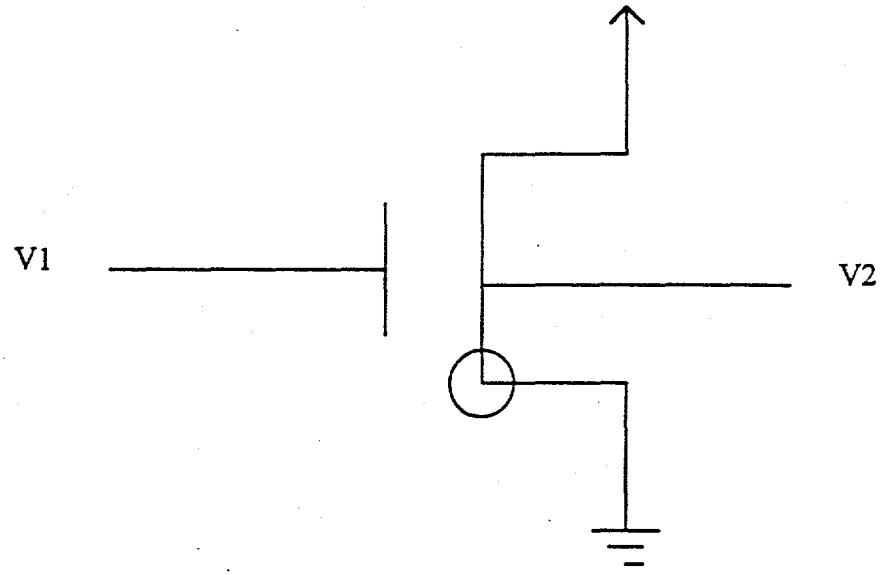


Figure 3. Center tap voltage vs Gate voltage for a fixed drain to source voltage.

Electrically, this device is equivalent to a non-inverting CMOS circuit with 4 MOSFETs. This is illustrated in Figure 4.



(a)



(b)

Figure 4. a) Standard 4 device CMOS non-inverting circuit. b) Proposed single device equivalent. The Schottky barrier that is circled is switched to reverse bias by the applied gate voltage at V1. This causes V2 to switch to a positive value.

An inverter can be made by placing a Schottky barrier at the center and ohmic contacts at the source and drain. However, the source and drain semiconductor regions be surrounded, and separated, by a continuous silicide region, where the silicide region should extend into the silicon to a depth greater than a typical MOSFET channel region depth. This is necessary because in the off state the device is essentially a short and this guard ring structure will limit current flow within

the device, and between adjacent devices. A possible structure may consist of an epilayer on high resistivity silicon where the guard ring silicide extends through the epilayer to the intrinsic layer. This is illustrated in Figure 5.

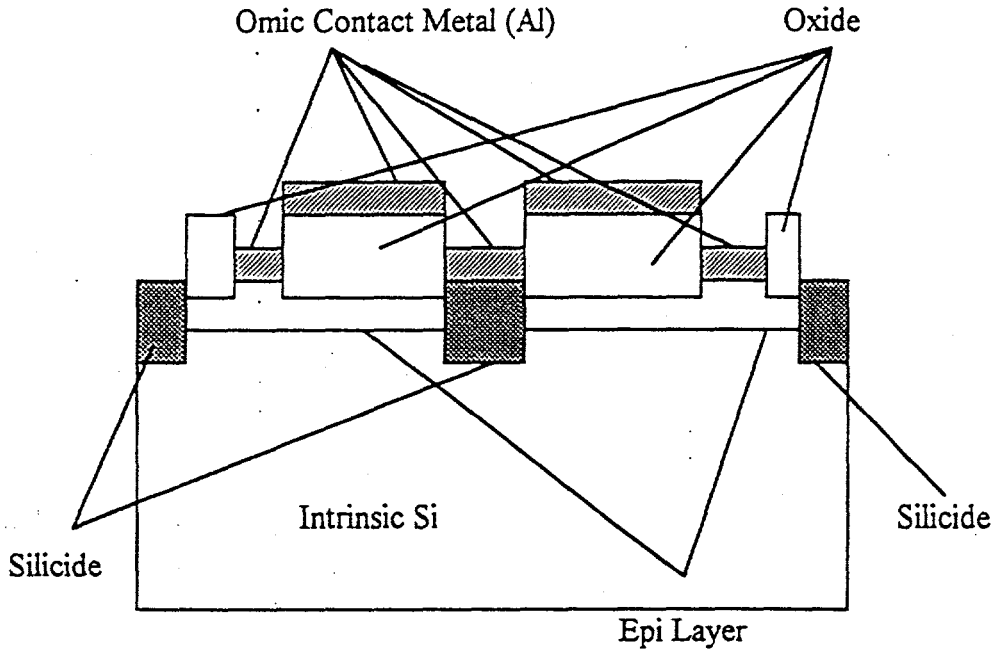


Figure 5. Schematic cross section on inverting structure.

Based on the structure in Figure 5, application of a voltage between the drain and source will cause one of the junctions, (ie., source to center tap silicide region or drain to center tap silicide region) to be forward biased and the other junction to be reverse biased. The device operational theory is that the voltage at the center tap silicide region should follow the forward biased junction. Application of a channel region inverting gate voltage will reverse the locations of the forward and reverse biased junctions. If initially, the drain to silicide region junction is forward biased, then the silicide region will be at essentially the voltage applied to the drain. Application of a voltage of the same polarity as applied to the drain will then cause the drain to silicide region junction to become reverse biased, by affecting an inversion of the semiconductor in the channel region beneath the gate oxide, and the source to center tap silicide region junction to become forward biased. As an example say the semiconductor is p-type and a positive voltage is applied to the drain with respect to the source. The drain to silicide region junction will be forward biased and the silicide region to source junction will be reverse biased. The applied drain voltage will appear at the silicide region through the forward biased junction. Application of a positive polarity gate voltage , (the same polarity as applied to the drain), will invert the semiconductor between each of the source and drain contacts, to the silicide region , and cause the location of the forward and reverse biased junctions to reverse. Thus an increase in gate voltage will cause the voltage present in the silicide region to decrease, much as occurs in dual device CMOS systems fabricated utilizing p-n junction technology. The dual device inverter is voltage V2 in Figure 5a.

We have not fabricated the inverting structure. Further, due to its increased complexity as compared to the non-inverting structure and the early stage of development of this structure, we will focus our efforts in this program in fully developing the non-inverting structure.

These non-inverting devices require roughly the same number of steps to fabricate than conventional a CMOS pair, resulting in higher yields and throughput, which will reduce fabrication costs. But the key advantage of these devices is the resulting higher packing density that is realized by the replacement of 4 conventional MOSFETs by 1 device to make non-inverting logic and 2 devices by one device when making inverting logic. This increased packing density is realized without a reduction in minimum feature size. Finally, the processes involved in the fabrication of the device requires minimal retooling and virtually no new equipment purchases on the part of semiconductor manufacturers. Thus we feel the single device equivalent to CMOS (referred to as SDCMOS) will be extremely attractive to industry.

Table I illustrates the steps required to fabricate conventional CMOS and the non-inverting SDCMOS devices.

Conventional CMOS Process	SDCMOS Process
Begin with n-type wafer	Begin with intrinsic wafer
1. Thermal Oxidation	1. Isolation a. CVD Nitride Deposition b. Photolithographically define field c. Strip Resist d. Field Oxidation-Nitride Removal
2. Photolithography-define p-well	2. Gate Fabrication a. Gate Oxidation b. Gate Metallization c. Gate Metal Definition via Photolith. and etching. Leave resist on.
3. Dope p-well	3. Source- Drain a. Open holes in gate oxide for source and drain using resist from 5c. b. Strip Resist c. Deposit chromium over entire substrate. d. Anneal to form $CrSi_2$ in source and drain regions. e. Selectively etch unreacted chromium from substrate via wet chemical chromium etch.
4. Isolation a. CVD Nitride Deposition b. Photolithographically define field c. Field Implant d. Strip Resist e. Field Oxidation-Nitride Removal	4. Gate Center Tap a. Photolithographically define center tap. b. Etch through gate metal c. Etch through gate oxide d. Strip Photoresist

5. Gate Fabrication a. Gate Oxidation b. Gate Metallization c. Gate Metal Definition via Photolith. and etching. d. Strip Resist	5. Contact formation a. Glass Deposition b. Photolithographically define source, drain, gate, and gate center tap regions. c. Metal Deposition d. Photographically define contacts e. Metal Etch
6. Source-Drain a. Mask p-well via Photolith. b. Ion Implant p-dopant (PMOS source and drain) c. PMOS source/drain anneal-diffusion d. Remove resist e. Mask PMOS area f. Ion Implant n-dopant (nMOS source and drain) g. nMOS source/drain anneal diffusion h. Strip Resist	6. Interconnects and Passivation
7. Contact formation a. Glass Deposition b. Photolithographically define source, drain, gate, and gate center tap regions. c. Metal Deposition d. Photographically define contacts e. Metal Etch	
8. Interconnects and Passivation	
Total Number of Steps (1-7) = 25	Total Number of Steps (1-5) = 21

A few comments are in order concerning the process. The field implant and field oxide in the conventional process serve to increase the threshold voltage of the parasitic FET that results from adjacent devices and metallization layers. In the SDCMOS process, adjacent devices and hence parasitic FETs exist as well, however, the Schottky barrier source and drain regions will form ohmic contacts to heavily doped material via the tunneling mechanism. Therefore, if conventional isolation techniques were employed in the SDCMOS process, this could cause a short between adjacent devices, rather than serve to isolate them. Hence the SDCMOS process relies only on the thick field oxide for isolation.

The elimination of 3 ion implantation steps should enhance the throughput since implantation has a limited throughput when compared to other steps. Further, implantation requires substantial energy, and cooling water for the magnets, and it is not an energy efficient process, thus cost savings in eliminating these steps will be realized. The lithographic step that is eliminated is a high yield step since all it does is mask devices as a whole. The anneal is also a high yield step, but is energy intensive since it is a thermal anneal. These steps are replaced by a metal deposition, thermal anneal and gate center tap process.

The net number of steps required for SDCMOS fabrication is less than that required for conventional CMOS which can result in an increased yield. As a simple example of the effect on yield of eliminating steps from the overall process, assume each step has a 0.95 yield. In the conventional process requiring 25 steps the overall yield is $(0.95)^{25} = 0.277$, while the SDCMOS process requires 21 steps resulting in an overall yield $(0.95)^{21} = 0.340$. Therefore the SDCMOS process increases yield by 22.7% without requiring a yield increase in the individual process steps. Furthermore, the lower the yield per step, the greater affect the SDCMOS process has in increasing overall yield. Again as previously discussed, the key advantage of the SDCMOS devices in greatly increased packing density.

In view of the potential advantages of SDCMOS we are proposing a program aimed at developing the these devices. Phase I of this program will consist of extending our preliminary results for the non-inverting structure by improving our processing and employing metals other than chromium for contact formation. Further, we will investigate the device isolation between like devices, and perform simple modeling of the device itself in order to explain its operating characteristics.

D. Technical Objectives

The Welch Research major technical objectives for Phase I are as follows:

I. Fabricate non-inverting devices employing molybdenum, and platinum as well as chromium as the Schottky barrier materials.

II. Investigate the isolation between like devices provided by the field oxide, and compare to conventional devices.

III. Characterize the Schottky barrier junctions and begin to develop device model.

While the proposed research program can be broken down into separate objectives, each one must be met to at least some extent in order to proceed to Phases II and III. Clearly, the first objective is key in that we must advanced processing to improve device performance and we should determine the utility of other metals in these structures in order to optimize device performance. The second objective directly impacts the minimum spacing allowed between devices, which plays a major role in circuit density. If we can achieve adequate isolation with just field oxide, devices can be spaced close together. If not, this may limit the packing density. The final objective lays the groundwork for device modeling, and hence design. This is critical to circuit design using these devices.

Achievement of these objectives paves the way for the fabrication of the more complex inverting SDCMOS devices in Phase II, and ultimately SDCMOS circuits in Phase II as well. The performance and density of these circuits can be directly compared to conventional circuits allowing us to determine if the proposed devices are a viable alternative to existing ones. If so, Phase III could center on bringing them to market independently, or by teaming with an outside concern capable of mass production of integrated circuits.

E. Phase I Work Plan

The main goals of the Phase I program are to fabricate non-inverting SDCMOS devices, identify the best metal from chromium, molybdenum, and platinum for Schottky barrier contact formation, determine the isolation between devices provided by a field oxide, and to develop a first model of the device.

Towards this end we have formulated the following work plan.

1. Device Fabrication

Based on the results obtained from our previous work, as described in Section C, we will fabricate inverting and non-inverting SDCMOS devices. This establishes the foundation for SDCMOS based circuits which will be developed in Phase II. The process and device cross sections are as follows:

Non-Inverting Device

1. Isolation a. Grow 1 micron wet oxide over entire wafer surface. Note: we do have not a CVD nitride capability b. Photolithographically define field c. Etch field oxide to define device regions d. Strip Resist
2. Gate Fabrication a. Gate Oxidation, dry oxide, 100-300nm thick b. Gate Metallization, sputtered Aluminum c. Gate Metal Definition via Photolith. and etching. Leave Resist on.
3. Source- Drain a. Open holes in gate oxide for source and drain using resist from 2c. b. Sputter clean substrate and sputter deposit metal over entire substrate. Note: metal will also be deposited over the field regions, and the photoresist on the gate metal. c. Lift-off resist from step 2. d. Thermally process to form silicide in source and drain regions. e. Selectively wet etch remaining metal.
4. Gate Center Tap a. Photolithographically define center tap. b. Etch through gate metal c. Strip Resist d. Sputter deposit SiO_2 dielectric layer e. Photolithographically define center tap connection, source and drain contacts

f. Etch through dielectric layer and gate oxide
g. Deposit Ohmic contact metal
h. Photolithographically define contact pattern
i. Etch Metal
j. Remove resist.
k. Sinter Ohmic contact metal

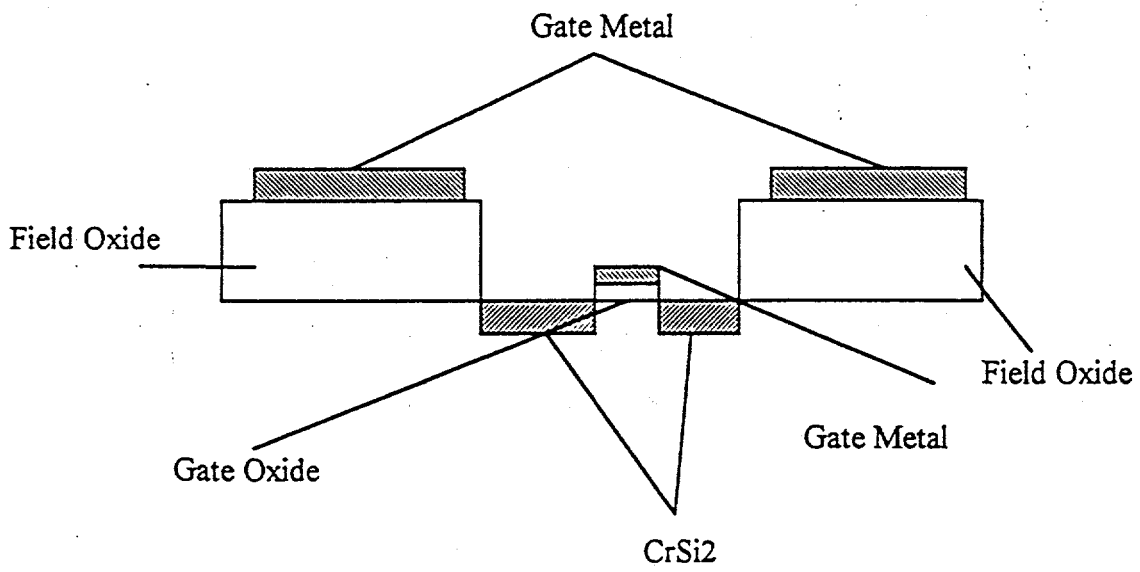


Figure 6. Structure after Step 3e.

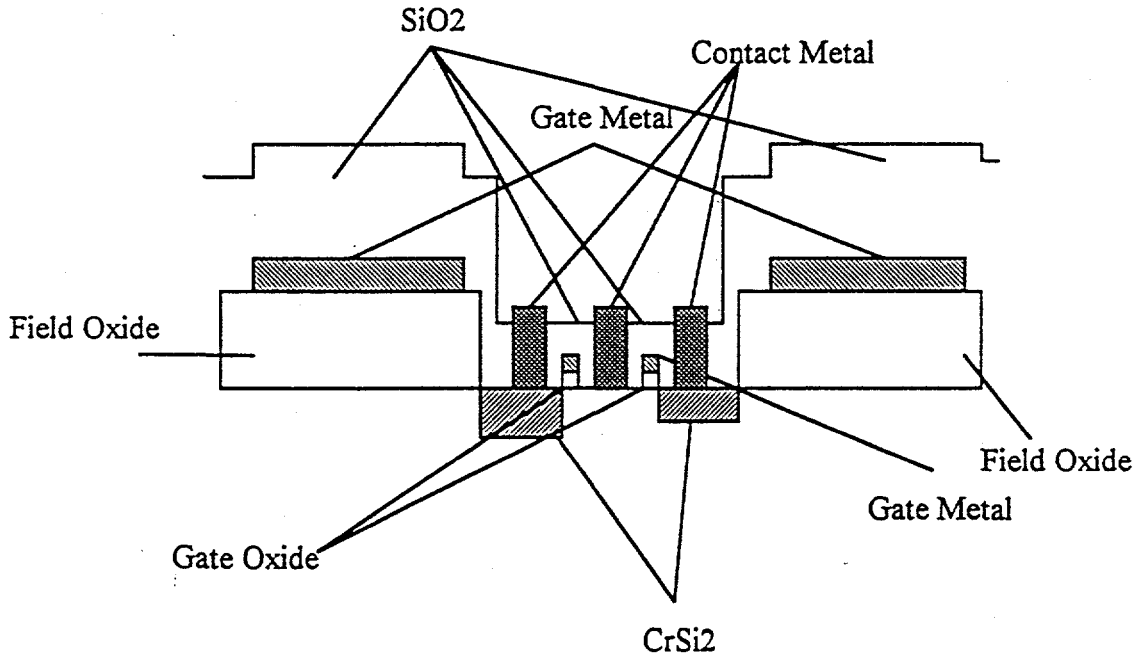


Figure 7. Structure after Step 4j.

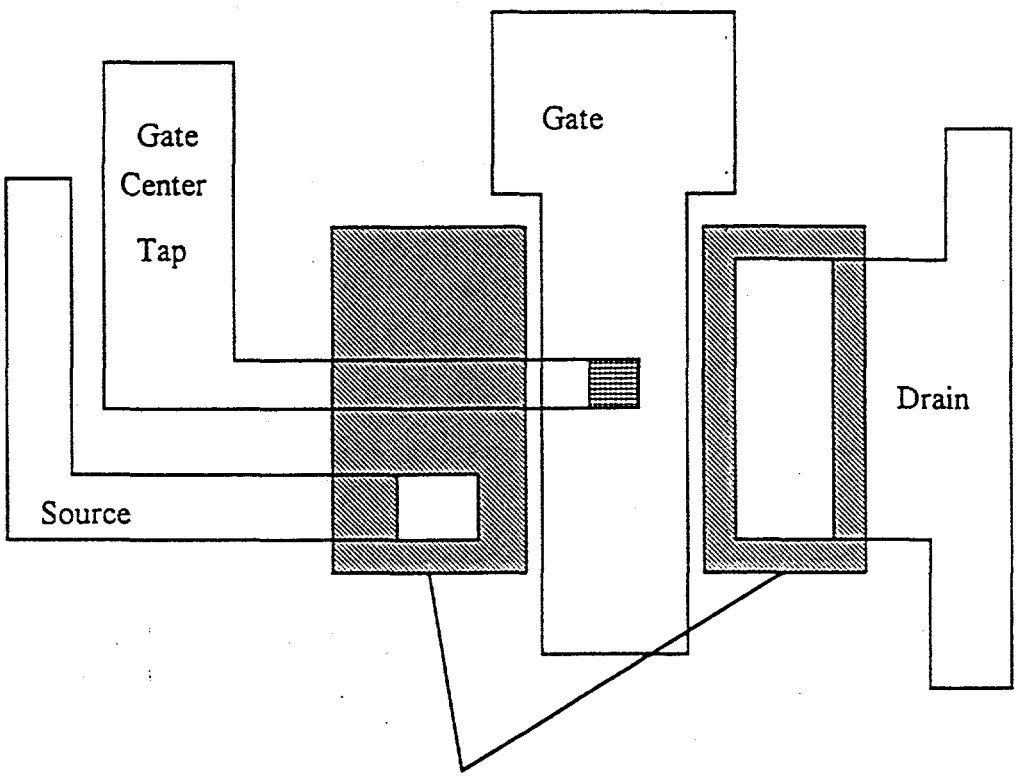


Figure 8 Top view of completed device. Silicon dioxide is used as a dielectric material to isolate the gate center tap from the gate and source metallization.

It should be noted that in the Figures chromium is identified as the silicide forming metal, but as stated previously we will employ molybdenum and platinum as well. The process identified above employs sputter cleaning of the substrate before silicide forming metal is deposited. This will enhance the barrier formation reproducibility over our current process. Also, the silicide formation will be performed in a furnace with a flowing forming gas atmosphere. Our current work has shown that sintering at 450 C for 30 minutes yields good $CrSi_2$ formation.[1] However, the physics of the reaction between chromium and silicon require that thermal processing after the silicide formation be kept to a minimum.[3] Therefore sintering of the aluminum ohmic contact to the gate center tap will be performed at 400 C. It should be pointed out that virtually no current will flow through contact, it is just a voltage sensor, therefore the quality of this contact is not as critical as it would be otherwise.

Devices employing chromium will be fabricated on intrinsic, p-type and n-type silicon. As stated in Section C we have achieved the best results with intrinsic silicon, but this may be a result of poor Schottky barrier formation on the doped material due to oxide at the metal/silicon interface. This will be eliminated by in-situ sputter cleaning of the substrate, a capability we have recently acquired.

Molybdenum based devices will be formed on each type of silicon as well, by sintering at 550 C .[4] This process temperature yields only $MoSi_2$. It should be mentioned that $MoSi_2$ formation is a strong function of the cleanliness of the Mo/Si interface, so sputter cleaning is essential. We should be able to sinter the aluminum contact at 500 C without disturbing the $MoSi_2$.

Platinum silicide (PtSi) will be formed by sintering at 650 C. It should be pointed out that PtSi is the desired phase, as opposed to Pt_2Si. However, Pt_2Si forms first and then the conversion to PtSi occurs.[2,5] The process will be adjusted to yield this material. Due to the barrier heights of PtSi with respect to n and p-type silicon, we will only explore the n-type substrate.

Device testing will consist of measuring their I-V characteristics employing the existing voltage sources, and an electrometer. The main goals of this work are to determine the drain to source leakage current and the threshold voltage as a function of Schottky barrier metal, and silicon doping. We hope to be able to identify a material system that provides reproducible results and a low leakage current which can serve as the basis for inverting devices and circuits.

Finally, the masks for this work will be fabricated by Dr. Salama at the University of Toronto, and purchased as part of the materials and supplies (see the Budget for costs).

2. Device Isolation

The fabrication procedure is designed to include parasitic Schottky barrier FETs. The characteristics of parasitic devices will be measured using the existing Hewlett Packard semiconductor Analyzer. It is anticipated that the major difference in threshold voltage will be directly related to the oxide thickness ratio of the field to the gate oxide. In standard junction devices the region under the field is heavily doped to also increase the V_t. The breakdown voltage of the diode formed between the source or drain region and this implanted region is still quite high, so leakage current between adjacent devices will be minimal. However, for the Schottky barrier based device proposed here, increasing the doping under the field region can lower the barrier, and establish conditions for tunneling which leads effectively to an ohmic contact between the metal and semiconductor, resulting in a short. We will have some data on FET properties as a function of substrate doping from our current work (see Section L. Current and Pending Support) and this will be employed here to determine the trade-offs between isolation by field oxide alone and altering the doping under the field oxide, which introduces additional steps, to achieve adequate isolation.

The work outlined in this Section lays the foundation for a major portion of Phase II; the fabrication of inverting devices and circuits based on the SDCMOS devices.

3. Junction Characterization

Development of a viable device model will play a key role in circuit design with the Schottky barrier devices. The first stage in developing a viable model is the characterization of the Schottky barrier junctions which control the device characteristics. A reasonable amount of information is already available concerning the PtSi junction. This will be employed to explain the behavior of devices based on this contact. Some information is available on the $MoSi_2$ and $CrSi_2$ junctions, but this will be supplemented by additional work. Specifically we will fabricate simple Schottky diodes from these materials and measure their V-I characteristics. The turn-on voltage, reverse breakdown voltage and leakage currents should be related to the characteristics of the SDCMOS devices. This will lay the groundwork for a true device model which will developed in Phase II. This a an important Phase II objective since commercialization virtually requires a device model to enable accurate circuit design.

4. Schedule of Major Events

Month	1	2	3	4	5	6
Task						
Mask Design	xxx					
Device Fab. & Analysis	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxx					
Junction Characterization	xxxxxxxxxxxxxxxxxxxxxxxxxxxx					
Final Report						xxxxxxxxxx

5. References

1. US patent 4,696,093, issued to James Welch 1987.

2. M.P. Lepselter, and S.M. Sze, Proc. of the IEEE, 1400, august 1968.

3. R.W. Bower, and J.W. Mayer, Appl. Phys. Lett., **20**, 359 (1972).

4. A. Guivarch, et. al., Martinez, J. Appl. Phys, **49**, 233 (1978).

5. S.P. Murarka, Silicides for VLSI Applications (Academic Press, New York, 1983).

F. Related Work

The Principal investigator is currently supported by DOE Grant #DE-FG47-93R701414 "Novel Procedure for the Fabrication of MOSFETs". The assigned monitor is Mr. Fred Hart. The DOE project is focused on the initial fabrication of working $CrSi_2$ based FETs through the thin film reaction of chromium with silicon on separate p and n-type substrates. As seen in Figures 1 and 2, the initial demonstration this has been successfully completed. Currently, the effect of doping level on device operation is being investigated.

G. Relationship with Future Work

1. Relationship to Phase II

The Phase I program seeks to fully investigate a new type of device. This new device is essentially a single device equivalent to a 4 device MOS non-inverting logic circuit. It is based on a novel MOS structure than employs Schottky barriers at the source and drain. In concert with this work will be adequate junction characterization to permit the development of a first order device model in Phase II. The successful completion of these tasks lays the groundwork for Phase II, which will be centered on the following tasks:

1. Fabricate an inverting single device equivalent.

2. Fabricate a simple circuit based on the inverting and non-inverting structures and compare its performance to standard CMOS circuits.

3. Develop a device model to allow circuit design.

3. Demonstrate the performance of the CMOS devices at low temperatures.

2. Relationship to Commercial Potential

As stated in Section C. the integrated circuit market is dominated by silicon based CMOS circuits. In this sense the market for the proposed devices already exists and is a multi-billion dollar per year market. The very nature of the proposed devices is such that they are economically attractive to industry. The devices proposed do not require any new or novel facilities for their fabrication, and offer drastically increased packing density without a reduction in feature size. Finally, their implementation in electronic circuits will be transparent to the end user. Therefore, we believe the key issues involved in the commercial success of the proposed devices is their performance and packing density as compared to conventional devices. If it can be shown that the SDCMOS circuits perform as well as conventional CMOS, and that they can fabricated in such a manner as to allow an increased packing density, we believe that commercialization will be successful. Furthermore, the Schottky barrier devices can also operate effectively at low temperatures, allowing their use in cryoelectronics applications.

At this time, the sole owner of all patent rights to the proposed devices is the Principal Investigator. If the devices develop as anticipated, they will be licensed to the semiconductor industry.

I. Key Company Personnel

The key company personnel and Principal Investigator, Mr. James D. Welch, received his Master's Degree in Electrical engineering from the University of Toronto in 1974, and Juris Doctorate in 1982 from University of Nebraska-Lincoln. He has developed the pMOS and nMOS $CrSi_2$ Schottky barrier FETs on his own and retains sole patent rights to devices fabricated by the thin film reaction of chromium and silicon through US patent 4,696,093 and additional patent protection is pending covering the fabrication of devices through the direct deposition of $CrSi_2$ and other metals. He is the Principal Investigator for DOE Grant #DE-FG47-93R701414 where he has successfully produced devices based on the thin film reaction of chromium and silicon.

J. Facilities

The proposed research will be performed at the University of Nebraska-Lincoln, where all facilities are located. The Principal investigator has an agreement with the University to allow him to use the equipment for the proposed research program. This agreement is attached. The facilities required for the proposed program are:

1. Laminar Flow Room and Photolithographic Facility
2. Oxidation and diffusion furnaces
3. Electron Beam Evaporator
4. Magnetron sputter deposition system
5. Hewlett Packard Semiconductor Parameter analyzer and probe station
6. Reactive Ion Etching System
7. Scanning Electron Microscope
8. Mechanical Stylus

K. Consultants and Subcontracts

The proposed research program is based on the device as developed by the Principal Investigator. He will be assisted in the fabrication and characterization of the devices by Professor N.J. Ianno, Professor R.J. Soukup, of the Department of Electrical Engineering. The consultants have all agreed to participate in the project at the prescribed levels and their certifications are attached.

N.J. Ianno has over 10 years experience in the field of plasma processing of semiconductors including plasma etching, sputter deposition, as well as experience in device fabrication. This work has led to over 20 publications in referred journals and numerous conference presentations. He will be responsible for patterning of the devices sputter deposition of the chromium, and rapid thermal processing.

R.J. Soukup has over 20 years experience in fabrication and characterization of Schottky barrier and p-n junctions. He will be responsible for the characterization of the $CrSi_2$ junctions.

An undergraduate student will hired through a University subcontract to help with the fabrication process.

L. Prior, Current and Pending Support

A. Current Support

The Principal investigator is currently supported by DOE Grant #DE-FG47-93R701414 "Novel Procedure for the Fabrication of MOSFETs". The assigned monitor is Mr. Fred Hart. This program ends January 1, 1995 and thus will not overlap with the proposed program. The DOE project is focused on the initial fabrication of $CrSi_2$ based FETs through the thin film reaction of chromium with silicon on separate p and n-type substrates. As seen in Figure 1, this has been successfully completed. This project accounts for approximately 50% of the Principal Investigator's time until January 1, 1995. This is the only current support in force involving the principal investigator.

B. Pending Support

This proposal is has also been submitted to another solicitation from the DOD SBIR program:

Title: Single Device Equivalent to CMOS
Topic: AF95-135
P.I.: James Welch
Submitted: 1/13/95

This proposal has also been submitted to the Dept. of Energy:

Title: Single Device Equivalent to CMOS
Topic: Energy Related Inventions
P.I.: James Welch
Submitted: 8/12/94

M. Cost Proposal

Welch Research
10328 Pinehurst Ave.
Omaha, NE 68124

Work performed at:
University of Nebraska-Lincoln
Department of Electrical Engineering
209N WSEC
P.O. Box 880511
Lincoln, NE 68588-0511

Title: Fabrication of Novel CMOS Devices

AF95-138, Innovative Microelectronics Device Development

Materials and Supplies

a. Cr, Mo, Al Targets	$750	f. Lab Clothing etc.	$300
Pt Target	$3000		
b. Chemical Reagents	$525	g. Lab Supplies	$300
c. Photoresist and Assoc. Chemicals	$500	h. Furnace Tubes	$700
d. Substrates	$720	i. Liquid Nitrogen	$300
e.Film for SEM and Optical Micro.	$380	j. Etch Gas for RIE	$500
		k. Misc.	$500
		l. Mask Fabrication	$1,800

Total Materials and Supplies: $10,275
Subcontract to University of Nebraska-Lincoln: $4,061

Direct labor

A. Senior Personnel

	Rate	Time	Total
James Welch	$50.57	500 hrs	$25,285

C. Fringe Benefits ($0)

Total Salary $25,285

Special Testing
Attached is an agreement to allow the P.I. to use the listed facilities and equipment for the proposed program for a cost of $5,000. This equipment is necessary for the completion of the proposed program and is all in place at the University of Nebraska-Lincoln.

UNL fee	$5,000

Travel

1 trip by the PI to University of Toronto to supervise Mask Fabrication	$1,800

Consultant Services

	Rate	Time	Total
N.J. Ianno	$443/day	23 days	$10,189
R.J. Soukup	$443/day	12 days	$5,316
Total			$15,505

N.J. Ianno is primarily responsible for device patterning via reactive ion etching (RIE), and sputter deposition of the chromium. Since each wafer must be patterned, this will require a substantial amount of time. He will assist the P.I. in mask design and device characterization.

R.J. Soukup will perform junction characterization. This will entail theoretical modeling of the Schottky barrier performance and experimental acquisition of appropriate parameters.

Cost: $61,926

Fee: 6% of Cost = $3,716

Total Request: $65,642

Name: James D. Welch, Sole Proprietor

_____ _____
Date

21.a No executive agency of the United States Government has reviewed the accounts or records in connection with any other government prime contract or subcontract in the past twelve months.

b No use of government equipment will be required.

c. Yes, Advanced payment.

22. firm-fixed price

N. Company Commercialization Report

Not Applicable

AF95-135 Single Device CMOS Equivalent

Submitted by

N.J. Ianno
Center for Microelectronic and Optical Research
Department of Electrical Engineering
209 N WSEC
Lincoln, NE 68588-0511
(402) 472-1965

Submitted To:

James D. Welch, Sole Proprietor
James D. Welch Research
10328 Pinehurst Ave.
Omaha, NE 68124
(402) 391-4448

Salaries:	
Student Worker	$5.5/hr, 520 hrs=$2,860
Overhead	42% of salary, $1,201
Total UNL Subcontract	$4,061

AF95-138 Single Device CMOS Equivalent

Submitted by

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Center for Microelectronic and Optical Research
Department of Electrical Engineering
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Student Worker	$5.5/hr, 520 hrs=$2,860
Overhead	42% of salary, $1,201
Total UNL Subcontract	$4,061

This proposal has also been submitted to the Dept. of Energy:

Title: Single Device Equivalent to CMOS
Topic: Energy Related Inventions
P.I.: James Welch
Submitted: 8/12/94

M. Cost Proposal

Welch Research
10328 Pinehurst Ave.
Omaha, NE 68124

Work performed at:
University of Nebraska-Lincoln
Department of Electrical Engineering
209N WSEC
P.O. Box 880511
Lincoln, NE 68588-0511

Title: Fabrication of Novel CMOS Devices

AF95-135, Solid State Electronics Applied Research

Materials and Supplies

a. Cr, Mo, Al Targets	$750	f. Lab Clothing etc.	$300
Pt Target	$3000		
b. Chemical Reagents	$525	g. Lab Supplies	$300
c. Photoresist and Assoc. Chemicals	$500	h. Furnace Tubes	$700
d. Substrates	$720	i. Liquid Nitrogen	$300
e.Film for SEM and Optical Micro.	$380	j. Etch Gas for RIE	$500
		k. Misc.	$500
		l. Mask Fabrication	$1,800

Total Materials and Supplies: $10,275
Subcontract to University of Nebraska-Lincoln: $4,061

Direct labor

A. Senior Personnel

	Rate	Time	Total
James Welch	$50.57	500 hrs	$25,285

C. Fringe Benefits ($0)

Total Salary $25,285

AGREEMENT TO CONSULT

WHEREAS JAMES D. WELCH RESEARCH WISHES TO GAIN ACCESS TO THE UNIVERSITY OF NEBRASKA DEPARTMENT OF ELECTRICAL ENGINEERING SOLID STATE FABRICATION LAB TO DO SOLID STATE DEVICE FABRICATION RESEARCH; AND

WHEREAS JAMES D. WELCH RESEARCH HAS APPLIED FOR GRANT FUNDS TO SUPPORT SAID SOLID STATE DEVICE FABRICATION RESEARCH; AND

WHEREAS THE UNDERSIGNED PROFESSOR AT THE ELECTRICAL ENGINEERING DEPARTMENT AT THE UNIVERSITY OF NEBRASKA IS KNOWLEDGEABLE IN SOLID STATE ELECTRONICS AT THE PH.D. LEVEL, AND IS AGREEABLE TO CONSULTING WITH JAMES D. WELCH DURING THE COURSE OF SAID RESEARCH AT THE RATE OF $55.37 PER HOUR; AND

WHEREAS THE UNDERSIGNED ATTESTS THAT SAID RATE IS HIS STANDARDLY QUOTED HOURLY RATE.

THEREFORE IT IS AGREED THAT UPON REQUEST OF JAMES D. WELCH RESEARCH THE UNDERSIGNED WILL SCHEDULE SUFFICIENT TIME TO CONSULT WITH MR. WELCH IN RETURN FOR THE ABOVE HOURLY FEE.

IT IS ALSO AGREED THAT THE UNDERSIGNED PROFESSOR SHALL NOT INCUR ANY LIABILITY FOR ADVICE PROVIDED.

IT IS ALSO AGREED THAT THE UNDERSIGNED SHALL NOT REVEAL ANY TRADESECRETS DEVELOPED DURING THE COURSE OF THE RESEARCH UNITL SUCH TIME AS AGREED TO BY JAMES D. WELCH RESEARCH, AND THAT THE UNDERSIGNED WILL MAKE NO CLAIM TO ANY PATENT RIGHTS RESULTING FROM SAID RESEARCH OTHER THAN TO BE LISTED AS AN INVENTOR WHERE APPROPRIATE.

IN AGREEMENT WITH THE ABOVE THE FOLLOWING PARTIES HERETO AFFIX THEIR SIGNATURES.

J.D. Welch

JAMES D. WELCH
FOR JAMES D. WELCH RESEARCH

1/11/95
DATE

Rodney J. Soukup

DR. RODNEY SOUKUP
PROF. ELECTRICAL ENGINEERING

1/11/95
DATE

AGREEMENT TO CONSULT

WHEREAS JAMES D. WELCH RESEARCH WISHES TO GAIN ACCESS TO THE UNIVERSITY OF NEBRASKA DEPARTMENT OF ELECTRICAL ENGINEERING SOLID STATE FABRICATION LAB TO DO SOLID STATE DEVICE FABRICATION RESEARCH; AND

WHEREAS JAMES D. WELCH RESEARCH HAS APPLIED FOR GRANT FUNDS TO SUPPORT SAID SOLID STATE DEVICE FABRICATION RESEARCH; AND

WHEREAS THE UNDERSIGNED PROFESSOR AT THE ELECTRICAL ENGINEERING DEPARTMENT AT THE UNIVERSITY OF NEBRASKA IS KNOWLEDGEABLE IN SOLID STATE ELECTRONICS AT THE PH.D. LEVEL, AND IS AGREEABLE TO CONSULTING WITH JAMES D. WELCH DURING THE COURSE OF SAID RESEARCH AT THE RATE OF $ 55.27 PER HOUR; AND

WHEREAS THE UNDERSIGNED ATTESTS THAT SAID RATE IS HIS STANDARDLY QUOTED HOURLY RATE.

THEREFORE IT IS AGREED THAT UPON REQUEST OF JAMES D. WELCH RESEARCH THE UNDERSIGNED WILL SCHEDULE SUFFICIENT TIME TO CONSULT WITH MR. WELCH IN RETURN FOR THE ABOVE HOURLY FEE.

IT IS ALSO AGREED THAT THE UNDERSIGNED PROFESSOR SHALL NOT INCUR ANY LIABILITY FOR ADVICE PROVIDED.

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IN AGREEMENT WITH THE ABOVE THE FOLLOWING PARTIES HERETO AFFIX THEIR SIGNATURES.

JAMES D. WELCH
FOR JAMES D. WELCH RESEARCH

1/11/95
DATE

DR. N.J. IANNO
PROF. ELECTRICAL ENGINEERING

1/11/95
DATE

USE AGREEMENT

This Use Agreement (the "Agreement") made this 9th day of June, 19 94, by and between the Board of Regents of the University of Nebraska (the "Board") and James D. Welch (the "User").

The parties agree as follows:

1. Premises to be Used. The Board hereby grants to the User the right to use See ATTACHMENT

(describe building, room number and equipment, if appropriate) (the "Premises") for the following described purposes: Solid State Device Fabrication

(describe usage purposes) (the "Usage Purposes").

2. (Amended). Term and Subordination. This Agreement, as it applies to Usage Purposes, shall be for a term of six months from the date payment as per Article 4 herein is made and proof of insurance as per Article 7 is provided, and shall be automatically renewable for consecutive six-month periods unless the Board of User notifies the other party in writing at least thirty (30) days prior to the end of the term that this Agreement will not be renewed. The right of the User to utilize the premises for the Usage Purposes is expressly subordinated to the use of the Premises by the Board for teaching and Board-funded or sponsored research.

Notwithstanding the provisions of this Section 2, the Board may terminate this Agreement, at any time if the Board determines, in its reasonable judgment, that (i) the Usage Purposes conflict with the ability of the Board to reasonably use the Premises for Board purposes, (ii) the Usage Purposes are inherently dangerous or harmful, (iii) the Usage Purposes are obnoxious as a result of noise, smell or unsightliness or, (iv) the Usage Purposes constitute a violation of laws, rules or regulations to which the Premises or the Board is subject.

This Agreement shall also terminate at such time as the User has made commercial sales of products or services derived from the Usage Purposes equal to $ 1.000.00 in any fiscal year. In such event, the usage of the premises shall cease and the User shall relocate within a reasonable time, not to exceed 6 months, to a Board-sponsored incubator facility or commercial space of the User's choice.

3. Use of Premises. User agrees to keep the premises in a clean, safe and sanitary manner and further agrees to conform with all applicable statutes, ordinances, rules, regulations and order of any governmental authority which apply to the Usage Purposes. If required, the Board shall permit the User to generate, use and maintain confidential laboratory and other business data, reports and files and to use and maintain locked doors and cabinets to insure privacy and confidentiality. Any established Board laboratory safety or other rules and regulations shall be applicable to the use of the Premises by the User.

4. (Amended). Fee for Usage. For access to the facilities during the term of this Agreement, the User shall pay the Board a fee of $5,000, payable in full, in advance.

5. Use of Board Equipment and Other Facilities. Subject to reasonable availability and the use by fully qualified personnel, the Board may grant the right to the User to use

laboratory instruments or other facilities of the Board. In doing so, the User shall be required to adhere to University regulations and standards including cleanup requirements. User shall be charged for all reagents, supplies and other consumables utilized by the User.

6. User Personnel. The User shall designate to the Board Department Head approving this Agreement the Board faculty member responsible for the Premises and shall also designate all other non-Board personnel who will be working on the Premises.

7. Maintenance of Insurance. The User shall obtain and maintain standard public liability insurance for the Premises at the User's expense with a reliable insurance company authorized to do business in the State of Nebraska in the minimum amount of $1,000,000 for each occurrence, $1,000,000 annual aggregate for personal injury and $100,000 for property damage. The policy or policies of insurance shall cover the User and the Board as named insured and shall provide that the insurance shall not be canceled or modified unless thirty (30) days prior written notice is given to the named insured. The User will also obtain and maintain at its expense appropriate workers' compensation insurance. Certificates of such policy(ies) of insurance shall be delivered to the Board after issuance of the policy(ies). The Board shall use its reasonable efforts to assist the User in obtaining such insurance coverage from Board's existing carrier or other sources.

8. Surrender of Premises. Upon termination of the usage portion of this Agreement for any reason, User shall, without further notice of any kind, quit and surrender the possession and occupancy of the Premises to the Board in as good of condition as when received, except for ordinary wear and tear, for damage or destruction by fire or other casualty not due to the carelessness or negligence of User or its agents, employees or invitees. Upon termination of the usage portion of this Agreement, User shall, at its sole cost and expense, remove all items of personal property and equipment.

9. Board Royalty or Ownership Position. If, by addendum to this Agreement, the parties agree that the Board has contributed to the development of an invention, discovery or process from research conducted by a Board faculty or staff member who is the User or a principal of the User, the parties agree to enter into a separate agreement providing for the payment to the Board of a commercial sale of products derived from the invention, discovery or process or the ownership of not less than a five percent (5%) equity interest in the entity which owns or is licensing the invention, discovery or process which equity ownership interest, either in the form of stock of a corporation or a profit and loss interest in a partnership. The agreement relating to the ownership position shall contain standard and appropriate provisions for antidilution. This provision of the Agreement shall survive notwithstanding the termination of the usage portion of the Agreement until a separate written agreement as provided herein is entered into and fully executed between the parties.[1]

10. Notices. All notices hereunder shall be in writing and delivered in person or by registered mail and addressed to the following locations unless another address for such notices shall have been given by one party to the other pursuant to the provisions hereof.

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1 It is expressly agreed that the Board shall have no claim to any rights covered by Patent Number 4,696,093 to Welch, or related rights unless said related rights are the exclusive result of research or advice by other than Welch.

SCHOTTKY BARRIER MOSFET SYSTEMS AND FABRICATION THEREOF

The invention in this Application was developed in part under support provided by a grant from the Energy Related Inventions Program of the United States Federal Department of Energy, Contract No. DE-FG47-93R701314. The United States Government has certain rights in this invention.

This Application is a Continuation-In-Part of copending Application Serial No. 08/250,906.

TECHNICAL FIELD

The present invention relates to Metal Oxide Semiconductor (MOS) device systems and procedures for fabrication thereof. More particularly, the present invention comprises single semiconductor type, Schottky barrier junction inverting and noninverting single devices which demonstrate operational characteristics similar to Complimentary Metal Oxide Semiconductor (CMOS) multiple device systems, and Schottky barrier junction voltage controlled switches which demonstrate operational characteristics similar to a nonlatching silicon controlled rectifier. In addition the present invention is, in part, a system utilizing insulator effected, channel end located, minimized Schottky barrier junction area, low leakage current Schottky barrier rectifying junction geometries in Intrinsic, N and/or P-Type semiconductor, preferably in a single substrate, to form Complimentary Metal Oxide Semiconductor Field Effect Transistor (CMOS) device systems, as well as N or P-channel Metal Oxide Semiconductor Field Effect Transistor (MOSFET) devices with (MOSFET) loads, and N or P-channel balanced differential (MOSFET) device systems. The present invention utilizes both rectifying and semiconductor doping and the like effected non-rectifying

Schottky barrier junctions.

BACKGROUND

The use of conventional diffused junction N and P-Channel Metal Oxide Semiconductor Field Effect Transistors, (hereinafter (MOSFETS), in functional seriesed combination to form Complimentary Metal Oxide Semiconductor, (hereinafter (CMOS)), field effect transistor device systems is well known, as are the benefits associated with the use thereof. Said benefits include enabling realization of very low power consumption digital switching logic circuitry such as is found in electronic wrist watches which run for years on one small battery.

Briefly, a conventional (MOSFET) is comprised of N or P-type semiconductor substrate, in the surface region of which are formed regions of oppositely doped material, separated by a distance therebetween in said semiconductor substrate. The regions of oppositely doped material are termed the "Source" and "Drain" and the distance therebetween is termed the "Channel Region". Diffused rectifying junctions are thus caused to exist at the ends of the channel region, both at the source and at the drain. Continuing, atop the channel region surface is present an insulating material, such as silicon dioxide, atop of which insulating material is present a "Gate" which is made from an electrically conductive material. Application of a voltage from the drain-to-source of a proper polarity, simultaneous with the application of a gate-to-source voltage of a proper polarity causes the channel region to "invert" and become of a doping type similar to that in the source and drain regions, thereby providing a conductive pathway between said drain and source. That is, application of a gate-to-source voltage modulates the conductivity of, hence flow of current between, the drain and source. Because the resistivity of the insulating material is

high, very little gate current is required to effect modulation of said drain to source current flow. As mentioned above, conventional (CMOS) device systems comprise a seriesed combination of electrically connected N and P-channel (MOSFET) devices, formed on P and N-type semiconductor respectively. To form (CMOS) the drain of an N-channel (MOSFET) device is electrically connected to the drain of the a P-channel (MOSFET) device and the source of the P-channel device is connected to a positive (+Vdd), while the source of the N-channel (MOSFET) device is connected to a lower voltage (-Vss), typically ground. In use, a relatively low, (approximately the voltage appplied to the source of the N-channel (MOSFET) device), gate voltage applied simultaneously to the gates of said electrically connected devices modulates the P channel device so that it conducts, while having no channel conductivity increasing effect on the N channel device. Similarly, simultaneous application of a relatively high, (with respect to the voltage applied to the source of the N-channel (MOSFET) device, eg. approximately +Vdd), gate voltage affects the N and P channel devices in an opposite manner. That is the N-channel device channel inverts and conductivity is effectively increased from the associated source to drain, while the P-channel device channel conductivity is not increased. The result being that varying gate-to-source voltage from relatively low, (-Vss), to relatively high, (+Vdd), causes the voltage present at the electrically connected N and P-channel device drains, which terminal is essentially electrically isolated from the gates, to vary essentially between that applied to the source of the P-channel device, (+Vdd), and that applied to the source of the N-channel device, (typically, but not necessarily, ground potential), respectively. Said (CMOS) is then inverting between input and output. As mentioned above, (CMOS) switching is effected with very little gate current flow, as the insulating material between the gate and the semiconductor is of a very high resistance, (eg. ten-to-the-forteenth ohms or

higher). As well, drain to source current flows only briefly at the switching point when both devices are momentarily conducting. This is because current cannot flow through an electrically connected series of (MOSFETS) when either thereof does not have a conducting inverted channel present. Conventional (MOSFET) and (CMOS) operational characteristics are described in numerous circuit design texts such as "Basic Integrated Circuit Engineering" by Hamilton and Howard, McGraw-Hill, 1975.

While conventional (CMOS) device systems provide benefits, fabrication thereof is by diffused junction technology which requires many steps, including many photoresist procedures, sequential mask alignments, and various etches. It is to be appreciated that each such step involves an efficiency factor, and thereby introduces defects leading to decreased yield of working devices on a fabrication substrate. In some instances the ratio of working to the total devices attempted on a substrate can be fifty (50%) percent or even less. For instance if a procedure step carries a ninety (90%) percent efficiency factor, (an extremely low value used for demonstrative purposes), after two such steps only eighty-one (81%) percent of the devices will be operational. After six (6) such steps, it should be appreciated, the effective yield of working devices will be less than fifty (50%) percent. Obviously, if the number of steps in a fabrication procedure can be reduced the yield of working devices can be increased. However, conventional diffused junction technology does not allow reducing the number of steps involved in a fabrication procedure below a relatively large number.

A fabrication procedure which requires a reduced number of fabrication procedure steps to provide functionally equivalent (CMOS) device systems would therefore be of utility.

With that in mind it is to be appreciated that an

alternative to conventional diffused junction technology is that of Schottky barrier junction technology. The present invention utilizes said schottky barrier junction technology in a fabrication procedure requiring a relatively few number of steps to provide Schottky Barrier (CMOS) device systems and a single substrate type single device equivalent to (CMOS).

A Schottky barrier is essentially a rectifying junction formed between, for instance, a nonsemiconductor (eg. metal or metal compound), and a doped semiconductor. Such a junction exhibits a "built-in" Schottky barrier potential which serves to inhibit current conduction when a voltage of one polarity is applied thereto, and allows current to flow more easily when an opposite polarity voltage is applied thereto. In important respects then, a Schottky barrier acts much like a diffused junction rectifier.

A Search of relevant references has provided an article by Hogeboom and Cobbold, titled "Etched Schottky Barrier (MOSFETS) Using A Single Mask". Said article describes the fabrication of a P-Channel (MOSFET) on N-type silicon with aluminum forming the rectifying junction schottky barrier source and drain junctions. (Note that aluminum does not form a rectifying junction schottky barrier on P-type silicon hence is not an appropriate metal for use in realization of N-channel Schottky barrier (MOSFETS)). Said article also describes both N and P-Channel conventional diffused junction (MOSFETS) fabricated using a single mask, but which required a diffusion of a dopant, hence, did not operate based upon schottky barrier junction presence. Aluminum present provided non-rectifying contact to diffused regions as in conventional (MOSFETS). This paper also suggests the use of vanadium to form source and drain regions. It is also noted that this paper describes use of a silicon dioxide undercutting etch which facilitates self delineation of fabricated devices

when essentially line-of-sight aluminum deposition is achieved. (The silicon etchant taught is a mixture of fifty (50) parts acetic acid, thirty (30) parts nitric acid, twenty (20) parts hydrofluoric acid and one (1) part aniline). A Patent to Welch, No. 4,696,093 describes a procedure for fabricating Schottky barrier (MOSFETS), including an approach requiring only one-mask and one-etch and the use of chromium, (which after application to silicon is subjected to an annealing procedure to form chromium disilicide), as the metal used to form rectifying source and drain Schottky barrier junctions. A Masters Thesis presented by James D. Welch at the University of Toronto in 1974 titled "Design and Fabrication of Sub-Micron Channel MOS Transistors by Double Ion-Implantation" mentions Schottky barrier rectifying junctions discovered to exist after a thirty (30) minute, six-hundred-fifty (650) degree centigrade anneal of chromium present on the back, unpolished, side of an N-type silicon substrate. The reverse breakdown voltage of said rectifying junctions was found to be upwards of eighty (80) volts. However, said thesis work did not include investigation of annealing deposited chromium on P-type silicon. A paper by Lebedev and Sultanov, in Soviet Physics Semiconductors, Vol. 4, No. 11, May 1971, pages 1900-1902 teaches the chromium diffused into P-type Silicon at high, (eg. twelve hundred (1200) degrees centigrade), for long periods of time, (eg. twenty (20) to fifty (50) hours), dopes said P-type silicon N-type. Nothing, however, is stated regarding the properties of chromium disilicide formed by annealing a thin film of chromium which has been deposited upon said P-type silicon silicon at lower temperatures. A paper by Lepselter and Sze, titled "SB-IGFET: An Insulated-Gate Field Effect Transistor Using Schottky Barrier Contacts for Source and Drain", in the Proceedings of the IEEE, August 1968, pages 1400 through 1402 describes a P-Channel schottky barrier insulated gate field effect transistor, (ie. IGFET), fabricated using schottky barrier junctions for source and drain. Said IGFET

utilized platinum silicide in the formation of the source and drain junctions. It is stated that during operation the source junction of the device is reverse biased in the inverted channel region and that reverse leakage or tunneling current therethrough is what applied gate voltage modulates. The Lepselter et al. article however, makes no mention of the use of Schottky barriers to form N-Channel devices on P-type silicon. In fact, owing to the rather large reverse barrier height difference between platinum silicide and N-type silicon, (ie. 0.85ev), and between platinum silicide and P-type silicon, (ie. 0.25ev), it is unlikely that N-channel devices would be operablle, or even if they were, that an effective (CMOS) device system could be achieved using platinum-silicide to form both N and P-channel devices. This is because the (MOSFET) devices in a (CMOS) device system must have essentially symetrical and complimentary operational characteristics to provide efficient switching capability. The Lepselter et al. article provides an equation for calculating tunneling current density through a reverse biased Schottky barrier junction:

$$J = \exp\left(\frac{-4}{3} \frac{(\mathrm{SQRT}\ 2m^*(PHI)2)^{3}}{q\ h\ E} \right)$$

where E is the electric field induced by application of a voltage across the junction,
m* is the effective mass,
h is Boltzman's constant,
PHI is the reverse barrier potential, and
J is current density.

The Lepselter et al. article is incorporated by reference herein. Many texts describe Schottky barrier junctions and they will not be further discussed in this Disclosure.

Continuing, a recent Patent to Honma et al., No. 5,177,568 describes a tunnel injection type semiconductor device having a Metal-Insulator-Silicon (MIS) structure comprising a semiconductor region, a source, a drain and a gate electrode wherein said source and drain are composed of a metal or metal compound member, respectively, and wherein both have an overlapping portion with said gate electrode. The Source provides a Schottky barrier junction to said semiconductor region while said drain provides an non-rectifying contact to said semiconductor region. A tunneling current is caused to flow across a Schottky barrier junction between said source and said drain, controlled by a gate voltage. This Patent describes formation of a (CMOS) device system wherein schottky barriers serve as source region contacts to N and P-type silicon and wherein interconnected drain contacts are non-rectifying. The devices described in this Patent are very interesting, but fabrication thereof obviously requires rather complicated channel region doping profile effecting and yield reducing steps to effect rectifying junctions at the source and non-rectifying junctions at the drain of a (MOSFET) structure. That is, economic savings as compared to conventional diffused junction (MOSFET) fabrication would seem to be reduced by the channel doping requirements. Use of doping and varying band gap materials are disclosed as approaches to realizing the devices described. It is also noted that the devices described apparently operate, (show gate controlled drain current flow), with the semiconductor between source and drain "accumulated" while a source Schottky barrier junction is reverse biased by applied drain to source voltage polarity. That is for a N-type substrate, a positive gate to source voltage is applied and for a P-type semiconductor a negative polarity gate to source voltage would be applied. As will be seen in following Sections herein, present invention devices preferably operate by effecting "inversion" in semiconductor between source and drain. For

instance, for an N-type semiconductor the applied gate voltage during operation is negative in polarity when applied drain to source voltage is positive in polarity. For P-type semiconductor the applied gate to source voltage polarity during operation is positive while the drain to source voltage polarity is negative. This is cited as a major distinction in operational bases between the Honma et al. devices and the present invention devices.

A Patent to Koeneke et al., No. 4,485,550 describes MOS and (CMOS) devices in which selective doping of regions surrounding Schottky barrier source and drain improves the operational characteristics of Schottky barrier MOS devices. The doping serves to reduce leakage current to the substrate in which said devices are fabricated and to increase current injected into the channel region. The later effect is at least partially due to the elimination of a gap between the channel region and Schottky barrier junctions at source and drain. Two problems inherrent in Schottky barrier (MOSFET) fabrication are thus attacked by the 550 Patent devices.

A Patent to Lepselter, No. 4,300,152 describes a (CMOS) device in which at least one of the N and P-Channel devices is a Schottky barrier based device. It is taught that a (CMOS) device system utilizing such is immune to latch-up based upon Silicon Controlled Rectifier-like action in (CMOS) device systems.

A Patent to Mihara et al., No. 5,049,953 describes a Schottky barrier device in which a shield layer of a second conductivity type imposed between a Schottky barrier and a substrate serves to reduce leakage current.

No known reference, however, teaches, as does the present invention disclosure, that a relatively simple fabrication

procedure utilizing both N and P-type semiconductor can simultaneously efficiently form low, insulator effected, leakage current balanced Schottky barrier rectifying junctions in (MOSFET) Source and Drain regions on both said N and P-type semiconductor, preferably in a single semiconductor substrate, thereby allowing essentially balanced complimentary N and P-channel (MOSFETS) with Schottky barrier junctions at both source and drain to be easily achieved, particularly on a single substrate. This is a very significant point as it would not be obvious to one skilled in the art that such a single simultaneous procedure should exist or what elements, (eg. metal, metal-silicide and semiconductor), should be utilized in said procedure or what the procedure should be followed. The present invention provides missing teachings along with documented experimental results supporting said teachings. The present invention, however, goes even further and teaches that a single device equivalent to (CMOS) can be achieved on a single dopant type, or even intrinsic, semiconductor substrate utilizing Schottky barrier technology, with or without leakage current reducing insulator material presence, by provision of a voltage monitoring contact to the channel region under the gate electrode of a Schottky barrier (MOSFET) structure. As described elsewhere in this disclosure, said device operates because Schottky barriers formed using appropriate semiconductors and metals and/or metal silicides form rectifying junctions with either N or P-type semiconductor, and effective (MOSFET) channel region semiconductor doping can be effected by application of a gate voltage in a (MOSFET) structure. All known (CMOS) devices require the presence of N and P-type doped semiconductor. The present invention teaches that a single device equivalent to (CMOS), in contrast, requires only a single type, (N or P-type), semiconductor substrate be present, emphasis added. This enables cost savings and improved fabrication efficiency.

It is mentioned that in a proprietory report, dated January 10, 1991, which was prepared by the National Institute of Standards and Technology, (NIST) in support of the grant which has funded work leading to the disclosure herein, it was concluded that the present invention could have an impact on energy conservation and utilization and that if the projected performance of the invention can be achieved, then commercial success seems assured. Said proprietory NIST report focused upon the use of chromium deposited onto both N and P-type silicon and a common anneal procedure to for Schottky barrier (MOSFETS) with rectifying junctions at both source and drain. Said NIST report was provided in response to a confidential application for grant funds submitted to the agency which is funding the present work, (the United States Department of Energy), years earlier by the inventor herein, in search of support to allow actual present invention reduction to practice.

The present invention teaches workable systems and recommended fabrication procedures therefore.

DISCLOSURE OF THE INVENTION

The present invention comprises Schottky Barrier Metal Oxide Semiconductor (MOS) devices and systems as well as recommended fabrication procedures therefore. The present invention is based in the fact that certain metals and compounds, (eg. silicides), etc. form rectifying Schottky barrier junctions with both N and P-type semiconductor, and that a gate voltage applied to a Metal Oxide Semiconductor (MOS) device can effect an accumulated, a depleted or an inverted surface channel region in a semiconductor surface, (that is, the effective doping type, (N, P and Intrinsic), of said semiconductor in said channel region can be controlled by application of a gate voltage). A Schottky barrier junction in a channel region then can be made to demonstrate rectifying properties, in opposite voltage polarity directions when a gate voltage is applied to effect, or not, a (MOS) semiconductor surface channel region doping type. As well, application of a gate voltage in a (MOS) device can, by controlling an effective semiconductor channel region doping level, (eg. number of carrier-per-centimeter-cubed), affect reverse bias current flow through a reverse biased Schottky barrier junction adjacent to said doping level controlled semiconductor channel region, and in a Metal Oxide Semiconductor Field Effect (MOSFET) Transistor device fabricated with Schottky barrier source and drain junctions, cause (MOSFET) drain current to vary with applied gate voltage. The present invention utilizes rectifying Schottky barrier junctions and also utilizes semiconductor region accessing Schottky barrier, (that is semiconductor-nonsemiconductor component), junctions which demonstrate essentially non-rectifying behavior as a result of being formed on, for instance, heavily doped semiconductor. Said essentially non-rectifying junctions provide nonrectifying electrical access to semiconductor regions.

Colaterally, the present invention also recognizes prior art disclosures to the effect that Schottky barrier junctions in (MOSFET) devices demonstrate two defects, these being high leakage current and, that typically, high resistance gaps exist between a Schottky barrier (MOSFET) source or drain and semiconductor channel region under a gate. As a solution thereto the present invention teaches etched, (preferably isotropic so as to undercut gate oxide), surface semiconductor regions at the ends of semiconductor channel regions, in which etched surface semiconductor regions small cross sectional area Schottky barrier junctions are present only in semiconductor regions at the ends of said semiconductor channel regions. Said result is accomplished by use of semiconductor protecting insulator material, (eg. Silicon dioxide where silicon is utilized), to cover and prevent Schottky barrier formation in etched surface semiconductor regions, other than at the ends of semiconductor channel regions.

In one embodiment, the present invention assumes the presence of a silicon substrate in which are present alternating N and P-type doped regions in a checkerboard pattern, similar to that required for fabrication of conventional Complimentary Metal Oxide Semiconductor (CMOS) device systems, (see Background Section), fabricated using diffused rectifying junction technology. Atop said silicon substrate surface there is caused to be present an insulating material, such as, but not limited to, thermally grown or deposited silicon dioxide and/or silicon nitride etc., into which insulating material are caused to be formed patterns above both said N and P-type regions. Said patterns typically consisting of two openings each, each of which openings is delineated by remaining insulating material, said insulating material between two associated openings being a gate insulating material above a silicon channel region, said channel

region being wholly present in either an N or P-type silicon region. Said openings, at a minimum, provide access to the upper surface of the silicon under said insulating material, and alternatively can comprise an etching into said silicon so that silicon walls are formed at the edges of said openings under the insulating material, and perhaps undercut said insulating material as the result of an isotropic silicon etch. Atop said insulating material and atop said silicon in the openings of said patterns, there is caused to be present metal and/or a metal-silicide, (typically by vacuum evaporation or sputtering techniques), which when processed, (typically by an elevated temperature anneal), causes said metal and/or metal-silicide in contact with said silicon, (whether N or P-type), to form rectifying Schottky barrier junctions with said N and P-type silicon simultaneously. It is noted that line-of-sight deposition of a metal-silicide into etched silicon regions might be more appropriate when very small dimension devices are fabricated, (see first fabrication procedure supra). This is because formation of a silicide from a metal deposited upon a semiconductor can involve significant, (eg. hundreds to thousands of angstroms), migration of metal atoms into the semiconductor. If a preformed metal-silicide is deposited onto a semiconductor, this effect might be greatly reduced because a lower temperature and/or shorter anneal time, for instance, can serve to form rectifying junctions between said deposited metal-silicide and semiconductor. However, removal of deposited silicide in areas where it is unwanted can be difficult.

While not limiting, it has been found experimentally that a workable single mask/single etch fabrication procedure for realizing the above described (CMOS) device system is as follows:

1. Provide a silicon substrate, (typically, but not necessarily, of (100) crystal orientation), with alternating N

and P-type regions, (each typically doped ten-to-the-fifteenth per-centimeter-cubed), present therein.

2. Grow silicon dioxide atop said substrate to a depth suitable for use as a gate oxide in a (MOSFET), (typically but not necessarily six-hundred (600) to three thousand (3000) angstroms).

3. Apply photoresist to the surface of said silicon dioxide.

4. Expose said photoresist through a mask which causes two openings to be effected therein over each N and P-type region, each of which openings is surrounded by silicon dioxide, with the silicon dioxide between each two associated openings being a gate oxide above a silicon channel region.

5. Etch the silicon dioxide, preferably anisotropically, to the surface of the silicon and then continue to isotropically etch into said silicon to a depth of hundreds of angstroms to one (1) micron or more. (Note that an isotropic silicon etch will undercut the silicon dioxide laterally a length approximately equal to the depth to which said silicon is etched perpendicular to the surface of the silicon substrate. This helps effect discontinuous metal or metal-silicide deposition in step 7 supra).

6. Remove said photoresist, preferably by an asher system in which plasma activated oxygen molecules effectively burn said photoresist away.

7. Deposit metal and/or metal-silicide by a line-of-sight method so that it is present atop the silicon dioxide and atop the resulting open surface of said silicon, in a discontinuous, device self-delineating, manner. A workable depth in the case

where chromium is utilized is eight-hundred (800) angstroms wherein, a step 6 isotropic silicon etch depth of one (1) micron or more is utilized. However, it is noted that said examples are not to be considered limiting of the invention.

8. Process, (typically but not necessarily by an elevated temperature anneal), the resulting substrate so that rectifying Schottky barrier junctions are simultaneously formed between said metal or metal-silicide and said silicon with which said metal or metal-silicide is in contact, in both N and P-type silicon regions. It has been found experimentally that a four-hundred-fifty (450) degree centigrade, thirty (30) minute vacuum anneal works well when chromium is utilized. Again, said example is not to be considered limiting of the invention.

9. Remove unwanted remaining unreacted silicide forming metal with an etchant.

It should be appreciated that the recited procedure can, in a relatively few fabrication procedure steps result in self-delineated N and P-Channel (MOSFETS) being simultaneously formed on the processed silicon substrate in P and N-type silicon regions respectively. To then form (CMOS) it is only necessary to electrically interconnect the drain of a device formed in one type, (eg. N or P-type), of silicon to the drain of a device formed in the other type, (eg. P or N-type), silicon. The sources of each such resulting pair of (MOSFET) devices can then be connected to appropriate external source(s) of constant potential electrical voltage, and gate-to-source voltages applied to the metal and/or metal silicide atop the silicon dioxide in the channel regions to control the voltage present at said electrically connected drains. Said recited procedure might be best suited to fabrication utilizing line of sight deposition of silicides where discontinuous deposition, that atop the silicon

dioxide and that atop the silicon in the source and drain regions, can be achieved.

As a variation on the above recited procedure one can, in step 5 thereof, cause an opening in silicon dioxide in an N-type region and an opening in a P-type region to be merged into a single opening, thereby effecting natural connection of the drain of one device with the drain another. The remaining openings from each pair of openings will then serve as the sources for connection to external source(s) of electrical voltage. The difference in the presently described embodiment is that the electrical connection of the drain regions of N and P-Channel devvices straddles the junction between associated N and P-type regions in contact with said silicon in said N and P-type regions, rather than by a means which provides insulation from the silicon substrate at said electrical connection point.

An etch and metal deposition as described in the article by Hogeboom and Cobbold cited in the Background Section, but in which the silicon substrate contains both N and P-type regions, and in which the metal deposited, however, is chromium, followed by an anneal at four-hundred-fifty (450) to five-hundred (500) degrees centigrade for thirty (30) minutes to simultaneously form Schottky barrier junctions in both N and P-type silicon regions, can cause simultaneous formation of operable N and P-Channel (MOSFET) devices which can be electrically connected to provide (CMOS) device systems. It is mentioned that while Hogeboom and Cobbold describe use of a wet acid etch to provide an isotropic silicon etch to undercut the silicon dioxide, a more controlable, (the etchant taught in the Hogeboom and Cobbold article has been found to etch silicon at approximately three-thousand 3000 angstroms a second), and hence, perhaps preferable approach involves use of dry plasma anisotropic etching of silicon dioxide using CF4 gas, (perhaps with a bit of hydrogen added thereto), at

low pressure, (eg. a militorr) and relatively high plasma energy, to provide silicon dioxide walls at the edges of the etched patterns which are essentially perpendicular to the silicon surface, followed by an elevated pressure, (eg. hundreds of militorr), reduced plasma power isotropic plasma etching of the silicon using CF4 gas with added oxygen (eg. five (5%) percent), to provide a an etched silicon which undercuts the silicon dioxide. As mentioned, undercutting said silicon dioxide aids achieving discontinuous metal or metal-silicide deposition. This can be important where chromium is deposited as it tends to adhere to the silicon dioxide edge. Where chromium deposition is by sputtering, it has even been found that chromium is deposited on the silicon beneath the undercut silicon dioxide. This effect can be used advantageously, however, (see supra).

Continuing, while the above recited fabrication method is workable, it has been found that it is highly dependent upon the silicide forming metal deposition step. That is, if the silicide forming metal, or silicide, deposition is not by a line-of-sight technique, (ionized cluster deposition would be a preferred approach), said silicide forming metal tends to cover the entire substrate, even under an undercut silicon dioxide, and cause a short between the drain and source. An alternative fabrication procedure which does not require such stringent control of the silicide forming metal deposition step, hence, which is preferred, is as follows:

1. Provide a silicon substrate, (typically, but not necessarily, of (100) crystal orientation), with alternating N and P-type regions, (each typically doped ten-to-the-fifteenth per-centimeter-cubed but not limited thereto), present therein.

2. Grow silicon dioxide atop said substrate to a depth suitable for use as a gate oxide in a (MOSFET), (typically but

not necessarily six-hundred (600) to three (3000) thousand angstroms).

3. Deposit a layer (eg. five-thousand (5000 Angstroms or more), of gate forming metal, (eg. Chromium or preferably Aluminum), atop said Silicon Dioxide.

4. Apply photoresist to the surface of said layer of gate forming metal.

5. Expose said photoresist through a mask which causes two openings to be effected therein over each N and P-type region, said openings corresponding to Source and Drain regions with the space therebetween between being a channel region in the Silicon beneath the Silicon Dioxide and layer of gate forming metal.

6. Etch the layer of gate forming metal and silicon dioxide, preferably anisotropically, to the surface of the silicon and optionally continue to etch into said silicon to a depth of hundreds of angstroms to one (1) micron or more.

7. Remove said photoresist, preferably by an asher system in which plasma activated oxygen molecules effectively burn said photoresist away.

8. Deposit a layer of silicide forming metal, so that it is present atop the layer of gate forming metal deposited in Step 3 and atop the surface of said silicon opened in step 6, (note that said metal can be the same or a different metal than that deposited in step 3).

9. Process, (typically but not necessarily by an elevated temperature anneal), the resulting substrate so that rectifying Schottky barrier junctions are simultaneously formed between said

layer of silicide forming metal and said silicon with which said layer of silicide forming metal is in contact, in both N and P-type Source and Drain silicon regions. It has been found experimentally that a four-hundred (400) to five-hundred (500) degree centigrade, thirty (30) minute vacuum anneal, works well when Chromium is the Schottky barrier rectifying junction forming silicide forming metal deposited in step 8. Again, said example is not to be considered limiting of the invention.

10. Perform an etch to remove the any remaining silicide forming metal deposited in Step 8, which did not form a silicide. This removes all such silicide forming metal from the edges of the Silicon Dioxide which was etched in Step 6. The layer of gate forming metal deposited in Step 3 remains atop the gate silicon dioxide, thereby providing a delineated (MOSFET) structure.

A variation of the above device system, which does not require the presence of a checkerboard alternate doping pattern, requires but a few additional processing steps to achieve, provides a present invention preferred, embodiment, (ie. a single device equivalent to (CMOS), or alternatively described, a single MOS device with operating characteristics similar to multiple device (CMOS) diffused junction systems). To form a single device equivalent to (CMOS) an additional etch through the gate forming metal and silicon dioxide, or a functionally equivalent device geometry providing approach, can be performed to provide "mid-point" access to the channel region. It can be appreciated that if a (MOSFET) device system formed on a doped semiconductor has a voltage applied between the Schottky barrier junctions thereof, one Schottky barrier will be forward, and one reverse biased. If an inverted channel is caused to form in the (MOSFET) structure surface channel region by application of an appropriate voltage to the gate of said device, the forward

biased Schottky barrier junction will become reverse biased, and the reverse biased Schottky barrier junction forward biased, in said channel region. This causes the voltage present in the channel region to vary essentially between that applied to the Schottky barrier junctions. That is, essentially the voltage applied to a forward biased Schottky barrier junction will appear at a channel accessing region. When this is done, unless the channel accessing region is small in size dimension so that a gate voltage effected fringing field effectively inverts the opened region, the channel accessing region silicon might be doped, (possible with N and P-type regions), to a depth of approximately one-hundred (100) Angstroms into the substrate so that reverse bias leakage current is increased, or so that a forward biased path exists regardless of semiconductor channel region doping type. This can be accomplished by additional processing steps prior to deposition of aluminum in the second fabrication procedure described above. It is possible, to avoid this complication, to form such a single device equivalent to (CMOS) using intrinsic semiconductor, in which applied gate voltage only controls the effective doping in a channel region, and the forward/reverse bias state of two Schottky barrier junctions, situated in reverse back to back order as in the (MOSFET) described above. Such devices fabricated on intrinsic silicon tested have been found to be operable by the Inventor/Applicant. A particularly surprising result was discovered in devices formed on intrinsic silicon. That being that application of drain to source voltage, without a like polarity gate to source voltage being applied, causes no mid-point channel accessing voltage to appear. It is also mentioned, and is better described in the Detailed Description Section of this Disclosure, that the single device equivalent to (CMOS) fabrication procedure described supra provides an non-inverting embodiment. That is application of a gate voltage effects a voltage at channel accessing region to increase. An

inverting version of the single device equivalent to (CMOS) is realized by causing the channel accessing region to have rectifying Schottky Barrier junctions present, rather than non-rectifying, and the source and drain regions to have non-rectifying junctions thereto rather than rectifying Schottky barrier junctions. This is better described in the Detailed Description Section of this Disclosure.

It is also mentioned that the voltage which appears at the mid-point channel accessing region is a result of applied drain to source and gate to source voltages. As a result the described devices can be utilized as modulators.

In addition, it is disclosed that if no voltage is applied to the drain, (or the drain is electrically interconnected with the source), but a voltage is applied to the non-rectifying contact at the mid-point channel accessing region with respect to said source, such that the Schottky barrier source is reverse biased then only a small reverse bias leakage current will flow through said Schottky barrier source, (and possibly drain if it is electrically interconnected to the source), junction. However, if a gate voltage induced inverted semiconductor channel region is caused to form, a forward biased current can flow through the source (and possibly drain). Configured as such, the device is a voltage controlled switch, functionally similar to a Silicon Controlled Rectifier (SCR) which does not latch. That is, said voltage controlled switch is turned on and off by simultaneous application of gate voltage. Said device can also be operated as a gate voltage controlled direction of rectification device. That is, it will conduct forward biased in one direction when the semiconductor is, under the control of an applied gate voltage, caused to be effectively N-type and the opposite direction when the semiconductor is effectively P-type. Of course, the present invention systems can be achieved by other

than the example procedures.

It is also noted that a common problem in Schottky barrier (MOSFETS) is the presence of relatively high leakage current. A slightly modified approach to fabrication Schottky Barrier devices serves to provide devices in which the rectifying junction is present only at the facing ends of a semiconductor channel region. Said fabrication comprises:

1. Providing a silicon substrate;

2. Growing silicon dioxide atop the surface thereof;

3. Etching through said silicon dioxide and into said silicon, a pattern comprising a (MOSFET) Source and Drain separated by a semiconductorr channel region;

3a. Depositing a layer of silicon protecting material such as silicon nitride and etching a pattern therein such that it remains at the ends of the channel region in the silicon.

4. Growing a layer of insulating silicon dioxide atop the etched open silicon regions;

4a. Removing remaining silicon protective material to provide access to silicon at the ends of said silicon channel region and proceeding directly to Step 6.

5. Etching said layer of insulating silicon dioxide to open the silicon in the etched silicon regions only at positions adjacent to the Source and Drain at the ends of said channel region in said silicon;

6. Depositing a layer of silicide forming metal over the

resulting substrate surface, preferably by a non-line-of-sight approach such as sputtering;

7. Processing the resulting system so that Schottky barrier junctions form between the deposited silicide forming metal and the opened silicon in the Source and Drain regions at the facing ends of said channel in the silicon;

8. Etching away remaining unreacted silicide forming metal;

9. Depositing conductor metal over the resulting substrate surface, (eg. aluminum); and

10. Etching said conductor metal to form isolated Source, Drain and Gate.

An additional etch through the gate and silicon dioxide in the channel region can also be performed to provide a single device equivalent to (CMOS) and voltage controlled switch/direction of rectification device structure as described infra.

Steps 3a. and 4a identify an alternative, and actually preferred, approach which can be utilized to effect Schottky barrier junctions at the ends of a semiconductor channel region, by depositing silicon protective material, (eg. silicon nitride), and etching patterns therein to allow silicon dioxide growth except at the ends of a channel region, then removing the silicon protecting material with non-silicon dioxide etching means. This can serve to protect the shape of an undercut silicon dioxide where a silicon dioxide etch to open silicon channel ends, (as in Step 5. above), would alter such.

The above devices are better described in the Detailed

Description Section of this Disclosure in conjunction with the Drawings.

Metals other than chromium and aluminum can also be utilized, but care must be exercised to assure that said metal does not adversely interact with a present insulating material. For instance, vanadium, titanium, niobium, and zirconium are reported to adversely react with silicon dioxide whereas chromium, molybdenum and tungsten do not. In particular, aluminum is a very safe metal to use as gate metalization material and is preferred. (Note that a preferred Chromium etchant comprising a mixture of cerric ammonium nitrate, (eight (8) grams), and perchloric acid, (three (3) milliliters), in deionized water, (forty (40) milliliters), does not noticeably attack Aluminum for many hours after contact therewith, thereby making Aluminum particularly attractive). As well, Aluminum easily withstands a five-hundred (500) degree centigrade silicide forming anneal temperature procedure.

Continuing, Schottky barriers of similar barrier heights on N and P-type silicon are desirable and the Schottky barriers should be formed on N and P-type silicon simultaneously whether metal and/or metal-silicide is provided during a reasonable process, such as an elevated temperature anneal in the range of five-hundred, (500), degrees centigrade or less. As well, many metal-silicon reactions provide numerous phases, (eg. titanium, iron, cobalt, nickel, rubidium, lead, hafnium, iridium, and platinum), whereas vanadium, chromium, zirconium, niobium, molybdenum, tantalum and tungsten form only a single disilicide phase with silicon. As thin film silicide formation driving forces are not well understood at the present time, a single phase formation is desirable as it reduces complications during a fabrication procedure.

Chromium-disilicide provides a documented Schottky barrier height on N-type silicon of 0.57 ev with an apparently essentially balanced similar barrier height on P-type silicon. Similar results are reported in the literature where Molibdinum Disilicide, Vanadium Disilicide Vanadium and Titanium Disilicide are present. Dipaladium silicide provides 0.75 ev on N-type silicon. Diplatinum silicide, provides 0.79 ev and Platinum silicide 0.88 ev, again on N-type silicon. Platinum Silicide provides 0.24 ev on P-type silicon. Elements which form silicides with Schottky barrier heights on N-type silicon similar to that of chromium are molybdenum with molybdenum disilicide providing 0.55 ev, tantalum with tantalum disilicide providing 0.59 ev, titanium with titanium disilicide providing 0.61 ev and zirconium with zirconium disilicide providing 0.55 ev. Cobalt silicide and cobalt disilicide each provide 0.65 ev. Eridium disilicide and gadnium disilicide each provide 0.38 ev. Rhubideum silicide provides 0.69 ev and tungsten disilicide provides 0.65 ev.

In view of the above, and in view of the fact that molybdenum is known to have a temperature expansion coefficient similar to that of silicon, molybdenum, as well as chromium, is a particularly suitable metal for use in realizing the present invention. Tungsten is also be particularly suitable, although its Schottky barrier height on N-type silicon might be a bit high.

It is also to be noted that transition metal-silicide formation is generally uniform, but that yittrium, rhubideum, paladium iridium and hafnium do not provide uniform silicide layers. It is believed that silicide formation is nucleation controlled and that this leads to interfacial nonuniformities which are more severe than for non-nucleation controlled transition metal silicide formation, (that is for diffusion or

reaction controlled metal silicide formation).

Other considerations involve compatability of a Schottky barrier metal or metal-silicide with aluminum which is typically used as interconnecting trace metal in integrated circuits. For instance it has been reported that when aluminum in contact with platinum or paladium is annealed at two-hundred-twenty-five (225) and two-hundred-fifty (250) degrees centigrade respectively, voids and thickenings are observed. Said effect is reported to be less pronounced when tantalum, chromium, molybdenum and cobalt are used. (See Colgan, "Aluminum-Transition Metal Thin Film Reactions", Ph.D. thesis, Cornell, 1987 and J. Appl. Phys., 62(4), 1224, 1987). It is noted that the information provided above regarding silicides was gleened primarily from the book titled "Electronic Materials Science", by Mayer & Lau, MacMillan Publishing, 1990.

It is further disclosed that the source or drain of a Schottky barrier (MOSFET) device fabricated on P-type or N-type semiconductor can be electrically connected to the source or drain of a second (MOSFET) fabricated on P-type or N-type semiconductor to form a (MOSFET) transistor with a (MOSFET) load and seriesed (MOSFETS). In addition, the sources of two (MOSFET) devices formed on P-type (or N-type) semiconductor can be electrically connected to one another to form balanced differential (MOSFET) systems such as are present in differential amplifiers. In addition, certain Schottky barriers can be caused to form on relatively highly doped regions of semiconductor, thereby effecting essentially non-rectifying junctions. As mentioned above, the present invention enables fabrication of single device equivalents to (CMOS) and voltage controlled switches. All such Schottky barrier (MOSFET) device systems are to be considered within the scope of the present invention.

The present invention will be better understood by reference to the Detailed Description Section of this Disclosure in conjunction with the accompanying Drawings.

SUMMARY OF THE INVENTION

Conventional Metal Oxide Semiconductor Field Effect Transistors (MOSFETS) are well known. Fabrication thereof utilizes diffused junction technology to create required rectifying junctions at the ends of a substrate surface channel region in a semiconductor substrate, and requires a relatively large number of fabrication steps. As each step in a fabrication procedure introduces defects to devices being fabricated, a process for fabricating (MOSFET) devices which requires a reduced number of fabrication steps provides utility. An alternative to diffused junction technology for creating rectifying junctions is that of Schottky barrier junction technology. The present invention teaches that Schottky barrier junction technology can be successfully applied to fabrication of rectifying junctions suitable for use in (MOSFETS). In addition, the present invention demonstrates that said Schottky barrier junction technology is applicable to simultaneous fabrication of (MOSFETS) on both N and P-type silicon when chromium is deposited thereupon and annealed thereto. The present invention thus teaches and demonstrates that Schottky barrier junction technology is applicable to the fabrication of Complimentary Metal Oxide Semiconductor Field Effect Transistor (CMOST) device systems, wherein N and P-channel (MOSFET) device drains are electrically interconnected to one another.

The present invention also teaches Schottky barrier (MOSFET) device systems comprised of Schottky barrier (MOSFETS) as described above, but in which two Schottky barrier (MOSFET) devices formed on N-type silicon, or two Schottky barrier (MOSFET) devices formed on P-type silicon have the source of one Schottky barrier (MOSFET) device electrically interconnected to the drain of the other, or have the sources of Schottky barrier

(MOSFET) devices electrically interconnected. Said device system configurations being Schottky barrier (MOSFET) transistor with a Schottky barrier (MOSFET) load and seriesed Schottky barrier (MOSFETS), or balanced differential Schottky barrier (MOSFET) systems respectively.

As well, and significantly, the present invention teaches the application of essentially non-rectifying as well as rectifying Schottky barrier junctions in (MOS) based non-inverting and inverting single (MOS) devices, fabricated on a single semiconductor type, which single (MOS) devices provide operating characteristics similar to multiple device (CMOS) systems. Said single (MOS) devices can also be configured as voltage controlled switches with operating characteristics similar to a non-latching Silicon Controlled Rectifier (SCR). Said devices can also be operated as modulators with an output voltage being dependent on both applied drain to source and gate to source voltages, and as gate voltage controlled direction of rectification devices.

The present invention also teaches the use of intrinsic silicon in realization of single inverting and non-inverting devices with operating characteristics similar to multiple device (CMOS) systems.

Low leakage current structure devices are achieved by use of an insulating material which serves to limit the surface area of Schottky barrier junctions to just that necessary to provide current to a semiconductor channel region, at the ends thereof.

It is therefore a purpose of the present invention to teach a Schottky barrier (CMOS) device system comprising two metal-N-type and/or metal-silicide-N-type semiconductor rectifying junctions separated by a first channel region, in

functional combination with two metal-P-type and/or metal-silicide-P-type semiconductor rectifying junctions separated by a second channel region.

It is another a purpose of the present invention to teach a Schottky barrier (MOSFET) device system comprising two metal-N-type and/or metal-silicide-N-type semiconductor rectifying junctions separated by a first channel region, in functional combination with two metal-N-type and/or metal-silicide-N-type semiconductor rectifying junctions separated by a second channel region.

It is yet another a purpose of the present invention to teach a Schottky barrier (MOSFET) device system comprising two metal-P-type and/or metal-silicide-P-type semiconductor rectifying junctions separated by a first channel region, in functional combination with two metal-P-type and/or metal-silicide-P-type semiconductor rectifying junctions separated by a second channel region.

It is yet still another purpose to teach a single device Schottky barrier (MOS) system, fabricated on a single type semiconductor substrate, which provides operating characteristics similar to multiple device (CMOS) systems fabricated on multiple semiconductor types.

It is still yet another purpose to teach that a single device Schottky barrier (MOS) system, fabricated on a single type semiconductor, which provides operating characteristics similar to multiple device (CMOS) systems, and which can be operated as a modultor.

It is a further purpose of the present invention to teach a Schottky barrier (MOS) voltage controled switch, fabricated on a

single type semiconductor, which provides operating characteristics similar to a non-latching Silicon Controlled Rectifier (SCR) and can be operated as a gate voltage controlled direction of rectification device.

It is yet a further purpose of the present invention to teach suitable fabrication procedures for Schottky barrier (MOS) device systems, which fabrication procedures require a lessor number of defect introducing fabrication steps, as compared to fabrication schemes utilizing diffused junction technology.

It still yet a further purpose of the present invention to teach the use of intrinsic silicon in reailzation of single inverting and non-inverting devices, fabricated on a single type semiconductor, which single inverting and non-inverting devices demonstrate characteristics similar to multiple device (CMOS) systems and can be operated as a modulator, a nonlatching (SCR) and/or a gate voltage controlled direction of rectification device.

It is another purpose of the present invention to disclose experimentally obtained results which demonstrate operational characteristics of Schottky barrier technology derived (MOSFET) devices fabricated by a disclosed fabrication procedure.

It is yet another purpose of the present invention to teach a low leakage current Schottky barrier (MOSFET) device structure which provides Schottky barrier junctions only at the ends of a semiconductor channel region, and a fabrication procedure for realization thereof.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1(a) shows a top view of a conventional (MOSFET).

Fig. 1(b) shows a side cross-sectional view of a conventional (MOSFET) taken at a-a in Fig. 1(a).

Fig. 2(a) shows a top view of a conventional (CMOS) device system.

Fig. 2(b) shows a side cross-sectional view of a conventional (CMOS) device system taken at b-b in Fig. 2(a).

Fig. 3 shows a side cross-sectional view of a Schottky barrier (MOSFET) device system of the present invention.

Fig. 4 shows a side cross-sectional view of a modified Schottky barrier (MOSFET) device system of the present invention.

Fig. 5 demonstrates the formation of a metal-silicide when a metal which has been deposited upon a semiconductor substrate is annealed.

Fig. 6. shows (MOSFET) drain-current vs. drain-to-source voltage curves, as a function of gate-to-source voltage, provided by a device formed on P-type silicon wherein chromium was deposited in drain and source regions and annealed thereto.

Fig. 7. shows (MOSFET) drain-current vs. drain-to-source voltage curves, as a function of gate-to-source voltage, provided by a device formed on N-type silicon wherein chromium was deposited in drain and source regions and annealed thereto.

Fig. 8 shows (CMOS) curves such as provided by a seriesed

combination of (MOSFET) devices, which provide drain-current vs. drain-to-source voltage curves as demonstrated in Figs. 6 and 7.

Figs. 9(a) through 9(j) show a silicon substrate at various stages of fabrication of (MOSFET) devices using a preferred fabrication process.

Figs 9(k) through 9(m) show structures similar to those shown in Figs. 3 and 4, but fabricated by the preferred fabrication method demonstrated by Figs. 9(a) through 9(k).

Figs. 10(a) through 10(i) show steps in fabrication of a non-inverting single device equivalent to (CMOS), and Figs. 10(j) through 10(r) show steps in fabrication of an inverting single device equivalent to (CMOS).

Figs. 11(ao) through 11(go), 11(a1) through 11(g1), 11(a2) through 11(g2p), and 11(a3) through 11(g3) show fabrication steps utilized in arriving at a low leakage Schottky barrier junction.

Figs. 11(ha), 11(hb), 11(i), 11(j) and 11(k) show various (MOSFET) geometries incorporating low leakage current Schottky barrier junctions.

Figs. 11(l), 11(m), 11(n) and 11(o) show various geometries for single device equivalents to (CMOS) incorporating low leakage current Schottky barrier junctions.

Figs. 12(a) and 12(b) show circuit symbols for conventional diffused junction P-Channel and N-Channel (MOSFETS).

Figs. 13(a) and 13(b) show circuit symbol representations for conventional diffused junction and for Schottky barrier (MOSFET) (CMOS) systems.

Fig. 14 shows circuit symbols for a balanced pair of Schottky barrier (MOSFETS) such as can be used in operational amplifiers.

Figs. 15(a) and 15(b) show active Schottky barrier (MOSFETS) with (MOSFET) loads. Active devices are shown as N-Channel but P-Channel (MOSFETS) could also be used.

DETAILED DESCRIPTION

Turning now to the Drawings, there is shown in Figs. 1a and 1b a conventional diffused junction silicon substrate (MOSFET) (1). Shown are a silicon substrate (4) of N or P-type doping with oppositely doped diffused source (2) and drain (3) regions present therein. Shown as well are gate (5) and gate pad (5a), with silicon dioxide (16) present between said gate (5) and a semiconductor channel region thereunder between said source (2) and drain (3). Figs. 2a and 2b show a (CMOS) device system (10) comprising a substrate with regions of N (11) and P-type (12) doping. Diffused source (2a) and (3b) and diffused drain (3a) and (2b) regions, of opposite type doping with respect to the type of substrate respectively with which they are associated, are shown on each of the N (11) and P-type (12) regions. Also shown are gates (6) and (7) and gate pads (6a) and (7a). During use gates (6) and (7) can be electrically interconnected, and drain (3a) can be electrically interconnected to drain (2b). Source (2a) can be connected to an external positive voltage (+Vdd) and source (3b) connected to external voltage (-Vss) which is typically ground. When a relatively low gate voltage is simultaneously applied to the electrically interconnected gates (6) and (7) the P-channel (MOSFET) on the N-type silicon (11) will have an inverted P-type channel region formed between its source (2a) and drain (3a), hence will provide a reduced resistivity therebetween. The (MOSFET) on the P-type (12) silicon will have an accumulated channel region and will continue to demonstrate a high resistivity. (Note that as used herein the term "inversion" means that a gate induced electric field causes silicon type to reverse in a channel region and the term "accumulation" means that a gate induced electric field causes a silicon type to become more so said type, (eg. N or P-type) in a channel

region). The voltage applied to the source (2a) will therefore appear at the electrical connection between drain (3a) and drain (2b). It should be appreciated that application of a relatively high gate voltage, (eg. approximately Vdd), will cause the voltage applied to the source (3b) to appear at the electrical connection point between drain (3a) and drain (2b). That is, a low resistivity inverted channel will form in the N-channel device formed on the P-type (12) silicon while the P-channel device formed on the N-type (11) silicon will demonstrate accumulated channel high drain (3a) to source (2a) resistivity. As the gate oxide is of a high resistance, (eg. ten-to-the-forteenth ohms), little gate current is required to switch the identified voltage at the electrical connection between drain (3a) and drain (2b). Also, as one of the devices is nearly always off during operation, except momentarily at the point of switching, very little source (2a) to source (3b) current flows. It should then be appreciated that the (CMOS) device system is very energy efficient. (CMOS) devices systems then allow applied gate voltage control of the voltage present at an essentially electrically isolated terminal.

Turning now to Fig. 3, there is shown a (CMOS) device system appropriate to the present invention. Both N (11) and P-type (12) doped regions are shown in a silicon substrate. Shown also are silicon dioxide (16), gates (15a) and (15b), sources (2a) and (3b) and drains (2b) and (3a) with metal (15) present, said metal (15) being discontinuous between that atop the silicon dioxide (16) and atop the N-type (11) and P-type (12) silicon. The gates (15a) and (15b) are shown electrically interconnected as are drain (2b) and drain (3a). Fig. 5 demonstrates that an anneal of metal (15) in contact with silicon can cause formation of a silicide (15s) at the metal-silicon interface or otherwise effects a Schottky barrier rectifying junction, between said metal (15) and said silicon.

This is the case whether the silicon is N (11) or P-type (12), when for instance, the metal is chromium or molybdinum. Fig. 5 demonstrates that a Schottky barrier is comprised of semiconductor and nonsemiconductor components.

Also, though not explicitly shown it is to be understood that said silicide can form laterally, into a channel region under a gate (15a) (15b), as well as vertically into a semiconductor substrate.

It should be appreciated that deposition of metal (15) upon a substrate etched as demonstrated in Fig. 3 can provide a self delineated (CMOS) device system if the metal deposited is not too thick and deposited by a line-of-sight technique, and it forms a silicide with silicon when annealed thereto. Fig. 4 shows a variation in which the oxide is removed between drain (2b) and drain (3a) providing immediate electrical interconnection therebetween.

The drain-current vs. drain-to-source-voltage operational curves of N-Channel and P-Channel, respectively, devices as shown in Figs. 6 and 7 are similar to those of normal (MOSFETS), with the exception that drain current flows in a direction opposite to that in conventional (MOSFETS). (Note that the parameter analyzer provides output data indicating the drain voltage as negative or positive with respect to the source, which is held at ground potential. However, as the tested Schottky Barrier (MOSFETS) are geometrically symetrical with regard to the drain and source relation to the gate, (see Figs. 1-4 to appreciate such symetry), the devices will work just as well if the source is biased with respect to a common point drain). Insight as to how said Schottky barrier (MOSFETS) might operate is provided in the Lepselter and Sze paper referenced in the Background Section. Briefly, said article considers that the source region junction of a P-channel device formed on

N-type silicon, using platinum as the metalization, is reverse biased during operation and that it is reverse leakage or tunneling current which is modulated by the applied gate voltage. This article states that it was the source which was reverse biased during operation. In addition, with respect to Fig. 13b herein, which shows a Schottky barrier (MOSFET) (CMOS) configuration, it will be appreciated that it is the source of N-Channel and P-Channel devices which are reverse biased during operation. Designation of source and drain are then, dependent upon position within a circuit.

Reference to Figs. 6 and 7 show that N and P-channel (MOSFET) devices fabricated on P and N-type silicon respectively by the inventor herein, using eight-hundred (800) angstroms of chromium as the metalization, which chromium was simultaneously vacuum deposited on both N (11) and P-type (12) silicon and then simultaneously vacuum annealed to said N (11) and P-type (12) silicon at four-hundred (400) degrees centigrade for thirty (30) minutes, provide (MOSFET)-type operational drain-current vs. drain-to-source voltage curves as a function of gate-to-source voltage. It is also disclosed that tested devices had a gate length and width of approximately ten (10) microns and seventy-five (75) microns respectively. It is noted that Fig. 6 drain-current vs. drain-to-source voltage curves for (MOSFET) devices, (as a function of gate-to-source volts), fabricated on P-type silicon (12) are in the third quadrant and the Fig. 7 drain-current vs. drain-to-source voltage curves for devices, (as a function of gate-to-source volts), fabricated on N-type (11) silicon are in the first quadrant. This is what would be expected by reference to the Lepselter et al. article. However it is noted that the present devices operate with the drain junction in each device reverse biased rather than the source junction, as is what the Lepselter and Sze article states was the case with their devices. This is an artifact of the

parameter analyzer system utilized, (eg. a Hewlett-Packard 4145B system) used to obtain curves in Figs. 6 and 7 and it is noted that the P-Channel device curves shown in the Lepselter et al. paper operate with the same polarities on Drain and Source as do the present invention P-Channel devices, (ie. those formed on N-Type substrate). It is noted and emphasized that the drain-current vs. drain-to-source voltage curves in Figs. 6 & 7 are quite complimentary and nearly symetrical. These attributes are substrate doping dependent, (which doping levels were approximately equal at ten-to-the-fifteenth-per-cm-cubed) for the presently discussed Fig. 6 and 7 represented N-Channel and P-Channel devices), which makes the devices which provided said drain-current vs. drain-to-source voltage curves quite appropriate for application in combined (CMOS) device systems. It is also noted that devices formed on both N (11) and P-type (12) silicon show a small drain current with zero (0.0) gate-to-source volts applied. This can be the result of "leaky" silicon dioxide or a function of substrate doping. That is, the zero (0.0) gate-to-source voltage drain current flow might be through the gate circuit or through the source circuit. In the former case a leaky oxide is the cause, and in the later a reverse bias Schottky barrier leakage or tunneling current is the cause. Superior oxide and varying substrate metalurgical doping levels can serve to adjust said current flow at zero (0.0) applied gate-to-source voltage drain current flow. Note that application of gate voltages of opposite polarities to those which serve to increase drain current flow serve to reduce said drain currents to essentially zero in the respective (MOSFET) devices formed on N and P-type silicon respectively. This shows depletion mode device operation is possible, but that the tested devices are primarily enhancement mode devices. (Note that "enhancement means that increasing the absolute value of gate voltage causes an increase in drain current. Depletion mode means that an increase in the absolute value of gate

voltage causes a decrease in drain current). It is also reported that the onset of drain current conduction in present fabricated tested N-Channel Schottky barrier (MOSFET) devices has been found to correlate very well with Capacitance-Voltage (CV) plot onset of channel inversion, (which occurs at approximately minus (-4.0) volts in N-Channel devices, leading to the proposal that positive ions in the oxide may account for a shifted threshold of conduction and the presence of zero (0.0) gate-to-source volts drain current flow rather than poor oxide or gate uninfluenced drain current flow. This would not explain a similar result in the presently fabricated and tested P-Channel devices however.

Continuing, of importance is the fact that (CMOS) operation can be effected by application of appropriate gate-to-source voltages because said current levels are small, essentially balanced and eliminated in each (MOSFET) device by application of a gate voltage which serves to increase the conductivity of the other present (CMOS) (MOSFET) device. In particular though, the present invention is not to be considered dependent on the presence of said zero (0.0) applied gate-to-source voltage, drain-to-source current flow shown in Figs. 6 and 7. See Figs. 8 and 13, and accompanying discussion for insight to (CMOS) operation.

Coupling drain (2b) and drain (3a) as described above to form a (CMOS) device system, and sequentially, but simultaneously, applying varying values of gate-to-source voltage to coupled gates (15a) and (15b) provides (CMOS) device system operational curves such as shown in Fig. 8. (See Fig. 13b for a circuit symbol representation thereof). Fig. 8 shows the voltage (Vm), (ie. voltage present at the electrical interconnection connection point of drain (2b) and drain (3a), switches between, essentially, that (Vss) applied to source (2a)

and that (-Vdd) applied to source (3b) by external circuitry, when the gate voltage applied simultaneously to electrically interconnected device gates (15a) and (15b) is varied. (See discussion of Fig. 13a (supra) for insight as to conventional diffused junction (CMOS) system operation and of Fig. 13b (supra) for additional insight to operation of Schottky barrier (CMOS) system operation).

It is also possible to form a series combination of two, (N-channel or P-channel), (MOSFETS) to form transistor-load device systems or balanced differential (MOSFET) transistor pair systems. Such configurations can be N-channel device and N-channel load, P-channel device and P-channel load, N-channel device and P-channel load and P-channel device and N-channel load, (See Figs. 15(a) and 15(b) and 14 for circuit symbol representations). In a transistor-load device system the source of one device is electrically interconnected to a drain of another and the gate of the load device is typically electrically interconnected to lead on the load device not connected to the transistor. The gates of the transistor and load are not electrically interconnected and during use a voltage input signal is applied between the free transistor gate and its source, while a load voltage is applied between the electrically interconnected load gate and the lead on the load transistor not electrically interconnected with the transistor, and the source of the transistor. In a balanced differential (MOSFET) transistor pair system the sources of two (MOSFETS) devices are electrically interconnected and the gates of the so interconnected devices are not directly electrically interconnected, but rather attach across a source of voltage. Each (MOSFET) drain is also attached to a source of voltage which is referenced to the electrically interconnected sources, normally through a load, and application of a voltage difference between the gates of the two (MOSFET) devices effects a current

flow through the drains. It should be appreciated that only the voltage difference between said gates has an effect on current through said balanced differential pair system drains. That is, common-mode voltage applied to both gates has no significant effect on current flow through the device system (MOSFET) drains. The present invention should be considered to include such configurations as the distinction therein is the type of silicon upon which two simultaneously fabricated electrically interconnected devices are formed. That is, instead of electrically interconnecting (MOSFET) devices formed on N and P-type silicon, two devices formed on N-type, or two devices formed on P-type, silicon are electrically interconnected. Referring to Figs. 3 and 4, this would correspond to interpreting both semiconductor regions (11) and (12) to be of one type, (ie. N or P-type) to demonstrate a (MOSFET) with a (MOSFET) load, along with, typically, considering the shown common gate electrical connection as broken, and with an electrical connection added between the load device drain and gate, perhaps through a resistor. A simple seriesed (MOSFET) configuration is realized by electrically connecting a rectifying junction drain (2b) of one (MOSFET) to a rectifying junction source (3a) of another. As well, simply considering rectifying junctions (2b) and (3a) to be electrically connected sources and (2a) and (3b) to represent drains of devices formed in semiconductor regions (11) and (12) in Figs. 3 and 4, provides pictorial representation of the balanced differential (MOSFET) pair configuration. As mentioned above, in such a balanced differential (MOSFET) pair system the gates of the devices are not electrically interconnected and the shown electrical interconnection would be broken so that a voltage difference could be applied therebetween.

It is of particular importance that if semiconductor regions (11) and (12) in Fig. 4 are considered to be of the same

doping type, (ie. N or P or intrinsic), and metal (15) or a silicide in regions (2a) and (3b), provides rectifying junctions on said semiconductor (11) and (12), then applying gate volts (Vg) simultaneously to gates (15a) and (15b) can effect a single substrate type, (ie. single device), equivalent to (CMOS). For instance, if semiconductor regions (11) and (12) are both N-type and a positive value of (Vdd) is applied to the rectifying junction at (3b) while a less positive voltage (Vss) is applied to rectifying junction (2a), then said applied voltages (Vdd) and (Vss) will cause the rectifying junction at (3b) to be forward biased and the rectifying junction at (2a) to be reverse biased. Application of a negative gate voltage to gates (15a) and (15b) just sufficient to cause onset of inverted channel regions thereunder in the semiconductor, in effect causes the rectifying junction at (3b) to become reverse biased and the rectifying junction at (2a) to become forward biased at said channel regions. That is, the reverse and forward biased rectifying junction positions are switched. It will be appreciated that if said forward biased rectifying junctions are not required or allowed to carry much current flow, which is effected by limiting the magnitude of the applied gate voltage and external loading connected at (2b) and (3a), the end effect will be to cause the voltage (Vm), as identified in Fig. 4, to shift between (Vdd) and (Vss). It is pointed out that it is preferable to effect an essentially non-rectifying contact for sensing (Vm) at (2b) and (3a). That is, the use of a different metal and/or silicide might be preferable in semiconductor regions (2b) and (3a) as compared to that utilized in semiconductor regions (2a) and (3b), said different metal and/or silicide serving to form non-rectifying rather than rectifying junctions with the semiconductor substrate at (2b) and (3a). The Semiconductor substrate (11) and (12) can also, or in the alternative, be caused to be of a doping level at (2b) and (3a) by diffusion or ion implantation for instance, so as to cause an

effectively non-rectifying junction at (2b) and (3a) using the same metal and/or silicide that forms Schottky barrier rectifying junctions at (2a) and (3b). (Note that metal-semiconductor and metal-silicide-semiconductor junctions wherein the semiconductor is relatively highly doped, (eg. typically ten-to-the-eighteenth-per-centimeter-cubed and higher), often demonstrate essentially non-rectifying current-voltage characteristics). As well, while introducing a high resistance region, use of a compensated essentially intrinsic semiconductor at the (2b) and (3a) regions can provide non-rectifying contacts to a metal deposited thereon, and will not form undesired rectifying junctions with adjacent regions of semiconductor which are doped metalurgically or by application of a gate voltage. In fact, the entire substrate can be intrinsic with N and P-type doping effected completely by applied gate voltages. This avoids the problem which can develop wherein a channel region accessing opening in a gate is sufficiently large that inverting channel voltage applied thereto can not serve to invert the channel region within the opening, thereby causing a rectifying junction between a doped semiconductor inverted channel and said channel accessing region. Where channel accessing regions are sufficiently small, this will not occur even in a doped semiconductor, and in fact reverse leakage current through such a rectifying junction, where it does exist, can make said semiconductor compensation unnecessary.

The single device equivalent to (CMOS) just discussed demonstrates non-inverting characteristics. That is, an increased gate voltage causes an increased mid-point channel accessing region voltage (Vm). Conventional diffused junction (CMOS) does not provide such a noninverting device without more than one (CMOS) device system present in series. As will be discussed supra, it is also possible to provide alternative

device geometry which demonstrates inverting characteristics by placing the Schottky barrier rectifying junctions at the mid-point channel accessing region, and ohmic junctions at the source and drain.

It will be appreciated that an equivalent single device (CMOS) system can also be effected on P-type semiconductor, wherein opposite polarity applied voltages (Vdd), (Vss) and (Vg) are utilized. In both cases, the required substrate is of one type doping only. That is, formation of a checkerboard of alternating N and P-type doping regions is not required. emphasis added. The appropriate Claims are, in particular, to be interpreted to cover such single device equivalents to (CMOS). It is also specifically noted that the electrically interconnected non-rectifying junctions in the (CMOS) type devices of the Honma et al. Patent cited in the Background Section herein are from opposite type semiconductor. The present invention device electrically interconnected non-rectifying junctions are on the same type material, emphasis added. It is also noted that non-rectifying junctions are easily achieved between aluminum and P-type silicon.

The present invention then can include devices in which Schottky barriers which are made essentially non-rectifying are present. It should also be understood that said Schottky barrier junctions which are made essentially non-rectifying do not have to be electrically interconnected, but could be represented by junctions (2a) and (3b), with junctions (2b) and (3a) being rectifying. This configuration on a single type substrate would, for instance, provide a balanced differential (MOSFET) pair in which, during operation, junctions (2b) and (3a) could be reverse biased and in which leakage current therethrough is controlled by application of appropriate semiconductor conductivity modulating gate voltages.

A voltage controlled switch can be configured from a (MOSFET) which has a rectifying Schottky barrier source junction, a non-rectifying drain junction, and a channel region therebetween, which channel region has an insulator and gate sequentially positioned adjacent thereto such that application of a voltage to said gate effects semiconductor doping in said channel region. That is, applying a positive voltage to the gate will attract electrons to the channel region and application of a negative gate voltage will attract holes to the channel region. Application of a voltage drain to source, such that the source junction is reverse biased, leads to little current flow. That is, only reverse bias Schottky barrier source current flows. By then applying a voltage between gate to source such that an inverted channel region is formed, a forward biased current through said source Schottky barrier junction can be effected. Such a voltage controlled switch is functionally a bit like a non-latching Silicon Controlled Rectifier (SCR). That is, forward current flow through a Schottky barrier can be started, and stopped, simply by the application of and removal of, a gate to source voltage. No known reference discloses such a configuration and use of a (MOSFET) device as described. This can also control the "direction" of rectification. That is if the device is not conducting in one direction with one polarity of drain to source voltage applied, it would conduct if the drain to source voltage polarity were reversed. Application of gate voltage would then terminate said conduction. Gate voltage can be applied gate to substrate, with drain to source serving as a gate voltage controlled rectification direction device. For instance, without gate voltage applied the device would conduct drain to source, and with gate voltage applied conduct source to drain. Again, the Schottky barrier forms a rectifying junction with either N or P-type semiconductor and the gate voltage controls

the effective doping type in the semiconductor channel region.

Figs. 9(a) through 9(k) demonstrate a preferred (MOSFET) fabrication process, including steps for providing isolation of devices via provision of relatively thick silicon dioxide therebetween. Fig. 9(a) shows a side view of silicon substrate (90). Fig. 9(b) shows said silicon substrate (90) in side view with relatively thick layer of silicon dioxide (91) grown atop thereof. Fig. 9(c) shows, in side view, said relatively thick layer of silicon dioxide (91) etched to the silicon (90) surface in the center region thereof. (Many such regions would be formed an a substrate in production setting). Fig. 9(d) shows a side view of a relatively thin layer of silicon dioxide (92) grown in said center region. This relatively thin layer of silicon dioxide (92) is of a depth appropriate for use as a gate oxide in a (MOSFET), (eg. typically hundreds to thousands of Angstroms). Fig. 9(e) shows, in side view, the structure of Fig. 9(d) with a relatively thick layer of gate forming metal deposited thereover. Fig. 9(f) shows a top view of the structure shown in Fig. 9(e), with a photoresist (96) pattern atop the relatively thick layer of gate forming metal (93) atop said relatively thin layer of silicon dioxide (92). Shown are device drain (94) and source (95) regions separated by a gate oxide formed from said relatively thin layer of silicon dioxide (92). Fig. 9(g) shows the structure of Figs. 9(e) and 9(f) in which said relatively thick layer of gate forming metal (93) and the relatively thin layer of silicon dioxide (92) have been etched to expose the underlying silicon substrate, prior to removal of the photoresist (96). Note that while not shown, a silicon substrate etch can also be performed at this point and be within the scope of the present invention preferred fabrication method. Such a silicon etch would provide a structure appearing much as shown in Figs. 3 and 4. Fig. 9(h) shows the structure of Fig 9(g) with the photoresist (96)

removed and with a relatively thin layer of silicide forming metal (97) deposited thereover. Fig. 9(i) shows the structure of Fig. 9(h) after a silicide (98) forming anneal, and an etch which removes any remaining silicide forming metal (97). Note that the etchant is selected so as not to adversely effect the relatively thick layer of gate forming metal, but so that it serves to remove any remaining thin layer of device drain (94) to source (95) shorting silicide forming metal on the etched, gate insulator forming, sides of the relatively thin layer of silicon dioxide (92). This is the case even where the relatively thick layer of gate forming metal and the relatively thin layer of silicide forming metal are the same element. It has been found, however, that Aluminum is a good element for use as a relatively thick gate forming metal (93) and that Chromium is a good relatively thin layer of silicide forming metal (97) element for use on either N or P-type silicon. This is in part because a chromium etchant comprised of cerric ammonium nitrate, (eight (8) grams), and perchloric acid, (three (3) milliliters), in deionized water, (forty (40) milliliters), is effective in etching chromium but essentially ineffective in etching Aluminum, and in part because Aluminum adheres well to silicon dioxide after deposition in a sputtering chamber. Unless done with a substrate held at an elevated temperature, deposited Chromium on silicon dioxide does not always adher so well, with water necessary in subsequent processing steps serving to "crinkle" said Chromium off of said silicon dioxide. Fig. 9(j) shows the structure of Fig. 9(i) but with the relatively thick layer of gate forming metal (93), over the relatively thick layer of silicon dioxide (91), removed. An additional but simple photoresist procedure accomplishes this when desired. In fact, the same mask used to effect etching of the relatively thick layer of gate forming metal and silicon dioxide as represented in Fig. 9(c), can be used at this point, coupled with use of an opposite type photoresist, (eg. positive

photoresist instead of negative photoresist). The above sequence of Figures demonstrates a preferred method of fabricating the (MOSFET) devices of the present invention. Fig. 9(k) represents a structure as in Fig. 9(i), but in which the silicon substrate (90) is comprised of two different dopings, (90a) and (90b) within one (MOSFET) device region. Said two dopings (90a) and (90b) could be of the same type, or of opposite (eg. N and P-type), types. Fig. 9(l) shows two (MOSFETS) on one substrate, each fabricated entirely over a doping single level or type of silicon, (ie. (90c) and (90d). If the doping types (90c) and (90d) are of opposite type this represents a (CMOS) structure. Fig. 9(m) shows a structure in which junction regions from two adjoining (MOSFET) structures are merged. It is again mentioned that the type of, and level of, doping of a semiconductor substrate annealed to a metal to form a junction determine the electrical characteristics of said formed junction. Annealing chromium at approximately four (400) to five (500) hundred and above degrees centigrade to either N or P-type silicon, doped to levels below about ten-to-the-eighteenth per centimeter cubed, provide rectifying junctions on both silicon types. Annealing chromium to silicon of either type doped approximately ten-to-the-eighteenth and above per centimeter cubed, provides junctions with essentially non-rectifying characteristics. Hence, controlling the type and the level of doping of silicon to which chromium is annealed can provide junctions with a wide variety of electrical characteristics. Metals other than chromium can also be utilized. As described earlier in this Disclosure, this enables production of a variety of devices.

Next, Figs. 10(a) through 10(i) demonstrate a preferred fabrication procedure for a non-inverting single device equivalent to (CMOS), which is fabricated on a single substrate type. Note that only device forming steps are shown and it is

to be assumed that device separation can be provided similar to as shown in Figs. 9(a) - 9(d). Fig. 10(a) shows a side view of a silicon substrate (100). Fig. 10(b) shows silicon dioxide (102) grown atop said silicon substrate (100) and Fig. 10(c) shows a layer of gate forming metal (106) deposited atop said silicon dioxide (102). Fig. 10(d) shows a top view of source (104) and drain (105) openings are made to the silicon (100) through gate forming metal (106) and silicon dioxide (102). Fig. 10(e) shows a side view of the same openings shown in Fig. 10(e). Fig. 10(f) shows a layer of silicide forming metal (107) deposited over the silicon substrate (100). Fig. 10(g) shows the presence of silicide (108) formed after an anneal procedure which, when chromium is utilized can be four-hundred-fifty (450) degrees centigrade for thirty (30) minutes. Fig. 10(h) shows a top view of the substrate of Fig. 10(g) but with a channel accessing opening (110) also present, etched through the gate forming metal (106) and silicon dioxide (102). Fig. 10(i) shows a side view thereof taken at b--b in Fig. 10(h). Note that in said side view of Fig. 10(i) the structure is validly described as two (MOSFETS) with one Schottky barrier, (with non-rectifying characteristics), of each being electrically interconnected, very much as shown in Fig. 4. (Note, in Figs. 9(a) through 9(m) and Figs. 10(a) through 10(i) no etch is shown into semiconductor substrates (90) and (100) as are shown in Figs. 3, 4 and 5. Said semiconductor etch is optional. It is noted that the silicon substrate (100) can be intrinsic, N-type or P-type and that silicon channel region in opening (110) can be intrinsic or oppositely doped, even where the silicon substrate (100) is N or P-type. It is noted that opening (110) might be two openings, the silicon under one being heavily doped N-type and heavily doped P-type in the other to enhance non-rectifying contact to the silicon channel region in both the metalurgical and inverted state, however, such is typically unnecessary because leakage current through even a

reverse biased junction will allow a voltage to be monitored in the channel through a reverse biased junction. It is noted that testing of fabricated devices tends to verify this conclusion. Where the hole (110) is sufficiently small fringing of an electric field due to a voltage applied to the gate will serve to invert the silicon channel region even under the hole (110), and a junction between inverted and noninverted silicon in the silicon channel region under the hole (110) will not exist. It should be clear in view of the foregoing that single device equivalent to (CMOS) can be considered as two (MOSFETS) formed on the same type semiconductor, with non-rectifying drain junctions interconnected. At this point it is specifically pointed out that while the Honma et al. Patent, the closest known art and cited in the Background Section herein, shows a (CMOS) device system in which non-rectifying drain junctions are interconnected, said non-rectifying drain junctions are to N-type silicon in one device and to P-type silicon in the other of two electrically interconnected devices. That is, the (CMOS) structure presented requires the presence of both N and P-type silicon. This is an extremely important contrasting distinction regarding the present invention, in which only a single substrate type (ie. N-type, P-type or intrinsic), is required, emphasis added. That is, the costly steps associated with forming an alternating checkerboard of N and P-type regions in a substrate common to all known (CMOS) devices are not necessary.

Testing of non-inverting single device equivalents to (CMOS) on intrinsic silicon has surprisedly shown that application of a voltage from drain to source, without any gate voltage being applied, produces zero (0.0) volts at the mid-point channel accessing region, with respect to source. Applying a voltage gate to source of a polarity similar to that applied drain to source effects a voltage present at said

mid-point channel accessing region. This occurs whether drain and gate are both provided positive or negative polarity voltages with respect to source. This is consistent with the formation of a forward biased rectifying junction at the drain. However, application of a gate to source voltage of an opposite polarity to that applied drain to source effects no drain to source applied voltage present at the mid-point channel accessing region, with respect to the source. This is consistent with the formation of a reverse biased rectifying junction at the drain junction.

Continuing, Figs. 10(j) through 10(r) demonstrate a fabrication procedure for an inverting single device equivalent to (CMOS). The fabrication process is similar to that described above for a non-inverting single device equivalent to (CMOS) but the end result is configured so that silicide (108) is present in the silicon at the center opening (110) rather than in the equivalent source and drain regions (104) and (105). Also shown is a delineating guard-ring of silicide (108) around the device which serves to help reduce leakage currents. Fig. 10(j) shows a silicon substrate (100). Fig. 10(k) shows silicon dioxide (102) grown atop the silicon substrate (100). Fig. 10(l) shows gate forming metal (106) deposited atop said silicon dioxide (102). Fig. 10(m) shows center opening (110) etched through the gate forming metal (106) and silicon dioxide (102) to provide access to the silicon substrate (100) surface. Fig. 10(n) is a cross sectional view taken at c--c in Fig. 10(m). Fig. 10(o) shows a layer of silicide forming metal (107) deposited over the substrate of Fig. 10(n). An anneal then causes silicide (108) to form where the silicide forming metal (107) is in contact with the silicon substrate (100) at the mid-point (110) opening. Fig. 10(p) shows all remaining silicide forming metal (107) removed. Fig. 10(q) shows source and drain regions (104) and (105) opened to the silicon substrate (100) surface. Fig. 10(r)

is a cross sectional view taken at d--d in Fig. 10(q). It will be appreciated that there are actually two, first and second, channel regions present in this device because the Schottky barrier rectifying junction is situated between two non-rectifying, (ie conductive) junctions. The first and second channel regions are between drain (105) and mid-point (110), and between source (104) and mid-point (110) respectively. Note that the drain (105) to mid-point (110) silicide (108) can be effectively replaced by a resistor, but that such is not optimum as when the mid-point (110) silicide (108) to source (104) Schottky barrier junction is caused, by gate applied volts, to become forward biased, no reverse biased junction then exists to limit current flow drain (105) to source (104) to a reverse bias Schottky barrier junction level. For the purpose of Claim construction such a configuration is to be considered but a case of a Schottky barrier which demonstrates non-rectifying essentially ohmic characteristics as a result of semiconductor doping and the like.

A bit of reflection should make it clear that application of a gate voltage to the device of Fig. 10(i) is necessary to effect a rectifying Schottky barrier drain (105) to source (104) applied voltage, at an non-rectifying mid-point (110) location. Say for instance the silicon substrate (100) is P-type and positive voltage is applied to rectifying Schottky barrier drain (105) with respect to source (104). Said rectifying Schottky barrier drain (105) junction will be reverse biased, said rectifying Schottky barrier source junction (104) will be forward biased. As a result no voltage appears at mid-point (110). Application of a positive gate to source voltage will invert the silicon in the channel region to N-type, thereby causing the rectifying Schottky barrier mid-point drain and source junctions to become forward and reverse biased respectively, thereby effecting a voltage at non-rectifying

mid-point (110).

A constant polarity drain (105) to source (104) applied voltage present at rectifying Schottky barrier mid-point (110) in the device of Fig. 10(r) however, will be caused to be reduced by application of a gate to source (104) voltage. For instance if the silicon substrate (100) is P-type, application of a positive voltage at non-rectifying drain (105) will cause said applied positive voltage to appear through forward biased rectifying Schottky barrier mid-point (110) junction through non-rectifying drain (105) with no gate volts applied with respect to non-rectifying source (104), said positive volts appearing across reverse biased rectifying Schottky barrier mid-point (110) junctions to the source (104). Application of positive gate volts with respect to non-rectifying source (104) will invert the silicon in the channel regions and cause the rectifying Schottky barrier mid-point (110) junction to the non-rectifying drain (105) to become reverse biased, and the rectifying Schottky mid-point (110) barrier to the non-rectifying source (104) to become forward biased, thereby lowering said mid-point (110) voltage.

It is to be understood that while the non-inverting and inverting embodiments are shown with channel physically between two Schottky barrier junctions, and with Schottky barrier junctions physically between two non-rectifying junctions respectively, such is demonstrative and not limiting. For instance, the channel region in the non-inverting embodiment could be physically split into two parts which are electrically interconnected and the Midpoint Schottky barrier junctions in the inverting embodiment could be located non-centrally but electrically interconnected. This could occur, for instance, if two separate devices are involved or if physical layout on a single substrate is changed. Functionally equivalent

embodiments to any device or device system demonstrated in this Disclosure are within the scope of the present invention and appropriate Claims.

It is also mentioned that a voltage present at a mid-point channel accessing region or mid-point Schottky barrier in non-inverting and inverting single device equivalents to (CMOS) respectively depend upon two applied voltages, namely, upon an applied drain to source and an applied gate to source voltage. As a result, the inverting and non-inverting single device equivalents to (CMOS) can be used as modulators to provide an output at the mid-point which is, at least in some operating voltage ranges, proportional to the product of the two applied voltages.

Figs. 11(ao) - 11(go), 11(a1) - 11(g1), 11(a2) - 11(g2p) and 11(a3) - 11(g3), there are shown generally similar approaches to forming Schottky barrier junctions which can be incorporated into the Schottky barrier junction based systems demonstrated by Figs. 9(a) - 9(m) and Figs. 10(a) - 10(r). The reason for incorporating such is to limit the area of Schottky barrier junction to the minimum necessary to provide a channel region current, but minimize leakage current to a semiconductor substrate from a drain.

Figs. 11(ao), 11(a1), 11(a2), and 11(a3) show a silicon substrate (100), and Figs. 11(bo), 11(b1), 11(b2) and 11(b3) show a silicon dioxide grown (102) atop thereof. Fig. 11(c0) shows the substrate of Fig. 11(bo) with the silicon dioxide (102) and silicon (100) etched anisotropically and isotropically respectively. Said silicon is etched to an underlying insulating substrate (sub). Fig. 11(c1) is the substrate of Fig. 11(b1) with the silicon dioxide (102) and silicon (100) etched anisotropically and isotropically respectively. Figs.

11(c2) and 11(c3) show the substrates of Figs. 11(b2) and 11(b3) with both the silicon dioxide (102) and silicon (100) etched anisotropically. It should be understood that isotropic etching is commonly achieved by a wet acid technique, and that anisotropic etching is typically achieved by dry plasma techniques. Figs. 11(do) is Fig. 11(co) repeated to hold the place in the sequence alongside the other drawings. Figs. 11(d1), 11(d2) and 11(d3) show insulating silicon dioxide (102) grown and etched in the etched silicon (100) regions. Note that Fig. 11(c3p) shows a diffused region (100d) which can serve to effect an essentially non-rectifying junction rather than a Schottky barrier junction with a deposited silicide forming metal (107) as shown in Figs. 11(e0), 11(e1), 11(e2) and 11(e3). It is best to deposit said silicide forming metal by a non-line-of-sight technique such as sputtering, when an undercut surface silicon dioxide device geometry is present so that said silicide forming metal can be deflected to the source and drain ends of said silicon channel. This is in contrast to the line-of-sight deposition approach required in devices with geometries such as demonstrated in Figs. 3 and 4. After a silicide forming anneal (eg. 450 degrees centigrade for 30 minutes if chromium and silicon are utilized), all remaining silicide forming metal (107) is removed by an etching procedure, leaving silicide regions (108) in place, as shown in Figs. 11(fo), 11(f1), 11(f2) and 11(f3). It is to be appreciated that the silicide (108) regions are present only adjacent to the ends of channel regions, thus the leakage currents, being proportionate to junction area, are reduced to essentially a minimum, emphasis added. Figs. 11(go), 11(g1), 11(g2) and 11(g3) show conductor metal (103), (eg. typically aluminum), applied and etched to provide contact to the Schottky barrier junction regions (108), and to provide gate metalization. Note that Fig. 11(g3p) shows a variation wherein the silicon dioxide (102) covers even more of the etched silicon (100) region.

Figs. 11(ha), 11(hb), 11(i), 11(j) and 11(k) show Schottky barrier (MOSFETS) with Source, Drain and Gates identified, fabricated to include the insulating material achieved low leakage Schottky barrier device geometries as just described. Devices fabricated as just described eliminate a large portion of the Schottky barrier junction area such shown as present in Figs. 3 and 4 between the metal (15) and semiconductor (11) and (12). It is also to be noted that the Schottky barrier junction in, for instance, Fig. 11(g0) and 11g1 are, as a consequence of the isotropic etching of the silicon (100), placed under a gate metalization. This eliminates another source of nonoptimum current limitation in that during operation no high resistance gap exists between a gate voltage applied induced channel in the silicon and the Schottky barrier at the source and drain ends of said channel region. The present Schottky barrier devices then overcome both high leakage current and high effective channel region to source and drain gap induced resistance problems. Said problems were the focus in the Patent to Koeneke et al, No. 4,485,550, which Patent described the use of source and drain ion implantations as an approach to the overcoming thereof.

Figs. 11(l), 11(n) and 11(o) show non-inverting single device equivalents to (CMOS) and Fig. 11(m) shows an inverting version. The same identifying numeral system is used in Figs. 11(ha) to 11(o) as was used in Figs. 11(a0) to 11(g3). Namely, silicon (100), silicon dioxide (102), silicide (108), doped silicon region (100d), conductor metal (103) and SUB is an insulating substrate such as saphire.

It is also within the scope of the present invention to effect selected insulated regions in an etched silicon source or drain region by deposition of a material, (eg. silicon nitride), which protects a silicon region during an oxidation procedure,

then remove said protective material after said oxidation procedure. As well, a deposited nonoxide insulator in an etched semiconductor region might be allowed to remain with portions thereof etched away at ends of a channel region to allow silicide formation thereat. Such approaches might provide better results than simply growing oxide and etching it away where desired, particularly where gate silicon dioxide is undercut by an isotropic silicon etch, because selective etchants could be utilized to avoid adversely affecting an undercut oxide geometry.

Turning now to Figs. 12(a) and 12(b) there are shown circuit symbols for conventional diffused junction P-Channel and N-Channel (MOSFET) devices. The directions of the arrowheads on the line representing the substrate identify the (MOSFET) device type. (It is noted that the substrate is shown electrically interconnected to the source in Figs. 12(a) through 15(b). This is not to be considered absolutely required for a conventional or Schottky barrier (MOSFET) to operate, but simply observes conventional symbolism). In use the Drain (D) junction is considered reverse biased and a negative/(positive) voltage is applied to the gate (G) of a P-Channel/(N-Channel) device respectively. Application of a positive or negative voltage to a gate causes carriers, (ie. electrons or holes respectively), to accumulate at the semiconductor-insulator, (in the case of silicon an oxide is a typical insulating material), interface channel region in the semiconductor thereby forming a channel between source and drain. When the semiconductor is P-type and a positive gate voltage is applied, a conducting inverted N-type channel will form. When the semiconductor is N-type and a negative gate voltage is applied, a conducting inverted P-type channel will form.

Fig. 13(a) shows a conventional diffused junction (MOSFET)

(CMOS) device system. Application of a gate voltage to interconnected gates (G) near positive (+Vdd) causes the N-Channel device to turn "on", (ie. form a conducting channel between its source (S) and drain (D)), while the P-Channel is turned "off" (ie. has no conducting channel between source and drain), thereby effecting a voltage near ground potential at the interconnected drains (D) point (M). Application of an essential ground potential to interconnected gates (G) causes the P-Channel device to turn "on", (while the N-Channel device is "off"), thereby effecting a voltage near positive (+Vdd) at said interconnected drains (D) mid-point (M).

Continuing, it must be understood that the present Schottky barrier (MOSFETS) operate differently than do conventional diffused junction (MOSFETS) in that applied Gate voltage effect on channel region substrate doping serves to modulate the leakage current through a reverse biased Schottky barrier junction. An effectively higher channel region doping serving to cause an increased reverse leakage current rather than simply effect a conducting similar type of doped semiconductor between source and drain. This difference in operational basis causes the voltage which must be applied between a drain and source of a Schottky barrier (MOSFET) to be opposite to that applied in a conventional diffused junction (MOSFET). That is, current flows in the opposite direction in a Schottky barrier (MOSFET) as compared to a conventional diffused junction (MOSFET) of the same channel type, (ie. N-Channel or P-Channel). The following table demonstrates the voltage polarity comparisons in a clear concise manner:

(MOSFETS)

	DIFFUSED JUNCTION		SCHOTTKY BARRIER	
	GATE	DRAIN	GATE	DRAIN
P-TYPE SUBSTRATE (N-CHANNEL)	+	+	+	-
N-TYPE SUBSTRATE (P-CHANNEL	-	-	-	+

Note that operational gate voltage (Vg) polarity is the same for both diffused junction and Schottky barrier (MOSFET) technologies as negative/(positive) gate volts attract holes/(electrons) to a channel region in a semiconductor channel region. However, the operational applied drain voltage (-Vdd), as identifed above, is reversed comparing conventional diffused junction and Schottky barrier (MOSFETS). This means that the position of N-Channel and P-Channel devices must be reversed in a Schottky barrier (CMOS) system. Fig. 13(b) shows this configuration using the same circuit symbols as used for conventional diffused junction (MOSFETS), but with a (SB) included to indicate that Schottky barrier junction technology is utilized in both source and drain. With a gate voltage (Vg) near (+Vss) applied to the interconnected gates (G), the N-Channel device will have an effectively positive voltage applied thereto between its gate (G) and source (S). This will attract electrons to, and cause inversion of, the channel region

therein, causing the Schottky barrier junction electrically connected to the (-Vdd) source to be reverse biased but conduct a gate controlled leakage, (ie. tunneling), current therethrough. The drain (D) of said N-Channel device will be forward biased in the inverted channel region thereby providing a voltage (Vm) at the mid-point interconnected drains (D) of the N-Channel and P-Channel devices to be at essentially negative (-Vdd). Note that while the inverted channel in the N-Channel device is conducting, the channel in the P-Channel device does not conduct and is "off". This is confirmed by the curves shown in Figs. 6 and 7, which curves were derived by test of actual fabricated P-Channel and N-Channel Schottky barrier (MOSFETS). It is believed that energy band pinning in the channel region accounts for this result. That is, a noninverted channel region seems to be prevented from accumulating and therefore does not form a reverse bias conducting Schottky barrier junction with an applied source (or drain) region metalization, as does an inverted channel region. This point is subject of continued investigation. Continuing, when the gate voltage (Vg) is caused to be near negative (-Vdd), it should be appreciated by symetry that the N-Channel device will be "off" and that a conducting inverted P-Channel will be effected in said P-Channel device. That is, an effective negative voltage applied to the interconnected gates (G) attracts holes to the channel region of the P-Channel Schottky barrier device causing channel region substrate type inversion. This of course, effects a voltage (Vm) very near -Vss at the mid-point interconnection of drains (D) as the drain Schottky barrier junction in the inverted channel region of the P-Channel device is effectively forward biased with respect to the source voltage applied thereto. It is to be understood the that +Vss in Fig. 13(b) can be replaced by a ground and the device system will still work.

Fig. 8 represents the gate voltage influence on voltage at

mid-point (M) connection of the drains (D) of the N-Channel and P-Channel devices shown in Fig. 13(b).

Fig. 14 shows circuit symbols for Schottky barrier (MOSFETS) of the same channel type, (shown P-Channel but simply changing device type indicating arrowhead direction represents N-Channel as well), configured in a balanced differential system such as commonly found in operational amplifiers. Note that nonsemiconductor components of Schottky barrier source junctions are electrically interconnected to effect the configuration. Also note that the gates are not electrically connected, but will connect across a source of voltage.

Figs. 15(a) and 15(b) show circuit symbols for N-Channel Schottky barrier (MOSFETS) configured in an active device with (MOSFET) load system. In Fig. 15(a) the load is an N-channel (MOSFET) and in Fig. 15(b) the load is a P-channel (MOSFET). Similar systems can be configured using P-Channel Schottky barrier active device (MOSFETS) with (MOSFET) loads and Figs. 15(a) and 15(b) can be considered to show said arrangements by assuming the device type indicating arrowheads reversed.

It is to be noted that Schottky barrier junctions are comprised of nonsemiconductor and semiconductor components, such as a (metal and/or metal silicide), and silicon respectively. Functional electrical interconnection of two Schottky barrier junctions is typically effected by connecting the nonsemiconductor components of two Schottky barrier junctions. Electrical interconnections can be achieved by conducting traces on a substrate, or by external wiring which accesses the nonsemiconductor component. It can occur that a common semiconductor area between two devices can effect a semiconductor electrical interconnection as well. In such a case a contact metal can be considered a nonsemiconductor

"electrical interconnection" component. Also, the channel regions of Schottky barrier (MOSFETS) are formed in semiconductor and are typically continuous between respective rectifying source and drain junctions. That is, nonsemiconductor components of a Schottky barrier junction typically "sandwich" a "continuous" semiconductor channel region, which has an insulator and gate sequentially situated adjacent thereto, therebetween. Also "respective" rectifying source and drain junctions are those rectifying junctions associated with a semiconductor channel region. As well, Schottky barrier junctions are typically assumed to be rectifying. It can occur, however, that a Schottky barrier can be made to demonstrate non-rectifying characteristics. Formation on heavily doped semiconductor, for instance, can provide this result. In the Claims, the term "non-rectifying" will be used to identify Schottky barrier junctions which demonstrate other than rectifying characteristics, said other characteristics typically being ohmic.

It is also to be understood that while Schottky barrier junctions are typically formed between a metal and a semiconductor or a metal-compound, (eg. silicide where silicon is utilized), and a semiconductor, the terms "metal forming silicide", in the case where the semiconductor is silicon, should be interpreted broad enough to include any material which forms a rectifying junction with a semiconductor, whether technically a metal or not, for the purposes of Claim interpretation.

It is also noted that (MOSFET) devices formed on N-type semiconductor and which operate when a channel region is inverted are termed P-Channel devices. Likewise, (MOSFET) devices formed on P-type semiconductor and which operate when a channel region is inverted are termed N-Channel devices. That

is, N-Channel (MOSFET) devices are formed on P-type semiconductor and P-Channel (MOSFET) devices are formed on N-type semiconductor. The reader should not be confused by this and in reading the Claims should keep this distinction clearly in mind.

The terminology "Single device equivalent to (CMOS)" has been used in the Disclosure because it draws attention to important similarities between the present invention devices and (CMOS), where the present invention involves one (MOSFET)-like device formed on a single type semiconductor, in place of two electrically interconnected (MOSFET) devices in series as required in conventional diffused junction (CMOS). For the purpose of Claim construction however, the terminology "single device with operating characteristics similar to (CMOS)" will be utilized.

Also, it is to be clear that when it is stated that a present invention device is formed on a "single-type" semiconductor, the intended meaning is that there is no requirement for a checkerboard of alternating N and P-type regions in a semiconductor to effect a single device with operating characteristics similar to conventional diffused junction (CMOS) device systems. It does not mean that regions of a single device of the present invention formed on N or P-type semiconductor can not have opposite type doping or intrinsic semiconductor present therein, or that single devices of the present invention formed on intrinsic semiconductor can not have regions of doped semiconductor present, or that a checkerboard of N and P-type regions, with single devices of the present invention in said regions can not be present, emphasis added. It means only that each present single device which provides operating characteristics similar to conventional diffused junction (CMOS) multiple device systems is formed in a

single type semiconductor and that there is no requirement that a device formed in N-type semiconductor be electrically interconnected to a device formed in P-type semiconductor to provide the (CMOS) operating characteristics. The use of the terms "single device" should be taken to sufficiently distinguish over conventional diffused junction (CMOS) device systems which require both an N and a P-Channel device be present with their drains electrically interconnected in series to provide a (CMOS) device system which demonstrates similar operating characteristics to a single device of the present invention.

In the Claims, it will be appreciated that when a Schottky barrier (CMOS) device system is described as resulting from electrical interconnection of present invention N and P-Channel Schottky barrier (MOSFETS) devices, the geometry of the Schottky barrier-channel region is well identified as providing Schottky barriers only at the end(s) of a channel region, which geometry serves to reduce leakage current problems, and it is this which distinguishes over known prior art in multiple present invention device systems.

It is also noted that rectangular source and drain geometry was used for demonstrative, not limiting, purposes in the foregoing. Circular geometry, wherein a source region is essentially surrounded by a drain region for instance is to be considered equivalent and within the scope of the present invention.

Having hereby disclosed the subject matter of the present invention, it should be obvious that many modifications, substitutions, and variations of the present invention are possible in light of the teachings. It is therefore to be understood that the present invention may be practiced other than as specifically described, and should be limited in breadth and scope only by the Claims.

CLAIMS

I CLAIM:

1. A non-inverting single Metal Oxide Semiconductor (MOS) device with operating characteristics similar to multiple device Complimentary Metal Oxide Semiconductor (CMOS) systems in which an applied gate voltage controls a voltage present at an essentially electrically isolated terminal thereof; comprising a semiconductor channel region and two rectifying channel region Schottky barrier junctions in a surface region of a single doping type semiconductor, selected from the group consisting of N-type, P-type and Intrinsic semiconductor, said rectifying channel region Schottky barrier junctions being separated by said semiconductor channel region, wherein a gate to which semiconductor channel region doping type modulating voltage can be applied is associated with said semiconductor channel region, said gate being offset from said semiconductor channel region by an insulating material, such that application of a sufficient negative voltage to the gate will attract holes into said semiconductor channel region, and such that application of a sufficient positive voltage to the gate will attract electrons into said semiconductor channel region, the purpose of applying such gate voltage being to modulate the effective doping type of said semiconductor channel region, such that when a constant polarity voltage is applied between said rectifying channel region Schottky barrier junctions one thereof forward conducts to the channel region while the other thereof does not, and vice versa, depending on the applied gate voltage effected semiconductor doping type in said semiconductor channel region, which essentially electrically isolated terminal electrically contacts said channel region and during use monitors a constant polarity voltage applied to one of the rectifying Schottky

barrier junctions, which constant polarity voltage appears at said essentially electrically isolated terminal essentially through the forward conducting channel region Schottky barrier junction, which constant polarity voltage monitored by said essentially electrically isolated terminal increases when the voltage applied to said gate is increased.

2. A non-inverting single Metal Oxide Semiconductor (MOS) device with operating characteristics similar to multiple device Complimentary Metal Oxide Semiconductor (CMOS) systems as in Claim 1 in which the essentially electrically isolated terminal contact to said semiconductor channel region is essentially non-rectifying.

3. A non-inverting single Metal Oxide Semiconductor (MOS) device with operating characteristics similar to multiple device Complimentary Metal Oxide Semiconductor (CMOS) systems as in Claim 1 in which at least one of said Schottky barrier junctions is formed in a region etched into said semiconductor, said etched semiconductor region being partially covered by an insulating material, the purpose thereof being to reduce leakage current by limiting the area of Schottky barrier junctions in contact with semiconductor to regions at ends of said semiconductor channel region.

4. A non-inverting single Metal Oxide Semiconductor (MOS) device with operating characteristics similar to multiple device Complimentary Metal Oxide Semiconductor (CMOS) systems as in Claim 1 in which the semiconductor is silicon and the Schottky barriers are formed between said silicon and a material selected from the group consisting of chromium, molybdnium, tungstun, vanadium, titanium, platinum and a silicide of any thereof.

5. An inverting single Metal Oxide Semiconductor (MOS) device

with operating characteristics similar to multiple device Complimentary Metal Oxide Semiconductor (CMOS) systems in which an applied gate voltage controls a voltage present at an essentially electrically isolated terminal thereof; comprising first and second essentially non-rectifying channel region junctions in a surface region of a single doping type semiconductor selected from the group consisting of N-type, P-type and Intrinsic semiconductor, said first and second essentially non-rectifying channel region junctions being separated by first and second semiconductor channel regions from electrically interconnected rectifying channel region Schottky barrier junctions, wherein a gate to which semiconductor channel region doping type effecting modulating voltage can be applied is associated with said first and second semiconductor channel regions, said gate being offset from said first and second semiconductor channel regions by an insulating material, such that application of a sufficient negative voltage to the gate will attract holes into said first and second semiconductor channel regions, and such that application of a sufficient positive voltage to the gate will attract electrons into said first and second semiconductor channel regions, the purpose of applying such gate voltage being to modulate the effective doping type of said first and second semiconductor channel regions, such that when a constant polarity voltage is applied between said first and second essentially non-rectifying channel region junctions one rectifying semiconductor channel region Schottky barrier junction forward conducts while the other does not, and vice versa, depending on the applied gate voltage effected semiconductor doping type in said first and second semiconductor channel regions, which essentially electrically isolated terminal electrically contacts said electrically interconnected rectifying channel region Schottky barrier junctions and during use monitors a constant polarity voltage applied to one of the essentially non-rectifying channel region junctions, which constant polarity

voltage appears at said essentially electrically isolated terminal essentially through the forward conducting semiconductor channel region Schottky barrier junction, which constant polarity voltage monitored by said essentially electrically isolated terminal decreases when the voltage applied to said gate is increased.

6. An inverting single Metal Oxide Semiconductor (MOS) device with operating characteristics similar to multiple device Complimentary Metal Oxide Semiconductor (CMOS) systems as in Claim 5 in which at least one of said Schottky barrier junctions is formed in a region etched into said semiconductor, said etched ~~semiconductor being~~ partially ~~covered by~~ an insulating material, the purpose thereof being to reduce leakage current by limiting the area of Schottky barrier junctions in contact with said semiconductor to regions at ends of said semiconductor channel regions.

7. An inverting single Metal Oxide Semiconductor (MOS) device with operating characteristics similar to multiple device Complimentary Metal Oxide Semiconductor (CMOS) systems as in Claim 5 in which the semiconductor is silicon and the Schottky barriers are formed between said silicon and a material selected from the group consisting of chromium, molybdnium, tungstun, vanadium, titanium, platinum and a silicide of any thereof.

8. A method of configuring a non-inverting Metal Oxide Semiconductor (MOS) device with operating characteristics similar to Complimentary Metal Oxide Semiconductor (CMOS) systems comprising the steps of:

a. providing two Metal Oxide Semiconductor Field Effect Transistor (MOSFET) devices, each formed in a surface region of the same single doping type semiconductor selected from the group

consisting of N-type, P-type, Intrinsic, N-type and Intrinsic, and P-type and Intrinsic, semiconductor, one said (MOSFET) device comprising two semiconductor Schottky barrier junctions, termed source and drain, separated by a first semiconductor channel region, and the second (MOSFET) device comprising two semiconductor Schottky barrier junctions, termed source and drain, separated by a second semiconductor channel region, wherein gates to which semiconductor channel region inverting voltages can be applied are associated with each of the first and second semiconductor channel regions are offset from said first and second semiconductor channel regions by insulating material, such that during use application a sufficient positive voltage to said gates will attract electrons to said first and second semiconductor channel regions, and such that application of sufficient negative voltage to said gates will cause attraction of holes to both of said first and second semiconductor channel regions, the purpose of applying such gate voltage being to, modulate the doping type of said first and second semiconductor channel regions between respective source and drain Schottky barrier junctions, which Schottky barrier drain junctions are each caused to be, by semiconductor doping and the like, essentially non-rectifying, and which Schottky barrier source junctions are rectifying, said Schottky barrier junctions each comprising a semiconductor and nonsemiconductor component;

b. electrically interconnecting a nonsemiconductor component of the essentially non-rectifying semiconductor Schottky barrier drain junction associated with said first semiconductor channel region, and a nonsemiconductor component of the essentially non-rectifying semiconductor Schottky barrier drain junction associated with said second semiconductor channel region;

c. electrically interconnecting said gates, such that during operation nonsemiconductor components of electrically

noninterconncted rectifying semiconductor Schottky barrier source junctions are held at different voltages, and application of a gate voltage controls effective semiconductor channel region doping type in both (MOSFET) devices, and thus which electrically noninterconnected semiconductor rectifying Schottky barrier source junction forward conducts and which does not forward conduct, thereby controlling the voltage present at the electrically interconnected essentially non-rectifying semiconductor Schottky barrier drain junctions essentially through said forward conducting rectifying semiconductor Schottky barrier junction.

9. A method of configuring an inverting Metal Oxide Semiconductor (MOS) device with operating characteristics similar to Complimentary Metal Oxide Semiconductor (CMOS) systems comprising the steps of:

a. providing two Metal Oxide Semiconductor Field Effect Transistor (MOSFET) devices, each formed in a surface region of the same single doping type semiconductor selected from the group consisting of N-type, P-type, Intrinsic, N-type and Intrinsic, and P-type and Intrinsic, semiconductor, one said (MOSFET) device comprising two semiconductor Schottky barrier junctions, termed source and drain, separated by a first semiconductor channel region, and the second (MOSFET) device comprising two semiconductor Schottky barrier junctions, termed source and drain, separated by a second semiconductor channel region, wherein gates to which semiconductor channel region inverting voltage can be applied are associated with each of the first and second semiconductor channel regions are offset from said first and second semiconductor channel regions by insulating material, such that during use application a sufficient positive voltage to said gates will attract electrons to said first and second semiconductor channel regions, and such that application of

sufficient negative voltage to said gates will cause attraction of holes to both of said first and second semiconductor channel regions, the purpose of applying such gate voltage being to, modulate the effective doping type of said first and second semiconductor channel regions between respective source and drain Schottky barrier junctions, which Schottky barrier source junctions are each caused to be, by semiconductor doping and the like, essentially non-rectifying, and which Schottky barrier drain junctions are rectifying, said Schottky barrier junctions each comprising a semiconductor and nonsemiconductor component;

b. electrically interconnecting a nonsemiconductor component of the rectifying semiconductor Schottky barrier drain junction associated with said first semiconductor channel region, and a nonsemiconductor component of the rectifying semiconductor Schottky barrier drain junction associated with said second semiconductor channel region;

c. electrically interconnecting said gates, such that during operation nonsemiconductor components of electrically noninterconnncted essentially non-rectifying semiconductor source junctions are held at different voltages, and application of a gate voltage controls effective semiconductor channel region doping type in both (MOSFET) devices, and thus which electrically interconnected rectifying semiconductor Schottky barrier drain junction forward conducts and which does not forward conduct, thereby controlling the voltage present at the nonsemiconductor components of the electrically interconnected semiconductor Schottky barrier drain junctions essentially through said forward conducting rectifying semiconductor Schottky barrier junction.

10. A Metal Oxide Semiconductor (MOS) device formed in a surface region of a semiconductor, comprising a Schottky barrier junction, (selected from the group consisting of rectifying and

semiconductor and the like doping effected essentially non-rectifying), to a semiconductor channel region, wherein a gate to which semiconductor channel region doping type controling voltage can be applied is associated with said semiconductor channel region and offset therefrom by insulating material, such that during use application of a sufficient negative voltage to said gate will cause attraction of holes into said semiconductor channel region, and such that application of sufficient positive voltage to said gate will cause attraction of electrons into said semiconductor channel region, the purpose of applying such gate voltage being to modulate the doping type of said semiconductor channel region; which said Schottky barrier junction is formed in a region etched into said semiconductor, which etched region ~~is~~ partially ~~covered with~~ comprises an insulating material, the purpose thereof being to reduce leakage current by limiting the area of Schottky barrier junction in contact with said semiconductor to a region near an end of said semiconductor channel region.

11. A Metal Oxide Semiconductor (MOS) device as in Claim 10 in which the etched region in said semiconductor is such that the insulating material by which the gate is offset from the semiconductor channel region is undercut thereby and in which said Schottky barrier is present only at the end of said semiconductor channel region which is located under said gate offsetting insulator material.

12 A Metal Oxide Semiconductor Field Effect Transistor (MOSFET) device system formed in a surface region of a semiconductor, comprising two N-type semiconductor Schottky barrier junctions, termed source and drain, separated by a first semiconductor channel region, in functional combination with two P-type semiconductor Schottky barrier junctions, termed source and drain, separated by a second semiconductor channel region, each Schottky barrier junction comprising a semiconductor and

nonsemiconductor component, said functional combination comprising an electrical interconnection between a nonsemiconductor component of one N-type semiconductor Schottky barrier junction and a nonsemiconductor component of one P-type semiconductor Schottky barrier junction, wherein gates to which channel region doping type and conductivity modulating voltages can be applied are associated with each of the first and second semiconductor channel regions, said gates being offset from said first and second semiconductor channel regions by insulating material, such that during operation application of a sufficient negative voltage to the gates atop the N and P-type semiconductors will cause formation of an inversion P-type channel in said N-type semiconductor channel region and perhaps an accumulation region in said P-type semiconductor channel region, and such that application of a sufficient positive voltage to the gates atop the P and N-type semiconductor will cause formation of an inversion N-type channel in said P-type semiconductor channel region and perhaps an accumulation region in said N-type semiconductor channel region, the purpose of applying such gate voltages being to modulate the effective doping type, conductivity and current carrying capability of the channel regions separating respective source and drain Schottky barrier junctions, and of tunneling and leakage current through said Schottky barrier junctions; in which MOSFET device system at least one of said source and drain Schottky barrier junctions is formed in a region etched into said semiconductor, which etched region is partially ~~covered with~~ an insulating material, the purpose thereof being to reduce leakage current at said source or drain by limiting the area of Schottky barrier junctions in contact with said semiconductor to regions at ends of the associated semiconductor channel region.

13. A (MOSFET) device system as in Claim 12 in which said electrical interconnection is also by semiconductor components of

said Schottky barrier junctions.

14. A (MOSFET) device system as in Claim 12 in which the semiconductor is silicon.

15. A (MOSFET) device system as in Claim 12 in which the N and P-type semiconductors are present on a single semiconductor substrate.

16. A (MOSFET) device system as in Claim 12 in which a same metal is used to form the N-type and P-type semiconductor Schottky barrier junctions with both the N and P-type semiconductors during a common simultaneous procedure.

17. A (MOSFET) device system as in Claim 12 in which a same metal-silicide is used to form the N-type and P-type semiconductor Schottky barrier junctions with both the N and P-type semiconductors during a common simultaneous procedure.

18. A (MOSFET) device system as in Claim 16 in which the metal includes chromium and the semiconductor is silicon.

19. A (MOSFET) device system as in Claim 17 in which the metal-silicide includes chromium-disilicide and the semiconductor is silicon.

20. A (MOSFET) device system as in Claim 16 in which the metal includes at least one selection from the group consisting of molybdenum, tungstun, vanadium, titanium and platinum and the semiconductor is silicon.

21. A (MOSFET) device system as in Claim 17 in which the metal-silicide includes at least one selection from the group consisting of molybdenum-disilicide, tungsten-disilicide,

vanadium-disilicide titanium-disilicide and platinum-silicide and the semiconductor is silicon.

22. A (MOSFET) device system as in Claim 16 in which the metal effects a Schottky Barrier Potential height of approximately half the bandgap of the semiconductor involved so that rectifying junctions on said N and P-type semiconductor have relatively balanced current-voltage characteristics.

23. A (MOSFET) device system as in Claim 17 in which the metal-silicide effects a Schottky Barrier Potential height of approximately half the bandgap of the semiconductor involved so that rectifying junctions on said N and P-type semiconductor have relatively balanced current-voltage characteristics.

24. A P-channel Metal Oxide Semiconductor Field Effect Transistor (MOSFET) device system formed in a surface region of N-type semiconductor comprising two N-type semiconductor Schottky barrier junctions, termed source and drain, separated by a first semiconductor channel region, in functional combination with two N-type semiconductor Schottky barrier junctions, termed source and drain, separated by a second semiconductor channel region, said Schottky barrier junctions each comprising a semiconductor and nonsemiconductor component, said functional combination comprising an electrical interconnection between a nonsemiconductor component of one N-type semiconductor Schottky barrier junction associated with said first semiconductor channel region, and a nonsemiconductor component of an N-type semiconductor Schottky barrier junction associated with said second semiconductor channel region, wherein gates to which semiconductor channel region doping type inverting voltage can be applied are associated with each of said first and second semiconductor channel regions and offset from said first and second semiconductor channel regions by insulating material, such

that during use application a sufficient negative voltage to said gates will cause both of said first and second semiconductor channel regions to invert, and such that application of sufficient positive voltage to said gates will perhaps cause both of said first and second semiconductor channel regions to accumulate, the purpose of applying such gate voltages being to modulate the type, conductivity and current carrying capability through said semiconductor channel regions between respective source and drain N-type semiconductor Schottky barrier junctions and of tunneling and leakage current through said Schottky barrier junctions; in which MOSFET device system at least one of said Schottky barrier source and drain junctions is formed in a region etched into said semiconductor, which etched region is partially ~~covered with~~ an insulating material, the purpose thereof being to reduce leakage current at said source or drain by limiting the area of Schottky barrier junctions in contact with said semiconductor to regions at ends of the associated semiconductor channel region.

25. A P-channel (MOSFET) device system formed in a surface region of an N-type semiconductor as in Claim 24, in which electrical interconnection is also by way of semiconductor components of said Schottky barrier junctions.

26. An N-channel Metal Oxide Semiconductor Semiconductor Field Effect Transistor (MOSFET) device system formed in a surface region of a P-type semiconductor comprising two P-type semiconductor Schottky barrier junctions, termed source and drain, separated by a first semiconductor channel region, in functional combination with two P-type semiconductor Schottky barrier junctions, termed source and drain, separated by a second semiconductor channel region, said Schottky barrier junctions each comprising a semiconductor and nonsemiconductor component, said functional combination comprising an electrical

interconnection between a nonsemiconductor component of one P-type semiconductor Schottky barrier junction associated with said first semiconductor channel region, and a nonsemiconductor component of a P-type semiconductor Schottky barrier junction associated with said second semiconductor channel region, wherein gates to which semiconductor channel region doping type inverting voltages can be applied are associated with each of the first and second semiconductor channel regions and offset from said first and second semiconductor channel regions by insulating material, such that during use application a sufficient positive voltage to said gates will cause both of said first and second semiconductor channel regions to invert, and such that application of sufficient negative voltage to said gates will perhaps cause both of said first and second semiconductor channel regions to accumulate, the purpose of applying such gate voltages being to modulate the type, conductivity and current carrying capability through said semiconductor channel regions between respective source and drain Schottky barrier P-type semiconductor junctions and of tunneling and leakage current through the Schottky barrier junctions; in which MOSFET device system at least one of said source and drain Schottky barrier junctions is formed in a region etched into said semiconductor, which etched region is partially covered with an insulating material, the purpose thereof being to reduce leakage current at said source or drain by limiting the area of Schottky barrier junctions in contact with said semiconductor to regions at ends of the associated semiconductor channel region.

27. An N-channel (MOSFET) device system formed in a surface region of an N-type semiconductor as in Claim 26, in which electrical interconnection is also by way of semiconductor components of said Schottky barrier junctions.

28. A (MOSFET) device system as in Claim 12 in which the

electrically interconnected Schottky barrier junctions are the rectifying drain junctions of an N-channel and a P-channel Schottky barrier (MOSFET) and the resulting system is a (CMOS) system in which the gates of the N-channel and P-channel (MOSFETS) are also electrically interconnected, such that when a constant polarity voltage is applied between the Schottky barrier rectifying source, application of sufficient negative gate voltage to form an inverted P-channel in the P-channel (MOSFET) controls the voltage present at the electrically interconnected rectifying Schottky barrier drain junctions to be closer to the constant polarity voltage applied to the rectifying source Schottky barrier junction of the P-channel (MOSFET) formed in N-type semiconductor, and application of positive gate voltage sufficient to form an N-channel in the N-channel (MOSFET) controls the voltage present at the electrically interconnected Schottky barrier rectifying drain junctions to be closer to the constant polarity voltage applied to the Schottky barrier source junction of the N-channel (MOSFET) formed in P-type semiconductor.

29. A (MOSFET) device system as in Claim 12 in which the electrically interconnected Schottky barrier junctions are the rectifying source and drain junctions of a P-channel and an N-channel (MOSFET) respectively, and the resulting system is an active (MOSFET) in series with a load (MOSFET), and in which the gate of said load (MOSFET) is electrically interconnected to another lead of said load (MOSFET), such that when a voltage is applied between the load (MOSFET) Schottky barrier rectifying source and the load (MOSFET) Schottky barrier drain said load (MOSFET) is electrically conductive from drain to source, and such that a voltage applied between the active (MOSFET) gate and Schottky barrier rectifying source controls the current flow through said load (MOSFET) drain to source.

30. A (MOSFET) device system as in Claim 12 in which the electrically interconnected Schottky barrier junctions are the rectifying source and drain junctions of an N-channel and a P-channel (MOSFET) respectively, and the resulting system is an active (MOSFET) in series with a load (MOSFET), and in which the gate of said load (MOSFET) is electrically interconnected to another lead of said load (MOSFET), such that when a voltage is applied between the load (MOSFET) Schottky barrier rectifying source and the load (MOSFET) Schottky barrier rectifying drain said load (MOSFET) is electrically conductive from drain to source, and such that a voltage applied between the active (MOSFET) gate and Schottky barrier rectifying source controls the current flow through said load (MOSFET) drain to source.

31. A P-channel (MOSFET) device system as in Claim 24 in which the electrically interconnected Schottky barrier junctions are the rectifying source junctions of two P-channel (MOSFETS) and the resulting system is a balanced differential (MOSFET) system, such that when voltages are applied between the Schottky barrier rectifying drain junction of each device and the electrically interconnected Schottky barrier rectifying source junctions, then a voltage difference applied between the gates of the two P-channel (MOSFETS), controls current flow through each said Schottky barrier rectifying drain junction.

32. A P-channel (MOSFET) device system as in Claim 24 in which the electrically interconnected Schottky barrier junctions are the rectifying source and drain junctions of two P-channel (MOSFETS) and the resulting system is an active (MOSFET) with in series with a load (MOSFET), and in which the gate of said load (MOSFET) is electrically interconnected to another lead of said load (MOSFET), such that when a voltage is applied between the load (MOSFET) Schottky barrier source and the load (MOSFET) Schottky barrier drain said load (MOSFET) is electrically

conductive drain to source, and such that a voltage applied between the active (MOSFET) gate and Schottky barrier rectifying source controls the current flow through said load (MOSFET) drain to source.

33. A P-channel (MOSFET) device system as in Claim 24 in which the electrically interconnected Schottky barrier junctions are drain junctions with semiconductor doping and the like effected essentially non-rectifying characteristics, and in which the gates of said devices are also electrically interconnected, such that when a constant polarity voltage is applied between the N-type semiconductor Schottky barrier rectifying source junctions, a voltage applied between the electrically interconnected gates and one N-type semiconductor rectifying source controls the voltage present at the electrically interconnected N-type semiconductor Schottky barrier junction drains with essentially non-rectifying charastics, which resulting system is a non-inverting single (MOS) device with operating characteristics similar to multiple device (CMOS) systems, fabricated on a single type semiconductor.

34. A P-channel (MOSFET) device system as in Claim 24 in which the electrically interconnected Schottky barrier junctions are drain junctions, and in which the gates of said devices are also electrically interconnected, such that when a constant polarity voltage is applied between the N-type semiconductor Schottky barrier source junctions with semiconductor doping and the like effected essentially non-rectifying characteristics, a voltage applied between the electrically interconnected gates and one N-type Schottky barrier semiconductor source junction with essentially non-rectifying characteristics, controls the voltage present at the electrically interconnected N-type semiconductor Schottky barrier rectifying junction drains, which resulting system is an inverting single (MOS) device with operating

characteristics similar to multiple device (CMOS) systems, fabricated on a single type semiconductor.

35. An N-channel (MOSFET) device system as in Claim 26 in which the electrically interconnected Schottky barrier junctions are the source junctions of two N-channel (MOSFETS) and the resulting system is a balanced differential (MOSFET) system, such that when voltages are provided between the Schottky barrier drain junction of each device and the electrically interconnected Schottky barrier source junctions, then a voltage difference applied between the gates of the two N-channel (MOSFETS), controls current flow through each said Schottky barrier drain junctions.

36. An N-channel (MOSFET) device system as in Claim 26 in which the electrically interconnected Schottky barrier junctions are the source and drain junctions of two N-channel (MOSFETS) and the resulting system is an active (MOSFET) in series with a load (MOSFET), and in which the gate of said load (MOSFET) is electrically interconnected to another lead of said load (MOSFET), such that when a voltage is applied between the load (MOSFET) Schottky barrier source and the load (MOSFET) Schottky barrier drain said load (MOSFET) is electrically conductive drain to source, and such that a voltage applied between the active (MOSFET) gate and Schottky barrier source controls the current flow through said load (MOSFET) drain to source.

37. An N-channel (MOSFET) device system as in Claim 26 in which the electrically interconnected Schottky barrier junctions are drain junctions with semiconductor doping and the like effected essentially non-rectifying characteristics, and in which the gates of said devices are also electrically interconnected, such that when a constant polarity voltage is applied between the P-type semiconductor Schottky barrier rectifying source junctions, a voltage applied between the electrically

interconnected gates and one P-type semiconductor rectifying source controls the voltage present at the electrically interconnected P-type semiconductor Schottky barrier junction drains with essentially non-rectifying characteristics, which resulting system is a non-inverting single (MOS) device with operating characteristics similar to multiple device (CMOS) systems, fabricated on a single type semiconductor.

38. An N-channel (MOSFET) device system as in Claim 26 in which the electrically interconnected Schottky barrier junctions are rectifying drain junctions, and in which the gates of said devices are also electrically interconnected, such that when a constant polarity voltage is applied between the N-type semiconductor Schottky barrier source junctions with semiconductor doping and the like effected essentially non-rectifying characteristics, a voltage applied between the electrically interconnected gates and one P-type semiconductor Schottky barrier source junction with essentially non-rectifying characteristics controls the voltage present at the electrically interconnected P-type semiconductor Schottky barrier rectifying junction drains, which resulting system is an inverting single (MOS) device with operating characteristics similar to multiple device (CMOS) systems, fabricated on a single type semiconductor.

39. A P-channel (MOSFET) device system as in Claim 24 in which the Schottky barriers are formed between N-type silicon and a material selected from the group consisting of chromium, molybdnium, tungstun, vanadium, titanium, platinum and a silicide thereof.

40. An N-channel (MOSFET) device system as in Claim 26 in which the Schottky barriers are formed between P-type silicon and a material selected from the group consisting of chromium, molybdnium, tungstun, vanadium, titanium, platinum and a silicide

thereof.

41. A (MOSFET) device system as in Claim 12, in which one of the two rectifying N-type semiconductor Schottky barrier junctions is rendered essentially non-rectifying by semiconductor doping.

42. A (MOSFET) device system as in Claim 12, in which one of the two rectifying P-type semiconductor Schottky barrier junctions is rendered essentially non-rectifying by semiconductor doping and the like.

43. A P-channel (MOSFET) device system as in Claim 24, in which one of the rectifying N-type semiconductor Schottky barrier junctions is rendered essentially non-rectifying by semiconductor doping and the like.

44. An N-channel (MOSFET) device system as in Claim 26, in which one of the rectifying P-type semiconductor Schottky barrier junctions is rendered essentially non-rectifying by semiconductor doping and the like.

45. A method of configuring a Metal Oxide Semiconductor (MOS) gate voltage controlled rectification direction device and voltage controlled switch with operating characteristics similar to a non-latching Silicon Controlled Rectifier (SCR), on N-type semiconductor comprising:

a. providing a (MOSFET) with a Schottky barrier source junction and a semiconductor doping and the like effected non-rectifying drain junction present in a surface region of an N-type semiconductor, said source and drain junctions being separated by a channel region in said N-type semiconductor, said channel region having an insulator region and gate sequentially situated adjacent thereto;

b. applying a constant positive polarity voltage drain to source such that said rectifying Schottky barrier source is reverse biased and such that only reverse bias current flows therethrough;

c. applying a negative polarity gate voltage between said gate and source such that the channel region is caused to be inverted P-type by the attraction of holes thereto, thereby effecting a forward bias between said inverted channel region and said rectifying source, such that forward biased current flows therethrough.

46. A method of configuring a Metal Oxide Semiconductor (MOS) gate voltage controlled rectification direction device and voltage controlled switch with operating characteristics similar to a non-latching Silicon Controlled Rectifier (SCR), on P-type semiconductor comprising:

a. providing a (MOSFET) with a rectifying Schottky barrier source junction and a semiconductor doping and the like effected non-rectifying drain junction in a surface region of a P-type semiconductor, said source and drain junctions being separated by a channel region in said P-type semiconductor, said channel region having an insulator region and gate sequentially situated adjacent thereto;

b. applying a constant negative polarity voltage drain to source such that said rectifying Schottky barrier source is reverse biased and such that only reverse bias current flows therethrough;

c. applying a positive polarity gate voltage between said gate and source such that the channel region is caused to be inverted

N-type by the attraction of electrons thereto, thereby effecting a forward bias between said inverted channel region and said rectifying source, such that forward biased current flows therethrough.

47. A method of configuring a Metal Oxide Semiconductor (MOS) gate voltage controlled rectification direction device and voltage controlled switch with operating characteristics similar to a non-latching Silicon Controlled Rectifier (SCR), on intrinsic semiconductor comprising:

a. providing, in a surface region of an intrinsic semiconductor substrate, a (MOSFET) with a Schottky barrier source junction and a semiconductor doping and the like effected non-rectifying drain junction which are apparent when a constant polarity voltage is applied between said drain and source junctions while a constant effective channel region doping level effecting polarity voltage is applied to a gate thereof, said source and drain junctions being separated by a channel region in said intrinsic semiconductor substrate, said channel region having an insulator region and said gate sequentially situated adjacent thereato;

b. applying a constant polarity voltage to said gate and a constant polarity voltage between said drain and source junctions such that said rectifying Schottky barrier source junction is reverse biased and such that only reverse bias current flows therethrough;

c. reversing the polarity of the constant polarity gate voltage such that the channel region is caused to be of a doping type such that said rectifying source Schottky barrier junction is forward biased, such that forward biased current flows therethrough.

48. A method of configuring a modulator comprising the steps of:

a. providing a MOSFET structure with Schottky barrier junctions present at a source and a drain present in the surface region of a semiconductor, wherein a semiconductor channel region is present therebetween, and adjacent to which semiconductor channel region is progressively present an insultaing material and a gate, to which semiconductor channel region access is provided via a channel accessing region;

b. simultaneously applying varying drain to source and gate to source voltages and monitoring a modulated resulting voltage presenting at the channel accessing region.

49. A method of configuring a modulator comprising the steps of:

a. providing a MOSFET structure with non-rectifying junctions present at a source and a drain present in the surface region of a semiconductor, wherein semiconductor Schottky barrier region is present therebetween, said source and drain each being set apart from said Schottky barrier region by semiconductor channel regions, adjacent to which semiconductor channel regions is progressively present an insultaing material and a gate, with access being available to said Schottky barrier region;

b. simultaneously applying varying drain to source and gate to source voltages and monitoring a modulated resulting voltage presenting at the Schottky barrier region.

ABSTRACT

(MOS) device systems utilizing Schottky barrier source and drain to channel region junctions are disclosed. Experimentally derived results which demonstrate operation of fabricated N-channel and P-channel Schottky barrier (MOSFET) devices, and of fabricated single devices with operational characteristics similar to (CMOS) and to a non-latching (SRC) are reported. Use of essentially non-rectifying Schottky barriers in (MOS) structures involving highly doped and the like and intrinsic semiconductor to allow non-rectifying interconnection of, and electrical accessing of device regions is also disclosed. Insulator effected low leakage current device geometries and fabrication procedures therefore are taught. Selective electrical interconnection of drain to drain, source to drain, or source to source, of N-channel and/or P-channel Schottky barrier (MOSFET) devices formed on P-type, N-type and Intrinsic semiconductor allows realization of Schottky Barrier (CMOS), (MOSFET) with (MOSFET) load, balanced differential (MOSFET) device systems and inverting and non-inverting single devices with operating characteristics similar to (CMOS), which devices can be utilized in modulation, as well as in voltage controled switching and effecting a direction of rectification.

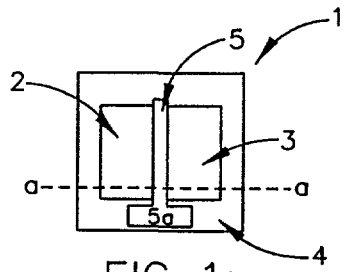

FIG. 1a
PRIOR ART

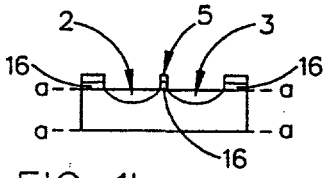

FIG. 1b
PRIOR ART

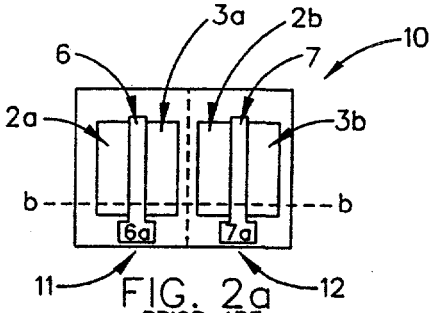

FIG. 2a
PRIOR ART

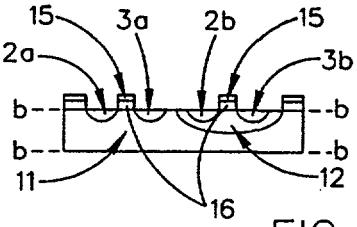

FIG. 2b
PRIOR ART

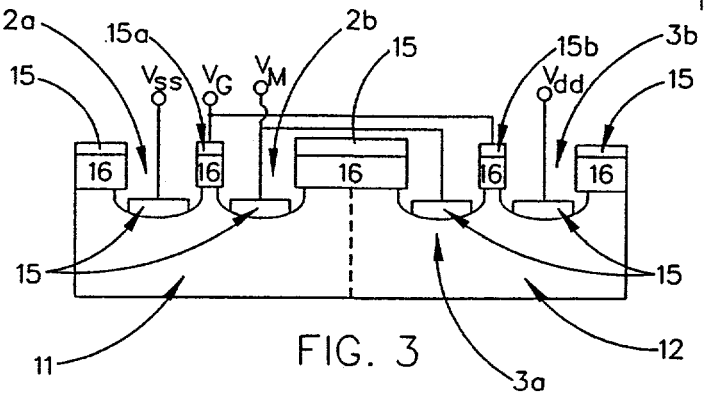

FIG. 3

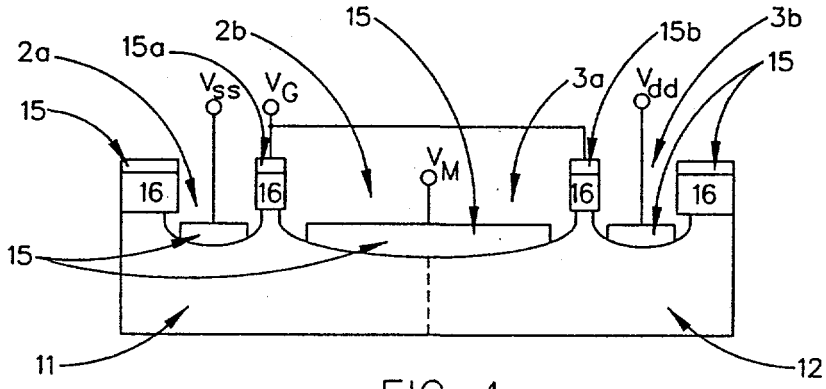

FIG. 4

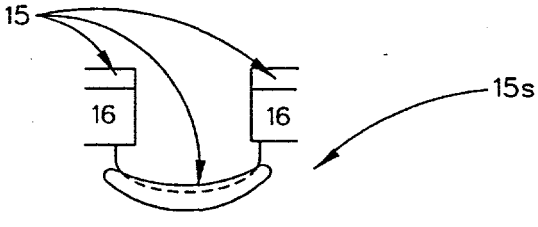

FIG. 5

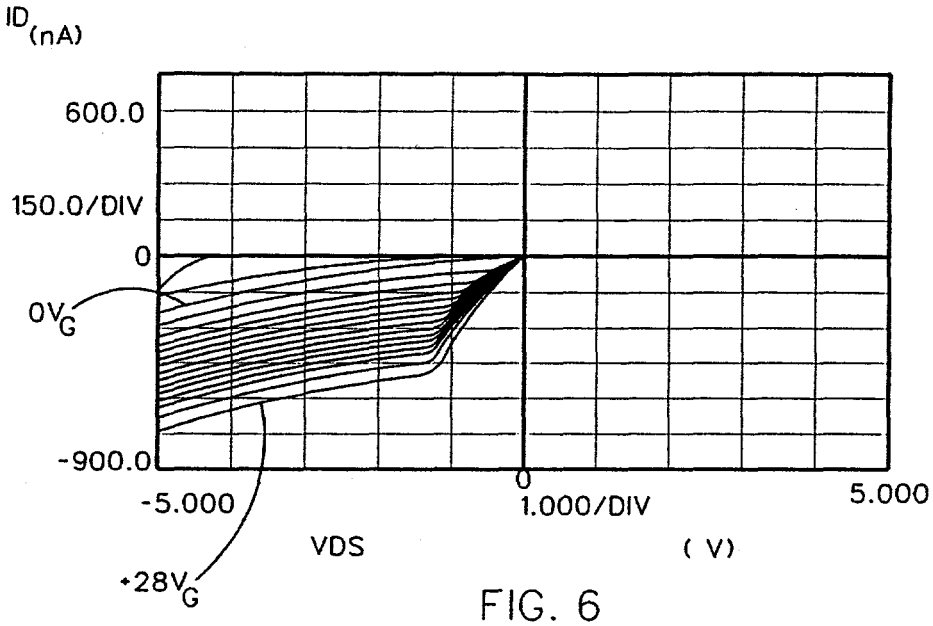

FIG. 6

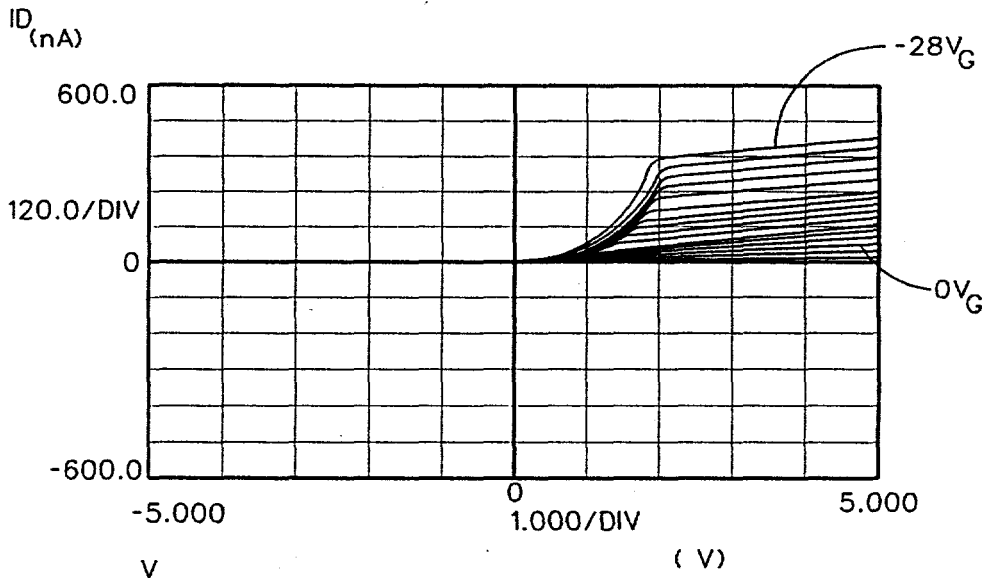

FIG. 7

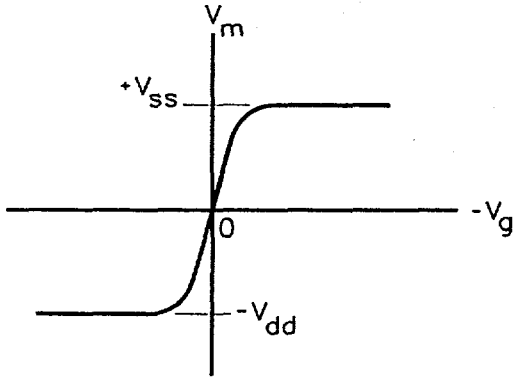

FIG. 8

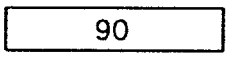

FIG. 9a

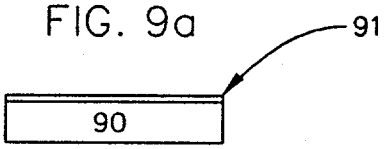

FIG. 9b

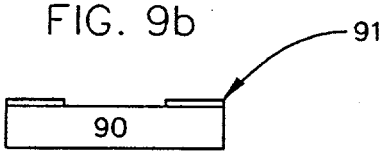

FIG. 9c

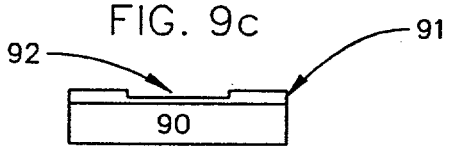

FIG. 9d

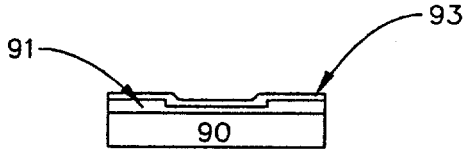

FIG. 9e

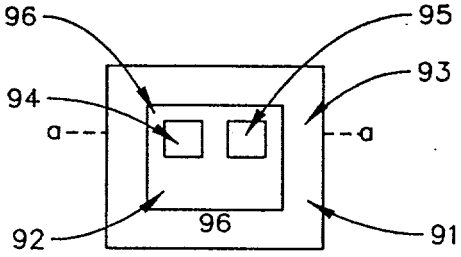

FIG. 9f

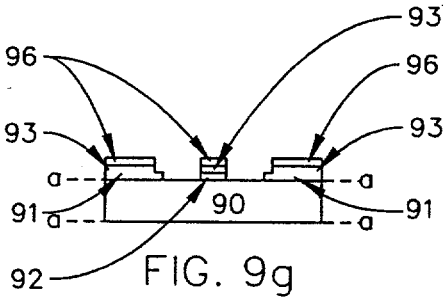

FIG. 9g

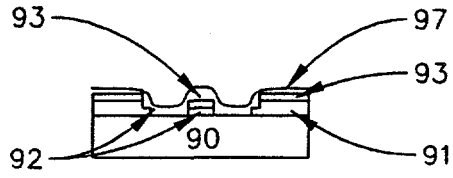

FIG. 9h

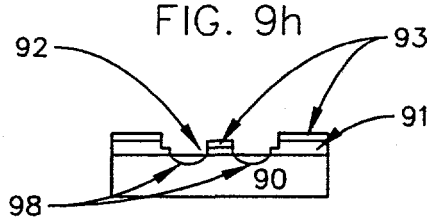

FIG. 9i

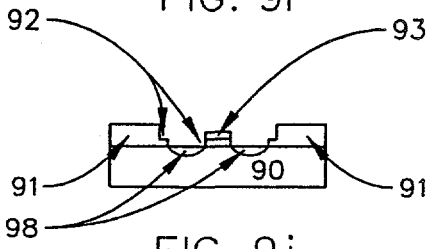

FIG. 9j

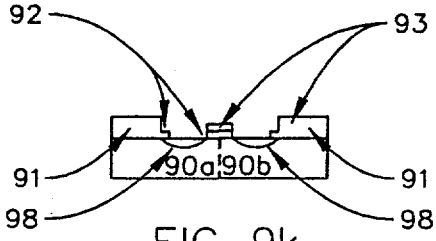

FIG. 9k

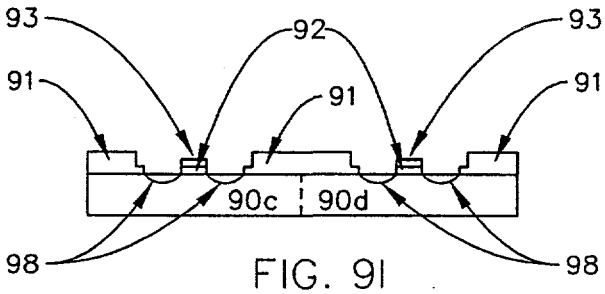

FIG. 9l

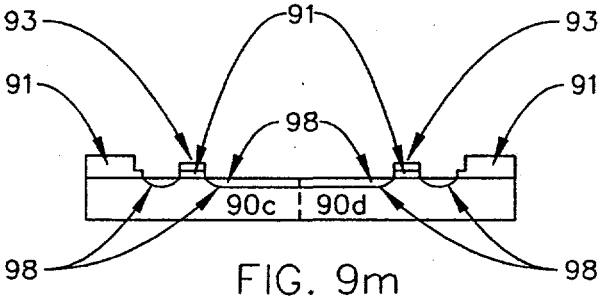

FIG. 9m

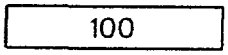

FIG. 10a

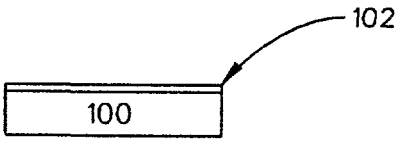

FIG. 10b

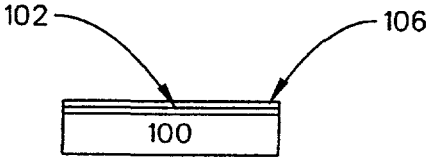

FIG. 10c

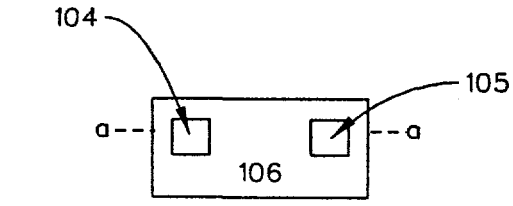

FIG. 10d

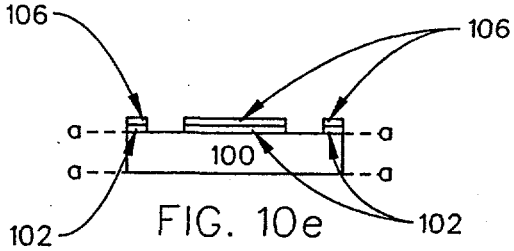

FIG. 10e

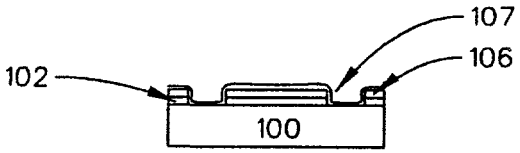

FIG. 10f

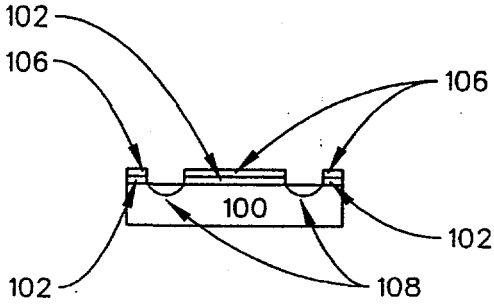

FIG. 10g

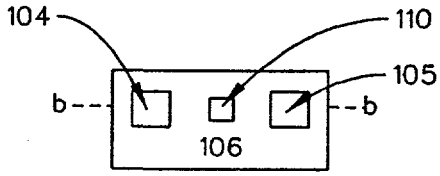

FIG. 10h

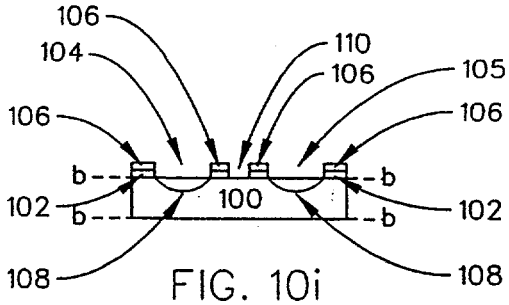

FIG. 10i

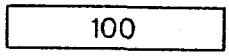

FIG. 10j

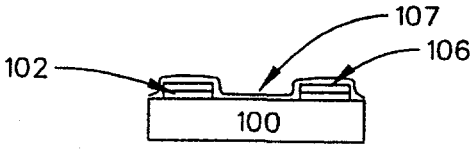

FIG. 10o

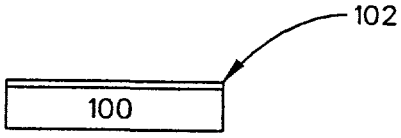

FIG. 10h

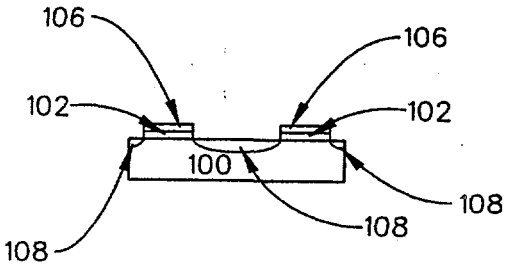

FIG. 10p

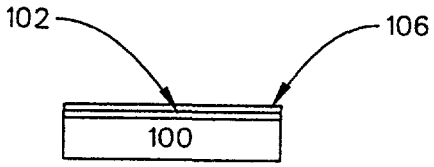

FIG. 10l

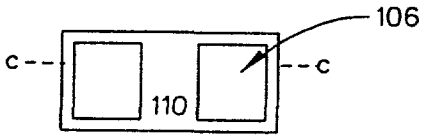

FIG. 10m

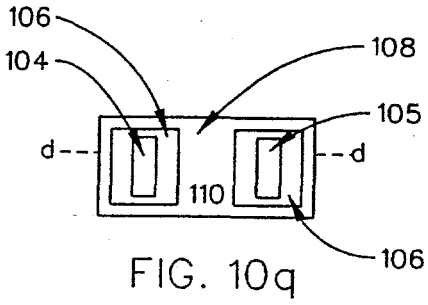

FIG. 10q

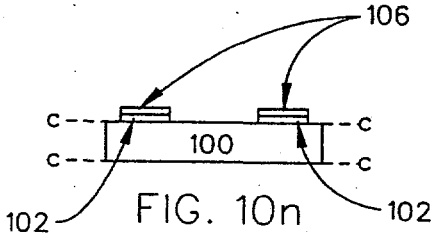

FIG. 10n

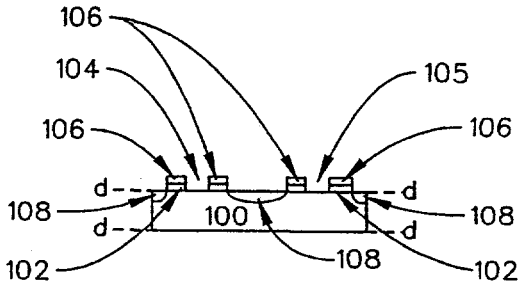

FIG. 10r

FIG. $11a_0$

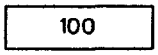

FIG. $11a_1$

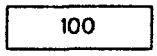

FIG. $11a_2$

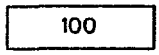

FIG. $11a_3$

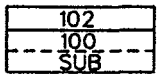

FIG. $11b_0$

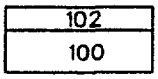

FIG. $11b_1$

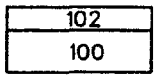

FIG. $11b_2$

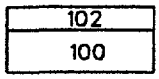

FIG. $11b_3$

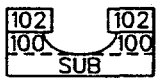

FIG. $11c_0$

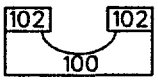

FIG. $11c_1$

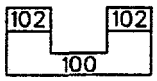

FIG. $11c_2$

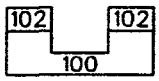

FIG. $11c_3$

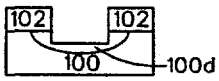

FIG. $11c_{3P}$

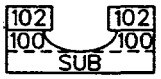

FIG. $11d_0$

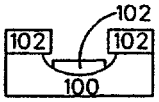

FIG. $11d_1$

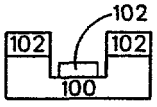

FIG. $11d_2$

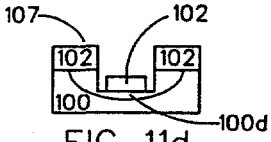

FIG. $11d_3$

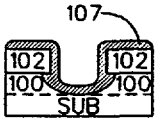

FIG. $11e_0$

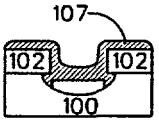

FIG. $11e_1$

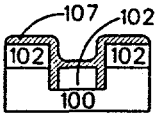

FIG. $11e_2$

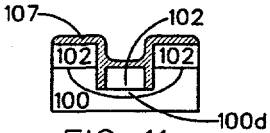

FIG. $11e_3$

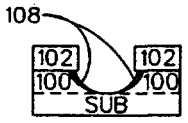

FIG. $11f_0$

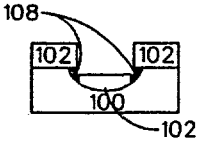

FIG. $11f_1$

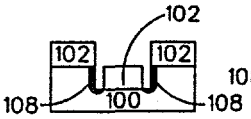

FIG. $11f_2$

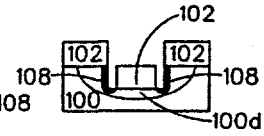

FIG. $11f_3$

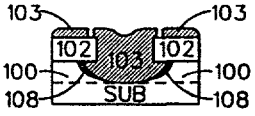

FIG. $11g_0$

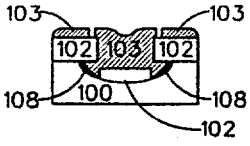

FIG. $11g_1$

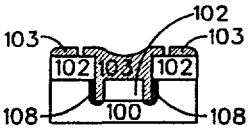

FIG. $11g_2$

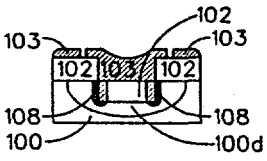

FIG. $11g_3$

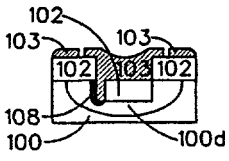

FIG. $11g_{3P}$

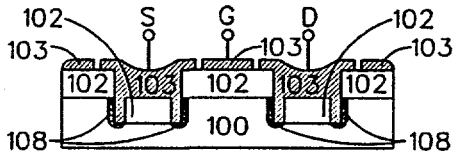

FIG. $11h_a$

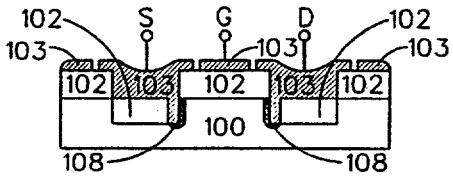

FIG. $11h_b$

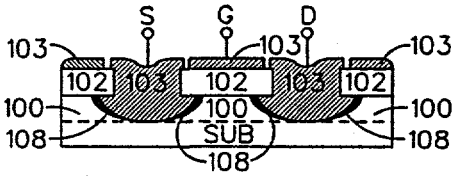

FIG. 11i

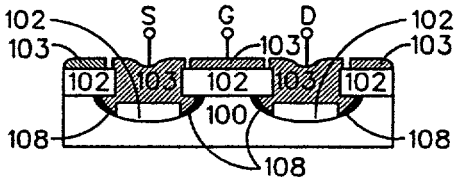

FIG. 11j

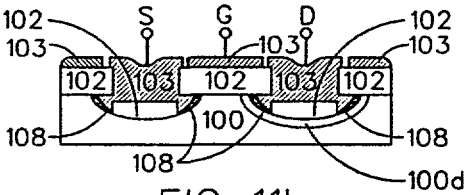

FIG. 11k

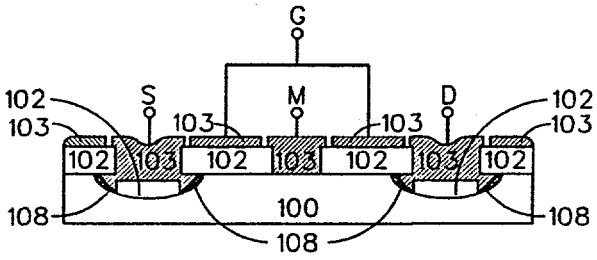

FIG. 11l

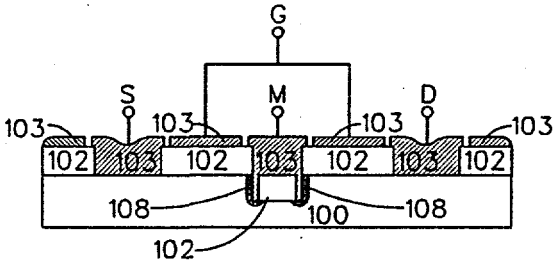

FIG. 11m

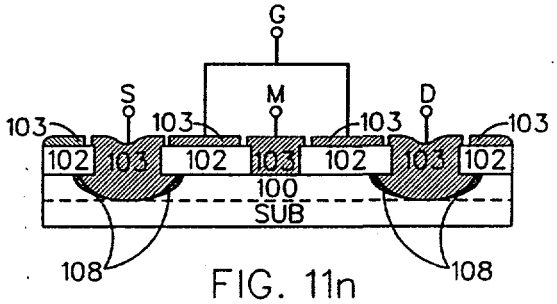

FIG. 11n

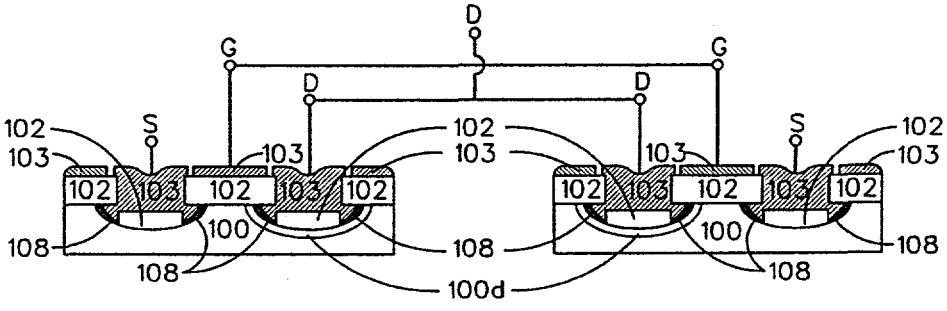

FIG. 11o

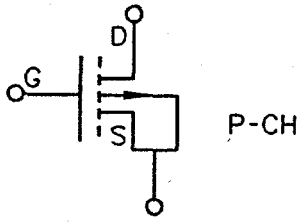

FIG. 12a

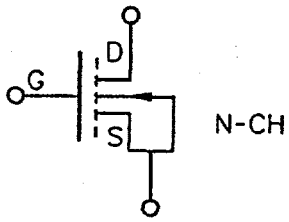

FIG. 12b

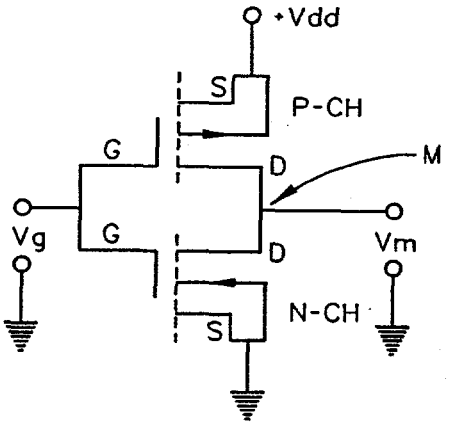

FIG. 13a

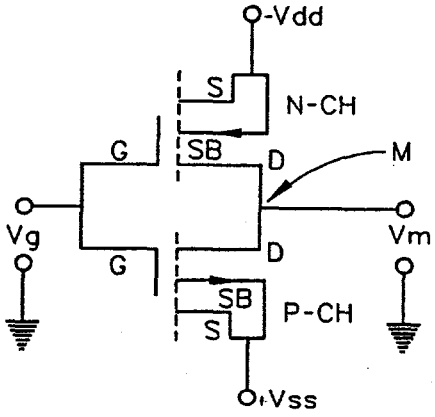

FIG. 13b

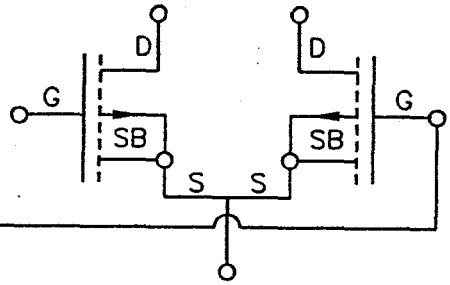

FIG. 14

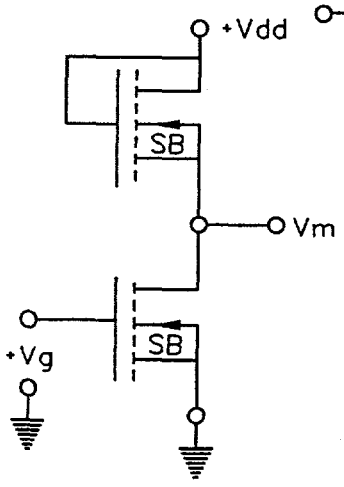

FIG. 15a

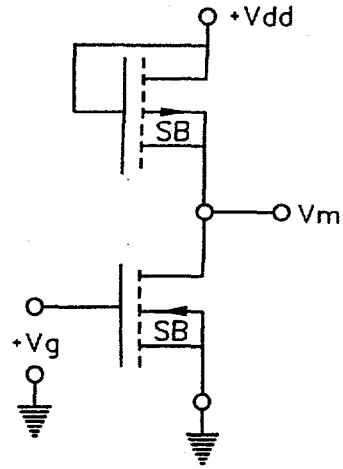

FIG. 15b