Project Final Report

100kW Energy Transfer Multiplexer Power Converter Prototype Development Project

DE-FG36-03GO13138

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March 21, 2006

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Dedication

This Final Project Report, as well as the entire ETM Converter Project, is dedicated to two men whose vision and drive were responsible for its existence: S. Merrill Skeist (1918-2005), who was the CEO of Spellman High Voltage Electronics Corporation; and Richard H. (Dick) Baker (1928-2006), who was a self-employed Consultant and President of The Baker Company. Both men enjoyed long, active and creative careers in the electronics industry.

At a time in their lives when most of their contemporaries were content primarily with relaxation and pursuits of fancy, these two technical giants among men were constantly seeking the methods and means for the improvement of electronic circuits and system, particularly in the area of power electronics. Their shared interests and technical foresight gave birth to the ETM Converter Topology, among many others. They recognized the benefits that such technology could provide to the renewable energy field, and they were powerful advocates for the adoption of the ETM technology by the Department of Energy and the renewable energy industry. They sought to leave a legacy of high-performance, cost-effective renewable energy conversion to their country and to their society.

We are all collectively better off for having had Merrill and Dick in our midst as colleagues, friends and teachers, and hopefully future generations will be similarly inspired by their ground-breaking spirit and their manifold accomplishments.

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A.) ETM Converter Test Setup

There were two setups used for the ETM Converter prototype. The first was a low power facsimile of the ETM converter power train for the debug and testing of the Control Board assembly. The second was the test lab setup used to observe the parametric and functional performance of the prototype ETM Converter. This two pronged test approach was used to decouple the programming and debug of the Control Board from the Power Train of the prototype so as to avoid damaging the expensive IGBTs and power resonant elements.

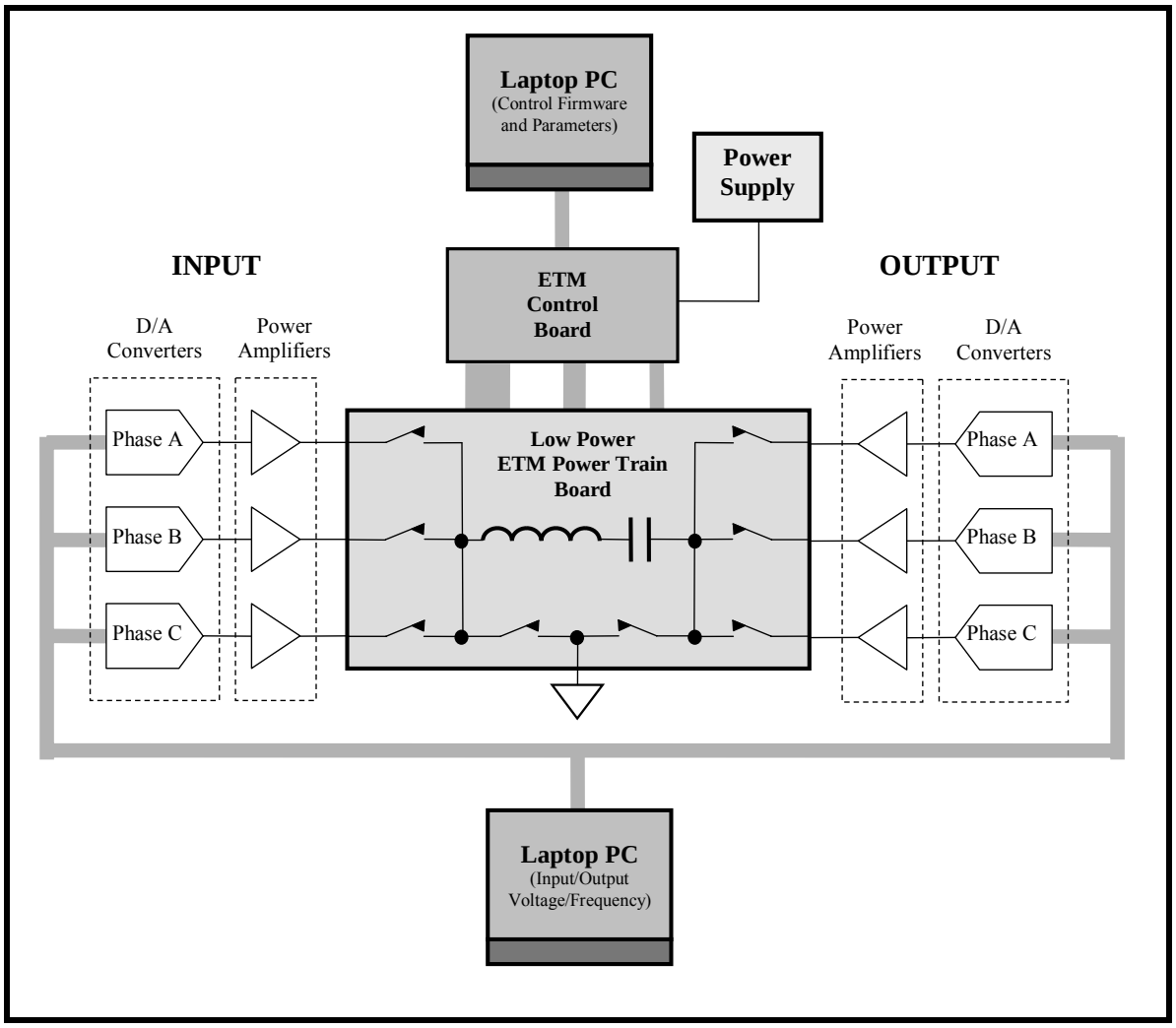
i.) ETM Control Board Debug Test Setup

The control board debug test setup was used for two purposes: To debug the firmware for the ETM Control Board (ECB) and to verify the ECB functionality during the testing of the ETM Converter prototype. The Control Board Test setup is shown in Figure A1. Six digital-to-analog converters (along with the power amplifiers) were used to provide variable amplitude, variable frequency input/output phase sources for the ETM Power Train stage. This low power replica of the 34kW prototype power stage was optimized for 20Vp-p input voltages (+/-10V) and a maximum peak current of 200mA. In this way, the operation of the ETM Converter may be achieved without high power/current/voltage to ease and simplify the software/firmware development and debug processes. The low power ETM Power Train Board also included current sensors to measure the resonant current and Phase A input current.

The two laptop computers were employed to: 1.) control the input/output voltage and frequency parameters of the operating ETM Converter; and 2.) to program the firmware on the ETM Control Board and to set the adjustable operating parameters (decision thresholds) of the of the Control Board software algorithm.

During the Control Board debug process and the ETM Converter prototype debug process, the low power facsimile board essentially provided a second prototype and the capability to make changes/modification to the firmware on a concurrent basis with the debug and performance testing of the 34kW ETM Converter prototype. All parameters involved in the operation of the ETM Converter could and were observed using this test

Figure A1. *ETM Control Board Debug/Programming Test Setup.*



setup, and excellent correspondence of operation and values was obtained using this testing methodology.

The low power ETM Converter test boards were constructed by dtm Associates and were located at TechEn, Inc., Milford, Massachusetts (the software/firmware developers) for the duration of the debug test activities.

Photographs of the actual low power ETM Converter test setup and the equipment used are shown in Figures A2 through A10, which follow.

Figure A2. *ETM Control Board Debug/Programming Configuration.*

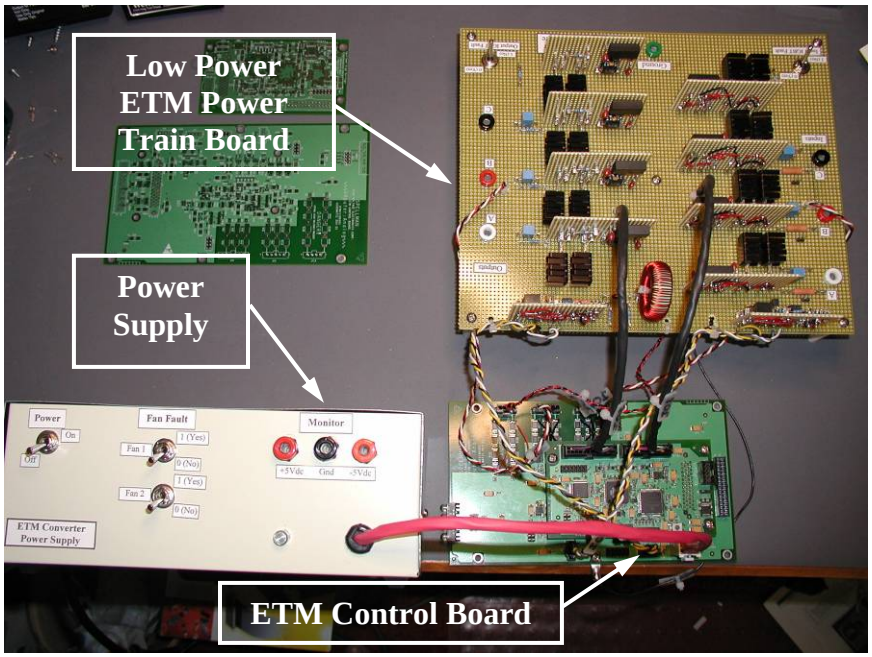


Figure A3. *ETM Control Board Debug/Programming Configuration.*

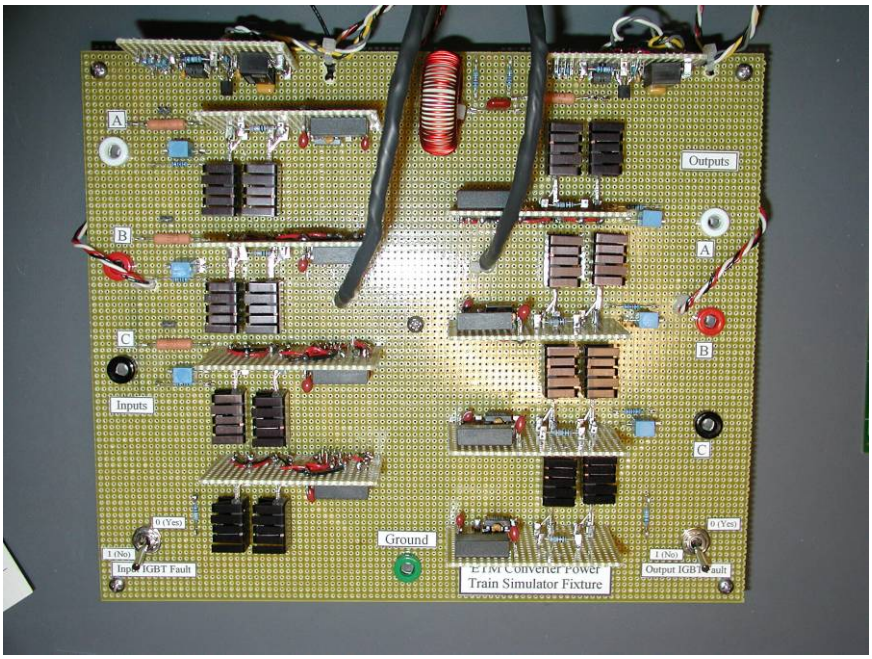


Figure A4. *Low Power ETM Power Train Board w/ETM Control Board.*

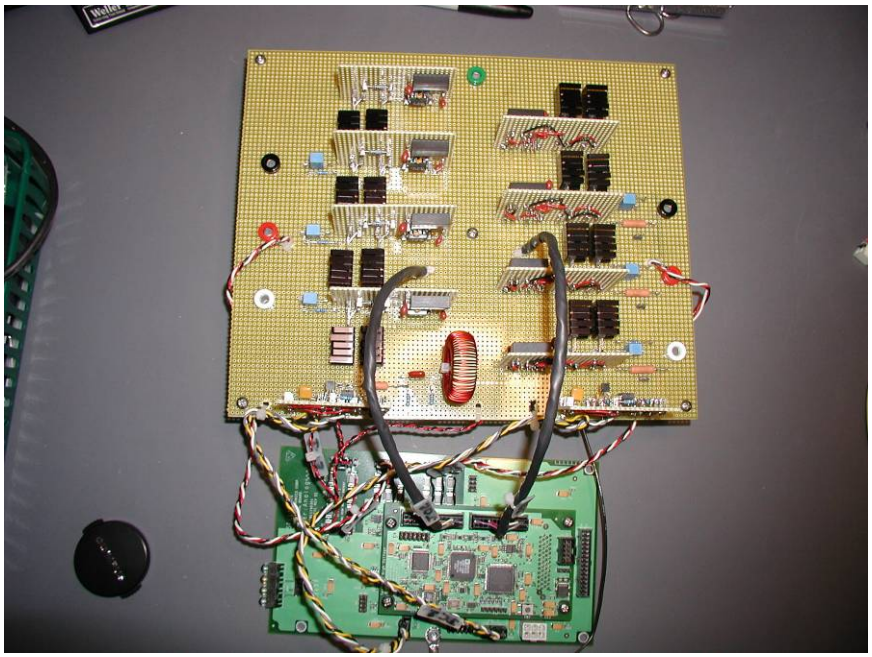


Figure A5. *Test Setup Auxiliary Power Supply.*

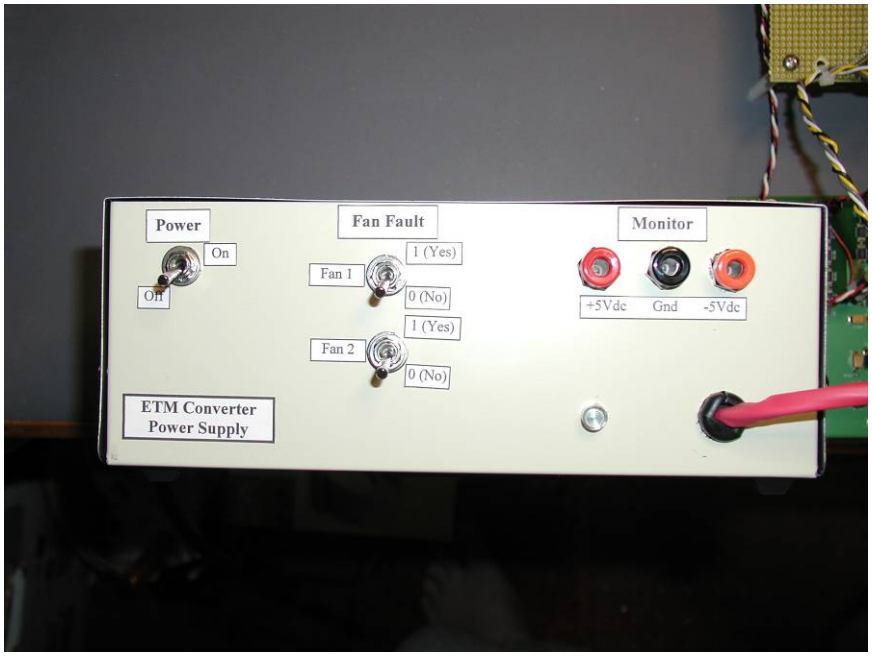
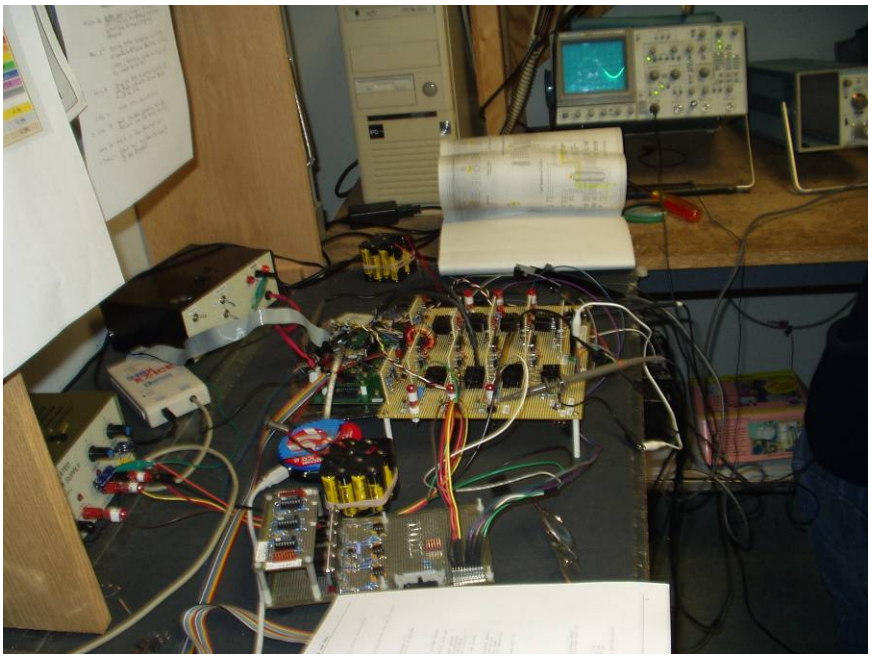
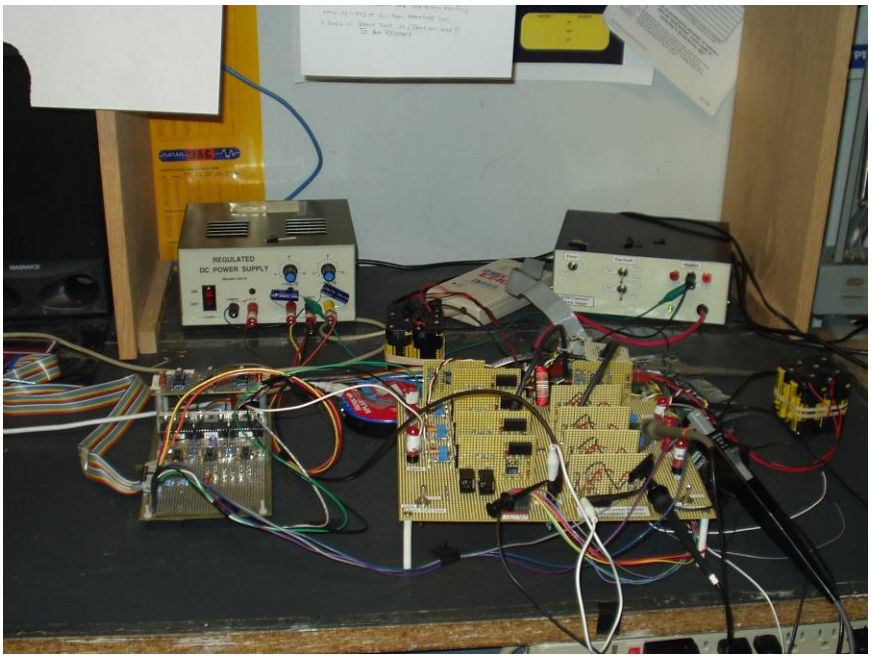


Figure A6. *ETM Firmware Debug Benchtop Test Setup.*



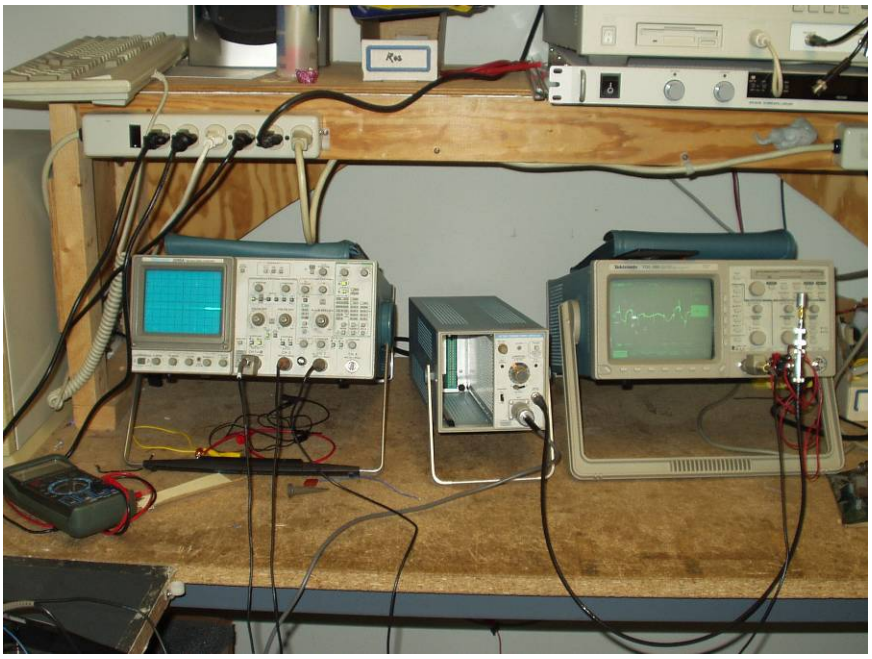
(at TechEn, Inc. Milford, MA)

Figure A7. *ETM Firmware Debug Benchtop Test Setup.*



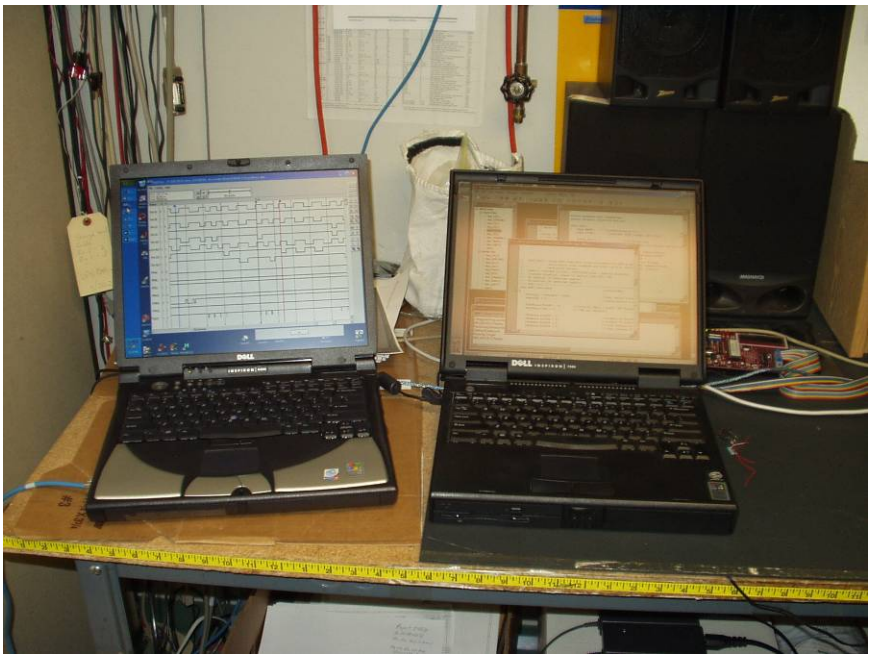
(at TechEn, Inc. Milford, MA)

Figure A8. *ETM Firmware Debug Support Test Equipment.*



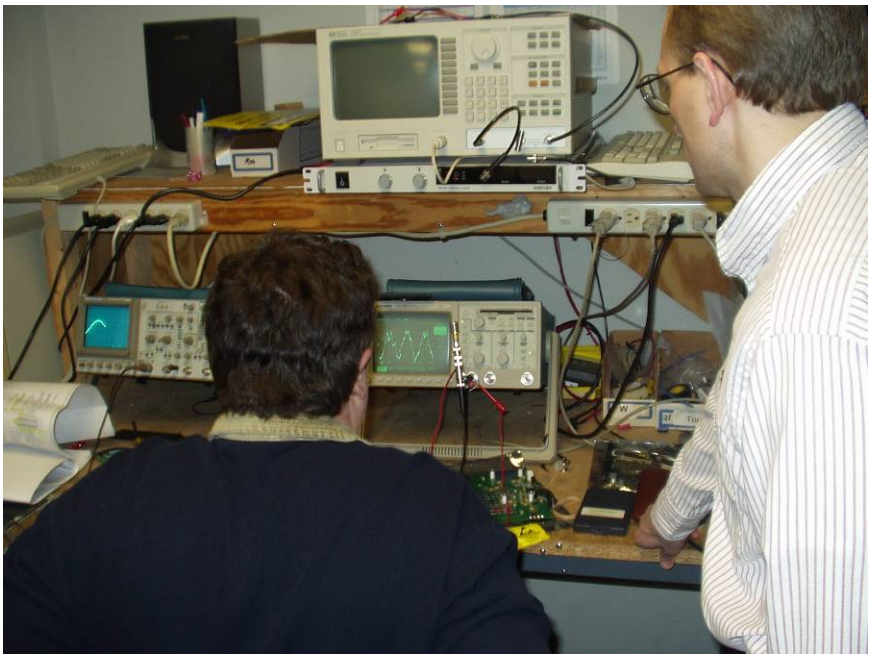
(at TechEn, Inc. Milford, MA)

Figure A9. *ETM Firmware Debug Test Support Computers.*



(at TechEn, Inc. Milford, MA)

Figure A10. *ETM Firmware Debug Test In-Progress.*

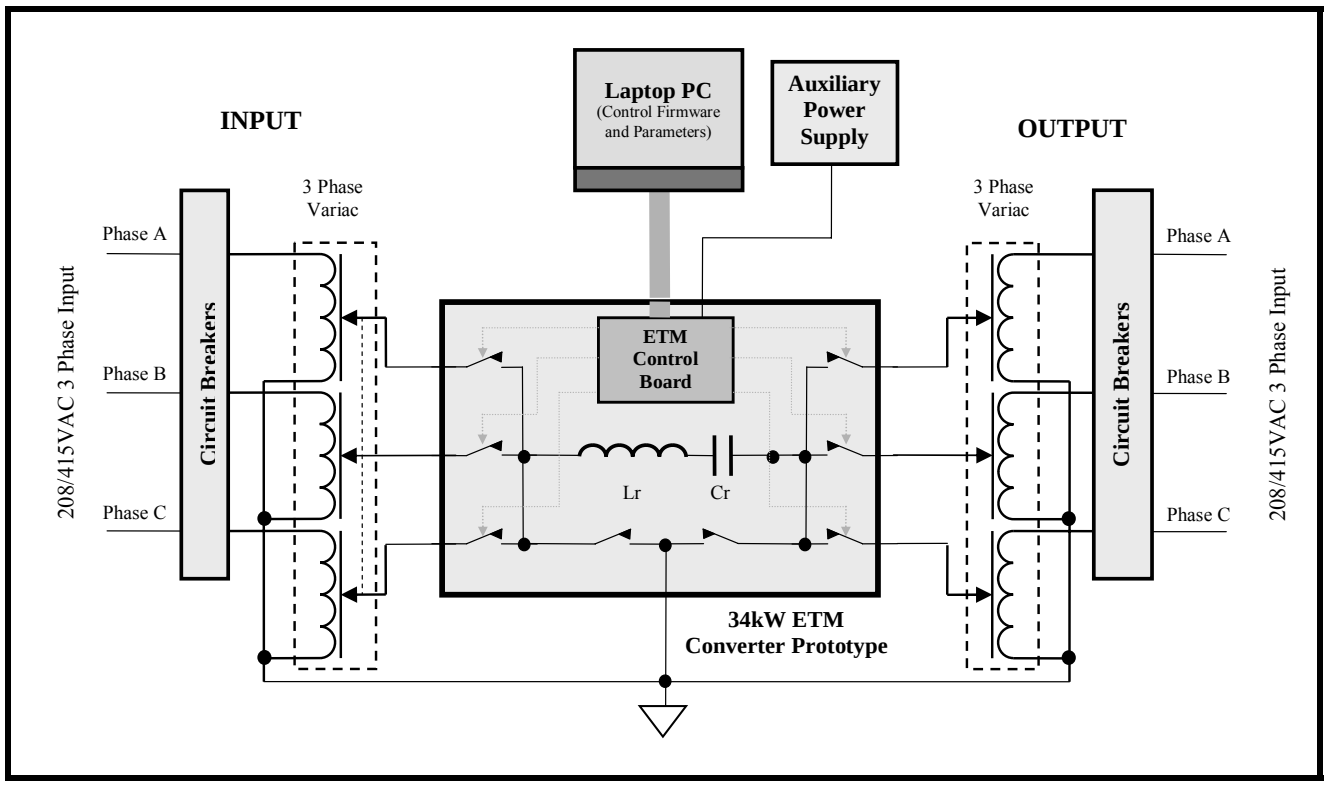


(at TechEn, Inc. Milford, MA)

ii.) 34kW Prototype ETM Converter Test Setup

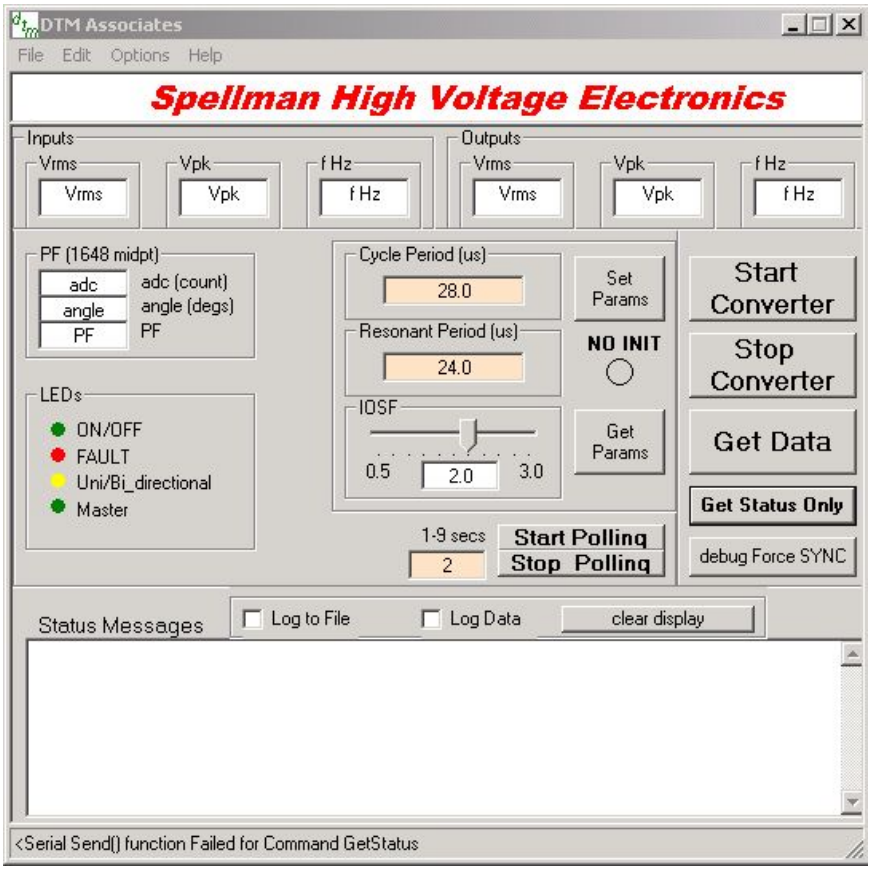
The ETM Prototype Debug and Performance Tests were performed at IQS LLC/Marlboro Test Labs in Marlborough, MA. This lab had the necessary facilitations to provide the required I/O utility voltage for the ETM Prototype. The test setup consisted of the elements shown schematically in Figure A11.

Figure A11. 34kW *Prototype ETM Converter Test Setup.*



The key elements of this test configuration are the three-phase Variacs used to vary the input and output voltages and the laptop PC computer used to set the operating variables of the ETM Converter. The laptop PC utilized custom GUI software to set the parameters and a screenshot of the software is shown in Figure A12.

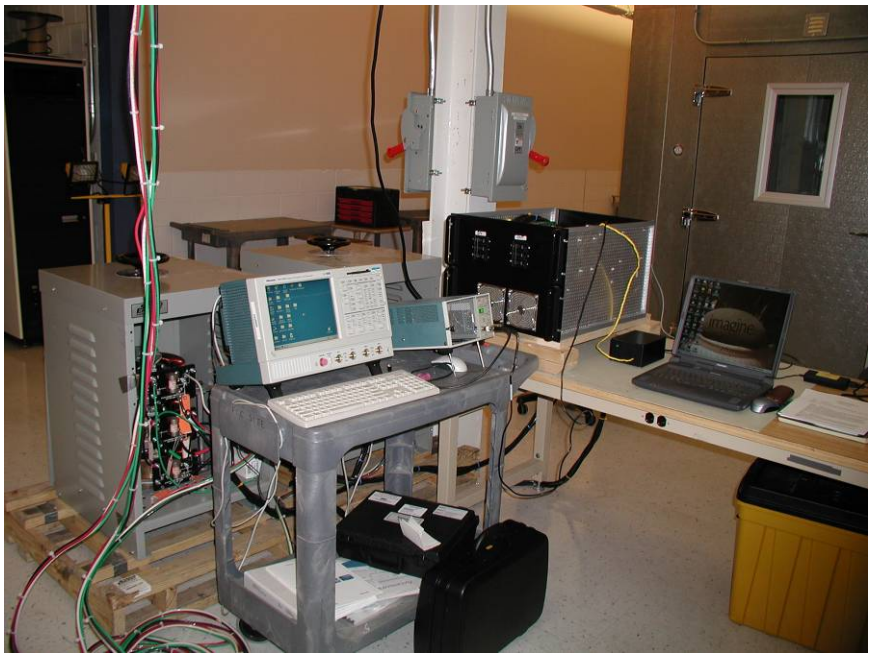
Figure A12. *34kW Prototype ETM Converter GUI Control Interface.*



The User Interface on the controller PC allows the setting and retrieval of firmware decision points and ETM Converter operating parameters. The decision point parameters include the Resonant Period time (this should match the measured L-C resonance of the power train), the Cycle Time (which is the Resonant Time plus two microseconds of idle/processing time) and the IOSF parameter (whose value corresponds to the ETM flowchart and sets the final voltage on the resonant capacitor). The operating parameters include the input and output phase voltages and frequencies, the power factor and the LED front panel indicator statuses. Additionally, the operating and fault status of the dsPIC and ADSP microcontrollers can be retrieved for debug information. Thus, during the debug and performance testing of the prototype, the decision point parameters of the ETM converter were varied and the resultant operating performance was observed.

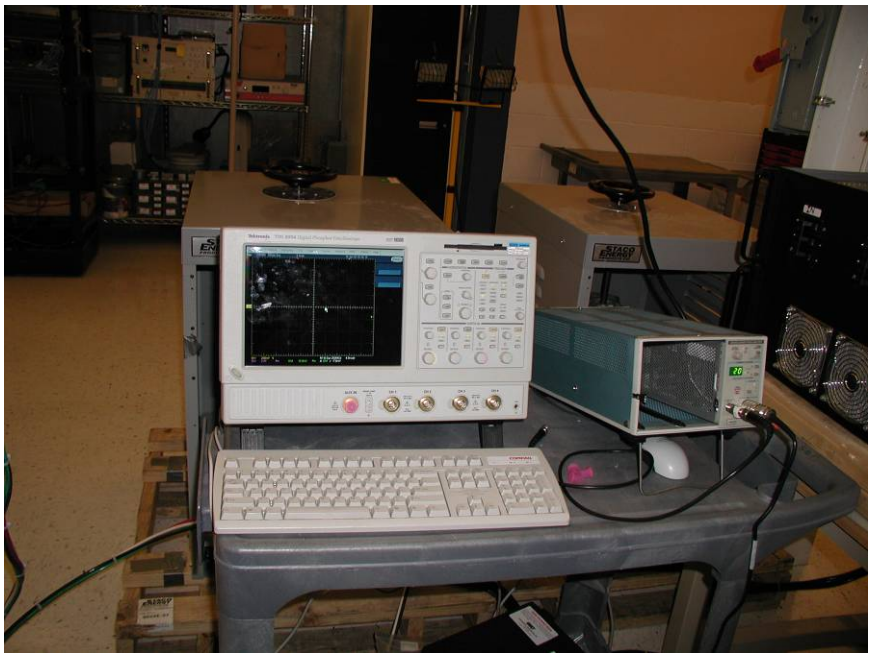
Photographs of the actual low power 34kW ETM Converter test setup and the equipment used are shown in Figures A13 through A17, which follow.

Figure A13. *34 kW ETM Converter Prototype Test Setup.*



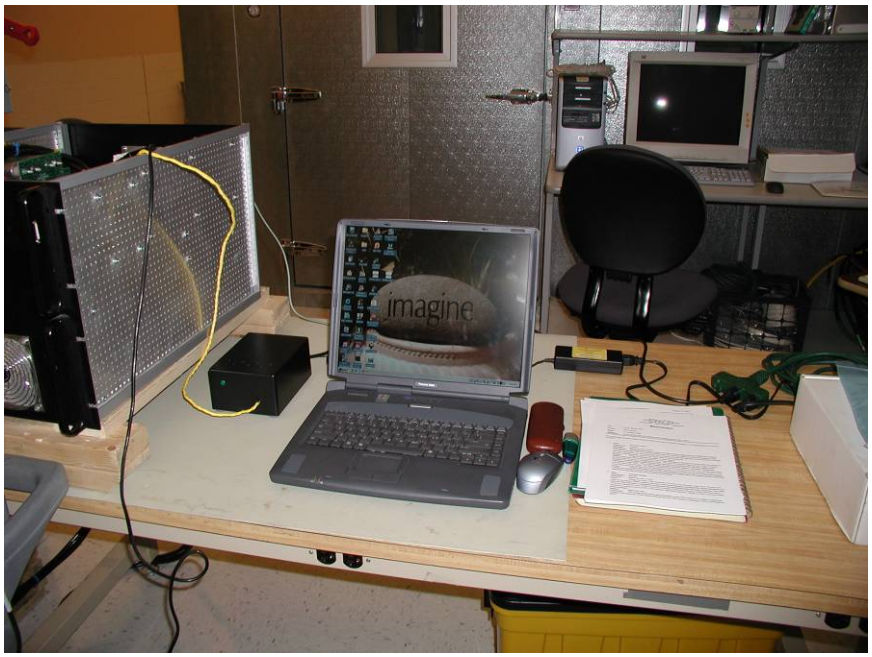
(at MTL/IQS LLC, Marlborough, MA)

Figure A14. *34 kW ETM Converter Prototype Test Support Equipment.*



(at MTL/IQS LLC, Marlborough, MA)

Figure A15. *34 kW ETM Converter Prototype Test Laptop PC Controller.*



(at MTL/IQS LLC, Marlborough, MA)

Figure A16. *Three Phase 40kVA Input and Output Variacs.*

(at MTL/IQS LLC, Marlborough, MA)

Figure A17. *34kW ETM Converter Prototype During Performance Test.*

(at MTL/IQS LLC, Marlborough, MA)

iii.) Test Equipment Used

The test equipment used during the Performance Test phase is shown in Figures A18 through A22. The majority of the waveform data captures were made directly on the ETM Control Board via the test point stake pins. The remainder of the performance measurements (AC voltage, AC current, Power Factor, etc.) were made on the external connections utility connections to the ETM Prototype, using the Fluke Model 434 Power Analyzer, as shown in Figure A23.

Figure A18. *Tektronix Model TDS5054B Oscilloscope.*

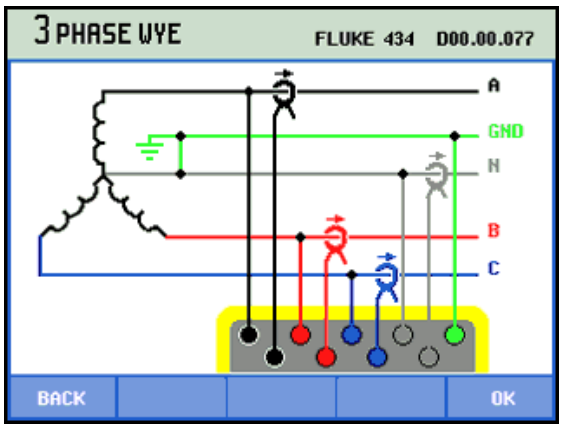
Figure A19. *Tektronix Model AM503 w/A6303 Current Probe.*

Figure A20. *Fluke Model 434 Three Phase Power Analyzer.*

Figure A21. *Fluke Model 87 Digital Multimeter.*

Figure A22. *Compaq Presario 3045US Laptop Computer.*

Figure A23. *Test Connections For The Fluke Model 434 Power Analyzer.*



B.) ETM Converter Host GUI Interface Description

The ETM Converter Host GUI Interface resides on a host PC used to set the operational parameters of the ETM Converter. The GUI Interface is necessary because the ETM Converter is a totally microprocessor/DSP-controlled power system. It does not have a hardware-based set point for operation or an inherent hardware-based mode of operation. The operation of the Converter is controlled by firmware code, downloaded to the Converter via the host PC and natively resident in non-volatile memory in each of the DSP microcontrollers used. The GUI Interface is used to set the variable parameters within the firmware code, which determine the operating points of the Converter in its application. Within the framework of the fixed firmware code utilized by the Converter, the GUI parameters can be thought of as "personalizing" the Converter. Because of this functionality, the ETM Converter may truly be considered a "Power Computer"!

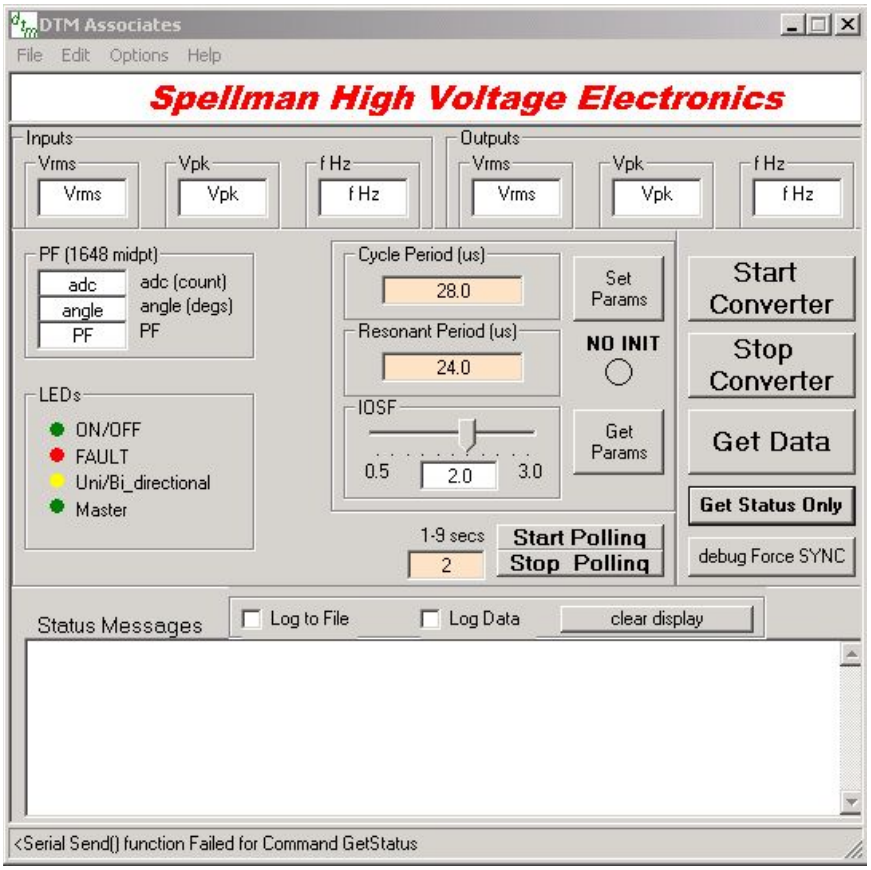
The ETM Converter Host GUI is written in Visual Basic, and it communicates a set of data parameters via an external RS-232 serial data link between the host PC (the laptop) and the ETM Converter Control Board within the Converter (ultimately communicating with the dsPIC30F6011 DSP microcontroller device). The GUI allows for the bidirectional exchange of data between the host and the Converter. Data parameters (Tres, Tcyc and IOSF values) controlling the Converter pass from the host PC to the ETM Converter and operating parameters (I/O frequencies, I/O voltages, the firmware-resident values of the previously-described data parameters, microcontroller status information and general Converter fault/status information) are passed from the ETM Converter to the host PC. The GUI Interface also allows for data logging and capture while the ETM Converter is operating.

Finally, the GUI Interface acts as the ON/OFF "softkeys" for the ETM Converter, as the ONLY way to turn the converter on and off is via the host GUI software; there are no mechanical ON/OFF switches on the ETM Converter housing. This is done to make the ETM Converter as autonomous as possible – once personalized for the particular application, the converter is started (turned ON) and left to operate until grid conditions or an internal fault cause the converter to shut down (i.e. go "off line"). This means the ETM Converter may be controlled or personalized from a physically remote location.

i.) ETM GUI Parameter Discussion

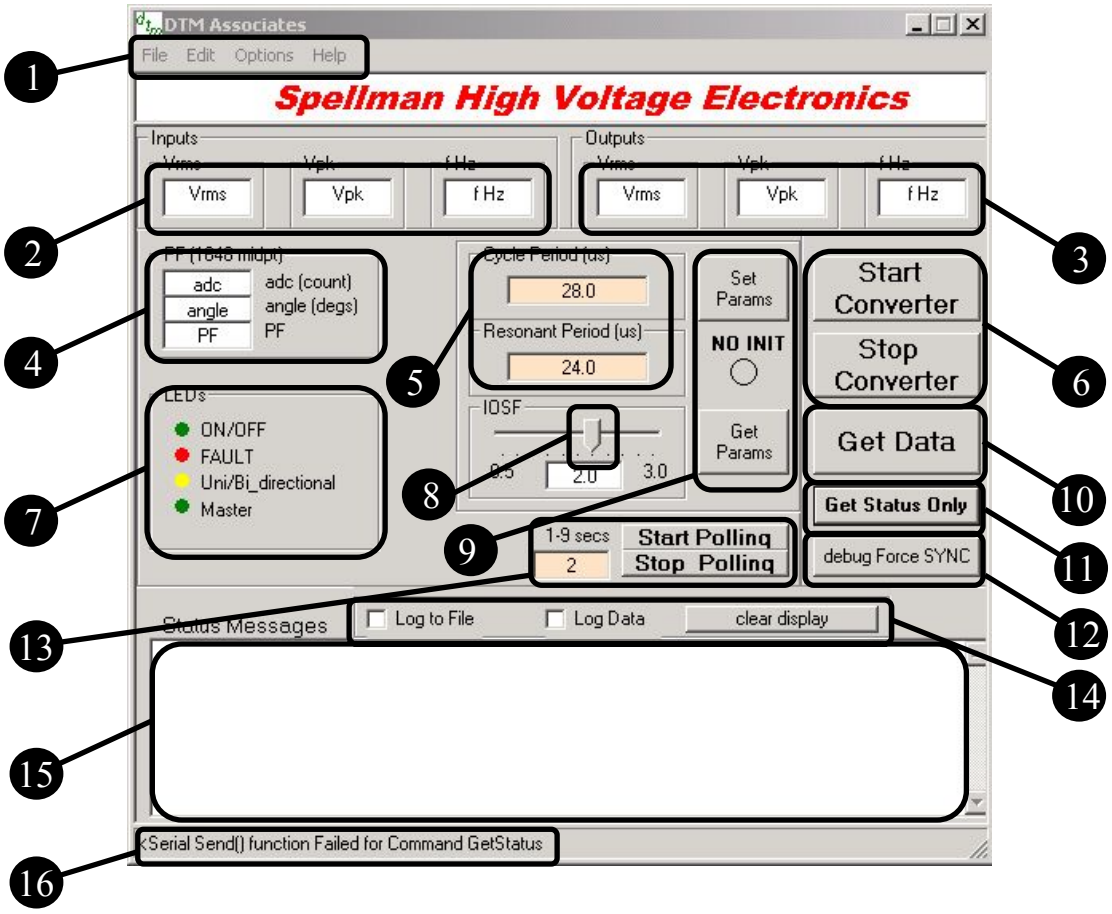
A screens shot of the main GUI Interface screen is shown in Figure B1.

Figure B1. *ETM Converter Main GUI Control Interface.*



This interface is the main data entry and retrieval location for the host PC. The various functionalities of this Interface window are shown in Figure B2.

Figure B2. *ETM Converter Main GUI Control Interface Functional Descriptions.*



The operation of the individual numbered function blocks is detailed as follows.

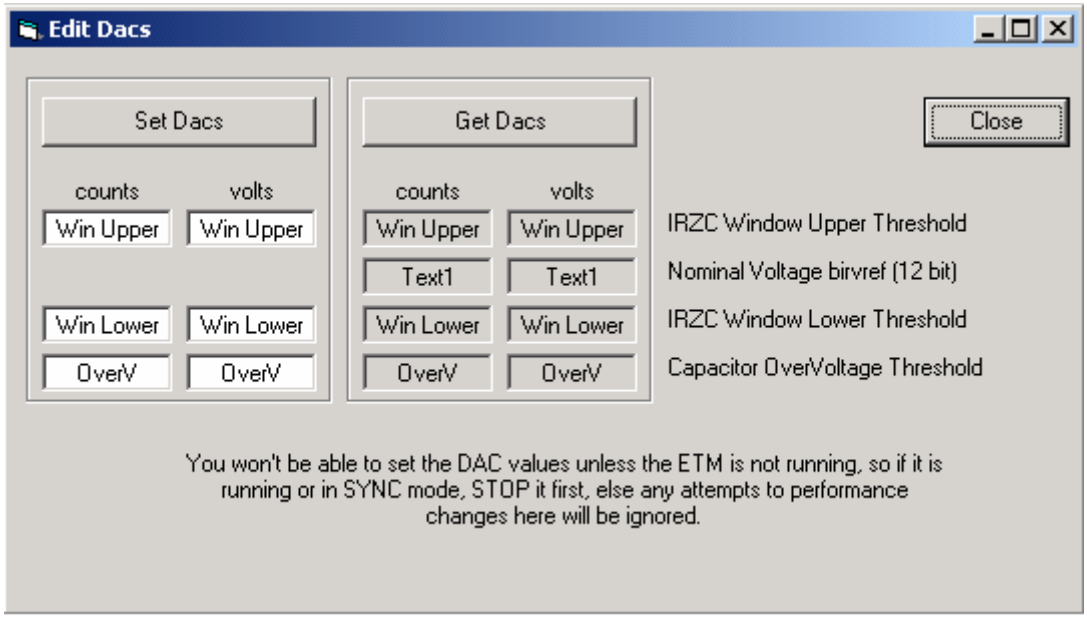
1. **Submenu Action Menu:** This menu allows for the selection of the various submenus available for parameter setting and debugging.
    a. *File:* Allows the User to dismiss/shut-down the GUI.
    b. *Edit:* Allows the User to set the values of the IRZC (current zero-crossing detector) upper and lower limit DACs and clear their values.
    c. *Options:* Allows the User to set the properties of the RS-232 Comm Port on the Host PC.
    d. *Help:* Unused at present.
2. **Input Parameter Display:** Allows the User to view the actual operating ETM Converter input voltage and frequency. In future revisions, input current is planned to join this list.

3. **Output Parameter Display:** Allows the User to view the actual operating ETM Converter output voltage and frequency. In future revisions, output current is planned to join this list.
4. **Power Factor (PF) Parameter Display:** Allows the User to monitor the input power factor and phase angle of the Phase A input (which is representative of all three phase inputs).
5. **Resonant and Cycle Time Parameter Input Areas:** Allows the User to enter the desired Resonance Time (Tres) and Cycle Time (Tcyc) into the input boxes.
6. **Start/Stop Converter "Softkeys":** These are the only means for the User to start and stop the ETM Converter. Once the Converter is started, it can only be stopped via the "Stop Converter" softkey.
7. **Front Panel LED Status Indicators:** This display area allows the User to view the status of the operating ETM Converter.
8. **IOSF Parameter Value-Setting Slider Bar:** This slider bar may bet set by the User to select the optimum IOSF parameter value during the debug phase. This control is not planned to be included in production ETM GUI displays, as this value will be hard-coded into the firmware.
9. **Set Params/Get Params Softkeys and NO INIT Indicator:** At the initial Converter start-up/turn-on, the NO INIT indicator flashes RED to indicate to the User that the values displayed in the Cycle Period and Resonant Period input boxes on the GUI may not agree with the values stored in the non-volatile memory (NVM) in the ETM Converter. The ETM Converter may not be started by the User while this indicator flashing persists – the Start Converter softkey is disabled. The indicator is extinguished by the User by placing the desired values into the Cycle and Resonant Period input boxes and then clicking the Set Params softkey. This action stores the values entered on the host GUI to be saved in the NVM of the ETM Converter. Once the Tres and Tcyc values have been set via the Set Params softkey, they may be retrieved from the Converter NVM by the User at any time in the future using the Get Params softkey. Once the Set Params softkey has been clicked, the converter may be started using the Start Converter softkey.

10. **Get Data Softkey:** Allows the User to retrieve real-time data from the ETM Converter. This data is the I/O voltage and frequency, which are displayed in the data boxes shown in 1. and 2., as previously described.
11. **Get Status Only:** Allows the User to retrieve the status of the dsPIC and ADSP microcontrollers in the ETM Converter. This status information is displayed in the Status Message Window Area as shown in 15 in Figure B2 and described in 15., following.
12. **debug Force SYNC:** Allows the User to manually force the GUI-to-ETM Converter serial interface communications to synchronize. This is used only in those debug testing situations where the serial communications are observed to be disrupted.
13. **Start Polling/Stop Polling Softkeys and Value Display Area:** Allows the User to continuous monitor the I/O parameters shown in 1 and 2 and the Status Messages as shown in 15 of Figure B2. This is a useful feature for debug activities and remote troubleshooting.
14. **Log to File/Log Data Action Check Boxes and Clear Data Softkeys:** Allows the User to capture and save the ETM Converter debug or operating data to a Log File (i.e. “logfile.txt) or to continuously log data to the Status Messages area as shown in 15 of Figure B2. The Clear Data Softkey allows the User to clear the Status Messages area of all data and status messages.
15. **Status Messages Display Area:** Allows the Use to view the real-time status messages received from the dsPIC and ADSP micontrollers in the ETM Converter, or to view the real-time data retrieved from the Log Data function of the GUI as described in 14., previously.
16. **Command Line Display:** allows the User to view the last command executed by the GUI as well as the direction of the information exchange. A “<” character preceding the command indicates that it was executed from the ETM Converter to the GUI, and a “>” preceding the command indicates that it was executed from the GUI to the ETM Converter.

When the Edit Submenu is selected and the DACs option is chosen, the display box shown in Figure B3 is displayed:

Figure B3. *ETM Converter DACs Submenu.*

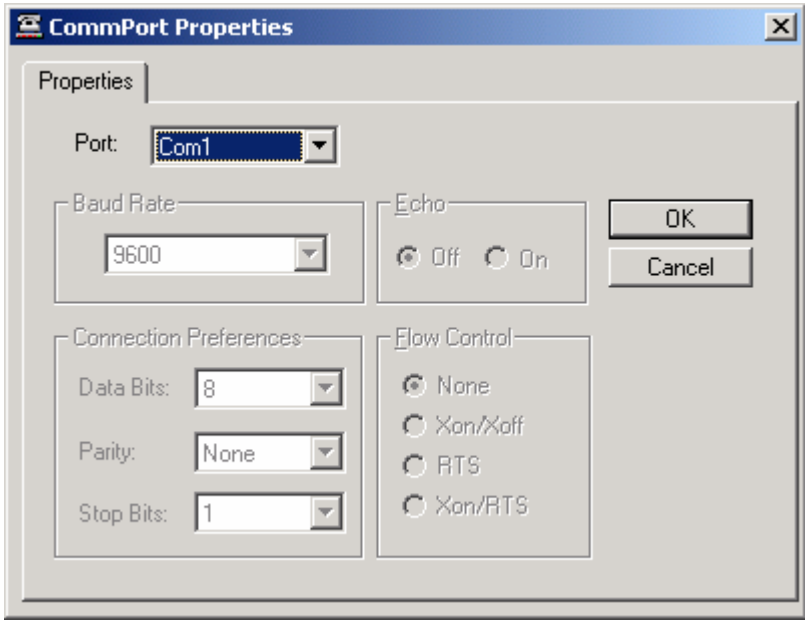


The operation of the individual functions for the Edit DACs window is detailed as follows:

1. **Set DACs:** This softkey allows the User to enter the DAC threshold information contained in either the "counts" or "volts" data boxes for the threshold point descriptions shown on the right side of the window. The upper two data boxes set the upper and lower IRZC thresholds for the zero crossing window detectors. The lower data box sets the threshold for the resonant capacitor over voltage threshold. These values may only be set if the ETM Converter is stopped.
2. **Get DACs:** This softkey allows the User to retrieve the information stored in the NVM of the ETM Converter. The values retrieved are displayed in the data boxes just beneath this softkey. It is always recommended to perform a "Get DACs" command after a "Set DACs" command is executed.

When the Options Submenu is selected and the CommPort Properties option is chosen, the display box shown in Figure B4 is displayed:

Figure B4. *ETM Converter CommPort Properties Submenu.*



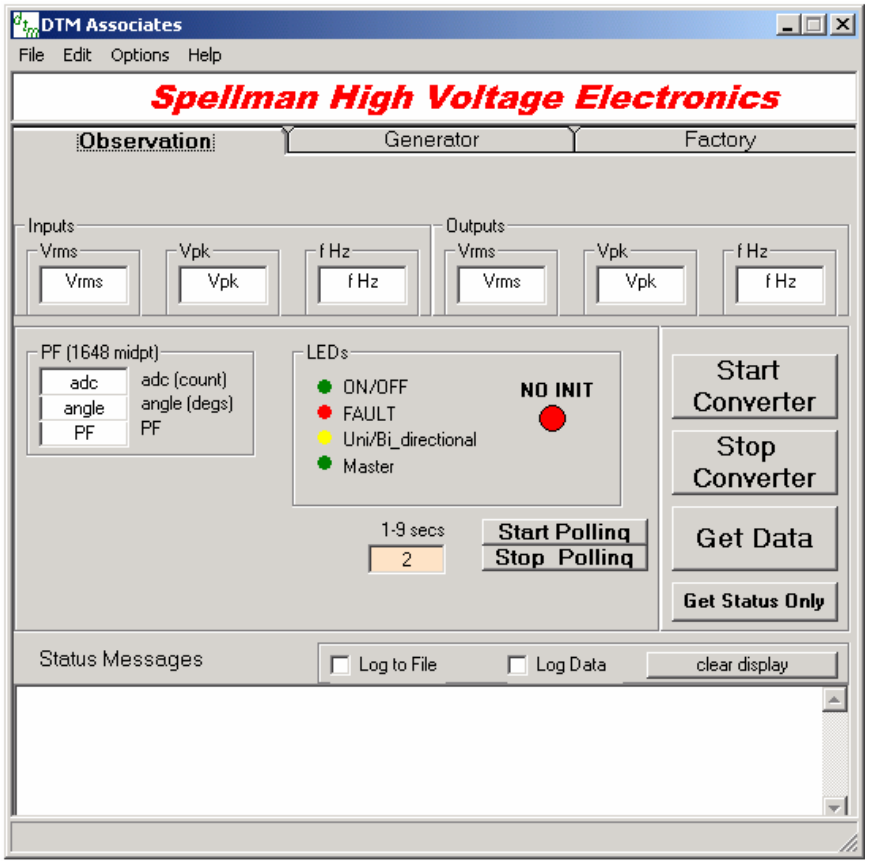
This submenu allows the user to choose the serial Com Port for communications with the ETM Converter. The remaining parameters are "greyed-out" at the default conditions that are compatible with the internal RS-232 interface of the ETM Converter.

ii.) Planned Enhancements to the ETM Converter Host GUI Interface

The host GUI interface was envisioned to undergo a sweeping change to make it more amenable to setting up the Converter for operation in an intended end-application. As such, there would be two distinct modes of operation for the GUI: the first would be to enable a User to perform cursory debugging and threshold set point functions; and the second is to perform the "personalization" of the Converter – setting voltage and frequency operating ranges and allowing for the input of the parameters as described in the "ETM Converter Programmers Guide". Thus the GUI would have two natures, making it more user-friendly and intuitive in its functionality.

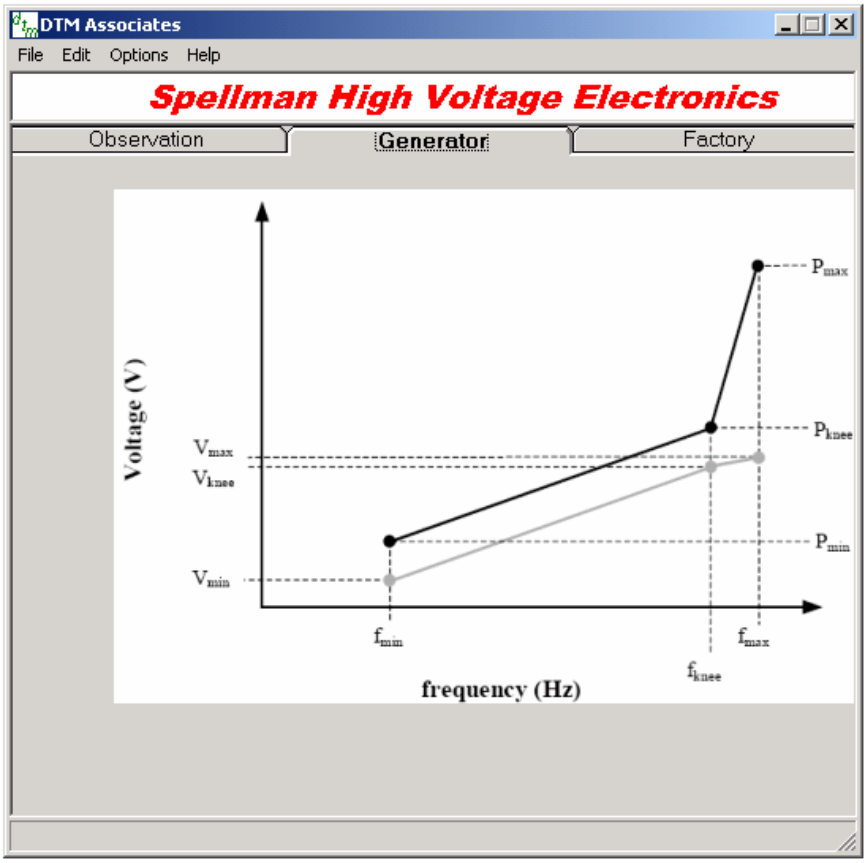
A screenshot of the improved GUI is shown in Figure B5.

Figure B5. *Proposed Improved ETM Converter Host GUI, "Observation".*



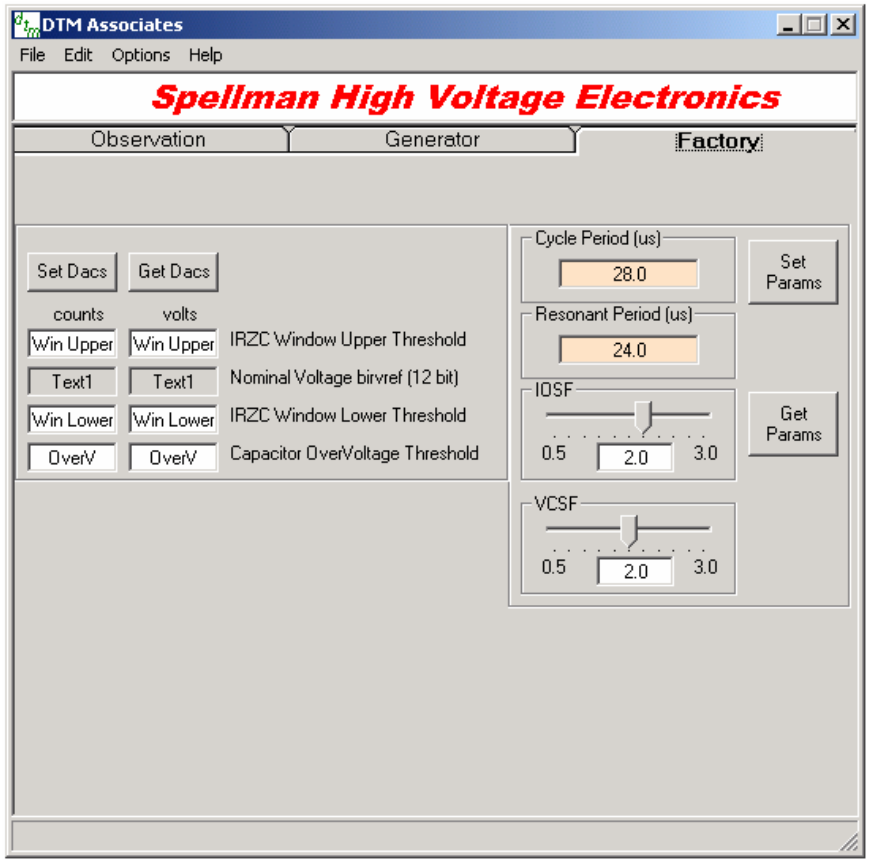
This screen, tabbed "Observation", will provide the means for monitoring the performance of the operating ETM Converter.

Figure B6. *Proposed Improved ETM Converter Host GUI, "Generator".*



This screen, tabbed "Generator", will provide the means for the User to personalize the ETM Converter to the wind turbine generator in the end-application.

Figure B7. *Proposed Improved ETM Converter Host GUI, "Factory".*



This screen, tabbed "Factory", will provide the means for the Spellman HV to set the operating parameter of the ETM Converter, matching the firmware to the actual hardware performance. This tab will probably be password-protected as once these values are set at the factory, there is never the need by the User to reset or change them in the future.

C.) Summary of Test/Debug Activities

The system-level debug and test activities for the 34kW ETM Converter prototype took place from September 1, 2004 until March 20, 2005. This time coincides with the successful power-on of the ETM prototype and continued until the funding for the project ran out.

i.) Initial Power-Up/Debug Testing (9/1/04 to 10/21/04)

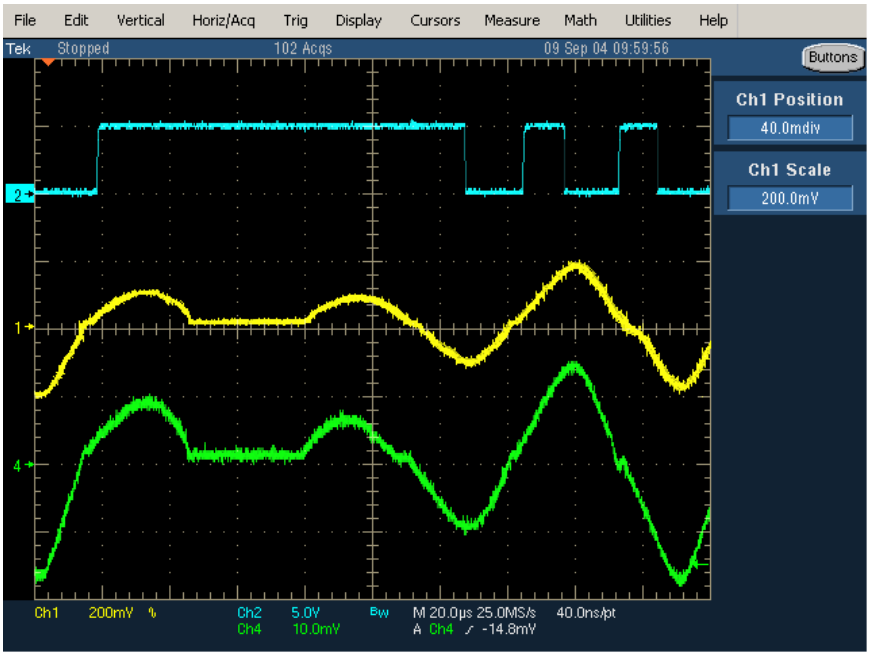
The initial power-up/debug testing commenced on September 1, 2004. These activities included the instrumentation of and then the powering-up of the ETM prototype at a greatly reduced input/output voltage level in order to observe and verify the key operating voltage and current waveforms in the circuit, and functional operation according to the "ETM Converter Programmers Guide".

For the initial power-up, the input and output voltages were set at $75V_{L\text{-}N}$ ($130V_{L\text{-}L}$). The test points for the resonant current (IRMAG_SIGN), the resonant crossing zero crossing (IRZC) and the resonant capacitor voltage (VRC) on the ETM Control Board as well as the direct measurement of the resonant current by current probe were monitored with a four channel oscilloscope. These points were initially monitored for any activity and close-too-normal operational waveforms, as well as for any abnormal, unexpected or transient behavior. A typical set of waveforms captured during this initial testing is shown in Figure C1.

This testing revealed that an excellent replica of the resonant current was obtained from the current transducer in the ETM Converter and this signal was further faithfully transmitted to the analog portion of the ETM Control Board. Figure C1 does demonstrate one of the debug issues encountered with the prototype at initial power-up: the fact that sense threshold of the current zero crossing signal was set too high (it can be seen that the first three low amplitude current zero crossings were "missed" by the IRZC detection comparator) and that the thresholds would need to be adjusted lower with a firmware change.

Data was collected to observe the typical operation of the converter in comparison with the expected operation, for example these reports: "Report #1", "Report #2" and

Figure C1. *IRZC, IMAG_SIGN and Measured Resonant Current Waveforms.*



"Report #3", and this information was shared with the software/firmware programmers for their analysis and input. Additionally, if any abnormal or unexpected operating behavior was observed, then this data was captured in a report and analyzed for the root cause. Typical of this activity is the report titled "Four Cycle Hiccup Mode", which details an unexpected resonant transfer event during the observed ETM prototype operation. Again, this data was shared with the software programmers for review analysis and action.

After minor revisions were made to the ETM Control firmware to correct the observed problems, the input/output (I/O) voltages were increased to $100V_{L\text{-}N}$ and then to $150V_{L\text{-}N}$. At both these I/O points, the circuit was observed to be operating normally. It was at the $150V_{L\text{-}N}$ operating point that an IGBT failure in the output switch matrix occurred. The ETM Converter prototype had operated more than five cumulative hours when the failure occurred. This failure, suspected to have been a random failure in a single IGBT, had the effect of damaging all four IGBTs in the output switch matrix (the three phase output and the ground switch devices), requiring their replacement for continuance of the testing. [Luckily there were four spares of the IGBTs and driver

boards remaining/available from the ETM Converter prototype build for the necessary repairs to be accomplished!]

With the repairs accomplished, the prototype Converter was again subjected to the $75V_{L-N}$ I/O voltage test value in order to test the efficacy of the repairs. Unfortunately, after approximately 30 seconds of operation, the prototype Converter experienced another IGBT failure both the input and output stages. It was determined that a total of four (4) IGBTs were destroyed before the internal circuit breaker tripped. These failures necessitated the ordering of replacement IGBTs (in a quantity sufficient to support the remaining testing) and incurred a ten week lead time before their receipt.

Although replacement IGBTs had been ordered, after significant searching activities it was determined that four IGBTs that were of a similar device type were found in the UK, these devices were obtained, the driver boards were repaired and the ETM prototype was ready for test once again.

Once again, with the repairs accomplished, the prototype Converter was again subjected to the $75V_{L-N}$ I/O voltage test value in order to test the efficacy of the repairs. This time, the Resonance Period time was set to 26.5 microseconds (the actual resonance time was determined to be 26us from previous measurements, see Figure C1) and the Cycle Period time was set to 28us. This action was performed to bring the firmware timing in line with the actual circuit performance. If this action were not done, there would be significant current flowing in the IGBTs when turning OFF depending upon the mismatch of the firmware resonance time and the hardware resonance time. It should be noted that the ETM Converter is by-design a zero current switching power converter, and to avoid excessive switching stresses and safe operating area (SOA) excursions the switches must open at or very near zero current.

Figure B1 demonstrated that the current zero crossing detector had a “dead spot” for lower magnitude resonant currents (measured to be less than 15A), so that it was critical that the firmware possess an accurate cycle time in light of the missing IRZC (zero crossing) signal. It was determined that the software allowed for a condition whereby a fixed resonance time IGBT switching event could not be guaranteed in the absence of the IRZC signal, and this condition existed during testing after the first failure

repair. It is believed that this software bug relating to resonance timing and switching caused the second failure observed during the debug testing.

However, at the power-up of the repaired ETM prototype, the internal circuit breaker tripped and it was determined that all four IGBTs in the input switching matrix were damaged. It was determined that this failure was caused by the fact that although a change in the Cycle Time or Resonance Time may have been accomplished via the GUI, there was no confirmation or update of the GUI parameters. Additionally, it was determined that there was no guarantee that the parameter data was properly exchanged between the host laptop and the dsPIC/ADSP microcontrollers in the ETM Converter after a change was initiated. The reason the particular failure occurred was that a value of 15us was somehow entered as the value of the Cycle Time, Tcyc. With this value, the IGBT switches would have been forced to open while carrying their maximum resonant current. This action subjected the switched IGBT to stresses exceeding their maximum ratings. This is a grievous flaw, and was immediately corrected with a revision to the GUI software and the microcontroller firmware to signal (as an indicator on the GUI) that matching values did not exist in microcontroller memory and in the GUI value registers.

The last failure encountered guaranteed that there would be a ten to twelve week hiatus in testing while waiting for the replacement IGBTs to arrive. It was decided to use this time as an opportunity to re-design and replace the resonant inductor in the ETM prototype. Observation of individual high current resonant pulses indicates that the shape of the pulse is not a true sinusoid, as expected. Rather, the actual pulses exhibited inward-tapering edges. This waveshape indicated nonlinearity in the magnetic material used, or an inadequate core size (see Figure C2). A new inductor was specified, procured and installed in the ETM prototype prior to the receipt of the IGBTs. The improved inductor is shown in Figure B3 and installed in the ETM prototype in Figure C4.

Figure C2. *Nonlinear Resonant Current Pulse.*

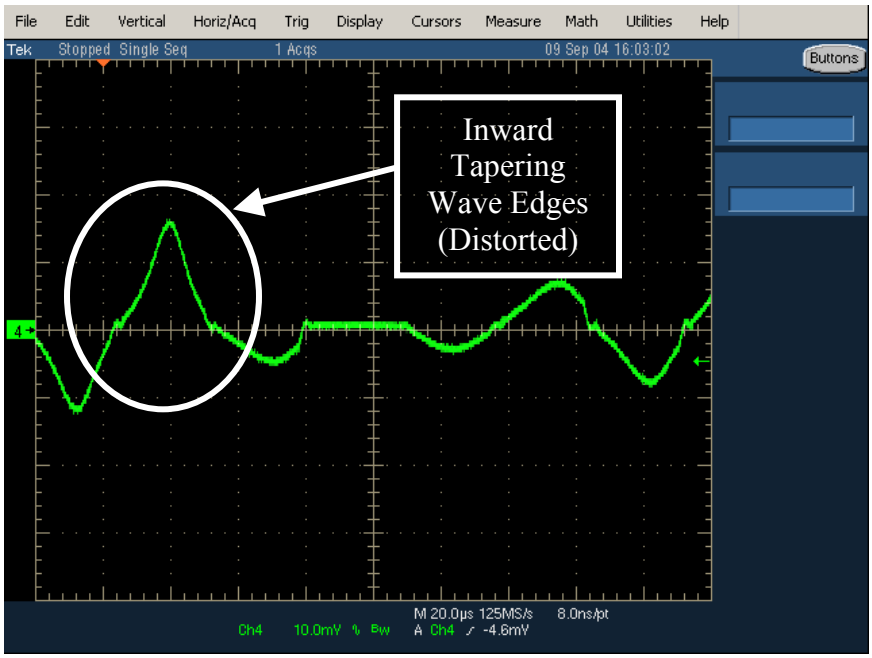
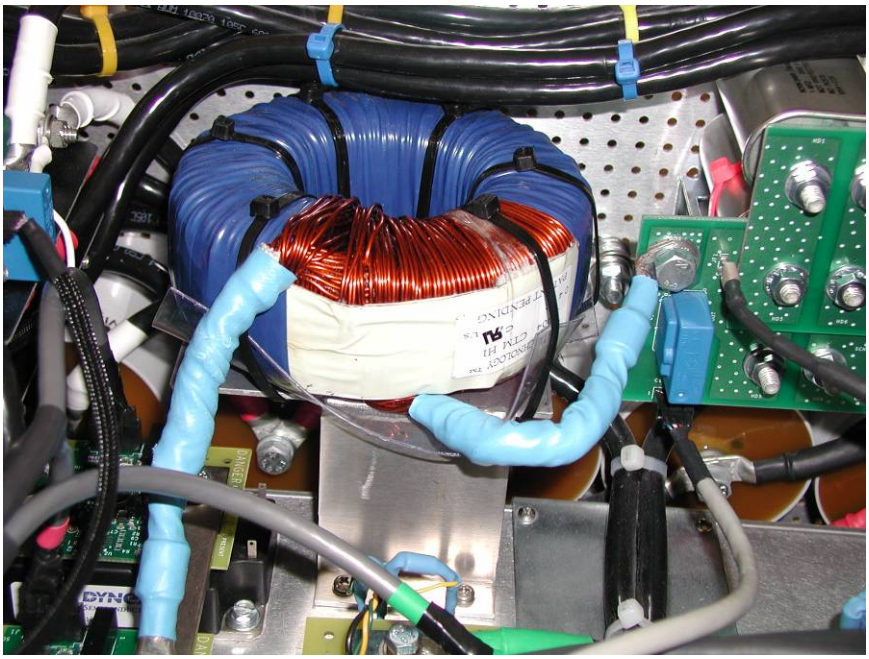


Figure C3. *Improved Resonant Inductor.*

Figure C4. *Improved Resonant Inductor Installed In ETM Prototype.*



Before any further testing commenced after the IGBT failure repairs, it was decided to lower the power train resonance from the observed 26 microseconds to the design goal of 20 microseconds by connecting an additional 1uF resonant capacitor in parallel to the to the existing capacitors to increase the overall value (see Figures B5 and B6). With the new inductor (Lr = 36.2uH, measured) and the modified capacitor (Cr = 1.49uF, measured), the power train resonance was calculated to be 23.1 microseconds.

Finally, during the initial debug test period, there were numerous minor changes made to the values of components on the Analog and Digital ETM Control Boards in order to fine tune performance (e.g. filter breakpoints), improve performance (higher slew rate amplifiers) or add additional power supply bypassing, as observed during the debug test cycle. Coinciding with the hardware changes were several firmware changes to optimize the conversion algorithm and switch-state sequence table, as well as a makeover of the GUI interface to add adjustability for the parameter IOSF and improvements in the data gathering and subsequent display of the phase voltage/frequency operating parameters.

Figure C5. *Increased ETM Power Train Resonant Capacitance.*

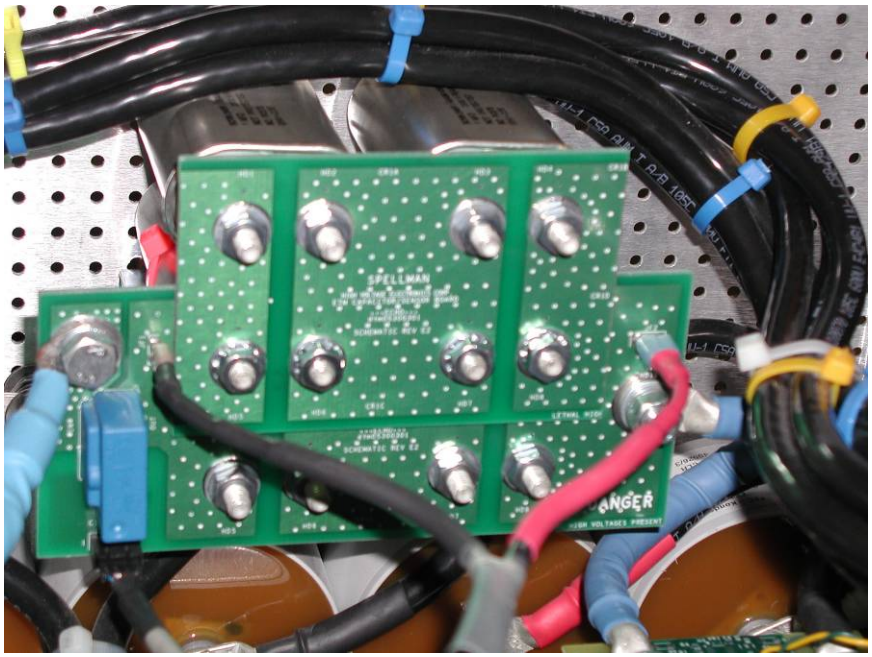
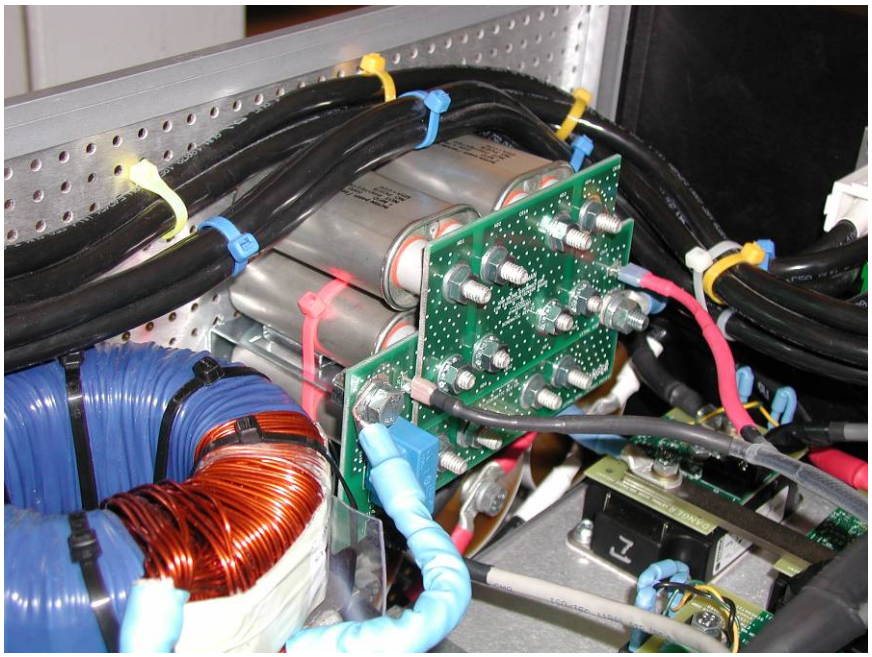


Figure C6. *Increased Resonant Capacitance In The ETM Converter Prototype.*



ii.) Performance Testing (12/23/04 to 3/10/05)

After the repairs to the IGBTs and the revisions to the ETM Control Board from the last set of hardware failures, it was determined that the hardware and firmware were robust enough in operation to support the commencement of performance testing. The test philosophy adopted was to start the performance testing at low I/O voltages ($75V_{L-N}$) and then increase the amplitude(s) in 50V steps until the design value of $230V_{L-N}$ ($400V_{L-L}$) is achieved. The actual resonance time was measured and found to be 21.5us (as opposed to the calculated 23.1us), and the GUI control parameters were set accordingly.

The testing was commenced and it was immediately noticed that there was a higher level of audible noise from the resonant inductor, as well as the fact that the ETM prototype would shut down at random after operating at random intervals from 60 seconds to 10 minutes. Once shut down, the prototype would remain latched off. This behavior was radically different from that noted before the repairs and revisions were accomplished. There are several events that can shut down the converter, not the least of which is an over voltage event on the resonant capacitor. This is the primary hardware event (that was not disabled for debug/test purposes) and as a result the differential capacitor signal VRC was monitored along with the resonant current signal IRMAG_SIGN on the ETM Control Board. Typical waveforms observed on the VRC and IRMAG_SIGN signals are shown in Figures C7 through C12.

Figure C7. *Resonant Signals VRC (green) and IRMAG_SIGN (yellow).*

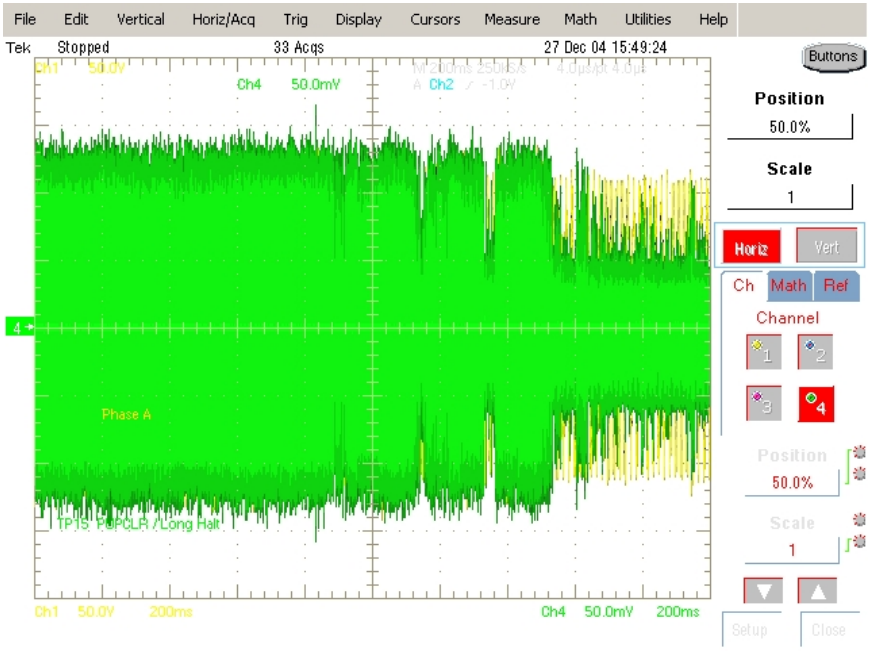


Figure C8. *Resonant Signals VRC (green) and IRMAG_SIGN (yellow).*

Figure C9. *Resonant Signals VRC (green) and IRMAG_SIGN (yellow).*

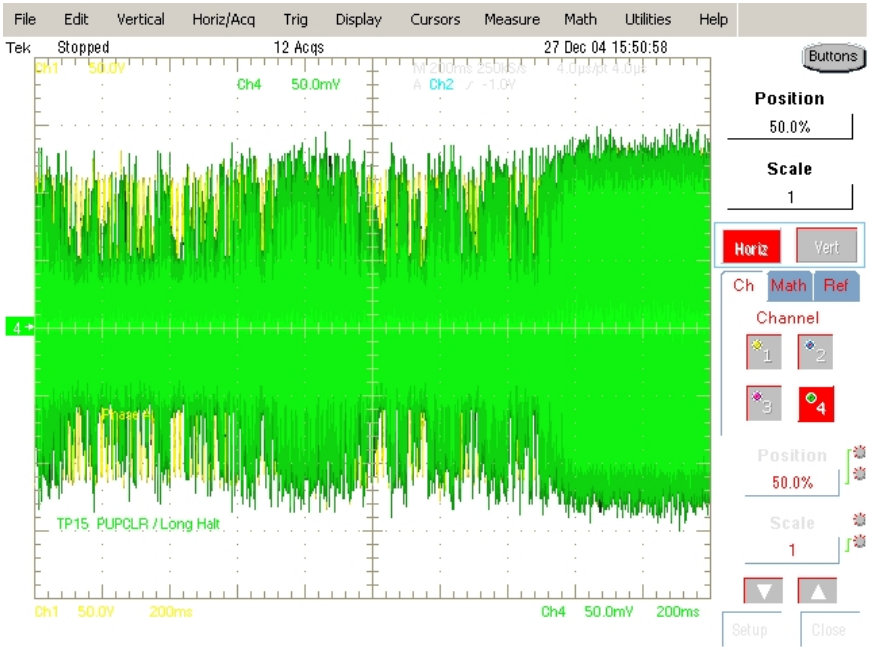


Figure C10. *Resonant Signals VRC (green) and IRMAG_SIGN (yellow).*

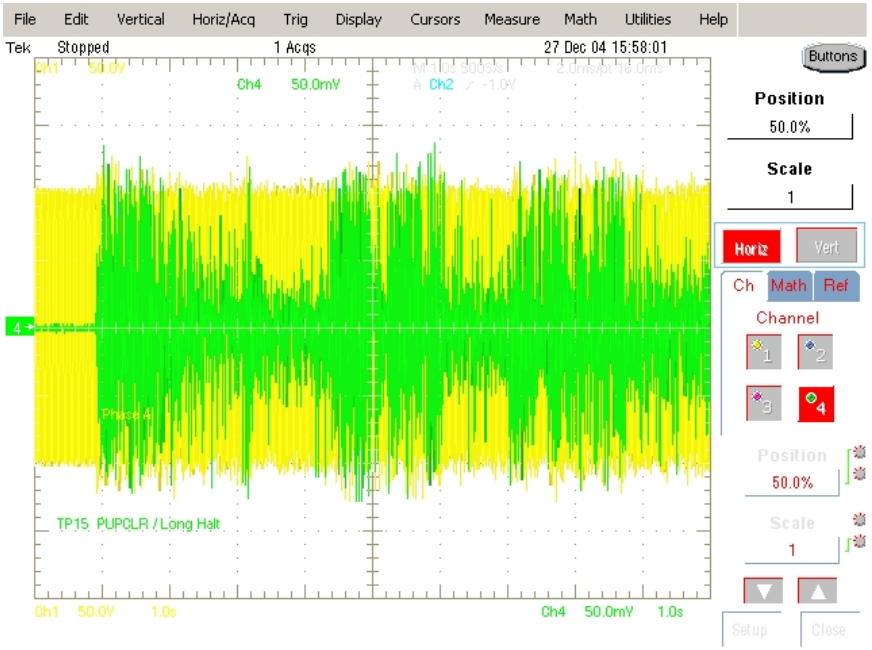


Figure C11. *Resonant Signals VRC (green) and IRMAG_SIGN (yellow).*

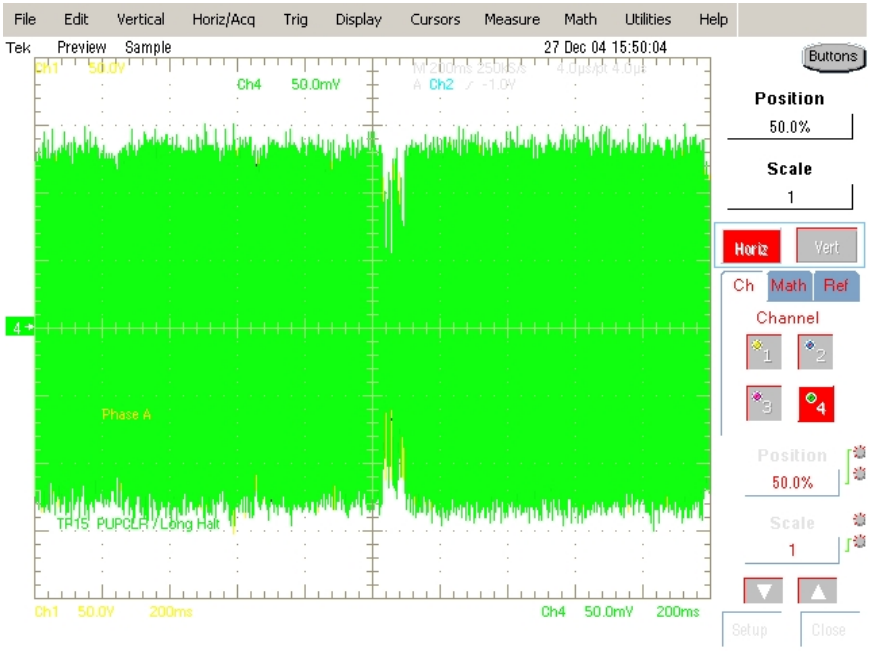
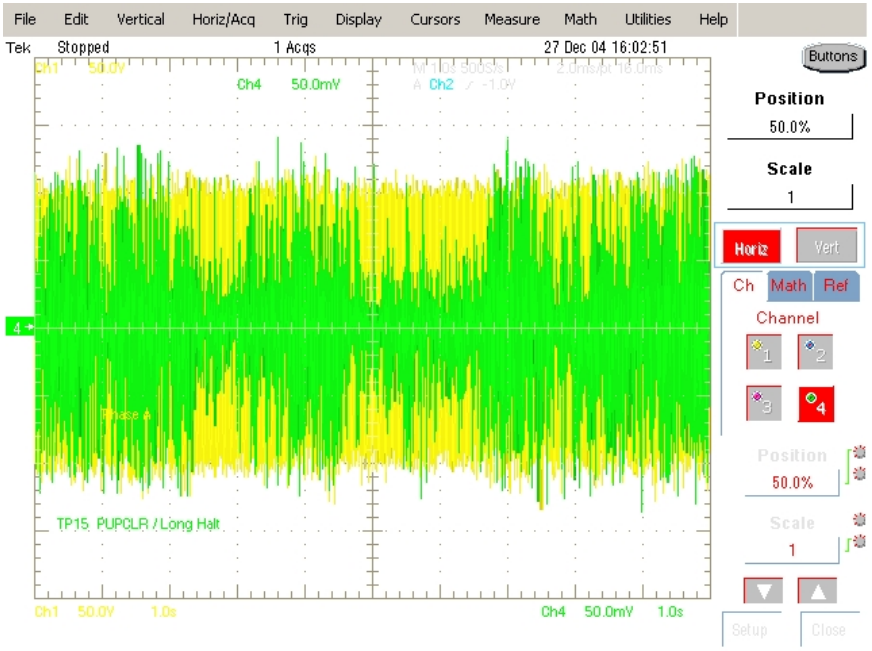


Figure C12. *Resonant Signals VRC (green) and IRMAG_SIGN (yellow).*

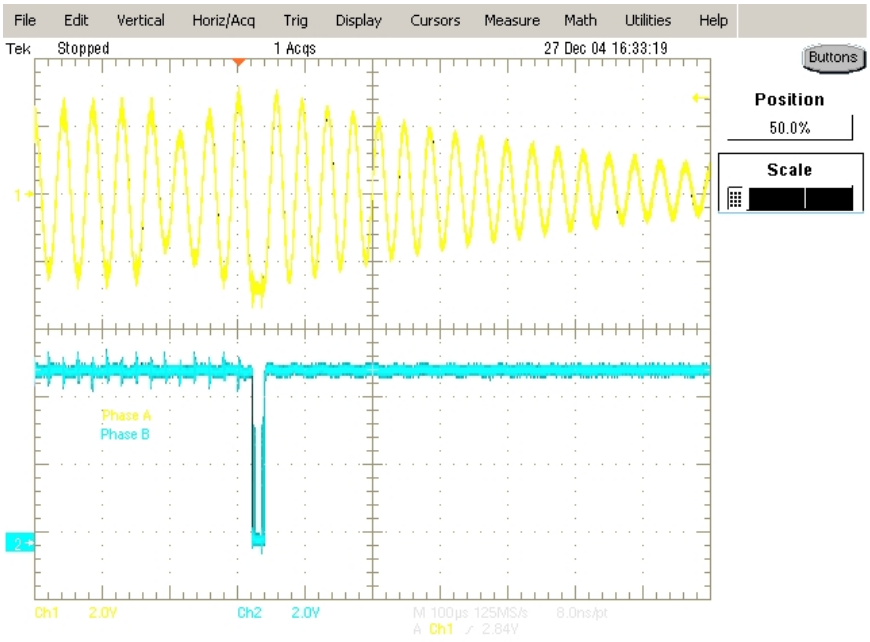


The one common characteristic of all these traces, taken at random times, are that they are inconsistent. During normal ETM Converter operation, one would expect to see a capacitor voltage and an inductor current that were reasonably stable in amplitude (in the

time scale shown of one second per division) with few random positive or negative amplitude fluctuations. This is obviously not the case! Figures C7 through C12 embody the behavior dubbed “breathing”, whereby the resonant capacitor voltage and resonant current took on a random, amplitude modulated appearance with time. It was this breathing phenomenon that was responsible for the very much increased audio noise from the resonant inductor. After considerable troubleshooting, the breathing phenomenon could not be attributed to a hardware bug or issue.

Furthermore, the latch off problem was highly inconsistent and very annoying. To determine where this behavior was originating, the signal VRC_OV_N (a negative-going signal indicating that the resonant capacitor has exceeded the firmware-set voltage threshold value of |1500V|) was monitored. The waveform, shown in Figure C13, shows that this level had indeed been exceeded by the presence of the negative-going pulse on this signal.

Figure C13. *VRC_OV_N Signal Actuation Event.*



In Figure C13, the yellow trace is the differential resonant capacitor voltage signal VRC and the blue signal is the resonant capacitor over voltage fault signal VRC_OV_N.

This condition (VRC_OV_N pulse) should have never existed by virtue of the operating algorithm – the converter will (should) ignore (i.e. "pass on") current transfer opportunities that would result in a final capacitor voltage of greater than |1500V|. The detection circuitry and signal were included solely as a fail-safe mechanism for the detection of a hardware failure or fault that existed in the ETM Converter, and quickly shut it down before damage may be propagated.

After two days of intensive troubleshooting and data analysis with the software developer (TechEn, Inc.), it was finally determined that the ADSP microcontroller was out of "real time" – that is that the required time to execute the software exceeded the Cycle Time (set at 23.5us) required for the ETM Prototype. The reason why this problem came to light after the last repair of the Prototype due to the fact that the resonance time was set to 21.5 microseconds (23.5us by calculation). With the 2us dead time added to this value, the Cycle Time became 23.5us. The difference of 4.5 microseconds between the original Cycle Time setting of 28us and the new value of 23.5us was enough to consume any real time software execution time buffer that may have existed. The reason that the breathing and the random resonant capacitor over voltage events existed was the fact that for certain code executions, times greater than the cycle time were required and were thus prematurely truncated without proper software flow and resolution. The result was random, unpredictable operation with the observed fluctuations in resonant capacitor and resonant current amplitudes. The ETM Converter simply will not work properly if there is not sufficient time for the microcontrollers to execute the software code and "think".

There were two solutions to this problem; an expedient solution that would allow testing to continue, and a longer-term solution that involved optimizing the software/firmware in the ADSP microcontroller to reduce the execution time to below 20 microseconds (to allow for a code execution safety margin). The expedient problem solution was determined experimentally – the Cycle Time was increased until the ETM Prototype began to function as was expected. This time was increased in 0.2 microsecond steps from the 23.5us value until no breathing or shutdown phenomena were encountered. This occurred at 24.2us – so the Cycle Time was set to 25us to add a safety margin for the remainder of the testing. This action is not without consequence; as the maximum power

available from the ETM Prototype will drop from 34kW to approximately 31kW. But this decrease in power would only temporarily exist until the software code was optimized to reduce the execution time to below 20us by converting time-consuming C code routines into corresponding functionality ADSP native assembly code.
For a more detailed description of this problem and the eventual solution, please refer to the document "34kW ETM Converter Prototype Project Status".

So, with the Cycle Time set to 25us, the performance testing was restarted. Data was gathered for the operating ETM Prototype at several different I/O operating voltages, including: Phase Input power factor, voltage, current, and power; Phase Output power factor, voltage, current and power; and the effects of the variation of the parameters Tres, Tcyc and IOSF. During this testing process, there were several minor changes made to the GUI control software and the ADSP firmware to improve the ETM Prototype operating characteristics and its controllability from the GUI interface.

In particular, the output voltage was set to $145V_{L-N}$ ($250V_{L-L}$) and the input voltage was set to $70/80/90/100/110/120/145V_{L-N}$, with the aforementioned parameters recorded at each input voltage step. Additionally, at each input voltage step, Tcyc was varied from 25 to 55us and the parameter IOSF was varied from 1.0 to 3.0 to observe their effects on the operation of the converter. The data obtained for this range of I/O voltages is summarized in a following section.

Unfortunately, when the input and output voltages were increased to $200V_{L-N}$ ($\sim 350V_{L-L}$) and the power was turned on, the circuit breakers immediately tripped, indicating an internal fault. Upon troubleshooting the ETM Prototype, it was determined that all the IGBTs in the power train were damaged, along with their associated IGBT driver boards. Due to a number of different factors, the testing was halted at this point, and this was the state of the Prototype when the testing was terminated.

D.) ETM Prototype Test Data Summary

The ETM Converter Prototype test data collected during the Performance Test phase over the time period of 12/22/04 to 3/10/05, and is summarized in the following discussion.

i.) IOSF Versus Phase Current Magnitude

The parameter IOSF was varied over the range of 1 to 3 in 0.25 unit increments while observing the Phase Output Current. This was done to determine the transfer characteristic of the parameter IOSF in relationship to the I/O characteristics of the ETM Converter. It should be noted that this parameter directly controls a variable placed in the ETM Converter operational flowchart for the decision point "$E_I + V_{cs} > E_o$", which ultimately controls the window of resonant capacitor voltages which may be allowed to initiate a resonant current transfer from input-to-output. The IOSF range is an arbitrary analog of the multiplicand "1 * E_o" in the previous equation. This value of 1 was capable of being varied over a 3-to-1 range by varying IOSF from 1 to 3. This data is shown in Tables D1 and D2 and Figures D1 and D2.

Table D1. *IOSF VS Phase Current Magnitude (IOSF vs IO).*

IOSF	IO, Phase A (Arms)	IO, Phase A (Arms)	IO, Phase A (Arms)
1	1.7	4	6
1.25	2	4.4	8
1.5	2.4	5.1	9.6
1.75	2.7	5.8	10.8
2	3	6.6	11.5
2.25	3.2	7.1	12.2
2.5	3.2	7.5	12.7
2.75	3.2	7.8	12.9
3	3.2	8.2	12.9

Figure D1. *IOSF VS Phase Current Magnitude (IOSF vs IO).*

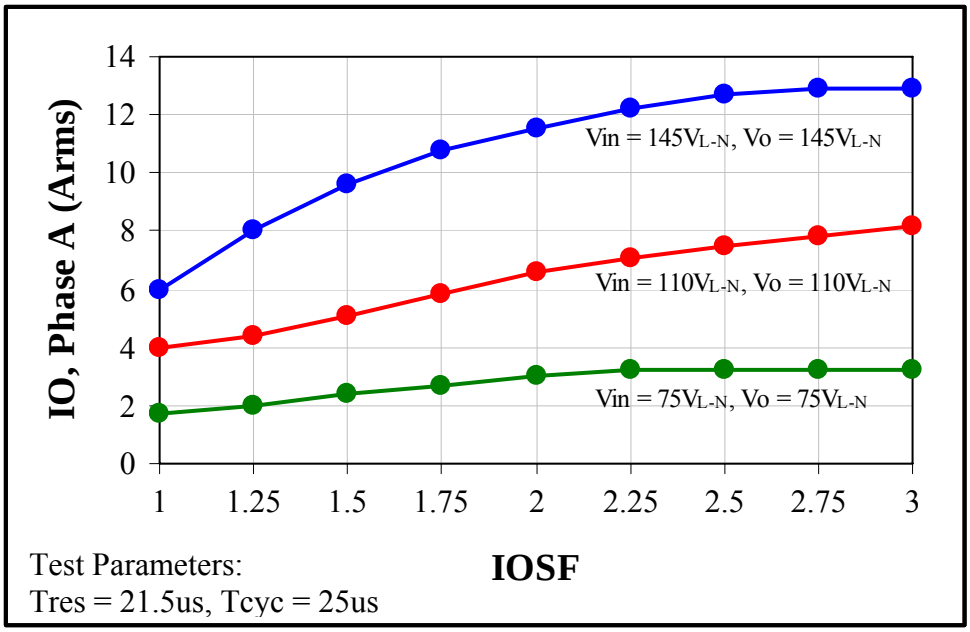
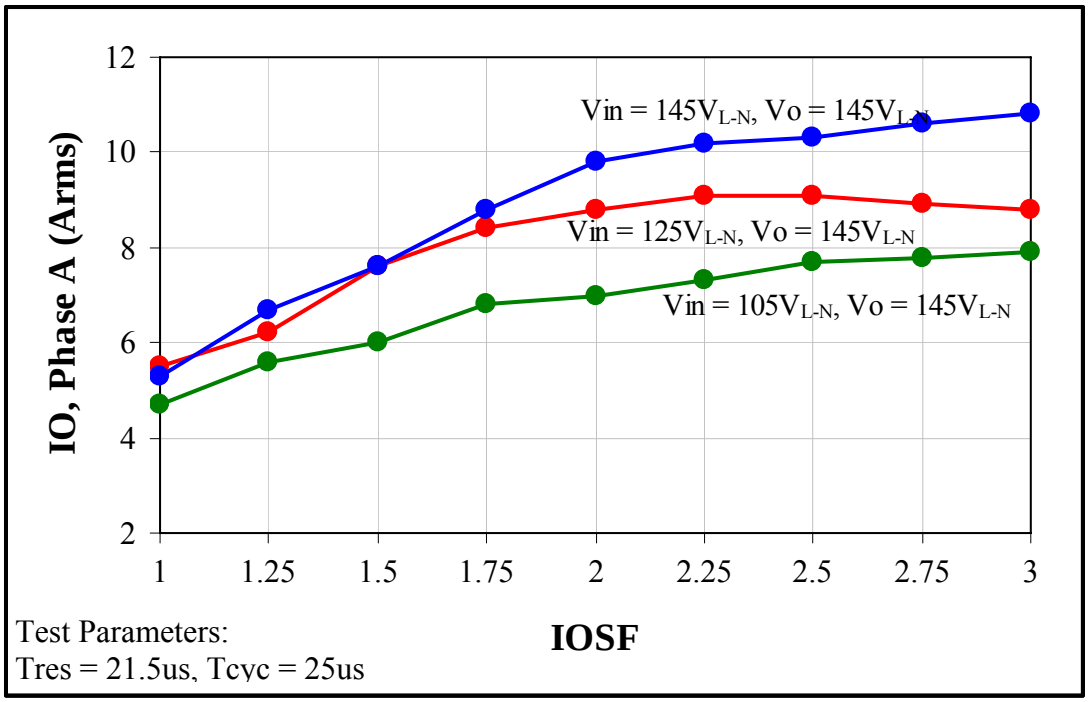


Table D2. *IOSF VS Phase Current Magnitude (IOSF vs IO).*

	Vout = $145V_{L-N}$		
	Vin =$105V_{L-N}$	Vin =$125V_{L-N}$	Vin =$145V_{L-N}$
IOSF	**IO, Phase A (Arms)**	**IO, Phase A (Arms)**	**IO, Phase A (Arms)**
1	4.7	5.5	5.3
1.25	5.6	6.2	6.7
1.5	6	7.6	7.6
1.75	6.8	8.4	8.8
2	7	8.8	9.8
2.25	7.3	9.1	10.2
2.5	7.7	9.1	10.3
2.75	7.8	8.9	10.6
3	7.9	8.8	10.8

Figure D2. *IOSF VS Phase Current Magnitude (IOSF vs IO).*



From the data gathered, it can be seen that there is a plateau level for the phase output current, for each setting of input voltage, at an IOSF value of 2.25. This makes sense, as the output current is expected to decrease as IOSF is decreased, because the ETM control loop will reject resonant current transfer events as the parameter is lowered.

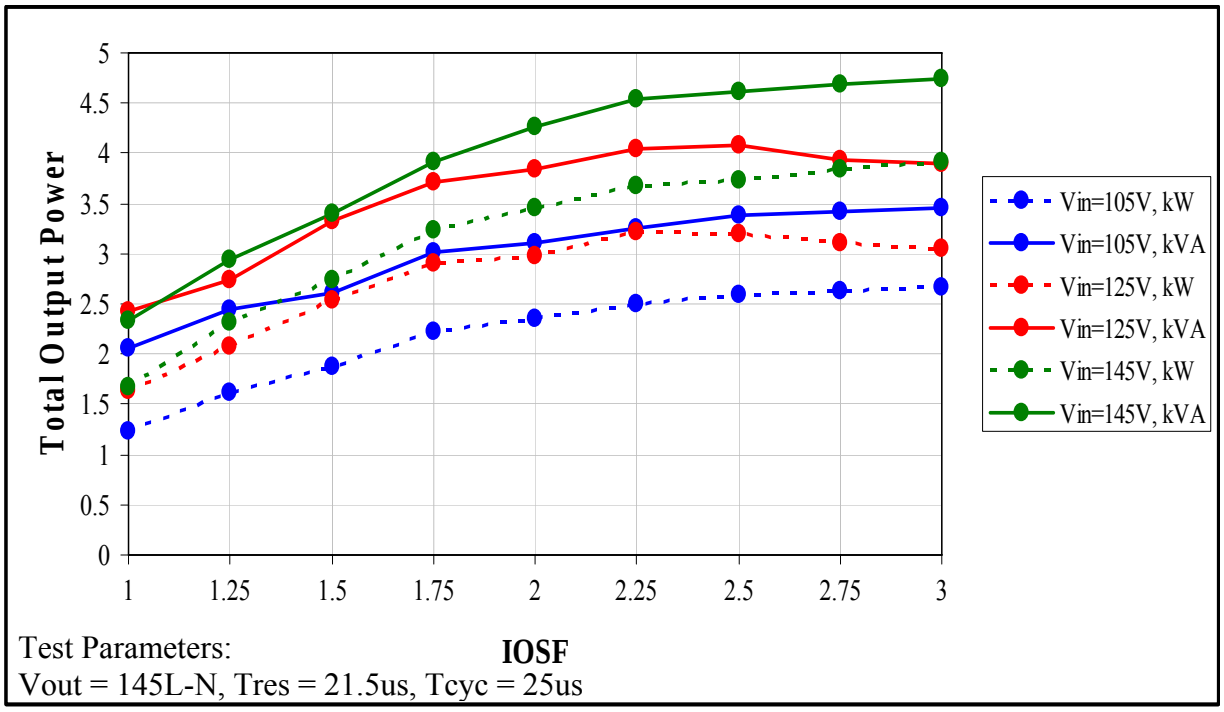
ii.) IOSF Versus Total Output Power

The Total Output Power was monitored via a three-phase power analyzer while the parameter IOSF was varied. The results are shown in Table D3 and Figure D3, following:

Table D3. *IOSF VS Phase Current Magnitude (IOSF vs IO).*

	Vin = 105V_{L-N}, Vout = 145V_{L-N}		Vin = 125V_{L-N}, Vout = 145V_{L-N}		Vin = 145V_{L-N}, Vout = 145V_{L-N}	
IOSF	**Total Output Power (kW)**	**Total Output Power (kVA)**	**Total Output Power (kW)**	**Total Output Power (kVA)**	**Total Output Power (kW)**	**Total Output Power (kVA)**
1	1.24	2.06	1.64	2.43	1.68	2.34
1.25	1.62	2.45	2.07	2.74	2.32	2.95
1.5	1.87	2.61	2.53	3.32	2.74	3.4
1.75	2.22	3.02	2.9	3.72	3.23	3.92
2	2.36	3.11	2.97	3.85	3.45	4.27
2.25	2.5	3.25	3.22	4.04	3.67	4.54
2.5	2.6	3.39	3.2	4.08	3.74	4.62
2.75	2.63	3.41	3.1	3.93	3.85	4.68
3	2.66	3.46	3.06	3.9	3.92	4.74

Figure D3. *IOSF VS Total Converter Output Power (IOSF vs PO).*



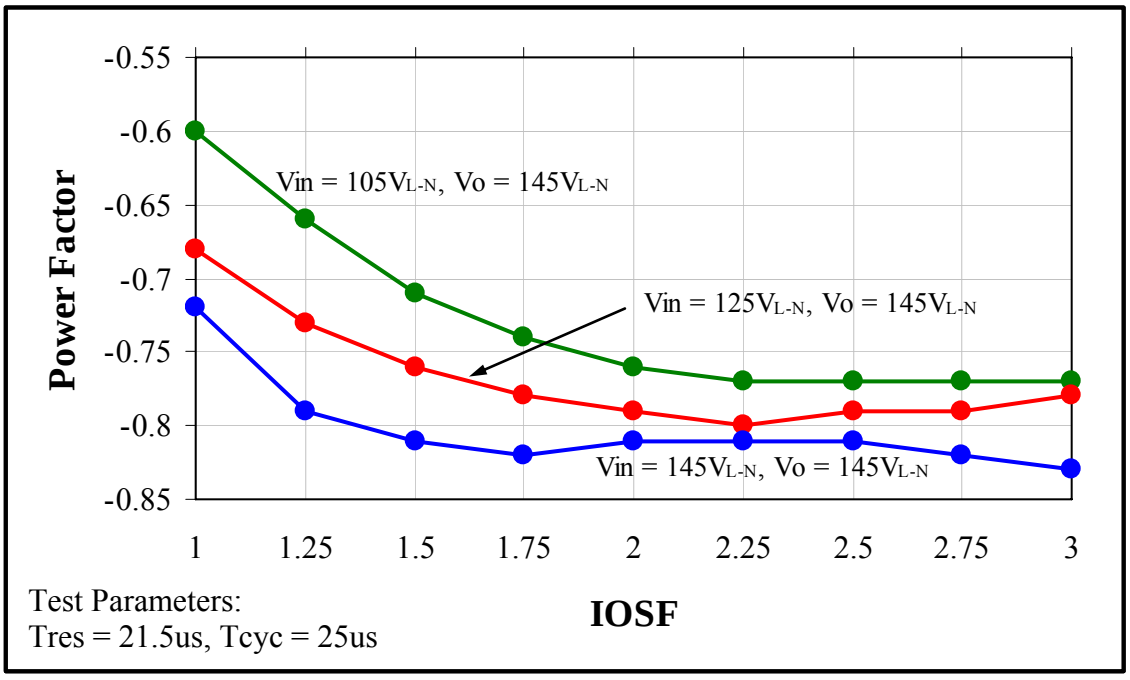
iii.) IOSF Versus Phase Output Power Factor

The Phase Output Power Factor was monitored via a three-phase power analyzer while the parameter IOSF was varied. The results are shown in Table D4 and Figure D4, following:

Table D4. *IOSF VS Total Phase Output Power Factor (IOSF vs PF).*

	Vout = 145V_{L-N}		
	Vin =105V_{L-N}	Vin =125V_{L-N}	Vin =145V_{L-N}
IOSF	**Output Power Factor**	**Output Power Factor**	**Output Power Factor**
1	-0.6	-0.68	-0.72
1.25	-0.66	-0.73	-0.79
1.5	-0.71	-0.76	-0.81
1.75	-0.74	-0.78	-0.82
2	-0.76	-0.79	-0.81
2.25	-0.77	-0.8	-0.81
2.5	-0.77	-0.79	-0.81
2.75	-0.77	-0.79	-0.82
3	-0.77	-0.78	-0.83

Figure D4. *IOSF VS Total Phase Output Power Factor (IOSF vs PF).*



It should be noted that the firmware version used during the Performance Testing did not have provisions for the ETM control loop to adjust or correct the I/O power factor. The resultant power factor resulted solely from the execution of the native ETM Converter operational algorithm. The observed power factors at low values of IOSF make sense in regards to operation of the ETM control loop – as resonant current transfers are excluded at low IOSF values, there is less "fill in" of the resultant output current and a higher harmonic distortion with an attendant power factor.

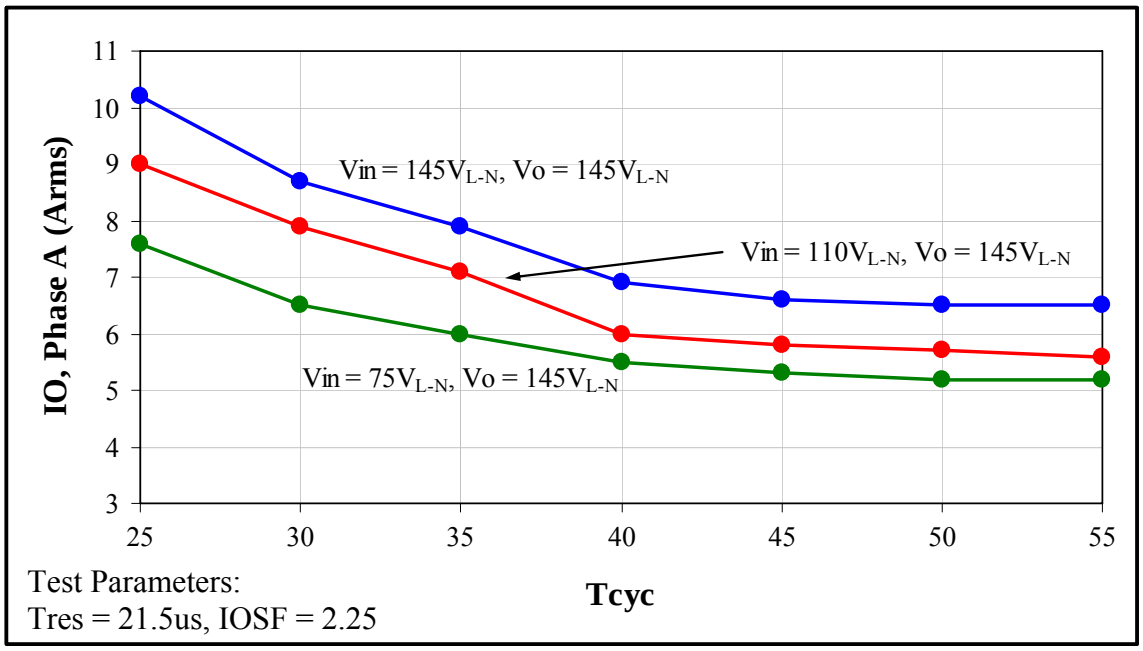
iv.) Tcyc Versus Phase Output Current

The Phase Output Current was monitored via a three-phase power analyzer while the parameter Tcyc was varied. The results are shown in Table D5 and Figure D5, following:

Table D5. *Tcyc VS Phase Output Current (Tcyc vs IO).*

	Vout = $145V_{L-N}$		
	Vin =$105V_{L-N}$	Vin =$125V_{L-N}$	Vin =$145V_{L-N}$
Tcyc (us)	**IO, Phase A (Arms)**	**IO, Phase A (Arms)**	**IO, Phase A (Arms)**
25	7.6	9	10.2
30	6.5	7.9	8.7
35	6	7.1	7.9
40	5.5	6	6.9
45	5.3	5.8	6.6
50	5.2	5.7	6.5
55	5.2	5.6	6.5

Figure D5. *Tcyc VS Phase Output Current (Tcyc vs IO).*



It is expected that as the parameter Tcyc is increased that the output current should decrease, due to the fact that an increasing Tyc with a Tres amounts to a lower pulse repetition rate. A lengthened cycle time can be thought of as a lower resonant current transfer event duty cycle. There is another plateau of results that is observed as the Cycle Time is increased, beginning at approximately 40us. This is not an expected behavior and requires further investigation for an explanation.

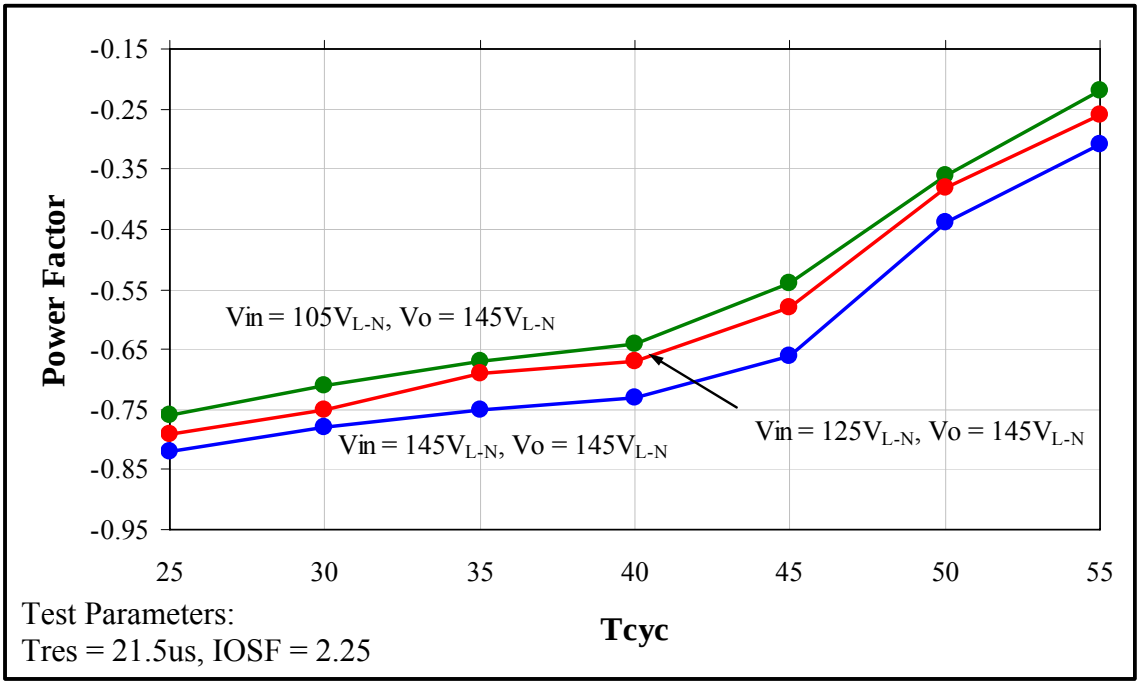
v.) Tcyc Versus Phase Output Power Factor

The Phase Output Power Factor was monitored via a three-phase power analyzer while the parameter Tcyc was varied. The results are shown in Table D6 and Figure D6, following:

Table D6. *Tcyc VS Phase Output Power Factor (Tcyc vs PF).*

	Vout = 145V_{L-N}		
	Vin =105V_{L-N}	Vin =125V_{L-N}	Vin =145V_{L-N}
Tcyc (us)	**Output Power Factor**	**Output Power Factor**	**Output Power Factor**
25	-0.76	-0.79	-0.82
30	-0.71	-0.75	-0.78
35	-0.67	-0.69	-0.75
40	-0.64	-0.67	-0.73
45	-0.54	-0.58	-0.66
50	-0.36	-0.38	-0.44
55	-0.22	-0.26	-0.31

Figure D6. *Tcyc VS Phase Output Power Factor (Tcyc vs PF).*



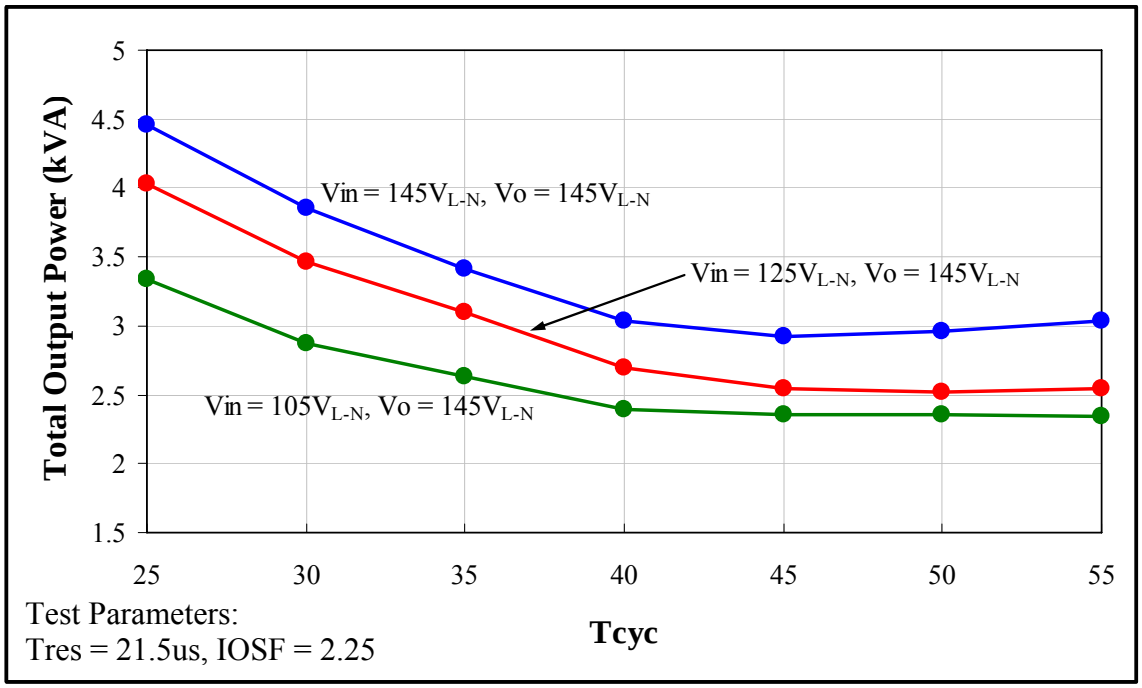
vi.) Tcyc Versus Total Output Power

The Total Output Power was monitored via a three-phase power analyzer while the parameter Tcyc was varied. The results are shown in Table D7 and Figure D7, following:

Table D7. *Tcyc VS Total Output Power (Tcyc vs PO).*

	Vout = $145V_{L-N}$		
	Vin =$105V_{L-N}$	Vin =$125V_{L-N}$	Vin =$145V_{L-N}$
Tcyc (us)	**Total Output Power (kVA)**	**Total Output Power (kVA)**	**Total Output Power (kVA)**
25	3.34	4.03	4.46
30	2.87	3.47	3.85
35	2.63	3.1	3.41
40	2.4	2.7	3.03
45	2.35	2.55	2.92
50	2.35	2.52	2.96
55	2.34	2.55	3.03

Figure D7. *Tcyc VS Total Output Power (Tcyc vs PO).*



As was the case of the Power Factor, the Output Power exhibits the same plateau behavior (as it should) for Cycle Times greater than 40us. This behavior is unexplained and requires further investigation.

vii.) Performance Test Data Set Point #1

The Performance Testing for the ETM Converter Prototype was planned to be a series of data gatherings at set points ranging from $145V_{L-N}$ output voltages to the maximum design value of $240V_{L-N}$ (corresponding to ~$408V_{L-L}$). The data set points would be increased in 20V increments from the minimum value to the maximum value. Performance data was collected for the input and the output at data set point #1, with the following fixed parameters: Tcyc = 25us, Tres = 21.5us, Vout = 145VL-N and IOSF = 2.25, and is shown in Table D8 and Figures D8 through D12:

Table D8. *ETM Converter Performance Set Point #1Test Data.*

Vin	Iin	KVA	KW	PF	Vout	Io	KVA	KW	PF
70	9.6	2.05	1.68	0.82	145	4.4	1.98	1.29	-0.65
80	9.6	2.31	1.92	0.83	145	5.1	2.23	1.54	-0.69
90	10.2	2.76	2.35	0.85	145	6	2.62	1.93	-0.74
100	11.6	3.47	2.84	0.82	145	7	3.06	2.33	-0.76
110	14	4.61	3.37	0.73	145	8	3.5	2.68	-0.78
120	16	5.69	3.72	0.65	145	8.6	3.8	3	-0.79
145	13.4	5.67	4.47	0.78	145	10.2	4.52	3.67	-0.81

Figure D8. *Input Voltage VS Phase Output Current (Vin vs IO).*

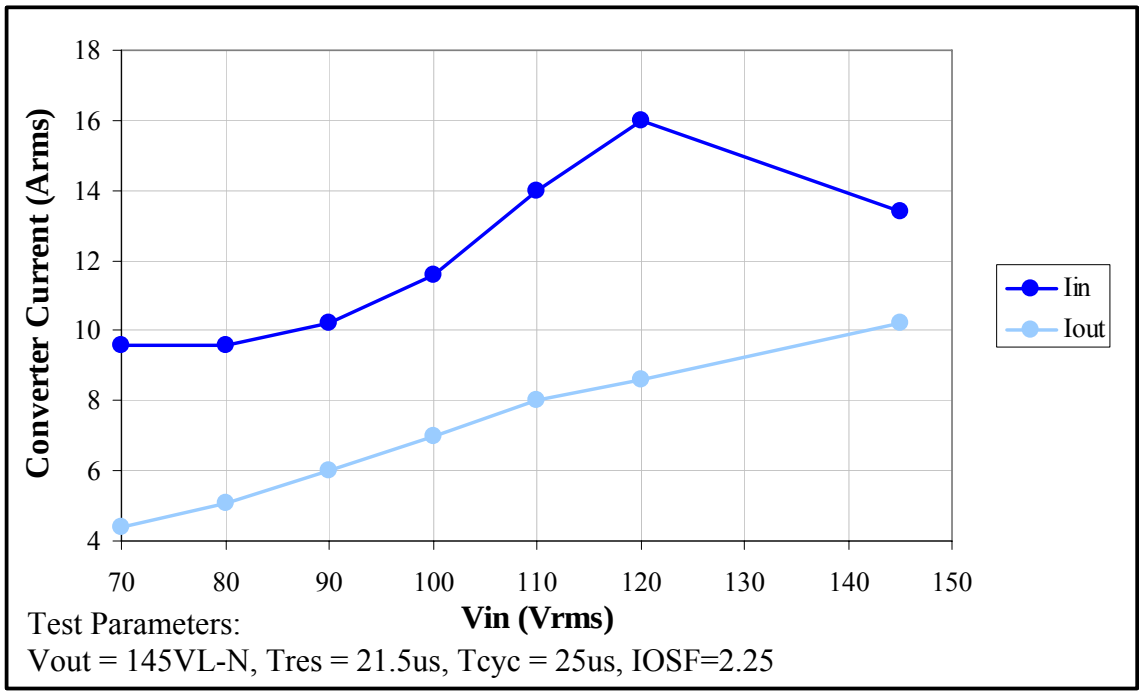


Figure D9. *Input Voltage VS Input and Output Power Factors (Vin vs PF).*

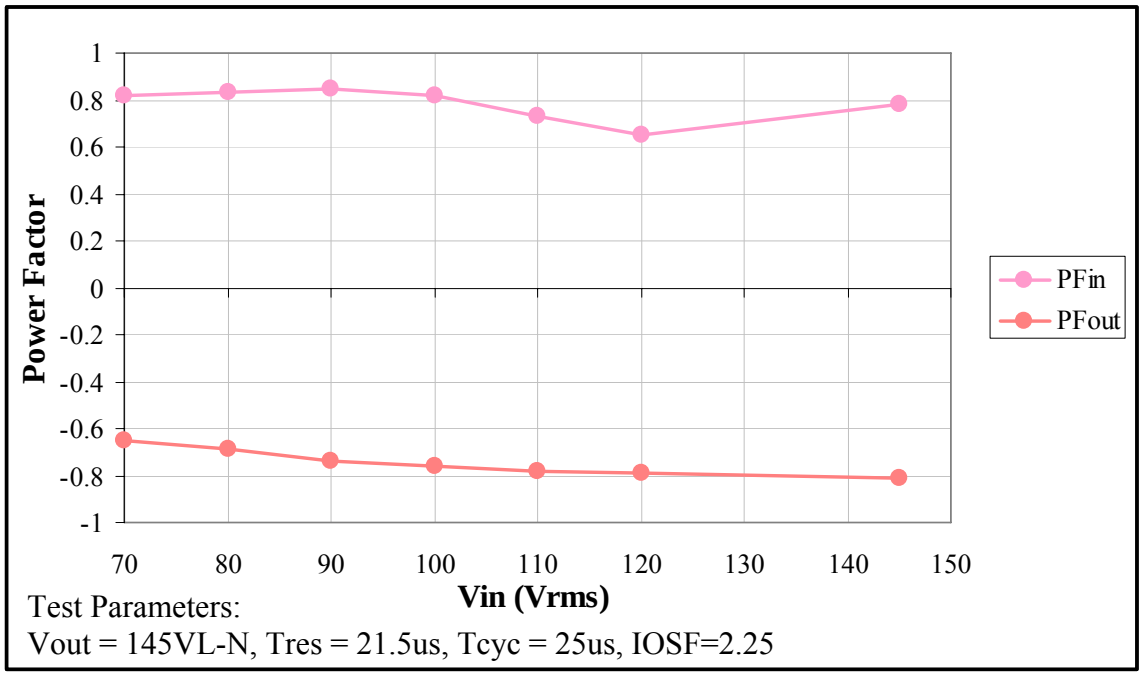


Figure D10. *Input Voltage VS Total Output Power, kVA (Vin vs PO).*

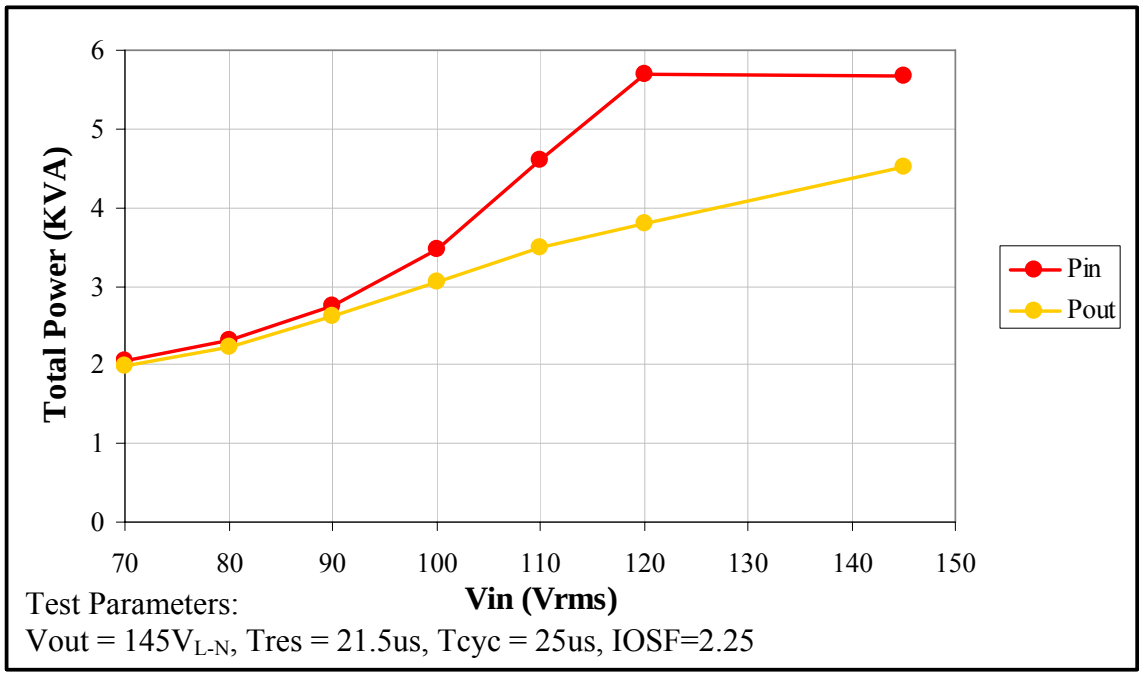
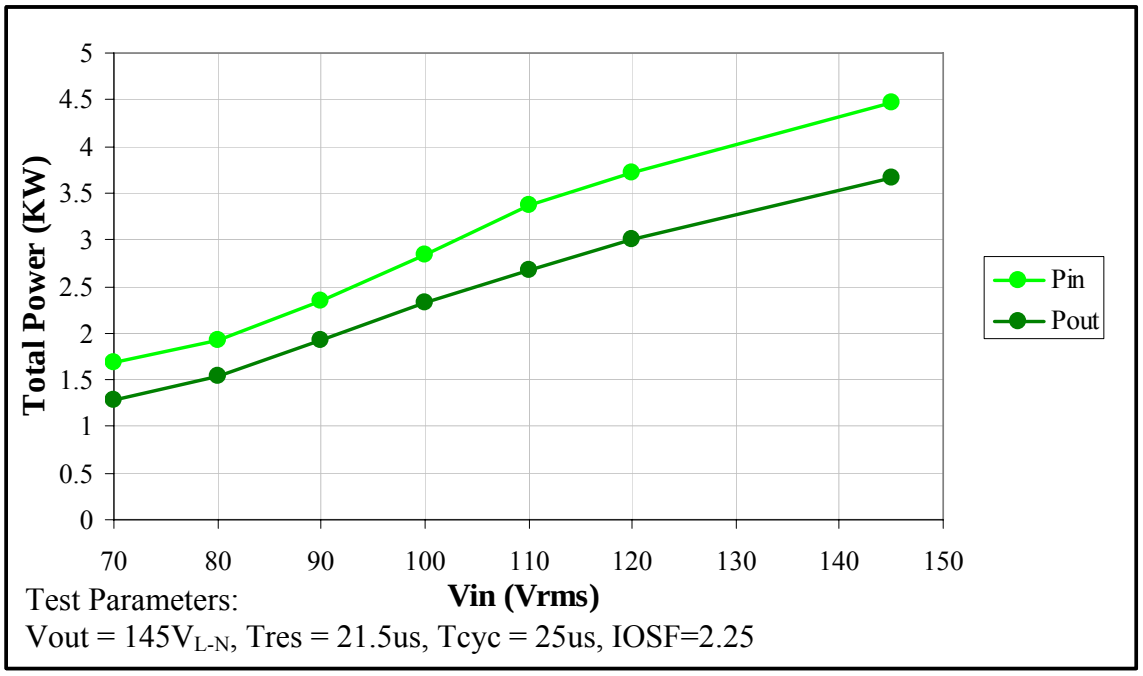


Figure D11. *Input Voltage VS Total Output Power, kW (Vin vs PO).*



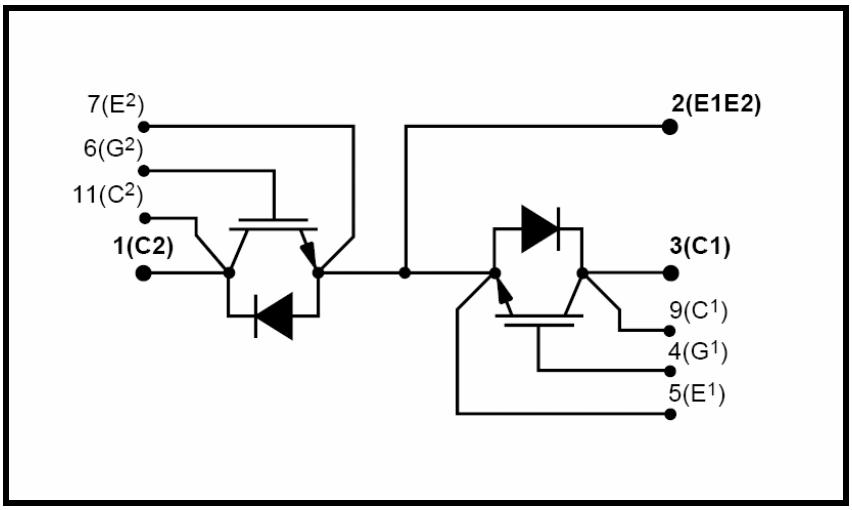
During the Data Set Pont #1 Performance Testing, there was anomalous behavior noted in the input current, power factor and total power (kVA) for input voltages between 100V and 145V. It is interesting, however that the total power in kW demonstrated the expected straight line variation as expected! This behavior is most likely due to the fact that the I/O power factors are uncontrolled by the ETM control loop with the revison level of the firmware used, so the resultant power factors during operation were “what they were”.

E.) Summary of IGBT Failures Encountered

i.) The IGBTs Used and Their Ratings

The IGBTS used in the ETM Converter are manufactured by Dynex Semiconductor, their part number DIM200MBS12-A000. These components are rated for +/-1200V and have an average current rating of 200A (400Apk for 1ms). This device is an AC switch composed of two series connected IGBTs (each with an anti-parallel silicon rectifier) with common emitters, as shown in Figure E1:

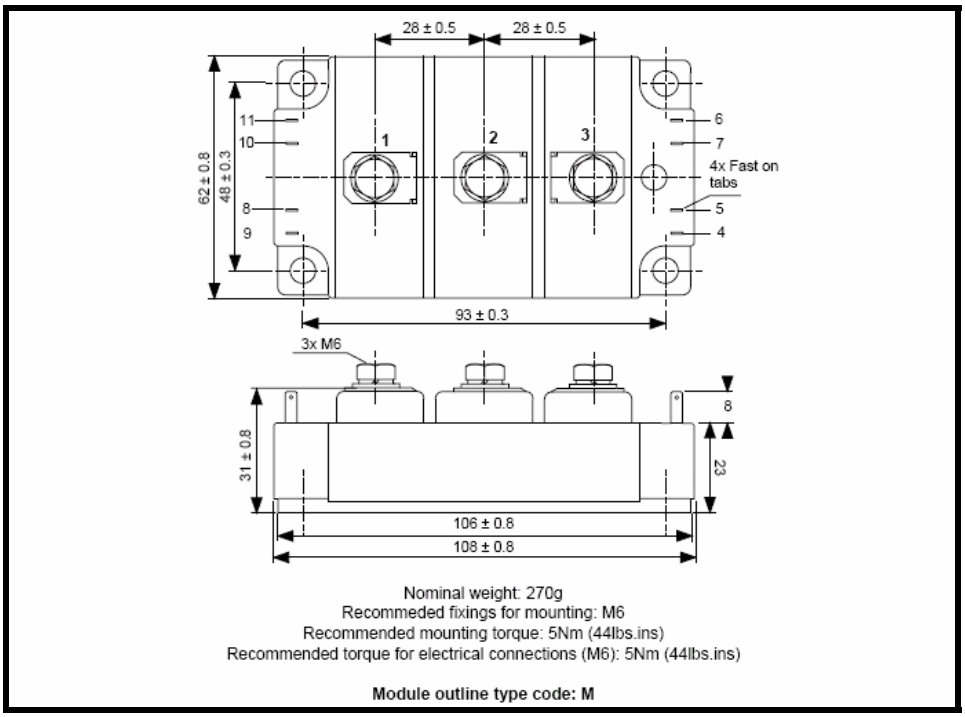
Figure E1. *Dynex DIM200MBS12-A000 Functional Schematic.*



These devices were selected for their 1200V breakdown voltage and their 200A current carrying rating, as well as for their very fast switching times. The data sheet of their electrical characteristics may be found here: DIM200MBS12-A000.

This device is housed in an M-6 modular package whose dimensions and electrical connections are shown in Figure E2.

Figure E2. *Dynex DIM200MBS12-A000 Mechanical Dimensions and Pinout.*



In the ETM Converter circuit application, each of the eight power train IGBTs had an isolated IGBT Driver Board integrated onto the package, as shown in Figure E3. This board consisted of a DC-DC converter, protection circuitry and an optically-isolated IGBT gate driver IC.

Figure E3. *DIM200MBS12-A000 IGBT With IGBT Driver Board.*

ii.) The First IGBT Failure Encountered

Since the initial power the ETM Converter Prototype had operated more than five cumulative hours when the first failure occurred. This failure manifested itself in the tripping of the internal circuit breakers of the ETM Prototype. Upon closer inspection, it was determined that all four in a single IGBT, had the effect of damaging/destroying all four IGBTs in the output switch matrix (the three phase output and the ground switch devices). It was at the $150V_{L\text{-}N}$ operating point that this IGBT failure occurred.

Upon closer inspection, it was observed that each IGBT failure consisted of a gate-emitter (G-E) shoot-through, whereby the G-E junction was short-circuited (with a resultant resistance less than 1Ω). Additionally, the IGBT Driver Board for each device was damaged and was observed to be non-functional – this is a result of the very high fault current that flows from the gate at the time of failure. A shoot-through failure is indicative of a safe operating area (SOA) overstress, where the semiconductor was forced to handle too much energy during a switching event, or from an over-breakdown voltage stress. Since the Prototype was operating at such a low I/O voltage level, the voltage overstress failure option was discounted. The low operating voltage also helped to discount the SOA overstress; so as a result, this failure was suspected to have been a random device failure. This failure will be further discussed in a following section.

The reason all four devices in the output switching matrix were destroyed is a direct result of the ETM Converter architecture. Upon failure of a single device in a short-circuit mode, it serves to permanently (actually temporarily until the protection circuit breaker trips!!) connect the central point of the matrix to a fixed bias point. This fixed bias point destroys each IGBT in turn (each successively failed and shorted IGBT adds to this situation) until all the IGBTs are destroyed. The destruction of all the devices in the switching matrix occurs because the ON cycle time of the resonance pulse (and consequently of any IGBT) is 20us; a time much shorter than the response time of the circuit breaker. After a time period of approximately 100us, all four IGBTs will be destroyed and shortly thereafter, the circuit breaker will trip.

iii.) The Second IGBT Failure

After the repair of the first failure, the converter was restarted for further debug activities. Unfortunately, after approximately 30 seconds of operation, the Prototype Converter experienced another IGBT failure in the output stage. It was determined that a total of four (4) IGBTs were destroyed before the internal circuit breaker tripped. This was a similar failure result as the first failure encountered. Like the first failure encountered, the I/O voltages were set to $75V_{L\text{-}N}$, and these failures were also observed to be G-E shoot-through failures for the IGBTs.

Again, since there was no reasonable explanation for this shoot-through event to have occurred, this failure was also assumed to be a random device failure.

iv.) The Third IGBT Failure

At power-up of the repaired ETM prototype, the internal circuit breaker immediately tripped and it was determined that all four IGBTs in the input switching matrix were damaged/destroyed once again. As was the case for the last failure, this test was conducted at $75V_{L\text{-}N}$ I/O voltages and the IGBT failures were all shoot-throughs.

After this exasperating failure, extensive debug activities were undertaken to determine the root cause of the IGBT failures. As a result, it was revealed that this failure was caused by the fact that although a reasonable value was entered in the data box for the Cycle Time or the Resonance Time (or even that a change may have been made to these two variables) on the GUI, there was no hardware confirmation or update of the parameters in the non-volatile memory (NVM) in the ETM Converter. Additionally, it was determined that there was no guarantee that the parameter data was consistently exchanged properly between the host laptop and the dsPIC/ADSP microcontrollers in the ETM Converter after a change was initiated. And, to make matters worse, there were instances observed where extraneous, random data was loaded into the NVM in the ETM Converter. It was determined that the root cause reason the third failure occurring was that a value of 15us was somehow entered in the NVM as the value of the Resonance Time, Tres. With this time value (approximately 50% of the actual resonant time), the IGBT switches would have been forced to open while carrying their maximum or very

close to their maximum resonant current. This switching situation subjected the IGBTs to stresses exceeding their maximum ratings, in particular their reverse SOA.

In light of the failure mode that accounted for the first two sets of failures observed, this newly-identified failure mode had made sense as the root cause. Rather than just random failures, the previous failures could be accounted for by the NVM random data problem. Although this theory could not be directly verified, it made sense as a reasonable explanation, as the only difference in the failures was the time span that had elapsed before a failure had occurred.

It should be noted that after the NVM-related problem was resolved, the converter was started and stopped more than 100 times and had successfully run at load levels up to ***8kW***, having logged an operating time of greater than 40 hours. It was during this time that the lion's share of the performance testing and data collection was achieved.

v.) Fourth (Last) Failure Encountered

Unfortunately, the fourth and final Prototype failure occurred when the input and output voltages were increased to $200V_{L\text{-}N}$ (~$350V_{L\text{-}L}$) and the power was turned on. The circuit breakers tripped within five seconds of power application, indicating an internal fault. Upon cursory troubleshooting the ETM Prototype, it was determined that all the IGBTs in the power train were damaged, along with their associated IGBT Driver Boards. In fact, the IGBT Driver Boards were damaged beyond repair in six of the eight cases (all except for the ground-references switches in the I/O switching matrix). Due to a number of different factors, the testing was halted at this point, and this was the state of the Prototype when the testing was terminated.

The remainder of the failure analysis is speculation based on this very limited troubleshooting and failure analysis, but due to the nature of the damage it was most likely that this failure was caused by dV/dt-induced turn-on of one or more the off-state IGBTs in the I/O switching matrix. It had been suspected that voltage rate-related problems might exist for the IGBTs at or above the maximum rated I/O voltage of $235V_{L\text{-}N}$ ($408V_{L\text{-}L}$), due to the gate drive levels that were utilized. So, it was not entirely surprising that failures occurred at this lower level. It had been a planned task activity that the IGBT Driver Boards were to be redesigned re-spun to incorporate a negative off-state gate bias of at

least 5V in order to improved the predicted dV/dT immunity to greater than 15,000V/us. Several steps were taken to improve the DV/dt immunity of the present hardware (optimizing the gate resistance value and the implementation of an improved gate driver IC), but in the absence of a negative gate bias potential, there was only a limited rate immunity improvement available.

At the operating point at which the failure had occurred, the calculated maximum rate of change was approximately 9,000V/us (dV at the switching common switching node = 1000V and the rise time, dt, for an IGBT = 120ns), which was uncomfortably close to the actual predicted value for the Prototype hardware of 12,000V/us (a number reached using numerous assumptions). For this performance parameter in particular, due to the variability in IGBT characteristics (junction capacitances and switching characteristics), a 2-to-1 (200%) tolerance in threshold sensitivity is desired to absolutely guarantee immunity to the effects, and one that should be measured and treated as a "datasheet" parameter. Due to budget, manpower and schedule constraints, this could not be achieved with the present design. It was *hoped* that unchanged/unimproved hardware would suffice (with adequate dV/dt margin) to enable the Prototype ETM to successfully complete the Performance Testing. This obviously was not the case.

At the time the project was terminated, the next step in the troubleshooting process was to construct a test jig/fixture and to measure/determine the dV/dt turn-on threshold of the actual hardware (IGBT and Driver Board). [The test jig had been constructed but no testing had commenced as of the time of project cancellation.] Additionally, a voltage rate-induced failure mode had been suspected (actually one of a longer list of suspects) as the root cause of the first three failures observed, but the operating level at which the failures occurred was too low to have absolutely been suspected as the root cause. Thus rate-induced failures were almost immediately ruled out in those cases. However, at that time, a new design for the IGBT Driver Board was accomplished – one that included a negative 5V off-state bias to improve that would dV/dt immunity to 15,000V/us. And, after the NVM issue was resolved, the Prototype Converter worked reliably for a long period of time, so the new design was "shelved" for future implementation. But, the change in operating condition caused the ultimate failure of the prototype, and until future work is done to reveal the actual, all the previous words are conjecture and speculation.

F.) Remaining Tests To Be Performed

The ETM Converter Test Matrix that was planned from early on in the ETM Converter development project was fairly ambitious. It covered the range of tests required, including: Debug, Functional, Performance, Safety/Compliance and System Integration Tests. These represented the tests required to fully characterize the ETM Converter Prototype in order to guarantee its fitness as a potential product, and to reveal any flaws in the design or the topology. This testing was also intended as a gateway to have prepared the Prototype for future testing at Sandia Labs, or another similarly-equipped DOE laboratory.

The test matrix that was planned for Sandia Labs was intended to perform those demanding tests that could not be performed at other lab sites available to the ETM Converter Prototype; most importantly those tests that involved providing variable frequency, variable amplitude input power to the Converter. The Sandia Labs Test Matrix emphasized the variable input tests, and the ability of the ETM Converter to process power from such inputs. It also strived to reveal the durability of the Converter in transient operating condition sweeps for the input of the Converter; these tests had sought to mimic the performance of a permanent magnet generator for a variety of output situations.

Finally, the Revised Performance Test Matrix, as shown in Table G1, was developed as a less aggressive, compromise testing regime to accommodate for the test deficiencies at the Marlboro Test Labs facility – particularly the inability to vary the input operating frequency. This testing was seen as the lead in to the ETM Converter Test Matrix; to have enabled the Prototype to have been thoroughly debugged and still have yielded test results pertaining to Performance test criteria.

i.) Test Progress Summary

It is clear that the testing that had been performed had only scratched the surface of even the most compromising test plan (Figure F1). This was due to the fact that the four sets of IGBT failures were unexpected, and the unavailability of replacement spares for the third failure set had quite negatively affected the test schedule. Even if adequate

spares had been available, the pauses in the test schedule to repair the Prototype Converter were a distraction and a drain of the very limited manpower available to the project. In the end, the need to make repairs consumed the available schedule and budget and made it impossible to complete the required testing.

Table F1. *Revised Performance Test Matrix.*

Test	**Purpose**
Low Voltage Bring Up (50Vrms/60Hz, Input and Output)	Initial Power On of 34kW ETM Converter Hardware.
Medium Voltage, *Fixed Voltage/Frequency* (220Vrms/60Hz, Input and Output)	a.) Test IGBT Drive Circuit Functionality. b.) Verify IRZC (Resonant Cycle Time) Operation. c.) Hardware Fault Reporting. d.) GUI Interface Function. e.) Power Transfer Efficiency. f.) Verify Power Draws and Operation of Individual Converter Subsystems.
Medium Voltage, Variable Input Voltage/Fixed Frequency (50-220Vrms/60Hz Input and 220V/60Hz Output)	a.) Verify IRZC (Resonant Cycle Time) Operation. b.) Power Transfer Efficiency.
High Voltage, *Fixed Voltage/Frequency* (408Vrms/60Hz, Input and Output)	a.) Verify IRZC (Resonant Cycle Time) Operation. b.) Verify GUI Interface Functionality. c.) Power Transfer Efficiency. d.) Verify Individual Converter Subsystem Operation.
High Voltage, *Variable Voltage/Frequency Input* (100-408Vrms/10-100Hz, Input and 408Vrms/60Hz Output)	a.) Verify ETM Converter Functionality b.) Power Transfer Efficiency. c.) Gather Operating Parametric Data d.) Create Hardware and Software Revision List(s).

G.) Present Condition of the ETM Converter Prototype

The present condition and operational state of the ETM Converter Prototype is described in this section. Also discussed are the actions required to restore the Prototype back to an operational state, as well as open/planned hardware and software issues.

i.) ETM Prototype Present Condition

The present condition of the ETM Prototype is that which resulted from the last voltage increment in the Performance Testing as performed on March 10, 2005. As was mentioned in a previous section, the voltage was incremented to 200VL-N from the initial 145VL-N data test point, and upon turning on the ETM Prototype the internal circuit breakers tripped. After troubleshooting the Prototype, it was determined that the eight (8) IGBTs in the power train were destroyed/damaged, as well as their associated IGBT driver circuit boards. This was as far as the troubleshooting activities were performed, so there is uncertainty that other constituent circuit boards may be damaged, although this scenario is probably remote as there is fault isolation included in the ETM circuit topology. Regardless, the complement of circuit boards in the Prototype will need to be re-tested in order to determine their wholesomeness.

In order for Performance Testing to continue, the reason for the final failure mode observed needs to be identified. At present, this is speculation, but the failure was most probably caused by dV/dt-induced failure in the IGBTs and their driver circuits. A cursory review of the failures indicated that the IGBT drivers and the drive strategy used may have a susceptibility to parasitic turn-on for the high dV/dt's observed in normal ETM operation, particularly at the nominal design I/O operating voltage. Again, this is conjecture and speculation, but it offers a viable theory as to why the IGBTs failed just after the I/O voltages were increased.

Even before the Prototype was damaged, there were a set of hardware and software changes and revisions that were for the ETM Prototype. The following discussions outline the hardware and software change activities planned for the 34kW ETM Converter Prototype in preparation for its integration into a 100kW system.

ii.) Hardware Changes and Revisions

The following changes, revisions and activities were planned for (or were necessary to restore the Prototype to proper operation to) the ETM Prototype:

1. Re-design the IGBT driver circuitry to provide for a negative off-state drive bias of 5V for the IGBTs. This will improve the dV/dt performance of the IGBTs in operation by a factor of four, or provide a calculated 10,000V/us rate turn-on immunity. This redesign will also require an IGBT Driver Board PCB re-spin.
2. Perform nominal I/O testing with the internal bias supply of the ETM Prototype connected. This power supply was disconnected for all the debugging and testing to date as the lower voltages used for the test data points were lower than the operating range of the AC-DC converters in the power supply. An external power supply was used to provide the 48V for the cooling fans and for the remainder of the circuitry in the Prototype.
3. Investigate and identify the characteristics of the new resonant inductor to determine why it experiences a higher-than-expected temperature rise. The new inductor was specified and designed to have a maximum power dissipation or total loss of 25 Watts at the 34kW power transfer level. The inductor was observed to dissipate 15 Watts of power at the 4.5kW level.
4. Incorporate later-revision dsPIC30F6011 microcontrollers capable of operating at a 30MHz clock rate (the ETM Prototype has original lot fabrication dsPIC prototypes, only capable of 20MHz operation, incorporated into it). This will allow the main system clock on the ETM Control Board to be increased from 20MHz to 30MHz, which further allows the ADSP-2186 to operate at 30MHz, thus improving the real-time operation of this microcontroller and providing further margin for the minimum Tres-to-Tcyc operating time ratio. This action does not require a Control Board PCB re-spin, only two component changes.

To get the ETM Prototype back into functional shape, the eight IGBTs in the power train and their associated, up-revisioned Driver Boards will need to be replaced. This will necessarily include a debug and data gathering session to vary the I/O voltages up to their maximum values to insure that the ERM Prototype will function at the expected maximum

conditions. The resultant dV/dt's to which the IGBTs are subjected must be measured and the margin of operation must be determined.

iii.) Software Changes and Revisions

There are several software/firmware-related issues that must be addressed in parallel with and in some cases prior to the further functional and performance testing. These include:

1. Determining the code execution real time burden required by the ADSP inner control loop microcontroller. This is a critical problem that will ultimately affect the power throughput of the converter. Ultimately, we will need to tune the resonance time and the real time of the processor such that the ratio of the Resonance Time to the Cycle Time is 90% or greater.
2. Change the value of the parameter VcLimit in the DoLogic Logic Flow. Presently the value of VcLimit is 1500V, which is the same value as the hardware threshold for system shutdown and latch off. This will lead to ambiguities in operation and unintended latch off events occurring. The value of VcLimit should be set to 1400V to provide a margin of operation between a logic operation and a hardware protection event (1500V is the absolute maximum capacitor voltage in order to prevent IGBT switch damage). It is also highly desirable that this parameter be user configurable from the GUI interface, as it is controlled in hardware by D/A converters that may be set from the dsPIC housekeeping microcontroller.
3. Adapt the GUI Interface to include a new user-adjustable parameter VCSF, where this parameter is defined as the variable that will replace the fixed value of "2" in the "*DoLogic Logic Flow*" subroutine, in the second operation where the inequality Vcs<2*Eo is tested. The new variable VCSF should be adjustable in the GUI in the same manner as the variable IOSF, with at least seven assignable values between 1.5 and 2.5 (inclusive of each). Although not a critical change, it is highly desirable to have the adjustability of this variable in order to observe the operation of the converter for parameter values other than "2".
4. Adapt the "*DoLogic Logic Flow*" subroutine to act in accordance with the input power versus frequency transfer function of Figure 1 (Typical Permanent Magnet Generator

Characteristic) on Page 6 of the "ETM Converter Programming Guide". It is essential that the converter demand power from the input according to this transfer characteristic, otherwise the generator can be easily overloaded and operate at less than optimum efficiency. This is a critical issue and must be implemented before performance testing of the prototype can be successfully completed. This functionality may be implemented in several ways, but it of primary importance that the pulse repetition frequency be kept as high as possible in order to preserve the highest operating efficiency. Additionally, the parameters shown in Figure 1 (Typical Permanent Magnet Generator Characteristic) on Page 6 of the "Programmers Guide" should be made available for user input via the GUI.

5. The output power factor must be made adjustable via the criteria shown on Page 12 of the "Programmer's Guide". This is a critical issue and must be implemented before performance testing of the prototype can be successfully completed. The proper readout/display of the power factor must also be corrected on the GUI interface readout.
6. The variable parameters set in the GUI must be made "non-volatile", assuming the last value set prior to the power being removed from the converter. It is desirable to have these parameters resident as data in the I2C EEPROM device (U2), for loading into U1 and U7 during the housekeeping phase of the converter at power on. This is a critical issue that needs correction before performance testing may commence. The presence of volatile converter operating parameters makes for the likely possibility of hardware-level "confusion" during the converter optimization process.
7. Fault protection must be added to the operating software code to account for the following fault situations:
    - The converter shall be made to cease power conversions BUT NOT LATCH OFF when the input frequency drops below fsl or exceeds fsh. The quantity fsl = 0.95 * fmin and fsh = 1.1 * fmax (see Figure 1, Page 6 of the "Programmer's Guide"). The phrase "cease power conversions" is defined as an idle state: the inner loop controller (ASDP, U7) is set to an STOP state, whereby the converter sit with all input and output phase IGBTs open (OFF) and the two ground IGBTs activated (ON).

Simultaneously, the outer loop controller (dsPIC, U1) shall continuously monitor the input/output phase voltages until favorable conditions are present for proper converter operation (fmax > fin > fmin, and Vo > 275V peak, for all three output phases), and then the converter is re-started.

- The converter shall be made to cease power conversions BUT NOT LATCH OFF (see previous for definition) when the peak voltage of any output phase drops below 30V for time durations of greater than 50ms.

8. Since the converter is phase sequence-dependent for proper operation and damage may occur to the power train when the I/O phases are incorrectly applied to it, the converter shall not start and sit in a benign, idle state when incorrectly phased I/O are applied to it. Operating software code must be added during the housekeeping routine at converter start up such that the three phase inputs and the three phase outputs are checked for proper phase sequencing. If either set of phases are incorrectly connected to the ETM converter when the **START** GUI "softkey" is clicked, then the converter shall remain in an idle state: the inner loop controller (ASDP, U7) is set to an STOP state, whereby the converter sit with all input and output phase IGBTs open (OFF) and the two ground IGBTs activated (ON). Simultaneously, the outer loop controller (dsPIC, U1) shall continuously monitor the input/output phase voltage phasing until each set of three voltages is properly connected (i.e. A/B/C) – the front panel fault LED shall be caused to blink at a 1 Hz rate if the inputs are incorrectly phased or the front panel bi-directional LED shall be caused to blink at a 1Hz rate if the outputs are incorrectly phased. As such, the Converter will act as its own phase sequence detection meter. This is a critical issue that, although does not affect functional or performance testing, will prevent costly damage from occurring if the ETM Converter is incorrectly wired.

iv.) The Future of the ETM Converter

Exclusive of the specific software revision tasks previously outlined, there is required to be an effort to review the present software and firmware to insure that it conforms to the requirements as defined in the "ETM Converter Programming Guide". During the debug process, absolute conformance to the Guide was deemed less important than functionality

(e.g. “make it work”). This task is important to remove the ambiguity that exists between what it thought to exist in software code (and the attendant functionality) and what really *does* exist. Additionally, the GUI-interface must be updated to make it a parameter-setting (personalization) interface for the user of the ETM Converter rather than the test data collection-centric interface that it is at present. This is an important task that must be performed as it turns the ETM Converter into a product, such that an operator may set up and personalize the Converter to the I/O conditions under which it will operate. Without this configurability, the real functionality of this Converter is greatly reduced, as it truly a “Power Computer” that relies on software to operate and it requires an initial set up to define its operating point and performance criteria before it is placed into operation.

Finally, after all these previous tasks are completed, three additional Prototypes need to be constructed in order to satisfy the original intent of the Grant Project (i.e. an operating 100kW ETM Power System). It will be necessary to update the ETM firmware to enable the built-in interface circuitry to perform sensing and fault detection functions required by a multi-module power system. Also, the GUI Interface will need to be modified to support the parametric programming of the three or four ETM Converters (depending upon redundancy), their fault sensing/reporting and their concurrent operation.

Supplemental Documents

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ETM Converter Programming Guide

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December 5, 2003

Document Page Count: 37

Revision History:

Revision	Date	Originator	Description
EE	24 Jun 03	AGPM	Initial Release
E1	18 Aug 03	AGPM	Revisions to eliminate memory references and other changes. General cleanup.
E2	05 Sep 03	AGPM	Added dual processor information and revisions to nets.
E3.2	04 Mar 04	AGPM	Changed RG9 in Figure 7.
E4	03 Apr 04	AGPM	Added Functionality Table and various other changes.
E5	22 Jun 04	AGPM	Changes to reflect RE2 Analog and Digital Control Hardware.

Table of Contents

Figures

Tables

I.) Executive Summary

The ETM converter is a resonant-link power converter that utilizes a power switch matrix to transfer energy from any one of three (phase) inputs to one of any three (phase) outputs, or conversely from any output to any input. The ETM converter is inherently bidirectional in its energy transfer, and it can act as a fixed voltage source, a fixed current source, a variable voltage/current source and a variable frequency source. The ETM converter design utilizes dual microprocessors (Microchip dsPIC30F6011 as a real-time digital signal processor and an Analog Devices ADSP-2186 to act as a dedicated IGBT switch state controller) to perform all analog sensing (of the phase voltages and resonant current) and digital control of the power switch state(s).

II.) Modes of Operation

The ETM converter has several modes of operation, detailed as follows.

a.) Power Converter/Current Source

It can be a bidirectional power converter whereby current is delivered from the input-to-output or from output-to-input. It can be a unidirectional power converter where current is delivered from input-to-output only. In these modes, the output is set at a fixed voltage and frequency, generally those of the voltage grid to which the converter is connected (i.e. 690V phase-to-phase at 60Hz), and the input is derived from a generator whose amplitude and frequency vary within a given operating range (e.g. 100-690V phase-phase and DC to 80 Hz). In this configuration, the ETM converter will balance the power (current) drawn from or provided to each of the three phase inputs or outputs. Additionally, based on the condition of a set of three analog inputs (POWER FACTOR, SPEED and PITCH), the converter will: control the output power factor within the range of 0.2 leading to 0.2 lagging; control the direction of current flow for a bidirectional converter in a proportional manner and; limit the deliverable current in a proportional manner. Finally, since the ETM is acting as a power converter into a fixed-voltage utility power grid, the energy supplied to the grid will be in the form of output current -- delivered as a low harmonic distortion, sinusoidal time-varying waveform at all times.

b.) Variable Voltage and Frequency Power Source

The ETM converter will be programmed for this operational mode in the future.

III.) User Interface

The User Interface will be via an RS-232 link to the ETM converter from an IBM PC. The information exchanged with the PC will be used to "personalize" the operation of the ETM converter. The User Interface shall consist of a programming screen (or series of screens) on the IBM PC that prompts the User to set the requisite parameters of operation. These parameters include:

Converter Parameters:

- (**U**)nidirectional or (B)idirectional Operation: **U**nidirectional for prototype.
- Output Voltage (V phase-to-phase): The valid range is 400 to 690VAC (**480**).
- Output Voltage Tolerance (%): The valid range is 1.0 to 10% (**5**).
- Output Power Factor Range[(1)]: The valid range is 0.2 to **1.0** (lagging and leading).
- Output Power Factor Tolerance (%): The valid range is 0 to 10% (**5**).
- Output Frequency (Hz): The valid frequency range is 47 to 63Hz (**60**).
- Output Current Ramp-Up Time[(2)](ms): The valid range is 50 to 1000ms (**250**).
- Input Voltage Range (V phase-to-phase): The valid range is 100**(250)** to 690(**490**)VAC.
- Input Current Range (Arms per phase): The valid range is 0A to **80**Arms.
- Input Frequency Range (Hz): The valid range is **DC** to **200**Hz.

Generator (Input) Parameters (See Figure 1):

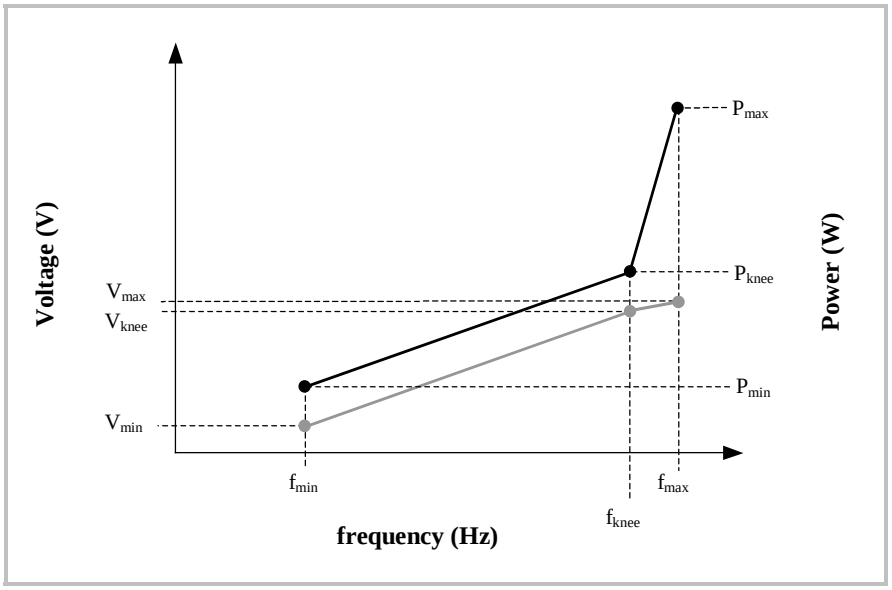
- Minimum Output Frequency (Hz), f_{min}: The valid range is DC to **50**Hz
- Knee Output Frequency (Hz), f_{knee}: The valid range is 100 to **200**Hz
- Maximum Output Frequency (Hz), f_{max}: The valid range is f_{knee} + 10% (**5%**)
- Maximum Output Power (kw), P_{max}: The valid range is 20kW to 50kW (**34**).
- Knee Output Power (kW), P_{knee}: The valid range is 10kW to 50kW (**P_{max}/2**).
- Minimum Output Power (kW), P_{min}: $P_{min} = P_{knee} * (f_{knee}-f_{min})^{0.33}$
- Output Voltage (V phase-to-phase) at Knee Frequency: The valid range is 100 to 350VAC (**480**).
- Output Voltage at Maximum Power (V phase-to-phase): The valid range is 400 to 690VAC (**480**).
- Output Voltage at Minimum Frequency (V phase-to-phase): The valid range is 100 to 300VAC (**250**)

NOTE: Default values are shown in **BOLD**.

(1) The output power factor is proportional to the DC voltage present on the "POWER FACTOR" analog input. When "POWER FACTOR"=0Vdc, then the power factor is at the maximum leading value and when "POWER FACTOR"=10Vdc, then the power factor is at the maximum lagging value. Regardless of the power factor range, when "POWER FACTOR"=5Vdc, then the power factor is 1.0 (unity).

(2) The output current ramp up time is defined as the time from the converter start up to the delivery of maximum current to each phase output. The current shall rise as a sinusoid in a linear envelope during this time.

Figure 1. *Typical Permanent Magnet Generator Characteristic.*



Once this information has been entered and communicated to the ETM converter, the converter is considered “personalized” and ready for operation.

The completion of the personalization of the ETM converter shall evoke another User input screen that prompts the User with the choice to “START”, “STOP”. “MONITOR” or “PRESONALIZE” the ETM converter.

The “MONITOR” choice will display a screen that has the following information:

RMS Phase-to-Neutral Input Voltages

RMS Phase-to-Neutral Output Voltages

Input Frequency

Output Frequency

RMS Input Phase Currents

RMS Output Phase Currents

Input Power Factor (Single Sampled Phase)

Output Per Phase Power Factor

Converter Temperature (From I2C Sensor on Control Board)

The monitor screen shall also give the User the choice to “STOP” the converter.

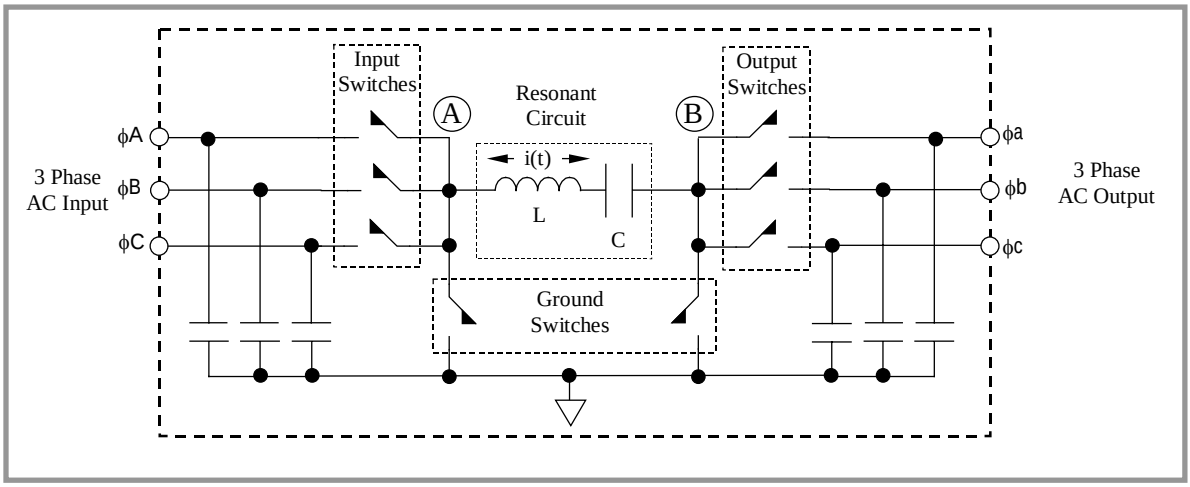
The “STOP” screen shall give the User the choice to “START”, “MONITOR” or “PRESONALIZE” the ETM converter.

IV.) Operation and Calculations

a.) ETM Converter General Operation.

The ETM converter transfers power to the input from the output via an L-C series resonant circuit and eight power switches, as shown in Figure 1.

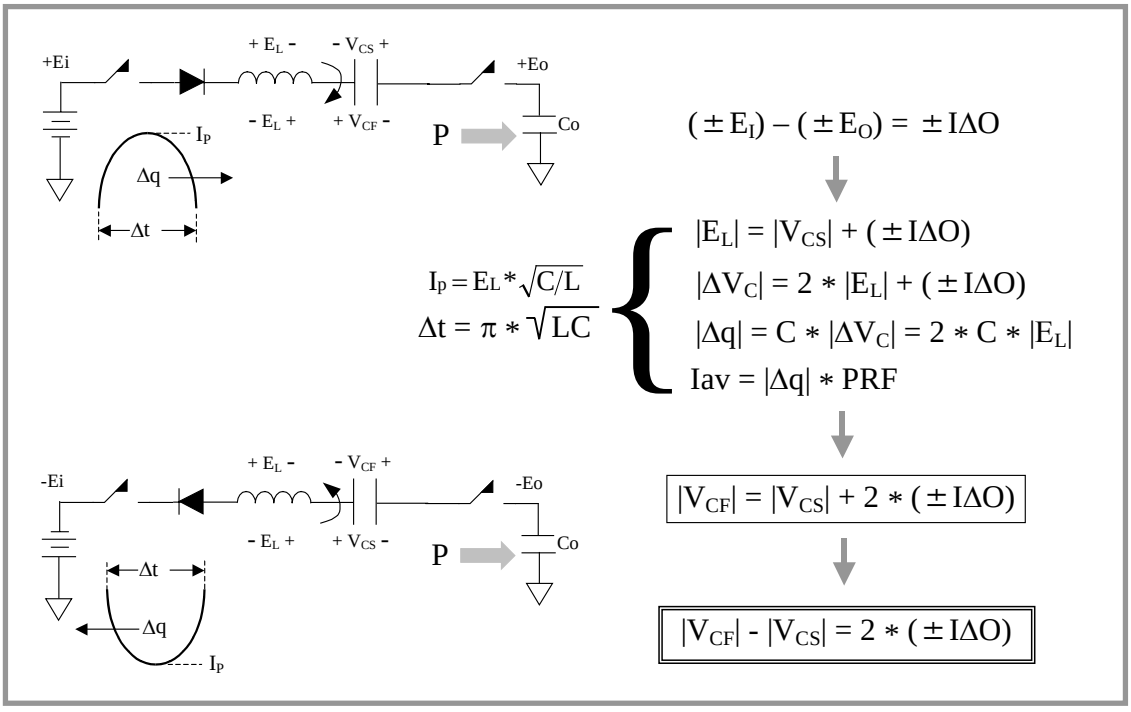
Figure 2. *ETM Converter Simple Block Diagram.*



In Figure 2, power may be transferred from any one of three inputs to any one of three outputs – hence the name *E*nergy *T*ransfer *M*ultiplexer – using one input and one output phase switches. Based on the initial conditions of resonant capacitor voltage and the voltages of the phases connected to the L-C circuit, a resonant current (*i(t)*) will flow. Again, depending upon the initial conditions, *i(t)* will flow from input-to-output or output-to-input with a given peak magnitude. Resonant current *i(t)* flows according to the equations shown in Figure 3. The remaining ground-connected power switches are utilized to "manage" the voltage on the resonant (shuttle) capacitor – in the case when both switches are activated, the polarity of the resonant capacitor may be reversed. There are several other factors that will influence the exact amount of charge that may be transferred at any given time, these being the magnitude of the input voltage and the voltages applied to the POWER FACTOR, SPEED and PITCH analog inputs. The voltage supplied by a voltage generator varies linearly with its' rotational speed. However, the available power can vary as the cube of the wind velocity. This means that

the power rating of the converter (in our case 34kW) is only available when the generator is rotating at or near its' maximum rotational speed. At lower rotational speeds, the current delivered by the ETM is limited in order to match the actual generator transfer characteristic (as programmed in the "PERSONALIZATION" set-up screen).

Figure 3. *ETM Converter Power Flow Equations.*



Along with the equations shown in Figure 3, the descriptive nomenclature shown in Figure 4 is also required.

Figure 4. *ETM Converter Power Flow Equation Nomenclature.*

Quantity	Description	Units
$\pm \mathbf{E_I}$	Positive or Negative Input Potential	Volts
$\pm \mathbf{E_O}$	Positive or Negative Output Potential	Volts
$\mathbf{E_L}$	Initial or Final Inductor Potential (Note that $E_{LI} \equiv E_{LF}$)	Volts
$\mathbf{V_{CS}}$	Initial Capacitor Potential	Volts
$\mathbf{V_{CF}}$	Final Capacitor Potential	Volts
$\mathbf{I\Delta O}$	Input-to-Output Potential Difference	Volts
$\lvert V_{CT} \rvert$	Total Potential Change on the Capacitor (Example if $-V_{CS}+ = 100V$ and $+V_{CF}- = 200V$, then $\lvert V_{CT} \rvert = 300V$)	Volts
$\lvert X \rvert$	Absolute Value of Quantity *X* Without Regards to Polarity	--
Δq	Charge per Pulse ($\Delta q = I_{average} * \Delta t$), where Δt is the pulse duration	Coulombs
PRF	Pulse Repetition Frequency	Hz
Energy Flow	$\Delta q * E * PRF$	Watts
Energy per Packet	$\Delta q * E$	Joules

The examination of the equation set in Figure 3 makes it clear that the peak value of the resonant current sinusoid is proportional to the instantaneous input-to-output voltage differential (when the power switches are closed and the initial capacitor voltage:

$$Ip = E_L * \sqrt{C/L}\ ,\ \left|E_L\right| = \left|V_{CS}\right| + \left(\pm I\,\Delta\,O\right);$$

$$Ip = \left(\left|VCS\right| + \left(\pm I\,\Delta\,O\right)\right) * \sqrt{C/L} \qquad \textbf{(EQ 1)}$$

The previous equation (**EQ 1**) is a re-verification of the concept of "voltage management" for the resonant (shuttle) capacitor in order to transfer the requisite charge. For the 34kW ETM Converter prototype, L = 40uH and C = 1.0uF. so $(C/L)^{0.5}$ = **0.158**, and the resonance time (per half resonant cycle) is $\pi * \sqrt{L * C} =$ 19.8us ~ **20us**.
The quantity $\pm I\,\Delta\,O$ is defined as the input-to-output voltage differential. The input voltage is a variable voltage and frequency sinusoid, and the output voltage is a

(reasonably) fixed voltage (V_p = 390.6V) and fixed frequency (60Hz) sinusoid. Thus, $I\Delta O(t)$ can be expressed as the difference of these two sine waves:

$$I\Delta O(t) = V_p(in) * [\sin(\omega t + \varphi)] - V_p(out) * [\sin(377t)] \quad \text{(Volts)}$$

b.) ETM Rules-Based Operation.

The operation of the ETM Converter is rules-based. The rules apply to the manner in which current is transferred from a particular input to a particular output. The flow chart shown in Figure 5 simplifies the operation of the ETM converter on a cycle-by-cycle basis. However, it does not state all the rules under which the ETM must operate. The rules are summarized as follows.

ETM Operational Rules:

R1.) Only one input-side and one output-side power switch (IGBT) shall be ON at any given time. Circuitry is included in the ETM converter control to prevent the simultaneous conduction of two (or more) input-or output-side IGBT power switches. Nonetheless, any code from the microcontroller that would cause simultaneous power switch conduction will result in NO SWITCHES BEING CLOSED – a situation where no power is transferred for the intended resonant cycle.

R2.) Provide as much power as possible to the output. The maximum allowable power is dictated by the power available at the input at a given rotational frequency, $P_{in}(f)$.

R3.) Keep the power factor of the Input as close to unity as possible. Power transfer is maximized when the generator power factor is unity.

R4.) Keep the average current provided to each output equal (i.e. balanced). The phase currents shall be balanced to within 5% over one cycle's transfer. The purpose of the ETM power conversion is to provide balanced current into a balanced line utility. Balance may be accomplished by equalizing the pulse repetition factors (over each 60Hz cycle) to all three output phases.

R5.) Above the knee frequency, a 5% maximum input phase voltage sag (over the idea nominal open circuit voltage) is tolerable. This sag is tolerable

over a three cycle maximum time period and may be corrected "on the fly" as an average, rather than on a resonant pulse-by-pulse basis.

R6.) Keep the pulse repetition frequency (PRF) as high as possible. This rule is adjunct to rule R2.

R7.) There shall be a minimum 2us wait time between resonant pulses. This dead time is required to allow for optimum switching turn-on/-off times. It is set to 2us for the prototype and may be lessened as a result of operational performance.

R8.) The output power factor shall vary according to the voltage present on the "POWER FACTOR" analog input (see Figure 5). The voltage scale as shown in Fig. 5 is determined from the input given in the "Personalization" User Input data screen.

R9.) **The output current delivered to each phase shall vary sinusoidally.** This rule is adjunct and subordinate to R7.

R10.) Never let the absolute voltage magnitude on the resonant (shuttle) capacitor exceed 1500V peak. Voltages beyond this level will damage the power switches and the capacitor.

R11.) Always open the power switches at or very near zero current. The ETM converter is by design a zero current switch and switching at zero current minimizes stresses on the power switches and other power train components. Signals are provided to detect the zero crossing of the resonant current waveform.

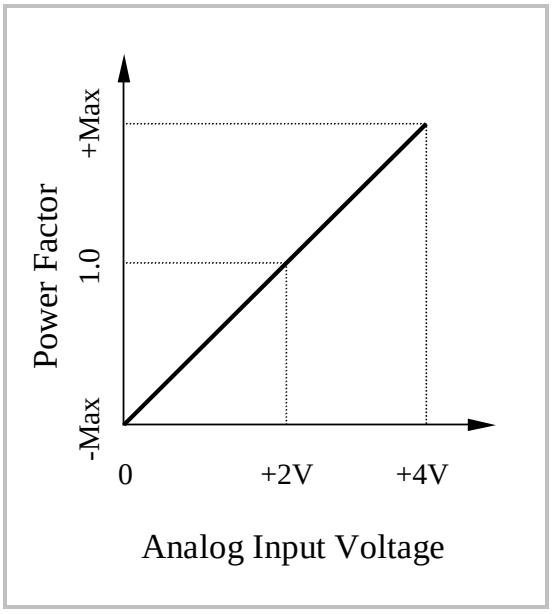
R12.) During shutdown and idle times when the ETM converter is OFF (i.e. delivering zero power), the two ground power switches shall be closed. This is to insure that the resonant capacitor discharges to and maintains a constant safe voltage potential level.

R13.) The operation of the ETM Converter shall be independent of the input generator phase (A,B,C) or utility line output phase (a,b,c) connected to any input or output of the ETM converter. The converter shall be fully functional with any random generator phase connected to any phase input or random utility phase connected to any phase output. This rule does not apply to the prototype.

c.) POWER FACTOR Analog Input Transfer Function.

The transfer function of the POWER FACTOR analog input is shown in Figure 5. The values of –Max and +Max are set according to those values entered in the "PERSONALIZATION" menu. The nomenclature for power factor is a minus (-) number indicates a leading (i.e. capacitive) power factor and a positive number (+) number indicates a lagging (i.e. inductive) power factor.

Figure 5. *POWER FACTOR Analog Input Transfer Function.*



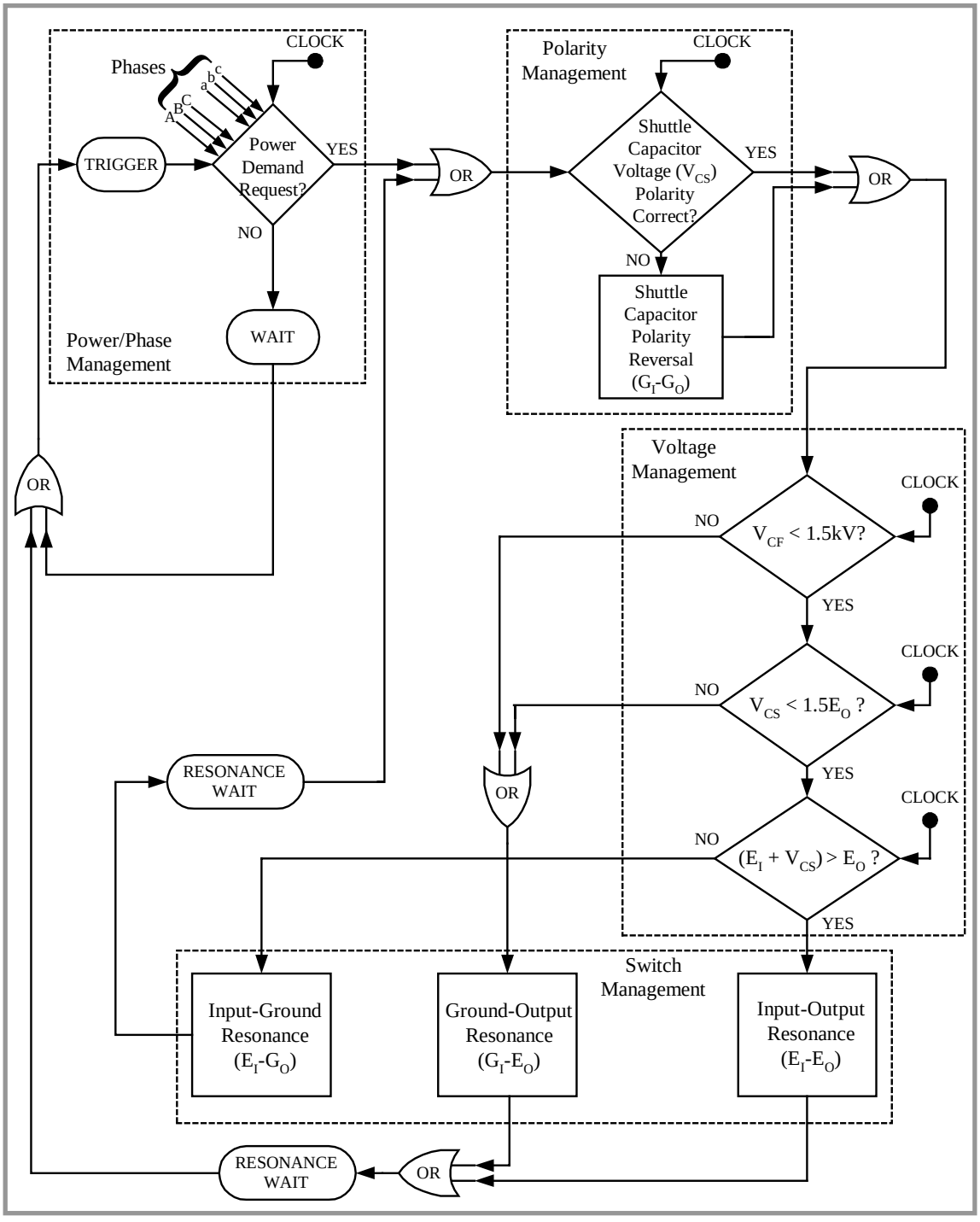
d.) SPEED Analog Input Transfer Function.

The SPEED input will not be utilized in the prototype ETM converter.

e.) PITCH Analog Input Transfer Function.

The PITCH input will not be utilized in the prototype ETM converter.

Figure 6. *ETM Converter Power Flow Chart.*



NOTE: *Never exceed the maximum resonant capacitor working voltage of 1500V!*

V.) Hardware Configuration and Considerations

The ETM converter is based around the Microchip dsPIC30F6011 (U1) and Analog Devices ADSP-2186 (U7) microcontrollers. These devices were chosen for their high I/O pin count, analog input capability and high clock speed (40MHz, max.). In the ETM converter application, both clock frequencies will be set at 20MHz. The dsPIC device will act as the real time processor (RTP). It will perform all the calculations required by the operating rules and execute the general operational flow shown in Figure 6. It will also be responsible for housekeeping and communications with the I2C devices and the RS-232 interface. The ADSP-2186 will have a single purpose function, as it will only be responsible for the IGBT power switch state control. It will be programmed such that it will insure that the proper switch closure sequence will be observed for all possible input voltages and frequencies. The ADSP-2186 device will accept commands to change the pulse repetition frequency (PRF) or to cease pulsing (in the case of a fault detected by the dsPIC device). Additionally, the ADSP device will control the initialization of the IGBT control bus PAL device (U7) at power on, and it will control the activation of the biasing power to the input and output quad IGBTs via the signals **IQDR** and **OQDR**. Finally, the communications between the dsPIC and ADSP microcontrollers will be accomplished via a private serial data bus (signals **SDO, SDI, SCK,** and **SS**). The control signals (**DSPINT0, DSPF1 and DSPF2**) are included to handle the handshake requirements of the bidirectional intra-processor data bus. The connections used for this processor to processor interconnect is shown in Figure 7.

a.) Switch State Control

The ADSP-2186 microcomputer (U7), using the general purpose I/O pins available on the memory IC U8, will be responsible for controlling the switch state and sequencing of the power switches. Using a software algorithm, U7 will serve as a an electronic “flywheel” – making sure that the proper switch state and sequence is observed at all power levels. Since it is highly undesirable to have two input or output power switches “ON” simultaneously, a PAL device (U9) has been incorporated into the gate drive circuitry as a “fail safe” option – it only allows the activation of a single switch in the input or output power switch quartets. If two or more bits in the data ranges **U8:*PA0-PA3*** (**IGD0-IGD3)** or **U8:*PA4-PA7*** (**IGD4-IGD7)** are “1” at any given time, then all “0”s are passed to the driver inputs of the IGBTs, turning them all OFF. This disabling of the power switches wastes a switching opportunity,

but protects all the power switches from unintentional destruction. Individual switch activation is determined according to the rules and previous equations, and Table I describes the data bit and control selection for the gate drive signals.

Figure 7. *U1-to-U7 Interconnections*.

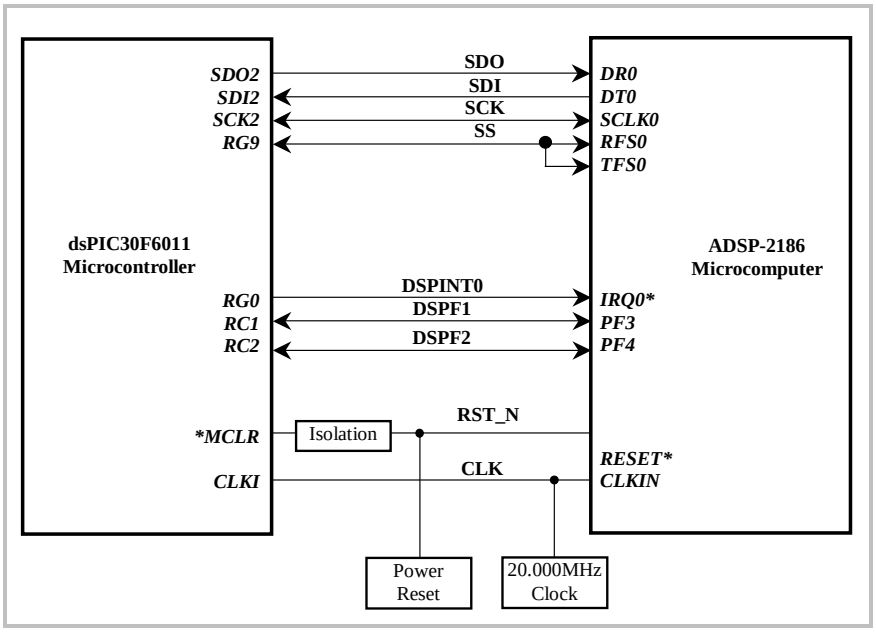
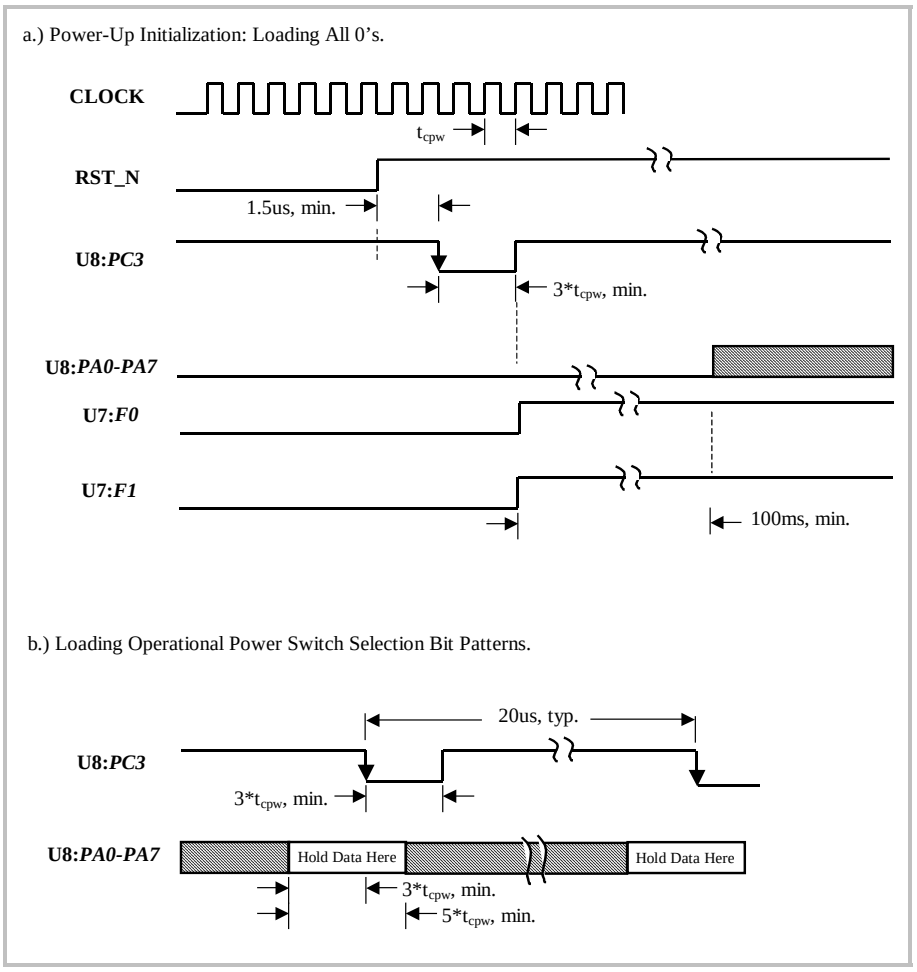


Table I. *Power Switch Selection Information.*

Power Switch Activated	Description	Logic Inputs / Outputs (*F0*=*F1*=H)								
		D0 (IGD0)	*D1* (IGD1)	*D2* (IGD2)	*D3* (IGD3)	*D4* (IGD4)	*D5* (IGD5)	*D6* (IGD6)	*D7* (IGD7)	*U8:PC3* (U9CLK)
None	Zero Load	L	L	L	L	L	L	L	L	↓
AD1	Input Phase A	H	L	L	L	X	X	X	X	↓
AD2	Input Phase B	L	H	L	L	X	X	X	X	↓
AD3	Input Phase C	L	L	H	L	X	X	X	X	↓
AD4	Input Ground	L	L	L	H	X	X	X	X	↓
AD5	Output Phase A	X	X	X	X	H	L	L	L	↓
AD6	Output Phase B	X	X	X	X	L	H	L	L	↓
AD7	Output Phase C	X	X	X	X	L	L	H	L	↓
AD8	Output Ground	X	X	X	X	L	L	L	H	↓
Any	Previous State	X	X	X	X	X	X	X	X	H
Any	Disabled	X	X	X	X	X	X	X	X	X

The timing for the power switch activation is shown in Figure 8.

Figure 8. *Power Switch Selection Timing.*

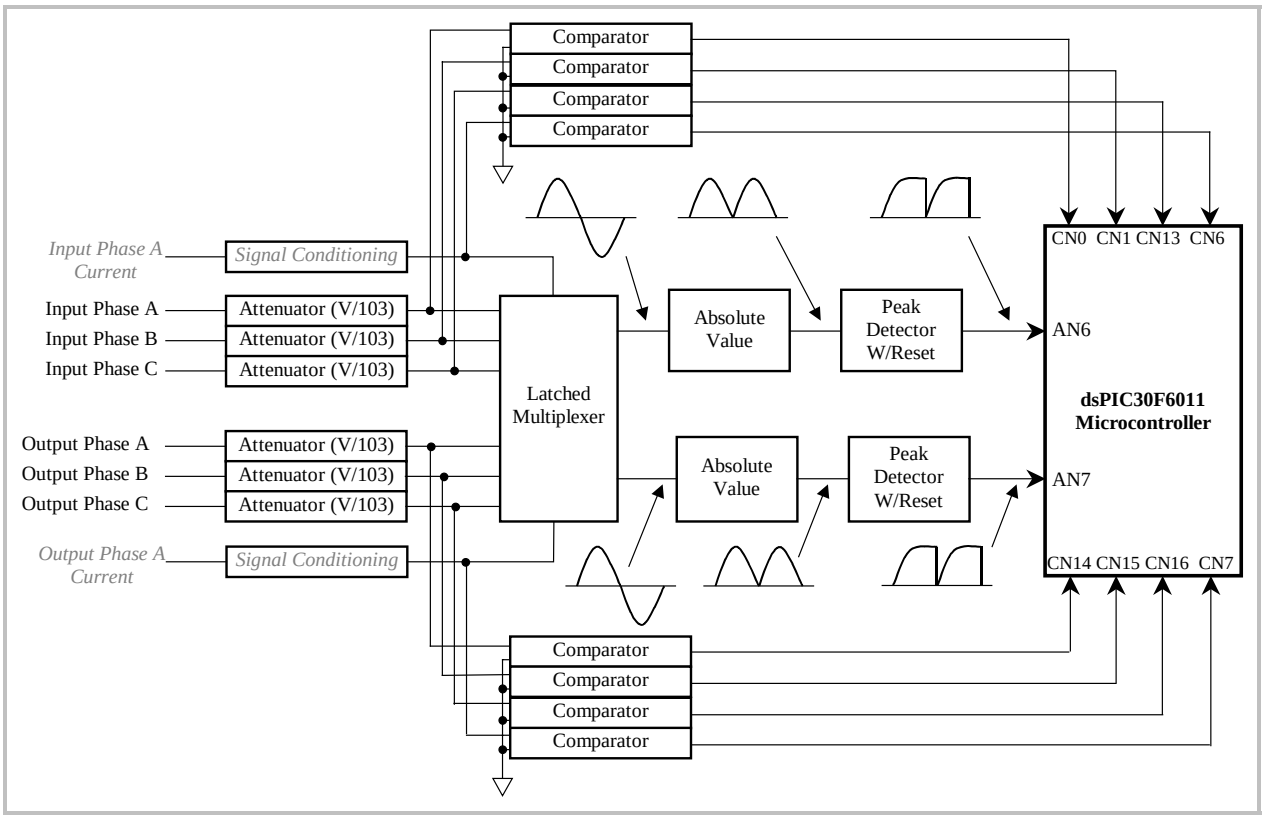


The power-up initialization sequence shown is required because the gate driver PAL (U9) initializes to an all 1's condition at power-up. The input and output quad IGBT enable bits ***F0*** (**IQDR**) and ***F1*** (**OQDR**) must only be activated (high) after PAL U9 is loaded with all 0's at power up. These two bits insure that no more than two IGBTs (one input side and one output side) can be on simultaneously. While in normal operation, the control bit **U8:*PC3*** should be used to enable/disable the power switches after each ~20us resonant pulse. The loading of data to the IGBT gate drive inputs is asynchronous with the master system clock. There are two possible techniques that may be used to determine when to open the power switches: the first is a software implementation whereby the power switches are activated and then after a fixed wait time of 20us the switches are opened; and the second is to utilize the zero crossing detector included in the control circuitry. The operation of the zero crossing detector will be discussed in a following section.

b.) Input/Output Phase Voltage Measurement

Before we consider transferring any energy from input-to-output (or vice-versa), it is necessary to understand in which phase amplitude sequence the input and the output reside (see Appendix). To do this and prepare for an energy transfer, we need to measure the frequency, polarity and amplitude of each input and the output phase. The ETM converter control circuit is equipped with analog circuitry to attenuate, select, signal condition and sense the polarity of each input and output phase. The voltage present at each phase is attenuated such that the resultant peak-to-peak voltage is **Vo = Vphase/103**. The attenuated input phases and output phases are then multiplexed to a single output (in preparation for presentation to the PIC microcontroller). An absolute-value amplifier and peak detector then processes the multiplexed and attenuated voltage in order to configure the signal for conversion by the A/D converter within the PIC device. This peak-absolute value signal is passed to the microcontroller as signals "**PK_MAGI**" to input ***AN6*** and the multiplexed, peak value signal for the output phases is passed to the microcontroller as signal "**PK_MAGO**" to input ***AN7***. This multiplexer is latched in preparation to obtain the peak value of the selected input and output phase. Additionally, this peak value amplifier is hardware reset each half cycle of the input and output signal in order to detect the peak value of those voltage cycles that may be lower in magnitude than the previous. The block diagram of the signal flow from the phase inputs/outputs to the microcontroller is shown in Figure 9.

Figure 9. *Input/Output Phase Signal Processing and Flow.*



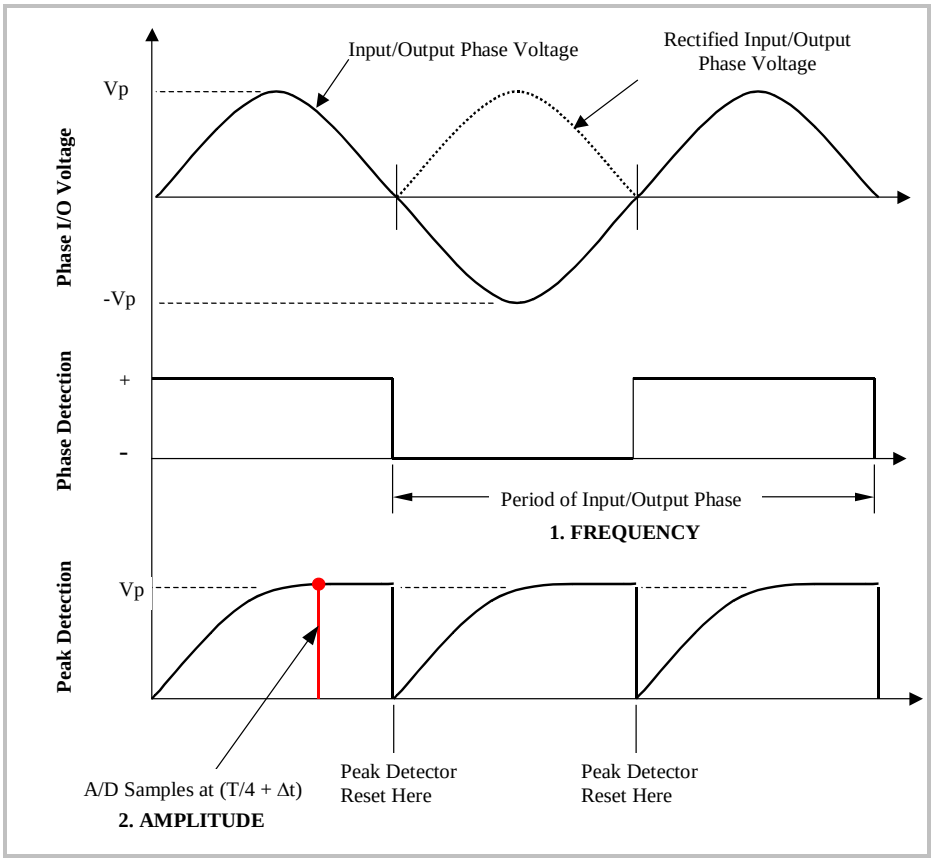
The information shown Figure 9 is used to determine: 1.) The polarity each phase of the input and output; 2.) The peak value of each input phase voltage and the phase A input current; 3.) The peak value of each) output phase voltage and the phase A output current; and 5.) The frequency of the input and output voltages and phase A current (from successive rising or falling edges of the **any *CNXX* signal**.

Once the voltage and frequency of the input and output voltages is known, then the time value of the amplitude and polarity may be determined at any time, via calculation, thus eliminating the necessity of sampling the waveform at each switching inflection point. This action helps to cut down on the A/D converter conversion time overhead and allows for a more economical number of A/D conversions to be utilized per cycle of power conversion by the ETM converter.

1.) *Predictive Frequency and Amplitude Control*.

In Figure 9 it is shown that there are several parameters regarding the input and output phase voltages that are obtained as real-time or sampled peak value signals. This particular set of data was chosen to satisfy the characteristics of the input and output phase voltages during normal operation of the ETM converter. In regards to the input, both the frequency and the amplitude of the voltage of the three phases will vary with time in relationship to the wind speed and strength. However, because of the mechanical characteristics of the wind turbine (inertia, momentum, etc.) and the nature of wind variations (d(windspeed)/dt), neither the amplitude nor the frequency of the voltage provided by the permanent magnet generator will change significantly on a line cycle-by-cycle basis. In short, impulse variations in the 16.67ms time range simply will not affect the input voltage or frequency. If we assume that a maximum voltage/frequency deviation of +/-3% (and likely very much less) may occur from cycle-to-cycle of a particular input phase, then we may use a predictive means for determining the time-varying (sinusoidal) amplitude of any of the phase inputs from the set of parameters determined in Figure 9. Consider the waveforms shown in Figure 10. We know the instantaneous phase frequency from the ***previous*** cycle's information by measuring the time between successive **CNXX** signal rising–edge transitions. We can then use that frequency (again, it will not change appreciably in one cycle!!) to determine the peak measurement time of the phase voltage by the A/D converter. This time will be at the sine wave peak (T/4) plus a small wait, Δt to account for the +3% possible frequency variation. So, the A/D converter will then take a peak voltage reading on the next input cycle on a particular phase at the time ($T/4+\Delta t$) for phase A, ($T/4+5.6ms+\Delta t$) for phase B or ($T/4+11.2ms+\Delta t$) for phase C. In other words, just after the assumed peak for each phase. The frequency (1.) and amplitude (2.) obtained will be used (predictively) for the ***next*** cycle power processing, for the phase in question, for all three phases.

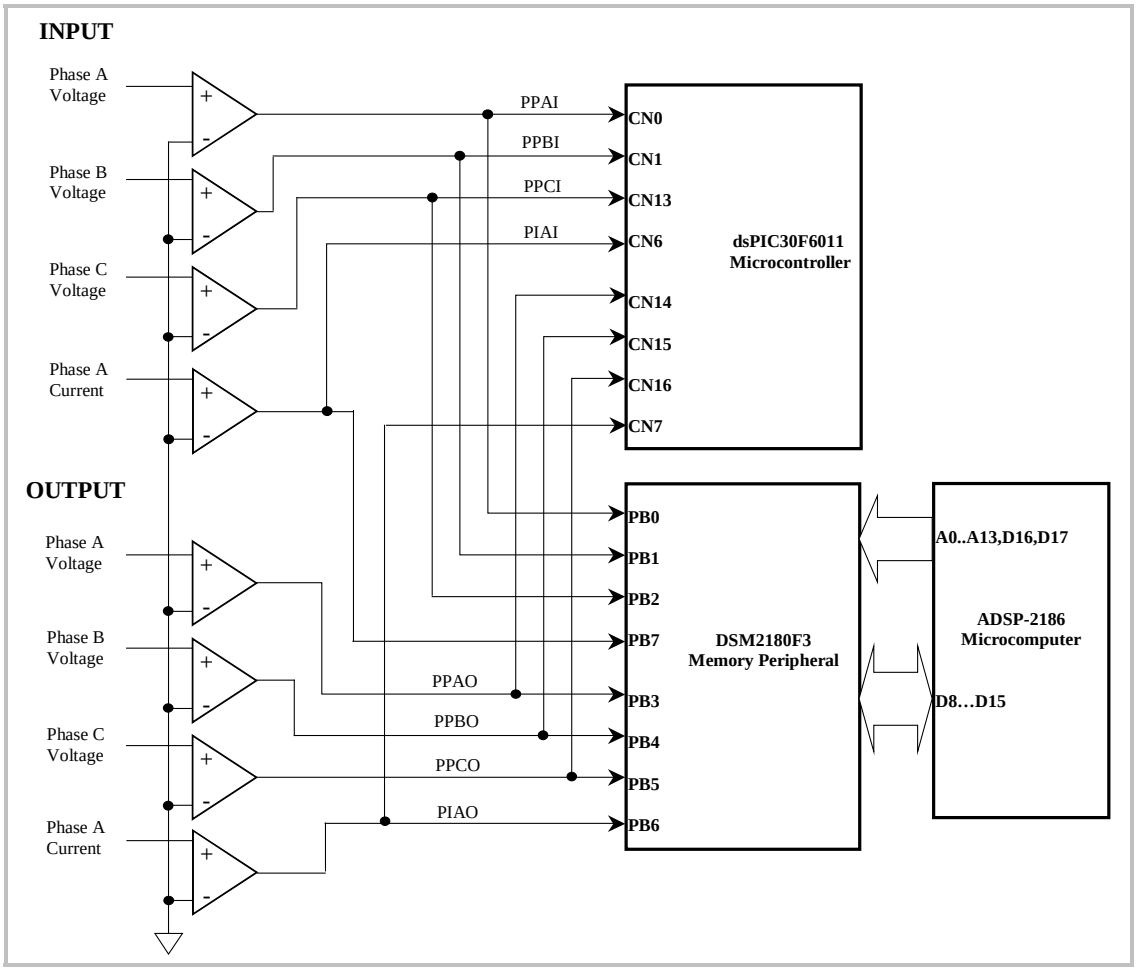
Figure 10. *Predictive Frequency and Amplitude Control Waveforms.*



c.) Phase Polarity Measurement

In order to properly determine the correct power switch switching criteria, it is essential to know the phasor placement of each input and output voltage phase. [The Appendix discusses how the resonant pulse PRF (to and from each phase) changes as each phase transitions from one quadrant to another.] In order to facilitate faster real time decision making within the microcontrollers, six comparators which monitor the individual phase voltage polarities and two comparators which monitor the phase A input and output current polarities, are included in the control circuitry to report these polarities to the microcontrollers. The output from these comparators is provided to each microcontroller as an eight bit word, as shown in Figure 11.

Figure 11. *Input/Output Polarity Signal Interconnections*.



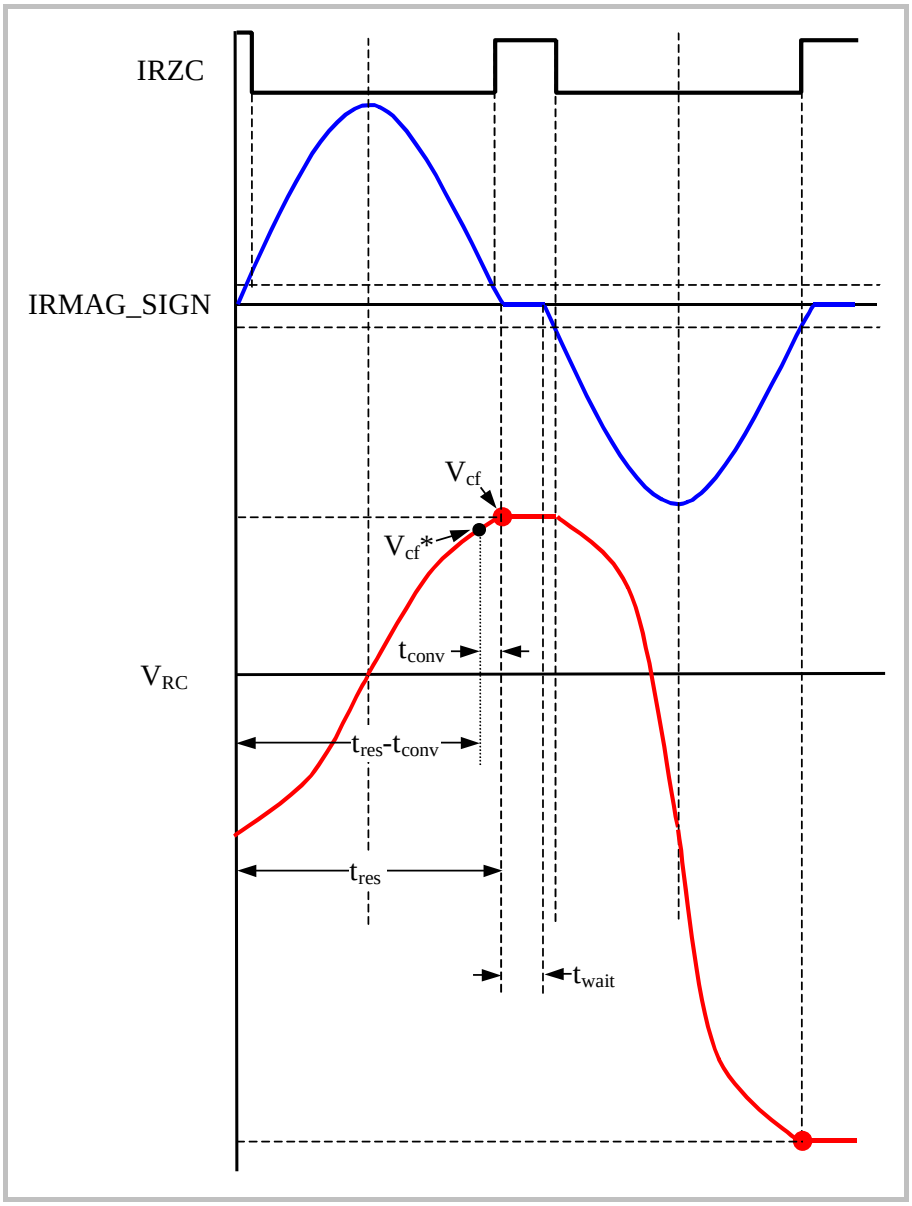
d.) Resonant Capacitor Voltage and Polarity Measurement

The key to the ETM power conversion process is the ability to "manage" the starting voltage (V_{CS}) on the resonant capacitor on a resonant cycle-by-cycle basis. Although the capacitor voltage may be accurately calculated (see Figure 3) after each resonant pulse by just measuring the input-output differential, it is desirable to have the ability to directly measure the resonant capacitor voltage. Such ability is included in the ETM control circuitry. A differential amplifier, whose inputs are attenuated by a factor of 534, samples the voltage potential of the resonant capacitor. The output of this differential amplifier is **$Vo = V_C/534$**. The differential output is passed an absolute value circuit and and analog-to-digital conversion is obtained by A/D converter UJ6. The serial output of this converter is passed to the ADSP-2186 (U7) microcontroller as signals "**AD_CS**", "**AD_SCLK**" and "**AD_SDATA**". The attenuated voltage is then sensed by a ground-

referenced voltage comparator to determine the polarity of this signal, which is passed to the ADSP-2186 microcontroller, as the high-true signal "**CR_POL**", to input ***PF6***. The "CR_POL" signal is high when the resonant capacitor voltage is polarized positive with respect to the output and negative with respect to the input – i.e the capacitor is polarized to make an energy transfer to a positive output phase voltage.

The capacitor voltage shall be sampled according to Figure 12.

Figure 12. *Resonant Capacitor Voltage Measurement Timing.*



The A/D converter shall be caused to convert at time (t_{res}-t_{conv}). The voltage sampled at this time is V_{CF}*. For the remainder of this analysis, we will assume an **SCLOCK** frequency value of 10MHz. Since the conversion time is 1.2us for an **SCLOCK** value of 10MHz, then the value of V_{CF}* is 95% of the actual final value, V_{CF}. Thus, to obtain the value of V_{CF}, it is necessary to multiply the A/D converter result by 1.05. The A/D conversion terminates coincident with the end of the resonant period, t_{res}. This action leaves the entire wait time, t_{wait} = 2us, for the ETM converter algorithm code execution and determination of the subsequent power switch closure.

e.) A Word on Phase and Capacitor Voltage and Polarity Measurements

Although it is desirable to have amplitude and polarity measurements of each input and output phase on a cycle-by cycle basis (at the 60Hz operating frequency), it is not absolutely essential. Amplitude and polarity information may be obtained on a "timely" basis depending upon the microcontroller activity load. Several cycles of measurements may be skipped while extrapolating the voltage time relationship for a particular input or output. The time may vary depending upon the verified accuracy of the extrapolation: the better the extrapolation, the lower the frequency of voltage and polarity measurements.

The resonant capacitor voltage and polarity should be measure on a resonant pulse-by-pulse basis so as to absolutely insure that the converter may maximize the transfer of energy from the input(s) to the output(s). Additionally, the capacitor voltage must ***never*** be allowed to exceed 1500V peak. To this end, a comparator circuit is included in the analog hardware to continuously measure the resonant capacitor voltage and report if this voltage exceeds the 1500V peak limit. The comparator circuit is comprised of UJ1 and UJ4. The digital-to-analog converter UJ1 is included as a variable reference for the resonant capacitor overvoltage comparison, and its output shall be set to a value of 1500/534 = 2.81Vdc. The output of this serial input D/A converter is set by signals "**DINDA**", "**SCLKDA**" and "**CSDA2_N**", and these signals are provided to DSP microcontroller U1 on pins ***SCK1***, ***SDO1***, and ***RD3,*** respectively. The output of this D/A converter serves as the reference voltage to which the attenuated and absolute-valued resonant capacitor voltage is compared by UJ4. The output of this comparator is signal "**VRC_OV_N**". This signal is high when the capacitor voltage exceeds the limit as set by

D/A converter UJ1. The signal "**VR_OV_N**" is provided to the DSP microcontroller U1 on pin ***OC2/RD1*** and to the memory peripheral U8 on pin ***PC4***.

f.) Analog Signal Selection for the dsPIC Microcontroller

The various analog voltage signals are selected with multiplexers controlled by the PIC microcontroller. The absolute-valued and peak stored absolute-valued signals are directed to the dsPIC30F6011 via the following truth table as shown in Table II.

Table II. *Analog Signal Selection Information.*

Microcontroller Input Signals		**Logic Signals**			
Signal	**dsPIC30F6011 Input**	***RG12*** **(MSA)**	***RG13*** **(MSB)**	***RG14*** **(MSC)**	***RG15*** **(MSL)**
$\|V_{in}\|/103$, Input Phase A	***AN6***	0	0	0	1
$\|V_{in}\|/103$, Input Phase B	***AN6***	1	0	0	1
$\|V_{in}\|/103$, Input Phase C	***AN6***	0	1	0	1
$\|I_{in}\|$, Input Phase A	***AN6***	1	1	0	1
$\|V_{out}\|/103$, Output Phase A	***AN7***	0	0	1	1
$\|V_{out}\|/103$, Output Phase B	***AN7***	1	0	1	1
$\|V_{out}\|/103$, Output Phase C	***AN7***	0	1	1	1
$\|I_{out}\|$, Output Phase A	***AN7***	1	1	1	1
Previous Input Selected at ***RG12(t=0)***, ***RG13(t=0)*** Latched	***AN6***	X	X	X	0
Previous Output Selected at ***RG12(t=0)***, ***RG13(t=0)*** Latched	***AN7***	X	X	X	0

g.) ETM Converter Operating Mode

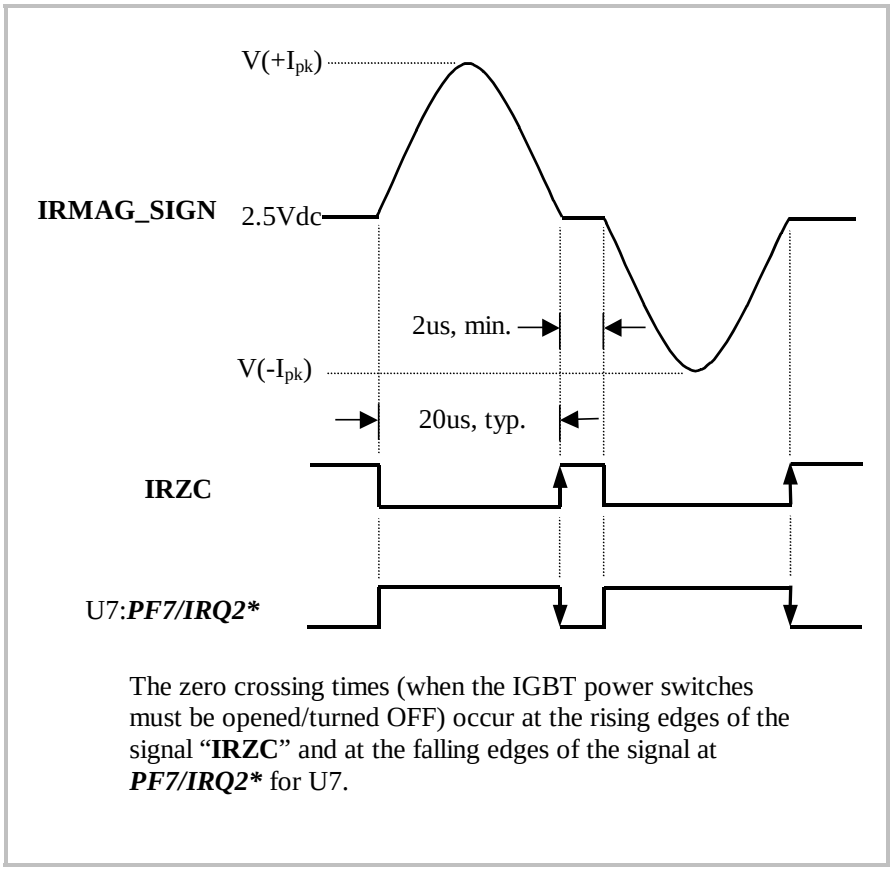
The ETM Converter shall be provisioned in software for two modes of operation. The first is ***synchronous*** mode, whereby the converter is caused to switch every $((1/t_{res})+2us)$. This mode requires that t_{res} is either known *a priori* or measured. It is preferred that t_{res} be measured during the start-up/housekeeping phase of the converter's operation. The second is the ***asynchronous*** mode, whereby the converter is caused to switch at the falling edge occurrences of the signal "**IRZC"**, provided as signal "**NIRZC"** to microcomputer U7 on input ***PF7/IRQ2****. This is a falling-edge triggered (i.e. 1-to-0 transition) zero crossing indication used as the "end of current pulse" trigger.

In order for proper zero-crossing detection, the circuit must be calibrated to the current sensor in order to set the required detection levels. This calibration must be done as part of the turn-on/housekeeping process of microcontroller U1, described in a later section. The process for setting the zero crossing threshold window is as follows:

1.) Using analog input ***AN8***, measure the resonant current sensor reference voltage level (2.50Vdc nominal), which is signal "**BIRVREF"**. This signal is Vref.
2.) Set the upper detection threshold to (Vref + 10 LSBs) by loading the appropriate input code to D/A converter, U24, for analog output OUTA. The 10 LSB code equates to an approximate 50mV positive threshold offset. The input code is presented to the D/A converter serially via signals ***RD2*** ("**CSDA_N"**), ***SDO1*** ("**DINDA"**) and ***SCK1*** ("**SCLKDA"**) – the chip select, serial data and serial clock inputs, respectively. See the TLV5637 (U24) data sheet for details.
3.) Set the lower detection threshold to (Vref – 10 LSBs) by loading the appropriate input code U24 for analog output OUTB. The 10 LSB code equates to an approximate 50mV negative threshold offset.

After the zero current calibration, the IRZC signal will reflect the time when the resonant current enters the zero current detection band.

Figure 13. *IRZC and PF7/IRQ2* Timing at Resonant Current Zero Crossing.*



The zero crossing times (when the IGBT power switches must be opened/turned OFF) occur at the rising edges of the signal "**IRZC**" and at the falling edges of the signal at ***PF7/IRQ2**** for U7.

Additionally, the actual resonant current time may be determined by measuring the time from a falling edge transition (1-to-0) to a rising edge transition (0-to-1) of the "**IRZC**" signal. If at any time the resonance current time increases or decreases by +/-10%, then this indicates a fault condition and the converter shall be immediately shut down.

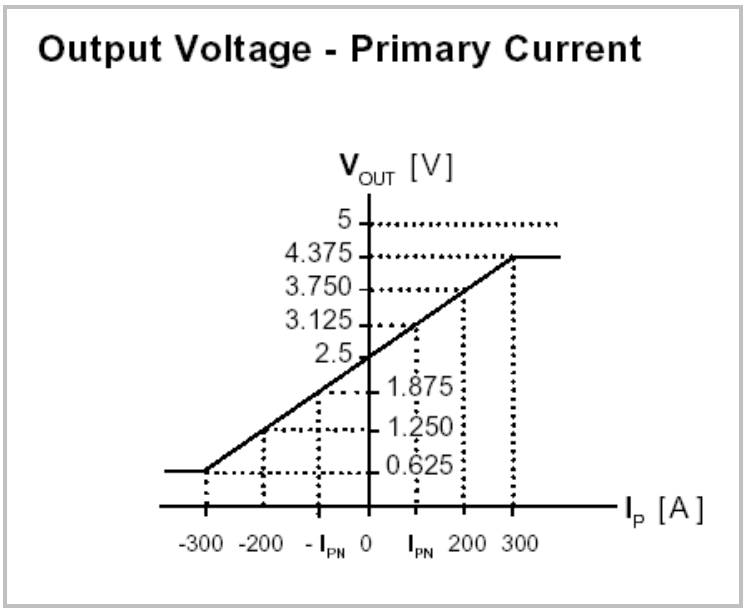
h.) Current Measurement

The ETM converter is provisioned with current sensors to measure the input and output currents for Phase 1 (which will be representative for all three input phases given the balanced nature of the ETM conversion).

The Phase 1 input sensor allows the determination of the input power factor. Keeping the input power factor (at 60Hz) close to unity is essential for deriving maximum efficiency from the generator. The Phase 1 input current sensor is input to the U1 microcontroller on analog input ***AN6*** and the Phase 1 output current sensor is input to U1 microcontroller on

analog input ***AN7***. Both sensors (LEM LAS 100-TP) have the output transfer characteristic as shown in Figure 13.

Figure 14. *Current Sensor (LAS 100-TP) Output Transfer Characteristic*.



The sensor characteristic demonstrates that its' output voltage signal contains both amplitude and polarity information. And the zero crossing of the current that is sensed may be detected at the time when the sensor output reaches 2.500Vdc. The sensor output voltage is described by the following equation over the range of $-300A < I_{sense} < +300A$:

$$V_o = 0.00625*(I_{sense}) + 2.5 \qquad \text{(Vdc)}$$

The sensors output(s) are level –shifted to 0V from 2.50Vdc, and the absolute value the signal is obtained, and peak held. This means that the equation for the sensor output voltage is:

$$V_o = 0.00625*(I_{sense}) \qquad \text{(V)}$$

i.) Startup, Housekeeping and State Control

At initial power up/startup the ETM converter shall be in a locked "STOP" state until the microcontrollers performs the following tasks:

1.) ETM Converter Housekeeping at Turn On

The premier event to be accomplished when the ETM converter initializes at turn on is the initialization of the gate control PAL, U9. When the PAL U9 initializes at turn on, all 1's are loaded to the gate driver outputs in order to properly initialize the internal registers within the PAL device. At microcomputer U7 power on, the IGBT Gate drive signals from U7 and U8 shall be disabled (via ***PC3:*****U8, *F0:*****U7 *and F1:*****U7** all set to "0") to insure that the IGBTs remain disabled until the PAL is set to the all "0s" condition. The PAL U9 should then be initialized and the IGBTs activated according to the timing sequence shown in Figure 8.

The remaining housekeeping tasks (all executed by the dsPIC microcontroller U1) consist of (in no particular order of importance):

- Performing a single resonant transfer event to obtain the measured value of t_{res}. Assuming the capacitor voltage is zero (0.0V) at startup, then a resonance event can be initiated by closing the input ground switch and an output switch associated with a positive output voltage (phase voltage). Only one pulse need be done to measure the time from a 1-to-0 transition until a 0-to-1 transition of the signal IRZC. This time, plus a processing time of 300ns is the time period t_{res}. After the single pulse event, the input and output ground switches shall be closed to reset the resonant capacitor to the fully discharged initial condition. There shall be a wait time of at least 1ms before any other switching may commence.
- Monitoring/establishing an RS-232 communications link with the host PC.
- Monitoring the Chassis Fan Fault input to monitor for a possible failure (A fan fault is indicated by a logic high ("1") on microcontroller logic inputs ***RRD8/INT1*** or ***RD9/INT2***.
- Initializing the I2C communications bus.
- Calibrating the resonant current sensor zero crossing circuit serial D/A converter, per Section V, subsection g.).
- Setting the Resonant Capacitor Overvoltage comparator reference serial D/A converter to a value of 2.81Vdc (for a maximum value of 1500Vp).
- Determining the chassis temperature via the LM75 temperature monitor, U5 (If the chassis temperature is greater than 50°C, then the ETM converter may not be "START"ed).

- Monitoring the IGBT input and output quad fault signals (**ERRI_N** and **ERRO_N**) for a possible fault (An input quad fault is indicated by a logic low (“0”) on logic input ***RD10/INT3*** and an output quad failure is indicated by a logic low (“0”) on ***RD11/INT4***).
- Determining the system configuration (via the I2C bus) and communicating with other ETM converters present on the I2C data bus. The protocol for this communication will be explained in a following section.
- Measuring the input and output voltage magnitudes and frequencies (for all three phases).

2.) ETM Converter State at Turn On

As previously mentioned, the ETM Converter shall be in a “STOP” state until the housekeeping tasks are complete. In order to insure that it detects any fault conditions or to wait until any turn-on induced transient faults are resolved, the converter shall remain in the “STOP” state for a time period of no less that 10 seconds. During the 10 second fault wait period, the converter indicator LEDs shall be tested in a sequential manner such that they are blinked at a 2Hz rate each for a time period of no less than 2 seconds each, followed by the POWER indicator LED flashing at a 2Hz rate for the remainder of the fault wait period. If after the 10 second time period any fault is reported, the converter shall remain in a locked “STOP” state and report this condition to: the FAULT LED (steady indication), the host PC and to the other converters (if any) in the system via the I2C bus. If no faults are reported, then the converter is ready for “START” and this condition shall be reported to: the POWER LED (steady indication), the host PC and to other converters (if any) in the system.

j.) I2C Bus Configuration

The I2C bus is used to communicate with the temperature sensor, the 256KB personalization/ attributes memory (U2), the converter status LEDs (driven by U26), the system slot/presence and fault inputs and outputs (driven or detected by U26 and U27), and the external I2C expansion busses (generated by U28) to the remainder of the ETM converters in the power system. The ICs U26, U27 and U28 reside on the Analog motherboard portion of the ETM control circuit. The I2C bus configuration used in the ETM converter is shown in Table III.

k.) Memory Configuration and Control

The system memory device, U2, is accessed via the I2C bus and is a 256KB EEPROM. All personalization data information gathered during user input interrogatories shall be stored in this memory as well as manufacturing information pertaining to the PCB and system (dates of manufacture, serial number, revision level, etc.). The memory information is detailed in Table IV.

l.) Fault Reporting

In the prototype, fault reporting shall consist of illuminating the red FAULT LED (see Table III) when a fan, temperature or IGBT quad switch fault is detected. A temperature fault shall be reported when the chassis temperature exceeds 55°C.

m.) LED Indications

In the prototype, after the power on housekeeping wait time period has expired, the UNIDIRECTIONAL LED and the MASTER LED (see Table III) shall be set ON continuously as the prototype will be a stand alone unit and will be by definition the master and unidirectional by function.

Table III. *I2C Bus Configuration Information.*

Functionality	Reference Designator	I2C Bus Address	I/O Pin Identity	(I)nput/ (O)utput	Description
POWER LED	U26	101	I/O0	O	Green Power ON LED. Low True.
FAULT LED			I/O1	O	Red Fault Status LED. Low True.
UNIDIRECTIONAL LED			I/O2	O	Yellow Function Status LED. Low True.
MASTER LED			I/O3	O	Green Function Status LED. Low True.
Slot Detection Input 1			I/O4	I	Low True Inputs. Input will be low corresponding to slot in which it resides in the system.
Slot Detection Input 2			I/O5	I	
Slot Detection Input 3			I/O6	I	
Slot Detection Input 4			I/O7	I	
Present Indication 1	U27	110	I/O0	O	Reports individual converter presence status to the system chassis. High True.
Present Indication 2			I/O1	O	
Present Indication 3			I/O2	O	
Present Indication 4			I/O3	O	
Fault Detection I/O 1			I/O4	O	Reports individual converter fault status to the system chassis. Low True.
Fault Detection I/O 2			I/O5	O	
Fault Detection I/O 3			I/O6	O	
Fault Detection I/O 4			I/O7	O	
I2C Expansion Bus 0 SD	U28	111	SD0	I/O	Redundant I2C external expansion busses to the three other system converters and the system chassis.
I2C Expansion Bus 0 SC			SC0	O	
I2C Expansion Bus 1 SD			SD1	I/O	
I2C Expansion Bus 1 SC			SC1	O	
I2C Expansion Bus 2 SD			SD2	I/O	
I2C Expansion Bus 2 SC			SC2	O	
I2C Expansion Bus 3 SD			SD3	I/O	
I2C Expansion Bus 3 SC			SC3	O	

Table IV. *Memory Addressing Information.*

Device	Function	Mode	Comments
U2 (for timing see Microchip 24FC256 Data Sheet)	256KB Attributes and Personalization Data Memory	Write	***RC15*** = L: Programmed via I2C Bus: I2C Bus Address = 001
		Read	***RC15*** = H: Read via I2C Bus: I2C Bus Address = 001

n.) System Communications Protocol

The prototype will have no inherent capability to communicate with other ETM converters in a system configuration.

o.) System Attributes Data Storage

The ETM Converter has an EEPROM memory device (U2) attached to the I2C bus to capture attributes information (system serial number, date of manufacture, PCB numbers and revisions, etc.) of the system and the components in the system. The prototype will not use this capability.

APPENDIX

At any time in a cycle of a three phase signal triad, the peak voltages of the phases will have twelve different polarity combinations as shown in Table AI:

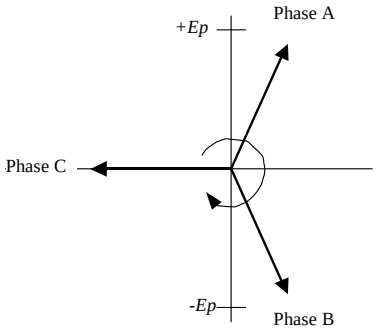
Table A1. *Three Phase Polarity Sequencing*.

Sequence	Phase A	Phase B (+120°)	Phase C (+240°)
1	Z	N	P
2	P	N	P
3	P	N	Z
4	P	N	N
5	P	Z	N
6	P	P	N
7	Z	P	N
8	N	P	N
9	N	P	Z
10	N	P	P
11	N	Z	P
12	N	N	P

These phase sequences will determine when power will be delivered from the input source to the output load. It should be noted that for an ETM converter, the output will always be connected to a 60Hz power grid of a known, fixed amplitude, whether the converter is unidirectional or bidirectional. The input, however, is connected to a generator whose output amplitude *AND* frequency vary with time. Thus, the ETM converter must extract energy from a time and amplitude varying three-phase input and transfer this energy as a fixed frequency current to the connected utility grid load. As a rule, power (resonant pulses) will be delivered singly and sequentially to each output phase in the when the ETM converter is in the unidirectional mode. Also, power will be taken from each input phase singly and sequentially. This rule insures that current is taken and delivered in a balanced manner from each individual input and output phase. Additionally, it is desirable to deliver power from the input and output that are closest in amplitude to one-another.

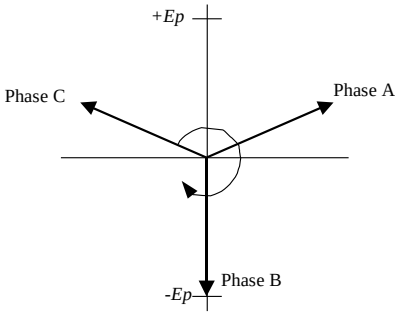
Figure A1. *PRF versus Phasor Voltage Relationship Illustration.*

time t=0: E(Phase A) = $+0.866E_p$
E(Phase B) = $-0.866E_p$
E(Phase C) = 0V



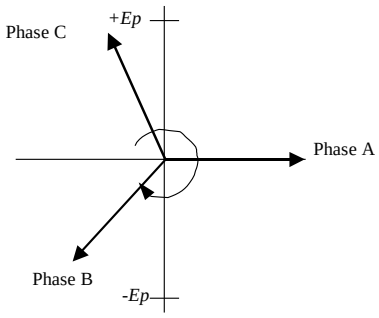
The PRF of positive resonant pulses to Phase A is equal to the PRF of negative resonant pulses to Phase B. The PRF to Phase C is obviously zero. This assumes a unity power factor.

time t=1: E(Phase A) = $+0.5E_p$
E(Phase B) = $-E_p$
E(Phase C) = $+0.5E_p$V



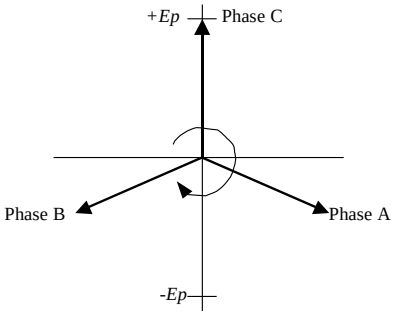
The PRF of positive resonant pulses to Phase A has decreased and the PRF of positive resonant pulses to Phase C has increased such that their PRFs are equal. The PRF to Phase B has increased to its maximum value. This again assumes a unity power factor.

time t=2: E(Phase A) = 0V
E(Phase B) = $-0.866E_p$
E(Phase C) = $+0.866E_p$



The PRF to Phase A is now zero and the PRF of positive resonant pulses to Phase C has increased such that its PRF is equal to the PRF of the negative resonant pulses to Phase B, which has decreased from the maximum value. This again assumes a unity power factor.

time t=3: E(Phase A) = $-0.5E_p$
E(Phase B) = $-0.5E_p$
E(Phase C) = $+E_p$



The PRF of negative resonant pulses to Phase A has now increased such that it is equal to the PRF of Phase B. The PRF of positive resonant pulses to Phase C has increased to the maximum value. This again assumes a unity power factor.

Figure A2 shows the PRF (duty cycle) versus phase angle over a single cycle for the three phases. Figure A3 is an example where three phase angles (times) for the PRF are considered.

Figure A2. *PRF Duty Cycle vs. Phase Angle.*

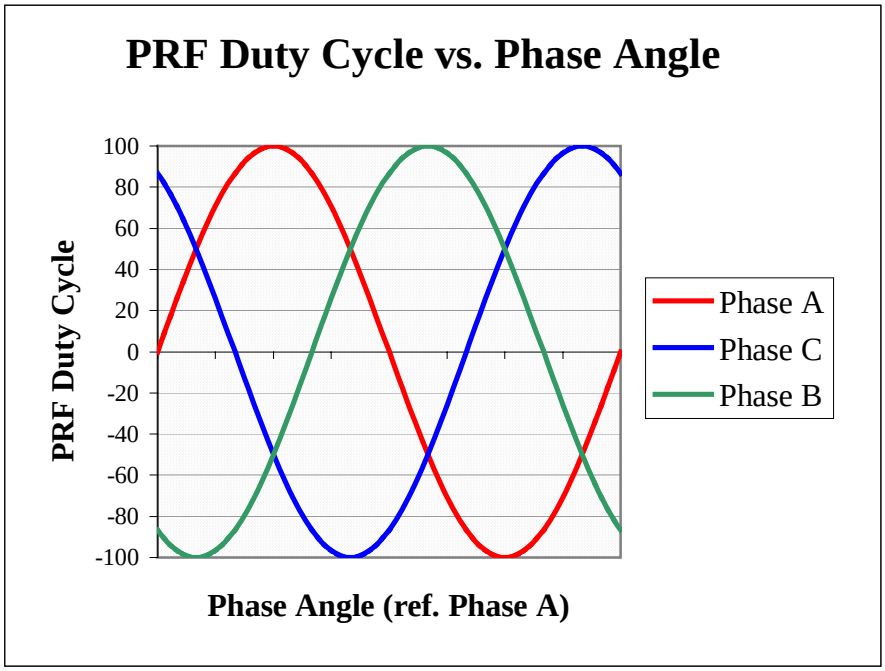
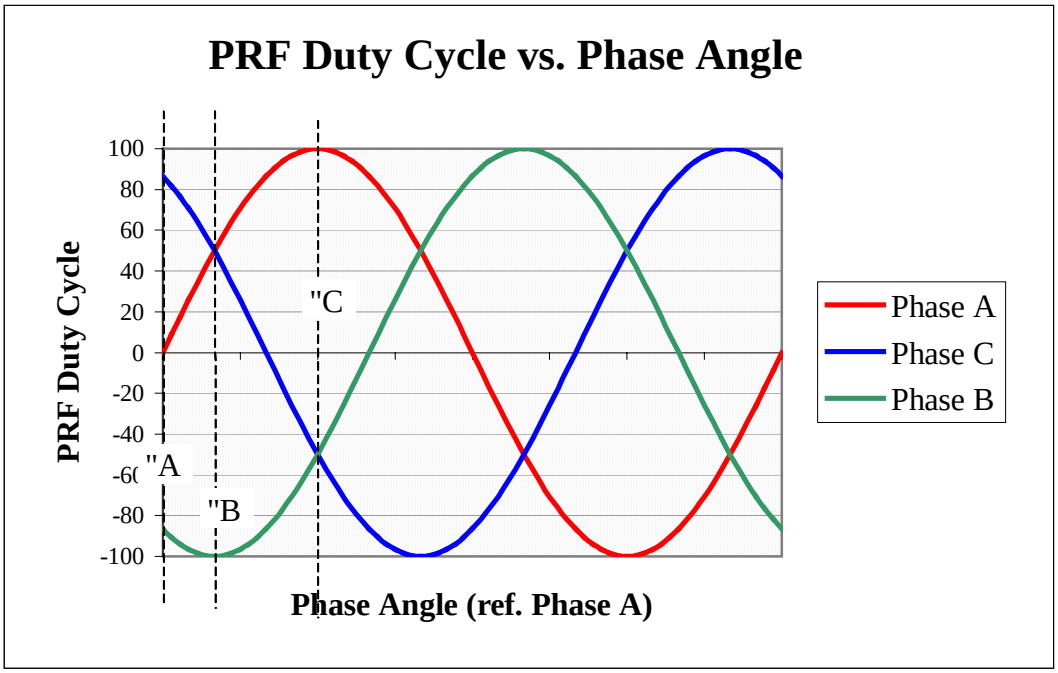


Figure A3. *PRF Duty Cycle vs. Phase Angle Example.*



At point “A”, at phase angle 0° (time t = 0), the PRF to Phase A is 0, to Phase B is 86.6% (of negative pulses), and to Phase C is 86.6% (of positive pulses). This means that for both the positive and negative pulses at this phase angle/time, 13.4% of the possible pulse opportunities are not used.

At point “B”, at phase angle 30° (t = 1.39ms for a 60Hz frequency), the PRF to Phase A is 50% (of positive pulses), to Phase B is 100% (of negative pulses), and to Phase C is 50% (of positive pulses). At point “B”, the positive and negative PRFs have risen to 100%.

Finally, at point “C”, at phase angle 90° (t = 4.17ms @ 60Hz), the PRF to Phase A is 100% (of positive pulses), to Phase B is 50% (of negative pulses), and to Phase C is 50% (of negative pulses). At point “C”, the positive and negative PRFs are at 100%.

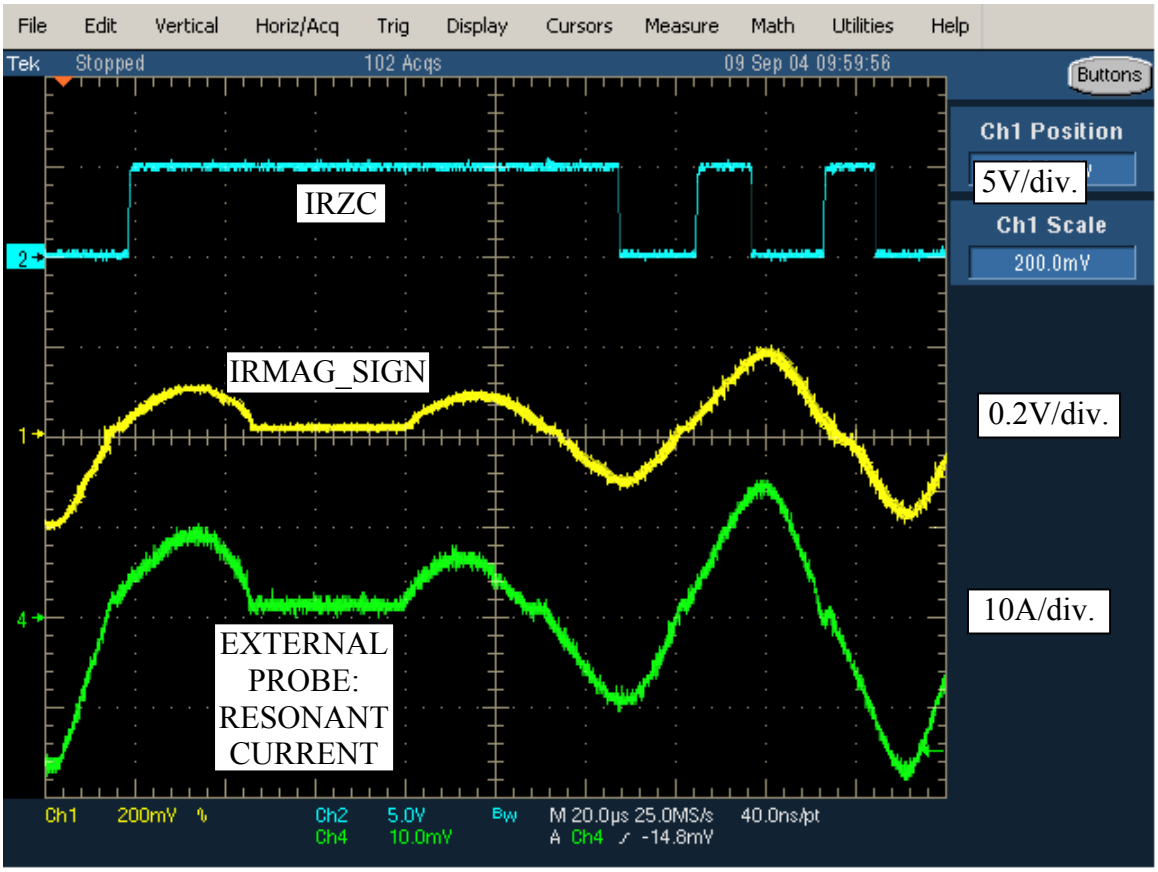
Thus, over a single cycle, the positive and negative PRFs vary between 86.6 and 100%, with the peak PRFs exactly 45° (2.08ms @ 60Hz) apart. And, interestingly enough, over the phase angle ranges 0-60°, 120-180° and 230-290°, the sum of the PRFs of positive pulses is equal to those of the negative pulses.

In conclusion, the energy transfer from any phase to any phase may be thought of in terms of a proportion at any time over a single waveform cycle. It will strictly obey the overall positive and negative PRF pulse proportions illustrated in the example of Figure A3, with the individual proportions following a similar proportionality over each cycle as well.

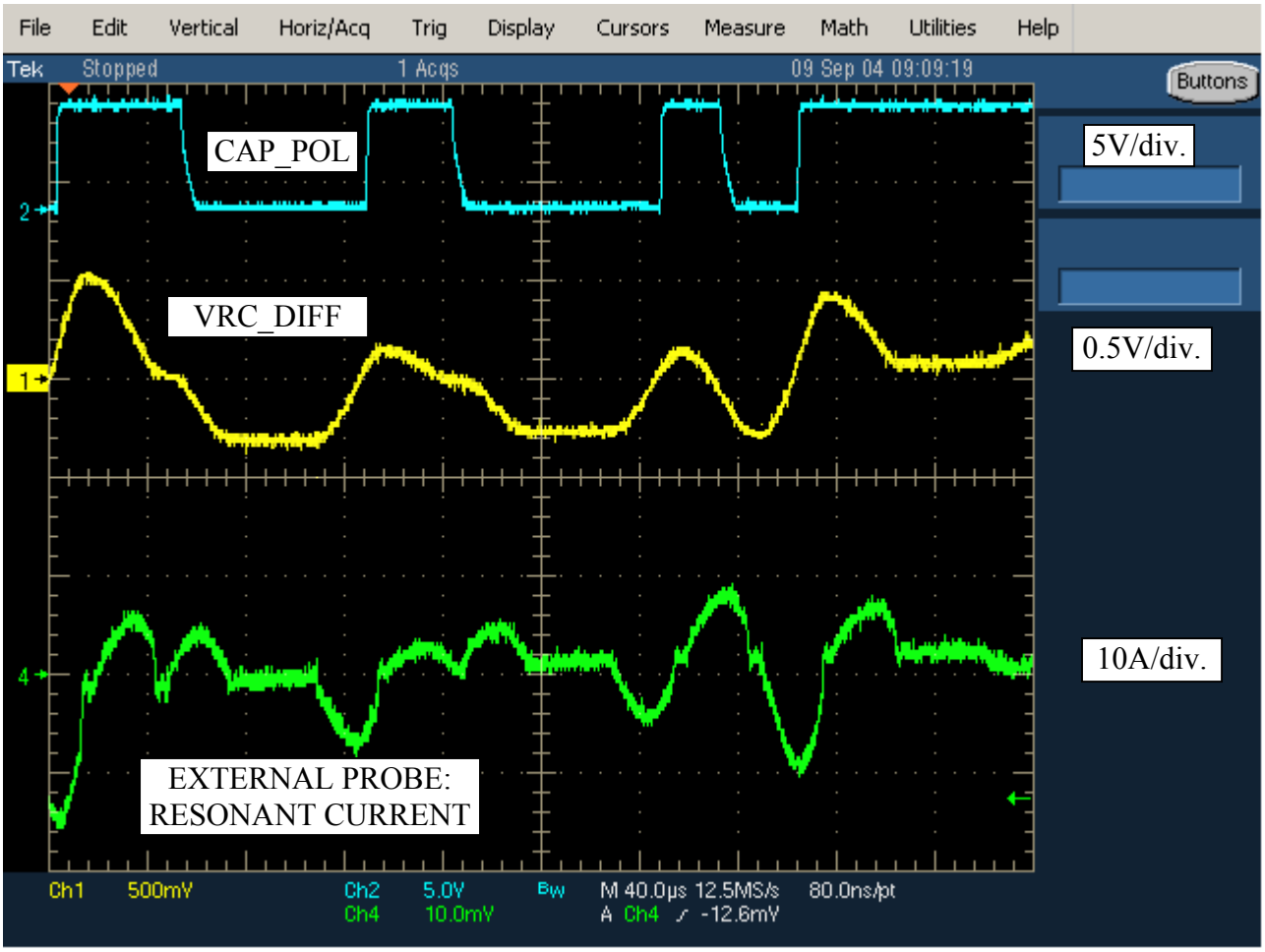
Raw Data from ETM Converter Test.

Conditions: Vin = Vout = 75Vrms (106V peak), fin = fout = 60Hz
Cycle Pulse Time = 31.5us, Resonant Pulse Time = 27.5us

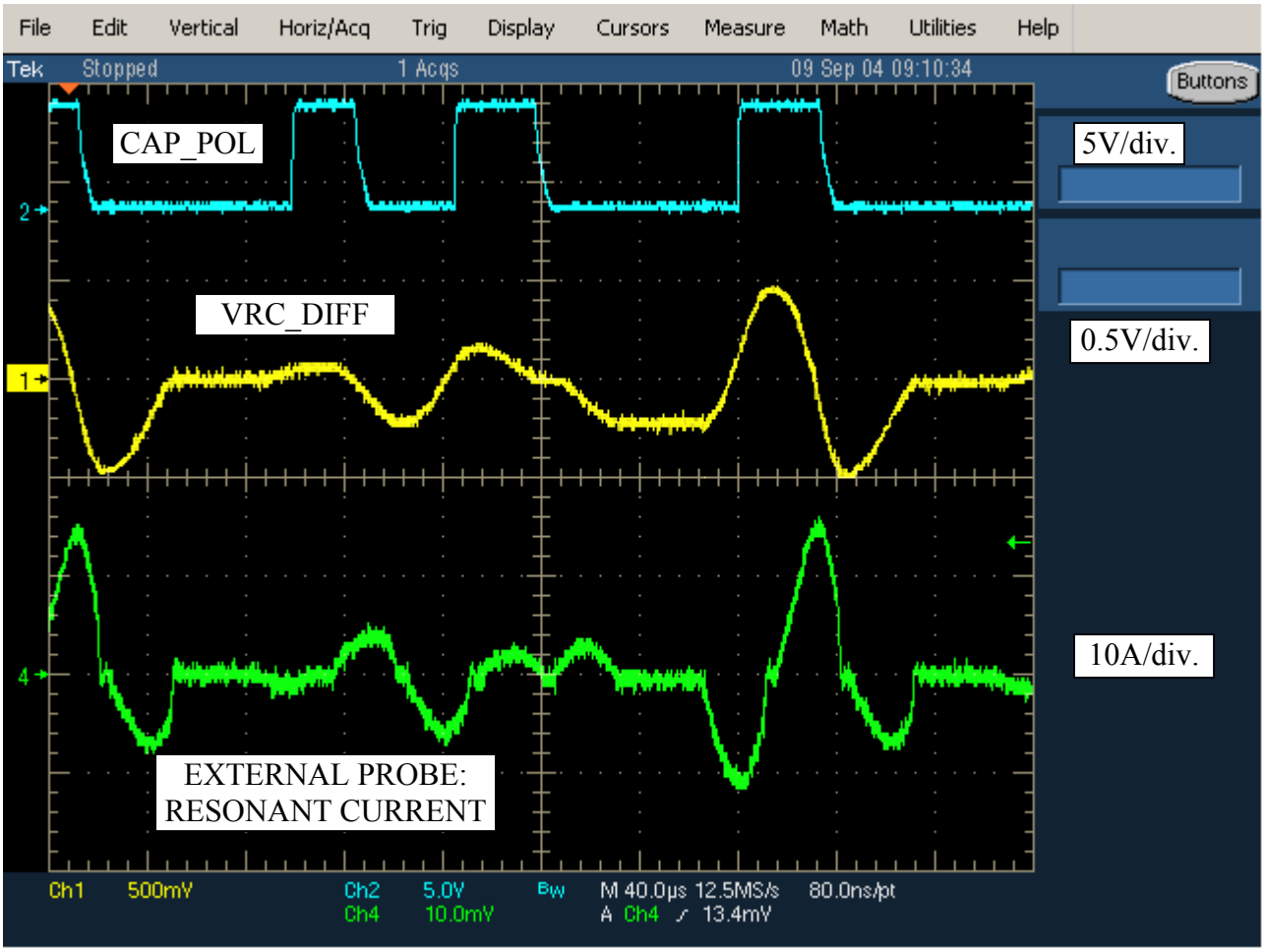
Waveform 1: IRZC, IRMAG_SIGN and External Probe Resonant Current Signals.



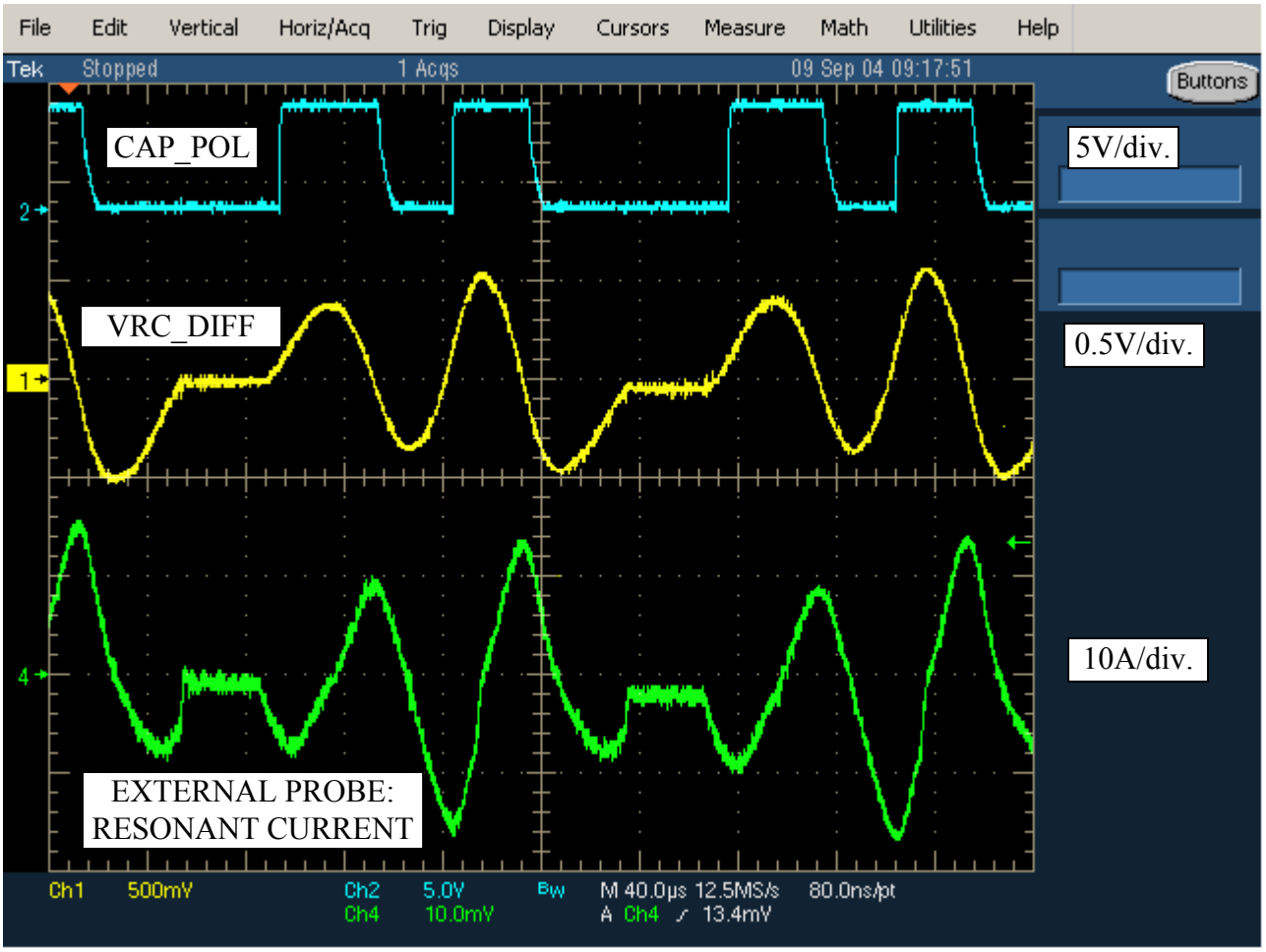
Waveform 2: CAP_POL, VRC_DIFF and External Probe Resonant Current Signals.



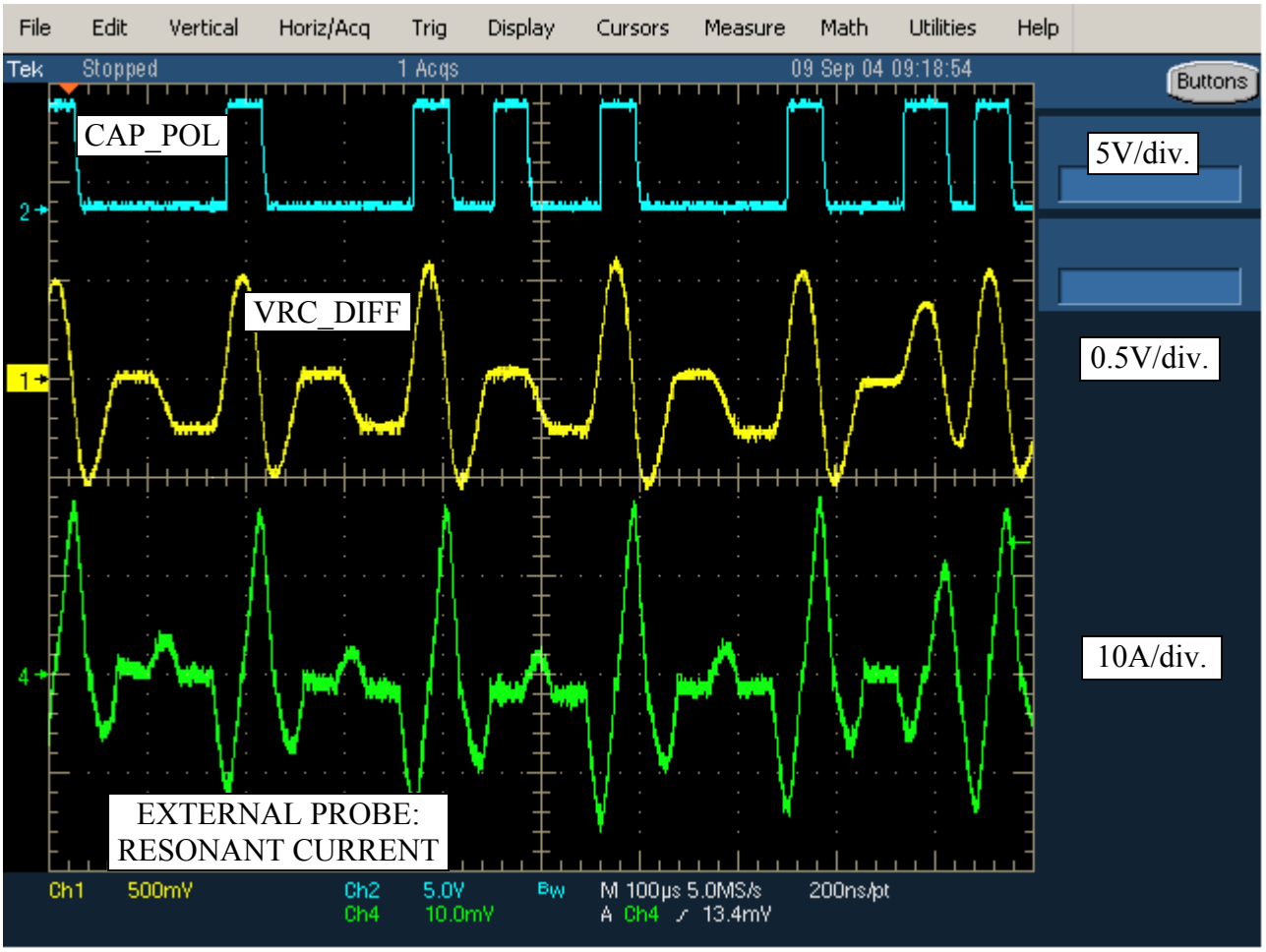
Waveform 3: CAP_POL, VRC_DIFF and External Probe Resonant Current Signals.



Waveform 4: CAP_POL, VRC_DIFF and External Probe Resonant Current Signals.

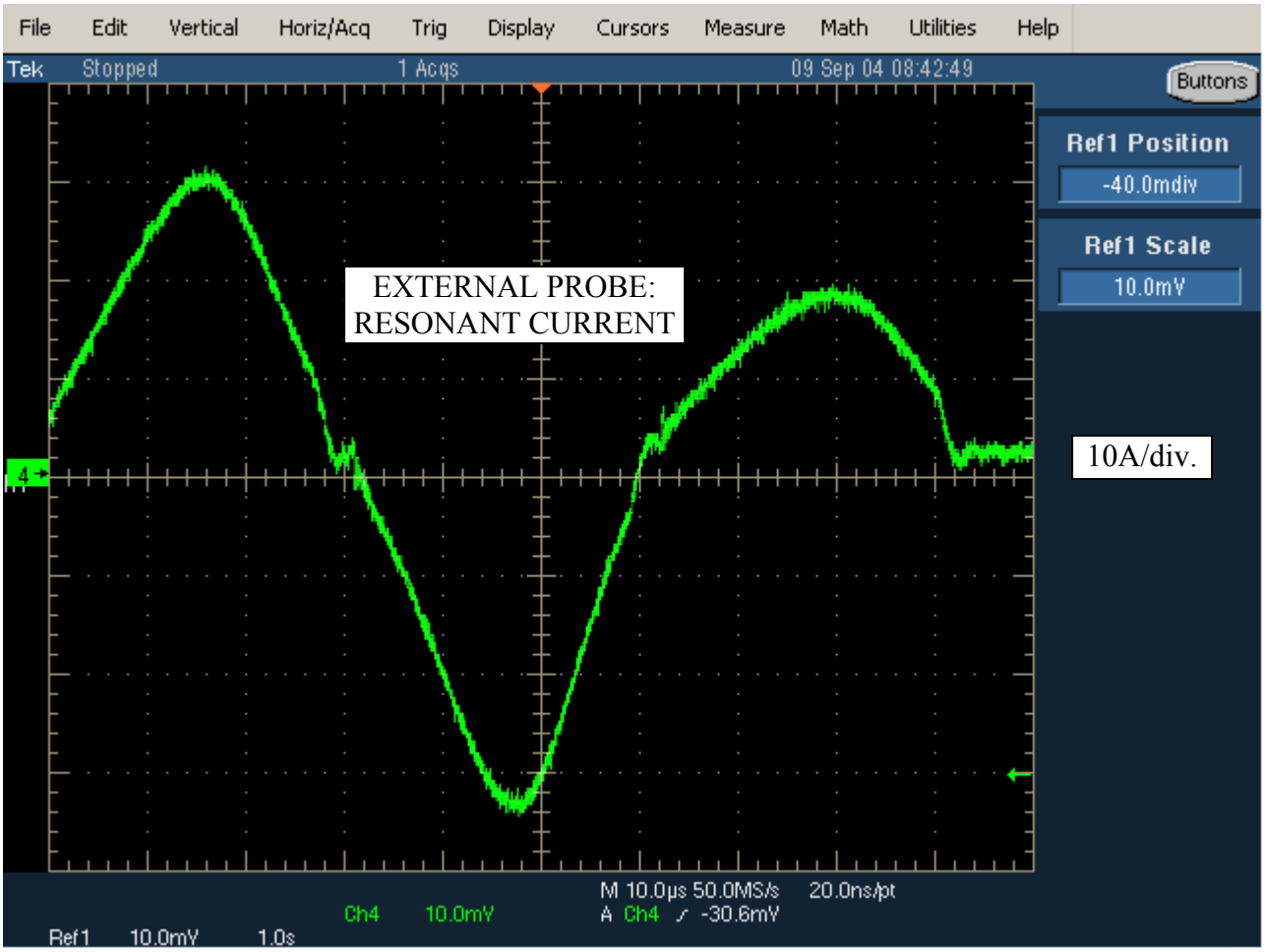


Wavetrain 5: CAP_POL, VRC_DIFF and External Probe Resonant Current Signals.

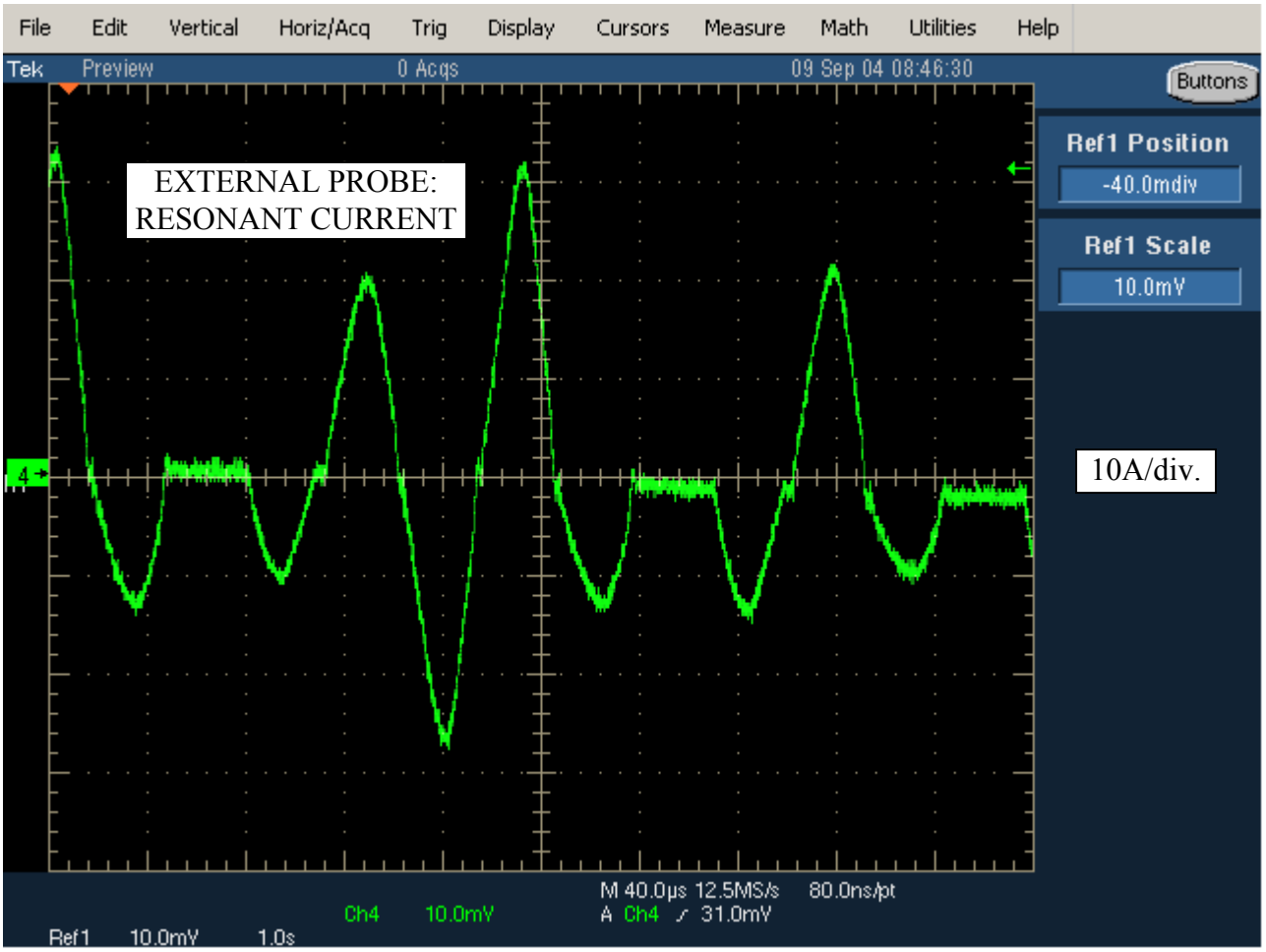


Wavetrain 6: CAP_POL, VRC_DIFF and External Probe Resonant Current Signals.

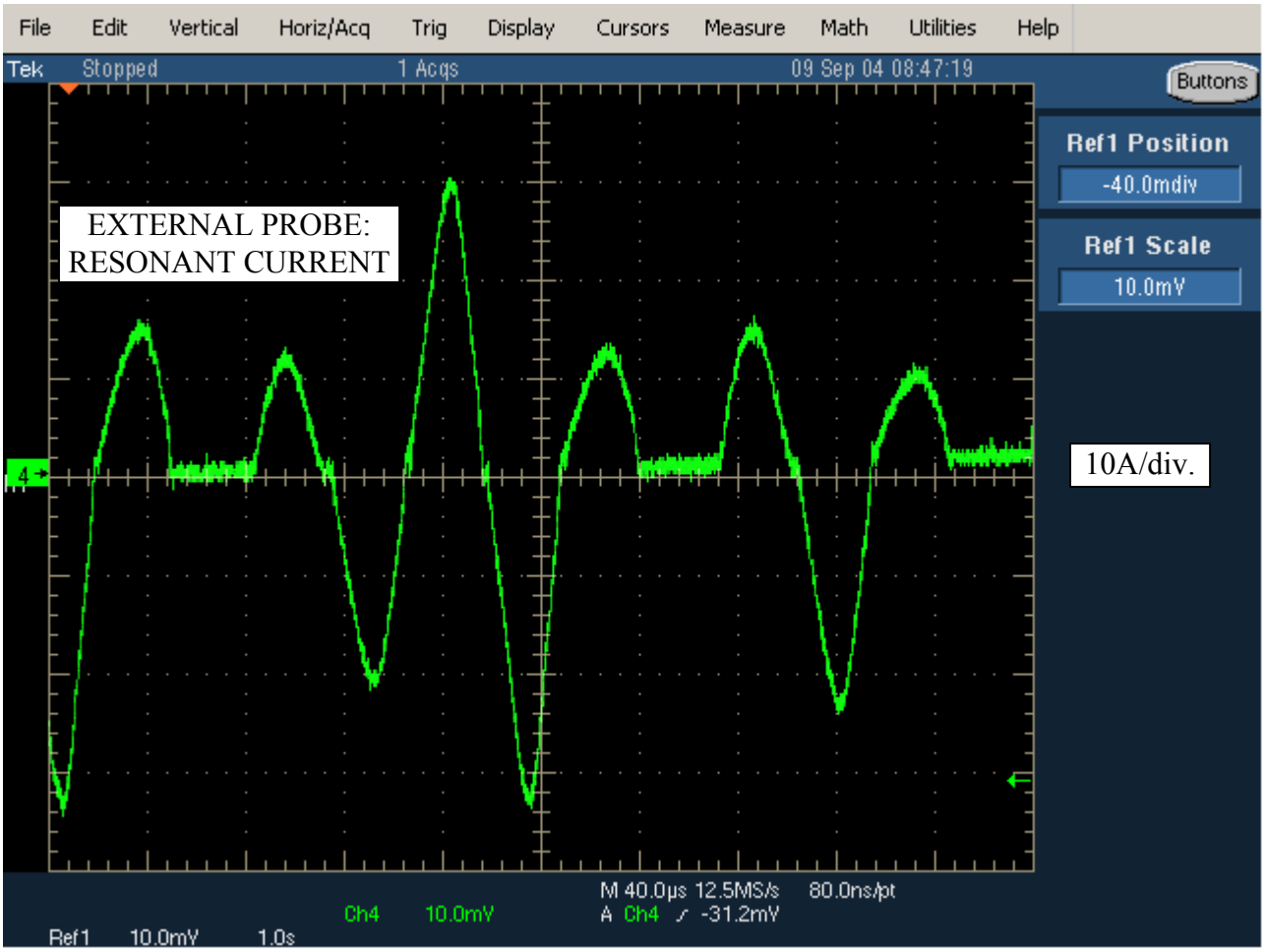
Waveform 7: External Probe Resonant Current Signals.



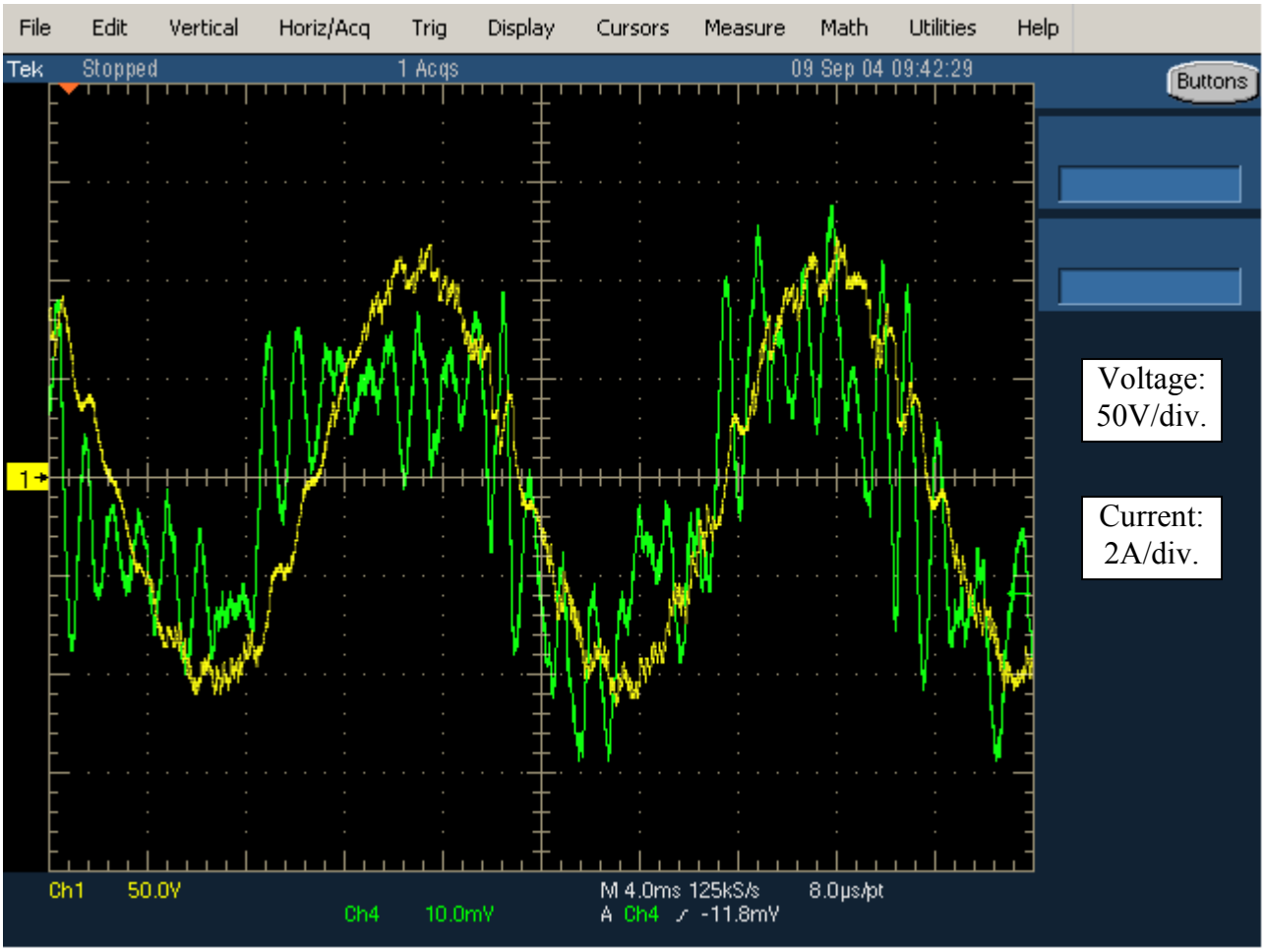
Waveform 8: External Probe Resonant Current Signals.



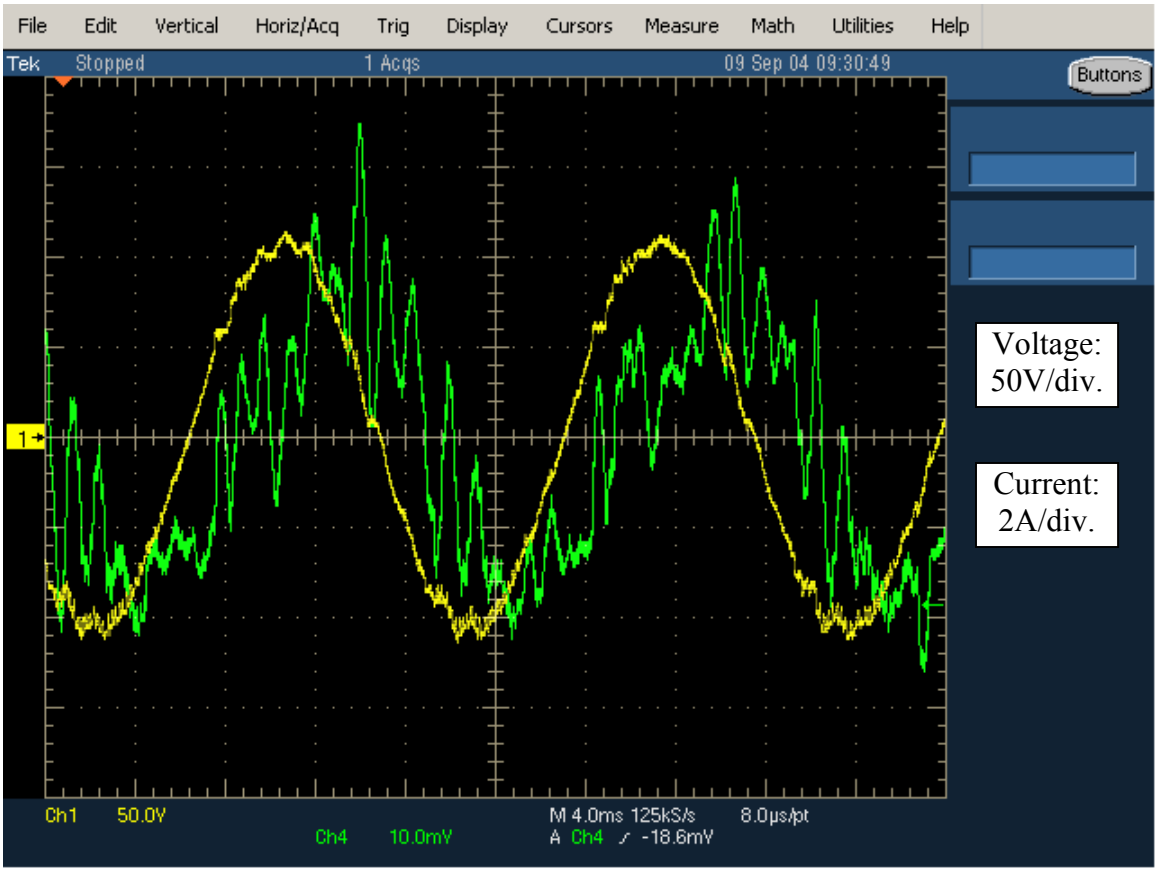
Waveform 9: External Probe Resonant Current Signals.



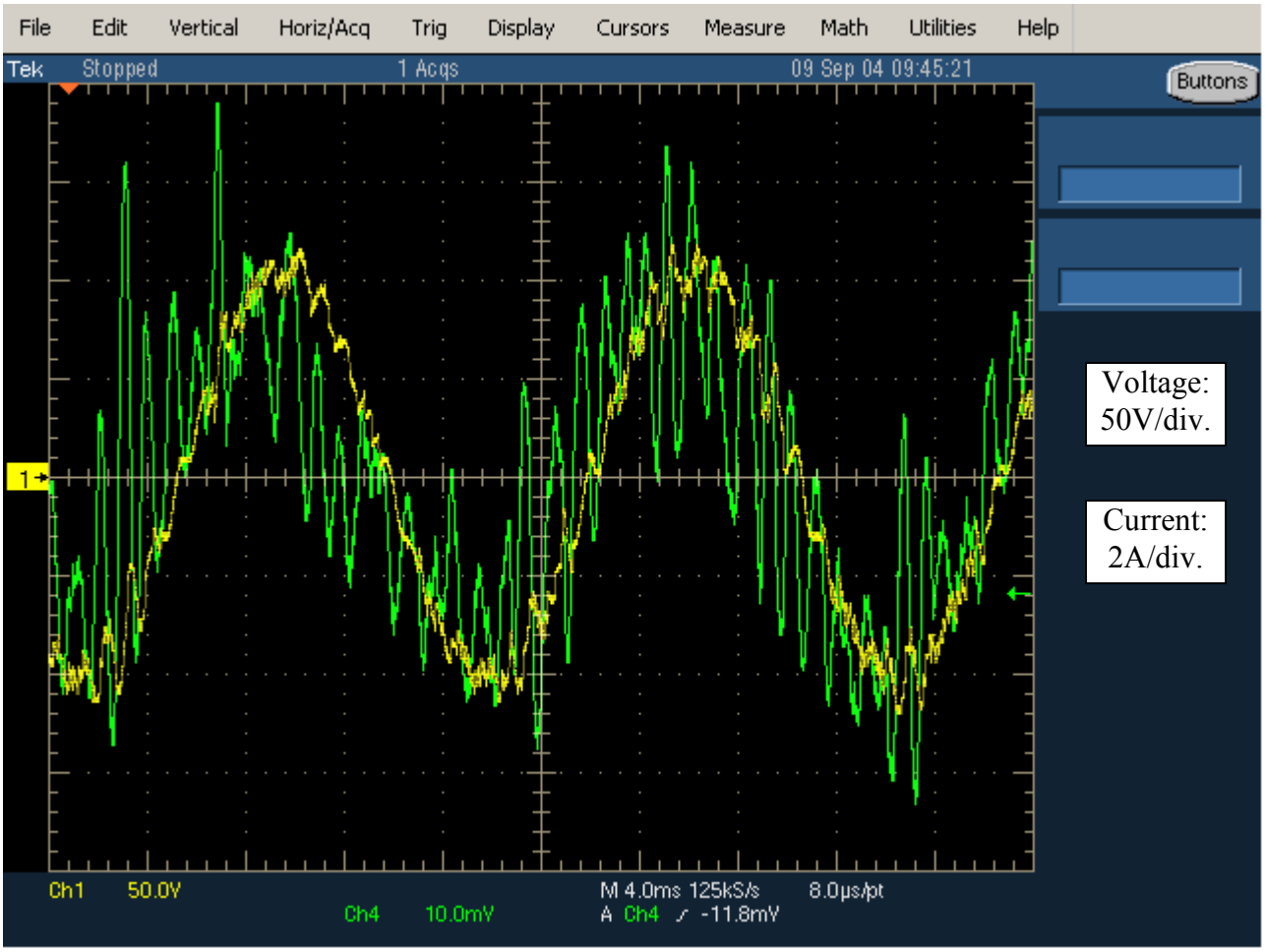
Waveform 10: Phase A Input Voltage (Yellow) and Current (Green).



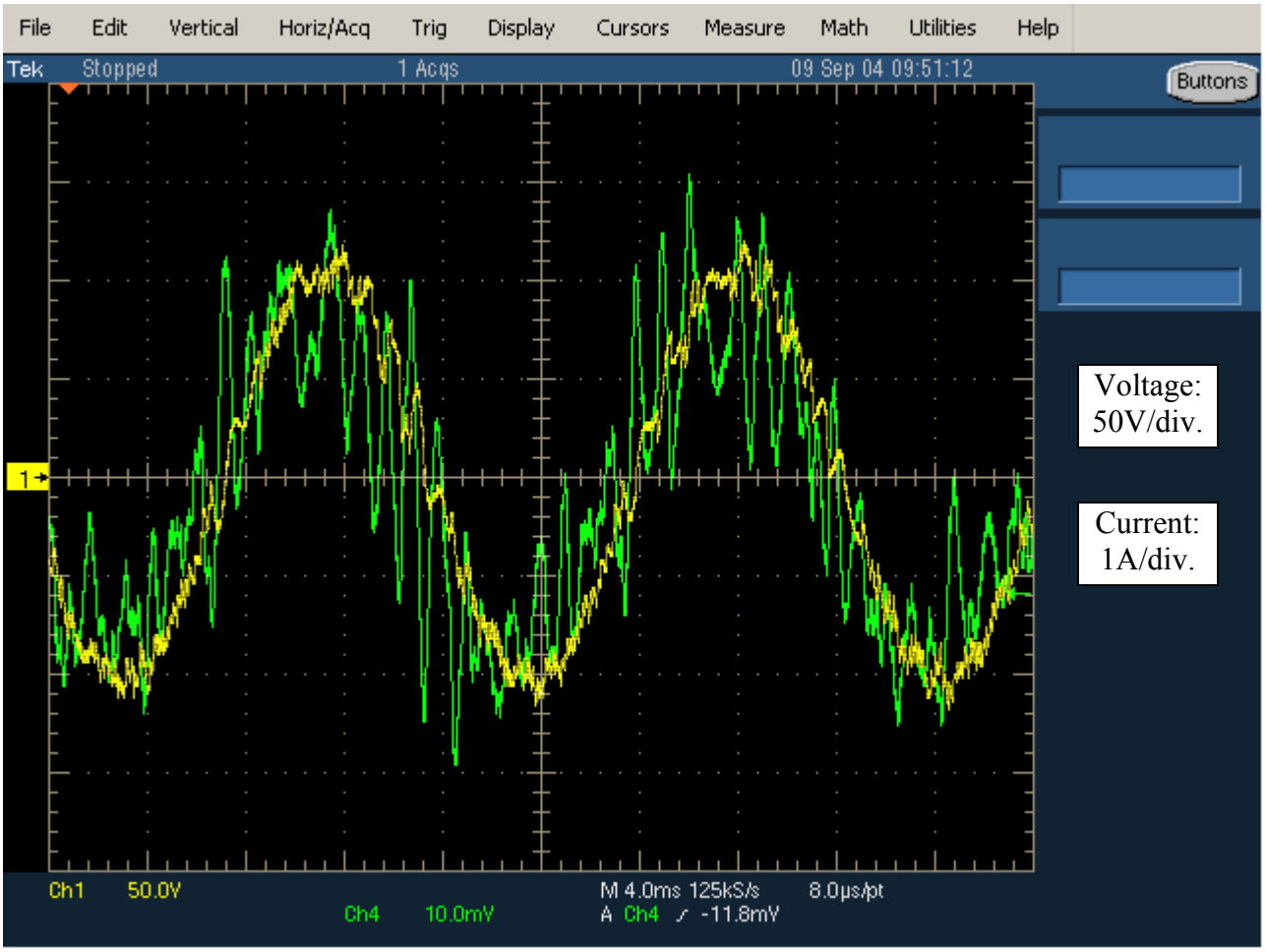
Waveform 11: Phase B Input Voltage (Yellow) and Current (Green).



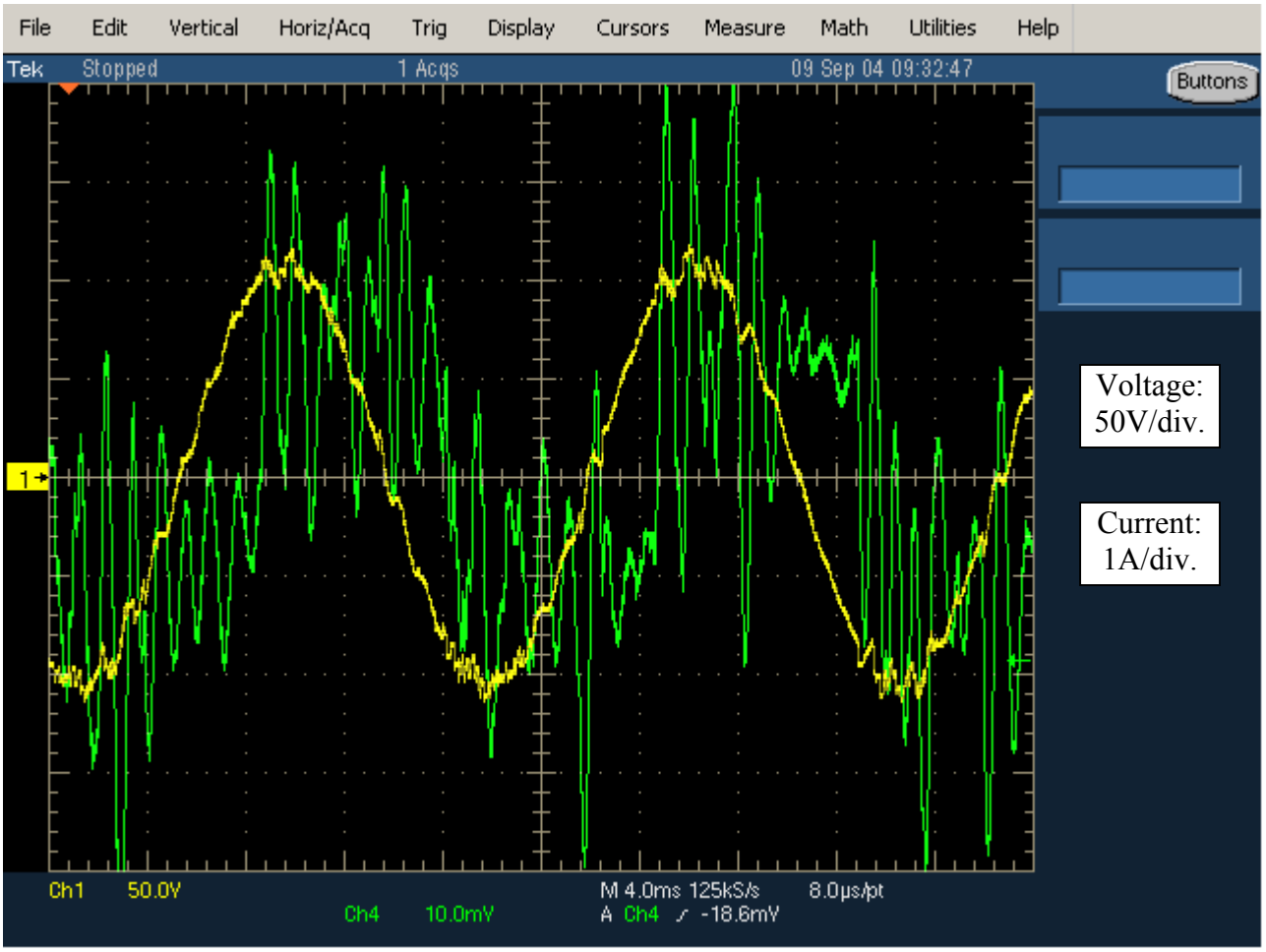
Waveform 12: Phase C Input Voltage (Yellow) and Current (Green).



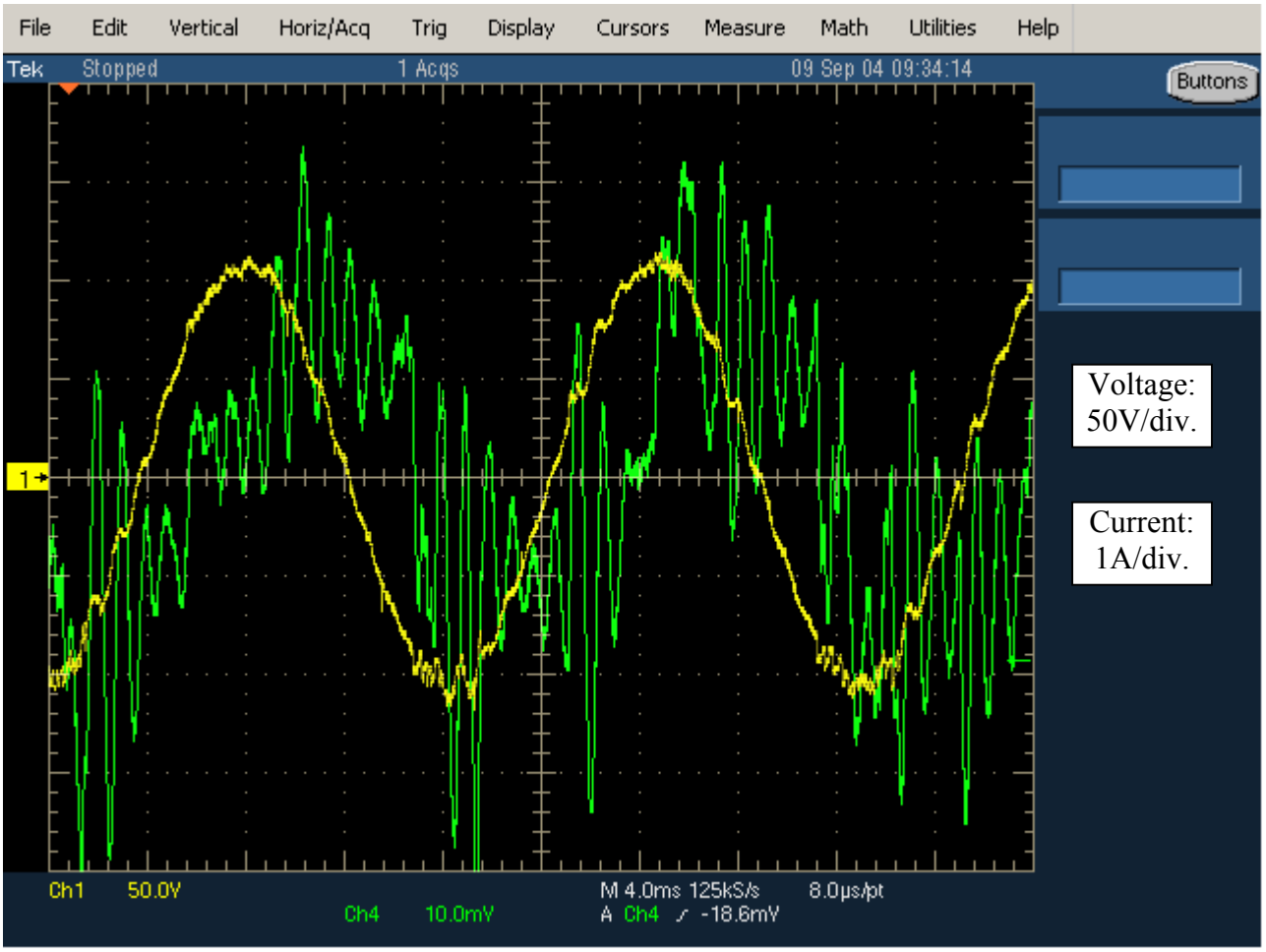
Waveform 13: Phase A Output Voltage (Yellow) and Current (Green).



Waveform 14: Phase B Output Voltage (Yellow) and Current (Green).



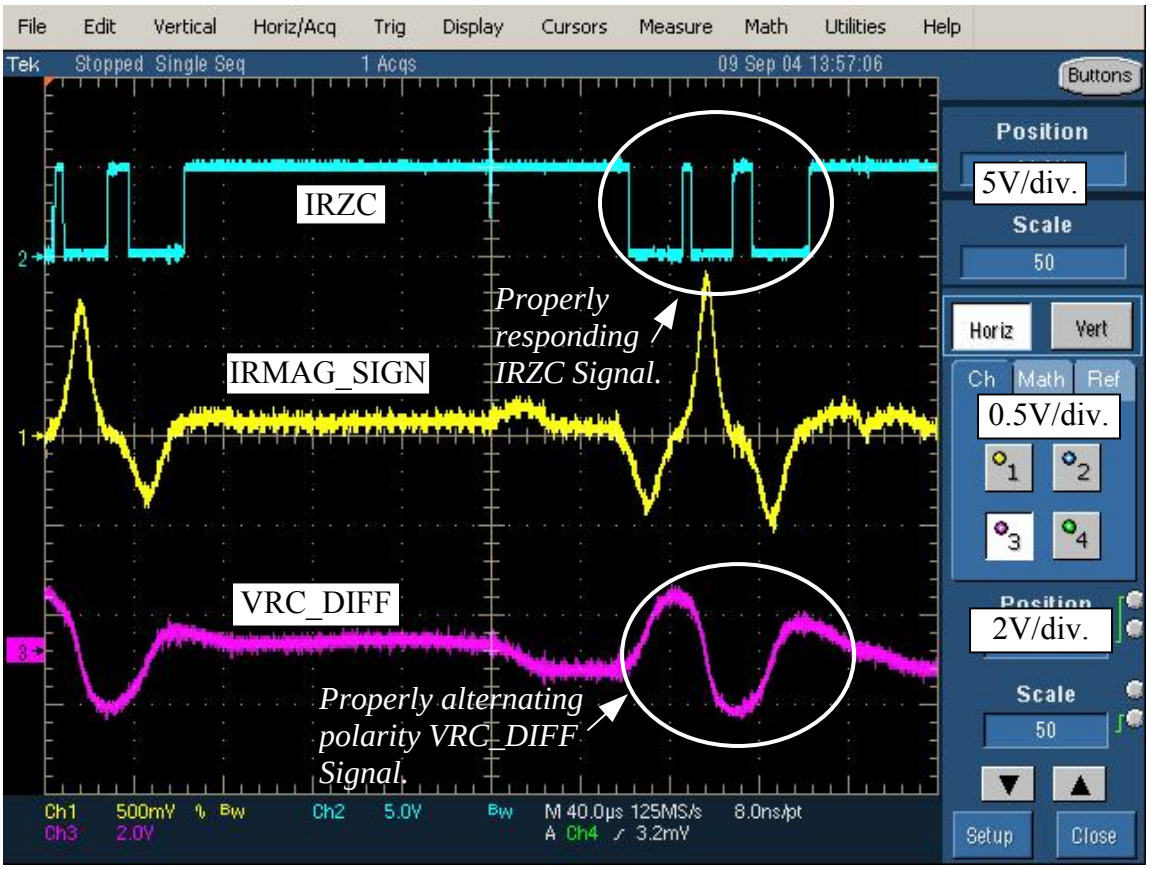
Waveform 15: Phase C Output Voltage (Yellow) and Current (Green).



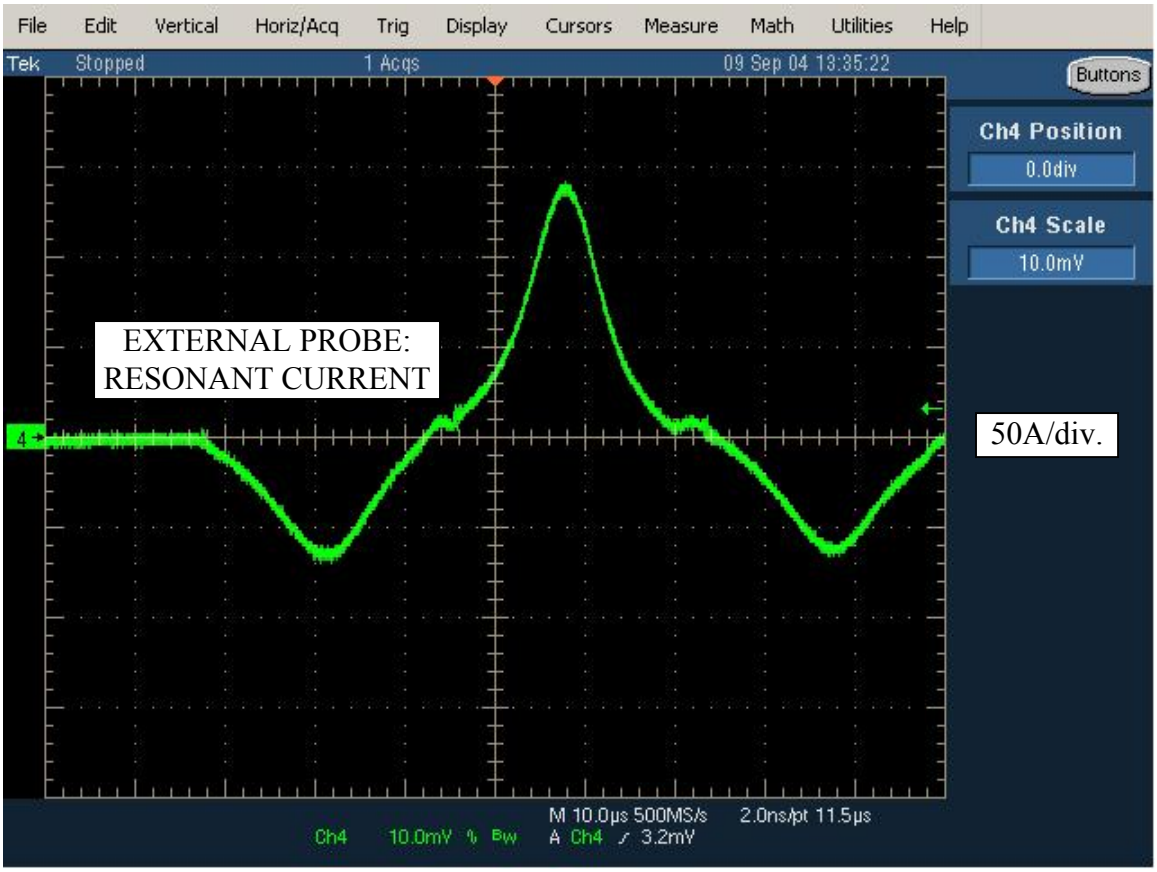
Raw Data from ETM Converter Test.

Conditions: Vin = Vout = 150Vrms (212V peak), fin = fout = 60Hz
Cycle Pulse Time = 28.0us, Resonant Pulse Time = 24.0us

Waveform 1: IRZC, IRMAG_SIGN and VRC_DIFF Signals.



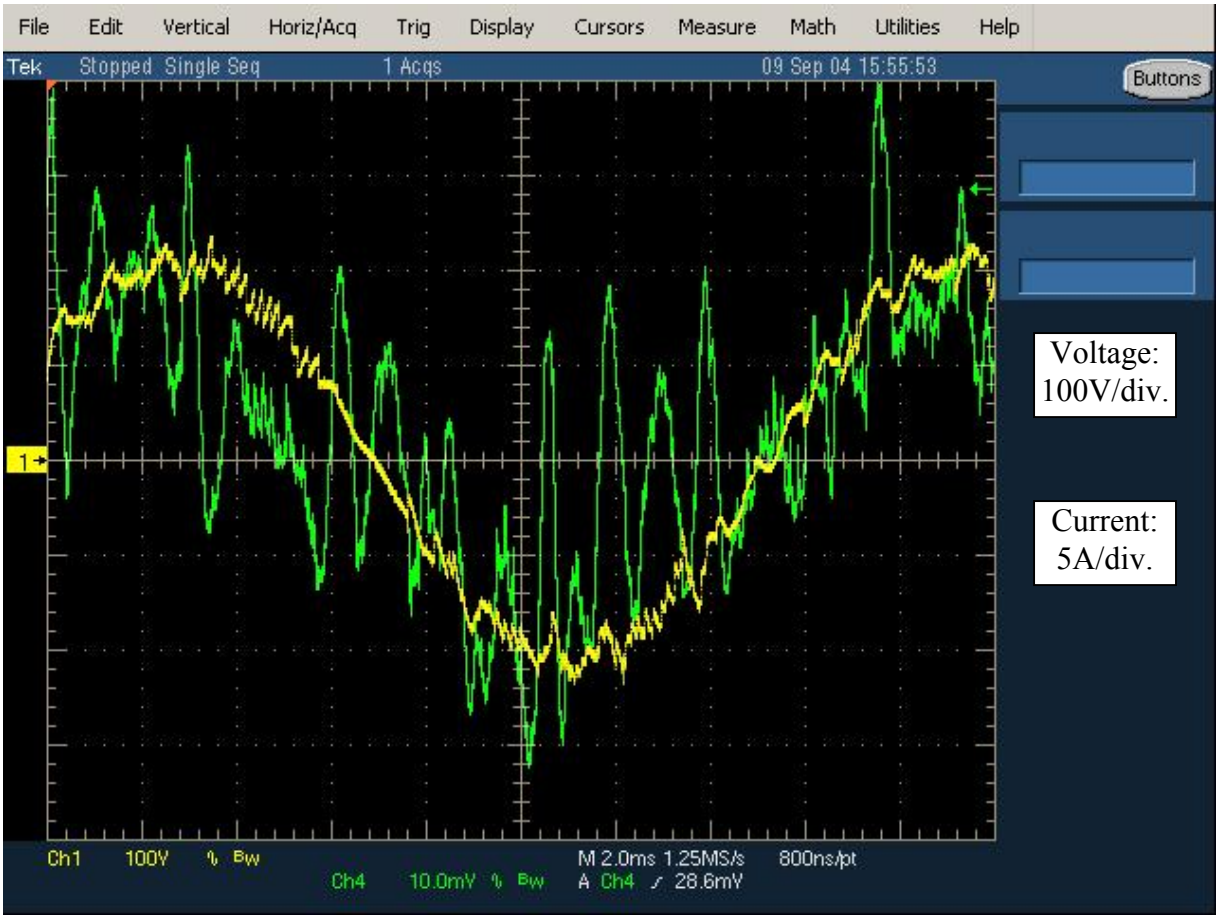
Waveform 2: External Probe Resonant Current Signal.



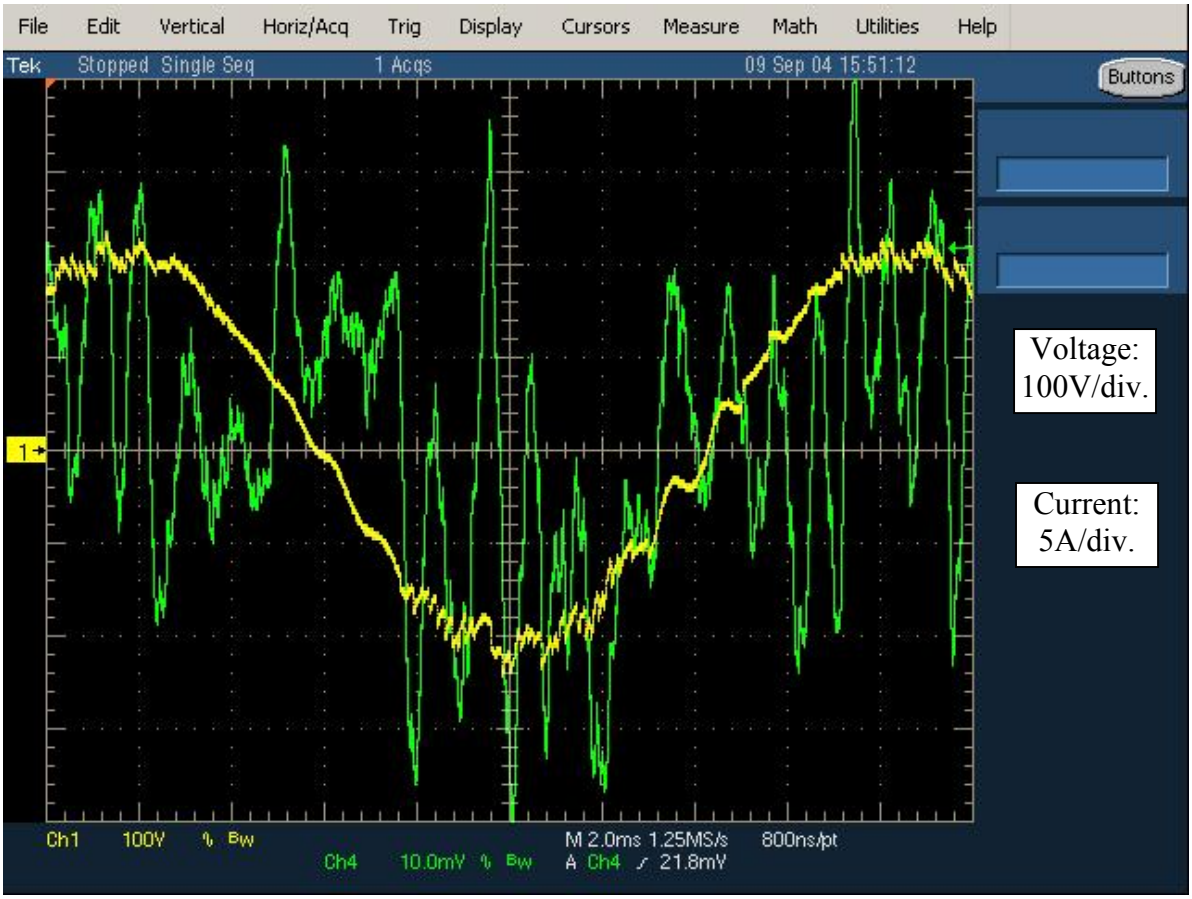
Waveform 3: Phase A Input Voltage (Yellow) and Current (Green).

Waveform 4: Phase B Input Voltage (Yellow) and Current (Green).

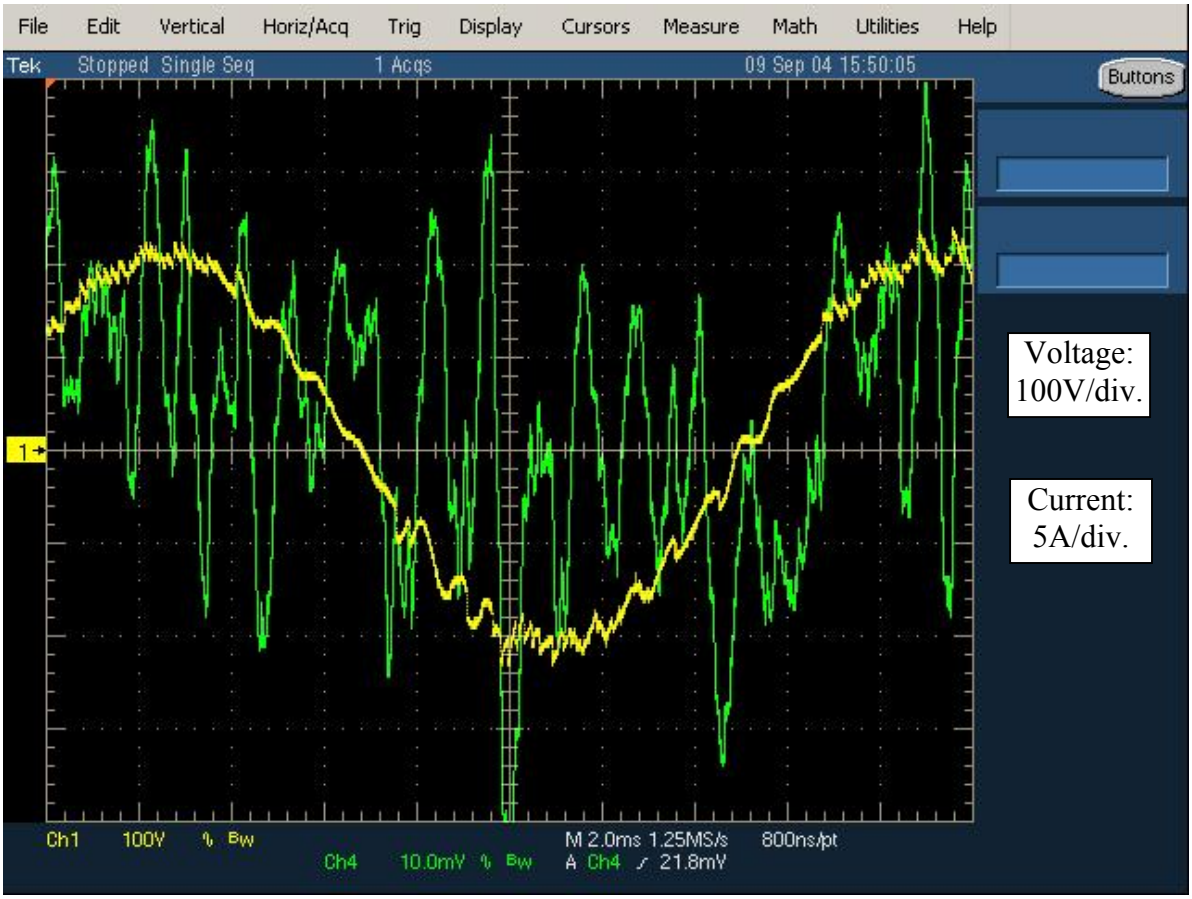
Waveform 5: Phase C Input Voltage (Yellow) and Current (Green).



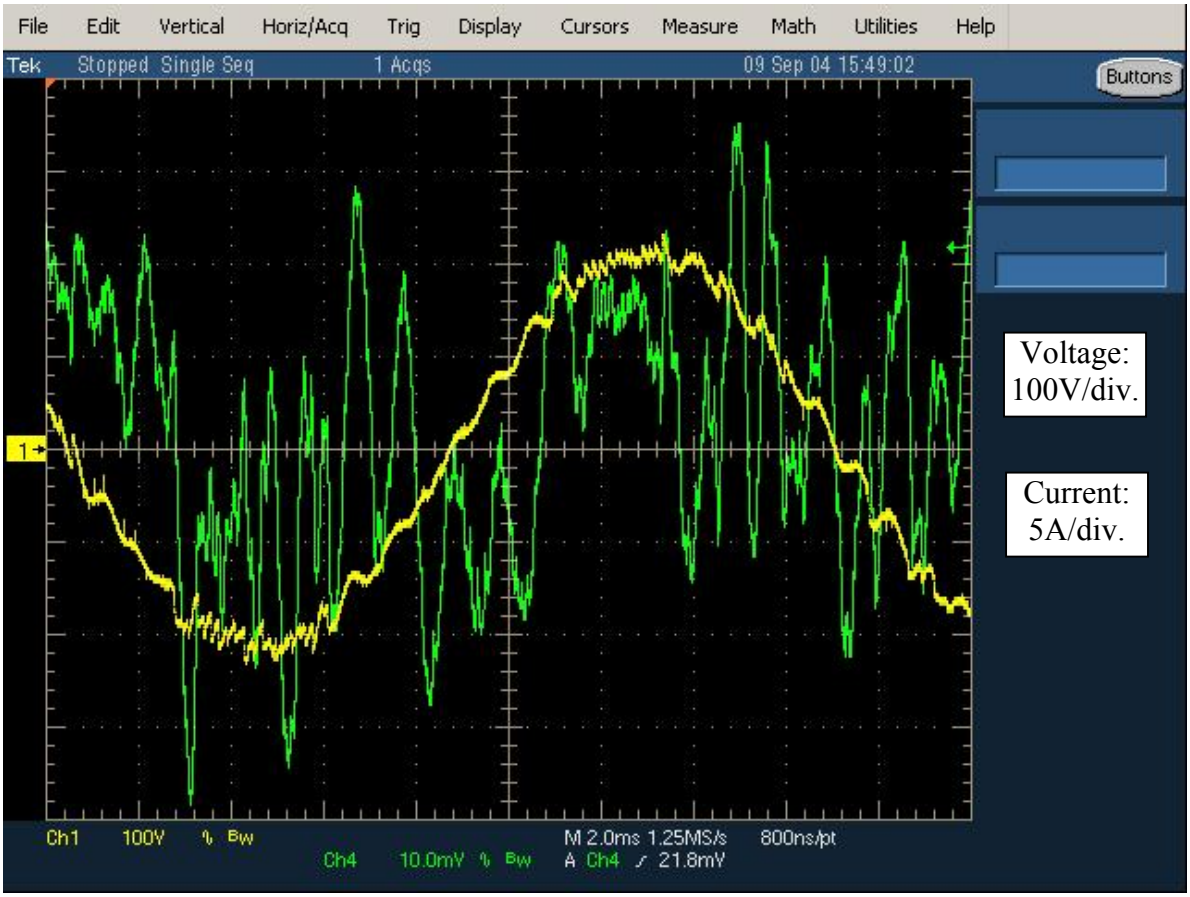
Waveform 6: Phase A Output Voltage (Yellow) and Current (Green).



Waveform 7: Phase B Output Voltage (Yellow) and Current (Green).



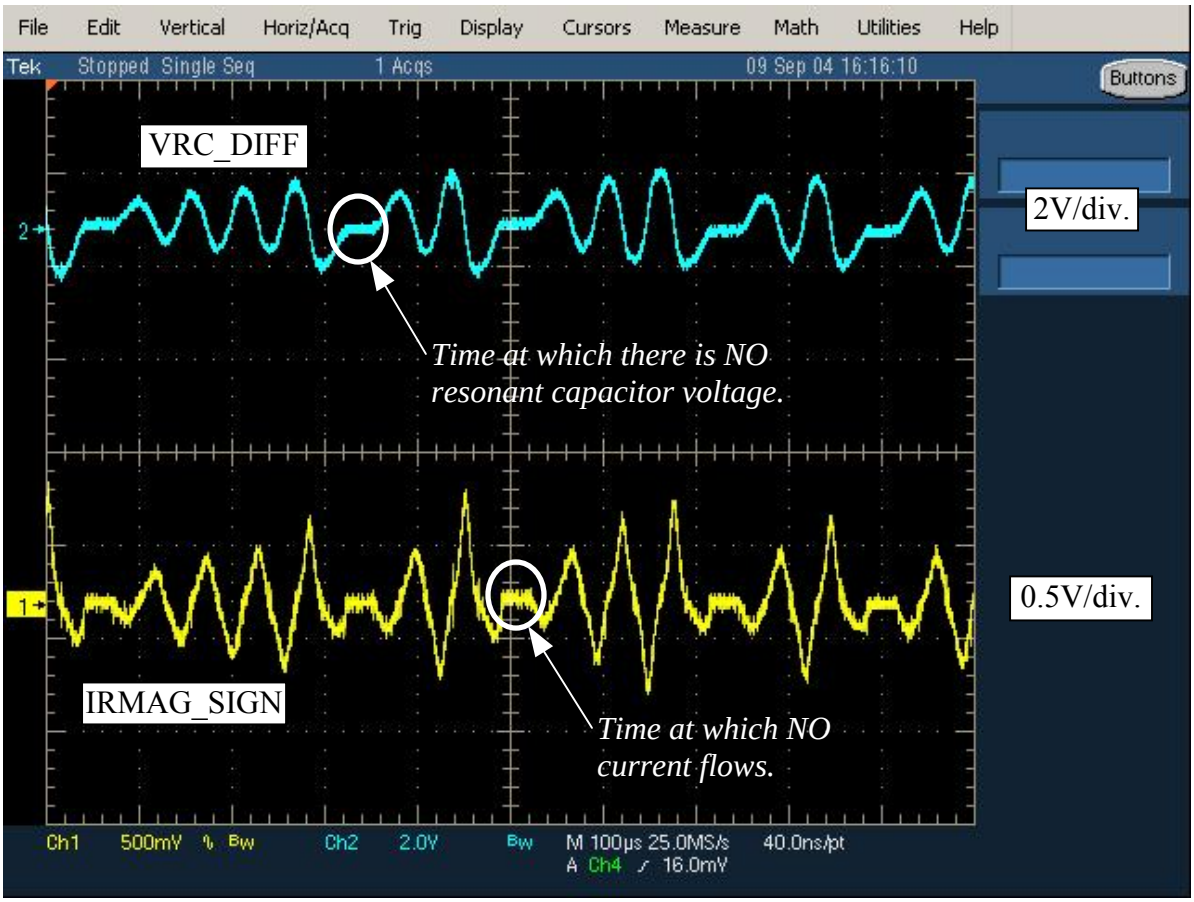
Waveform 8: Phase C Output Voltage (Yellow) and Current (Green).



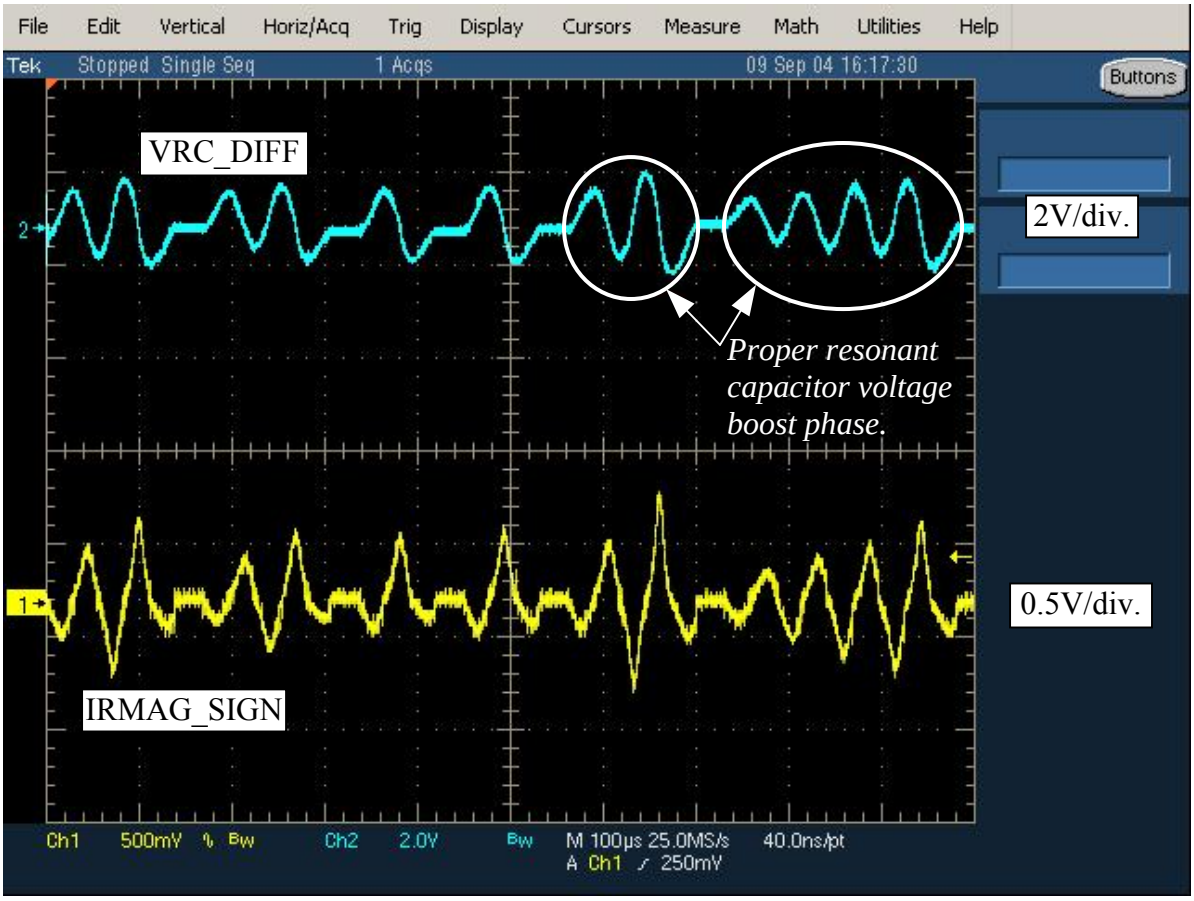
Raw Data from ETM Converter Test.

Conditions: Vin = 100Vrms (141V peak), Vout = 150Vrms (212V peak), fin = fout = 60Hz
Cycle Pulse Time = 28.0us, Resonant Pulse Time = 24.0us

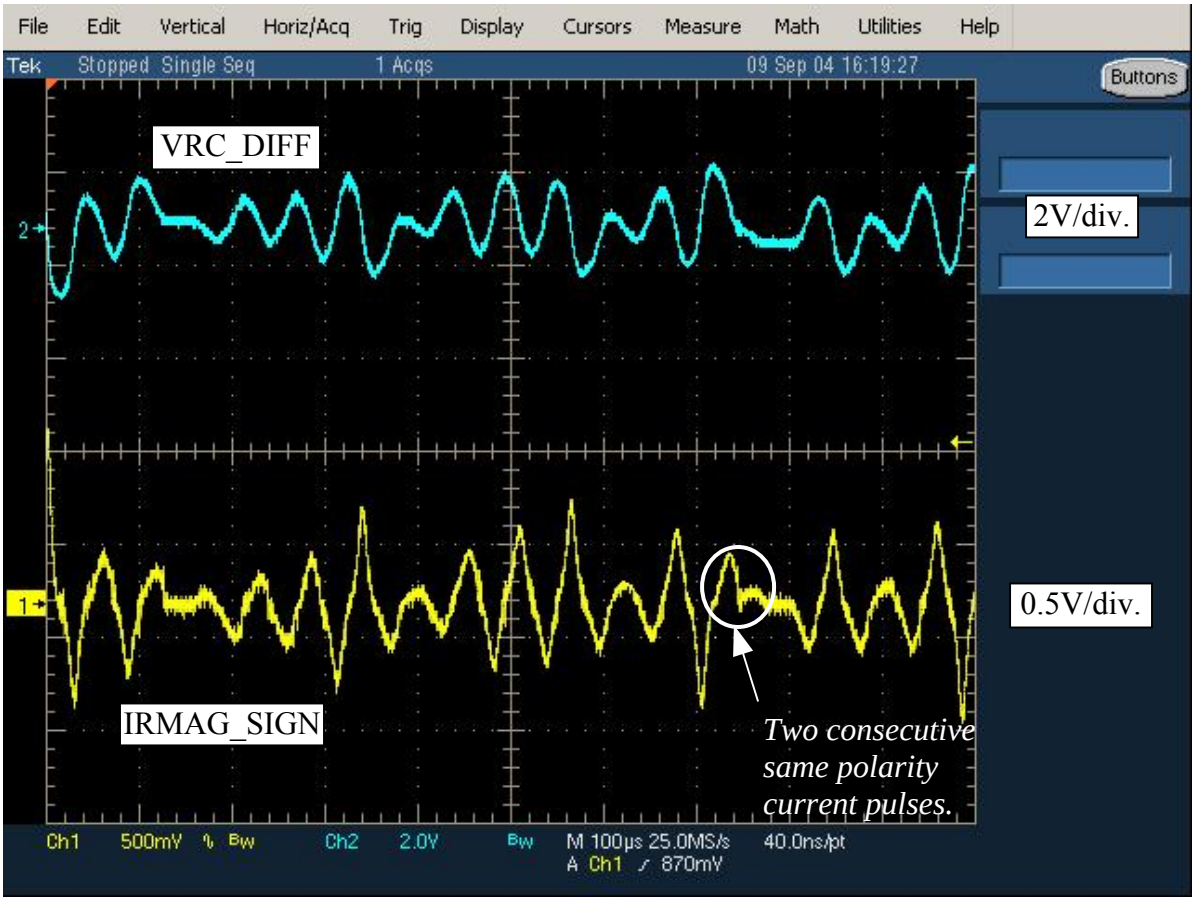
Waveform 1: IRMAG_SIGN and VRC_DIFF Signals.



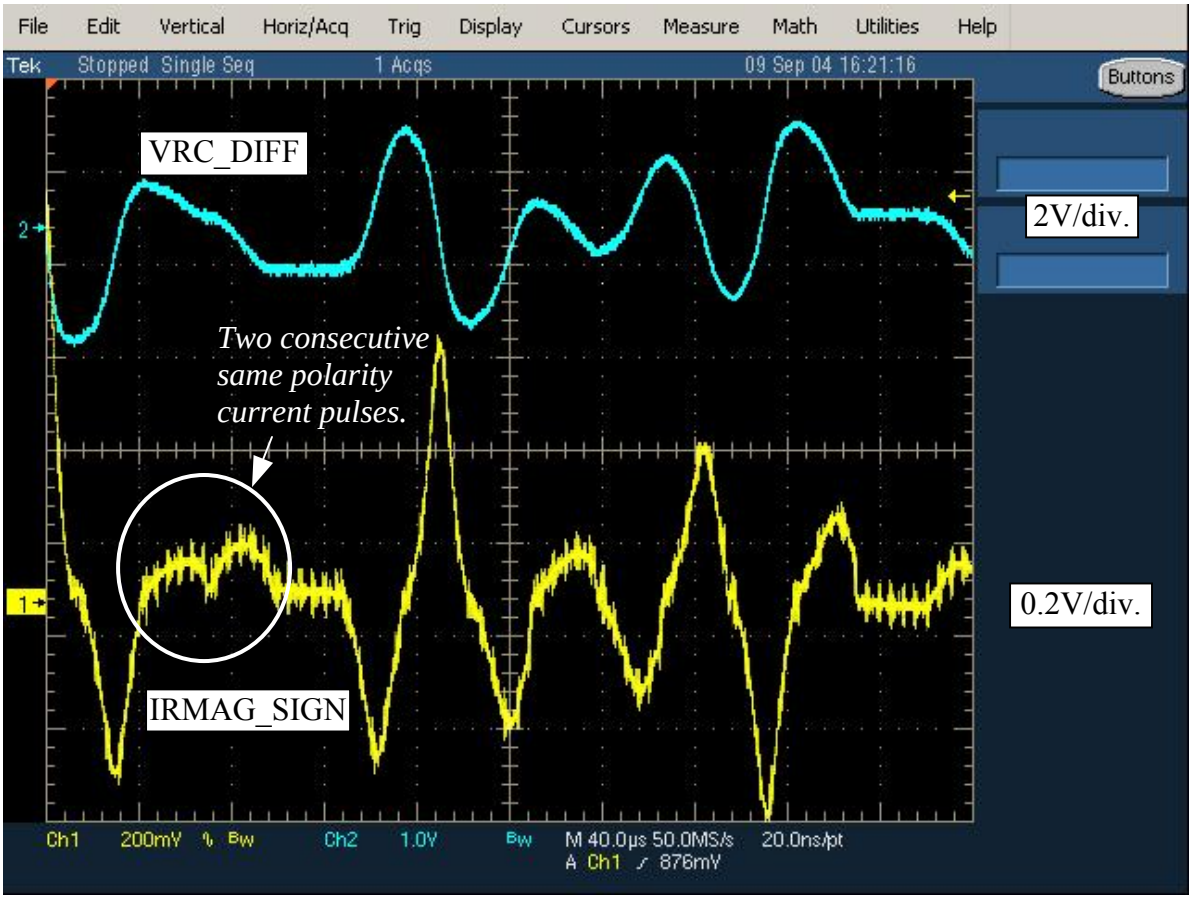
Waveform 2: IRMAG_SIGN and VRC_DIFF Signals.



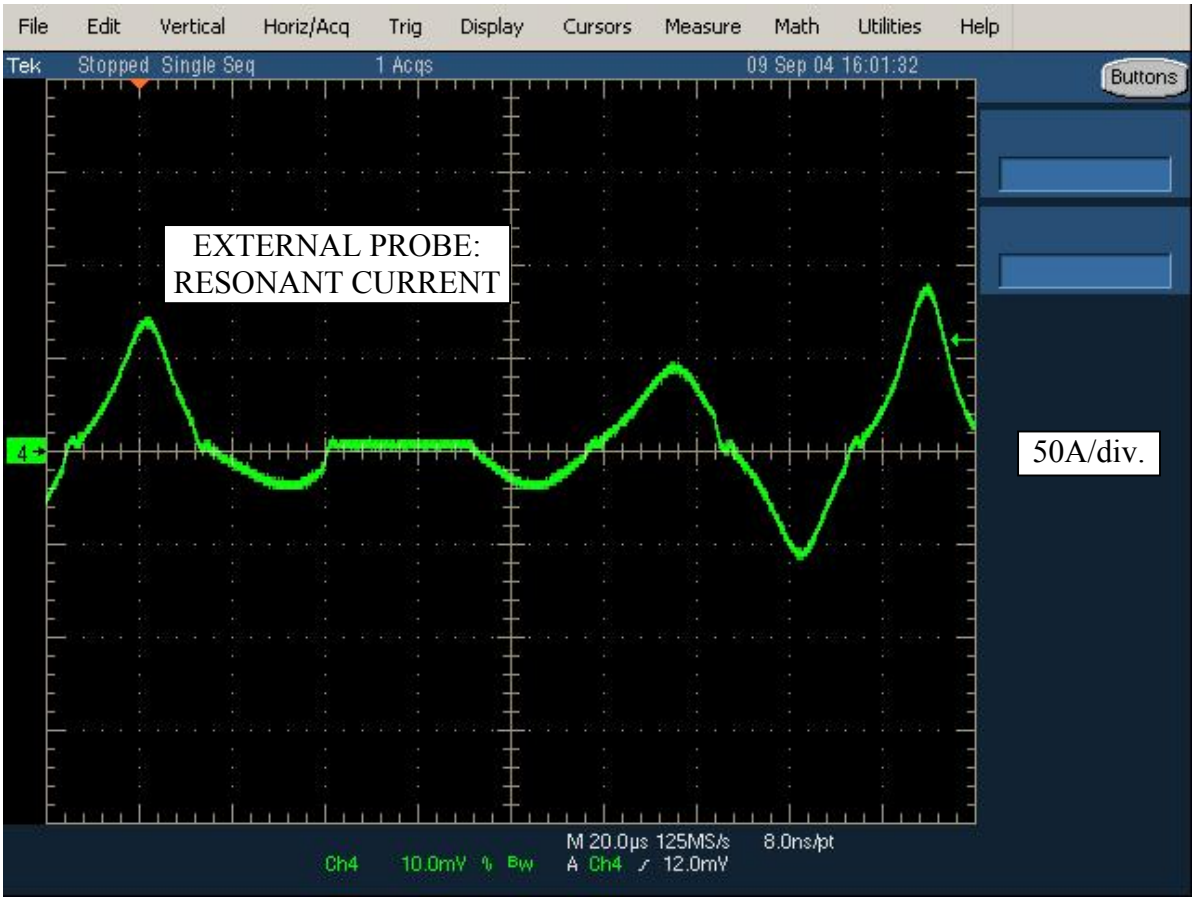
Waveform 3: IRMAG_SIGN and VRC_DIFF Signals.



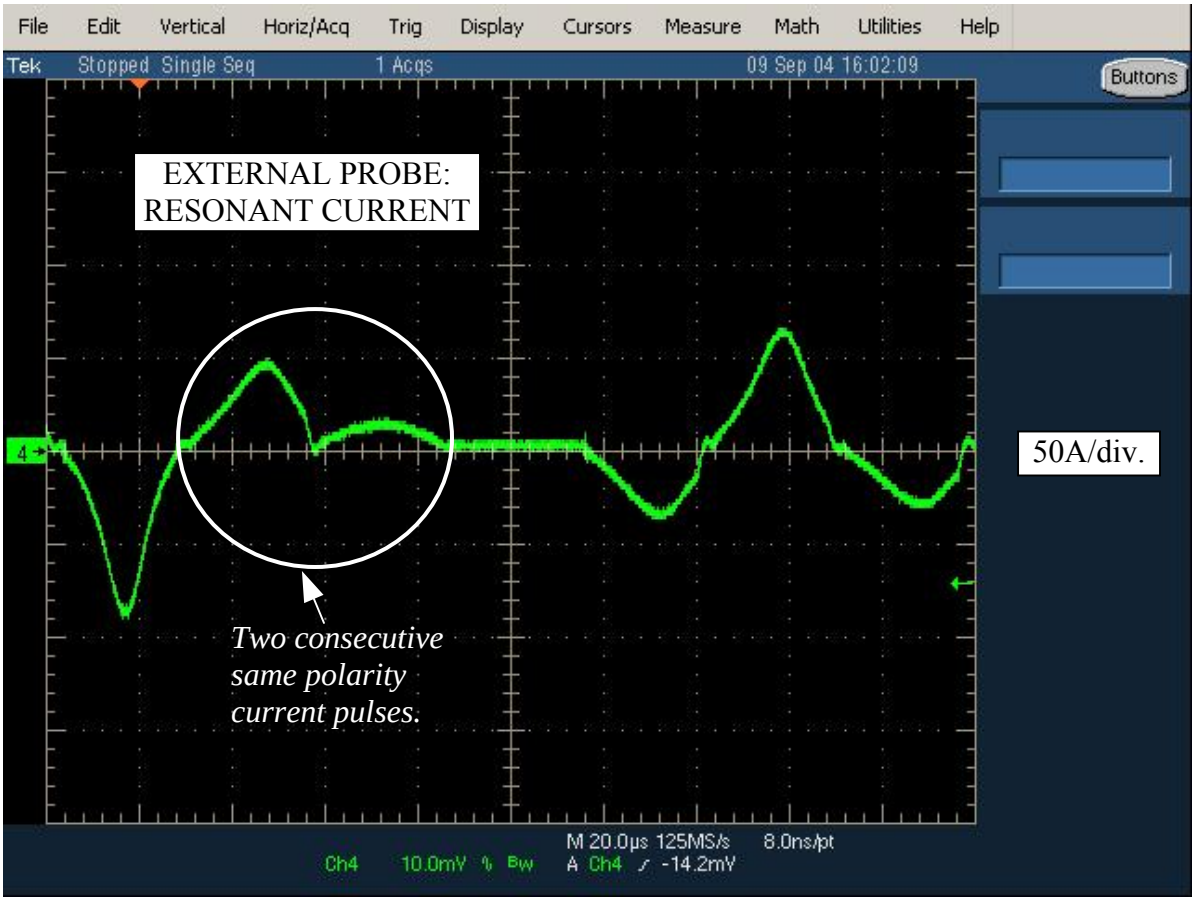
Waveform 4: IRMAG_SIGN and VRC_DIFF Signals.



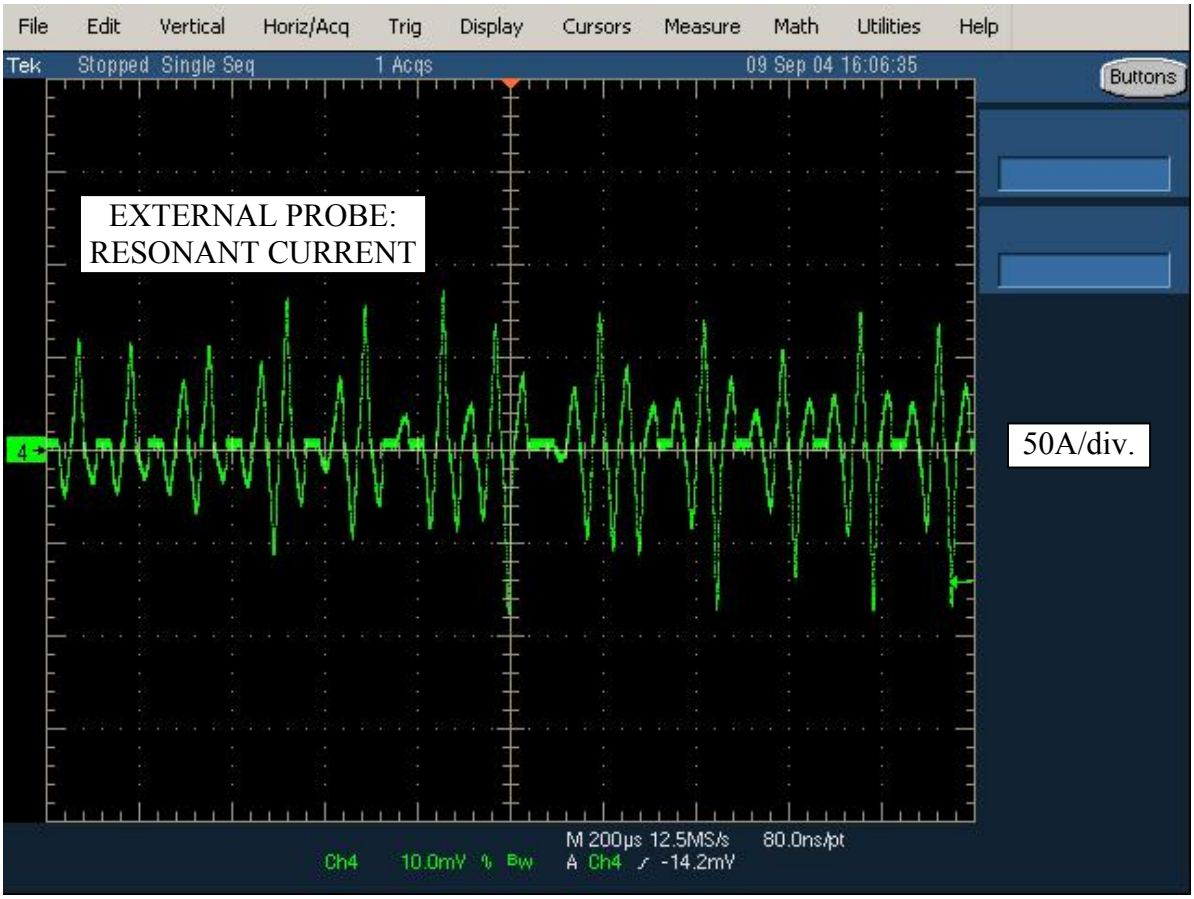
Waveform 5: External Probe Resonant Current Signal.



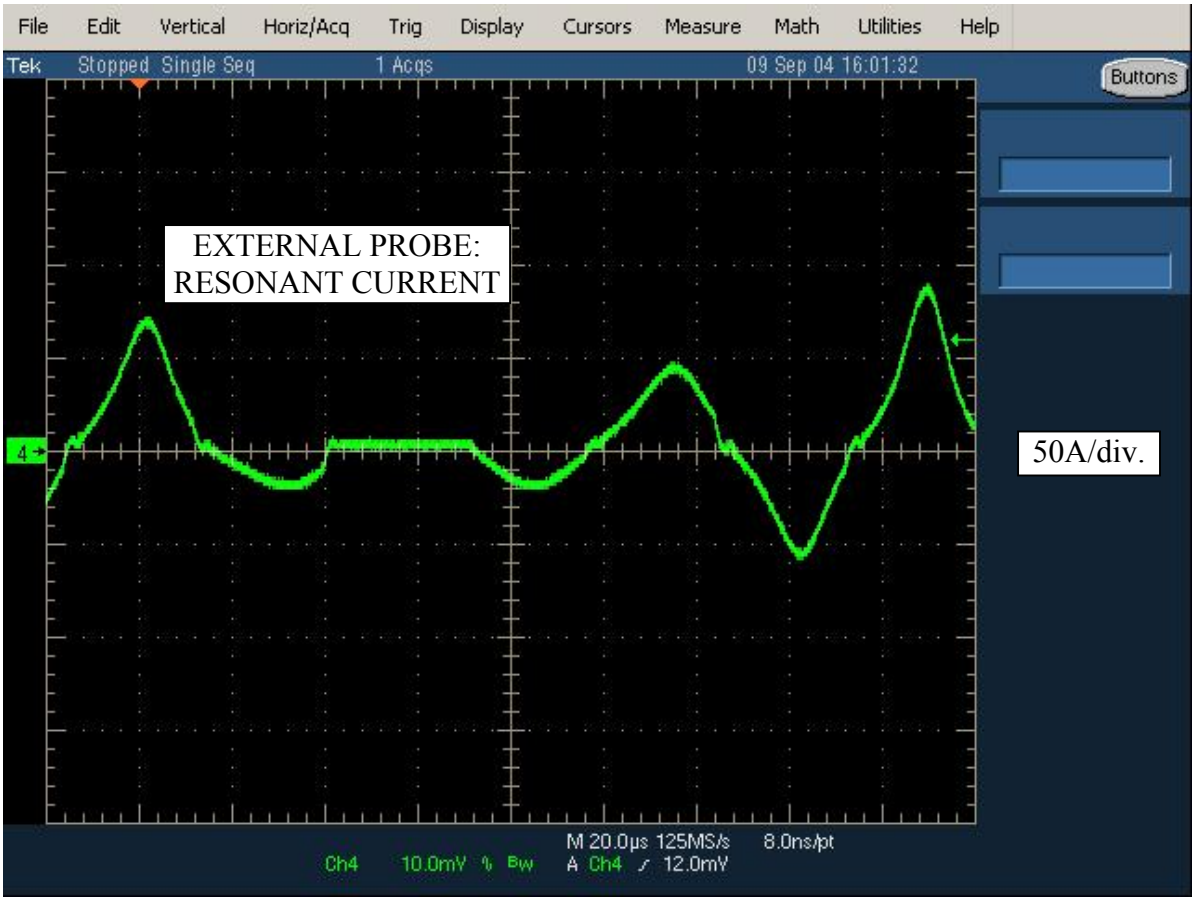
Waveform 6: External Probe Resonant Current Signal.



Waveform 7: External Probe Resonant Current Signal.

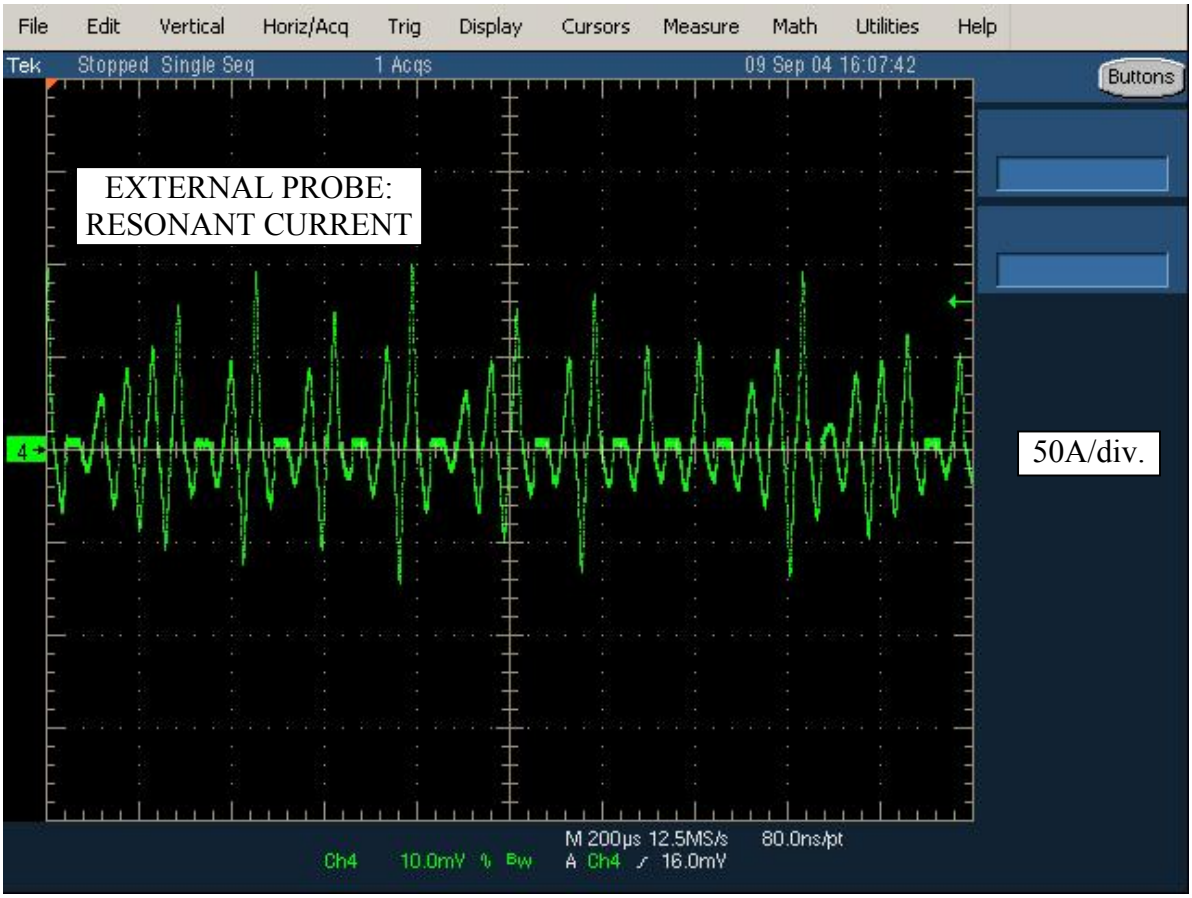


Waveform 8: External Probe Resonant Current Signal.

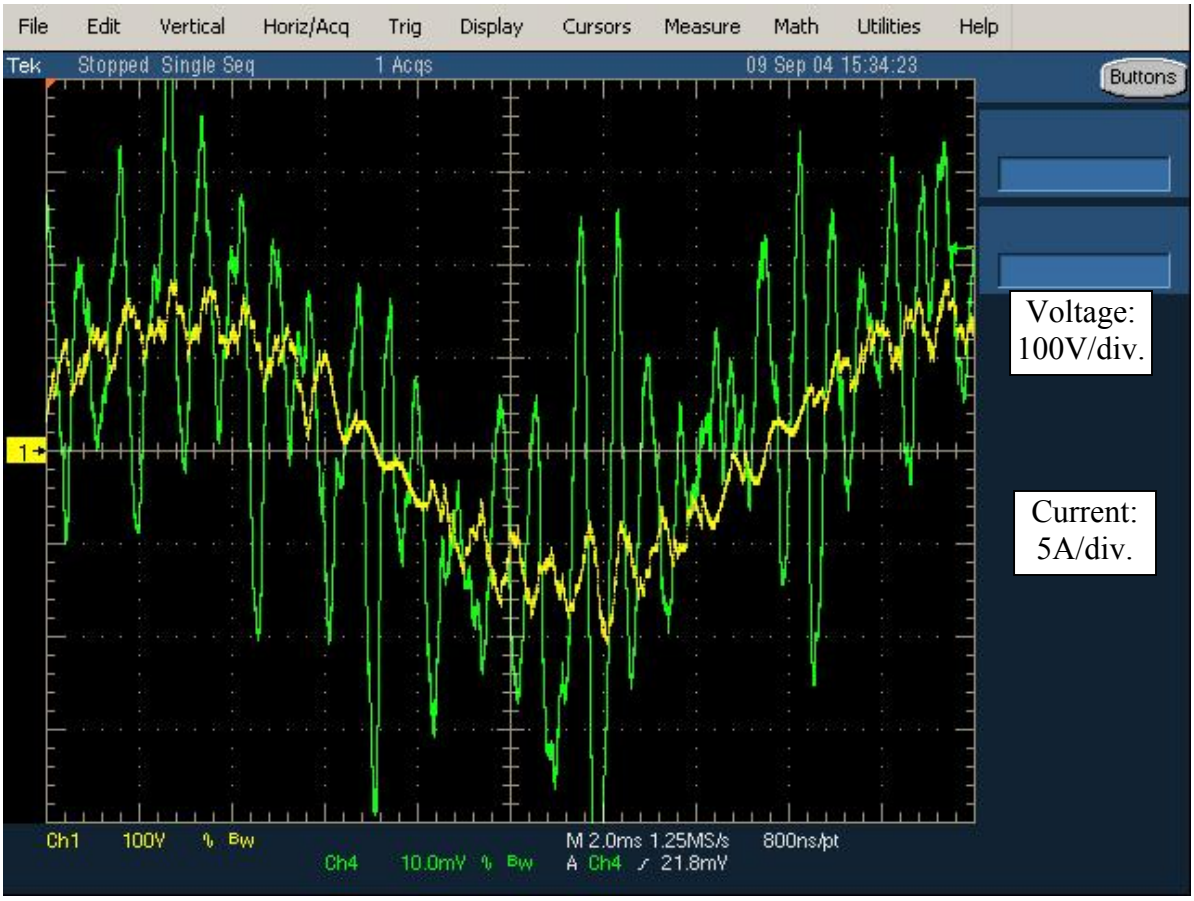


Waveform 9: External Probe Resonant Current Signal.

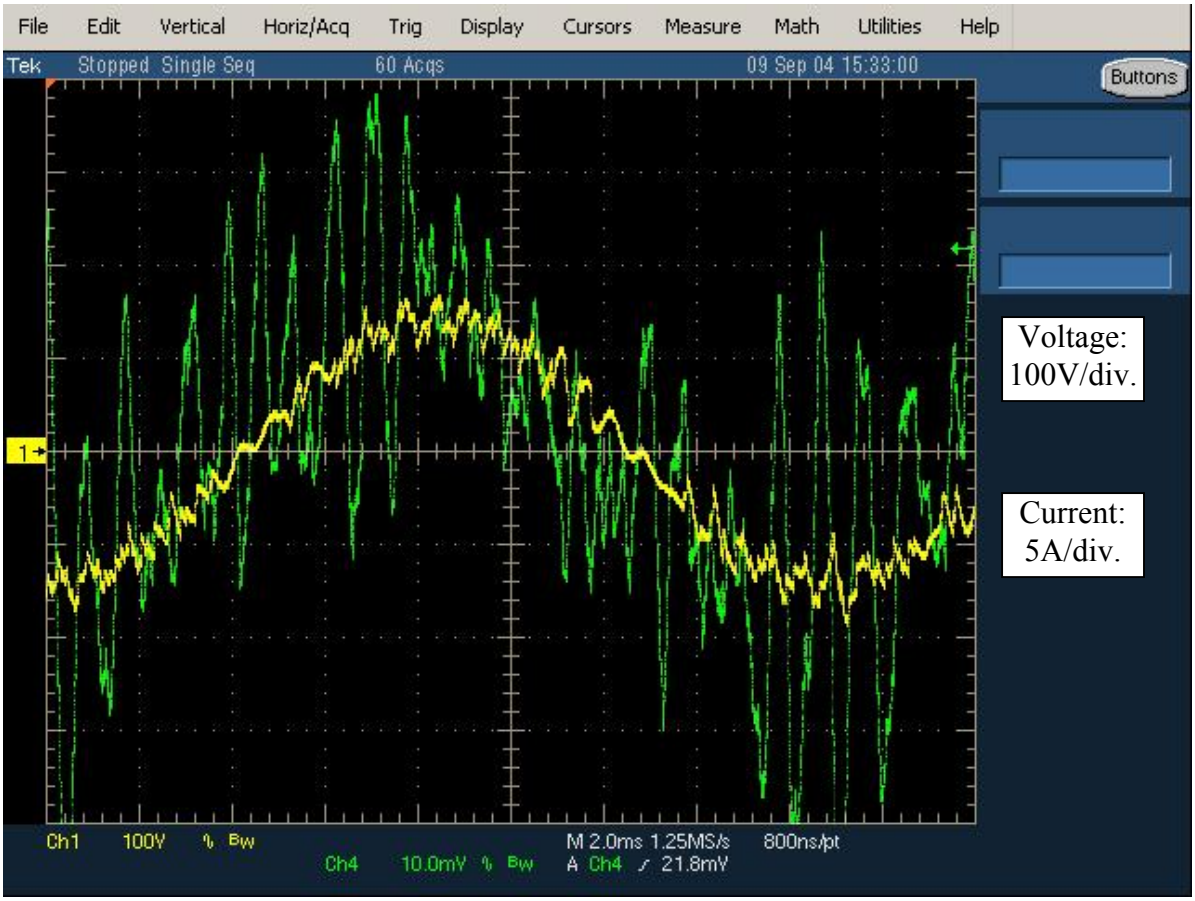
Waveform 10: External Probe Resonant Current Signal.



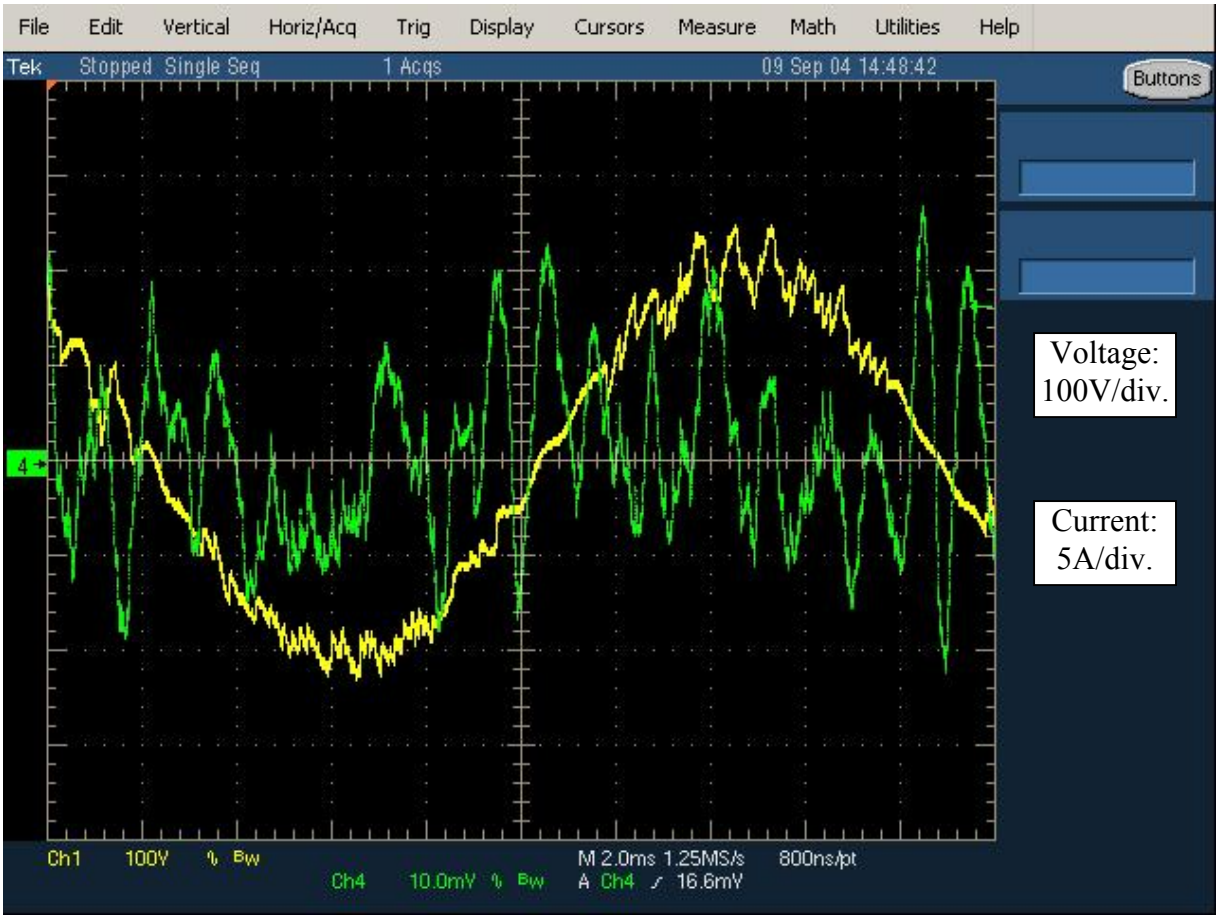
Waveform 11: Phase A Input Voltage (Yellow) and Current (Green).



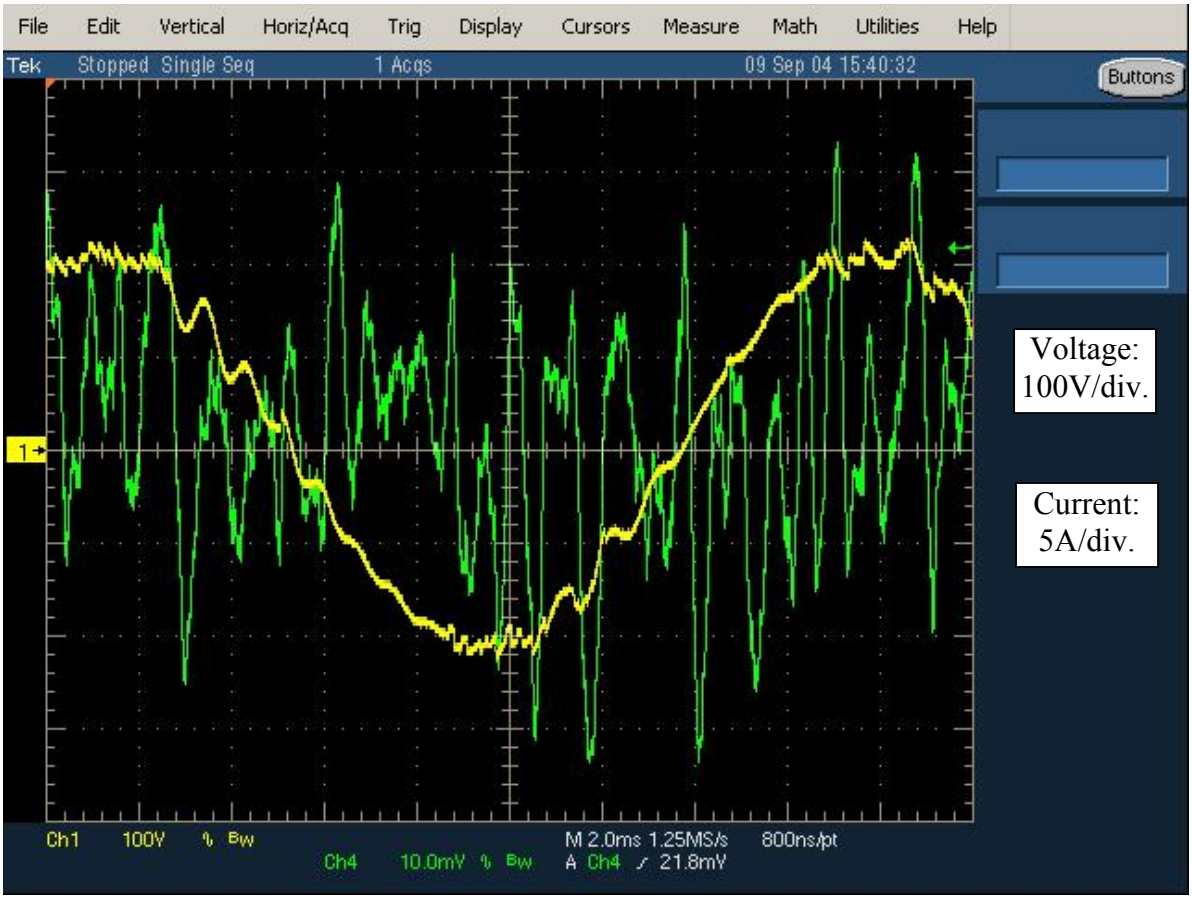
Waveform 12: Phase B Input Voltage (Yellow) and Current (Green).



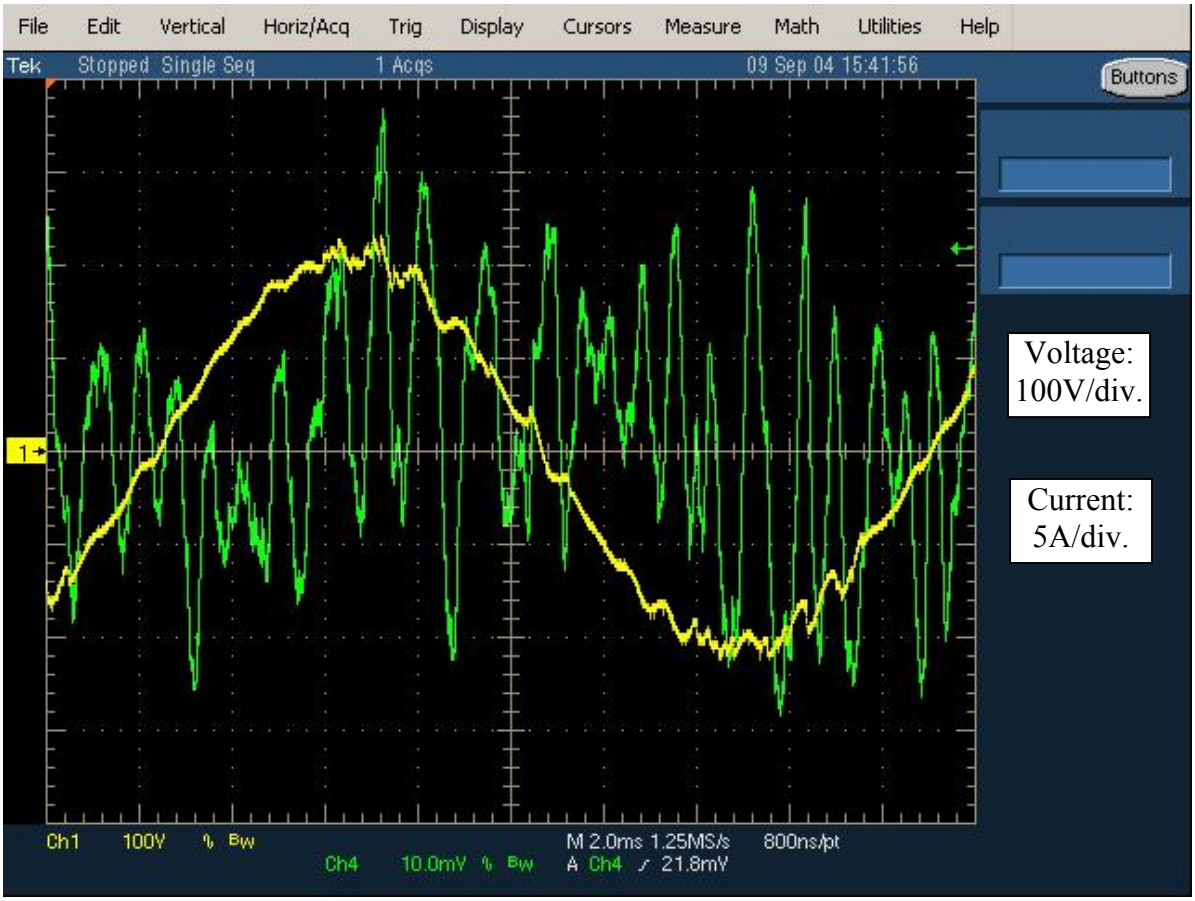
Waveform 13: Phase C Input Voltage (Yellow) and Current (Green).



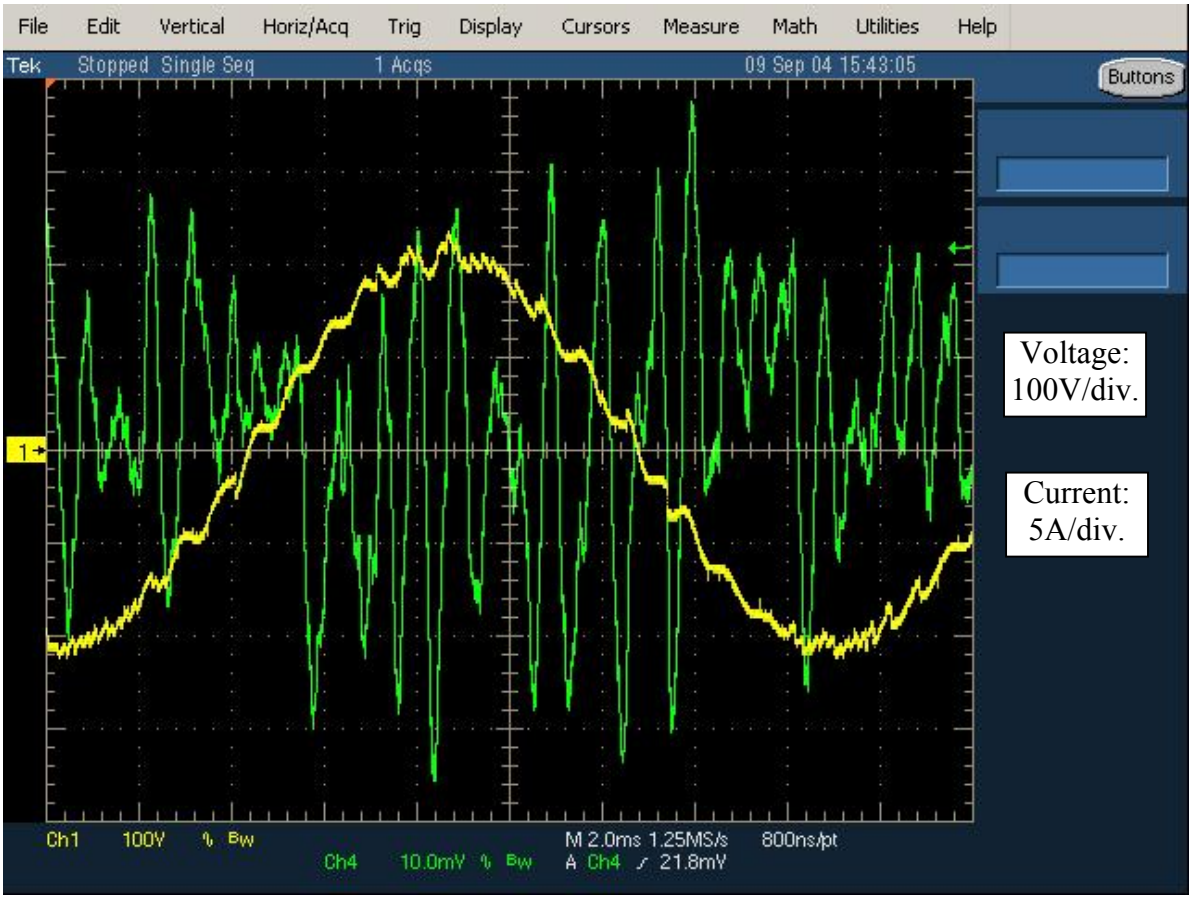
Waveform 14: Phase A Output Voltage (Yellow) and Current (Green).



Waveform 15: Phase B Output Voltage (Yellow) and Current (Green).



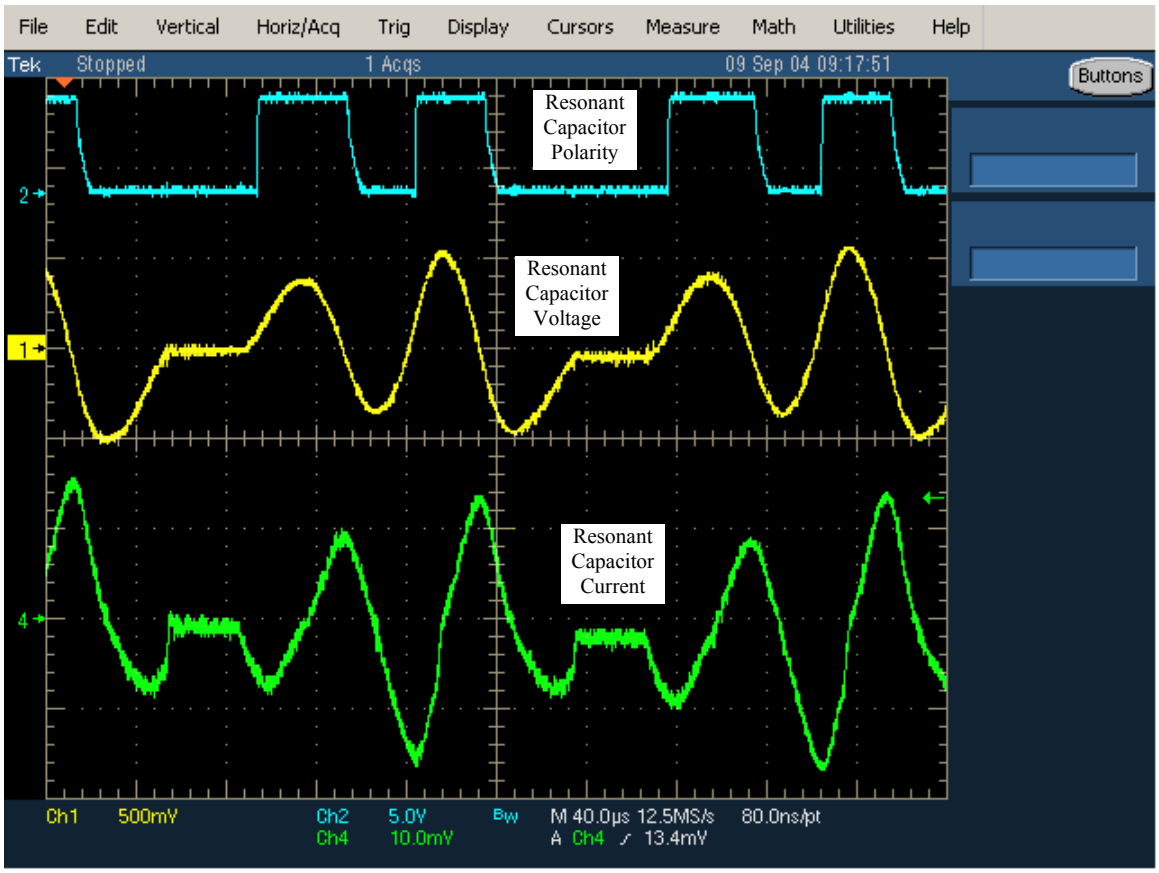
Waveform 16: Phase C Output Voltage (Yellow) and Current (Green).



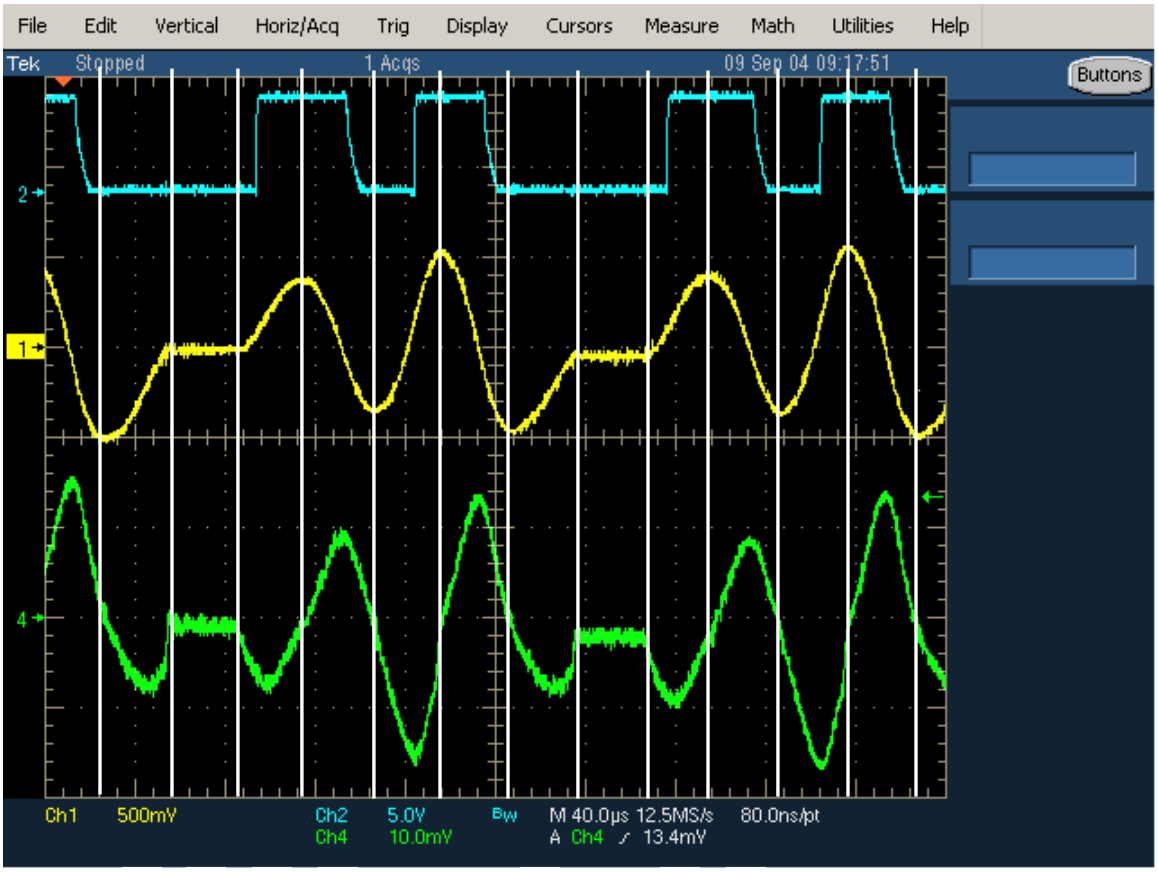
Example of 4 Cycle Hiccup Mode: 4 Good Cycles Then 1 Idle Cycle.

Conditions: Vin = Vout = 75Vrms (106V peak), fin = fout = 60Hz
Cycle Pulse Time = 31.5us, Resonant Pulse Time = 27.5us

The waveform pattern is shown, following:



The waveform with cycle-by-cycle commentary is shown as follows:



Poor Decision Here: Polarity Didn't Change

No Action Here!

Capacitor Charging Cycle Here

Good Decision Here!!

Good Decision Here!!

Good Decision Here!!

Poor Decision Here: Polarity Didn't Change

No Action Here!

Capacitor Charging Cycle Here

Good Decision Here!!

Good Decision Here!!

Good Decision Here!!

Please note that the cycle prior to the "No Action" cycle is the result of a bad or poor decision – it results in a voltage change that results in an extremely low final capacitor voltage and no polarity reversal. Remember that a goal of he present algorithm implementation is to reverse the capacitor polarity after each resonant pulse. Key in this outcome is the Polarity Management decision tree, the key question being "*Is Vcs*

polarity correct?" In the example pulse train, this is obviously not true. We have a tiny negative or quite-near-zero starting voltage on the capacitor with the wrong polarity, the logic decision indicates a ground-to-ground resonance to invert this voltage polarity. For extremely low capacitor voltages, particularly those less than the "ON" voltage of the IGBTs, ***an inversion will not occur***! Thus, the logic is "flawed" in allowing this condition.

To avoid this issue we have two choices: Ignore the 4 Cycle Hiccup Mode of operation and the attendant lost current cycle or We can add modify the logic decisions to insure that not only does the polarity invert, but it does so with sufficient margin such that near zero final capacitor values will never be encountered.

34kW ETM Converter Prototype Project Status:

The Plan for Remaining Functional and Performance Testing, and the Hardware and Software/Firmware Changes Required

Anthony G.P. Marini
***dtm* Associates**

January 10, 2005

34kW ETM Converter Prototype Project Status: 1/10/04

I.) Executive Summary

Functional power transfer at the ~3kW level was achieved by the ETM Converter prototype according to the operating algorithm/flow chart on 1/3/06. The resultant current into one of the input phase voltages (Phase A) and out of one of the output phase voltages (Phase A) was monitored. Nearly sinusoidal current (of the same frequency as the voltages) flowed at an approximate unity power factor for the input and at a –0.83 power factor for the output was observed and was used to verify proper operation. The remainder of the functional testing may now be completed at IQS/Marlboro Test Labs, with high range (200-415VAC) and variable input frequency testing remaining to be completed. Additionally, there are several functionality requirements that must be added via software/firmware revision.

II.) Test Summary

Since Functional Testing has commenced at the test labs, there were several catastrophic prototype problems encountered with the ETM prototype:

- IGBT and driver circuit destruction (set of 8) due to a GUI-related software issue. This issue has been corrected as of 10/04.
- IGBT failure (1 device) due to an unknown cause. The failed device is still undergoing failure analysis at the vendor (Dynex Semiconductor). New IGBTs were obtained and the prototype was repaired as of 12/04.

There were also several issues that occurred with the test equipment (oscilloscope and current probe amplifier) – the both pieces of equipment failed in a non-operational mode. As a result, the test equipment was replaced by the rental vendor on 12/20/04.
The consequence of the single IGBT failure and the equipment failure was an approximate 4 weeks loss of test time.

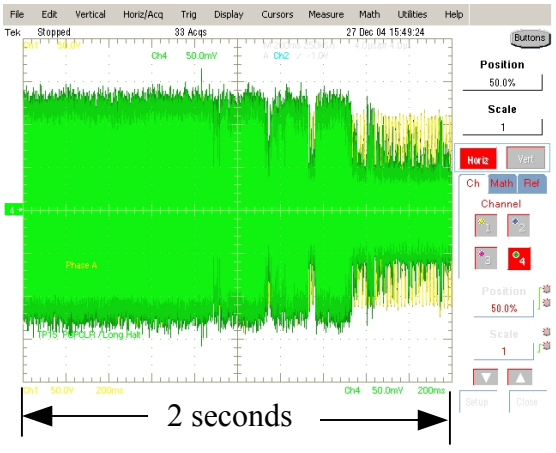
Functional Testing was re-started on 10/23/04. The prototype was brought to a 100Vrms input and output voltage level to observe the efficacy of the repairs. The GUI-related operating parameters for the prototype were optimized – the Resonance Time (17.5us), the Cycle Time (21.5us) and the IOSF (flow chart question #3) scale factor (1.5). The operation of the converter was observed for the following parameters:

- Resonant Capacitor Voltage,
- Resonant Inductor Current,
- Phase A Output Voltage and,
- Phase A Output Current

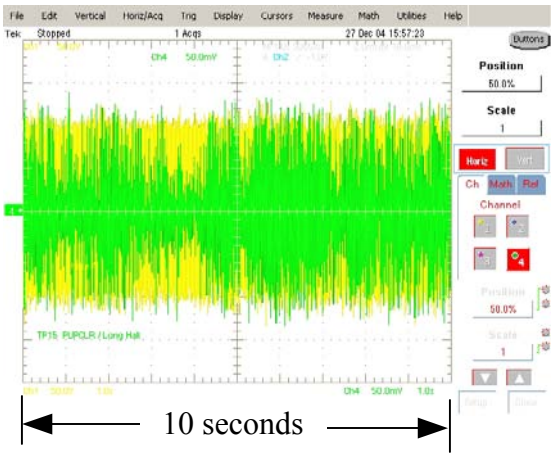
As a result of the testing it was observed that the operation of the converter was inconsistent, and the converter eventually self-shut down in a random manner with time. The inconsistent operation is characterized by a "breathing" of the resonant voltage and current waveforms. The breathing is a random amplitude modulation of the voltage and current amplitudes with time. The level of the amplitude modulation observed was in the range of 40-200%.

Some examples of the breathing behavior are shown in the following oscilloscope traces (The green traces are the resonant capacitor voltage at 1068V per vertical division) and the yellow traces are Phase A Output voltage at 50V per vertical division):

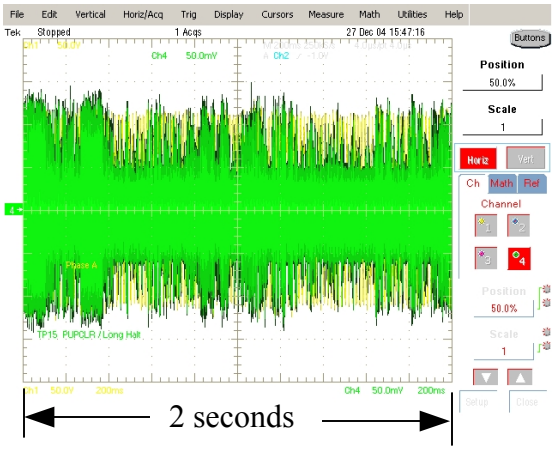
Trace 1



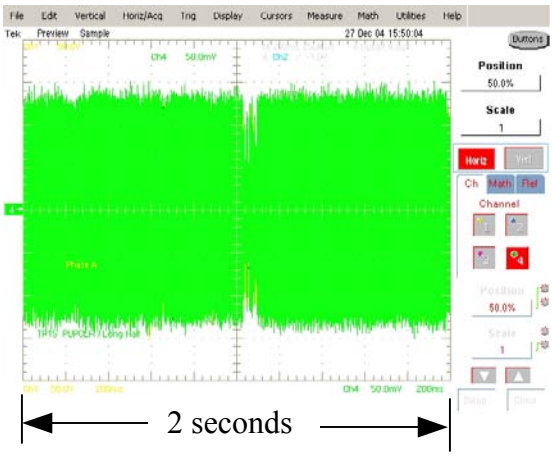
Trace 2



Trace 3



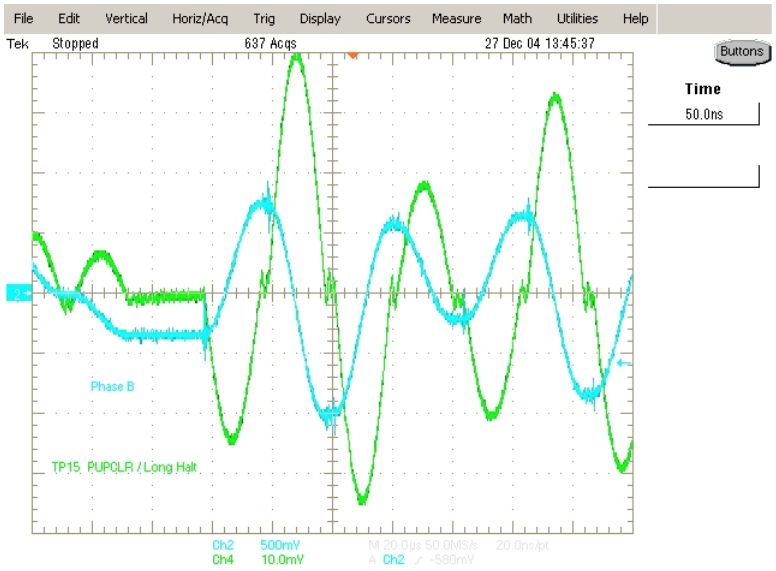
Trace 4



Please note that the previous traces are obtained during operation with unvarying input and output conditions. Trace 4 is indicative of the expected operation – continuous operation with a resultant consistent amplitude level resonant capacitor voltage and resonant inductor current (at least on a 60Hz cycle-by-cycle basis. It should be noted that there is an appreciable notch in operation where the resonant capacitor voltage amplitude drops to approximately 60% of the average peak value – an indicator of a problem.

It should be mentioned that exclusive of the breathing phenomenon that the resonant current transfer operation of the converter appears to be working properly, albeit inconsistently. The resonant current waveforms are properly formed – with alternating polarity and zero crossing switching behavior and with alternating resonant capacitor voltage polarity with successive pulses of resonant current (with some exceptions that are explainable by the converter operational logic flow chart). Oscilloscope Trace 5 highlights a typical resonant current (green) and capacitor voltage (blue) wave train sequence:

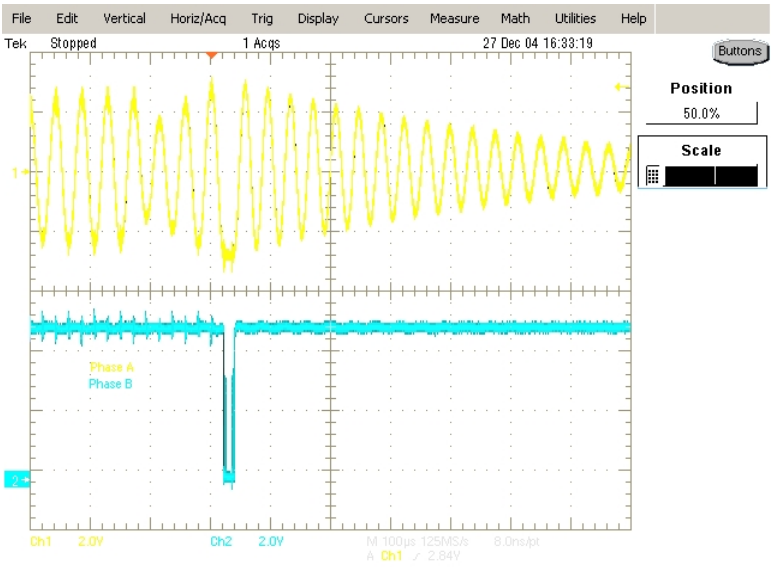
Trace 5



Another abnormal characteristic of operation of the prototype is a random shutdown/latch-off of the converter. After a successful operational start, the converter would operate for time periods of 1 second to a maximum of 20 seconds, followed by the shutdown event. After the shutdown/latch-off, the converter can always be successfully restarted via the GUI interface. The duration of operation until the shutdown event was observed to be independent of the IOSF scaling factor value, but it was dependent upon (and inversely proportional to) the value of the input and output voltages. As the input and output voltages are increased, the shorter the time period until the converter shut down.

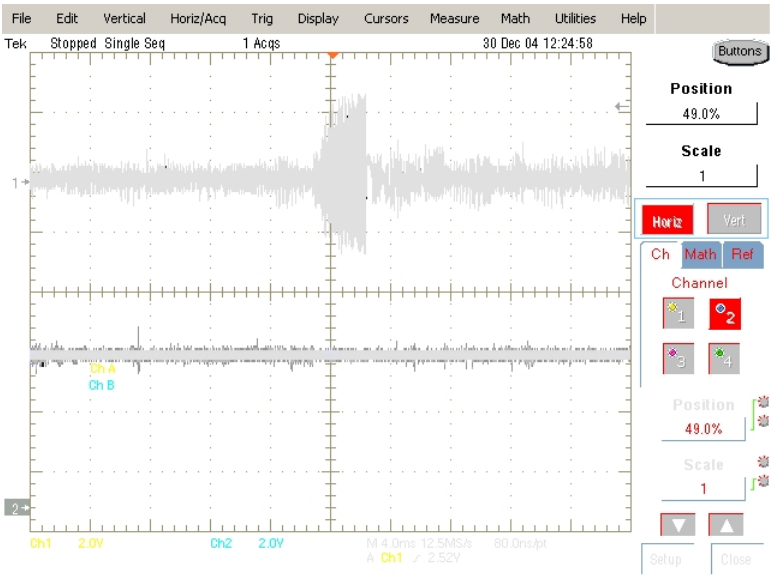
It was determined that the only event that could effect the shutdown of the converter is a resonant capacitor overvoltage (OV) event, as detected and reported by the dedicated hardware OV circuit to the ADSP inner loop microcontroller (U7). The output of this OV circuit was monitored in order to determine if the shut down was a result of noise in the converter, or an actual capacitor OV event. Oscilloscope Trace 6 shows the resonant capacitor voltage (yellow) and the low true logic OV event output (blue), demonstrating that there is indeed an actual OV event encountered:

Trace 6



Trace 6 also indicates that resonant capacitor voltage operates at a very high level (>1200Vpeak) prior to the OV event and the subsequent shutdown. This is an improbably high value, particularly since both the input and output voltages were set to 100Vpeak! After observation of the resonant capacitor voltage, it was determined that the capacitor voltage would run away in increasing peak amplitude over time periods of 15 to 50 resonant transfer cycles (~17.5us). It was also determined that these amplitude run away events would not necessarily always result in a system shutdown – the converter would many times recover to normal operation before the shutdown voltage threshold (1500V peak) was encountered. However, it was observed that a system shutdown was always coincident with a run away resonant capacitor voltage event. Oscilloscope Trace 7 indicates a resonant capacitor voltage run away event (top trace at 1068V per vertical division) that does not result in a system shutdown:

Trace 7



Based on the testing until that time, it appeared that the breathing and the run away voltage problem were the only impediments to proper ETM converter prototype operation. The initial thoughts were that the breathing problem was associated with noise in the system and that the run away problem was associated with a flawed implementation of the operational logic flow chart.

As a result of the speculation and to get a firm handle on the problems once-and-for-all, hardware and software debugging was convened at the on-site test labs on Jan. 3, 2005. The problem solving effort was divided into two parts according to the two problems observed. Much work was done to reduce/eliminate the breathing inconsistency observed. It was originally felt that the breathing was caused by jitter noise (on the AC input and output phase signals) influencing the proper time when zero crossings of the phase inputs were detected. Improper or multiple detections due to noise would cause the inner loop control to jump ahead in the switch index table and cause improper energy transfer at a given time in the cycle. To this end, the cutoff frequencies for the low pass filters associated with the phase detectors were decreased from ~40kHz to ~400Hz. Additionally, the firmware associated with the inner loop controller (ADSP) was changed to correct the scaling factors associated with the digitization of the resonant capacitor

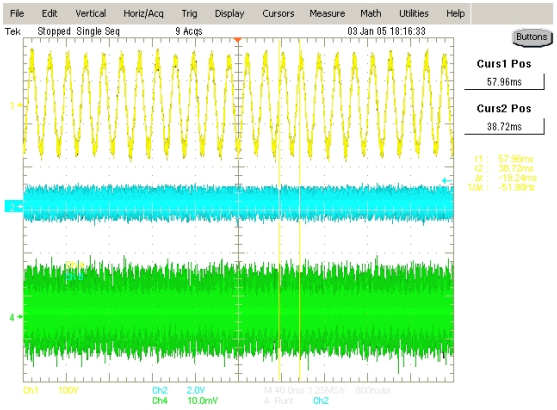
voltage. The firmware change corrected an approximate 60% error in the scaling factor. With these two changes implemented, the breathing problem was eliminated!

Attention was next turned to the run away capacitor voltage event. After a thorough review, there were no firmware/software or hardware reasons for this event's occurrence. It was next speculated that the ADSP microcontroller might be out of "real time", meaning that the amount of time required to execute the program code exceeds the presently used Cycle Time. This symptom is probably aggravated by the fact that the resonance time for the prototype is 17.5us (versus the intended design value of 20us). To this end, the Cycle Time was increased from 21.5us to 23.5us. As a result, with the increased cycle time, the run away capacitor voltage event was eliminated! Indeed the ADSP was out of real time.

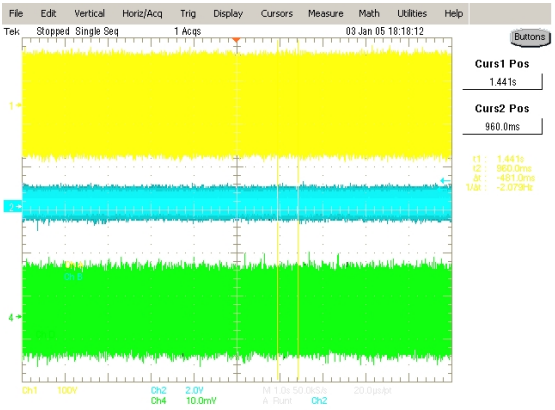
In order to check the results obtained from the changes implemented and to obtain a one-to-one correspondence between each change and the resultant outcome, the changes were "backed out" of the prototype by incorporating unchanged (original revision) Analog and Digital controller boards, and the cycle time was reduced to 21.5us. With the prototype in this configuration, the breathing and run away problems were both re-introduced. Next, the modified Analog board (with the decreased phase detector cutoff frequencies) was coupled to an unmodified Digital controller board. Both the breathing and the run away problems were present as in the unmodified case. (It was anticipated that the lower cutoff frequency would eliminate the breathing – this did not occur!) While still in the previous configuration, the Cycle Time was increased to 23.5us. The run away capacitor voltage event was eliminated. Next, the unmodified Analog board was coupled to a modified Digital board (changed scaling factor code). The cycle time was reduced to 21.5us. The breathing problem was eliminated, but however the run away problem was still present. The cycle time was increased to 23.5us and as a result the run away problem was eliminated. These results call into question the efficacy and necessity of the reduced phase detector cutoff frequencies. It is good design practice, however, to incorporate some level of filtering/cutoff frequency reduction for the phase detectors. However, there is still further work that needs to be done to arrive at the optimum filter values.

Oscilloscope Traces 8 and 9 show the resultant resonant current and resonant capacitor voltage waveforms. It should be noted that along with being very consistent with time, the amplitudes of both the current and the voltage assume more reasonable amplitude levels (Vcap = 230Vpeak and Ires = 25Apeak). Trace 8 is shown at 40ms per horizontal division and Trace 9 is 1 second per division.

Trace 8



Trace 9



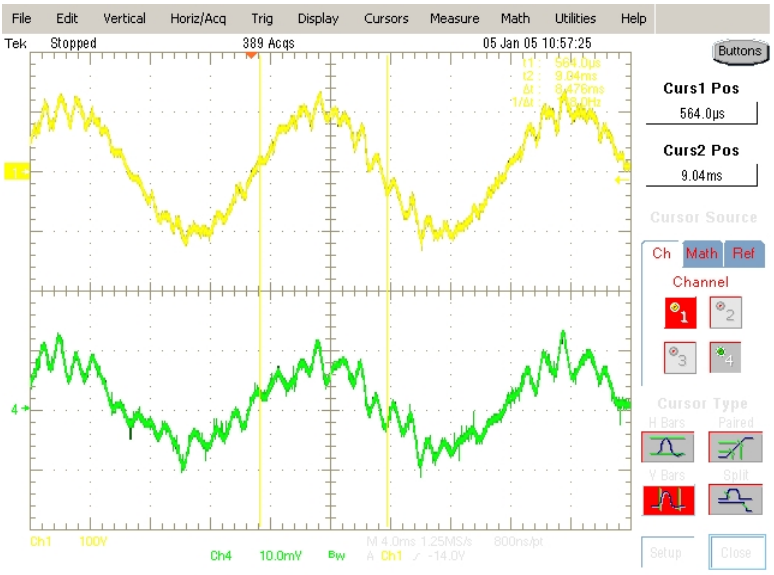
The consistency and stability of the resonant capacitor voltage (blue) and the resonant current (green) should be noted over the wide time spans observed.

Before the modifications were made to the prototype converter, the unit would not operate for more than 20 seconds before a shutdown/latch off event. After the change, the converter operated continuously for more than 45 minutes before it was manually shut down (via the GUI)!

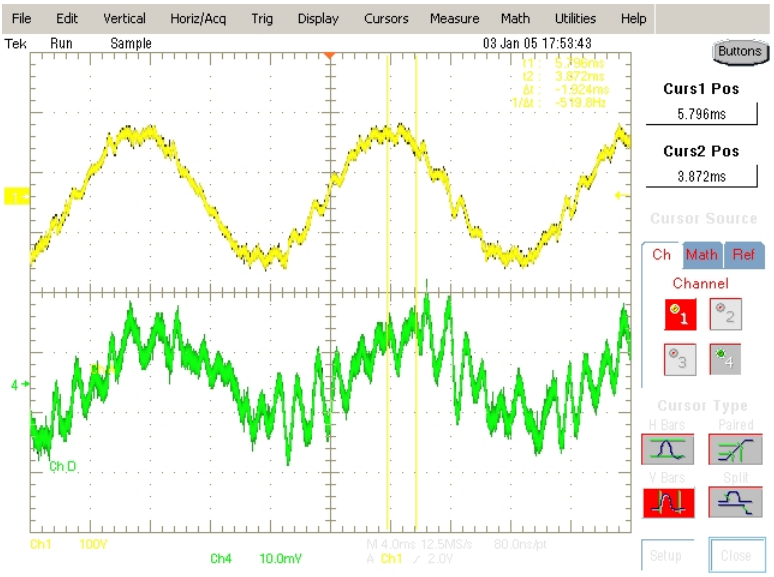
Regardless of how uniform and well-formed the resonant waveforms appear, the purpose of the ETM converter is to draw sinusoidal current at a unity power factor from the input phases and to provide sinusoidal current at a unity (but adjustable) power factor to the output phases. To this end, the voltage and current were observed for the Phase A input and output. Oscilloscope Trace 10 shows the input voltage (yellow) and the input current (green), and Trace 11 shows the output voltage (yellow) and output current (green). Note

that the resultant converter currents are nearly sinusoidal, the input power factor is approximately 1.0 and the output power factor is approximately –0.8.

Trace 10



Trace 11



The distortion or dV/dt jaggedness that appears on the input and output phase voltages is due to the relative smoothing provided by the phase input/output capacitors. In the present

prototype, these capacitors have a value of 33uF. Since the observed value of the deviations is approximately 10% of the peak-to-peak voltage amplitude (200Vp-p), or each dV is approximately 20V, maximum. These deviations will be worst-case "inside the box" due to the inductance presented by the grid load to the converter. Thus, in order to reduce the effects (erroneous zero crossing detections) of the dV/dt on the sensing circuitry in the ETM converter control, particularly the input/output/current phase detectors, these capacitors may require an increase in value to smooth out the resultant voltage deviations when the converter is operated at full grid voltage (415VAC/680Vp-p per line).

III.) Functional Test Wrap Up

Although the sources of the breathing and run away problems have been identified and corrected, there is still some functional testing that requires completion. The main area of test is the resonant current detection circuit (IRZC) for the zero crossing detector. Activities will center on obtaining Oscilloscope trace captures of the IRZC signal under various conditions of I/O voltage in the 100-415Vrms levels in order to observe that valid IRZC events occur at every resonant cycle. The last functional testing to be accomplished is the verification of the Phase A input and output current detectors and their associated phase detectors. This parametric sensing is required to be functional so that the control circuitry may determine/calculate the input and output power levels and power factors. Although not necessarily testing and data capture, there is one remaining circuit that must be verified for proper operation – the internal power supply circuit. Up to this point, an external +48Vdc power supply has been used provide power to the prototype converter. This is due to the low value of input/output voltage used to debug/troubleshoot the prototype; the magnitude of this voltage is inadequate to turn on the internal (to the converter) power supplies. Once these three areas have been addressed, the converter is ready to progress to parametric/performance testing.

IV.) Performance Test Progression

With the major impediments to the proper operation of the ETM Converter prototype understood and addressed and the eventual completion of the remaining functional

testing, performance testing of the prototype as a power converter may progress – limitations of the equipment available at the test labs). In order to facilitate easier data capture in future performance testing, a Fluke Model 434 Three Phase Power Quality Analyzer was obtained. Performance testing will include, but not be limited to, input variation testing, input frequency variation testing, input and output power factor testing (including output power factor adjustability), and fault event testing.

DIM200MBS12-A000

IGBT Bi-Directional Switch Module

Preliminary Information

Replaces issue May 2002, version DS5543-1.3

DS5545-2.1 June 2002

FEATURES

- 10µs Short Circuit Withstand
- Non Punch Through Silicon
- Isolated Copper Baseplate

KEY PARAMETERS

V_{DRM}		±1200V
V_T	(typ)	4.3V
I_C	(max)	200A
$I_{C(PK)}$	(max)	400A

APPLICATIONS

- Matrix Converters
- Brushless Motor Controllers
- Frequency Converters

The Powerline range of high power modules includes half bridge, chopper, dual, single and bi-directional switch configurations covering voltages from 600V to 3300V and currents up to 2400A.

The DIM200MBS12-A000 is a bi-directional 1200V, n channel enhancement mode, insulated gate bipolar transistor (IGBT) module. The IGBT has a wide reverse bias safe operating area (RBSOA) plus full 10µs short circuit withstand.

The module incorporates an electrically isolated base plate and low inductance construction enabling circuit designers to optimise circuit layouts and utilise grounded heat sinks for safety.

ORDERING INFORMATION

Order As:

DIM200MBS12-A000

Note: When ordering, please use the whole part number.

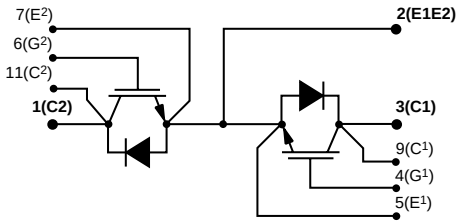
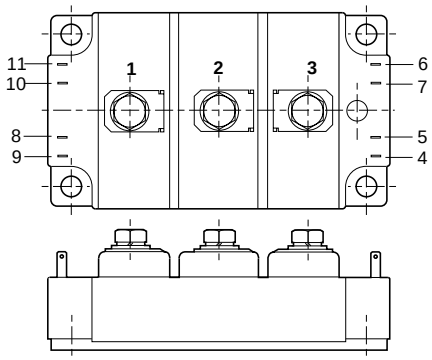


Fig. 1 Bi-directional switch circuit diagram



Outline type code: M

(See package details for further information)

Fig. 2 Electrical connections - (not to scale)

ABSOLUTE MAXIMUM RATINGS - PER ARM

Stresses above those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. In extreme conditions, as with all semiconductors, this may include potentially hazardous rupture of the package. Appropriate safety precautions should always be followed. Exposure to Absolute Maximum Ratings may affect device reliability.

T_{case} = 25˚C unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
V_{DRM}	Collector-emitter voltage (measured across terminals 2 and 3)	V_{GE} = 0V	1200	V
V_{GES}	Gate-emitter voltage	-	±20	V
I_C	Continuous collector current	T_{case} = 80˚C	200	A
$I_{C(PK)}$	Peak collector current	1ms, T_{case} = 115˚C	400	A
P_{max}	Max. transistor power dissipation	T_{case} = 25˚C, T_j = 150˚C	1435	W
I^2t	Diode I^2t value	V_R = 0, t_p = 10ms, T_{vj} = 125˚C	6.25	kA^2s
V_{isol}	Isolation voltage - per module	Commoned terminals to base plate. AC RMS, 1 min, 50Hz	2500	V
Q_{PD}	Partial discharge - per module	IEC1287. V_1 = 1300V, V_2 = 1000V, 50Hz RMS	10	PC

THERMAL AND MECHANICAL RATINGS

Internal insulation: Al_2O_3
Baseplate material: Cu
Creepage distance: 22mm
Clearance: 12mm
CTI (Critical Tracking Index): 175

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$R_{th(j-c)}$	Thermal resistance - transistor (per arm)	Continuous dissipation - junction to case	-	-	87	˚C/kW
$R_{th(j-c)}$	Thermal resistance - diode (per arm)	Continuous dissipation - junction to case	-	-	194	˚C/kW
$R_{th(c-h)}$	Thermal resistance - case to heatsink (per module)	Mounting torque 5Nm (with mounting grease)	-	-	15	˚C/kW
T_j	Junction temperature	Transistor	-	-	150	˚C
		Diode	-	-	125	˚C
T_{stg}	Storage temperature range	-	–40	-	125	˚C
-	Screw torque	Mounting - M6	-	-	5	Nm
		Electrical connections - M4	-	-	2	Nm

ELECTRICAL CHARACTERISTICS

T_{case} = 25˚C unless stated otherwise.

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Units
I_{CES}	Collector cut-off current	V_{GE} = 0V, V_{CE} = V_{CES}		-	-	0.25	mA
		V_{GE} = 0V, V_{CE} = V_{CES}, T_{case} = 125˚C		-	-	6	mA
I_{GES}	Gate leakage current	V_{GE} = ±20V, V_{CE} = 0V		-	-	1	µA
$V_{GE(TH)}$	Gate threshold voltage	I_C = 10mA, V_{GE} = V_{CE}		4.5	5.5	6.5	V
$V_{CE(sat)}$ †	Collector-emitter saturation voltage	V_{GE} = 15V, I_C = 200A		-	2.2	2.6	V
		V_{GE} = 15V, I_C = 200A, , T_{case} = 125˚C		-	2.6	3.0	V
V_T	On-state voltage	V_{GE} = 15V, I_C = 200A		-	4.3	5.0	V
	(measured across terminals 2 and 3)	V_{GE} = 15V, I_C = 200A, T_{case} = 125˚C		-	4.7	5.4	V
I_F	Diode forward current	DC		-	-	200	A
I_{FM}	Diode maximum forward current	t_p = 1ms		-	-	400	A
V_F †	Diode forward voltage	I_F = 200A		-	2.1	2.4	V
		I_F = 200A, T_{case} = 125˚C		-	2.1	2.4	V
C_{ies}	Input capacitance	V_{CE} = 25V, V_{GE} = 0V, f = 1MHz		-	23	-	nF
L_M	Module inductance - per arm	-		-	30	-	nH
R_{INT}	Internal transistor resistance - per arm	-		-	0.27	-	mΩ
SC_{Data}	Short circuit. I_{SC}	T_j = 125˚C, V_{CC} = 900V,	I_1		1375	-	A
		$t_p \leq 10\mu s$, $V_{CE(max)}$ = V_{CES} – L*. di/dt	I_2		1125	-	A
		IEC 60747-9					

Note:
† Measured at the power busbars and not the auxiliary terminals)
L* is the circuit inductance + L_M

ELECTRICAL CHARACTERISTICS

T_{case} = 25°C unless stated otherwise

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$t_{d(off)}$	Turn-off delay time	I_C = 200A	-	600	-	ns
t_f	Fall time	V_{GE} = ±15V	-	50	-	ns
E_{OFF}	Turn-off energy loss	V_{CE} = 600V	-	20	-	mJ
$t_{d(on)}$	Turn-on delay time	$R_{G(ON)}$ = $R_{G(OFF)}$ = 4.7Ω	-	240	-	ns
t_r	Rise time	L ~ 100nH	-	95	-	ns
E_{ON}	Turn-on energy loss		-	25	-	mJ
Q_g	Gate charge		-	2	-	µC
Q_{rr}	Diode reverse recovery charge	I_F = 200A, V_R = 600V,	-	30	-	µC
I_{rr}	Diode reverse current	dI_F/dt = 2100A/µs	-	125	-	A
E_{REC}	Diode reverse recovery energy		-	13	-	mJ

T_{case} = 125°C unless stated otherwise

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$t_{d(off)}$	Turn-off delay time	I_C = 200A	-	800	-	ns
t_f	Fall time	V_{GE} = ±15V	-	70	-	ns
E_{OFF}	Turn-off energy loss	V_{CE} = 600V	-	27	-	mJ
$t_{d(on)}$	Turn-on delay time	$R_{G(ON)}$ = $R_{G(OFF)}$ = 4.7Ω	-	385	-	ns
t_r	Rise time	L ~ 100nH	-	110	-	ns
E_{ON}	Turn-on energy loss		-	40	-	mJ
Q_{rr}	Diode reverse recovery charge	I_F = 200A, V_R = 600V,	-	50	-	µC
I_{rr}	Diode reverse current	dI_F/dt = 1900A/µs	-	140	-	A
E_{REC}	Diode reverse recovery energy		-	20	-	mJ

TYPICAL CHARACTERISTICS

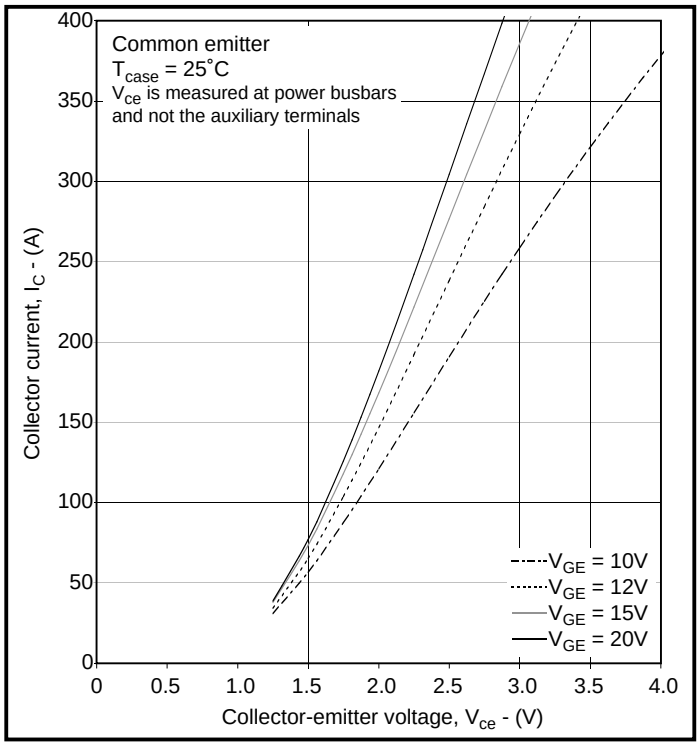


Fig. 3 Typical output characteristics

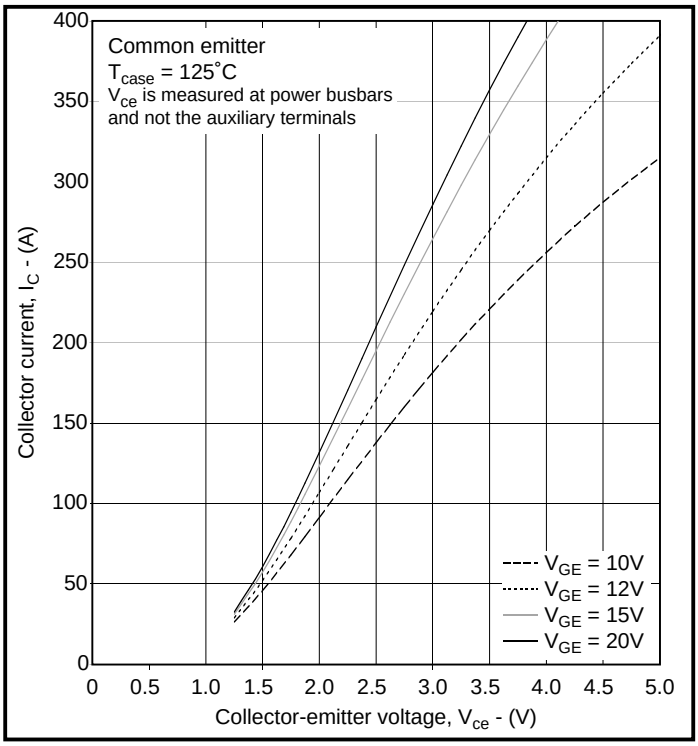


Fig. 4 Typical output characteristics

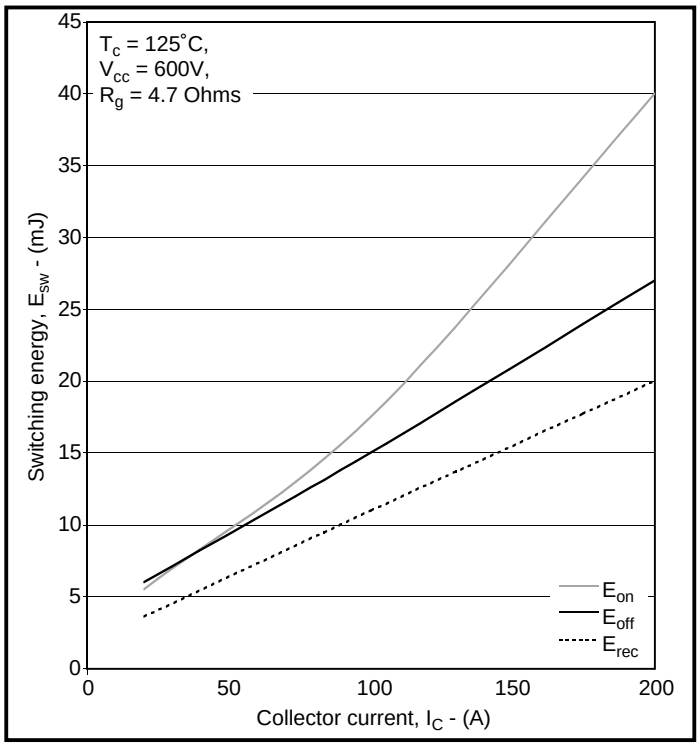


Fig. 5 Typical switching energy vs collector current

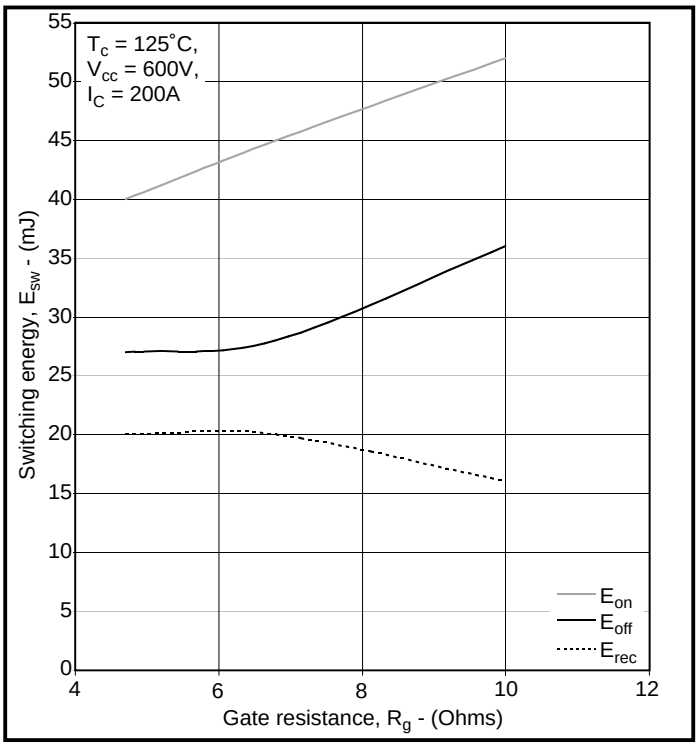


Fig. 6 Typical switching energy vs gate resistance

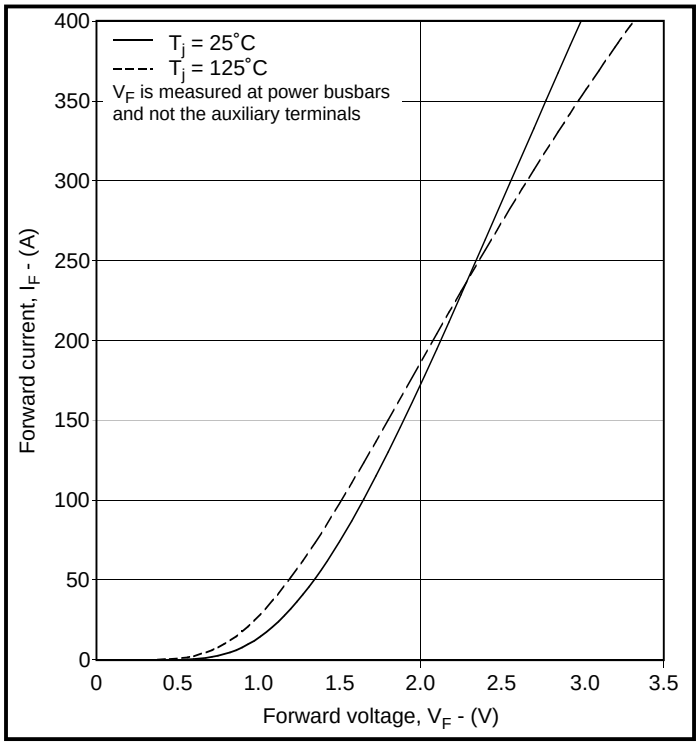


Fig. 7 Diode typical forward characteristics

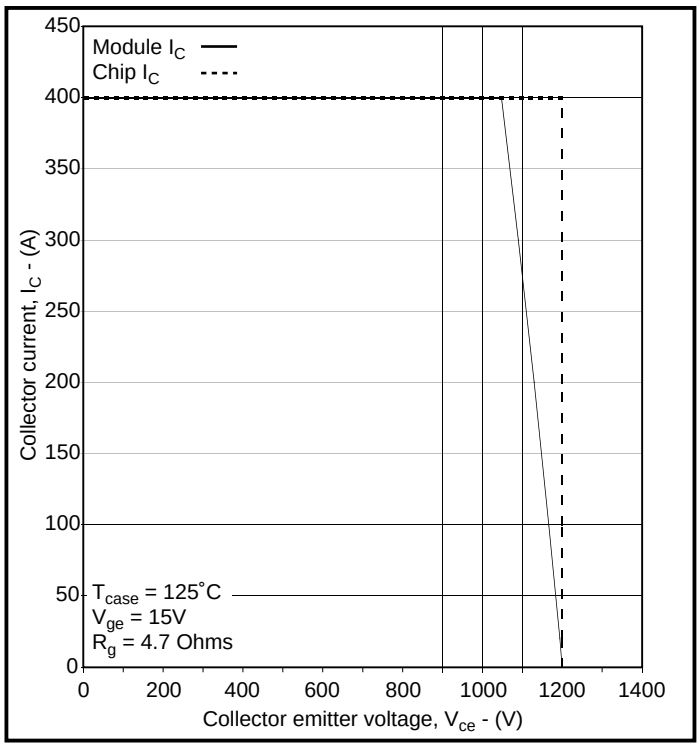


Fig. 8 Reverse bias safe operating area

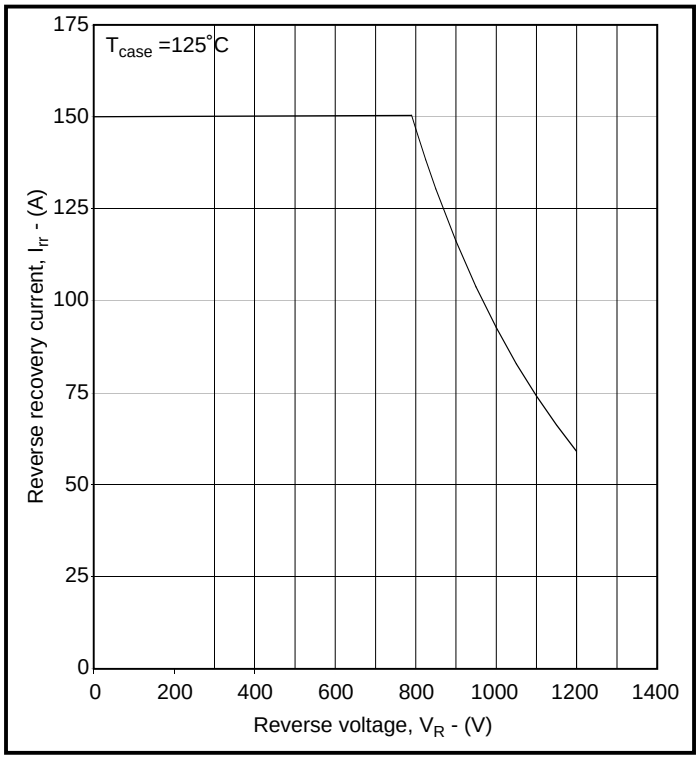
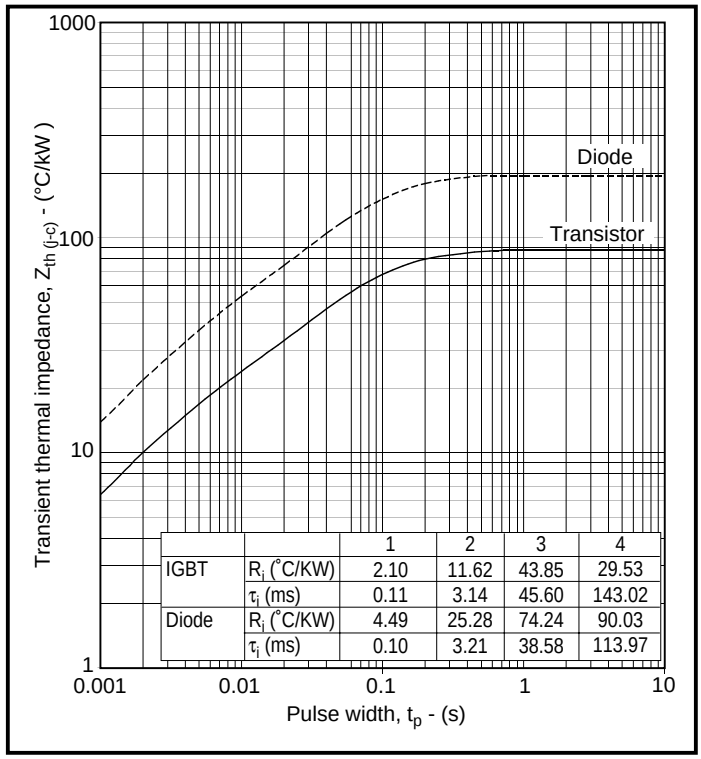


Fig. 9 Diode reverse bias safe operating area



		1	2	3	4
IGBT	R_i (˚C/KW)	2.10	11.62	43.85	29.53
	τ_i (ms)	0.11	3.14	45.60	143.02
Diode	R_i (˚C/KW)	4.49	25.28	74.24	90.03
	τ_i (ms)	0.10	3.21	38.58	113.97

Fig. 10 Transient thermal impedance

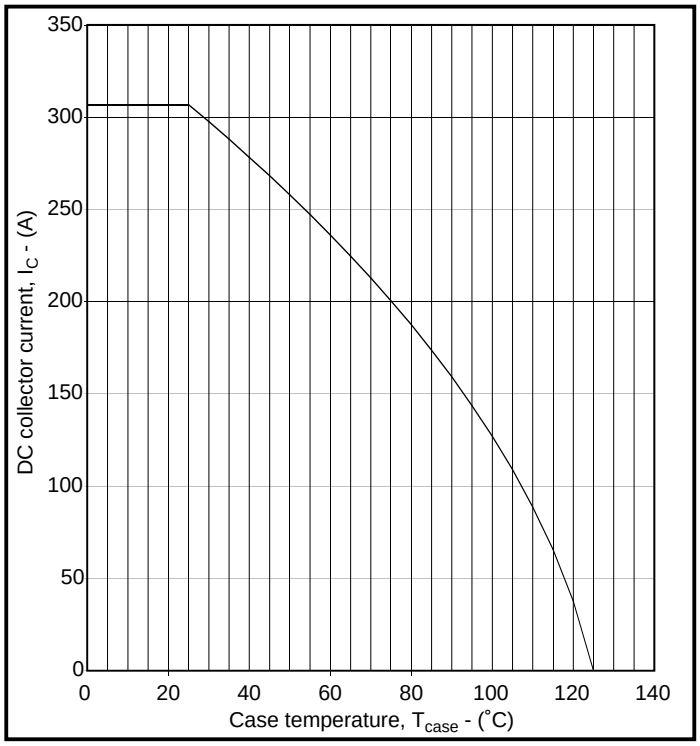


Fig. 11 DC current rating vs case temperature

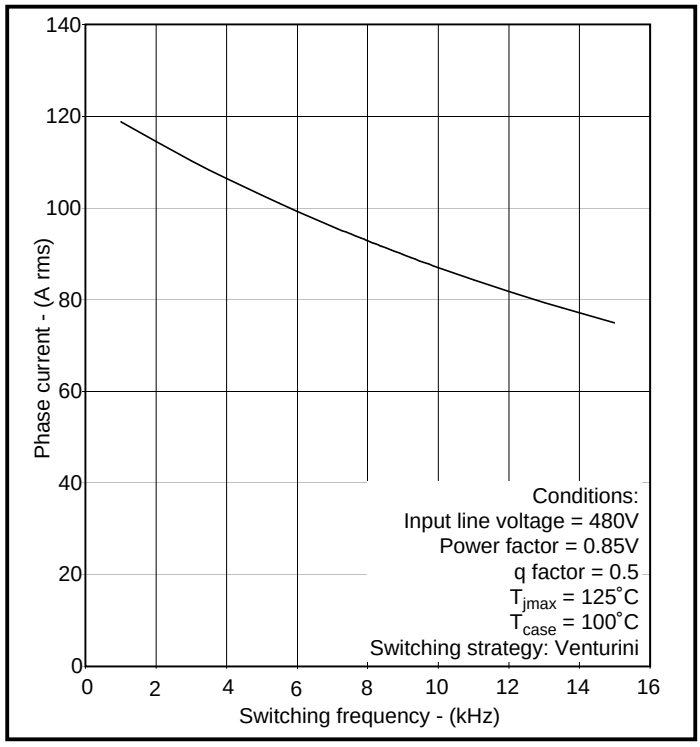
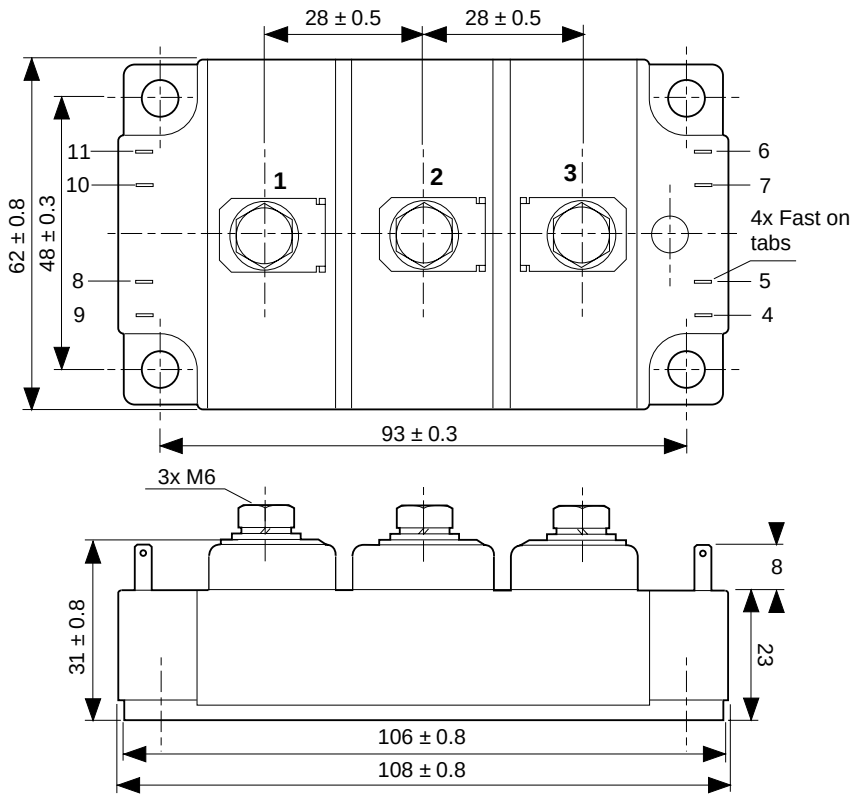


Fig. Fig. 12 Matrix converter phase current vs switching frequency

PACKAGE DETAILS

For further package information please visit our website or contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.



Nominal weight: 270g
Recommeded fixings for mounting: M6
Recommended mounting torque: 5Nm (44lbs.ins)
Recommended torque for electrical connections (M6): 5Nm (44lbs.ins)

Module outline type code: M

POWER ASSEMBLY CAPABILITY

The Power Assembly group was set up to provide a support service for those customers requiring more than the basic semiconductor, and has developed a flexible range of heatsink and clamping systems in line with advances in device voltages and current capability of our semiconductors.

We offer an extensive range of air and liquid cooled assemblies covering the full range of circuit designs in general use today. The Assembly group offers high quality engineering support dedicated to designing new units to satisfy the growing needs of our customers.

Using the latest CAD methods our team of design and applications engineers aim to provide the Power Assembly Complete Solution (PACs).

HEATSINKS

The Power Assembly group has its own proprietary range of extruded aluminium heatsinks which have been designed to optimise the performance of Dynex semiconductors. Data with respect to air natural, forced air and liquid cooling (with flow rates) is available on request.

For further information on device clamps, heatsinks and assemblies, please contact your nearest sales representative or Customer Services.

DYNEX SEMICONDUCTOR

http://www.dynexsemi.com

e-mail: power_solutions@dynexsemi.com

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Datasheet Annotations:

Dynex Semiconductor annotate datasheets in the top right hard corner of the front page, to indicate product status. The annotations are as follows:-

Target Information: This is the most tentative form of information and represents a very preliminary specification. No actual design work on the product has been started.

Preliminary Information: The product is in design and development. The datasheet represents the product as it is understood but details may change.

Advance Information: The product design is complete and final characterisation for volume production is well in hand.

No Annotation: The product parameters are fixed and the product is available to datasheet specification.

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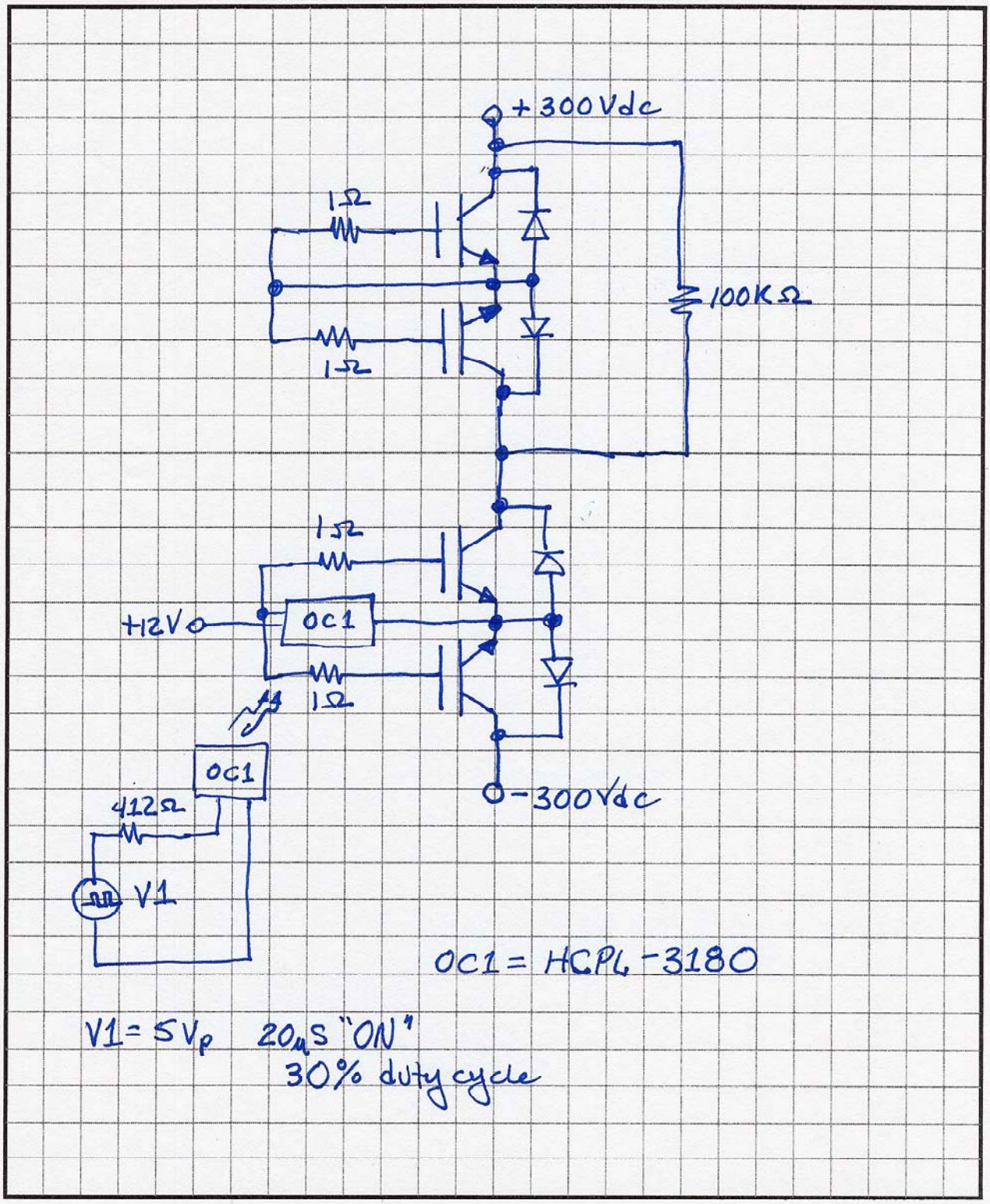
[redacted]



Engineering Consultants Specializing In Design and Development
Of Electronic Components, Circuits and Systems.

ETM Converter Test Matrix

Prepared by Tony Marini ***dtm*** **Associates** **1/22/2004**

Electrical Tests	Debug Tests	Functional Tests	Performance Tests	Safety/Compliance Tests	System Integration Tests
Input-to-Output Power Processing: Power Level					
Low Frequency/Low Amplitude		X	X		X
Nominal Frequency/Nominal Amplitude	X	X	X		X
High Frequency/High Amplitude		X	X		X
Conversion Efficiency			X		X
Quiescent Power		X	X		X
Input Current Verification					
Waveform Fidelity		X	X		X
Power Factor	X	X	X		X
Output Current Verification					
Waveform Fidelity		X	X		X
Harmonic Distortion			X		X
Power Factor Adjustability	X	X	X		X
Input/Output Fault Performance					
Input Phase Shedding			X		X
Input Overcurrent			X		X
Input Undervoltage			X		X
Input Overvoltage			X		X
Output Phase Shedding			X		X
Output Overcurrent			X		X
Output Undervoltage			X		X
Output Overvoltage			X		X
Output Sags/Transient Undervoltage			X		X
Output Noise Immunity					X
Abnormal Operating Condition Tests					
Output Surges				X	X
Output Transients				X	X
Input Short Circuit			X	X	X
Output Short Circuit			X	X	X
Loss of Control Fault (Fail Safe)			X	X	X
Safety/Compliance Tests					
IEEE-519				X	X
UL-1741				X	X
UL-1950				X	
FCC Part 15J				X	
EN5002				X	
Dielectric Breakdown Tests			X	X	
Heatsink Temperature				X	X
Impaired Cooling				X	X

Debug Tests: Require lab instruments and fixed frequency, variable voltage AC power sources for input and output power supplies. These tests will be performed on the 34kW prototype device only.

Functional Tests: Require lab instruments and variable frequency/voltage AC power sources for input and output power supplies. The input source may be a VSD motor driving a 100kW generator, and the output may be a transformer-coupled grid connection to 408VAC. These tests will be performed on the 34kW prototype and the 100kW system and individual modules.

Performance Tests: Require lab instruments and variable frequency/voltage AC power sources for input and output power supplies. The input source will be a VSD motor driving a 100kW generator, and the output will be a direct-coupled grid connection to 408VAC. These tests will be performed on the 100kW system and individual modules.

Safety/Compliance Tests: Require lab instruments and variable frequency/voltage AC power sources for input and output power supplies. The configuration will be determined by UL and any other appropriate agency requirements. These tests will be performed on the 100kW system and individual modules.

System Integration Tests: Requires a wind powered generator in an operating configuration to act as the power source for the converter. The output will be connected directly to a three phase 408VAC utility grid or pseudo-grid. These tests will be performed on the 100kW system and individual modules.

34kW ETM Converter Test Matrix for Sandia Labs

Normal Grid Tests							
			I/O Parameters				
Test#	**Test Name**	**Test Duration**	**Vin**	**fin**	**Vout**	**fout**	**Parameters Measured**
1	Static Input @ fin(min), Vin(min)	30 minutes	min	min	415L-L	60Hz	PFin, Pin, Pout, T(start), T(end), Efficiency
2	Static Input @ (fin(max)-fin(min))/2, (Vin(max)-Vin(min))/2	30 minutes	(Vin(max)-Vin(min))/2	(fin(max)-fin(min))/2	415L-L	60Hz	PFin, Pin, Pout, T(start), T(end), Efficiency
3	Static Input @ fin(max), Vin(max)	30 minutes	min	min	415L-L	60Hz	PFin, Pin, Pout, T(start), T(end), Efficiency
4	Static Input @ fin(min), Vin(min)	30 minutes	min	min	415L-L	47Hz	PFin, Pin, Pout, T(start), T(end), Efficiency
5	Static Input @ (fin(max)-fin(min))/2, (Vin(max)-Vin(min))/2	30 minutes	(Vin(max)-Vin(min))/2	(fin(max)-fin(min))/2	415L-L	47Hz	PFin, Pin, Pout, T(start), T(end), Efficiency
6	Static Input @ fin(max), Vin(max)	30 minutes	min	min	415L-L	47Hz	PFin, Pin, Pout, T(start), T(end), Efficiency
7	Static Input @ fin(min), Vin(min)	30 minutes	min	min	415L-L	63Hz	PFin, Pin, Pout, T(start), T(end), Efficiency
8	Static Input @ (fin(max)-fin(min))/2, (Vin(max)-Vin(min))/2	30 minutes	(Vin(max)-Vin(min))/2	(fin(max)-fin(min))/2	415L-L	63Hz	PFin, Pin, Pout, T(start), T(end), Efficiency
9	Static Input @ fin(max), Vin(max)	30 minutes	min	min	415L-L	63Hz	PFin, Pin, Pout, T(start), T(end), Efficiency
10	Dynamic Sweep Input: fin Swept fin(min) to fin(max) and Vin Swept from Vin(min) to Vin(max): Sweep Duration = 30 seconds.	500 Input Sweep Cycles: 5 Second Pause Between Sweeps	Vin(min) to Vin(max)	fin(min) to fin(max)	415L-L	60Hz	PFin, Pin, Pout, T(start), T(end), Efficiency, Harmonic Instabilities
11	Dynamic Sweep Input: fin Swept fin(min) to fin(max) and Vin Swept from Vin(min) to Vin(max): Sweep Duration = 30 seconds.	500 Input Sweep Cycles: 5 Second Pause Between Sweeps	Vin(min) to Vin(max)	fin(min) to fin(max)	415L-L	47Hz	PFin, Pin, Pout, T(start), T(end), Efficiency, Harmonic Instabilities
12	Dynamic Sweep Input: fin Swept fin(min) to fin(max) and Vin Swept from Vin(min) to Vin(max): Sweep Duration = 30 seconds.	500 Input Sweep Cycles: 5 Second Pause Between Sweeps	Vin(min) to Vin(max)	fin(min) to fin(max)	415L-L	63Hz	PFin, Pin, Pout, T(start), T(end), Efficiency, Harmonic Instabilities
13	Dynamic Step Input: Step Pause = 3 Seconds, Ramp Time Frequency-to-Frequency = 2 Seconds (See Note 2)	500 Input Step Cycles: 5 Second Pause Before New Step Sequence	Vin(min) to Vin(max)	fin(min) to fin(max)	415L-L	60Hz	PFin, Pin, Pout, T(start), T(end), Efficiency, Harmonic Instabilities
14	Dynamic Step Input: Step Pause = 3 Seconds, Ramp Time Frequency-to-Frequency = 2 Seconds (See Note 2)	500 Input Step Cycles: 5 Second Pause Before New Step Sequence	Vin(min) to Vin(max)	fin(min) to fin(max)	415L-L	47Hz	PFin, Pin, Pout, T(start), T(end), Efficiency, Harmonic Instabilities
15	Dynamic Step Input: Step Pause = 3 Seconds, Ramp Time Frequency-to-Frequency = 2 Seconds (See Note 2)	500 Input Step Cycles: 5 Second Pause Before New Step Sequence	Vin(min) to Vin(max)	fin(min) to fin(max)	415L-L	63Hz	PFin, Pin, Pout, T(start), T(end), Efficiency, Harmonic Instabilities
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Note 1 Input Frequency and Voltage increased according to Figure 1

Note 2 Input Frequency and Voltage increased according to Figure 1. Input Frequency Increased From fin(min) by 10%, Then Decreased by 5%, Then Increased by 10%, Then Decreased by 5% and so on Until fin(max) is reached.