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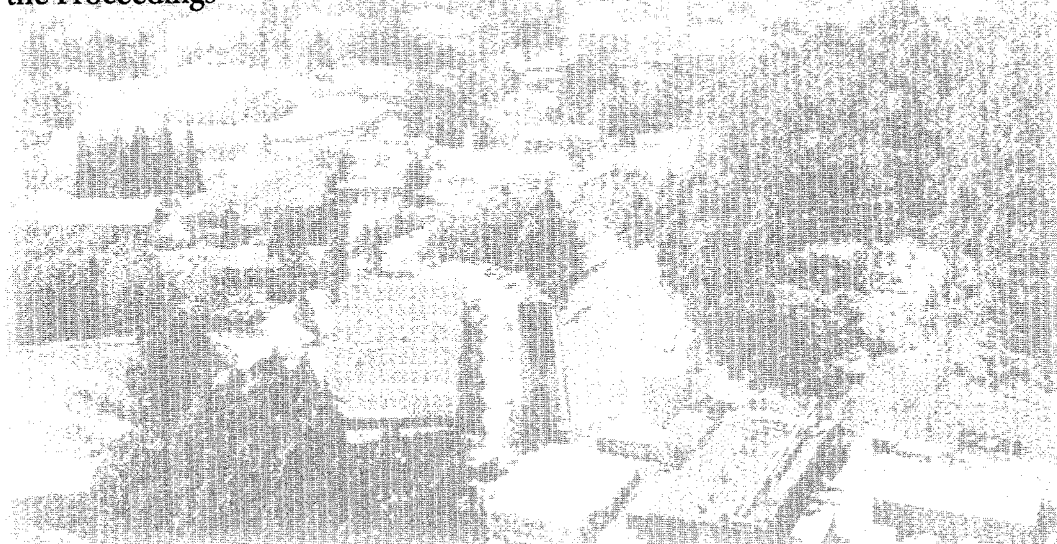

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Adaptive Readout Technique
for a Sixteen Channel Peak Sensing ADC in the FERA Format[1]

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Abstract

An adaptive, variable block-size readout technique for use with multiple, sixteen-channel CAMAC ADCs with a FERA-bus readout has been developed and designed. It can be used to read data from experiments with or without coincidence, i.e. singles, without having to change the readout protocol. Details of the implementation are discussed and initial results are presented. Further applications of the adaptive readout are also discussed.

I. Introduction

Modern synchrotron X-ray sources are characterized by high intensities. In order to utilize this advantage one has to design very fast processing-electronics for the synchrotron radiation detectors. We have built a 64-element X-ray detector system based on a silicon detector array wirebonded to an integrated circuit for charge integration, signal shaping, and amplification [1]. We have developed an IC to process the signals from this detector at high rate [2]. To digitize the signals from this IC we have constructed a sixteen-channel ADC with FERA-readout packaged in a single width CAMAC module [3]. This module contains sixteen independent 11-bit ADC daughter boards mounted on a motherboard. When multiple modules are placed on the same FERA-bus, bus-contention becomes a serious problem at high rates. This issue had to be addressed in this application because the different ADCs can have widely different count rates. The main motivation to implement this new readout method was to utilize the FERA-bus more efficiently than the way a conventional readout does. This is normally done by forcing a readout when a FIFO is half full. Also, every event from the buffer has to be read out when data collection is halted. In a conventional system the solution would be to issue a command to flush all FIFOs to recover all the data that remain unread. Our readout has been designed to adapt the buffer size dynamically from 1 to 32 words. This results in the efficiency of a 32-word block size when needed at high rates. At the same time, every word from the buffer memory is read automatically from each module in the data acquisition system.

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II. Module Description

All of the logic for this CAMAC Module is implemented in a XILINX XC4008 FPGA. In the FPGA multiple state machines are realized. The ADC state machine handles the data flow from the daughter boards into a buffer memory. Another state machine, the FERA state machine, handles the readout of the buffer memory onto the FERA-bus. The adaptable block size function is realized in both of these state machines. The module was designed to be compatible with commercially available electronic modules. We have, therefore, chosen the CAMAC standard for parameter control and mechanical housing and the FERA protocol for high-speed readout.

The ADCs are self-triggering and can, therefore, be used to collect random single or coincidence events (see below). In order to read the random data from the ADCs, a priority encoder is used to control the flow of data into a buffer memory 32-words deep. The readout of this buffer depends on the time structure of the incoming pulses and on the limits imposed on the block size. For example, if a minimum block size of 16 words is set, the block of data will adapt, i.e. vary from 16 words through 32 words, depending on the incoming rate. By setting the minimum block size to 1 word the block size adapts from 1 word through 32 words. In this case, if the rate is low, every event will be read out individually. At higher rates the data are collected into blocks of increasing size. By grouping the data words into larger blocks, the overhead associated with the capture of the FERA-bus and generation of a header word is minimized. If the acquisition is stopped, all remaining data in the buffer memories are read out since this case is interpreted as a low rate situation.

III. Circuit Description

As the individual ADC daughter boards are digitizing incoming pulses, the ADC state machine is in operation storing data in the buffer memory. While the ADC state machine is operating, the adaptive logic is checking to see if certain criteria are meet. The criteria are:

a) Minimum Block Size
b) No More Requesting ADCs

c) Time limit exceeded from last ADC read, i.e. Time Window

Once these conditions are met, the ADC state machine is halted and control is transferred to the FERA state machine. Normally the ADC state machine could continue to operate, but in this case the buffer memory implemented in the XILINX FPGA did not have the capability to perform read and write operations simultaneously. To avoid contention in the buffer memory the ADC state machine and the FERA state machine are interlocked so that they operate exclusively. Once the FERA state machine has control, it will request the FERA bus and read out the buffer memory until it is empty. Therefore the block size is determined and the data read out, once the criteria are met and control is transferred to the FERA state machine.

Below is a simplified circuit that generates increasing block size with increasing load. Only two of the above-mentioned criteria are used here, a) a minimum block size of half-full and b) no more requesting ADCs.

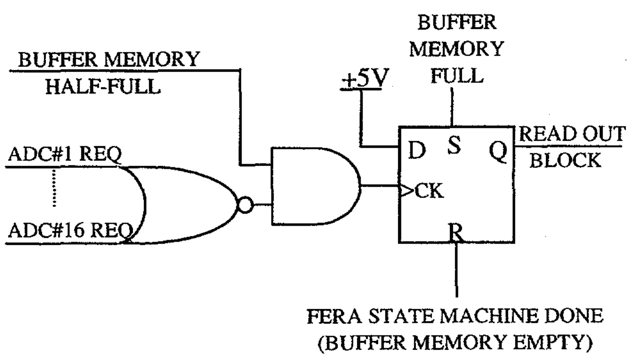

Figure 1: Increasing block size with load.

If the minimum block size criterion is met and there are no more ADCs requesting to be read, the flip-flop is set. This halts the ADC state machine and transfers control to the FERA state machine. Once the FERA state machine is done reading out the buffer memory the stack pointer is empty and clears the flip-flop. This allows the ADC state machine to resume its operation. Under a low rate condition, as the buffer memory fills to the half-full point, there are gaps in time between the requesting ADCs. The probability is large that the block size will be that of a half-full memory. As the rate increases, there is a greater probability that there are additional ADCs requesting to be read. These additional ADCs will be read into the buffer memory before control is transferred to the FERA state machine. Note that there is a forced setting of the flip–flop if the stack pointer is full. This prevents any data loss by forcing a readout if the buffer gets full.

The shortest time to fill the 32 word buffer memory occurs if all 16 ADC daughter boards convert simultaneously twice. The ADC conversion time is 10µs. Therefore, 20µs is the shortest time in which the buffer memory can fill. The FERA state machine requires less then 6µs to acquire the FERA bus and read out a full buffer memory. In addition to the buffer memory, each of the sixteen ADC daughter boards has a single word register that can store the results of a conversion and allow the daughter board to start another conversion. This provides more than enough time for the FERA state machine to control the buffer memory for readout.

The first implementation of the adaptive readout is shown in figure 1. After testing a minimum block size of sixteen words in the buffer memory (half full), the minimum blocksize was changed to one word. If one or more words are in the buffer memory it is not empty. Decoding the pointer of the buffer memory easily generates a "not empty" signal. Using the "not empty" signal insures that no data remains in the buffer memory. When incoming pulses are halted, there are no more ADCs requesting to be read. At this time if one or more words are in the buffer memory it is not empty and control is transferred to the FERA state machine which reads out the remaining data in one block.

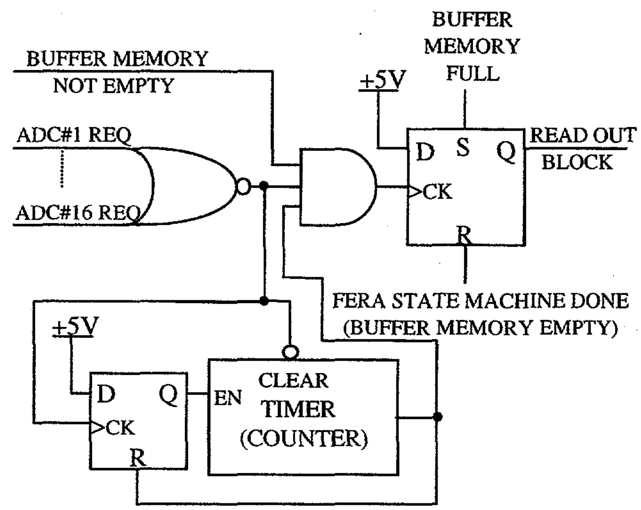

Figure 2: Incorporation of Time Window in determining block size.

To enhance FERA-bus utilization with a mixture of ADCs with both low and high rates we have introduced a time window, criterion c), listed above. After the minimum block size condition is met and the last requesting ADC is read, a timer starts. Only after it times out is control switched from the ADC state machine to the FERA state machine. The time that is currently in use is 2µs. This allows every individual ADC module to optimize the block size. Figure 2 above shows this implementation.

This readout technique is useful if one wants to acquire coincidence data. The time-window can be used as the "slow coincidence time window" in a fast slow coincidence system. The minimum block size defines then the required minimum number of ADCs in each module, which have to contribute to the coincidence event.

IV. Results

To demonstrate the inefficiency of using small block sizes, the 16 Channel CAMAC ADC module was run with a fixed block read out depth of two words. All sixteen ADCs in a single CAMAC module were fed in parallel from a test pulser. An ORTEC model HM413 Histogramming Memory was used for the data acquisition and the FERA request line was observed [4]. This is shown in the upper waveform of figure 3. As can be seen, the module has to acquire the FERA bus eight times. It takes 12µs to read out all sixteen words.

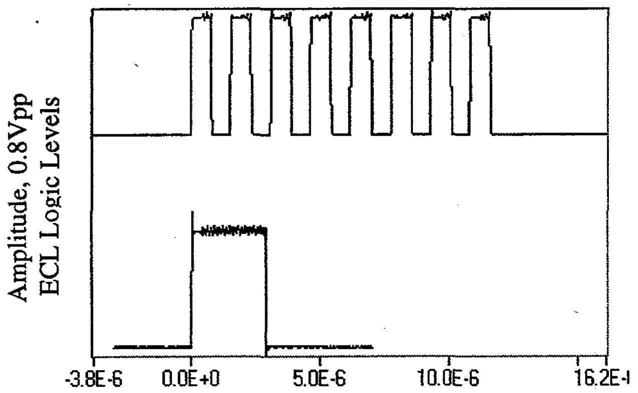

Figure 3: Comparison of FERA request signals using a fixed two word block size read out, upper wave form; and with the adaptive block size read out, lower wave form.

Feeding the same CAMAC module in the same way, but using the adaptive readout, produced the lower waveform of figure 3. It now only takes 2.95µs.

The extra time in the first read out is caused by the fact that the CAMAC module has to capture the FERA bus and write out a header word eight times instead of once. The time it takes to do this is as follows:

- 200ns for the "REO" signal to become available from the HM413 histogramming memory [4].
- 150ns for the 16 Channel CAMAC ADC Module to acquire the FERA bus.
- 150ns per header, i.e. another three machine cycles, for the ADC Module to put out the header word.
- 50ns for the "REO" signal from the HM413 to get synchronized to the 20 MHz system clock in the 16 Channel CAMAC ADC Module.

The total time for the above process is 550ns. After this the FERA state machine writes out each word in the buffer memory, taking three machine cycles per word, i.e. 150ns per word. The total request time for the ADC module with the adaptive readout is Treq = 550ns + N x 150ns, where N is the number of words to be read out.

Doing seven extra FERA bus captures and writing a header word every time, takes an extra 7 x 550ns = 3.85µs. Note that in Figure 3 the extra time used in the upper waveform is the time that the request line is high. While it takes 12µs to read out a block of sixteen words, the total requesting time is 8 x (550ns + 2 x 150ns) = 6.8µs for the upper waveform compared to 2.95µs for the lower.

Figure 4 demonstrates another example of the adaptive readout. Again, the FERA request signal is shown. It is produced with a test pulser feeding the ADC channels in parallel. The upper trace is a read out of eight words; the lower trace is a readout of sixteen words. Note that the request line becomes active once to read out all words from the buffer.

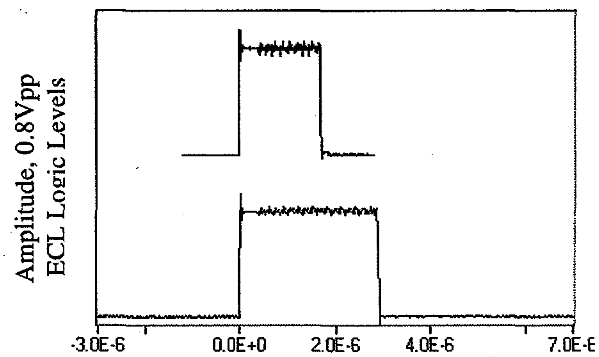

Figure 4: FERA request signal showing the variable block size read out when the ADC module is stimulated by eight ADC channels simultaneously, upper wave form, and by stimulating sixteen ADC channels signals simultaneously, lower wave form.

When a second ADC module is added to the FERA bus and high rates have to be processed, the block size increases further. This is due to the ADC module taking longer to acquire the FERA bus, as the bus is now being shared by another ADC module. When the ADC module does get the bus, it has a larger number of ADCs to read out. With the variable block size readout, the block size increases and thus makes the bus utilization more efficient.

V. SUMMARY

All the logic, including the state machines, buffer memory, CAMAC interface, and housekeeping, is implemented in a XILINX XC4008 Field Programmable Gate Array (FPGA). Currently the limits that control the minimum block size and the time window are changed by reprogramming the XILINX FPGA. Once the limits are set, the block size becomes dynamic, changing according to the set values. Figure 5 shows the flow diagram for determining block size.

Utilization of the FPGA is currently at 60%. Therefore resources are still available in the FPGA to implement additional functions. In the future, the FPGA can be reprogrammed to read the data through the CAMAC data way and to set the limits via the CAMAC-bus and thus allow the user to change them for individual experiments. This can be useful for applications where the experimenter wants to optimize the readout. The user can match the readout to the number of modules on the data bus and to the structure of the data.

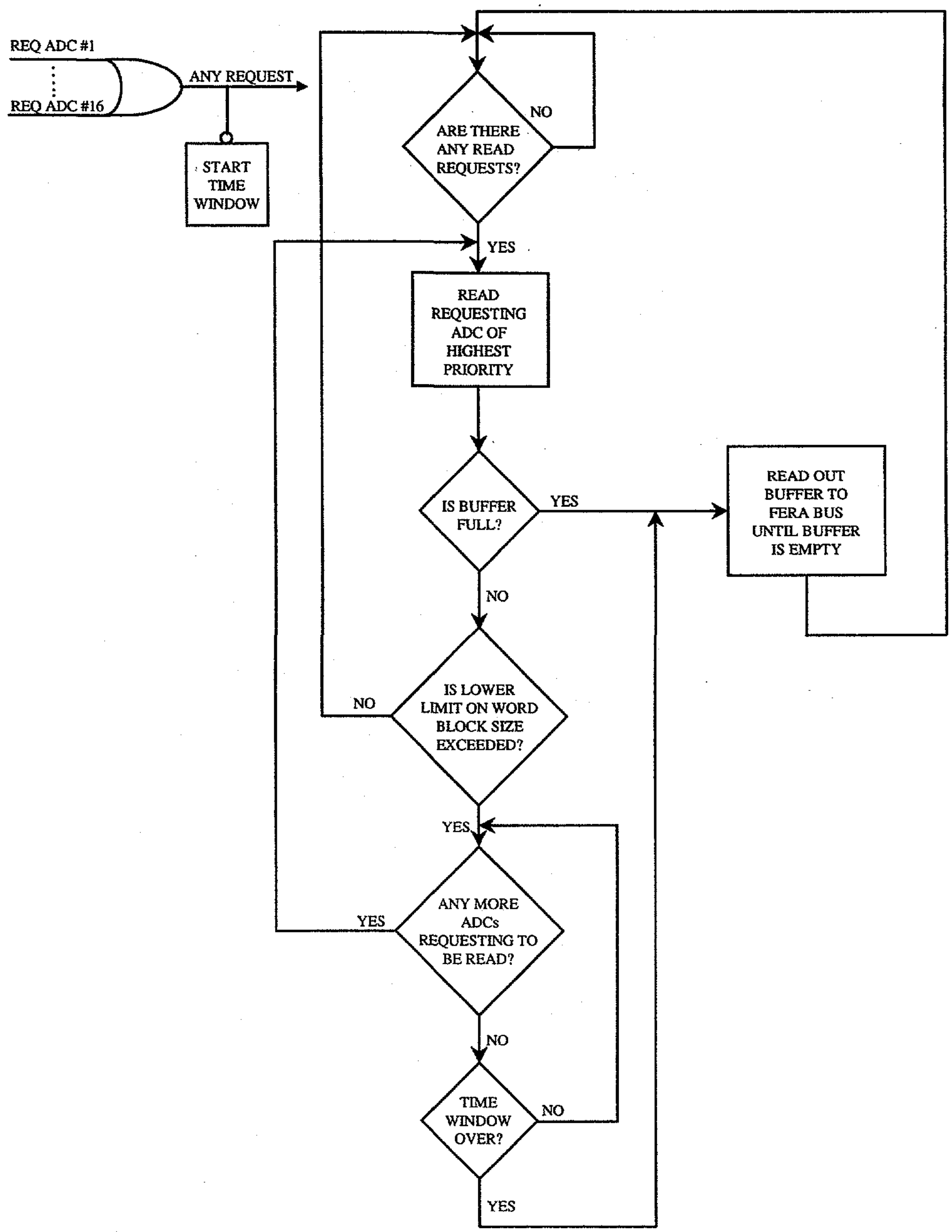

Figure 5: Flow diagram for block size determination

In conclusion, we have designed a flexible readout technique that is easy to implement with FPGAs and can be useful for many other applications.

Reference to a company or product name does not imply approval or recommendation of the product by the University of California or the U.S. Department of Energy to the exclusion of others that might be suitable.

VI. References

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