

# PARTICLE DEFECT REDUCTION IN THE ENDURA TITANIUM NITRIDE PVD SPUTTER SYSTEM

**Mark D. Louis**  
Intel Corporation  
Austin, TX

**Diane Peebles**  
Sandia National Labs  
Albuquerque, NM

**Tony Ohlhausen**  
Sandia National Labs  
Albuquerque, NM

**Roger Spencer**  
Intel Corporation  
Hudson, MA

**Hal Whitehair**  
Intel Corporation  
Hudson, MA

**RECEIVED**  
JUL 13 1999  
**OSTI**

## Biography:

Mark Louis is a Project Manager in Fab Equipment Defect Reduction for Intel Corporation. He is currently an Intel assignee at SEMATECH, a consortium of semiconductor manufacturers located in Austin, Texas. While at SEMATECH, he developed the project plan and led a cross functional team to reduce titanium nitride defects on an Applied Materials Endura physical vapor deposition (PVD) system. Louis received a B.Sc. degree in Electrical Engineering from the University of Texas at Arlington and a Masters in Business Management from the University of Houston. Prior to joining Intel in 1996, he served in the U.S. Air Force as an Engineering Program Manager.

Diane Peebles is a Principal Member of Technical Staff at Sandia National Labs in Albuquerque, New Mexico. She was the primary project leader at Sandia Labs. Peebles received B.Sc degrees in Chemistry and Physics from New Mexico State University. She also completed a Ph.D. in Physical Chemistry from the University of Texas at Austin. Since completing her doctoral studies in 1983, Peebles has worked at Sandia Labs. She has specialized in the field of interfacial materials science including areas such as thin film deposition and adhesion, surface wear and tribology, solid state lubricants, interfacial cleaning and analysis, and contact resistance issues.

Tony Ohlhausen is a Principal Technologist at Sandia National Labs in Albuquerque, New Mexico. He has been at Sandia Labs since 1990. Tony designed the shield temperature measurement experiments and associated defect reduction measures. Ohlhausen received a B.Sc. in Chemistry at Abilene Christian University. He has been involved with ultra-high vacuum surface analysis and related techniques for over 10 years.

Roger Spencer is a Senior Defect Reduction Engineer at Intel Fab 17 in Hudson, Massachusetts. He has spent over nine years in process engineering and has spent the past four years working in defect reduction and yield enhancement. Spencer was responsible for leading the team at the Intel Fab 17 site. He graduated with a B.Sc. degree in Electrical Engineering/Materials Science from Cornell University at Ithaca, New York. Roger also has a Masters degree in Business Administration from Babson College in Wellesley, Massachusetts.

Hal Whitehair is an Equipment Engineer at the Intel Fab 17 in Hudson, Mass. He directed the experiments on the Endura in Fab 17, and provided engineering analysis of the results. Whitehair has 17 years experience in the semiconductor industry. He attended Devry Institute of Technology and graduated with a technical degree in electronics.

## **DISCLAIMER**

**This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency Thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.**

## **DISCLAIMER**

**Portions of this document may be illegible in electronic image products. Images are produced from the best available original document.**

## Abstract:

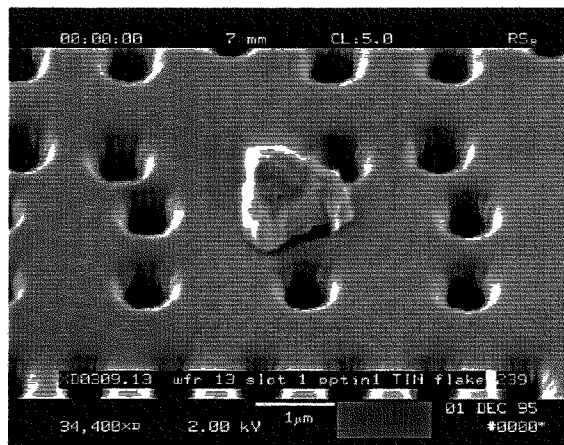
Particles are inevitably generated in physical vapor deposition (PVD) systems due to the delamination of deposited films on various process chamber parts and shielding. Non-collimated (blanket) and collimated PVD Titanium Nitride (TiN) deposition processes are used for metal ARC (anti-reflective coating) and underlayers, and for the “contact liner” deposition steps (TiN adhesion layers before plug formation).

Probe yield analysis and SRAM bit failure analysis, using conventional failure analysis, have shown that particles at these process steps can have a significant impact on wafer yields. In many typical semiconductor wafer fabs, particles generated by TiN film deposition rank consistently at or near the top of the defect pareto.

This paper summarizes the results of defect reduction experiments conducted on an Applied Materials Endura Physical Vapor Deposition (PVD) system and various off-line experiments examining film and adhesion characteristics. It includes the results of film adhesion and shield temperature control experiments aimed at reducing defect levels. Key findings, particle reduction results, and recommended defect reduction measures are presented. The reduction in particles not only can improve yields, but also result in substantial cost savings through the extension of chamber kit end-of-life (EOL).

## Data:

Titanium Nitride (TiN) PVD systems have historically been plagued with particle problems due largely to the film stress and the adhesion capability of the film to chamber parts/shielding. The stress, if high enough, can exceed the elastic limit of the film and cause it to break up or spall. This leads to delamination from process chamber parts and shielding, resulting in particle defects on the wafer. Figure 1 shows a scanning electron microscope (SEM) micrograph of a typical TiN particle which can either block plug formation (causing a contact electrical open), or result in the shorting of lines at the subsequent metal layer.



**Figure 1.** *TiN particle blocking a contact and thus the subsequent plug formation*

The total stress of a film can be described with the following equation <sup>1</sup>:

$$\sigma = \sigma_{external} + \sigma_{intrinsic} + \sigma_{thermal}$$

**Equation 1.** *Total film stress*

where the external film stress is due to some external force (not important for this paper). The intrinsic stress is due to lattice mismatch between the atoms/molecules of the film and substrate. The thermal stress arises due to differences in thermal expansion between the film and substrate. If the thermal expansion coefficients of the film and chamber parts differ, then the normal temperature cycles that occur during wafer processing can lead to additional thermal stress leading to deformation or delamination. This delamination leads to greater particle generation.

Adhesion is also important for maintaining a stable film that does not delaminate and cause particles. Various factors can contribute to the adhesion properties of a film substrate combination<sup>2</sup>. PVD system users typically apply a variety of techniques to improve the adhesion properties of films on the “kit” components (chamber parts and shielding). These techniques include:

1. Coatings: Chamber parts and shielding are pre-coated with films to improve the adhesion and stress properties of the films being deposited during wafer processing. Aluminum is a typical coating used on a stainless steel part.
2. Surface roughness: Chamber parts are roughened by bead blasting in an effort to improve the adhesion of the films during wafer processing.
3. Other techniques to prolong chamber kit life such as "pasting," where films are intentionally deposited on chamber parts and shielding in between wafer runs. The "pasting" is done to encapsulate particles being produced from delamination of the existing films, and to reduce the total accumulated intrinsic stress in the coatings deposited on the kit surfaces.

This paper describes the results of a project that began in 1997 as part of SEMATECH's Defect Reduction in Leading Edge Interconnect Equipment Project. It also highlights some of the key findings and experiments performed which produced the most useful results (i.e., produced the most particle reduction). The experiments included:

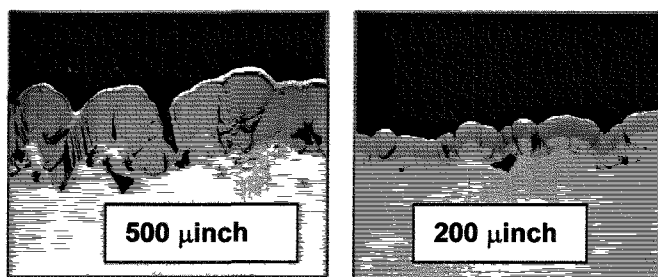
- 1) Microscopic analysis of process kits to examine possible sources of contamination resulting from imperfections in the shield and chamber parts.
- 2) Shield surface roughness and adhesion experiments to examine the impact of changing various parameters of shield cleaning and preparation methods.
- 3) Shield temperature experiments to study shield temperature cycles on particle generation (i.e. minimize the thermal expansion cycles and, thus, the particle generation).

#### Microscopic Analysis of Process Kits:

Microscopic analysis of Endura process kit shields and wafer defects obtained from SEMATECH member companies was performed in an effort to find root cause sources for particle generation. Shields with "good" and "bad" particle defect generation histories were examined by optical

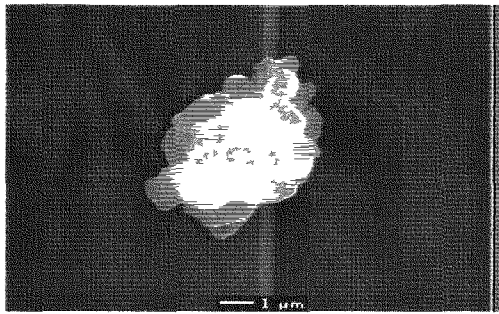
microscope, SEM, and atomic microprobe. Similar studies were completed for particles on wafers processed with these same sets of shields.

Detailed analysis of shield cross-sections showed the primary difference between "good" and "bad" shields to be the degree of surface roughness. In every case, shields with high particle generation histories showed significantly higher surface roughness values than those with low particle generation histories. High surface roughness levels were found to be in the 300-500 micro-inch range, while "good" shields tended to be less rough (see Figure 2). Major changes in surface curvature induce the formation of fracture zones within the deposited coatings on the shields. High surface roughness values induce serious fracture of the coatings, with a resulting columnar growth mode and extensive formation of voids. The combination of this columnar growth mode and coating fracture is believed to play a role in particle generation. During wafer processing the shields are thermally cycled, and these fracture sites are believed to be produced from the resulting mechanical fatigue.



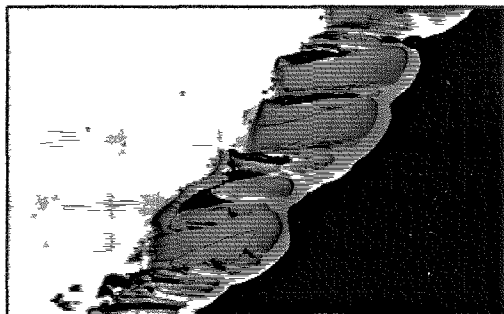
**Figure 2. High and Moderate Surface Roughness**

Rougher surfaces also tend to retain more of the grit blasting material that is used in process kit recycling, cleaning, and surface roughening procedures. Since film coatings do not adhere well to the grit media and the sharp corners of small grit media induce fracture of the deposited films, embedded grit media has also been identified as a significant source for particle generation. This finding is also supported by identification of grit media particles found on wafers processed on the Endura (see Figure 3).



**Figure 3.** *Wafer Defect Containing SiC Grit Blast Particle*

In addition, the deposited coatings have a preference to grow on flat horizontal surfaces, such as the wafer. Unavoidably, vertical surfaces are also located within the process chamber. These vertical surfaces often exhibit an abnormal film growth characterized by small “feathery” outgrowths, which are believed to be another source for particle generation (see Figure 4).

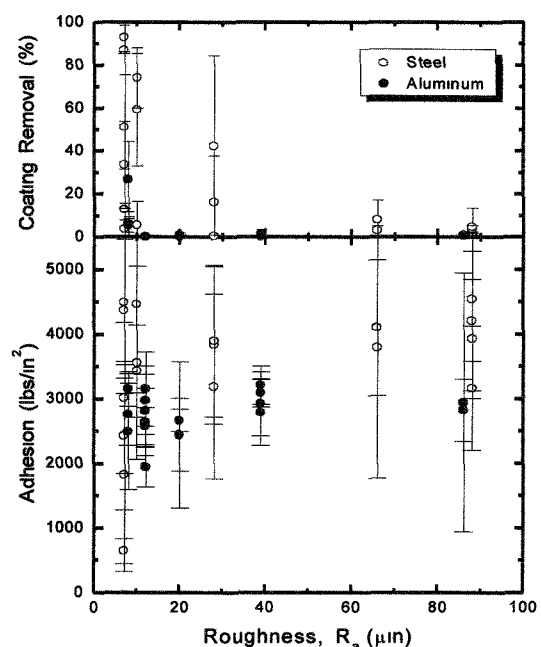


**Figure 4.** *Feathery Outgrowths on Vertical Surfaces*

To reduce particle defect generation, surface roughness of process kit shields must be controlled to a moderate level. Stainless steel shields are better than aluminum in this regard since the harder surface provided by stainless steel does not roughen to the same degree under identical blasting conditions. Reducing embedded grit media in the shields must also be accomplished to reduce particle defects. Again, stainless steel shields are preferred over aluminum because the harder stainless steel does not retain as much embedded grit media.

## Adhesion & Roughness Experiments:

Film adhesion was evaluated for samples (called coupons) of stainless steel and aluminum as a function of substrate preparation and film processing parameters. For smooth samples (not roughened or coated), acoustic emission scratch testing was used to evaluate the film adhesion to the substrate. Rougher samples were evaluated by standard tensile pull testing. This test is done by determining the tensile load required to pull a standardized area of film from the substrate. The adhesion testing results as a function of surface



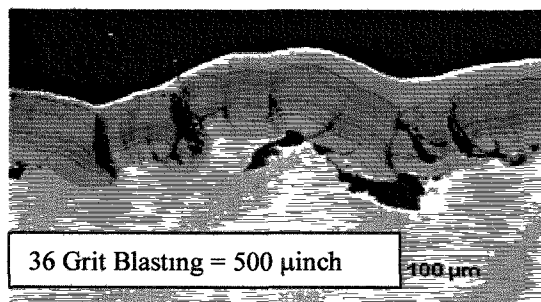
roughness are shown in Graph 1.

**Graph 1.** *Adhesion as a Function of Surface Roughness*

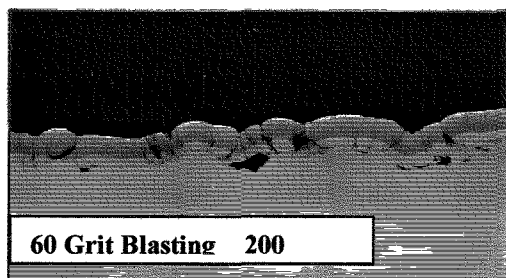
Note that only pull testing results were obtained for the rougher surfaces since scratch testing does not perform well on rough surfaces. As surface roughness is increased, only a slight trend, if any, is seen to higher failure loads. However, there is a rapid decrease in the tendency to spall as the surface roughness is increased.

Since adhesion appears to be a weak function of surface roughness throughout this range, a lower limit for acceptable surface roughness was set at  $R_a = 50$  micro-inches. This is above the roughness

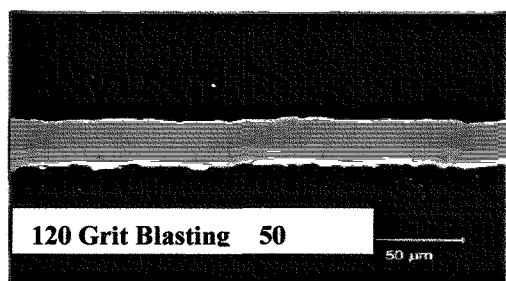
at which the film tended to spall or delaminate from the substrate. The upper bound for acceptable surface roughness was determined by examination of micrographs of coatings on substrates of various surface roughness values. In this case, the upper limit was set at a value of  $R_a = 200$  micro-inches above which fracture of the coatings first began to appear as a result of extreme topography changes of the substrate. The variation of film topography with surface finish and grit media particle size is illustrated in Figures 5a, 5b, and 5c.



**Figure 5a.** Film topography, 500micro-inch roughness



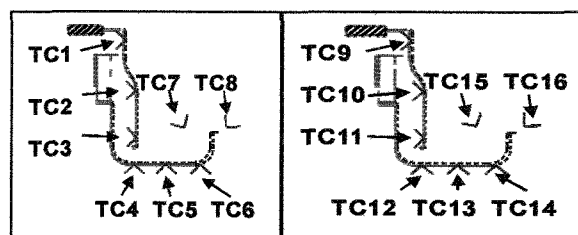
**Figure 5b.** Film topography, 200 micro-inch roughness



**Figure 5c.** Film topography, 50 micro-inch roughness

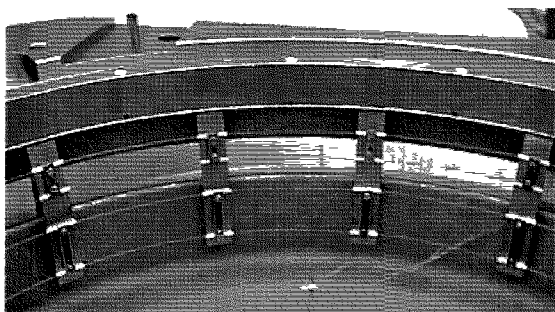
## Shield Temperature Experiments:

Thermal cycling plays a key role in film delamination and subsequent particle generation. Thermal cycling is common in PVD chambers because of the changes in equipment status from idle to process conditions. These changes occur throughout the life of process shield kits during normal production operation. In-situ thermocouple sensor test results, performed during normal Ti/TiN deposition in a G12 (standard TiN) Durasource chamber, showed large differences in temperature across the surface of the shield kit. Temperatures of the shield surfaces were measured at sixteen locations by resistively welding thermocouple junctions to the shields (see Figure 6).



**Figure 6.** Thermocouple (TC) layout

Thermocouple junctions were resistively welded to the outside of the shields at two cross-sectional locations. Each location was 90 degrees apart around the shield circumference. The thermocouple wiring was routed to a computer data acquisition system where the temperature measurements were recorded at a rate of one sample per second. To provide active temperature control, a supplemental heater system was designed and built by Sandia National Laboratories. This system consisted of a temperature controller used with a power supply. Four heater filaments of 0.25-mm diameter tungsten wire were strung in parallel horizontally between the upper and lower shield (see Figure 7).



**Figure 7.** Heater filaments connected to the shield

The top two wires were closely spaced near the top of the shield to concentrate heat at that location, where heat is drawn to the chamber walls. The lower heater wires heated both upper and lower portions of the shield simultaneously. One temperature controller was connected to the top two filaments, while an additional controller was connected to the bottom two, which provided independent control of the two sets of filaments. Each controller required thermocouple feedback for active temperature control. Nine experiments were performed at different pedestal temperatures and bakeout lamp power with and without supplemental heating (see Table 1).

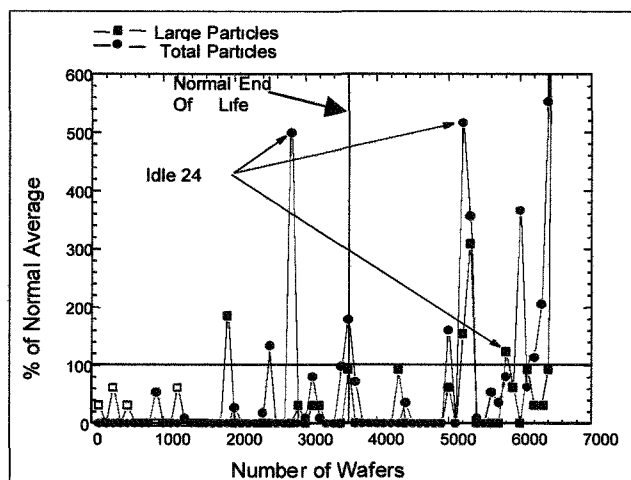
Experiment Number	Pedestal Temp	Heater Setpoint	% Power @ Idle
1	High	Off	Off
2	Medium	Off	Off
3	Off	Off	Off
4	Off	Off	60
5	Off	High	Off
6	Off	High	50
7	Off	Medium	Off
8	High	High	Off
9	Medium	High	Off

**Table 1.** Heating Experiments

Maximum temperatures usually occurred during full wafer processing conditions. The largest temperature variations (130-200°C) occur when no heating is used within the system and the shields reach room temperature during idle times. When the pedestal temperature is controlled to a

higher temperature, temperature differences on the shield of up to 160°C are seen. Some improvement was noted when the bake-out lamps are controlled to 60% power during idle. Lower shield temperature differences from idle to process was only 10-20°C, but the upper shield still had swings up to 130°C. The best results were obtained when the supplemental heater system was used. Temperature variations were reduced to only 20-70°C across the entire shield set.

Given these results, another experiment was performed simulating product runs throughout the entire kit life. Tests were performed with the pedestal set at high temperature, the supplemental heater enabled, and no bake-out lamps. Recipes were modified so that one wafer simulated five, with normal idle times entered into the recipe to simulate wafer moves in and out of the chamber. Particle tests were performed every 100 simulated wafers. The results are shown in Graph 2. Due to the ultra low particles seen during the experiment, kit life was extended until it appeared the particle levels went out of control. This occurred at nearly 2X normal kit life. Results of this test show that for 100% normal kit life (3,500 wafers), large particles were reduced by 97%, and total particles were reduced by 92%. For the entire length of the experiment (180% normal kit life), large particles were reduced by 73% and total particles by 47%.





## Graph 2. Supplemental heater test results

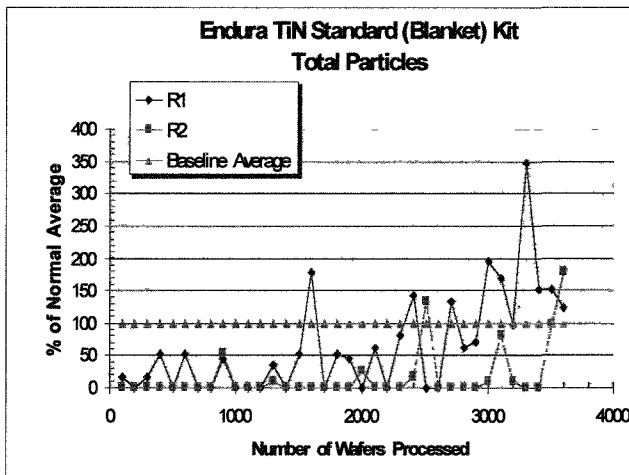
### Combined Roughness, Coating and Heating Experiments:

Defect reduction experiments were performed to look at process kit surface roughness and supplemental heating. Two experiments were performed (Table 2).

Test	Target	Roughness	Coating	Heat
1	G12	R1	None	No
2	G12	R2	None	Yes

**Table 2. Roughness, coating & thermal experiments**

The two experiments involved the G12 (Standard non-collimated TiN) process kit. In experiment #1 with the G12 process kit at the first roughness level, there was a 76% reduction in large particles and a reduction in total particles by 35%. The particle results from experiment #2 at the alternate roughness level yielded even better results. Large particles were reduced by 97%, total particles were reduced by 92% (see Graph 3).



**Graph 3. Total TiN Particles**

### Conclusions:

A two-year project was completed with SEMATECH and Sandia National Labs in an effort to reduce the particle generation on the

Endura 5500 system. The experiments and particle testing described in this paper produced the following key results:

1. Excessive roughness on the Endura process kit surfaces resulted in severe fracture zones within the deposited films. The presence of residual embedded grit blast particles on the shield resulted in fracture zones within the deposited films.
2. Experiments indicated that the recommended surface roughness should be maintained at a moderate level, between 50 and 200 micro-inches for optimal adhesion and minimal coating fracture.
3. The process kit shields were found to have wide temperature swings and gradients during and between film deposition cycles. Supplemental heating has been shown to significantly reduce the temperature swings resulting in a particle reduction of up to 92% when compared to tests run without supplemental heating over the normal kit life.

### References:

1. Maissel and Glang, "Handbook of Thin Film Technology", Section 12, p. 22, 1983 Reissue.
2. Chapman, B.N. "Aspects of Adhesion", Proceedings of 7<sup>th</sup> Conference On Adhesion and Adhesives, 1969, D.J. Alner (ed.).

### Acknowledgments:

The authors would like to acknowledge the many individuals and teams who contributed to the success of this project. Intel Factory Engineers and Technicians: P. Zamora, F. Allen, B. Reisner, S. Creamer, R. Setturland, P. Zanghi, T. Cassidy, D. Dichauzi, C. Benson, R. Grandmaison, L. Swagger, M. Hamel, B. Costa, B. Gay, C. Cross, W. Langlois, A. Sandy, J. Goodrich, J. Hawkins, J. King, C. Lesser, R. McCoy, J. Watson, and T. Thayer. Sandia National Labs Staff: K. Eckelmeyer, A. Kilgo, J. Hunter, A. Carter, P. Hlava, M. Eatough, G. Zender, W. Wallace, W. Buttry, T. Geller, M. Dugger, M. Kelly, R. Bourcier, M. Neilsen, J. Benecke, C. Cooper, E. Sorroche, M. Campo, M. Kelly, E. Chason, and

G. Poulter. Intel Endura/Films Process Engineers:  
J. Maziarz, and E. Bonner. Fab 17 Yield Group:  
M. Seliger and K. Zinke. Applied Materials: J.  
Li, K. Hansen, R. Metevier, G. Mori, and L.  
Sharp. A portion of this work was completed at

Sandia National Laboratories in collaboration with  
SEMATECH under CRADA number CR92/0182,  
supported by the U. S. Department of Energy  
(DOE) under contract number DE-AC04-  
94AL85000.