Design Specifications for Manufacturability of MCM-C Multichip Modules

Kansas City Division

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1.0 General

1.1 Scope

The scope of this document is to establish design guidelines for electronic circuitry packaged as multichip modules of the ceramic substrate variety, although many of these guidelines are applicable to other types of multichip modules. The guidelines begin with prerequisite information which must be developed between customer and designer of the multichip module. The core of the guidelines focuses on the many considerations that must be addressed during the multichip module design. The guidelines conclude with the resulting deliverables from the design which satisfy customer requirements and/or support the multichip module fabrication and testing processes. Finally, considerable supporting information, checklists, and design constraints are captured in specific appendices and used as reference information in the main body text. The final appendix, Appendix G, presents some real examples of multichip module design.

1.2 Definitions

This document may utilize any of the following acronyms, symbols, units and KCD drawing prefixes.

ACRONYMS

ASCII American Standard Code for Information Interchange
ASIC application-specific integrated circuit
BIST built-in self test
CAD computer-aided design
CMOS complementary metal-oxide semiconductor
CVD chemical vapor deposition
DOE U. S. Department of Energy
EDMA Electronic Design and Manufacturing Automation
ES&H Environment, Safety and Health organization
IR infrared
KCD the Kansas City Division
KCP the Kansas City Plant
LCC leadless chip carrier
LTCC low-temperature cofired ceramic
MCM multichip module
MCM-C MCM based on a multilayer ceramic substrate having thick film networks and vias
MCM-D MCM based on a multilayer substrate developed by depositing each dielectric and metal layer
MCM-L MCM based on a multilayer laminated substrate similar to a printed wiring board
MIL-STD Military Standard
MTBF mean time between failures
MWCU Modular Weapon Control Unit
NC numeric control
PGA pin grid array
QC quality control
QCD quality, cost and delivery
SM surface mount or surface mount device (SMD)
SPICE Simulation Program with Integrated Circuit Emphasis
TCE thermal coefficient of expansion
TFN thin film network
TKN thick film network
VHDL Very High Speed Integrated Circuit Hardware Description Language
WR war reserve

SYMBOLS

Ag silver
Al aluminum
AlN aluminum nitride
Al_2O_3 alumina
Au gold
Be beryllium
BeO beryllia
C carbon
Co cobalt
Cu copper
Fe iron
GaAs gallium arsenide
Mo molybdenum
Ni nickel
Pb lead
Si silicon
SiC silicon carbide
Sn tin
W tungsten

UNITS

°C	degrees Celsius (sometimes just **C**)
°F	degrees Fahrenheit (sometimes just **F**)
°K	degrees Kelvin (sometimes just **K**)
F	frequency (measured in **Hz** format)
g	gram
Hz	Hertz (**kHz** = 10^3 Hz; **MHz** = 10^6 Hz; **GHz** = 10^9 Hz)
I	current (measured in amps format)
J	joule
m	meter (**cm** = 10^{-2} m; **mm** = 10^{-3} m; **µm** = 10^{-6} m)
mil	1/1000 of an inch (0.001 inches)
Ω	resistance (measured in ohms format)
Pa	pascal (**MPa** = 10^6 Pa; **GPa** = 10^9 Pa)
ppm	parts per million (also **PPM**)
V	voltage (measured in volts format)
W	wattage (measured in watts format)
Z	impedance

KCD DRAWING PREFIXES

AC	inspection document (substrate and device test)
AY	assembly drawing (MCM and substrate)
CK	schematic drawing (MCM only)
DD	definition data (trace and via master patterns)
(ML)	material list (MCM and assembled pieceparts)
NC	numeric description (via numeric locations)
PS	product specification (MCM inspection and test)

1.3 References

Several MCM test vehicles have recently been designed and produced in small quantities at KCD. Further, there are several individuals who now possess considerable knowledge of the many facets of MCM design and production and may be used as MCM reference sources.

1.3.1 Documents

As a consequence of the MCM test vehicle development work, the following report is available as reference information.

Report No.	Title
KCP-613-5076	High-Speed Digital Project, Waveform Synthesizer (6/93)

As the test vehicle development continues, additional reports will be drafted to document specific areas of MCM development, and all such reports will serve as additional reference information.

1.3.2 Personnel

While many people have participated in the development of the cited MCM test vehicles, the key KCD individuals involved in their design and production have developed expertise in the following areas and may be considered as reference sources.

MCM Design
Substrate and MCM Layout
Substrate Design and Fab
MCM Assembly and Rework
MCM Testing

2.0 PREREQUISITES

The following subsections detail the desired prerequisite information necessary to successfully initiate the MCM design activities as addressed in Section 3. While such information may be available from the customer, it is more likely that a concurrent effort between the MCM design team and the customer will be needed to develop part of this information.

2.1 ELECTRICAL REQUIREMENTS

2.1.1 Functionality

A brief, high-level description of the MCM functional requirements is required. This description should include information on MCM usage in the user system, and it should provide a concise listing, preferably tabular, of the pertinent functional parameters with associated accuracies and precision.

2.1.2 Block Diagram

An MCM block diagram is desirable and should identify by name:

- the major function blocks within the MCM boundary,
- the signal paths between these blocks, and
- the signal paths crossing the MCM boundary.

2.1.3 Draft Schematic

An MCM draft schematic is necessary to expand the block diagram, and, as a minimum, it must define the module electrical architecture. It can be a completed schematic with all components and interconnects fully identified.

2.1.4 Electrical Interface

An electrical interface definition is required to specify the MCM electrical inputs and outputs. Key details to be declared include:

- signal-to-pin or lead assignments;
- interconnect impedances, terminations, loads and bandwidths;
- required stimuli and expected responses; and
- logic levels, sequencing and protocols.

2.2 MECHANICAL REQUIREMENTS

2.2.1 Space and Size

The physical requirements of the MCM must be identified to establish the maximum available footprint size and headroom for the MCM. If applicable, constraints on MCM mass and/or center of gravity must also be identified.

2.2.2 Heat Transfer

Adequate detail of the appropriate user system parameters should be provided so that a detailed MCM thermal analysis can be conducted. As a minimum, such detail should include the available mechanisms and the maximum rate of heat transfer from the MCM to the user system.

2.2.3 Mechanical Interface

The MCM mechanical interface must be specified, including information on MCM mounting method and attachment materials. Specified details should include:

- pin or lead geometry and locations and associated tolerances,
- thermal coefficient of expansion of the MCM attachment surface,
- attachment material composition and process temperatures,
- encapsulation materials, and
- location of thermal pathways.

2.3 ENVIRONMENTAL REQUIREMENTS

2.3.1 Radiation

Radiation environments must be identified, including anticipated radiation types and dose rates. The maximum radiation levels required for MCM survival and continuous operation should also be specified.

2.3.2 Thermal

Thermal environments must be identified since they communicate the anticipated thermal extremes and rates of change for MCM survival and continuous operation.

2.3.3 Hermetic

Hermeticity requirements must be specified for the MCM die cavity and should detail the maximum acceptable gaseous leak rates under specific conditions; i.e., pressure, temperature, humidity, gaseous composition, etc. For example, MIL-STD-883D provides specific details for hermetic sealing and testing as applied to microelectronics.

2.3.4 Atmosphere

The atmospheric conditions under which the MCM will operate must be specified, including humidity levels (condensing and noncondensing) and atmospheric pressure ranges.

2.3.5 Storage and Transportation

The nonoperating environments (storage and transportation events) must be identified for the MCM. These environmental factors should include:

- temperature extremes and cycling,
- humidity levels,
- radiation types and dose rates, and
- shock and vibration duration and spectra.

2.4 TESTING REQUIREMENTS

2.4.1 Electrical

To electrically verify MCM functionality, the electrical testing requirements must be identified for the MCM. Stimuli and expected responses should be listed for each test sequence specified.

2.4.2 Temperature

Operating and nonoperating MCM temperature testing requirements must be specified, including temperature extremes and rates of change.

2.4.3 Burn-in

Burn-in requirements must be identified for the MCM, including temperature, duration, MCM operational status (unpowered, powered or operating), and monitoring requirements.

2.4.4 Shock and Vibration

Shock and random vibration testing requirements must be specified. Shock test details should include shock waveform shape, peak acceleration, duration, axes to which shock is applied, MCM operational status (unpowered, powered or operating), and monitoring requirements. Vibration test details should include vibration spectra, duration, axes to which vibration is applied, MCM operational status (unpowered, powered or operating), and monitoring requirements.

2.4.5 Special

Special test modes, stimuli and/or responses must be identified for the MCM. Customer resources (expertise, facilities or equipment) should be specified which may be used in detailed test plan development, test setup, test execution, and/or troubleshooting.

2.4.6 Data Type, Format and Medium

The data type, format and storage medium for all recorded test data must be identified. Instructions should be provided regarding whether acceptance limits should be recorded with the test data.

2.5 Documentation Requirements

2.5.1 Reports

A listing of reports to be delivered to the customer shall be specified. A brief description of the scope of each report and its delivery time within the program shall also be specified.

2.5.2 Analyses

Documented analyses to be delivered to the customer shall be specified. A brief description of the scope of each analysis and its delivery time within the program shall also be specified.

2.5.3 Drawings

A list of all drawings to be delivered to the customer shall be specified. A brief description of the content of each drawing, the delivery format and medium, and delivery time within the program shall also be specified.

2.6 Other Requirements

In addition to MCM performance and documentation, other customer requirements including cost, quantity, schedule and quality must be defined. Since these items are interrelated and invariably require tradeoffs, the design team can most effectively analyze and communicate such tradeoffs by first understanding the customer's priorities in these areas.

2.6.1 Schedule

A schedule shall be specified indicating the time available for MCM development and production. If applicable, production rates shall also be specified (for example, 10 MCMs per month).

2.6.2 Quantity

The total quantity of fully functional MCMs shall be specified, including the number of prototypes to be produced in development. Also, any required non-functional MCMs must be specified.

2.6.3 Cost

The overall cost of MCM development and the desired production cost per unit shall be specified.

2.6.4 Classification

The level of classification of the MCM shall be specified. If classified, a classification guide shall be provided indicating which aspects of the program are to be protected.

2.6.5 Quality Level

The desired quality level of the assembled MCM shall be specified. This level may range from a desired MTBF to a detailed quality plan.

3.0 Design Considerations

The following subsections encompass the many interrelated considerations which must be addressed during an MCM design: electrical, mechanical, packaging, substrate, manufacturing and testing factors. The MCM design must evolve through concurrent, team effort that iterates among the cited factors until the design is optimized, not only for the desired form and functionality, but also for manufacturability and testability.

3.1 Electrical Design

The electrical design of the MCM must produce the schematic definition inclusive of all component symbols, signal I/O definitions, and signal timing relationships or event sequences. This design cannot be considered complete until some degree of design testing is successfully conducted, such as the use of simulation and analysis tools and/or actually breadboarding the design and testing for correct functionality.

3.1.1 Schematic Definition

The MCM schematic, a diagram of the MCM electrical connectivity of a circuit with components represented by graphical symbols, is the first step in the creation of any MCM definition. After the schematic has been completed and verified, it is available for use by MCM design evaluation tools (e.g., bill of materials, circuit simulations, and netlist generation) and for the MCM package design/layout process. Some MCM designs may require the creation of new schematic symbols.

3.1.1.1 New Schematic Symbols

The EDMA system has a large library of commercial components and their schematic symbols (the schematic graphical representation of the electronic components). However, because many MCMs utilize custom ASICs and new technology components, schematic symbols must be created for these new devices to facilitate schematic capture.

3.1.1.2 Schematic Capture

Schematic capture is the process of entering the electrical schematic into the EDMA system along with pertinent defining notes, special net requirements (e.g., conductor width, length, layer and spacing), TKN resistor information and other electronic parameters. This MCM schematic, once entered and verified, becomes the foundation for subsequent substrate layout and automatic routing activities.

3.1.2 Simulation

Simulation of the MCM design offers the ability to manipulate device parameters and study their effects on module performance. The typical sequence of events leading up to a simulation would include the following items.

- The MCM schematic must be captured within the EDMA system.
- Each MCM component, be it ASIC, logic block, clock, transistor, resistor, etc., must be modeled. In the simpler component cases, SPICE or similar models may be available in existing libraries. For the more complex cases such as digital ASICs, a VHDL behavioral model from the die supplier is almost imperative.
- Once the schematic and compatible component models are available for the EDMA simulation, setup conditions such as stimuli, input event timing, and output monitoring can be specified, and then the simulation can be run.

The ability to conduct circuit simulation is currently in an evolutionary state for the EDMA system.

3.1.3 Analysis

Design of an MCM should invariably include several different analyses which give credibility to the design. As a minimum, these analyses should encompass the following areas:

- MCM functional analysis, particularly if simulation is not possible;
- I/O compatibility with the system application;
- component power dissipation, substrate trace, and I/O current carrying capabilities; and
- quantity, piecepart availability, cost and schedule.

3.1.4 Breadboard

Perhaps one of the most effective ways of verifying a new design is to actually build the "MCM" and test it. Usually, the resulting hardware is created from available components (possibly packaged counterparts rather than die devices) and a substrate (possibly a printed wiring board in place of ceramic). Although the final package related effects on functionality can only be extrapolated at best, a valid functional demonstration of the MCM breadboard hardware goes far in validating the MCM design.

3.2 Packaging Design

MCM-C multichip module substrates can serve as both the interconnecting network and the module package. As such, electrical and mechanical design issues must be considered as detailed in the following subsections.

3.2.1 Electrical Considerations

Once the electrical design has been completed, implementation techniques must be identified that will ensure the required electrical performance. Issues to be resolved include power distribution (voltage, current, grounding), and signal integrity (isolation, controlled impedance interconnects, dielectric effects, propagation delay, MCM I/O launch). The product of this effort should be MCM layout and routing rules, a preliminary layer stackup, dielectric tape selection, and a concept for MCM I/O interconnect to the user system.

3.2.1.1 Voltages

All supplied voltages required for MCM operation shall be identified and named. Power planes may be dedicated to any voltages which are used by many components. To minimize any variation in potential across the MCM, each power plane should be connected to the user system with multiple pins or leads. Voltages requiring special attention should be indicated; e.g., high voltage.

3.2.1.2 Currents

Anticipated currents (average and peak) for each supplied voltage should be identified. Connections and traces (signal, power or ground) expected to carry large currents should be indicated, and the techniques used to accommodate such currents

should be described. Techniques used to accommodate high currents include:

- parallel pins or leads for current splitting;
- wider traces; and
- larger bond wire diameters, ribbons and/or multiple wires (refer to Tables D.6 and D.7).

3.2.1.3 Grounding

One or more dedicated ground planes may be used to provide a low impedance, uniform reference across the MCM. To minimize any variation in ground potential across the MCM, the ground plane should be connected to the user system with multiple pins or leads.

3.2.1.4 Isolation (shielding and guarding)

Signals requiring isolation to minimize undesired energy coupling must be identified. Isolation techniques (such as shielding and guarding) should be evaluated for effectiveness and design complexity. The selected technique must then be incorporated into the layout rules for this class of signals. These rules could include minimum trace separation, routing alternating layers in orthogonal directions, or placing a power or ground plane between routing layers.

3.2.1.5 Controlled-Impedance Interconnects

Controlled-impedance transmission lines are needed to transmit high-speed signals; i.e., signals with transition times less than the signal propagation times between the source and destination. Geometries providing controlled impedance include microstrip, stripline, slotline and coplanar. Factors affecting geometry selection include:

- ceramic dielectric properties,
- cross-talk and isolation requirements,
- desired signal density and the number of available routing layers, and
- accuracy and precision of trace fabrication processes.

Once a transmission line structure has been selected, parameters such as dielectric thickness, dielectric permittivity, trace width, and trace thickness can be specified for 50 Ω characteristic impedance signal connections. Additionally, a parametric sensitivity analysis of the characteristic impedance should be performed with regard to variations in these same parameters to evaluate the impact of material and process variations.

3.2.1.6 Dielectric Properties

Dielectric properties of the substrate material affect controlled-impedance, transmission line design, signal coupling, distributed line capacitance, and other characteristics. Selection of the dielectric material to be used in the MCM substrate should include an examination of these effects. Table A.3 lists several substrate materials and their dielectric properties including relative dielectric constant (or permittivity), loss tangent, and electrical resistivity.

3.2.1.7 Propagation Delay

For synchronous signals, such as digital data buses or clock distribution networks, the propagation delay of each signal must be controlled to avoid undesired timing skew. Matched trace lengths integrated into the layout rules can limit layout-induced skews.

3.2.1.8 Method and Locations of I/O Launch

The electrical interface between the MCM and the user system must be designed to transmit the signal content accurately. Factors which degrade the transmission include coupling from adjacent signals, impedance mismatches, reactive loading, and path resistance. To ensure a quality electrical interface, an analysis should be performed on the launch geometry and interface materials. Factors which can usually be varied to enhance interface integrity include signal pin assignment, pin or lead dimensions, and pin or lead spacing.

In addition to I/O launch by pins or leads, other launch techniques include pigtail cable, SM connector, optical interconnect, etc.

3.2.2 Special Considerations

In addition to the normal electrical operating considerations discussed above, special environmental conditions may impact package design.

3.2.2.1 Radiation

Exposure to radiation can adversely affect MCM performance; therefore, radiation considerations must be included in the MCM design. Various design methods are available to manage the radiation effects, depending on the type of radiation (photons, charged particles, neutrons) and the operating requirement (operate through or allow shutdown during radiation events). These methods include circumvention, shielding, careful layout of metals and dielectrics, component selection, redundant functions, etc. Analysis and customer

requirements will dictate the methods to be implemented.

3.2.2.2 Thermal and Hermetic

The thermal and atmospheric environments the MCM is intended to operate in may affect MCM design. Ambient temperature and the heat sinking capacity of the user system could limit the power dissipation of the MCM and affect MCM reliability. Hermeticity requirements impact cavity sealing options. Other design areas which can potentially degrade MCM hermeticity include thermal vias, substrate material, and lid design.

3.2.2.3 Shock and Vibration

Mechanical shock and vibration requirements will affect the MCM design with regard to maximum acceptable wire bond length, minimum substrate thickness, substrate material selection, mechanical interface design, and encapsulation within the user system. Analysis and/or laboratory testing may be required to validate the MCM design.

3.2.3 Component Definition

A definition is required for each unique component to be used in the MCM design. The component characteristics which are essential for proper MCM design are detailed in the following subsections.

3.2.3.1 Size (L x W x T)

The length, width and thickness dimensions are required for each component.

3.2.3.2 Bond Pad Pitch, Size and Material

Information about bond pad dimensions, pitch and the material composition is required for MCM layout and assembly.

3.2.3.3 Die Bond Pad Layout (vendor map)

A die bond pad layout showing the location of all bond pads with meaningful names is required for MCM layout and assembly. This information could be in the form of a die photograph or a scaled drawing.

3.2.3.4 Die Technology (GaAs, CMOS, etc.)

Knowledge of the die technology is required to establish appropriate assembly, handling and testing processes. Die technology includes semiconductor material (Si or GaAs), logic type (TTL, CMOS, FET, ECL, etc.), and information on die passivation.

3.2.3.5 Backside Metallization and Potential

Knowledge of the semiconductor die backside potential is required so that the die attach pad may be connected to the proper voltage or allowed to float. Also, information regarding the semiconductor die backside metallization is required as it impacts die attach options.

3.2.4 Thermal Analysis

A thermal analysis is always in order for any MCM design. Failure to adequately design for MCM self-heating can result in component drift, reduced MTBF, and catastrophic failure. Several factors must be examined in the thermal analysis. These are addressed in the following subsections.

3.2.4.1 Materials

The materials used in the MCM are critical to its thermal performance. The thermal conductivity of the material affects the temperature differential between the heat generating devices and the surface of the MCM. Also, any TCE mismatches between MCM materials will result in mechanical tension and compression which can cause fatigue, micro-cracking and, if severe enough, component fracture. The material selection process must address these issues. As an aid, Appendix A provides a convenient reference for some key properties of materials used in multichip module applications, including TCE.

3.2.4.2 Semiconductor Devices

From a thermal analysis viewpoint, semiconductor devices are just another MCM material and have the same considerations mentioned previously. In addition, the semiconductor devices will likely represent a heat source. Active devices (transistors, diodes) on the surface of the semiconductor die not only dissipate heat but are also the focus of concern in the thermal analysis. Material properties of silicon and gallium arsenide devices are presented in Table A.5.

Semiconductor MTBF is often directly related to device junction temperature; i.e., shorter MTBFs are associated with higher operating junction temperatures. Thus, a thermal analysis will often strive to achieve a given junction temperature (hence, a device MTBF) by minimizing the thermal impedance between the surface of the die and the outer surface of the MCM.

One option available to the designer is die thinning by the die supplier. Die material (Si or GaAs) may be the source of significant thermal impedance. By thinning the die, the thermal impedance due to the die itself can be reduced. Another alternative is to flip-chip bond the die to the substrate with z-directional electrically conductive epoxy, thereby placing the active surface of the die in close proximity to the substrate. However, this technology is not currently available at KCD.

3.2.4.3 Die Attach Technology

The basic goal of MCM thermal analyses is to minimize the thermal impedance between the semiconductor die surface (where the active, heat-generating junctions are located) and the outer surface of the MCM (where the heat transfer to the environment or to the user system occurs). Die attach techniques dramatically impact this thermal impedance between the semiconductor die and the MCM substrate. Many adhesive materials are available and several are included in Tables A.4 and D.5. Metal attach methods such as solders and eutectics are not currently compatible with cofired substrate technology due to irregular surfaces and incompatible metal systems.

3.2.4.4 Passive Devices

Passive devices may also represent a significant source of heat dissipation within the MCM. In these cases, an acceptable operating device temperature must be determined which in turn dictates the maximum acceptable thermal impedance between the heat dissipating device and the MCM outer surface. As in the case of die attach, component attachment techniques and material selection can be critical to the thermal performance.

3.2.4.5 Substrate Configuration

MCM thermal characteristics are often dominated by the substrate characteristics. Thus, special attention should be paid to the thermal design of the substrate.

One factor impacting substrate thermal performance is the thickness of the substrate beneath the heat-dissipating devices. By placing these devices in cavities, substrate thickness can be reduced locally.

Another option available to the designer is the use of thermal vias. Cofired metals typically have significantly higher thermal conductivity than cofired ceramics. Therefore, by placing dense arrays of large, metal-filled vias beneath hot components, the thermal impedance through the substrate can be significantly reduced. Substrate fabrication capabilities limit the maximum size and packing density of these thermal vias as stipulated in Table C.1.

3.2.4.6 Heat Spreader

To facilitate heat transfer, use of a heat spreader is sometimes beneficial. A heat spreader is a layer of material with a relatively high thermal conductivity which spreads the heat flow laterally and increases the heat transfer surface area. Materials usually considered for heat spreading application include metals (copper and aluminum), metal alloys with TCEs close to those of ceramics (Kovar, Invar and others), ceramics with good thermal properties (aluminum nitride, beryllia, silicon carbide), and synthetic diamond (CVD and polycrystalline). Properties of these materials are listed in Tables A.1, A.2 and A.3. Selection of a heat spreader material must include evaluation of the material's thermal and electrical properties, density, ES&H concerns, and cost.

Current substrate fabrication capabilities require that heat spreaders not be integral parts of the substrate; rather, the heat spreader must be added in a subsequent MCM assembly process. Heat spreaders can be used both internal to the MCM (as a component carrier) and external to the MCM thereby enhancing heat transfer to the user system or the environment. In either case, attachment techniques (solder, thermoplastic adhesive, epoxy) will impact overall thermal transfer characteristics and must be included in the analysis.

3.2.5 Substrate Definition

This section discusses the information that must be gathered and defined to design an LTCC substrate. Fabrication considerations and constraints are addressed because of equipment, tooling and/or process limitations. If additional information is required or the application presents unique fabrication considerations, the substrate engineer should be contacted for assistance.

Throughout the LTCC substrate design, all design dimensions are post-fired (final) dimensions. Dimensions that apply to the pre-fired green tape are simply scaled up to account for the tape shrinkage that will occur during the firing process (about 13% in length and width and about 15% in thickness).

3.2.5.1 Thickness and Contour

The minimum post-fired thickness for an MCM-C substrate is set at 40 mils at its thinnest point (typically in the cavity area). The minimum thickness for an MCM-C substrate outside the

cavity area is set at 60 mils. These thicknesses are established to ensure that the LTCC substrate will have a strength similar to a 25-mil-thick alumina substrate (see Table D.2.). The tightest dimensional tolerance on the contour of a substrate can be held if the substrate is rectangular (see Table C.1). Arcs, keyways and irregular shapes are possible but not with tight tolerances because they are cut before firing. The largest post-fired substrate possible is a 2.25-inch square or 2.25 inches on the minor side of the rectangle as restricted by the current work holder and automated wire bonding tool. Other substrate sizes may be possible after consultation with the substrate and assembly engineers.

3.2.5.2 Layer Allocation

Layer allocation is a two-step process: first, establishing the number of layers for the designed thickness, and second, assigning electrical functionality to each layer. The substrate thickness will be based on the mechanical requirements of the substrate and its physical features including those layers which form the die cavity. The electrical functionality of the substrate layers will be assigned based on the number of ground and/or power planes required and the electrical interconnect density of the signal layers. Finally, if required, layer assignment must include any stripline or microstrip traces with appropriate layer separation from related ground or power planes (see Figure C.1).

3.2.5.3 Cavity Definition

The MCM design will typically have a hermetically sealable cavity area where bare die components can be attached and bonded to the substrate. The maximum cavity depth is 150 mils, inclusive of seal ring height, as restricted by the substrate test system, and it is measured from the lowest wire bond pad (substrate or die) to the top of the seal ring. Table D.2 provides design guidelines for the die bond pad and wire bond pad features for bare die components. Table D.5 provides general processing information about the different die attach materials, and Tables D.6 and D.7 provide information about different bond wire and ribbon materials and assembly processes. After the final cavity size has been determined, Figure C.2 presents a method for defining the seal ring, seal ring braze pad, and lid dimensions.

3.2.5.4 Power and Ground Planes

Usually, voltages and grounds are distributed to the MCM components by metal planes designed into specified substrate layers, one plane for each voltage and ground. Each plane is typically composed of metal printed on the specified layer in a cross-hatched pattern. The cross-hatching enhances lamination adhesion to the adjacent tape layer. Table C.1 provides guidelines for defining such planes, including the material pattern and clearance requirements for vias.

3.2.5.5 Signal Layers

An adequate number of substrate signal layers must be defined so that all of the MCM interconnections can be successfully routed. Signal layers are normally defined as a pair of two conductor layers where one layer is used to route traces primarily in an X direction while the traces on the other layer are routed primarily in the Y direction. This orthogonal routing technique tends to reduce coupling between layers and retain planar external surfaces.

3.2.5.6 Traces and Vias

The recommended width for an internal trace is 8.7 mils (10 mils, pre-fired). Spacing between traces should be 8.7 mils (10 mils, pre-fired). Wider traces are possible for unique signal properties. Traces of lesser widths are possible, but substrate yield could be reduced. The recommended diameter for an internal electrical via is 8.7 mils (10 mils, pre-fired). Larger via diameters are possible, but the ratio of via diameter to tape thickness becomes critical (the ink may not remain in the via until firing). Smaller via diameters are possible, but forcing the ink into the smaller via becomes more difficult and substrate yield would be reduced. Each electrical via must have a cover pad that is twice the via's diameter. The minimum spacing between electrical via centers should be three times their diameter. Vias should be staggered every two layers with a minimum stagger of twice the via diameter. Thermal vias are treated separately from electrical vias. Their recommended diameter is 17.4 mils (20 mils, pre-fired). The minimum spacing between thermal via centers should be twice the via diameter. The thermal vias do not require cover pads.

These recommendations are tabulated in Table C.1 along with more detailed recommendations for traces and vias. Also, a summary of typical paste properties is presented in Table C.2.

3.2.5.7 Component Placement

Component placement on the substrate should follow the guidelines listed in Table D.2 for die and Table D.3 for surface mount components. In general, components should be placed to provide

adequate room for attachment and connection. Components should be placed and oriented for the shortest trace interconnect lengths. The interconnect length of high-speed signal traces requires particular attention.

3.2.5.8 Bond Pads and Wires

After each die has been attached to the substrate, it must be electrically connected to the substrate. This interconnect is accomplished with wires bonded between appropriate die and substrate bond pads. It is recommended that the substrate bond pads be at least 10 mils square. The spacing (gap) between bond pads should also be 10 mils. In general, the wire length from die to substrate should not be over 100 mils. Additional recommendations in this area are listed in Table D.2. Details on the physical limitations of the wire and ribbon bonding processes, rework procedures, and current carrying capabilities are listed in Tables D.6 and D.7.

3.2.5.9 Test Pads

Test pads may be included in any MCM design. Some of these pads (test points) can aid in pre-lid and post-lid MCM electrical testing. Other test points can be utilized to verify substrate integrity (i.e., nonfunctional continuity loops). Such pads must be considered in the very early phases of any design and directly reflect the substrate and module test plans. Typical test pads are 30-mil-square pads.

3.2.5.10 Printed Resistors

The EDMA system has the capability of designing thick film resistors based on specified design factors. These factors include geometry, resistor inks, aspect ratio, power, voltage and other parameters. The basic resistor material parameters are defined in Table C.1, and resistor pad dimensions are defined in Table D.3. The remaining parameters are based on the specific resistor application.

There are three basic considerations associated with thick film resistor designs:

- resistance value,
- required power dissipation, and
- allowable resistance tolerance.

The resistor value is defined by its length-to-width ratio; the power dissipation is a function of the resistor area; and the resistor tolerance is a function of the manufacturing processes.

The resistor value is defined by the resistor material (sheet resistance) and the length-to-width ratio of the resistor; neither the width nor the length of the printed resistor should be less than 50 mils. This resistance value may be calculated as

$$\text{Resistance} = \frac{\text{sheet resistance} \times \text{length}}{\text{width}} .$$

For a given power dissipation, an equation for calculating the minimum resistor width is as follows:

$$W = \sqrt{\frac{P \cdot P_s}{D \cdot R}} ,$$

where

- P = maximum power dissipation in resistor (mW);
- P_s = sheet resistance of resistor material (ohms/sq.);
- D = power density rating of system (W/sq.in.);
- R = resistor value (k ohms); and
- W = minimum resistor width (mils).

Thick film resistors can typically be printed to within ±35% of nominal value. However, thick film resistors are typically trimmed closer to nominal value with a tolerance listed in Table C.1. The trimming operation can only provide an increase in resistance; therefore, the resistor should be designed to 70% of the final value.

All resistors that are to be trimmed or have their values measured must have connected probe pads. However, since the resistor trimming operation generally occurs before components are attached, probe areas may naturally exist without resorting to the addition of special probe pads (for example, the conductor pad for a capacitor may be schematically connected to one side of the resistor; thus, no special probe pad will be required on the substrate).

3.2.5.11 Surface Mount Components

These components are usually LCCs, chip resistors, or chip capacitors. Guidance on their layout, attachment and rework is provided in Tables D.3 and D.9. Interconnect traces for these components are typically located on internal layers to eliminate solder dams. The surface mount pads used for attaching these components must be a double printing of platinum/gold. This double print is required to minimize the tin/lead solder from leaching the gold out of the vias and causing opens.

3.2.5.12 Pins and Leads

Pins or leads are typically used for the electrical interface and mechanical support between the

MCM and the user system. The dimensions of these parts must be defined. For example, a pin definition should include the pin diameter and length and the pin head diameter and thickness. Likewise, a lead definition must include lead length and thickness where the initial length may be associated with lead frame dimensions and the final length would then be the trimmed length following lead frame-to-substrate assembly. Pins and leads typically have a base material of Kovar with a plating specification of 75 microinches minimum Au over 50 microinches minimum of electrolytically plated Ni.

3.2.5.13 Soldering Considerations

There are many options for soldering components to the substrate. The primary consideration is to choose a solder system compatible with the component termination material. A common solder used is 63/37 tin/lead. It can be applied by screen printing, preforms or automated dispensing. Component reflow soldering attachment can be accomplished by using a convection or IR belt furnace or a vapor phase chamber. Tin/lead and eutectic solder properties are presented in Table A.6, and a description of the solder and rework processes is contained in Table D.9.

3.2.5.14 Brazing Considerations

Brazing (high-temperature soldering) is possible with LTCC MCMs. Typically, it is used to attach pins or leads and a seal ring. The ability to braze a seal ring to the substrate allows a hermetic die cavity to be formed with the addition of a lid. Several constraints and recommendations on the design of a seal ring, its braze pad, and the companion lid are illustrated in Figure C.2. A braze pad must be printed on the substrate before the seal ring is attached. The braze pad is composed of two separate ink layers: an adhesion layer and a barrier layer, printed sequentially as listed. The adhesion layer must be printed 5 mils smaller on a side than the barrier layer. The barrier layer is between the adhesion layer and the braze solder. The braze solder material can be based on a gold/tin system. If it is printed on, it must be printed 5 mils less on a side than the barrier layer printing. The manufacturing process for attaching the seal ring is listed in Table D.4 and is typically a belt furnace operation using graphite fixturing.

Pins or leads can also be attached using the process described above. The printed braze solder can be eliminated if the pins or leads are purchased with a solder preform already attached or if a solid preform is used. The manufacturing process used for attaching the pins or leads is also described in Table D.4.

3.2.5.15 Hermetic Seal

With a seal ring brazed to the LTCC substrate around the die cavity, the cavity can then be sealed by brazing a lid to the ring after die assembly. Recommendations for specifying the seal ring and lid are contained in Figure C.2. The process of attaching the lid to the seal ring is described in Table D.8 along with the methods used to test for hermeticity. It should be noted that testing per MIL-STD 883 requires different preconditioning parameters depending on the cavity size. The particular parameters requiring consideration for a specific size can be found in the MIL-STD or by consulting the assembly engineer.

3.2.5.16 Substrate and MCM Marking Requirements

To provide traceability, the MCM and its substrate can both be marked for identification (part and serial numbers as a minimum) by specifying location, size, format and method of the marking characters. The marking area must be proportional to the amount of encoded information and the application method. The final identifying characters can be marked on the lid or on a section of exposed substrate. In-process identification can be placed under surface mount components. In all cases, adequate room must be allocated in the design.

3.2.5.17 Additional Printing Considerations

Typically, dielectric inks are used to print the "pin one" indicators and to produce a guide line for the diamond sawing operation. Other inks can be used to print these two features; however, this type of ink is the least expensive of the thick film inks.

3.2.6 Component Summary

With the aid of Appendix F (Tables F.2 and F.3), a component summary should be prepared to facilitate MCM layout and aid MCM assembly, test and troubleshooting. This summary includes relevant component characteristics discussed in section 3.2.3 such as dimensions, metallization, power dissipation, die bond pad layout, etc. Frequently the vendor data sheet summary will satisfy this requirement. For die components, a photograph of the die with bond pads numbered and/or labeled consistent with the schematic and layout is also recommended. This information

should be collected into a single package for ease of use and reference.

3.2.7 Substrate Summary

With the aid of Appendix C, a substrate summary should also be prepared to facilitate MCM layout and aid MCM assembly, test and troubleshooting. This summary includes relevant substrate characteristics discussed in section 3.2.5 such as drawings depicting the layer allocation and substrate cross section, layout and routing rules, pin and lead data, seal ring dimensions, heat spreader information, etc. This information should be collected into a single package for ease of use and reference (the Table C.3 summary can serve as the first page).

3.2.8 Testing Considerations

The MCM package design must address testing considerations as detailed in the following subsections and in Appendix E. The test engineer should review the MCM design for substrate and MCM testability before the design is committed to manufacturing. The MCM testing review should be based on the Table E.1 checklist.

3.2.8.1 Substrate Testing

Substrate network verification is essential prior to MCM assembly, and it typically occurs either just before or just after pins or leads and the seal ring are attached to the substrate. This verification is usually conducted on a probe test system and can include continuity, isolation, capacitance and resistance (including resistor trim) measurements. The incorporation of test fiducials (see section 3.3.5.3) and test pads (see section 3.2.5.9 and 3.2.5.10) into the substrate design ensures adequate test alignment and probe target features, and the Net Data test file (see sections 3.3.9 and 4.3.5) provides the X, Y and Z locations of all substrate network nodes that require probing.

3.2.8.2 MCM Test Levels

There are generally two MCM test levels: pre-lid and post-lid. The pre-lid test level will include tests requiring access to components and/or test pads not available after the lid is attached. These tests may include some or all of the following:

- functional resistor trimming,
- functional resistor select,
- component timing verification,
- component functionality verification, and
- MCM system verification.

The post-lid test level will limit accessibility to components and/or test pads; therefore, post-lid testing will usually consist of a subset of the pre-lid tests.

3.2.8.3 MCM Test Specifics

The MCM design must adequately consider each of the following test specific areas to ensure an achievable test interface.

- Spacing and location of components and/or test pads must permit reliable test probe access.
- In the case of controlled impedance probing (i.e., dual tip probing), component and test pad placement must be compatible with dual probe tip access.
- The MCM package design must provide physical orientation features for correct insertion into test fixturing.
- The MCM input/output pin or lead definition and location must provide reliable interconnect to the test fixturing.
- Package strength must permit test fixturing to hold the MCM in place during testing (this may include keepout regions on the MCM to allow for fixture clamping).

3.2.9 Mechanical Interface

The mechanical interface between the MCM and the user system will be documented. Details to be addressed include:

- pin or lead geometry and locations and associated tolerances and signal pin assignment,
- scheme for addressing the thermal coefficient of expansion mismatch between the MCM and the user system,
- recommended MCM attachment material composition and process temperatures,
- encapsulation constraints relating to heat transfer and shock/vibration, and
- documentation of MCM to user system thermal pathways including heat flux and any assumptions regarding user system temperatures and coolant flow rates.

3.3 Substrate Design/Layout

The substrate design/layout is the concluding process in the MCM design where all of the MCM customer requirements, the manufacturing process capabilities, and the remaining design tradeoff options are merged together to create the final MCM package definition. The process of creating the MCM package definition also defines the substrate features due to the nature of the MCM-C technology.

3.3.1 Seed File Definition

The EDMA seed file is a master file from which new MCM designs are established. This file contains information used throughout the MCM EDMA design cycle such as clearances, trace widths, and layer definitions. At the initialization of the design cycle, the seed file parameters must be modified to include the requirements for each new MCM design. These parameters are developed in section 3.2.5.

3.3.2 New Component Cells

The component cells are the graphical representation of the electrical components that make up the complete MCM design. The EDMA system has a large library of component cells. However, previously undefined components must have cells created within the EDMA system. These cells are created using component information found in sections 3.2.3 and 3.2.5.

3.3.3 Netlist

A netlist is a listing of the logical connections found in the MCM schematic, and it is used during the MCM conductor routing process. It is sometimes called a "To/From" list because it lists all established interconnects between components, I/O pins, connectors, etc. This ASCII file contains a listing of the schematic electrical nets and any errors or warnings that can affect electrical connectivity (e.g., unconnected pins).

3.3.4 Physical Features

Physical features are those features that are part of the MCM package but are not part of the schematic/netlist or the component cell definitions. Hence, these features must be added to the MCM package definition by the designer/draftsman. These features include package size, pin one indicator, cavity cutout dimensions, thermal vias, braze pads, manufacturing tooling features, and fiducials.

3.3.5 Fiducials

Fiducials are physical features, typically metal pads, that should be strategically placed on the MCM substrate for aiding the MCM assembly and testing processes.

3.3.5.1 Wire Bonding and Wire Pull

To ensure alignment of the wire bonding tip to each local bonding area such as a die site, a 20-mil-square pad should be placed at each corner of the local area. These local bonding fiducials are typically most beneficial around small, tightly clustered die bond sites.

3.3.5.2 Component Pick and Place

The current KCD pick and place equipment for die components does not require any special alignment fiducials on the substrate because it can align on existing features such as a wire bond pad. Similarly, the current KCD surface mount pick and place equipment does not require unique alignment features because this equipment can be aligned to the substrate test alignment fiducials (refer to section 3.3.5.3).

3.3.5.3 Test Alignment (both sides)

To facilitate substrate alignment for testing, four 40-mil-diameter pads are required on the top and bottom surfaces of the substrate. They should be electrically connected to a ground plane, and all other substrate metal should clear these fiducials with a 20-mil all-around clearance. These pads should be located as close as possible to the substrate outside corners, and they can be located under large surface mount components. In some cases, circular PGA bond pads can also serve as test fiducials, thereby eliminating the need for separate fiducials. Typically, substrate testing will be conducted before surface mount components are attached and possibly before brazing of pins/leads and the hermetic seal ring.

3.3.6 Verification and Routing

At this point, the substrate should be ready for net routing. However, prior to initiating the routing process on the EDMA system, one final check of the substrate design and layout considerations should be conducted. Appendix B contains two checklists and the first list, Table B.1, should be used for this final pre-routing check.

Routing is the process of placing the electrical conductor traces and vias (layer by layer) that interconnect the components of the MCM design. The netlist (refer to section 3.3.3) is the file that is used by the EDMA router, and the routing process is accomplished by using the EDMA system automatic router. Conductor traces that are not placed by the automatic router must then be routed manually by a designer/draftsman. When the routing process is complete, verification of the connections is accomplished using the EDMA design rules checking (DRC) software and/or by manually reviewing each electrical net (again, layer by layer).

Table B.2 provides a checklist of post-routing activities which must be satisfactorily conducted to verify an acceptably routed substrate.

3.3.7 Manufacturing Aids

During the substrate layout stage of the MCM design, alignment holes are commonly added outside the active substrate outline to aid manufacturing. Typical alignment features and the function of each are listed below.

- Four 25-mil-diameter holes are added to each layer to ensure identical print screen alignment for each layer.
- Two 34-mil-diameter holes are added on the horizontal axis of each layer to ensure layer-to-layer alignment during the lamination process.
- Two more 25-mil-diameter holes are added to each layer as alignment targets for the first post-fired print.
- 60-mil-square pads (two per each subsequent post-fired print) are added as part of the first post-fired print to aid alignment of all subsequent post-fired prints.
- Two 50-mil-square matching pads are included as part of each subsequent post-fired print screen for alignment to two of the 60-mil pads of the first post-fired print.

Additional tooling features can be placed outside the active substrate outline as required to aid alignment for other manufacturing processes such as substrate sizing.

3.3.8 MCM and Piecepart Drawings

After completion of the MCM design, drawings depicting the MCM assembly and its substrate can be created. The graphical representations of the MCM and its substrate can be extracted from the MCM and substrate design files, and various requirements and manufacturing notes may be added to these drawings. The designer is encouraged to use the Table D.1 checklist when finalizing these drawings to ensure recommended coverage of drawing content for enhanced producibility. If the drawing definition is to be of WR quality, then Table D.1 also provides a checklist for the comprehensive development of component drawings and test documents.

3.3.9 Manufacturing and Testing Files

Upon completion of the substrate design process, specific data can be extracted from the EDMA system as file information, either in ASCII format or as a graphical picture with dimensions.

- X-Y Hole Summary - This file, also called the via drill coordinates output, is an ASCII file which contains all via and mounting hole X-Y locations, layer by layer.
- Cavity Cutout Coordinates - The output of this file is a graphical representation of the cavity forming cutouts with applicable layers and dimensions. These graphics can be plotted as hardcopy for distribution to manufacturing.
- TKN Resistor Trim Coordinates - The output of this file is a graphical representation of the resistor trim coordinates with corresponding dimensions.
- Component Info List - This ASCII file contains all X-Y coordinates of every component pin in the design along with the reference designator.
- Net Data - This file is an ASCII file containing all X-Y probe coordinates in a format compatible with the substrate test system.

3.4 MCM PRODUCIBILITY

When an MCM design is completed but before it is committed to manufacturing, a final assessment of MCM producibility must be conducted. This assessment is the culmination of an on-going producibility assessment which should have been occurring throughout the design process, particularly just prior to substrate routing. The overall producibility assessment must evaluate two basic questions: can the MCM design be manufactured, and is the resulting MCM testable? Clearly, if the answer to both questions is yes, then the MCM design is complete, except for a final evaluation of the cost and delivery parameters. If not, then each factor which detracts from producibility must be analyzed, and resolution may require changes in the MCM design.

Finally, adherence to the design rules presented in this document is expected to produce MCM designs that lead to optimum substrate fabrication, MCM assembly, and testing yields and MCMs that can be delivered on schedule at a reasonable cost. Customer design requirements that exceed the preferred dimensions, materials and equipment listed in this document should be jointly evaluated by the customer and the KCD MCM team for producibility. Use of the concurrent engineering checklists from Appendices B, D and E will assist the designer during the initial phases of the MCM design and enhance the producibility of the MCM.

3.4.1 Component Availability and Quality

The producibility of an MCM design can be influenced by the availability and quality of the MCM pieceparts, particularly die components such as ASICs. Unlike packaged components, when a die is incorporated into the design, it is not readily

replaceable with a functionally identical die from another supplier (i.e., different die size and bond pads will require a new substrate layout). Even if die quantities are expected to be available, additional die testing may be required (either by the supplier or at KCD) to ensure die quality (known good die) prior to MCM assembly; otherwise, excessive "die replacement" rework will be inevitable. For example, if an MCM has five die devices, each with a good probability of 0.95, then 23 MCMs out of every 100 MCMs will require die replacement rework. Thus, die suppliers must be carefully selected based on their ability to provide timely die quantities, preferably at the desired quality levels; otherwise, MCM producibility can be jeopardized (refer to Table F.1 for additional information on component considerations).

3.4.2 Manufacturing

The ability to manufacture an MCM design must not only address the availability of those processes and equipment directly related to the assembly of the MCM (refer to Appendix D) but also the processes and equipment required to produce all MCM pieceparts such as the LTCC substrate (refer to Appendix C). While all processes and equipment may be available, acceptable producibility must also permit an achievable assembly sequence that provides die protection, cleanliness and decreasing process temperatures with subsequent processing steps.

3.4.3 Testing

The ability to test the assembled MCM must address the availability of test equipment and the adaptation of that equipment to the MCM during all required test environments. If the MCM design incorporates BIST and/or boundary scan features, then the MCM testability can only be enhanced. Also, the testability assessment must encompass the MCM pieceparts, particularly the substrate and the die components. Substrate testability includes the ability to test the substrate networks and laser trim the TKN resistors. Thus, in addition to the availability of appropriate test and manufacturing equipment, a substrate probing capability must be available in both cases. The testability of die components must directly reflect the strategy for die acquisition, where all testing may be conducted by the supplier. If additional testing is required at KCD, then testability becomes a function of die handling, contacting and interconnecting to a test system; and all facets of the equipment must be available and operational to support the producibility of the MCM design.

3.5 Cost and Delivery Evaluation

Once the design is judged to be producible, then the cost and time required to produce and deliver the required MCM quantities must be evaluated. This evaluation should provide quantity, cost and delivery (QCD) estimates of the following areas as a minimum.

- All MCM components (including die, SM, LCC, etc.) - The QCD estimate must reflect the supplier QCD information and any additional or special testing required on any of these components.
- LTCC substrates - If purchased, the QCD estimate must reflect the supplier QCD information and any additional inspection and testing at KCD; if fabricated at KCD, the QCD estimate must project all manufacturing and testing costs and the flow time through this combined sequence.
- Other MCM pieceparts - A QCD estimate must be provided for the remaining MCM pieceparts (ring, lid, pins, leads, etc.) and reflect the supplier QCD information.
- MCMs - The QCD estimate must project the estimates for assembly, test, inspection and rework of each module.

4.0 DELIVERABLES

In general, the MCM design may be documented by several different techniques: formal drawings; other documentation methods such as summaries, reports and analyses; and the EDMA electronic data files. All such items of documentation evolve from Section 3 and are deliverable entities, either to the customer, the manufacturing and testing processes, or both. The following subsections describe these documentation techniques as applied to the MCM design.

4.1 DRAWINGS

Development of a drawing set defining the MCM and its pieceparts is a required approach at KCD to establish and control the product definition.

4.1.1 MCM Definition

The development drawing definition of the MCM is that set of drawings that fully defines the MCM as listed below (the n-string represents a 7-digit KCD development product number).

- MCM Parts List (nnnnnnn)
- MCM Assembly (AYnnnnnnn)
- MCM Schematic (CKnnnnnnn)

The make piecepart items such as the substrate and lid are defined by their own lower level drawings and called out in the MCM parts list.

4.1.2 Substrate Definition

The development drawing definition of the LTCC substrate is that set of drawings that fully defines the substrate as listed below (the m-string is another 7-digit KCD development product number).

- Substrate Parts List (mmmmmmm)
- Substrate Assembly (AYmmmmmmm)

The substrate piecepart items such as the seal ring and the pins or leads are called out on the substrate parts list and defined by their own lower level drawings (if make items); if commercially available, they are simply called out on the substrate parts list by commercial number. Also, since the substrate is a piecepart of the MCM, it is called out on the MCM parts list.

4.1.3 Electrical Component Definitions

MCM electrical components include all electrical devices incorporated into the MCM design and all I/O features affecting electrical performance. These components are called out on the MCM parts list.

4.1.3.1 Devices

In most cases, electrical devices incorporated into the MCM design are commercially available devices (surface mount components and some die devices). In the remaining cases, the devices (such as ASICs) are developed under contract by a commercial die supplier. Thus, typical supplier documentation may include many of the following items that encompass device definition, and, as such, become deliverable information to the customer:

- schematic,
- data sheet,
- footprint or package geometry,
- I/O signal versus bond pad allocation,
- vendor map,
- test vectors, and
- simulation model.

4.1.3.2 Pins and Leads

Generally, the MCM I/O is realized by using commercially available pins or leads. If the selected commercial part requires modification or special adaptation for the MCM substrate application, then a separate drawing is created to define such usage, or an I/O detail is incorporated into the substrate AY drawing. Thus, the commercial drawing defining the pin or lead, its material composition, dimensions, etc., and any related application specific drawing become deliverables to the customer.

4.1.4 Mechanical Component Definitions

MCM mechanical components include all mechanical pieceparts required in the assembly of the MCM or its substrate. These pieceparts include the seal ring and its lid and the heat spreader.

4.1.4.1 Seal Ring and Lid

The substrate cavity seal ring can be a custom piecepart (unique drawing required) or possibly purchased as a commercially available part (supplier drawing). In either case, the seal ring drawing defines the dimensional characteristics and material properties of the seal ring and becomes a deliverable to the customer. Also, this piecepart is called out on the substrate material list and shown on the substrate AY drawing.

The lid required to seal the substrate cavity is a companion part to the cavity seal ring. Again, the lid can be a custom piecepart (unique drawing required) or possibly purchased as a commercially available part (supplier drawing). In either case, the lid drawing defines the dimensional characteristics, material properties, and solder preform (if applicable) of the lid and becomes a deliverable to the customer. However, unlike the ring, this piecepart is called out on the MCM material list and shown on the MCM AY drawing.

4.1.4.2 Heat Spreader

A heat spreader may be incorporated into the design of an MCM to aid heat transfer. If so, the spreader is defined by a separate drawing (if custom) or a supplier drawing (if commercially available). In either case, the drawing defines the dimensional characteristics and material properties of the spreader and becomes a deliverable to the customer. This piecepart is then called out on the MCM material list and shown on the MCM AY drawing.

4.2 DOCUMENTATION

Deliverable hardcopy documentation other than development drawings can include summaries of components and substrates, reports, analyses, test plans, and cost and delivery schedule information.

4.2.1 Summaries

Since an MCM is composed of its components interconnected by its primary LTCC substrate and any secondary component substrates and since the

LTCC substrate defines the I/O characteristics of the MCM, then summaries of these areas may be appropriate as deliverable information to the customer.

4.2.1.1 Components

A summary of the MCM components (both electrical and mechanical) would be additional information supplementing the development drawings listed in section 4.1. This summary might touch on any of the following areas:

- collection of all component package, geometric and I/O features by supplier;
- primary and secondary suppliers for each component with related cost and delivery information;
- special considerations such as operating speed, power dissipation, size (relative to system constraints), etc.; and
- rationale for component selection.

Such component summary information may be readily presented in the tabular forms of Tables F.2 and F.3.

4.2.1.2 Substrates

Usually an MCM design will encompass only one substrate, the LTCC substrate. However, special cases can exist where one or more secondary component substrates are incorporated into the MCM design to enhance heat transfer from selected devices. Thus, a summary of the substrates incorporated into the MCM design is appropriate and represents a deliverable to the customer. This summary might be expected to add information in the following areas:

- expanded cross-section of the LTCC substrate, with signal assignments and primary direction of trace runs for each metal layer;
- if purchased from an LTCC substrate supplier, cost and delivery information with rationale for supplier selection;
- if fabricated in-house, flowchart of the LTCC substrate fabrication sequence supported by estimates of labor and material required at each sequence step, and the projected overall flowtime through the sequence; and
- for secondary component substrates, rationale for their utilization and projected supplier, cost and delivery information.

Much of this substrate summary information can be presented as a completed Table C.3.

4.2.2 Analyses

There are many possible analyses that may occur during the course of the MCM design, and such information should be documented and delivered to the customer to support and justify the design. Such analyses may include but are not restricted to the following areas:

- component power dissipation and heat transfer;
- trace, via and pin/lead current carrying capabilities;
- controlled impedance interconnect;
- worst-case functionality;
- worst-case fit; and
- producibility (see section 3.4).

4.2.3 Test Plans

Test plans developed for the MCM and its major pieceparts (substrate and large die components) are deliverables to the customer. Each test plan should amply address the following items as a minimum:

- MCM or piecepart description,
- testing assumptions,
- block diagram of probable test system,
- accuracies and environments,
- test sequences,
- functional tests, and
- estimate of testing throughput.

4.2.4 Test Data

At the conclusion of the MCM design, available MCM-related test data will not exist other than preliminary data from simulation, breadboard and/or mechanical type testing such as shear and pull test data. However, the proposed approach for test data should be presented to the customer for concurrence, and it should address the following areas with emphasis on content, format and method of data transmission:

- MCM electrical test data (functional test results),
- MCM hermetic seal test data,
- MCM size conformance data,
- substrate electrical test data (functional test results),
- substrate mechanical verification (pin/lead integrity),
- substrate size conformance data, and
- component test data.

4.2.5 Cost and Delivery Schedule

Cost and delivery information is a standard deliverable to the customer. Such information may best be delivered in two parts: first, the projected cost and time required to conduct the MCM design, and, later, at the conclusion of the design, the projected cost and time required to build, test and deliver MCMs per the design, both in prototype and production quantities (refer to section 3.5).

4.2.6 Reports

One or more of the subsections of 4.1 and the previous subsections of 4.2 can be consolidated as applicable into a comprehensive MCM design report of broad coverage. Virtually all design considerations and features, from concept to completed design with projected costs and schedules, can be captured in a single report document and delivered as an entity to the customer.

4.3 CAD Files

After completion of substrate design and layout (concluding with section 3.3), various reports can be generated to aid the manufacturing and inspection processes. These report files are normally stored on the EDMA system as ASCII data and can be viewed or written to a 3.5-inch floppy disk which is an IBM PC-compatible, high-density diskette formatted in compliance with the MS-DOS format. In a few cases, the information is currently available in graphical hardcopy form only; however, even this information is expected to be available as ASCII data in the near future.

4.3.1 Definition Data (DD) Files

DD files are files that contain the material printing definition for each substrate layer (i.e., traces, pads, resistors, dielectric, alignment and test features, etc.). These data are normally generated after successful completion of the substrate routing and verification (see section 3.3.6). DD information can be supplied on a 3.5-inch disk or as 1:1 photo-plotted film.

4.3.2 Via Drill Coordinates

The EDMA via drill coordinates report is used to generate NC drill data that specify the diameter and location of every via within each substrate layer. This report is normally generated as part of the activities that develop tooling aids (section 3.3.9), and the final product is an ASCII file. This file can be copied to a 3.5-inch disk in an NC format that can directly control via drill or punch equipment.

4.3.3 Cavity Cutout Coordinates

All cavity cutouts are also defined as part of the development of tooling aids (see section 3.3.9), and they currently exist only as graphical information. These graphics depict the final dimensions of all cavity features where the dimensional origin is typically at the lower left corner of the finished substrate. This information is not currently available from the EDMA system as ASCII data. Consequently, the cutout dimensions must be manually entered into the machining equipment.

4.3.4 TKN Resistor Trim Coordinates

The probe and trim coordinates and the maximum cut length for each printed, thick film resistor are defined as part of the development of tooling aids (see section 3.3.9). However, these data are not directly available as ASCII data. Consequently, a separate file must be manually prepared that defines the location and maximum length of cut and the location of each probe tip. Once prepared, this information can be manually entered into the resistor trim equipment.

4.3.5 Substrate Test Coordinates

Test coordinates as described in the manufacturing and testing files of section 3.3.9 can be extracted from the EDMA system using a custom software package. The output is written in ASCII to a file named "Net Data" and is formatted for input to the substrate test system. This file is generated by reading the netlist data (see section 3.3.3) and the Pin/Pad table created in the seed file definition (see section 3.3.1).

Appendix A

MATERIAL PROPERTIES

The purpose of this appendix is to provide a convenient reference of some key properties of materials used in multichip module applications. The appendix summarizes thermal, electrical, mechanical, and processing information on these materials, and the parametric values come from a variety of sources listed at the end of the appendix.

The appendix contains six tables as itemized below.

Table A.1 **Properties of Pure Metals**

Table A.2 **Properties of Alloys**

Table A.3 **Properties of Substrate Materials**

Table A.4 **Properties of Adhesive Materials**

Table A.5 **Properties of Semiconductor Materials**

Table A.6 **Properties of Solder Materials**

PURE METALS

		Silver	Copper	Gold	Aluminum	Nickel
Parameter	Units	Ag	Cu	Au	Al	Ni
Manufacturer		--	--	--	--	--
Density @ 25°C	g/cm^3	10.5[1]	8.92[1]	19.3[1]	2.702[1]	8.90[1]
Thermal Conductivity @ 100°C	W/m-K	427[1]	398[1]	315[1]	237[1]	89.9[1]
Thermal Expansion @ 0°-200°C	ppm/°C	19[1]	16.6[1]	14.2[1]	25[1]	13[1]
Specific Heat	J/g-K	0.234[1]	0.385[1]	0.129[1]	0.900[1]	0.444[1]
Young's Modulus	GPa	82.7[5]	129.8[5]	78.5[5]	70.6[5]	199.5[5]
Electrical Resistivity @ 20°C	Ω-cm	1.59μ[1]	1.67μ[1]	2.35μ[1]	2.65μ[1]	6.84μ[1]
Process Info - Melting Temperature	°C	962[1]	1083[1]	1064[1]	660[1]	1453[1]
KCD ES&H Approval?						

Table A.1 Properties of Pure Metals

ALLOYS

		CMSH A-40	Cu-Mo-Cu	Invar	Kovar	Thermkon 76
Parameter	Units	Al60/Si40	Mo74/Cu26	Fe64/Ni36	Fe54/Ni29/Co17	W80/Cu20
Manufacturer		Sumitomo	AMAX, Inc.	INCO	Stupakoff Labs	CMW, Inc.
Density @ 25°C	g/cm^3	2.53[9]	9.9[10]	8.1[20]	8.36-8.50[5]	15.56[11]
Thermal Conductivity @ 100°C	W/m-K	138[9]	195[10]	11[20]	17.1[25]	180[11]
Thermal Expansion @ 0°-200°C	ppm/°C	13.5[9]	5.66[10]	1.7-2.0[5]	4.81[5]	7.6[11]
Specific Heat	J/g-K	0.879[9]	0.295[10]	0.515[20]		
Young's Modulus	GPa	101[9]	228[10]	140-150[5]	14.1[5]	240[11]
Electrical Resistivity @ 20°C	Ω-cm	8.35μ[9]	3.5μ[10]	75-85μ[5]	48.9μ[5]	4.21μ[11]
Process Info - Melting Temperature	°C		2575-2675[25]		1450[25]	
KCD ES&H Approval?						

Table A.2 Properties of Alloys

SUBSTRATE MATERIALS

Parameter	Units	Natural Diamond Type IIa	CVD Diamond	Polycrystalline Diamond	Beryllia	Aluminum Nitride
		C	C	C	BeO	AlN
Manufacturer			Crystallume	Diamonex	Brush Wellman	Carborundum
Density @ 25°C	g/cm^3	3.515[2]	3.5[16]	3.2 to 3.4[15]	2.85[12]	3.26[12]
Thermal Conductivity @ 100°C	W/m-K	2000[2]	1300[16]	>1300[15]	260[12]	170[12]
Thermal Expansion @ 0°-200°C	ppm/°C	1.34[2]	2.0[16]	2[15]	7.2[12]	4.1[12]
Specific Heat	J/g-K		0.519[16]		1.0[12]	0.7[12]
Young's Modulus	GPa	900-1000[2]	1050[24]		262[12]	276[12]
Flexural Strength	MPa	300[3]			240[3]	450[3]
Electrical Resistivity @ 20°C	Ω-cm	10^4 to $>10^{16}$[2]	10^{12} to 10^{16}[24]	$>10^{11}$[15]	$>10^{14}$[12]	$>10^{14}$[12]
Rel. Dielectric Constant @ freq		5.68 @ 3 kHz[2]	5.7 @ ?[24]	5.7 @ ? [15]	6.7 @ 10 MHz[12]	8.8 @ 10 MHz[12]
Dielectric Loss Tangent @ freq	$x10^{-3}$	10 @ ?[3]	0.5 @ ?[14]	<0.5 @ 15 GHz[15]	1 @ 10 MHz[12]	<1 @ 10 MHz[12]
Process Info - Melting Temperature Max Useful Temperature	°C	500-700[2]		700[15]	1700[12]	1800[12]
KCD ES&H Approval?						Y

Table A.3 Properties of Substrate Materials

SUBSTRATE MATERIALS (CONT.)

Parameter	Units	Silicon Carbide SiC	Alumina 96% Al_2O_3	LTCC 901	LTCC 951
Manufacturer		Brush Wellman	Coors	Du Pont	Du Pont
Density @ 25°C	g/cm^3	3.2[12]	3.75[13]	2.6[21]	3.1[6]
Thermal Conductivity @ 100°C	W/m-K	70[12]	20[13]	3.0[6]	3.0[6]
Thermal Expansion @ 0°-200°C	ppm/°C	3.8[12]	6.3[13]	3.0[6]	5.7[6]
Specific Heat	J/g-K	0.8[12]	0.88[13]		
Young's Modulus	GPa	407[12]	303[13]		
Flexural Strength	MPa	490[17]	399[13]	230[6]	320[6]
Electrical Resistivity @ 20°C	Ω-cm	$>10^{11}$[12]	$>10^{14}$[13]		
Rel. Dielectric Constant @ freq		40 @ 10 MHz[12]	9.5 @ 100 MHz[13]	5.2 @ 1 kHz[6]	7.8 @ 10 MHz[6]
Dielectric Loss Tangent @ freq	$x10^{-3}$	80-170 @ 10 MHz[12]	0.4 @ 100 MHz[13]	< 2.0 @ 14 MHz[6]	1.5 @ 10 MHz[6]
Process Info - Melting Temperature Max Useful Temperature	°C	1900[12]	1500[12]	650[21]	650[21]
KCD ES&H Approval?			Y	Y	Y

Table A.3 Properties of Substrate Materials (cont.)

ADHESIVE MATERIALS

Parameter	Units	Abelbond 84-1LMIT	Epibond 7002	Epo-Tek H20E	Staystik 101	Staystik 151
		Silver-filled epoxy	Silver-filled epoxy	Silver-filled epoxy	Silver-filled Thermoplastic	Gold-filled Thermoplastic
Manufacturer		Abelstik	Furane	Epoxy Technology	Staystik	Staystik
Density @ 25°C	g/cm^3	3.99[8]	2.99[18]	2.60[19]		
Thermal Conductivity @ 100°C	W/m-K	5.9[8]	1.67[18]	1.59[19]	3.0[7]	2.0[7]
Thermal Expansion @ 0°-200°C	ppm/°C	52[8]	50[18]		40[7]	40[7]
Specific Heat	J/g-K				0.46[7]	0.88[7]
Die Shear Strength @ 25°C	MPa	34.5[8]	11.9[18]		30.0[7]	31.7[7]
Lap Shear Strength @ 25°C	MPa	11.0[8]	13.8[18]	10.3[19]		
Electrical Resistivity @ 20°C	Ω-cm	70μ[8]	200μ[18]	100-400μ[19]	10-100μ[7]	100μ[7]
Process Info - Curing Temperature Glass Transition Temperature	°C	150[8] 103[8]	165[18] 145[18]	50-175[19] 50-60[19]	250-300[7] >150[7]	250-300[7] >150[7]
KCD ES&H Approval?			Y	Y	Y	Y

Table A.4 Properties of Adhesive Materials

ADHESIVE MATERIALS (CONT.)

Parameter	Units	Staystik 181 Silver-filled Thermoplastic	Stayform 401 Thermoplastic	Stayform 501 Silver-filled Thermoplastic	Stayform 581 Silver-filled Thermoplastic
Manufacturer		Staystik	Staystik	Staystik	Staystik
Density @ 25°C	g/cm^3				
Thermal Conductivity @ 100°C	W/m-K	3.0[7]	0.20[7]	3.0[7]	3.0[7]
Thermal Expansion @ 0°-200°C	ppm/°C	40[7]	60[7]	40[7]	50[7]
Specific Heat	J/g-K	0.46[7]	1.26[7]	0.46[7]	0.46[7]
Die Shear Strength @ 25°C	MPa	20.7[7]	24.8[7]	29.0[7]	19.3[7]
Lap Shear Strength @ 25°C	MPa				
Electrical Resistivity @ 20°C	Ω-cm	10-100μ[7]	10^{16}[7]	10-100μ[7]	100μ[7]
Rel. Dielectric Constant @ freq			3.0 @ 50 MHz[7]		
Dielectric Loss Tangent @ freq	$x10^{-3}$		10 @ 50 MHz[7]		
Process info - Curing Temperature Glass Transition Temperature	°C	150-250[7] >150[7]	230-320[7] >150[7]	275-380[7] >150[7]	150-250[7] >150[7]
KCD ES&H Approval?		Y	Y	Y	Y

Table A.4 Properties of Adhesive Materials (cont.)

SEMICONDUCTOR MATERIALS

		Silicon	Gallium Arsenide
Parameter	Units	Si	GaAs
Manufacturer			
Density @ 25°C	g/cm^3	2.3283[1]	5.316[1]
Thermal Conductivity @ 100°C	W/m-K	83.5[1]	46[3]
Thermal Expansion @ 0°-200°C	ppm/°C	3[1]	6[4]
Specific Heat	J/g-K	0.707[1]	0.327[1]
Young's Modulus	GPa	131[23]	85.5[23]
Flexural Strength	MPa		
Electrical Resistivity @ 20°C	Ω-cm	230k[5]	10^8[22]
Rel. Dielectric Constant @ freq		12[3]	12.9 @ 4-18 GHz[22]
Dielectric Loss Tangent @ freq	$x10^{-3}$		
Process Info - Melting Temperature	°C	1410[1]	1238[1]
KCD ES&H Approval?			

Table A.5 Properties of Semiconductor Materials

SOLDER MATERIALS

		Tin/Lead	Eutectic
Parameter	Units	Sn63/Pb37	Au80/Sn20
Manufacturer		Williams	Williams
Density @ 25°C	g/cm^3	8.40[25]	14.51[25]
Thermal Conductivity @ 100°C	W/m-K		68.2[25]
Thermal Expansion @ 0°-200°C	ppm/°C		15.93[25]
Specific Heat	J/g-K		
Die Shear Strength @ 25°C	MPa		
Lap Shear Strength @ 25°C	MPa		
Electrical Resistivity @ 20°C	Ω-cm		
Process Info - Liquidus Temperature	°C	183[25]	280[25]
KCD ES&H Approval?			

Table A.6 Properties of Solder Materials

FOR INFORMATION ON WIRES AND RIBBONS (FOR DIE CONNECTIONS) SEE APPENDIX D.

MATERIAL PROPERTIES REFERENCES

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Appendix B

MCM-C CAD CHECKLISTS

The MCM design engineer and design draftsman should develop an MCM package design concurrently with the manufacturing engineers and consistent with the recommendations of this guideline. Toward that end, this appendix provides the designer with two checklists (itemized below) to support the initial phases of the MCM design. The first checklist should be reviewed and completed prior to any routing of substrate conductor traces, and the second checklist should be reviewed and completed after substrate trace routing and the availability of the electronic data files.

Table B.1 Substrate Pre-Routing Checklist

Table B.2 Substrate Post-Routing Checklist

PRE-ROUTING TASKS	DATE COMPLETED	DATE TO BE COMPLETED	N/A
VERIFICATION			
Schematic vs. draft schematic			
Electronic netlist file vs. schematic			
Components CAD definition vs. component definitions			
CONSIDERATIONS			
Controlled impedance conductor lines			
Propagation delay			
High current conductor lines			
Isolation, shielding and cross talk			
Thermal management			
Die backside metallization and potential			
PRINTED RESISTORS			
Verify each resistor value			
Power dissipation considered for each resistor			
Low resistance paths to low value resistors			
Probe pads for resistor trimming			
Place all resistors for active trimming on one side of LTCC			
Provide opening in all resistor loops			
DESIGN DEFINITION			
Electrical interface			
Mechanical interface			
LTCC layers (number, planes and XY runs)			
LTCC cavity (features and components)			
MANUFACTURABILITY			
Substrate considerations reviewed with engineer			
MCM package considerations reviewed with engineer			
TESTABILITY			
Requirements reviewed with test equipment engineer			
Test nodes defined for key signals			

Table B.1 Substrate Pre-Routing Checklist

POST-ROUTING TASKS	DATE COMPLETED	DATE TO BE COMPLETED	N/A
Verify CAD conductor routing vs. schematic			
Verify conductor lines widths/spacings/vias meet design definition			
Verify special features			
Controlled impedance conductor lines (W)			
Propagation delay (L)			
High current conductor lines (W)			
Thermal management			
Verify all surface mount component pads have double print of metal			
Verify alignment marks for automatic equipment			
Verify placement of pin one indicator for components and substrate			
Verify seal ring, lid and braze pad are correct for final MCM package design			
Verify final MCM package design against MCM requirements			

Table B.2 Substrate Post-Routing Checklist

Appendix C

SUBSTRATE INFORMATION AND CONSTRAINTS ON DESIGN

The purpose of this appendix is to provide guidance to a designer during the initial phases of the MCM design. Failure to adhere to this guidance may lead to an MCM that is more expensive and time consuming to produce and could lead to a substrate that is simply not producible.

The appendix summarizes the information and constraints for building LTCC substrates and addresses the internal metallization, external metallization, and thick film resistors that are part of an LTCC substrate. The data presented is for standard processing. Finer substrate features are available if required.

Every attempt has been made to make this information as complete as possible; however, not even a comprehensive document can substitute for direct exchanges between the designer and the substrate engineer.

This appendix contains two figures and three tables as itemized below.

Figure C.1 **Conceptual Substrate Cross-Section and Layer Allocation**

This figure represents a generic MCM-C with the substrate internal layers visible to provide a graphical illustration of substrate and MCM-C assembly. All traces, both pre-fired and post-fired, are printed thick film inks.

Table C.1 **LTCC Substrate Dimensional and Parametric Information and Constraints for a Typical Dielectric Tape**

This table lists the preferred dimensional features when the substrate is formed from dielectric tape.

Table C.2 **Typical Paste Properties**

This table summarizes the properties and applications of the pastes used in the fabrication of an LTCC substrate.

Figure C.2 **Seal Ring, Braze Pad and Lid Definition**

This figure illustrates the seal ring, braze pad and lid design requirements.

Table C.3 **MCM Substrate Summary**

When completed, this table provides a summary of the salient features of the substrate.

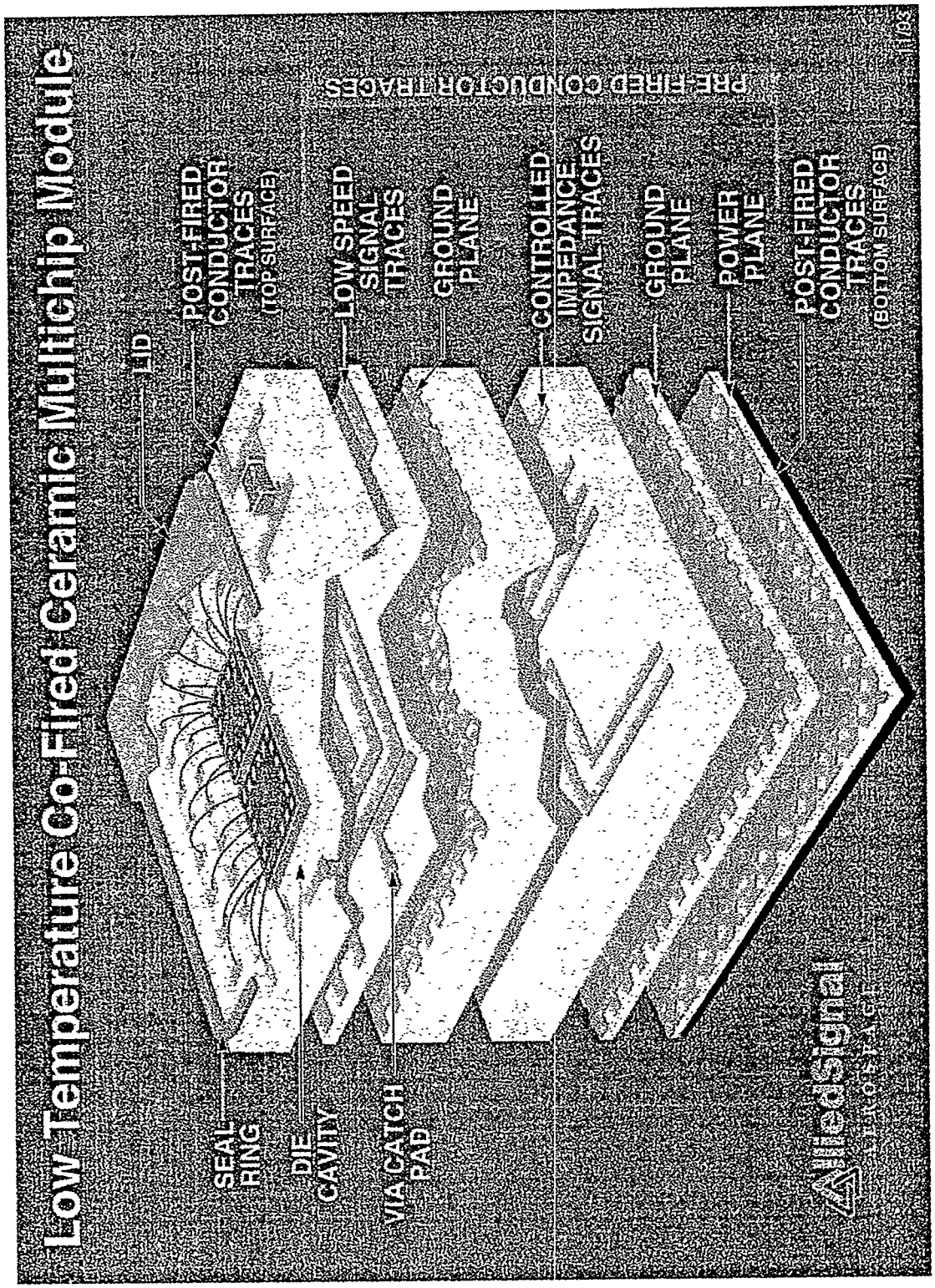


Figure C.1 Conceptual Substrate Cross-Section and Layer Allocation

LTCC SUBSTRATE DIMENSIONAL AND PARAMETRIC INFORMATION AND CONSTRAINTS for Typical Dielectric Tape

(All dimensions are in mils except where noted, 1 mil = 0.001 inches)

General Information on KCD Capabilities		
Maximum Part Size (Post-Fired)	2.61 X 2.61 inches	
Post Fired Dimensional Tolerances		
Pre-Fired Sizing	+/- 10%	
Post-Fired Sizing	+/- 2	
Maximum Number of Layers	50 *	
* Any design should minimize the number of layers needed.		
Camber (mils/inch)	3	typical

Typical Manufacturer's Data		
Shrinkage (from Pre-Fired to Post-Fired)		
X & Y Directions	13%	
Z Direction	15%	
Tape Thickness (in "Z" direction)	Pre-Fired	Post-Fired
Tape 1	4.5	3.8
Tape 2	6.5	5.5
Tape 3	10	8.5
Breakdown Voltage	>1000 Volts/mil	

Conductor Lines	Pre-Fired Dimension	Post-Fired Dimension
Line Width (As Printed)		
Pre-Fired	10	8.7
Post-Fired	N/A	10
Line Spacing (As Printed)		
Pre-Fired	10	8.7
Post-Fired	N/A	10
Spacing from line to edge of part	10	8.7

Electrical Vias	Pre-Fired Dimension	Post-Fired Dimension
Via Diameter	10	8.7
Via Spacing - Center to Center	30	26.1
Via Cover Pad	20	17.4
Clearance from Via Pad to Conductor Line	10	8.7
Distance from Via Center to Edge of Part	30	26.1
Via Stagger (at least every 2 layers)	20	17.4

Thermal Vias	Pre-Fired Dimension	Post-Fired Dimension
Via Diameter	20	17.4
Via Spacing - Center to Center	40	34.8

Ground/Power Planes	Pre-Fired Dimension	Post-Fired Dimension
Style	Cross-hatched	
Coverage	75% maximum	
Spacing from Edge of Plane to Edge of Part	30	26.1
Diameter of Opening in Ground or Power Plane for Via		
Signal Via	50	43.5
Thermal Via	70	60.9

Resistors	
Post-Fired Resistors (Typical)	
Range of Values	1k to 100k ohms
Length and Width	50 minimum
Overlap	10 minimum
Aspect Ratio (Length:Width)	
Minimum	1:5
Maximum	5:1
Trim Tolerance	+/- 5%
Maximum Power Density	25 Watts/square inch

Table C.1 LTCC Substrate Dimensional and Parametric Information and Constraints for a Typical Dielectric Tape

Typical Paste Properties

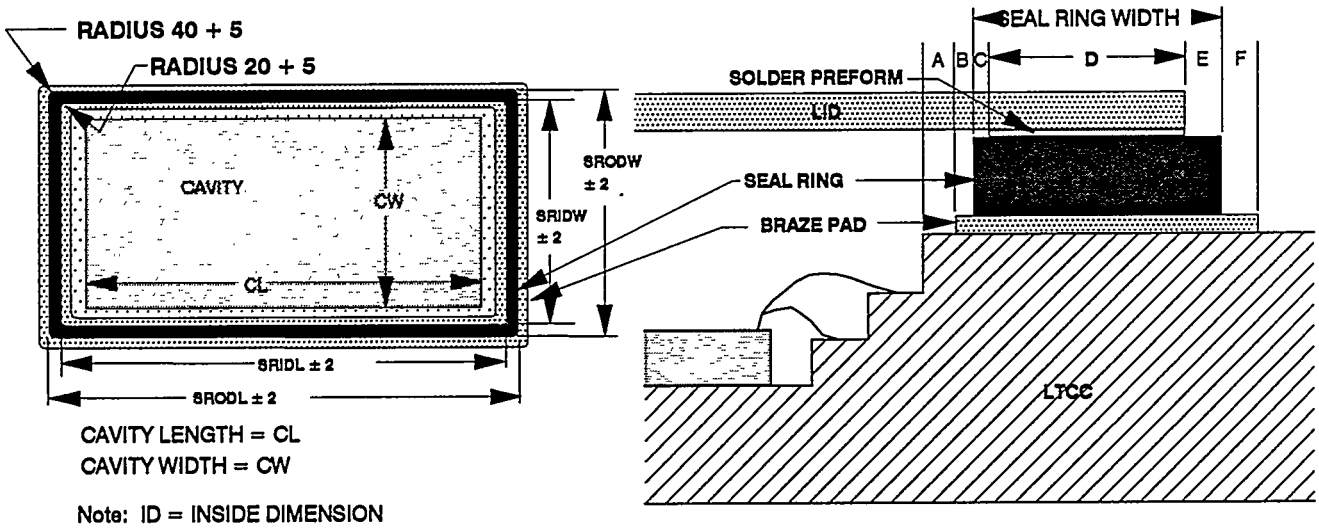
Primary Purpose	Metal Type	Resistivity (mohms/sq)	Nominal Thickness (microns)	Primary Use	Available at KCD
Cofire Systems					
Via Fill Conductors	Gold Gold	5	1 Layer 6 to 9		Yes Yes
Via Fill Conductors	Silver Silver	3.3	1 Layer 6 to 9		No No
Via Fill Conductors	Palladium/Silver Palladium/Silver	20	1 Layer 6 to 9		No No
External Post-Fire Materials					
Conductors	Gold	4	8	Gold Wire Bondable	Yes
Conductors Conductors	Palladium/Platinum/Gold Palladium/Gold	80 80	15 15	Tin/Lead Solder Lead/Indium Solder	Yes Yes
Conductors	Palladium/Silver	20	15	Tin/Lead Solder	No
Insulator	Glass	N/A	12	Cross-over Dielectric	Yes

Table C.2 Typical Paste Properties

SEAL RING, BRAZE PAD AND LID DEFINITION

(ALL DIMENSIONS ARE POST-FIRED, EXCEPT WHERE NOTED)

(ALL DIMENSIONS ARE IN MILS, EXCEPT WHERE NOTED. 1 MIL = 0.001 INCHES)



CAVITY LENGTH = CL
CAVITY WIDTH = CW

Note: ID = INSIDE DIMENSION
OD = OUTSIDE DIMENSION

SEAL RING

SEAL RING ID LENGTH (SRIDL) = CL + 2A + 2B
SEAL RING ID WIDTH (SRIDW) = CW + 2A + 2B
where A = 10 MIN (20 TYPICAL) and B = 10 MIN (TYPICAL)
SEAL RING OD LENGTH (SRODL) = SEAL RING ID LENGTH + SEAL RING WIDTH
SEAL RING OD WIDTH (SRODW) = SEAL RING ID WIDTH + SEAL RING WIDTH
where SEAL RING WIDTH is 50 (TYPICAL)
NOTE: A LARGE CAVITY WILL REQUIRE A LARGER SEAL RING WIDTH.

SEAL RING DRAWING NOTES: (TYPICAL)

1. MATERIAL: KOVAR.
2. FINISH BURR FREE.
3. PLATING SPECIFICATION ON RING TO BE 75 MICROINCHES MIN. AU OVER 50 MICROINCHES MIN. NI.

BRAZE PAD

BRAZE PAD ID LENGTH = SEAL RING ID LENGTH - 2B
BRAZE PAD ID WIDTH = SEAL RING ID WIDTH - 2B
BRAZE PAD OD LENGTH = SEAL RING OD LENGTH + 2F
BRAZE PAB OD WIDTH = SEAL RING OD WIDTH + 2F
where F = 10 MIN (15 TYPICAL)
BRAZE PAD RADIUS SHOULD BE THE SAME AS THE SEAL RING.

LID

LID LENGTH = SEAL RING OD LENGTH - 2E
LID WIDTH = SEAL RING OD WIDTH - 2E
where E = 10 MIN (TYPICAL)
LID RADIUS = 40 + 5 (or same as SEAL RING outside radius)
LID THICKNESS = 15 (TYPICAL)

LID DRAWING NOTES: (TYPICAL)

1. MATERIAL: KOVAR
2. FINISH BURR FREE
3. PLATING SPECIFICATION: 75 MICROINCHES MIN. AU OVER 50 MICROINCHES MIN. NI.

LID SOLDER PREFORM

SOLDER ID LENGTH = SEAL RING ID LENGTH + 2C
SOLDER ID WIDTH = SEAL RING ID WIDTH + 2C
where C = 5 MIN (TYPICAL)
SOLDER OD LENGTH = LID OD LENGTH
SOLDER OD WIDTH = LID OD WIDTH
where D = SOLDER OD - SOLDER ID and should not be less than 35
SOLDER PREFORM THICKNESS IS 3 +/- 0.3 (TYPICAL)

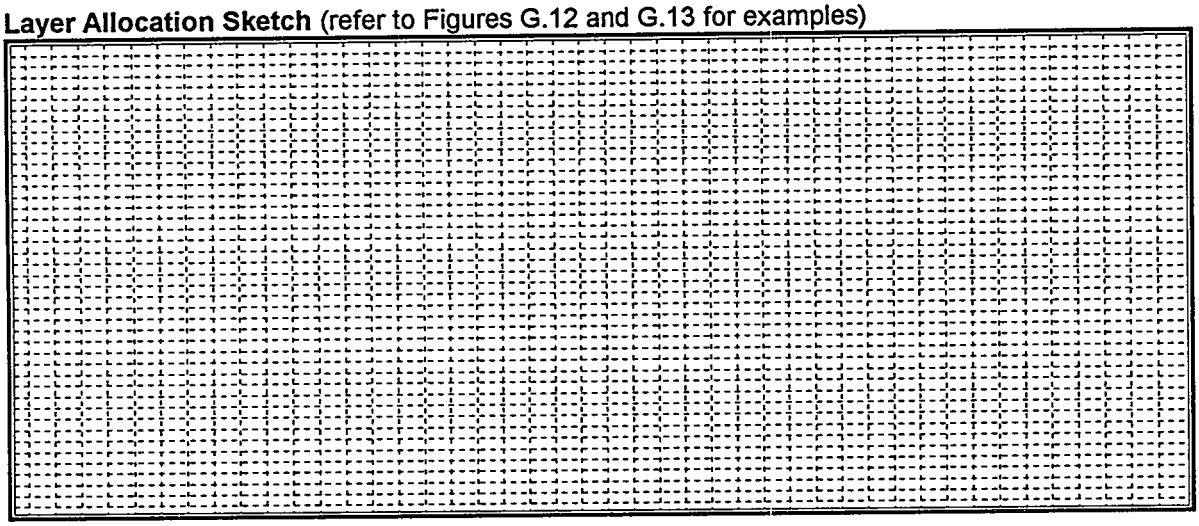
Figure C.2 Seal Ring, Braze Pad and Lid Definition

Date:___/___/___

MCM SUBSTRATE SUMMARY

MCM NAME _____ **PART NUMBER** _____

Layer Allocation Sketch (refer to Figures G.12 and G.13 for examples)



Substrate Specification

Substrate size (length/width/thickness):
Number of tape layers:
Tape thickness and part number:

Conductor Traces

Standard width/spacing (mils):
Special width/spacing (mils):

Electrical Vias

Standard diameter and catch pad (mils):
Special diameter and catch pad (mils):

Thermal Vias

Applicable component:
Via diameter and pitch (mils):

I/O Interface

Number of I/Os:
Pin or lead definition [size and pitch] (mils):

Thick Film Resistors

Total number:
Schematic designators:

Seal Ring Definition (Final layout determines L & W)

Height (mils):

Special Features

Test fiducials:
Wire bond fiducials:
Pin one indicators:

Table C.3 MCM Substrate Summary

Appendix D

ASSEMBLY INFORMATION AND CONSTRAINTS ON DESIGN

The purpose of this appendix is to summarize standard assembly information and constraints that must be considered during the design of any multichip module. The appendix is divided into three sections of one or more tables as itemized below.

Table D.1 **MCM-C Assembly Drawing Checklist**

This assembly checklist provides producibility guidance for the MCM team members during initial MCM design and preparation of drawings.

Table D.2 **Cavity and Component Layout Definition**

Table D.3 **Surface Mount Layout Definition**

These two tables provide design rules for the assembly of MCM-C multichip modules. Preferred dimensions and assembly layout guidelines are provided to optimize the manufacturability and reworkability of the MCM design.

Table D.4 **Substrate Pin, Lead and Seal Ring Attachment**

Table D.5 **Die Attachment**

Table D.6 **Wire Bonding**

Table D.7 **Gold Ribbon Bonding**

Table D.8 **Sealing and Leak Testing**

Table D.9 **Surface Mount Assembly**

These six tables provide the characteristics of available MCM-C assembly and rework processes such as materials, process times and temperatures, and equipment. These characteristics should be reviewed prior to the MCM design to ensure that the resulting design can be manufactured within the envelope of the available processes.

REQUIRED INFORMATION	DATE COMPLETED	DATE TO BE COMPLETED	N/A
MCM Graphic Layout			
Components and circuitry on one or both sides of the substrate			
Die attachment requirements			
Temperature restrictions			
Wire length and loop height restrictions			
Wire diameter requirements			
Wire layout enlargement			
Wire and ribbon requirements			
Component/lid clearance			
Surface mount soldering flag notes			
Solder dispensing flag notes			
Marking requirements			
Static handling flag notes			
Active trimming flag notes			
MCM Material List			
Drawings			
LTCC substrate			
Other substrates			
Epoxy materials			
Eutectic die attach materials			
Wire and ribbon materials			
Solder materials			
MCM final package			
MCM lid			
Components			
MCM Schematic			
Electrical schematic for verification and troubleshooting			

Table D.1 MCM-C Assembly Drawing Checklist

REQUIRED INFORMATION	DATE COMPLETED	DATE TO BE COMPLETED	N/A
MCM Electrical Test Specification			
Electrical requirements			
Electrical test temperatures			
Temperature cycling			
Power burn-in			
Centrifuge test			
Shock and vibration			
MCM operating and storage conditions			
Substrate Graphic Layout			
Substrate dimensions			
Conductor widths and spaces			
Substrate cavity dimensions			
Substrate wire bond pad ledge depth, width and height			
Number of ledges in each cavity			
Double-printed thick film for surface mount soldering			
Substrate solder screen printing requirements			
Alignment marks for automated wire bonding, wire pull testing, component pick-and-place, solder dispensing, and substrate testing			
Seal frame solder attachment materials			
Pin and lead solder attachment materials			
Substrate Material List			
Design Definition			
Substrate materials			
Thick film paste - chip and wire			
Thick film paste - surface mount			
Thin film materials			
Thick film paste - seal frame			
Thick film paste - pins and leads			
Pins, leads, seal rings			
Solder stencil			

Table D.1 MCM-C Assembly Drawing Checklist (cont.)

REQUIRED INFORMATION	DATE COMPLETED	DATE TO BE COMPLETED	N/A
Component Drawings			
Component dimensions - length, width and thickness			
Component wire bond pad dimensions and pitch			
Component materials (Si, GaAs)			
Component topside metallization and passivation			
Component backside metallization and potential			
Die bond pad layout (vendor map)			
Component wire bond pads - gold or aluminum			
Component termination materials compatible with surface mount soldering			
Component storage conditions			
Component Considerations			
Component testing (known good die)			
Component visual inspection			
Component library for future tests and failure analysis			
High-yield components using mature technology			
Commercial-grade component requirements			
Military-grade component requirements			
Part Drawings			
Lid dimensions			
Lid materials and plating conditions			
Lid solder attachment materials			

Table D.1 MCM-C Assembly Drawing Checklist (cont.)

(ALL DIMENSIONS ARE POST-FIRED, EXCEPT WHERE NOTED)
(ALL DIMENSIONS ARE IN MILS EXCEPT WHERE NOTED. 1 MIL = 0.001 INCHES)

	Min/Max Dimension	Typical	Figure Item
Cofired package thickness	60 min		P
LTCC thickness at bottom of cavity	40 min	40	G
Bond wire length [1]	100 max		L
Wire bond pad (Width and Length) [2]	10 min	10	W & 3
Die mounting pad (width and length beyond die) [3]	5 min	10	1
Die edge distance to edge of wire bond pad. Minimun or 2.0 X thickness of die (whichever is greater) ONLY FOR WIRE PADS ON THE SAME LAYER AS DIE PAD	20 min	20	2
Die to die mounting pad spacing	10 min		4
Die bond pad neck down should conform to conductor requirements	Line width min		5
Bond wire angle from die to substrate wire bond pad	30° max		
Wire bond pad spacing	10 min	10	S & 6
Cavity Depth	NA		K
First ledge height = Die height +/- 10 for single ledge or Die height - 10 for multiple ledges			F
Distance from die edge to cavity wall	10 min	20	E
Wire bond pad length (FOR CAVITY DESIGN). B = C - A	15 min		B
Seal ring height (minimum) = Die height (max) - K + M Where: M = Bond wire loop height + 10 min (20 typical) for wire to lid clearance WIRE SIZE: 1 Au / 5 Al Bond wire loop height (typical): 10 / 30	20 min		H
Cavity edge to seal ring (minimum) = H/Tan ϕ	20 min	30	J
Cavity ledge length C = (A + D) + (T/Tan ϕ)		30	C
Where:			
Pad pull back	3 min		A
Bondable pad length	10 min		D
Bond ledge height	one - n LTCC layers		T
Tool angle	70° Wire bonder 60° Integri -Test probe		ϕ

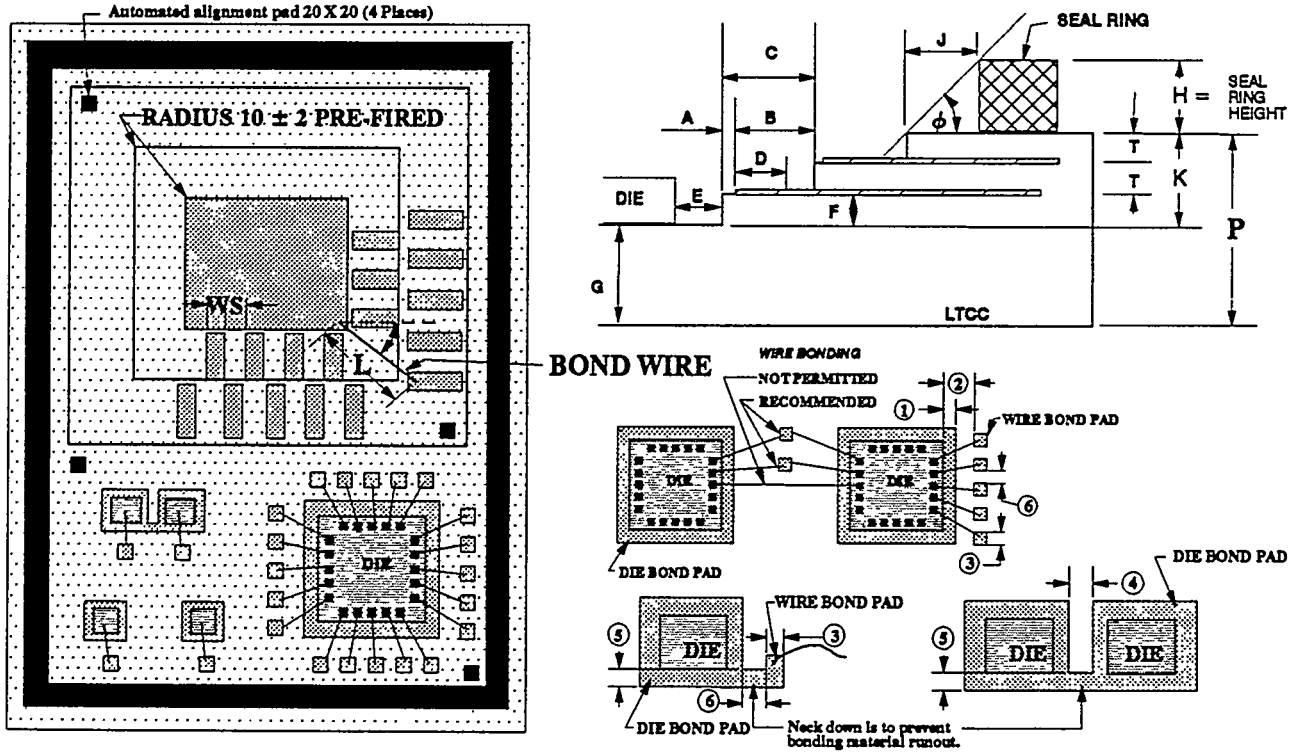


Table D.2 Cavity and Component Layout Definition

Cavity and Component Layout Definition Notes

[1] **Wire Length.** Maximum wire length (bond-to-bond) for high shock or acceleration shall not exceed 80 mils.

[2] **Wire Bond Pads.** Wire bond pads shall be positioned to prevent bonding wires from crossing over semiconductor die, another bonding wire, or exposed conductor line.

A "1" indicator should be placed next to the number one wire bond pad. This indicator will aid the operator during the wire bonding process.

Die-to-die wire bonding is not permitted.

Electrical vias should be located away from the wire bonding area to avoid bonding problem.

For each additional wire bond, increase bond pad 10 mils minimum in direction of bonding.

[3] **Die Mounting Pad.** Die mounting pads are used for epoxy or eutectic bonding of back-bonded semiconductor dice (transistors, diodes and integrated circuits) to the substrate metallization.

When attaching semiconductor die it is important that the correct electrical "potential" be connected to the die mounting pad. That "potential" may be voltage, GND or floating condition.

Table D.2 Cavity and Component Layout Definition (cont.)

(ALL DIMENSIONS ARE POST-FIRED, EXCEPT WHERE NOTED)
(ALL DIMENSIONS ARE IN MILS EXCEPT WHERE NOTED. 1 MIL = 0.001 INCHES)

	Min/Max Dimension	Typical	Figure Item
Chip bond pad [1]			
Chip pad width	22 min	35	1
Pad beyond chip width	10 min	10	2
Pad beyond chip end	10 min	15	3
Chip to pad overlap	12 min	20	4
Chip pad-to-chip pad spacing	10 min	10	5
LCC mounting pads [2]			
Pad width	same as LCC		
Pad length beyond LCC package	20 min	20	6
Nearest conductor	15 min		7
Thick film resistor [3]			
Resistor length	50 min		8
Resistor width	50 min		9
Pad beyond resistor width	10 min	10	10
Resistor to pad overlap	10 min	10	11
Pad beyond resistor end	10 min	20	12
Nearest conductor	15 min		13
Probe Pad (length and width)	20 min	30	14
Distance from seal ring to LCC or chip	20 min	40	

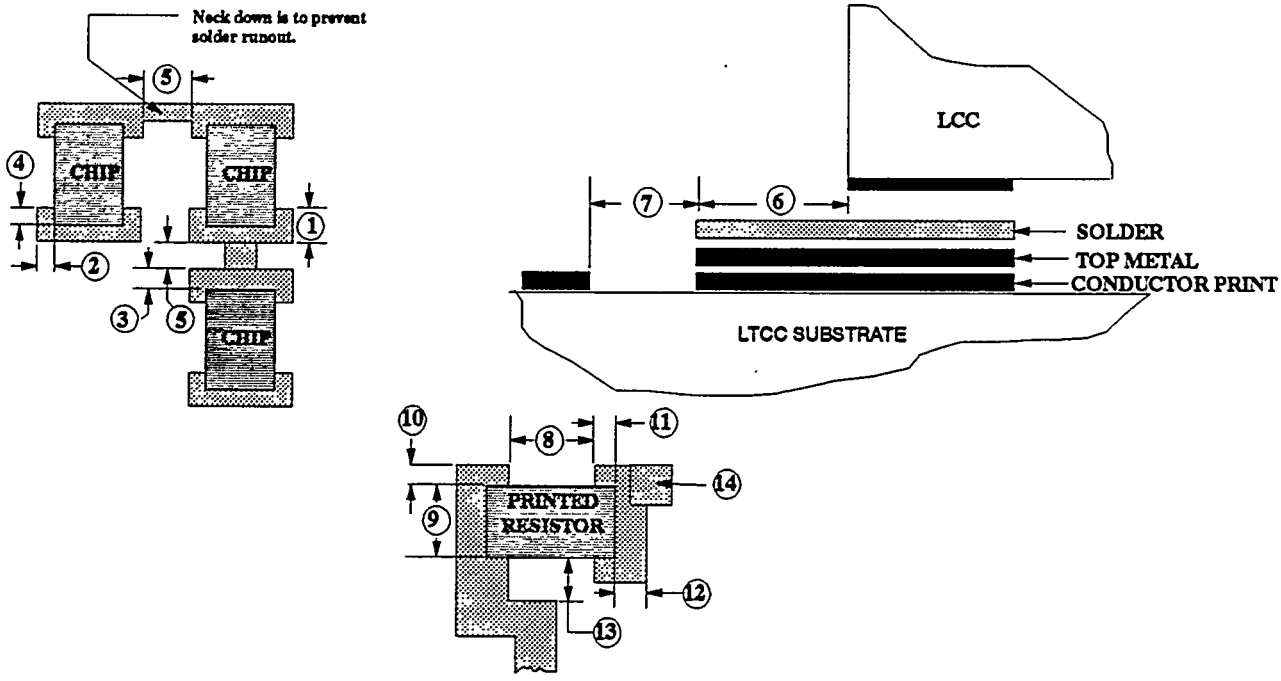


Table D.3 Surface Mount Layout Definition

Surface Mount Layout Definition Notes

[1] **Component Solder Pads.** When circuits are to be assembled using solder techniques, the conductors that receive solder shall be double printed. This double printing makes subsequent soldering operations less critical and provides for enhanced conductor adhesion.

Components requiring orientation should include a notch, where possible, on one component solder pad to aid part installation.

Use nominal component dimensions when designing solder pad geometries. Pad sizes are designed to accept component variations from nominal.

Components with length greater than or equal to 200 mils should use the typical pad dimensions or larger.

Both pads should be the same dimensions to minimize the possibility of component misalignment during the soldering operations.

[2] **LCC Mounting Pads.** It is important to obtain an accurate representation of the LCC metallization pattern.

A "pin one" indicator for an LCC on the substrate is typically a longer solder pad. This uniqueness will aid the operator during the assembly process.

[3] **Thick Film Resistors.** There are three basic considerations in designing a thick film resistor: 1) the resistance value, 2) the power dissipation required, and 3) the allowable resistance tolerance. The resistor value is influenced by its length-to-width ratio, and the power dissipation is a function of the resistor area.

All resistors that are to be trimmed to value must have associated probe pads. Other resistors that do not require trimming should still have associated probe pads, if practical, since such resistors still must be probed to check if they are within specified resistance limits.

When the schematic design includes parallel resistors (for example, resistor loops), a break in an associated substrate conductor trace shall be provided to establish independence among such resistors for resistor trimming. The break is closed later during MCM assembly by bridging with bond wire.

Table D.3 Surface Mount Layout Definition (cont.)

	ASSEMBLY				REWORK		
PROCESS	MATERIAL	PROCESS TIME/TEMP	EQUIPMENT		REWORK-ABILITY	PROCESS TIME/TEMP	EQUIPMENT
Pin/Lead Attachment[1]	80/20 AuSn	280°C liquid, 350°C max., 20 minute cycle	Belt furnace		No solder rework; repairable by conductive epoxy[2]	Epoxy repair Replace: 160°C, 75 minutes	Epoxy repair Heated workstage, tweezers, microneedle, microknife; manual attachment; oven cure
Seal Ring Attachment[1]	80/20 AuSn; AuSnAgCu	Same as above	Same as above		Same as above	Same as above	Same as above

1 - Pins, leads and seal rings are typically Kovar with nickel and gold plating.

2 - Pins and leads repaired with conductive epoxy will provide electrical functionality but will not exhibit the same pull strength as the original soldered pins and leads. Seal rings repaired with epoxy will not provide the same hermeticity as the original soldered seal rings.

Table D.4 Substrate Pin, Lead and Seal Ring Attachment

	ASSEMBLY			REWORK		
PROCESS	MATERIAL	PROCESS TIME/TEMP	EQUIPMENT	REWORK-ABILITY	PROCESS TIME/TEMP	EQUIPMENT
Epoxy Attach[1]	Conductive or nonconductive paste (1-3 mils) or film (3 mils)	160°C, 75 minutes	Manual attachment: tweezers, microneedle, microknife; automated component pick-and-place; oven cure	Yes	Remove 200°C, 5 minutes Replace See Assembly	Heated workstage, tweezers; manual removal and attachment; oven cure
Thermoplastic Adhesive Attachment[1]	Conductive or nonconductive paste (1-3 mils) or film (3 mils)	As specified in vendor data sheet; typical temperature range 150°C - 350°C	Manual attachment: vacuum pencil, tweezers, microneedle, microknife; hot plate, oven, or die bonder	Yes	Remove As specified in vendor data sheet; typical temperature range 150°C - 250°C minimum Replace See Assembly	Hot plate, tweezers; manual removal and replacement

Table D.5 Die Attachment

	ASSEMBLY				REWORK		
PROCESS	MATERIAL	PROCESS TIME/TEMP	EQUIPMENT		REWORK-ABILITY	PROCESS TIME/TEMP	EQUIPMENT
Eutectic Die Attach[2,3]	Preforms (1 mil) Gold: phosphorus - doped (N-type); boron-doped (P-type)	Workstage: 410°C; collet: 200°C; scrub: 9 mils; bond time: 9 sec; hot plate cool down: 30 sec minimum	Eutectic die bonder		No		

1 - **Via posts.** Cofired substrate thermal via posts can affect die attachment by creating unlevel surfaces under the die. The design layout and substrate fabrication should exclude via posts in die attachment areas if possible; if not, such vias should be symmetrically located under the die.

2 - Eutectic die bonding is suitable for ceramic packages with plated gold or substrates with thin film gold. The backside of the die must be appropriately metallized so that it is compatible with the eutectic solder. Eutectic die bonding is not currently available for thick film substrates including cofired substrates.

3 - The maximum die size is restricted to 250 x 250 mils. The eutectic die bond pad on the substrate shall be 50% larger than the die in both length and width to permit space for scrubbing the die during attachment.

Table D.5 Die Attachment (cont.)

	ASSEMBLY			REWORK		
PROCESS	**MATERIAL**	**PROCESS TIME/TEMP**	**EQUIPMENT**	**REWORK-ABILITY**	**PROCESS TIME/TEMP**	**EQUIPMENT**
Thermosonic Gold Wire Bonding[1]	Gold Wire Sizes (mils): 0.7, 1.0, and 2.0 diameter wire and 1 x 3 ribbon Currents:[2]	Workstage temperature: 160°C - 200°C; bond time: automated ball/wedge - 100 wires/min; manual ball/wedge or wedge/wedge - 2 wires/min.	Thermosonic gold wire bonders: automated ball/wedge;[3] manual ball/wedge;[4] manual wedge/wedge[5]	Yes: wedge bonds on substrate; no: ball or wedge bonds on component; preferred: replace component and rebond	See Assembly	See Assembly
Ultrasonic Aluminum Wire Bonding[6]	Aluminum wire Sizes (mils): 1, 2, 5 - 15; note: 5 - 15 mil wire for development applications only Currents:[7]	Workstage temp: ambient; force: 30 g; time: 30msec; energy: variable; bond time: automated - 100 wires/min; manual - 2 wires/min.	Ultrasonic aluminum wire bonders:[8] automated wedge/wedge; manual wedge/wedge	Yes : limited rework of wedge bonds on component if space allows; limited rework of wedge bonds on package or substrate	See Assembly	See Assembly

1 - Cofired substrate via posts and sloped ledges in gold wire bonding areas can cause unacceptable wedge bonds, both electrically and mechanically. Electrical vias should be located outside of wire bonding areas as described in Table D.2.

2 - **Gold Wire/Ribbon Maximum Current** (Reference: Mil-M-38510J, Paragraph 3.5.5.3)

Gold Wire/Ribbon Size	Wire Length < 40 mils	Wire Length > 40 mils
0.7 mil dia.	0.56 A	0.38 A
1.0 mil dia.	0.95 A	0.65 A
2.0 mils dia.	2.7 A	1.8 A
1 x 3 mils	2.6 A	1.8 A

Table D.6 Wire Bonding

3 - **Automated Ball/Wedge Bonder.** The maximum substrate size is 2.25 x 2.25 inches. The bonder is set up for 1-mil-diameter gold wire. The maximum wire bonding depth is 250 mils as measured from the lowest wire bond pad (substrate or die) to the top of the seal ring. Component bond pads can be gold or aluminum. The minimum component bond pad size is 4 x 4 mils with 5-mil pitch. PGA pin and cantilevered lead layouts are restricted by the bonder tool and workstage and must be reviewed by the assembly engineer. The bonder workstage will accept an MCM with a PGA designed on 100-mil centers on the backside of the substrate. PGA pins or cantilevered leads are restricted to two opposite sides when located on the wire bond side of the substrate.

4 - **Manual Ball/Wedge Bonder.** The maximum substrate size is 4.0 x 4.0 inches. The bonder is set up for 1-mil-diameter gold wire. The maximum wire bonding depth is 250 mils as measured from the lowest wire bond pad (substrate or die) to the top of the seal ring. Component bond pads can be gold or aluminum. The minimum component bond pad size is 4 x 4 mils with 5-mil pitch. PGA pin and cantilevered lead layouts are restricted by the bonder tool and workstage and must be reviewed by the assembly engineer. The bonder workstage must first be modified before bonding to an MCM with a PGA designed on the backside of the substrate. Pins are acceptable on two opposite sides, and cantilevered leads are acceptable on up to four sides of the wire bond side of the substrate.

5 - **Manual Wedge/Wedge Bonder.** The maximum substrate size is 2.25 x 2.25 inches. The bonder is set up for 1-mil-diameter gold wire. Other possible gold wire and ribbon sizes include 0.7 mil, 2 mils, 1 x 3 mils, and up to 1 x 10 mils; however, new bond tools and schedules will be required. The maximum wire bonding depth is 500 mils as measured from the lowest wire bond pad (substrate or die) to the top of the seal ring. The component bond pads must be gold. The minimum component bond pad size is 2 x 2 mils with 3-mil pitch. PGA pin and cantilevered lead layouts are restricted by the bonder tool and workstage and must be reviewed by the assembly engineer. The bonder workstage must first be modified before bonding to an MCM with a PGA designed on the backside of the substrate. PGA pins are acceptable on two opposite sides, and cantilevered leads are acceptable on up to four sides of the wire bond side of the substrate.

6 - Ultrasonic aluminum wire bonding is suitable for ceramic packages with plated gold or carrier substrates with thin film gold.

7 - **Aluminum Wire Maximum Current** (Reference: Mil-M-38510J, Paragraph 3.5.5.3)

Aluminum Wire Size	Wire Length < 40 mils	Wire Length > 40 mils
1 mil dia.	0.70 A	0.48 A
2 mils dia.	2.0 A	1.4 A
5 mils dia.	7.8 A	5.4 A

8 - **Aluminum Wire Bonders.** The maximum substrate size is 2.0 x 2.0 inches. The typical wire bonding depth from the seal ring to the bottom of the package is 50 mils. The typical distance from the package post to the bottom of the package is 30 mils. The typical die thickness is 5 to 10 mils. The component bond pad metallization must be aluminum. The minimum component bond pad size is 3 x 3 mils with 4-mil pitch. A special workholder is required for MCM designs with PGA pins or cantilevered leads.

Table D.6 Wire Bonding (cont.)

	ASSEMBLY			REWORK		
PROCESS	MATERIAL	PROCESS TIME/TEMP	EQUIPMENT	REWORK-ABILITY	PROCESS TIME/TEMP	EQUIPMENT
Gold Ribbon Bonding[1]	Gold Ribbon Sizes (mils):[2] 2 x 5, 2 x 10, 3 x 20, 3 x 25 Currents:[3]	Interface temperature: 200 - 250°C; bond time: 1 - 2 seconds per bond; bond force: 400 - 1250 g	Manual ribbon bonders:[4]	Limited rework; cut ribbon, scrape bond from substrate, and rebond	See Assembly	See Assembly

1 - Cofired substrate via posts in ribbon bonding areas can cause unacceptable ribbon bonds, both electrically and mechanically. Electrical vias should be located outside of ribbon bonding areas.

2 - Thin film metallization is more suitable for gold ribbon bonding than thick film. The maximum ribbon size recommended for bonding to thick film metallization is 2 x 10 mils. Other ribbon sizes such as 1 x 3 mils and up to 1 x 10 mils are available if used with the gold wedge bonder (see Table D.6).

3 - **Gold Ribbon Maximum Current** (Reference: Mil-M-38510J, Paragraph 3.5.5.3)

Gold Ribbon Size	Ribbon Length < 40 mils	Ribbon Length > 40 mils
2 x 5 mils	6.4 A	4.4 A
2 x 10 mils	11 A	7.4 A
3 x 20 mils	24 A	17 A
3 x 25 mils	29 A	20 A

4 - The maximum substrate or package size is 2.5 x 2.5 inches. The maximum ribbon bonding depth is 200 mils as measured from the lowest ribbon bond pad (substrate or die) to the top of the seal ring. The bonder workstage will accept substrates or packages with flat bottoms. A special workholder is required for MCMs with PGA designs.

Table D.7 Gold Ribbon Bonding

	ASSEMBLY				REWORK		
PROCESS	MATERIAL	PROCESS TIME/TEMP	EQUIPMENT		REWORK-ABILITY	PROCESS TIME/TEMP	EQUIPMENT
Heated Platen Sealing[1]	Gold and nickel plated Kovar lid with 80/20 AuSn solder preform	Lid/seal ring interface is estimated 350°C. Typical sealing schedule[2]	Heated Platen Sealer		Limited rework, development parts only; normal rework, new package	See Assembly	See Assembly
Belt Sealing[3]	Gold and nickel plated Kovar lid with 80/20 AuSn solder preform	80/20 AuSn: 280°C liquid, 350°C max., 20-minute cycle	Belt Furnace		No rework, new package		
Fine Leak Testing[4]	Helium	Pressurized per MIL-STD-883D, Method 1014	Mass spectrometer leak detector		Retest	See Assembly	See Assembly
Gross Leak Testing[4]	Nitrogen; Fluorinert	Pressurized per MIL-STD-883D, Method 1014; Fluorinert - 1 minute, 125°C	Gross leak tester; bubble tester		Retest	See Assembly	See Assembly

1 - The Heated Platen Sealer is used to hermetically seal cofired MCM substrates and metal packages that contain epoxy-attached components. The maximum substrate or package size is restricted to 2.5 x 2.5 inches. One lid is recommended for sealing MCMs that contain multiple component cavities. Special tooling is required for MCMs with PGA pins designed on the backside of the substrate.

2 - **Heated Platen Sealing Schedule.** All MCMs are vacuum baked at 150°C for 16 hours prior to sealing. Then, the typical MCM sealing schedule includes four steps:
1) vacuum pre-soak time of 30 seconds with heater set at 250°C,
2) ramp-up time of 45 seconds,
3) dwell time of 30 seconds with heater set at 425°C, and
4) cool-down time of 15 seconds.

3 - The belt furnace is used to hermetically seal ceramic packages such as LCCs that contain eutectically-attached components. The maximum package size is restricted to 3.0 x 3.0 inches.

4 - The maximum MCM or package size for fine and gross leak testing is 3.0 x 3.0 x 0.75 inches.

Table D.8 Sealing and Leak Testing

	ASSEMBLY			REWORK		
PROCESS	MATERIAL	PROCESS TIME/TEMP	EQUIPMENT	REWORK-ABILITY	PROCESS TIME/TEMP	EQUIPMENT
Surface Mount Reflow Soldering[1]	Solder: 63/37 SnPb; thick film minimum: double-printed PtAu	Vapor phase 63/37 SnPb, 180°C liquid, 220°C max. for 1-1.5 minutes, 3-4 min. cycle Convection Same as vapor phase except 5-6 min. cycle	Vapor Phase; Convection	Yes	Hot air rework 230 - 250°C; Solder iron and hot plate rework solder iron: 370°C (700°F); hot plate: 130°C	Hot air equipment; hot plate

1 - The maximum substrate size for surface mount soldering is 6 x 10 x 1 inches. Component termination materials must be compatible with 63/37 SnPb solder. Edge clips are an option for cantilevered leads for MCMs and are soldered during surface mount assembly. Prior to surface mount assembly, solder is applied to the substrate component pads by one of three methods: 1) solder dispensing, 2) solder printing, or 3) solder preforms. The 63/37 SnPb solder paste is applied at ambient temperature during dispensing. During solder printing, the MCMs are processed through a 10-minute cycle where temperatures range from 180°C to a maximum of 210 to 235°C. Solder preforms are applied manually at ambient temperature prior to surface mount soldering.

Table D.9 Surface Mount Assembly

Appendix E

TESTING CONSTRAINTS ON DESIGN

The MCM design engineer should develop an MCM test plan concurrently with the module design, and the test equipment engineer should conduct an in-depth review of the plan with recommended changes submitted to the MCM designer. This plan must define all tests required to ensure module functionality and the preferred methods and sequences of tests. The following checklist of items or activities details information that forms the basis of the test plan and the required test equipment.

Table E.1 Test Plan Checklist

REQUIRED INFORMATION	DATE SUPPLIED	DATE TO BE SUPPLIED	N/A
PHYSICAL INFORMATION			
Pin/lead definition & locations			
Size (L x W x T)			
MCM z profile			
Alignment and orientation features			
Mechanical fragility			
Probe accessibility			
Spring-loaded probes (nodes on bottom preferred)			
Needle probes (nodes on top required)			
Coplanar/dual probes (nodes on top required)			
E-beam probes (nodes on one surface required)			
ENVIRONMENTAL INFORMATION			
Temperature range & soak time			
Heat dissipation required			
Shock & vibration			
FUNCTIONAL INFORMATION			
I/O definition / pin assignment			
Definition of test nodes			
Definition of component nodes (single or dual probing)			
Sequence of tests			
Stimuli definition (V, I, F, Z_S, loads, guarding)			
Measurement definition (V, I, F, Z_M, timing, guarding, sampling rates)			
Initial setup			
Expected measurement values & limits			
OTHER INFORMATION			
Static sensitivity			
Classification level			
Quantity			
BIST & boundary scan considered to simplify overall testing			

Table E.1 Test Plan Checklist

Appendix F

MCM-C COMPONENT PROCUREMENT AND ENGINEERING

This appendix is designed to help MCM design engineers develop definition of particular components for their applications. The appendix consists of three tables as itemized below.

Table F.1 General Component Considerations

This table presents some general considerations dealing with KCD Component Engineering and component quality requirements contingent on product application. It also itemizes desirable component drawing content and a number of considerations which should be examined when selecting any component. The table concludes by emphasizing the value of concurrent engineering between the MCM design engineer and the component engineer.

Table F.2 MCM Die Component/Assembly Summary

This table consists of a combined die component and die assembly summary sheet that can be expanded to multiple pages as required. As each die device is selected and incorporated into the MCM design, the die and assembly specifics should be documented by completing the listed information of the summary table.

Table F.3 MCM Surface Mount Component/Assembly Summary

This table is similar to Table F.2, except its focus is summarizing the device and assembly specifics of the selected surface mount devices.

Component-related acronyms listed below but not in section 1.2.

ACRONYMS

CVR	current viewing resistor
DIP	dual in-line package
DPA	destructive physical analysis
HMC	hybrid microcircuit
IC	integrated circuit
JFET	junction field effect transistor
LCCA	leadless chip carrier assembly
MMIC	monolithic microwave integrated circuit
MOSFET	metal oxide semiconductor field effect transistor
NTC	negative temperature coefficient
PIN	positive-intrinsic-negative
PPT	purchased product team
PTC	positive temperature coefficient
QC-1	quality criteria (document)
RF	radio frequency

KCD Components Engineering receives primary direction and control from DOE document, QC-1. The QC-1 document describes the responsibilities and duties of Components Engineering in substantial detail.

It is common for Components Engineering, Purchasing, and Quality Engineering to form a PPT (Purchased Product Team - the primary constituents). The responsibilities of this team are to ensure that all the requirements of QC-1 and KCD procedures and goals are satisfied. These requirements cause KCD to establish partnerships with suppliers for long-term relationships.

QC-1 stipulates many controls that regulate both KCD and our suppliers including provisions for DOE auditing. KCD has responded by defining different levels of supplier certification. The PPT will use these different levels of supplier classification and institute PC&C (process capability & control) accordingly.

Whether prototype or product, the design and component engineers need to be cognizant of the following areas:

Component Drawings
- Schematic Functional Properties
- Dimensions
- Pad dimensions, function, pitch
- Materials
- Topside metallization/passivation
- Backside metallization/potential
- Solderability
- Shipping, handling, storage

Component Considerations
- Component maturity (yield)
- Known good die strategies
- Component testing
- Visual inspection
- Commercial-grade requirements
- Military-grade requirements
- Quantities
  - MCM build
  - Manufacturing preparations
  - Testing preparations
  - Assembly attrition
  - Characterization

Table F.1 General Component Considerations

DATE:___/___/___

MCM DIE COMPONENT/ASSEMBLY SUMMARY

MCM NAME _____

PART NUMBER _____

COMPONENT NAME:
PART NUMBER:
SUPPLIER:
SCHEMATIC DESIGNATOR:
FUNCTIONAL DESCRIPTION:
DIE TECHNOLOGY:
DIE POWER DISSIPATION:
DIE OPERATING FREQUENCY:
DIE BACKSIDE MATERIAL AND BIAS POTENTIAL:
DIE SIZE (length/width/thickness):
DIE WIRE BOND PAD (length/width/pitch):
DIE WIRE BOND PAD MATERIAL:
DIE ATTACHMENT MATERIAL AND NOMINAL THICKNESS:
SUBSTRATE WIRE BOND PAD (length/width/pitch):
BOND WIRE MATERIAL AND SIZE:
QUANTITY/COST/DELIVERY:

COMPONENT NAME:
PART NUMBER:
SUPPLIER:
SCHEMATIC DESIGNATOR:
FUNCTIONAL DESCRIPTION:
DIE TECHNOLOGY:
DIE POWER DISSIPATION:
DIE OPERATING FREQUENCY:
DIE BACKSIDE MATERIAL AND BIAS POTENTIAL:
DIE SIZE (length/width/thickness):
DIE WIRE BOND PAD (length/width/pitch):
DIE WIRE BOND PAD MATERIAL:
DIE ATTACHMENT MATERIAL AND NOMINAL THICKNESS:
SUBSTRATE WIRE BOND PAD (length/width/pitch):
BOND WIRE MATERIAL AND SIZE:
QUANTITY/COST/DELIVERY:

PAGE ___ OF ___

Table F.2 MCM Die Component/Assembly Summary

DATE:___/___/___

MCM SURFACE MOUNT COMPONENT/ASSEMBLY SUMMARY

MCM NAME ____________

PART NUMBER __________

COMPONENT NAME:	
PART NUMBER:	
SUPPLIER:	
SCHEMATIC DESIGNATOR:	
FUNCTIONAL DESCRIPTION:	
POWER DISSIPATION:	
OPERATING FREQUENCY:	
SIZE (length/width/thickness):	
SOLDER PAD (length/width/pitch):	
SOLDER ATTACHMENT MATERIAL:	
TERMINATING METALLIZATION:	
QUANTITY/COST/DELIVERY:	

COMPONENT NAME:	
PART NUMBER:	
SUPPLIER:	
SCHEMATIC DESIGNATOR:	
FUNCTIONAL DESCRIPTION:	
POWER DISSIPATION:	
OPERATING FREQUENCY:	
SIZE (length/width/thickness):	
SOLDER PAD (length/width/pitch):	
SOLDER ATTACHMENT MATERIAL:	
TERMINATING METALLIZATION:	
QUANTITY/COST/DELIVERY:	

COMPONENT NAME:	
PART NUMBER:	
SUPPLIER:	
SCHEMATIC DESIGNATOR:	
FUNCTIONAL DESCRIPTION:	
POWER DISSIPATION:	
OPERATING FREQUENCY:	
SIZE (length/width/thickness):	
SOLDER PAD (length/width/pitch):	
SOLDER ATTACHMENT MATERIAL:	
TERMINATING METALLIZATION:	
QUANTITY/COST/DELIVERY:	

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Table F.3 MCM Surface Mount Component/Assembly Summary

Appendix G

MCM-C DESIGN EXAMPLES

The purpose of this appendix is to present examples of some of the MCM-C layouts designed by KCD. These examples (listed below) are taken from three different MCM designs: the high-speed Digital Waveform Synthesizer (DWS), the high-density digital Processor Module (PM), and the Input/Output Module (IOM).

DWS MCM

PM MCM

IOM MCM

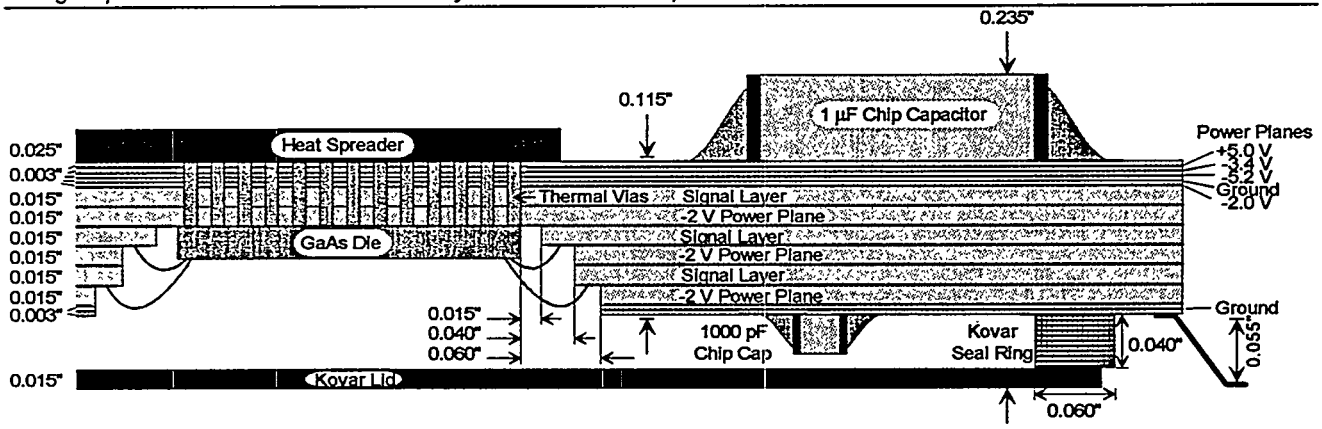
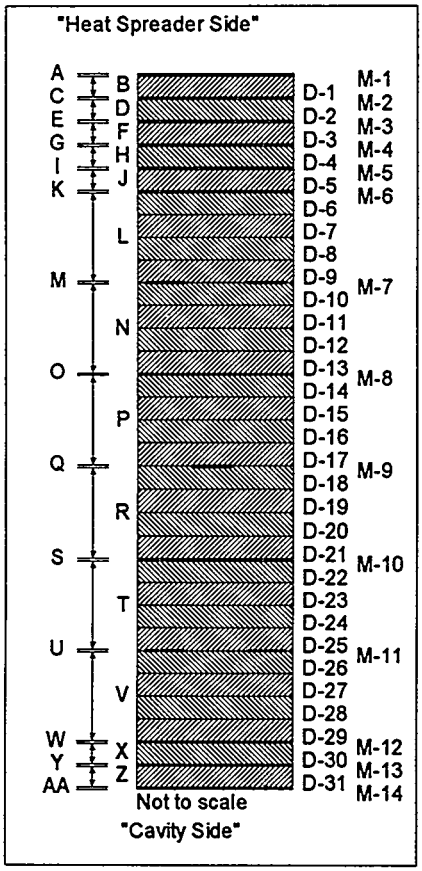


Figure G.1 DWS - Packaging Cross-Sectional View

Waveform Synthesizer Substrate Stackup



Layer	Function		Thickness (mils)
A	Surface Mount/Heat Spreader Layer	M-1	0.5
B	1st Dielectric Layer	D-1	3.7
C	+5.0 V Power Plane	M-2	0.5
D	2nd Dielectric Layer	D-2	3.7
E	-3.4 V Power Plane	M-3	0.5
F	3rd Dielectric Layer	D-3	3.7
G	-5.2 V Power Plane	M-4	0.5
H	4th Dielectric Layer	D-4	3.7
I	Ground Plane	M-5	0.5
J	5th Dielectric Layer	D-5	3.7
K	-2.0 V Power Plane	M-6	0.5
L	6th Dielectric Layer	D-6,7,8,9	3.7+3.7+3.7+3.7
M	Signal Layer	M-7	0.5
N	7th Dielectric Layer	D-10,11,12,13	3.7+3.7+3.7+3.7
O	-2.0 V Power Plane	M-8	0.5
P	8th Dielectric Layer	D-14,15,16,17	3.7+3.7+3.7+3.7
Q	Signal Layer	M-9	0.5
R	9th Dielectric Layer	D-18,19,20,21	3.7+3.7+3.7+3.7
S	-2.0 V Power Plane	M-10	0.5
T	10th Dielectric Layer	D-22,23,24,25	3.7+3.7+3.7+3.7
U	Signal Layer	M-11	0.5
V	11th Dielectric Layer	D-26,27,28,29	3.7+3.7+3.7+3.7
W	-2.0 V Power Plane	M-12	0.5
X	12th Dielectric Layer	D-30	3.7
Y	Ground Plane	M-13	0.5
Z	13th Dielectric Layer	D-31	3.7
AA	Surface Mount Layer	M-14	0.5

Table G.1 DWS - Substrate Layer Allocation

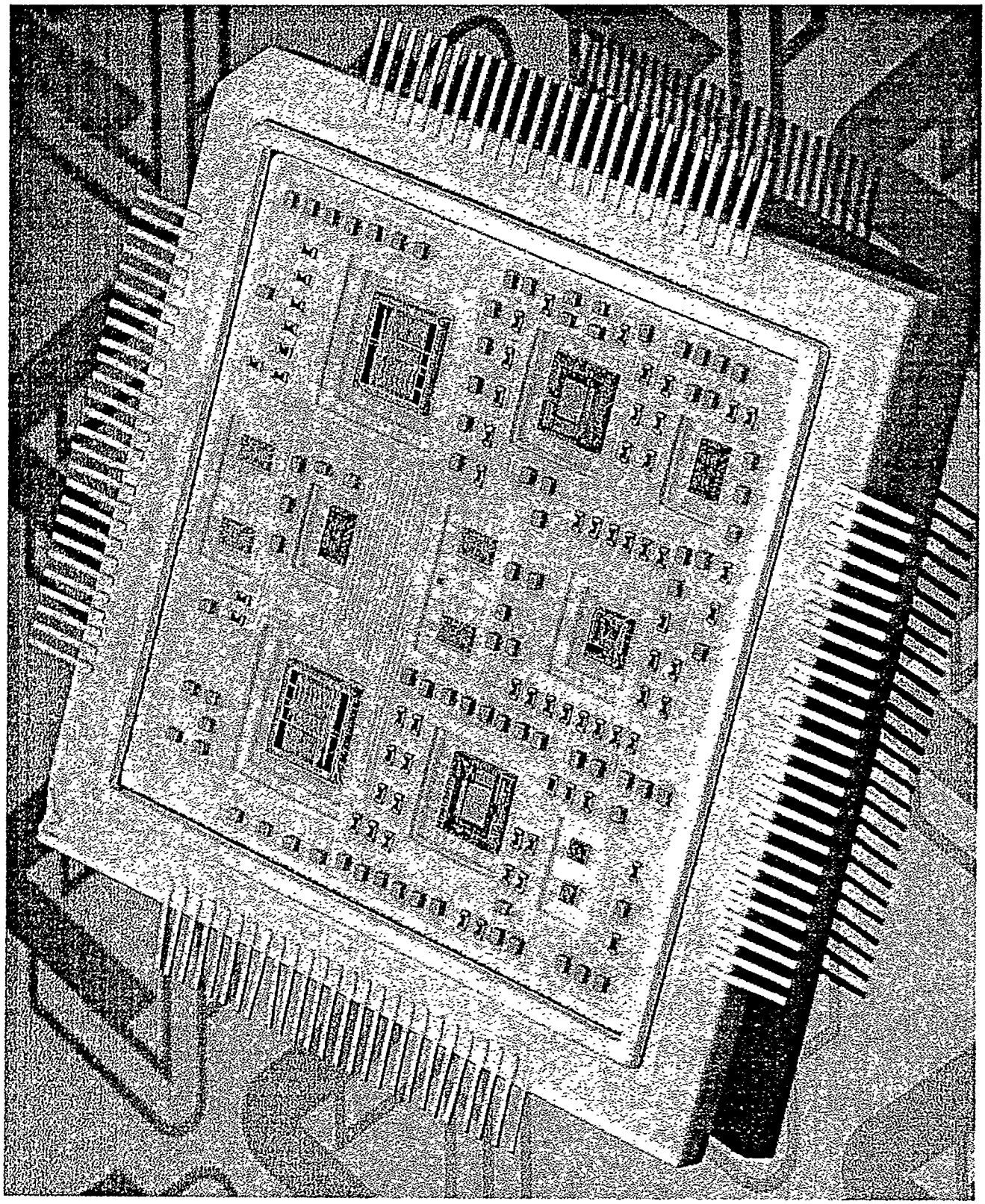


Figure G.2. DWS -- Photograph with Open Cavity

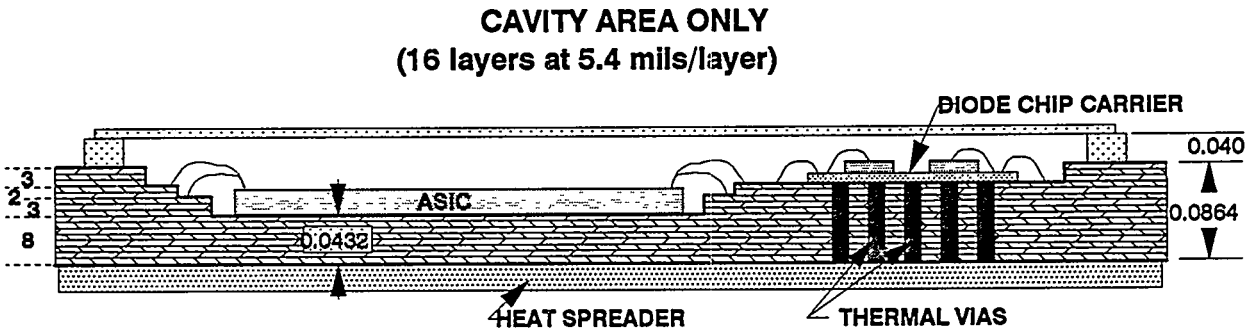


Figure G.3 PM - Package Cross-Sectional View

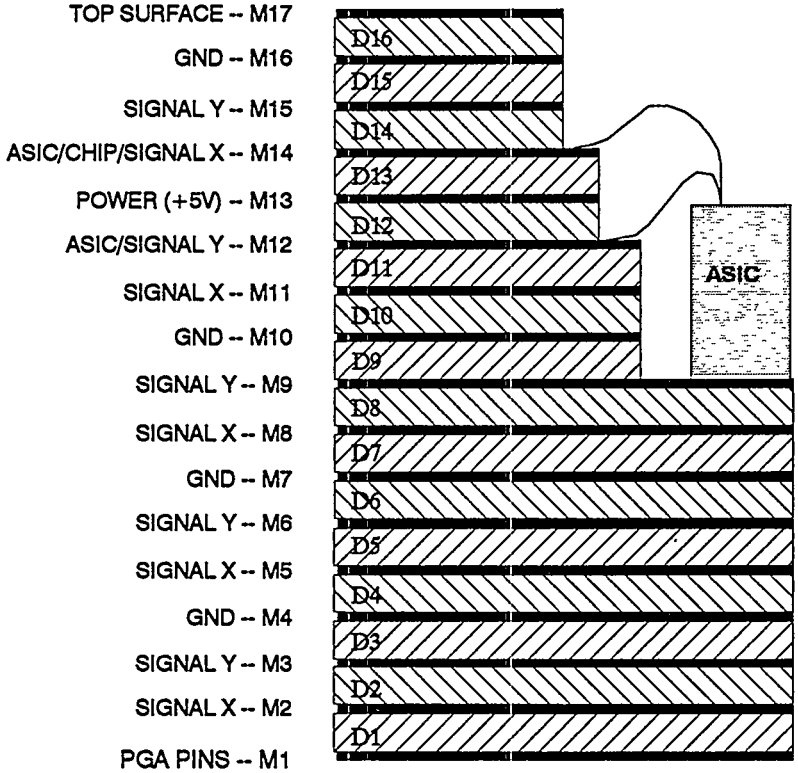


Figure G.4 PM - Substrate Layer Allocation

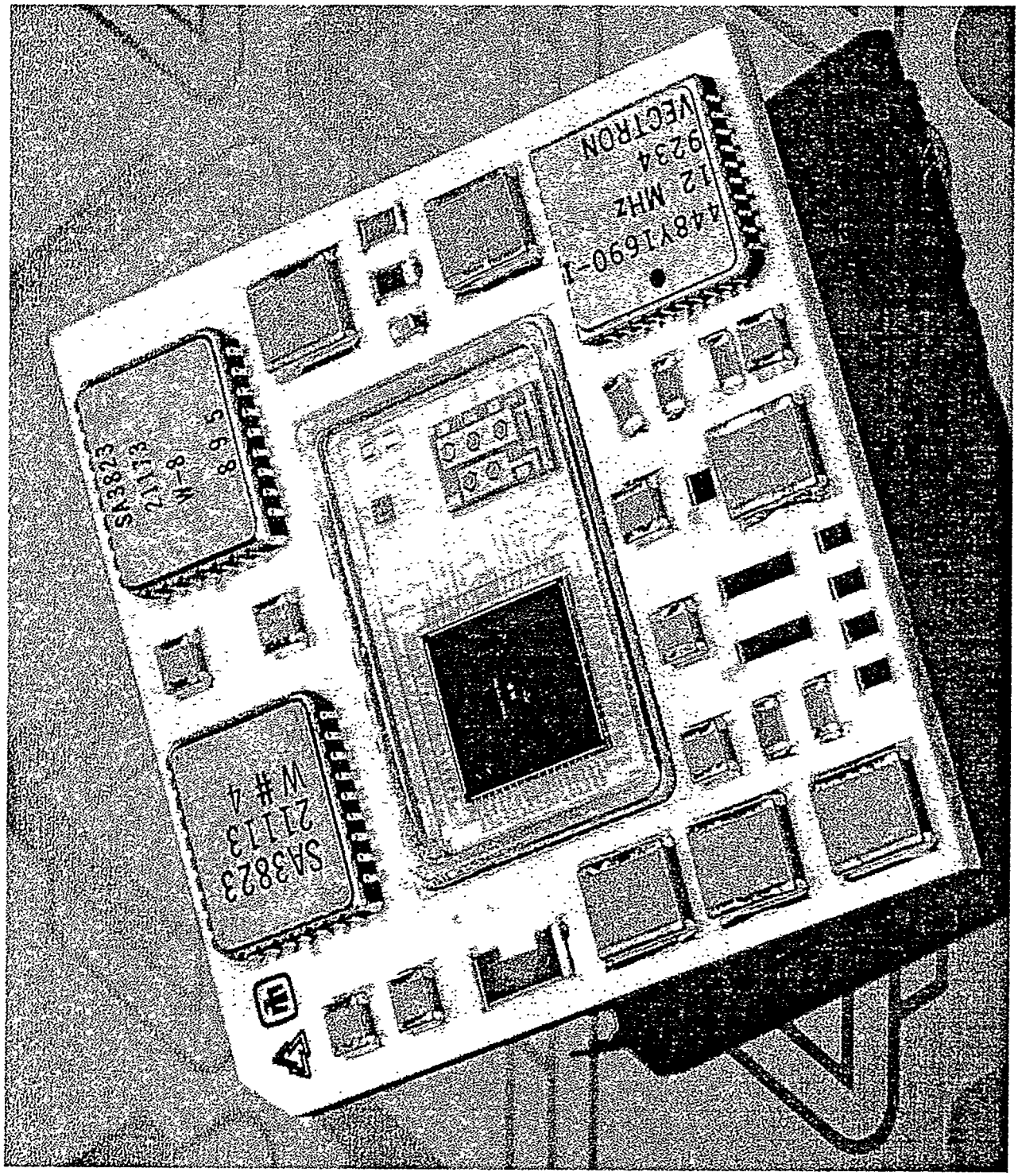


Figure G.5 PM - Photograph with Open Cavity

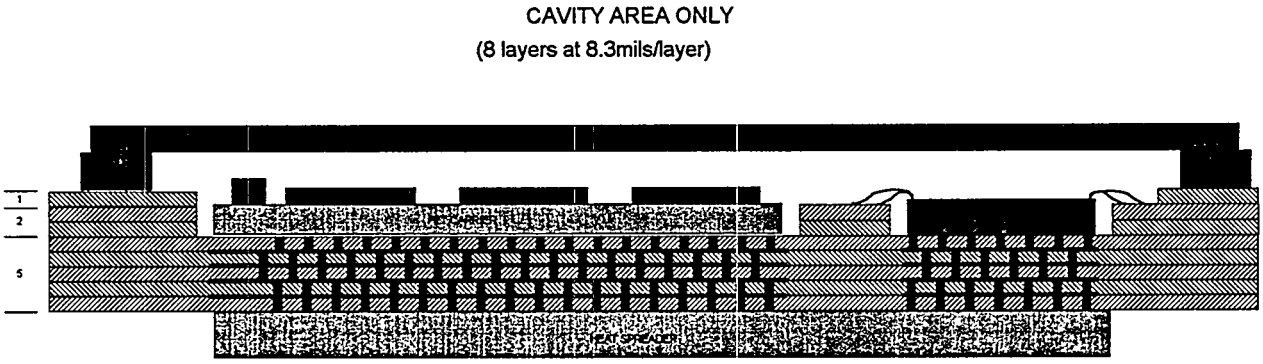


Figure G.6 IOM - Package Cross-Sectional View

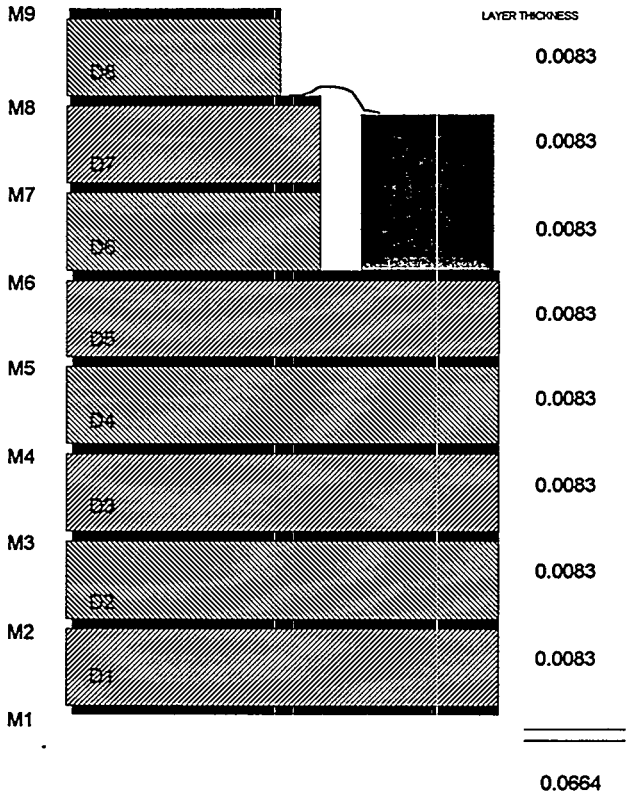


Figure G.7 IOM - Substrate Layer Allocation

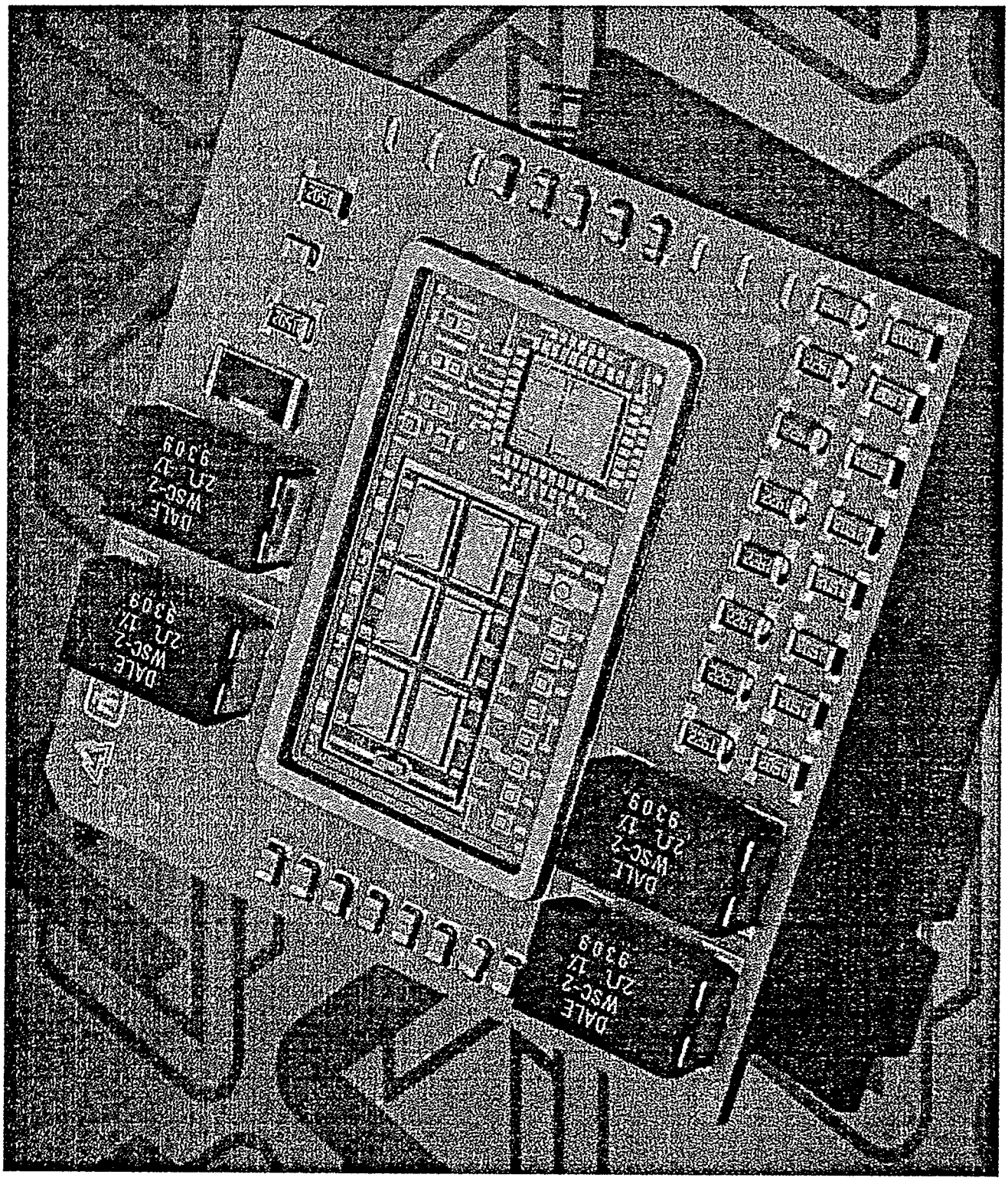


Figure G.8 IOM - Photograph with Open Cavity