

Research on High-Efficiency, Large-Area CuInSe₂-Based Thin-Film Modules

Final Subcontract Report
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Preface

Siemens Solar Industries (SSI) has pursued the research and development of CuInSe₂ (CIS) thin film PV technology since 1980. Prior to the contract, SSI had demonstrated a 14.1% efficient 3.4 cm² active-area ZnO/thin CdS/CIS/Mo/glass cell, unencapsulated integrated modules with aperture efficiencies of 11.2% on 940 cm² and 9.1% on 3900 cm² and an encapsulated module with 8.7% on 3883 cm² (verified by NREL).

The objective of this contract (No. ZN-1-19019-5) was to achieve progress toward the polycrystalline thin-film milestones of the DOE Five Year Plan. SSI began this 3-year, 3-phase cost-shared contract on May 1, 1991 with the overall project goal of fabricating a large area, stable, 12.5% aperture efficient encapsulated CIS module by scalable, low-cost techniques on inexpensive substrates. This document is the final contract report.

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Summary

Demonstrated encapsulated module efficiencies (encapsulated 12.8% efficient mini-module on 68.9 cm² and an NREL-verified 12.7% efficient unencapsulated circuit on 69 cm² with a prismatic cover) are the highest reported mini-module efficiencies for any thin film technology. A champion large area (3860 cm²) encapsulated module efficiency of 10.3% has also been demonstrated (verified by NREL). This is the first thin film module of its size to exceed the 10% efficiency level. SSI also supplied NREL with a one kilowatt array of large area (~3890 cm²) approximately 30 watt modules. The NREL verified performance of this array is a significant step toward meeting the efficiency target of the U.S. DOE Five-Year Plan Goals of 8-10% efficient commercial thin film flat plate modules.

Long term outdoor stability of CIS and CIS-based absorbers has been demonstrated by testing at NREL. Excellent stability has been demonstrated for six years of outdoor exposure. Stability of the 1 kW Siemens CIS array installed and tested at NREL has also been demonstrated for an exposure of approximately one year.

The major challenge to move from development to production is to improve reproducibility rather than to improve champion device performance. Therefore, current emphasis has been placed on reduction of process variation. These continuing reduction of variation efforts are based on the application of the statistical process control (SPC) discipline, improved diagnostics, and thorough protocols. Implementation of SPC techniques has been used to identify major sources of process variation and to successfully reduce this variation. Reduction of variation efforts have also accelerated progress in other tasks by providing a consistent and well defined baseline process.

The foundations have been laid to meet the thin-film milestones of the DOE Five Year Plan. Outdoor testing has demonstrated excellent intrinsic module stability. Future plans include scaling these results to larger areas and emphasizing the reduction of variation methodology to lay the foundation for demonstrating the potential of CIS as a future commercial product.

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Introduction

CuInSe₂-based Technology

CuInSe₂-based polycrystalline thin films (CIS) represent a promising family of materials for high-power, low-cost photovoltaics (PV), both as a stand-alone single junction and as the narrow bandgap component of a tandem structure [1-3]. Figure 1 compares the photon currents generated in CIS, CdTe, thin film silicon:hydrogen alloys, and crystalline Si calculated from the optical absorption coefficients and assuming no reflection losses [4-7]. The photon current increases as a function of optical path length (that is, absorber layer thickness), and J_{\max} is the maximum available photon current density for the material. For CIS (direct band-gap of about 0.95 eV) 90 percent of the photons are absorbed in a thickness of less than 1 μm . The cost of materials is potentially low since absorber layer thicknesses of only 1-3 μm are sufficient for PV applications.

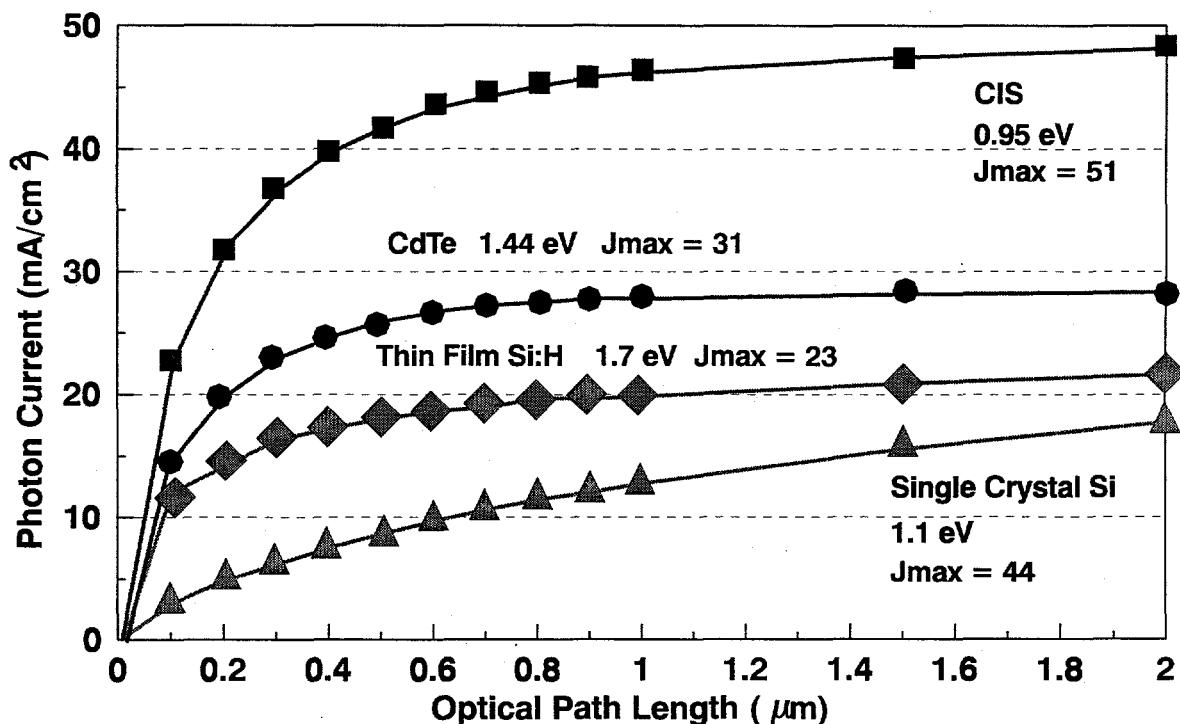


Figure 1. Photon current vs. optical path length for various materials. (100 mW/cm² ASTM AM 1.5 global spectrum, 25°C)

Recently CIS-based device efficiencies have surpassed 17% active area efficiency [8] demonstrating significant progress toward reaching 20% efficiency [9-15]. CIS modules are typically fabricated on soda-lime glass substrates, one of the more desirable PV substrate materials available today due to its abundance and low cost. In fact, the highest reported efficiencies for CIS-based modules and devices utilize soda-lime glass substrates. Thus, CIS-based polycrystalline materials have the potential to address the Department of Energy (DOE) Five Year Plan polycrystalline thin-film milestones, namely the fabrication of stable modules with efficiencies of 15% (150 W/m²) or more made by scalable, low-cost techniques on inexpensive substrates.

The objective of this contract (No. ZN-1-19019-5) was to achieve progress toward the polycrystalline thin-film milestones of the DOE Five Year Plan (Preface). Siemens Solar Industries (SSI) has pursued the research and development of CuInSe_2 (CIS) thin film PV technology since 1980. Prior to the contract, SSI had demonstrated a 14.1% efficient 3.4 cm^2 active-area $\text{ZnO}/\text{thin CdS/CIS/Mo/glass}$ cell, unencapsulated integrated modules with aperture efficiencies of 11.2% on 940 cm^2 and 9.1% on 3900 cm^2 and an encapsulated module with 8.7% on 3883 cm^2 (verified by NREL). The purpose of this program was to build upon this foundation, to address identified processing difficulties, and to improve materials and device quality over large areas.

Module Design

The module design, illustrated in Figure 2, consists of 53 series-connected $\text{ZnO}/\text{CdS/CIS/Mo/glass}$ cells fabricated on a 4141 cm^2 ($128.6 \times 32.2 \text{ cm}$) glass substrate with a nominal aperture area of 3895 cm^2 ($127.3 \times 30.6 \text{ cm}$). A standard module interconnect region including the layers which form the solar cell devices is portrayed in the expanded cross section. The module fabrication process including absorber formation steps is represented schematically in Figure 3.

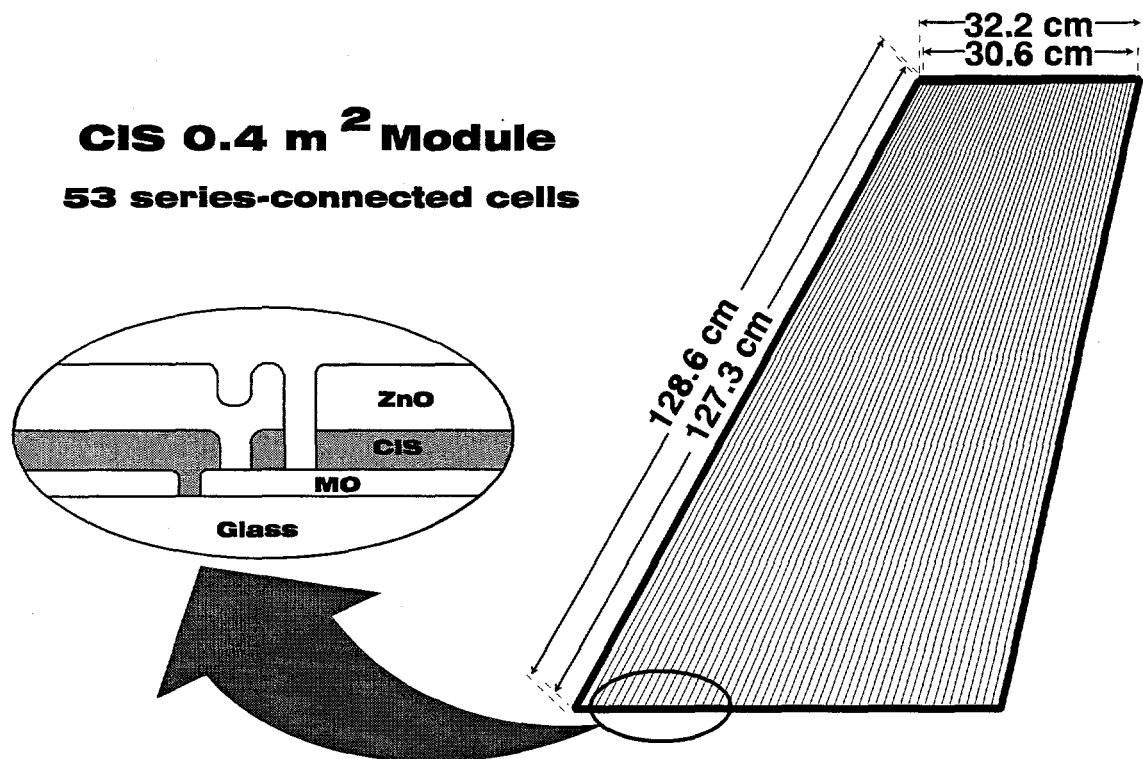


Figure 2. Basic design of 0.4 m^2 CIS module. The details of the standard integrated interconnect are illustrated in the inset.

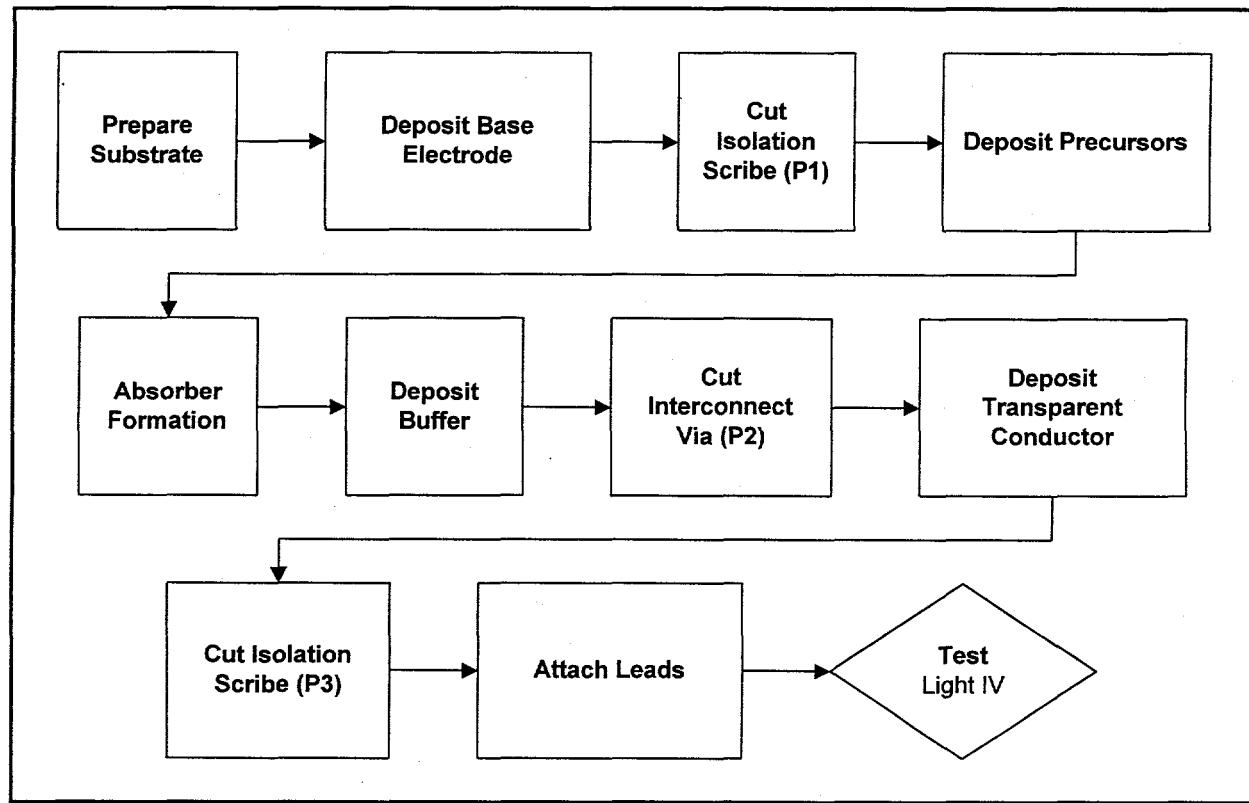


Figure 3. Schematic of module fabrication process.

In the standard module design, the cell spacing is 0.577 cm (0.227"). The back electrode isolation scribe, typically 25 to 75 μm wide, is cut with a laser. The ZnO/Mo interconnect is made through a 25 to 50 μm wide via created in the CIS. This via is made using either laser or mechanical scribing techniques. The nominal contact resistance is in the range of 0.5-2 $\text{m}\Omega\text{-cm}^2$. The ZnO/ZnO isolation scribe is also performed by either mechanical or laser scribing. The CIS circuits are laminated behind tempered glass and framed using a reaction injection mold (RIM) process or aluminum frames. Electrical connection is provided by a two-conductor cable. Discussions include improvements which have been implemented to address yield and performance issues related to these module designs.

Module Deliverables

The contract performance milestones for encapsulated CIS modules are summarized in Table 1. Milestone deliverable dates have been revised to reflect increases in the contract duration which were made to accommodate reduced annual funding levels.

Table1 . Contract Deliverables.

Milestone	Date	Deliverable
Phase 1		
M1	7/31/91	4 encapsulated CIS modules (1 ft ²) for reliability testing at NREL.
M2	4/30/92	An encapsulated 36.5W, 9.4% efficient (aperture area) CIS module.
Phase 2		
M3	7/31/92	4 encapsulated CIS modules (1-4 ft ²) for reliability testing at NREL.
M4	7/31/92	An encapsulated 38.8W, 10% efficient (aperture area) CIS module.
Phase 3		
M5	12/31/93	An encapsulated 44.6W, 11.5% efficient (aperture area) CIS module.
M6	12/31/93	4 encapsulated CIS modules (1-4 ft ²) for reliability testing at NREL.
M7	1/31/95	An encapsulated 48.5W, 12.5% efficient (aperture area) CIS module.

Based upon an encapsulated 53-cell, 3883 cm² aperture area module.

Phase 1

Phase 1 Overview

During Phase 1, SSI met all performance milestones and program deliverables. A new world record of 37.7W and 9.7% aperture efficiency for a 3883 cm² (126.9 x 30.6 cm) encapsulated CIS module was demonstrated and verified at NREL. Unencapsulated CIS module plate performance achieved 40.8 W and 10.5% aperture efficiency. Excellent measurement agreement between SSI and NREL was verified.

Establishing a baseline CIS module fabrication process was emphasized. Module performance strongly depends on the spatial uniformity of the absorbers, electrodes and on interconnect performance. Spatial uniformity and interconnect performance were characterized by implementing a number of improved module diagnostic techniques and by using experimental studies with special emphasis on glass substrate quality and cleaning. The impact of macroscopic and microscopic variations in performance were related to uniformity and defects using optical beam induced current (OBIC), electron beam induced current (EBIC), scanning electron microscopy (SEM), and other techniques such as tape adhesion testing.

Five CIS modules were shipped to NREL to meet the Phase 1 deliverables. Table 2 summarizes their photovoltaic parameters. The best module measured 37.7 watts (9.7% aperture efficiency) at NREL. The remaining four CIS modules were in the 30-31 watt range. The 37.7 W, 9.7% aperture efficient CIS module fulfilled the M2 milestone of the contract and was shipped to NREL with the M1 milestone deliverables.

Table 2. Parameters for CIS modules delivered to NREL (Phase 1).

Module #	P _{max} (W)	I _{sc} (A)	V _{oc} (V)	FF
182-5	37.7	2.44	24.0	0.644
282-5	31.0	2.42	22.7	0.563
324-4	30.9	2.38	22.4	0.580
324-6	30.0	2.38	22.0	0.575
324-16	29.8	2.40	21.9	0.566

Module Diagnostics

During Phase 1, several techniques were implemented or upgraded in order to evaluate the large area (0.4 m²) CIS modules. The following provides a partial list of these analytic techniques:

Light and Dark Current-Voltage

Spectral Response

Open-Circuit Voltage Mapping

- * Forward Bias Voltage Mapping
- * J_o and Diode Factor Mapping of each Module Cell
- * Interconnect and Sheet Resistance Measurements

Optical Transmission/Reflection/Absorption

Optical Microscopy

Optical Beam Induced Current (OBIC) Analysis

Scanning Electron Microscope (SEM) Imaging

Electron Beam Induced Current (EBIC) Analysis

Auger Surface Analysis and Depth Profiling

- * Atomic Force Microscope (AFM) Imaging
- * Fog Box Imaging

Adhesion Tape Pull Test

* Implemented or upgraded during contract.

This section summarizes the application of these techniques to the characterization of the CIS modules.

Voltage Mapping

V_{oc} maps, where the module is cut into 10 cm wide strips and the voltages of the 53-cell strips are mapped, provide information on uniformity of the junction quality and module integration processing. Resistance losses due to individual interconnects or ZnO sheet resistance can be determined by mapping the cell voltage drops at a fixed forward bias current. In addition, individual cell I-V curves can be evaluated by measuring the dependence of the voltage drop of each cell on the applied module current. The physical nature of the

defects is then correlated using optical beam induced current (OBIC), electron beam induced current (EBIC), scanning electron microscopy (SEM), and other techniques such as tape adhesion testing.

The V_{oc} maps for a 39 W (10.0% efficient) and a 32 W (8.2% efficient) module are compared in Figure 4. The voltage is very uniform for the higher power module. In contrast, the cell voltages for the lower power module are both suppressed overall and non-uniform. OBIC studies indicate that the reduced V_{oc} cells have localized areas of low response. One source of low response identified by SEM and EBIC are areas of abnormal ZnO growth associated with "dust" contamination of the surface before the ZnO. Other areas do not correlate with surface features but have reduced adhesion between the CIS and Mo. Interconnect problems can substantially reduce the module fill factor (FF) as evidenced in Figure 5. The 0.53 module FF results from the poor FF of individual module slices (Figure 6). Comparison of the V_{oc} and forward bias maps in Figure 7 show the junctions are fairly uniform but some cells have high voltage drops associated with poor quality interconnects.

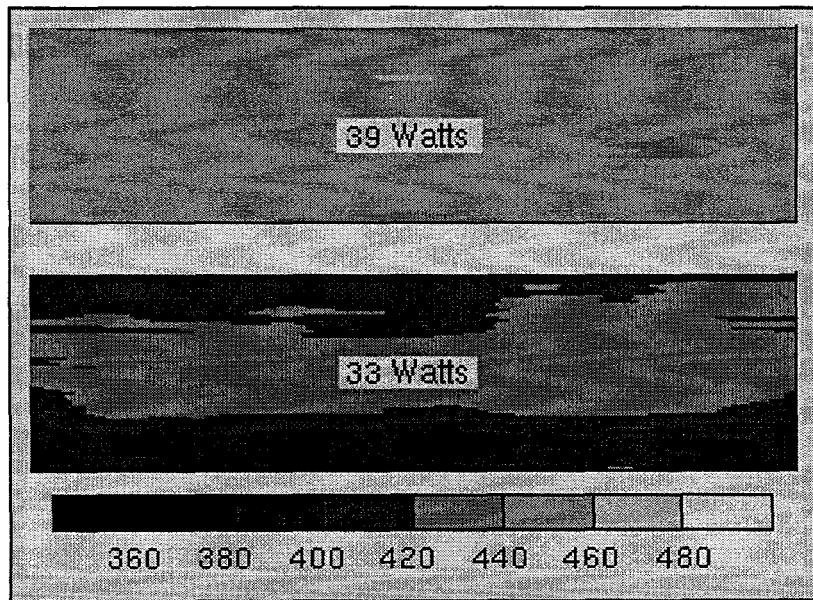


Figure 4. V_{oc} maps comparing higher and lower power CIS modules.

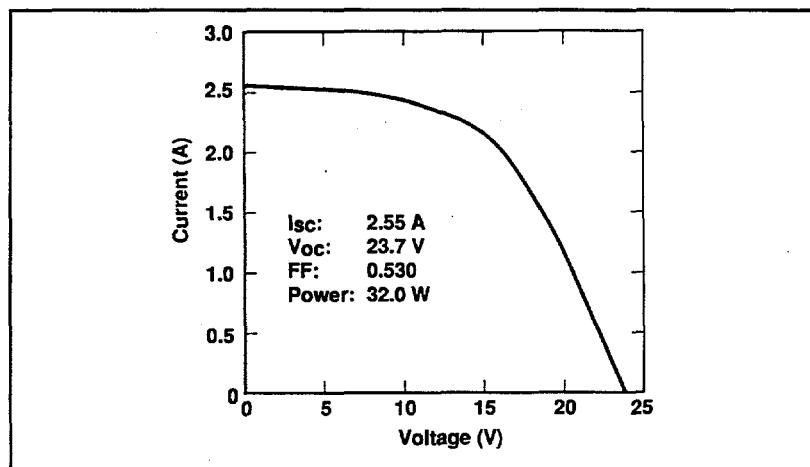


Figure 5: I-V curve of an unencapsulated 0.4 m^2 CIS module.

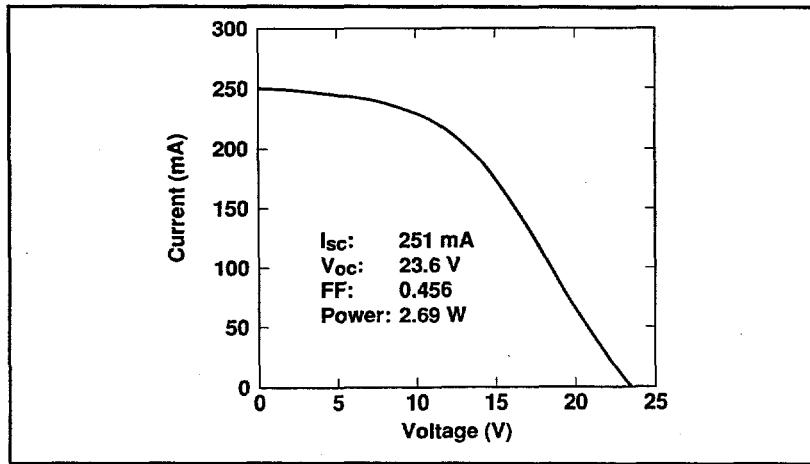
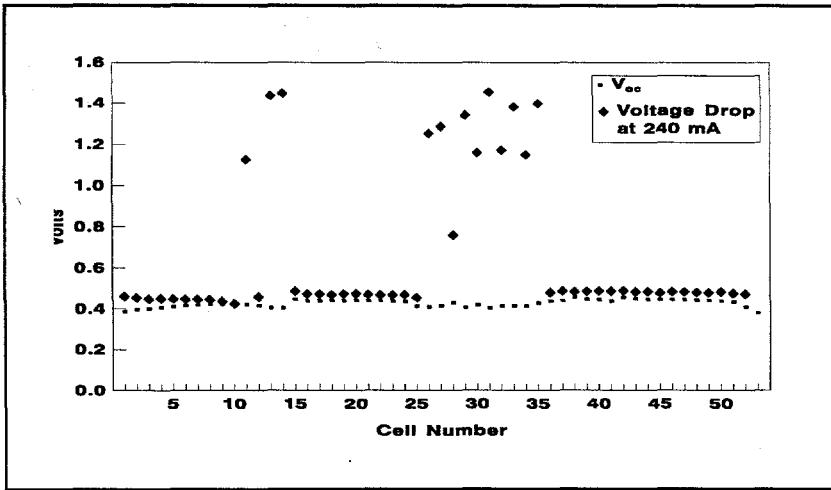


Figure 6: I-V curve of one slice of the module of Figure 5.



An extension of the above voltage mapping techniques is the determination of the individual light and dark cell I-V curves by incrementing the current through the module and measuring the voltages across each of the 53 cells. The V_{oc} variations may be caused by localized microshunts due to dust or other contamination or to variations in the CIS stoichiometry. Diode factors J_o 's were measured for individual cells in a module and the 1-sun cell V_{oc} 's were calculated. Correlation between measured V_{oc} and junction quality was demonstrated.

Defect Characterization

Optical beam induced current (OBIC), electron beam induced current (EBIC), scanning electron microscope (SEM) imaging, Auger spectroscopy, and adhesion tape pull tests are the primary techniques used to compare cells with different V_{oc} 's and determine the physical nature of the defects. SEM and EBIC imaging data were compared with adhesion testing using 25 oz/in. tape. Similarities were found between areas around patterning and small randomly located areas of poor adhesion and patterning. The CIS pulls away within the interconnect region. Most cleavage occurs at the CIS/Mo interface. These studies were continued and extended in following phases and the results are discussed in later sections of this report.

The quality of the incoming glass substrates is another source and promoter of defects in the CIS module. Variation in glass quality which are not significant for the primary customers of the glass industry may affect performance. Figure 8 illustrates how small cracks in the incoming glass surface can lead to abnormal growth of the Mo layer, stress build-up in the Mo layer and subsequent loss of adhesion. Studies of the impact of glass cleaning strategies on CIS performance are presented in following sections.

Thin Film CIS and CdS Characterization

Scanning electron microscopy (SEM) and atomic force microscopy (AFM) were used to evaluate the structure of the CIS layer and subsequent CdS layer. The general morphology of the CIS surface indicates a distribution of grain size on the order of one micron and some porosity in the film surface. AFM images illustrate the surface features of a CIS grain with and without CdS. The CIS grain surface is featureless on the 500 Å scale before CdS deposition. After CdS, grain structure is evident on the order of 500 Å in size.

Summary

A baseline characterization of the CIS modules was established during Phase 1 as described above. Fabrication of large area CIS modules on 0.4 m² glass substrates (32.2 x 128.6 cm) presented issues of the defect distributions in the incoming low-cost glass substrates, spatial uniformity of large area processing, and defects introduced during module fabrication. The cell interconnects in a monolithic module introduce electrical and morphological issues which are not present in discrete devices.

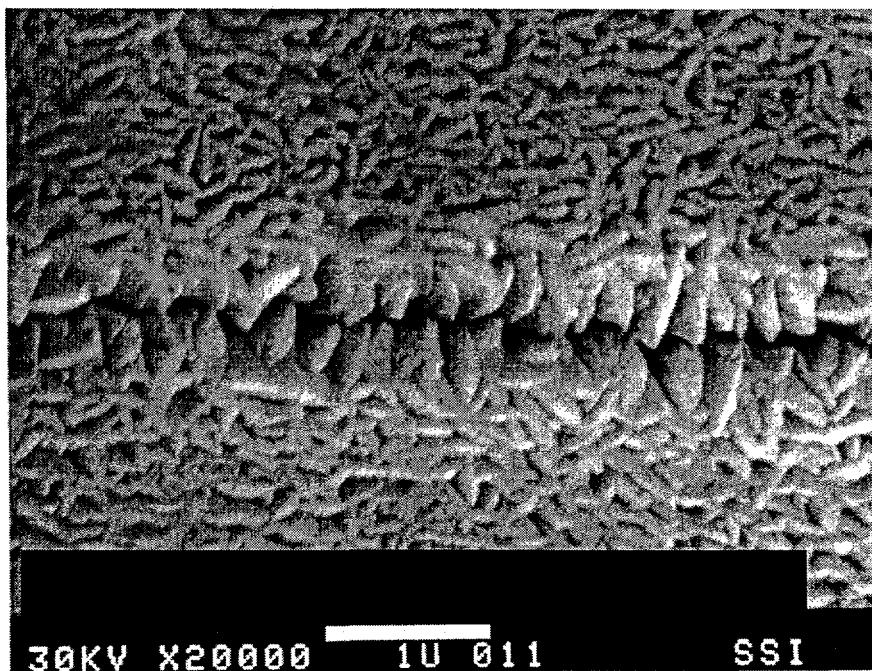
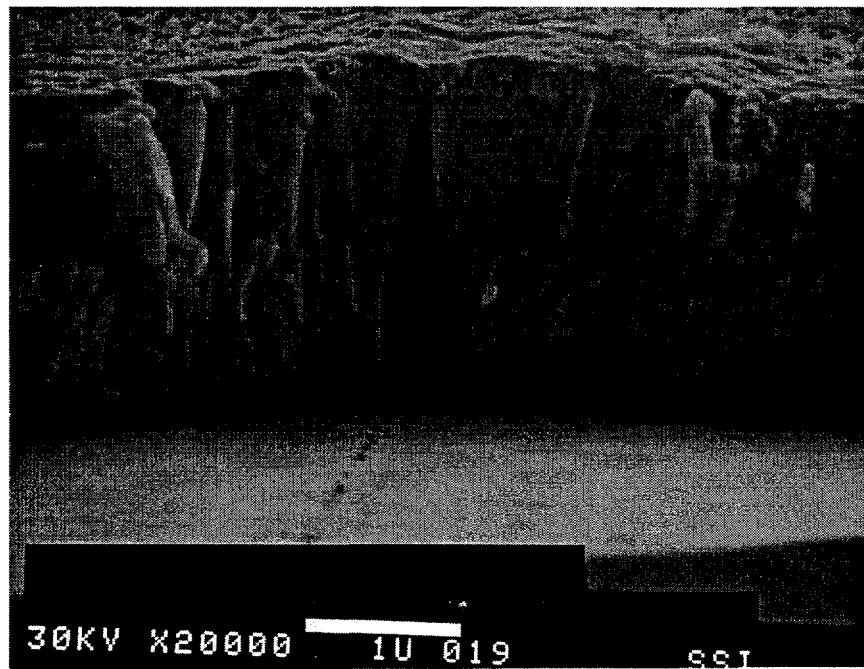


Figure 8. SEM images of Mo growth effected by a microcrack in the glass substrate.

Experimental Studies

This section summarizes several experimental studies that were carried out to correlate large area CIS module performance to the glass substrate properties and to module processing.

Glass Substrate Studies

During Phase 1, it became apparent that examination of the incoming glass cleanliness and correlation to defects in the subsequent thin film layers was necessary. The cleanliness (or rather, the lack thereof) of the incoming glass substrates can substantially compromise the performance and yield of the CIS modules.

A new apparatus called a "Fog Box" was fabricated in order to image contamination and other defects on the glass surfaces. The box, which supports a 1x4 ft glass plate, includes a source of water vapor which condenses on the glass in patterns which highlight the contamination and other features. Findings include:

- 1) As received glass has a number of different patterns of surface contamination associated with it (that vary part-to-part, side-to-side, batch-to-batch). These include glove marks, edge marks and at least two different types of "track" marks (one associated with the vendor's glass handling machine; and another with vendor applied powder coatings to separate glass plates);
- 2) The current glass washing procedures do not remove all of the contamination patterns observed on as-received glass;
- 3) The Siemens Solar glass washer can leave its own set of contamination marks on the glass surface. The patterns are typically identified by their periodic spacing consistent with the wash roller circumference and their orientation relative to the glass edge. The glass washer was rebuilt including new rollers and bearings from the vendor.
- 4) Some patterns of device performance across a module plate correlate with the patterns seen with the "Fog Box";
- 5) Some glass batches have what appear to be oils present around the edges. This was traced back to materials used during glass cutting by the glass manufacturer to give "clean" cuts.

SEM images of a circular defect in a CIS module indicated that the defect influences the surrounding film morphology several hundred micrometers away. Cracks are evident in the center of the defect which are associated with scratches in the glass. Depressions in the surface of the ZnO window layer are also associated with linear scratches in the underlying glass substrate. In other studies, optical beam induced current (OBIC) measurements of CIS modules reveal that large (500 μm) shunt defects are caused by CIS adhesion failure in a relatively small (30 μm) region around very small (approximately 1 μm) scratches in the glass substrates.

Two parallel strategies were initiated during Phase 1. One was to implement more aggressive substrate preparation/glass cleaning procedures which would reduce our susceptibility to the quality of the as-received glass surfaces. The second was to re-evaluate glass from different vendors in order to review which vendors could deliver consistent quality to produce high performance CIS modules with a good yield.

CeO₂ Glass Polishing

CeO₂ polishing was one approach to glass surface preparation that was explored. Module parameters were compared for fabrication with and without CeO₂ polished glass (5 min electric polisher with CeO₂ powder + DI H₂O):

An average module power increase of 1.2W resulted from the polishing due to an improvement in V_{oc} and fill factor. Diagnostics of the module plates indicated that the CeO₂ reduced the number of defects and improved the film uniformities across the module plate. Although the CeO₂ polished glass substrates were found to have a lower density of the large shunt defects, a higher density of small optically-unresponsive (i.e. "dead") areas were evident with OBIC.

Glass Cleaning Matrix Study

To further investigate methods to improve the quality of the glass surface, a matrix of 120 10x10 cm test structures were divided into four groups and processed separately as follows: (1) normal baseline detergent wash; (2) polished with CeO₂ before detergent wash; (3) 3 min 5% HF etch before detergent wash; and (4) CeO₂ polish before detergent wash followed by the 3 min 5% HF etch after the detergent wash. The results are summarized in Tables 3 and 4.

Table 3. Overall Average Cell Performance.

	Eff (%)	V _{oc} (mV)	J _{sc} (mA/cm ²)	FF
Baseline	9.68	417	37.0	0.622
HF etch	9.73	422	36.7	0.628
CeO ₂ polish	8.93	406	36.1	0.605
CeO ₂ + HF	9.48	418	36.5	0.616

Table 4. Average Cell Performance without Shunted Cells.

	Eff (%)	V _{oc} (mV)	J _{sc} (mA/cm ²)	FF
Baseline	9.77	421	37.0	0.626
HF etch	9.73	422	36.7	0.628
CeO ₂ polish	9.02	408	36.2	0.608
CeO ₂ + HF	9.65	422	36.6	0.624

Although the result of the experiment is that there was essentially no effect of the HF etch or the CeO_2 polish plus HF etch on the cell performance distribution, a more detailed evaluation of the data brings out several points of interest. The baseline cell population can be characterized by a bimodal distribution, namely cells with an average efficiency of 9.77% in addition to some cells that are very shunted (1% efficiency range), resulting in an overall average efficiency of 9.68%. HF etching by itself eliminates the number of very shunted cells giving an overall average efficiency of 9.73%, which is slightly less than the non-shunted baseline average of 9.77%. Polishing alone also reduces the number of very shorted cells (1% efficiency range), but degrades the average non-shunted cell performance to 9.02%, resulting in an overall average for the polished sample population of 8.93%. This is attributed to the removal of large defects and the creation of many very small defects (trading a few large shunts for many small ones). Polishing plus HF etching apparently smooths out these distributed small defects (improving the average non-shunted efficiency to 9.65%), but somehow creates large defects again, possibly by opening up "potential shunts" or defects just below the surface of the glass that would otherwise not be exposed. The result is an overall average efficiency for this group of 9.48%.

The implication of this study for CIS modules is that there are important aspects to glass preparation.

Vendor Glass Evaluation

A preliminary comparison split between two glass vendors showed module outputs of 34-36 watts (440 mV average cell V_{oc} 's) for one vendor compared to 30-33.5 watts (425 mV average cell V_{oc} 's) from another. This study was then expanded to include glass samples from several manufacturers. All soda-lime glass samples showed adhesion failure of the Mo/CIS at Pattern 1, ("P1", Mo isolation laser scribe) and varying width low OBIC response regions adjacent to the interconnect. OBIC losses extend up to 0.5 mm beyond the physical interconnect patterns, reducing module power by about 10 points. In addition, poor adhesion in this near-P1 region can cause shunting which reduces module power by another 10 points.

Chemically treated glass (which changes both the surface morphology and the glass surface chemistry) shows minimal "dead" (low OBIC response) regions. Samples grown on Mo deposited with an air/water leak showed no dead region. In addition, 7059 borosilicate glass and quartz both showed no dead region. The dead regions around the Pattern 1 are believed to be caused either by contamination, film stress, or both.

Module Processing Studies

Two processing studies carried out in Phase 1 were a study of the effect of time delays during CIS module fabrication and an investigation of the impact of background water levels during processing. Four types of processing time delays were evaluated, namely time delays between: (1) Mo and CIS deposition; (2) CIS and CdS deposition; (3) CdS and ZnO deposition; and (4) overall start-to-finish.

Trends are apparent although data was collected from a large number of different processing studies and scatter exists in the data. Time delays between the Mo and CIS deposition steps have little influence on module performance. For the junction formation steps, a slight loss in V_{oc} due to delays between the CIS and CdS layers and between the CdS and ZnO layers is observed, although there is no significant loss in module power. Delays at these steps would increase the probability of damage or dust and other contamination of the junction interfaces. Finally, except as noted for the junction fabrication steps, there is no significant power loss due to differences in total fabrication time.

Modules fabricated with very high (5 relative % H₂O) partial pressures of water vapor during CIS film deposition resulted in modules with more severe CIS delamination from the Mo electrode layer in the region adjacent to Pattern 1. The CIS/Mo adhesion in the cell areas away from the patterns was unaffected. Overall, high water background levels do not seem to have a serious impact on the formation of CIS.

CIS Unencapsulated Module Performance

During Phase 1, several unencapsulated CIS module plates achieved output powers above 40 watts with the best at 40.8 watts or 10.5% aperture efficiency based on a 3890 cm² aperture area at 100 mW/cm² ASTM air mass 1.5 global spectrum and 25 °C.

CIS Module Measurement Comparison between NREL and SSI

Verifying agreement between SSI and NREL CIS module measurements was an important issue early in the contract. Prior to the contract, when NREL upgraded their Spire 240A solar simulator during the summer of 1990, the I_{sc} values of the SSI CIS MAR10 modules at NREL measured 7% less than their values before the upgrade. Thus, in May 1991, a laminated/framed CIS module (#182-5) was delivered to NREL for testing. Spectral mismatch correction is required. Without spectral correction, the measured CIS I_{sc} using Si reference cells is low compared to its true value (that is, I_{actual} equals I_{measured} divided by the spectral mismatch factor M, where M equals 0.975). A 20-cell, 10 cm wide CIS mini-module fabricated at SSI was calibrated on the NREL X25 solar simulator and used to set the NREL LAPSS intensity. The NREL LAPSS has much better illumination uniformity (+/- 0.5%) and measurement electronics than the NREL Spire 240. The NREL Spire 240 measured 7% lower J_{sc} than SSI, consistent with the J_{sc} drop noted for the CIS MAR10 modules. The NREL LAPSS data compares very closely with the SSI data. J_{sc} data agrees within 1.6%.

Table 5. SSI and NREL data comparison for module 182-5 (Phase 1).

	Power (W)	Eff (%)	I _{sc} (A)	V _{oc} (V)	FF
SSI R&D LAPSS (Before)	38.1	9.8	2.51	24.3	0.626
SSI R&D LAPSS (After)	37.5	9.7	2.48	24.3	0.624
SERI Spire 240	36.2	9.3	2.31	24.2	0.647
SERI LAPSS	37.7	9.7	2.44	24.0	0.644
SERI LAPSS/SSI Ratio (%)	100.5	100.5	98.4	98.8	103.2

Notes:

1. Efficiency based on 3883 cm² (30.6 x 126.9 cm) aperture area.
2. SERI Spire data has 0.975 spectral mismatch correction. SERI LAPSS was calibrated from the SERI X25 using a CIS minimodule.

Phase 2

Phase 2 Overview

During Phase 2 (originally 5/1/92-4/30/93), the duration of the contract was increased from 36 to 45 months due to fiscal constraints in the polycrystalline program at NREL. Phase 2 was extended to span from 5/1/92 through 8/15/93. During Phase 2, SSI met all performance milestones and program deliverables.

In Phase 1, the emphasis of the research effort was on establishing the baseline CIS module fabrication processes including detailed characterization of the cells and interconnects. In Phase 2, the initial focus was to implement the processing and characterization methods demonstrated in Phase 1 to meet the deliverables schedule for the contract and to produce statistically significant quantities of large area modules for verification of performance for both outdoor and accelerated environmental exposure. Over 2300 1'x4' CIS modules have been fabricated since processing began in the Camarillo facility.

Although the process produced high-efficiency cells and modules, average performance was poor and inconsistent. The origins of module reproducibility problems were unclear. Large area module fabrication was temporarily suspended to determine the critical issues affecting yield losses in module fabrication using small area test devices (3.3 cm² active area cells) and modules (60 cm² aperture area) as the experimental test bed. This shift greatly enhanced our ability to identify the root causes of yield loss in module fabrication.

The most critical issues determining module yield losses can be grouped into three major categories:

1. The uniformity and reproducibility of the absorber formation process dominates the fundamental performance of the material over a large area. Results are described of implementing a graded absorber formation process on both improved champion and average performance and yield.
2. The interaction of the substrate with the films requires appropriate selection criteria and preparation techniques for minimizing defects that lead to shunting and areas of poor photoresponse. Discussions include the impact of substrate-induced defects and techniques developed for imaging and understanding them.
3. Performance losses near interconnects reduce module performance and can cause inadequate performance through module durability testing. Development of alternate strategies for fabricating interconnects and diagnostics implemented for characterizing and quantifying interconnect performance are discussed.

Through the adoption and further refinement of a graded absorber formation process in which the surface layer of CIS incorporates sulfur, combined with the appropriately prepared substrate, mean efficiency for 3.3 cm² test devices was improved from 9% to 14%, with the champion cell active area efficiency of 16.2%. Perhaps more significant is that the occurrence of cells below 10% efficiency was virtually eliminated.

Alternate techniques for fabricating interconnects were developed to address losses near pattern lines [6]. In these approaches, the interconnects are made after the formation of the absorber and employ the application of insulating and/or conducting materials (typically polymer-based). This approach has produced

a mini-module with 11.7% aperture area efficiency, which was at that time an SSI record for a CIS integrated module.

Four CIS modules were shipped to NREL to meet the M3 deliverable. One module (#483-11) broke and was replaced with #308-05. The performance parameters for these modules are summarized in Table 6. The power outputs are in the 31-36 watt range. The CIS circuits are laminated behind tempered glass. Framing and termination are achieved using an extruded aluminum frame and plastic junction box (except #308-05, which utilizes a reaction injection molded frame and a two-conductor cable). M4 deliverable requirements were met with the earlier M2 deliverable module of 37.7 watts (within 3% of the 38.8 watt milestone). Furthermore, champion cell performance improved to 16.2% on 3.3 cm² active area test devices.

Table 6. Parameters for CIS modules delivered to NREL. (Phase 2).

Module #	P _{max} (W)	I _{sc} (A)	V _{oc} (V)	FF
483-11*	37.1	2.45	24.4	.621
482-11	35.8	2.45	23.4	.624
482-8	35.4	2.49	23.5	.606
482-9	35.0	2.47	23.4	.607
308-05*	31.5	2.31	22.8	.570

*Note: Module #483-11 broke and was replaced with module #308-05.

Table 7 below is a summary of the best SSI CIS performance results at the end of Phase 2

Table 7. SSI CIS Performance Achievements (Phase 2).

	Power (W)	Area (cm ²)	Eff (%)	I _{sc} (mA)	J _{sc} (mA/cm ²)	V _{oc} (V)	FF
Test Structure	-	3.3	16.2*	-	41.0	0.558	.71
10x10 cm module plate	.707	60	11.7	136	35.1	7.47	.70
1x1 ft module plate	10.5	938	11.2	641	39.3	25.5	.64
1x4 ft module plate	40.8	3890	10.5	2550	37.0	24.5	.65
1x4 ft module	37.7	3883	9.7	2440	35.5	24.0	.64

(100 mW/cm² ASTM air mass 1.5 global spectrum, 25°C)

*Active Area, reported efficiency

In addition to scheduled deliverables, thirty-six prototype 1'x4' RIM-framed CIS modules were delivered to NREL for the installation of a one kilowatt array at NREL's outdoor test site. SSI and NREL have also continued to monitor the outdoor performance of CIS prototype modules, demonstrating inherent stability of the material for more than six years.

Absorber Material

This section summarizes the results of investigations into the impact of the quality and uniformity of the absorber materials on cell and module yield. The fundamentals of the two-step absorber formation process are discussed. Also summarized are results of implementing a graded absorber formation process in combination with improved selection and preparation of substrates. During Phase 2, average active area cell efficiency improved from 9% to 14%, and a new champion cell was produced with 16.2% active area efficiency.

Absorber Formation Studies

Initial efforts in characterizing module yields focussed on separating material issues from interconnect issues. The repeatability of the basic cell fabrication process was evaluated by producing 6048 3.3 cm² test devices. The performance distribution of these cells is plotted in Figure 9, superimposed with the performance distribution of the 2352 modules. The difference between the module and cell distributions are attributed to a combination of active area loss (ca. 7 rel %), series resistance losses due to the increased transfer lengths and interconnect contact resistance in modules (ca. 7% rel), and the averaging effects of large area processing (one module represents the area equivalent of over 1000 test cells) [16]. These results indicate that although high efficiency cells and modules were repeatedly produced, the basic process being used for fabrication of modules would be inadequate to produce high yields of large area modules or to meet the goals and objectives of this contract.

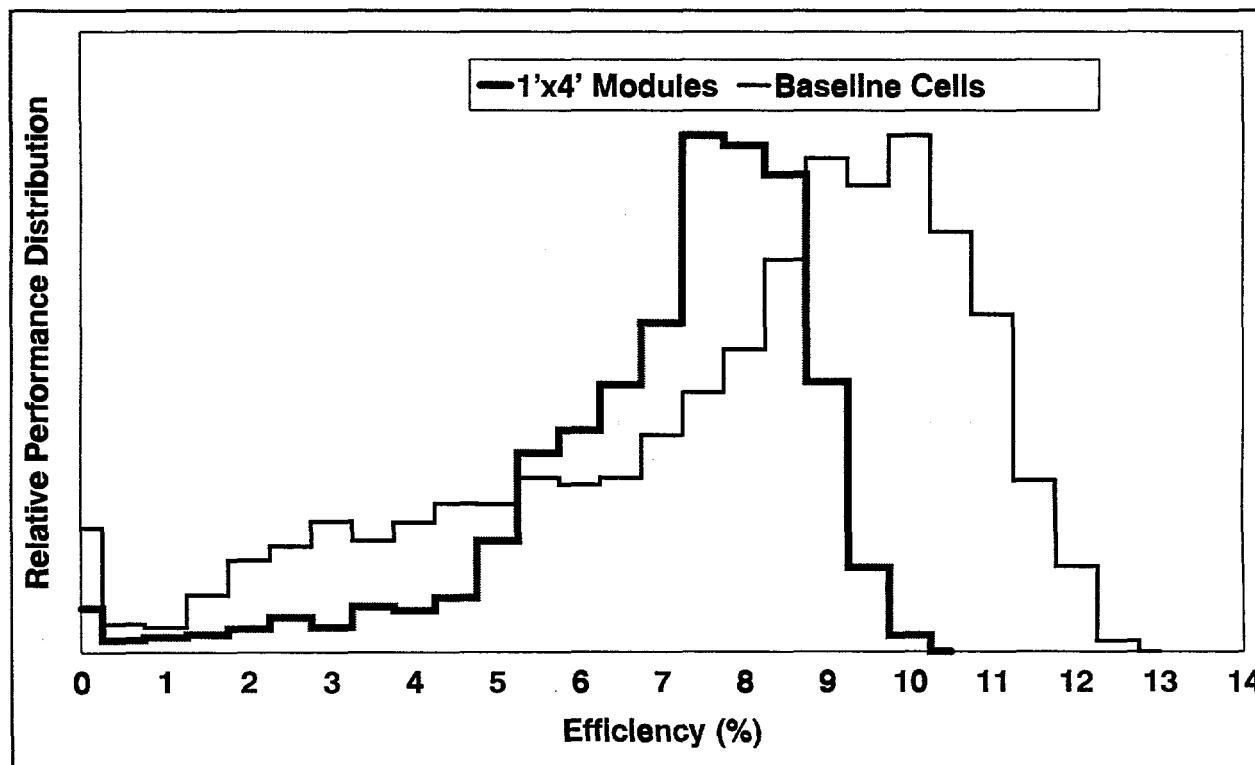


Figure 9. Module & Old Baseline Distribution.
(100 mW/cm², ASTM air mass 1.5 global spectrum , 25° C)

Several groups have undertaken research to develop an improved understanding of the reaction pathways and mechanisms for the formation of CIS-based thin film polycrystalline materials as well as an understanding of the behavior and characteristics of the absorber material and the junctions that give rise to high-quality solar cells [15, 17-24].

SSI conducted a series of experiments similar to published information [17-24], to evaluate the applicability of this work to SSI's two-step process approach. Figure 10 illustrates the selenium to metals ratio (based in ICP analysis) for Cu/Ga films, In films, and Cu/In/Ga films as a function of anneal temperature for a 15-minute anneal time in the presence of H_2Se . All films were on molybdenum-coated soda-lime glass substrates. The selenium-to-metals ratios shown for various combinations of possible binaries are based on atomic metals ratios only; they do not represent XRD or other data indicating the presence of these species. We find that Cu/Ga films reach a constant Se/Metals ratio at 300°C, and do not incorporate significantly more selenium until the temperature exceeds 400°C. The indium, on the other hand, exhibits a monotonic increase in selenium incorporation with temperature, as does the composite Cu/In/Ga film.

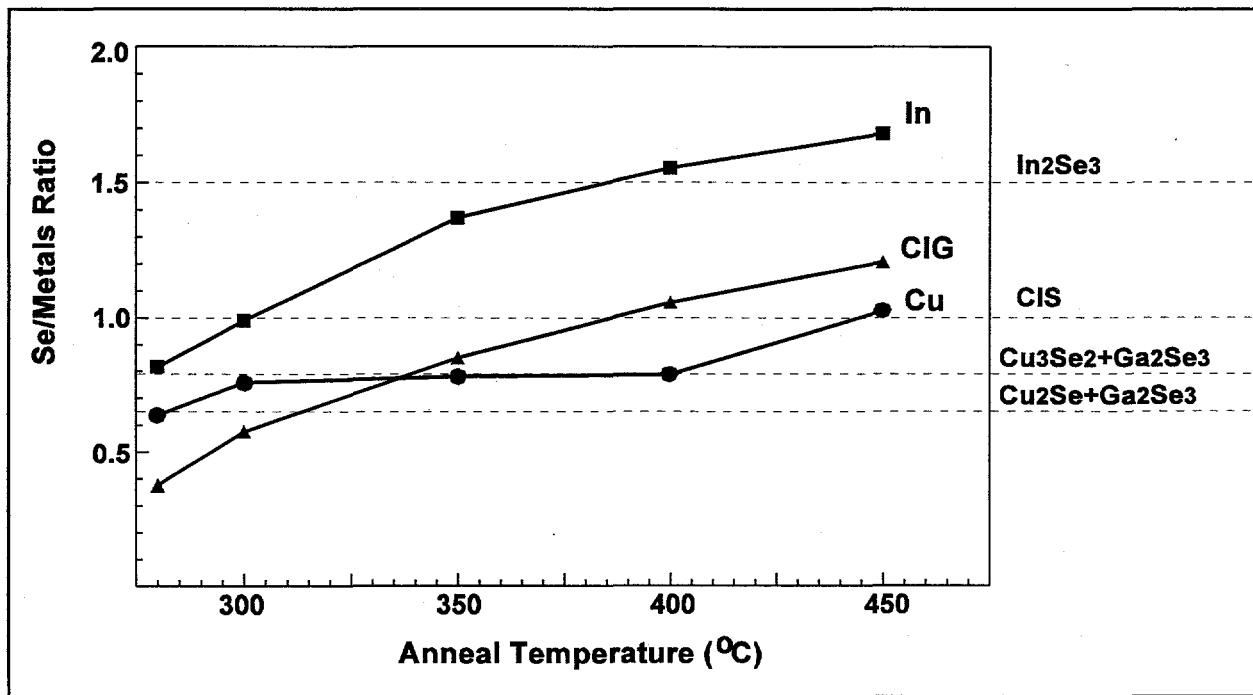


Figure 10. Selenium to metals ratio vs. anneal temperature.

Graded Absorber Structure

For a homogeneous absorber device model, the optimum bandgap for solar cell applications is in the range of 1.4 to 1.5 eV [25], much greater than the bandgap of pure CIS at around 1 eV. A plot of theoretical efficiency versus bandgap is shown in Figure 11 (based on Sze [25]). Reasonable efficiencies have been

reported for various multinary polycrystalline alloys in the CIS family of materials [26]. There are many such alloys from which to choose, many of which are shown in Figure 12 [27]. SSI's graded absorber process evolved from work originally aimed at developing high-efficiency wide-bandgap materials.

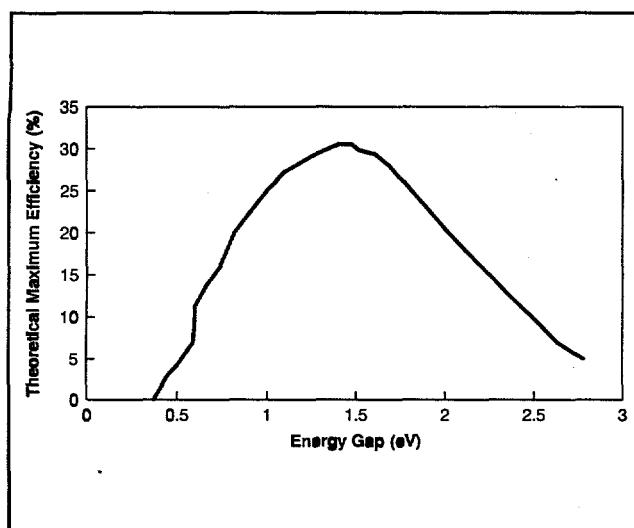


Figure 11. Theoretical maximum efficiency vs. bandgap.

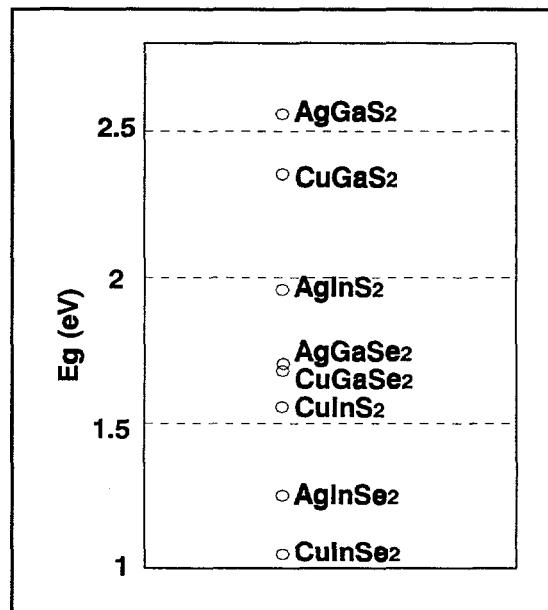


Figure 12. Bandgap of CIS-related materials.

Higher efficiencies are theoretically attainable and have been demonstrated by employing inhomogeneous absorbers using various substitutions of gallium and sulfur for indium and selenium [9-15, 28-32]. These can be comprised of composite absorbers formed from films with discrete bandgaps, absorbers with a compositional gradient or theoretically with multi-junction devices. The physics of the inhomogeneous absorbers is not yet well understood, and many groups are currently working to understand the behavior of these devices.

SSI's two-step absorber formation process can be tuned to tailor compositional gradients in the absorber layers by substituting sulfur for selenium. One such process substitutes sulfur for selenium near the surface of the device. Figure 13 is an Auger depth profile of the composition as a function of depth into a homogenous absorber layer. Figure 14 is the corresponding depth profile for the graded absorber layer, showing the sulfur incorporation near the surface.

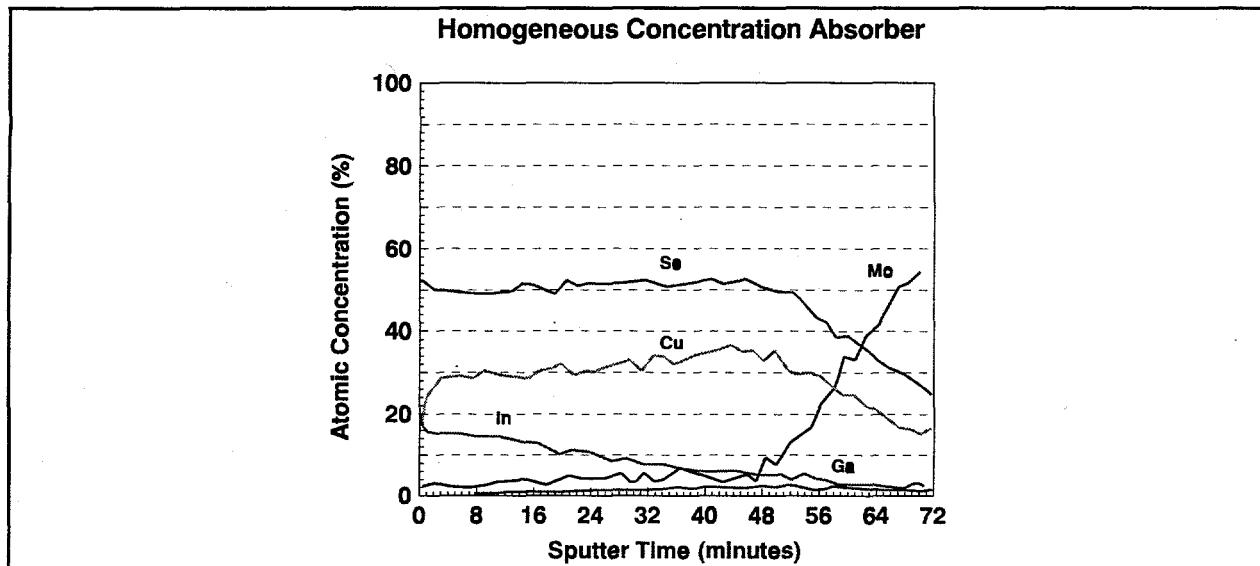


Figure 13. Homogeneous absorber Auger compositional profile.

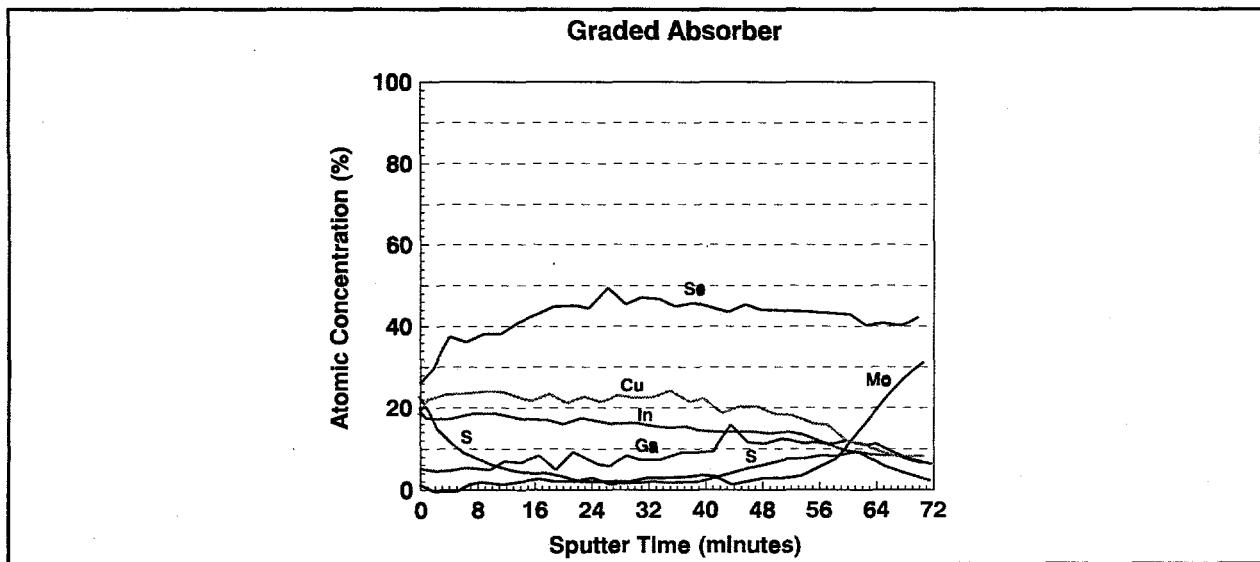


Figure 14. Graded absorber Auger compositional profile.

Graded Absorber Performance and Yield

The basic performance benefit from the graded absorber process was an increase in cell voltage with minimal loss in current collection. This characteristic is illustrated in the spectral response for a homogenous absorber cell and a graded absorber cell presented in Figure 15.

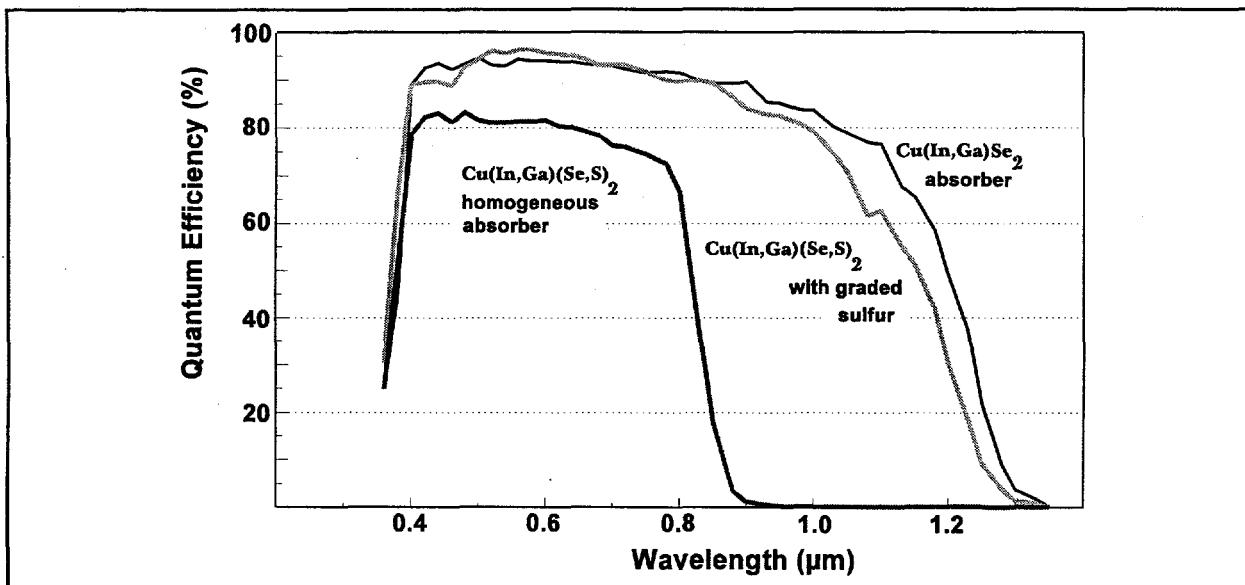


Figure 15. Homogeneous and graded absorber spectral response.

The graded absorber process, combined with substrate selection and preparation (discussed in Section 3), greatly improved the performance and yield of test devices. Figure 16 illustrates the progression of cell distribution with modifications to the absorber formation process as the process continues to be optimized.

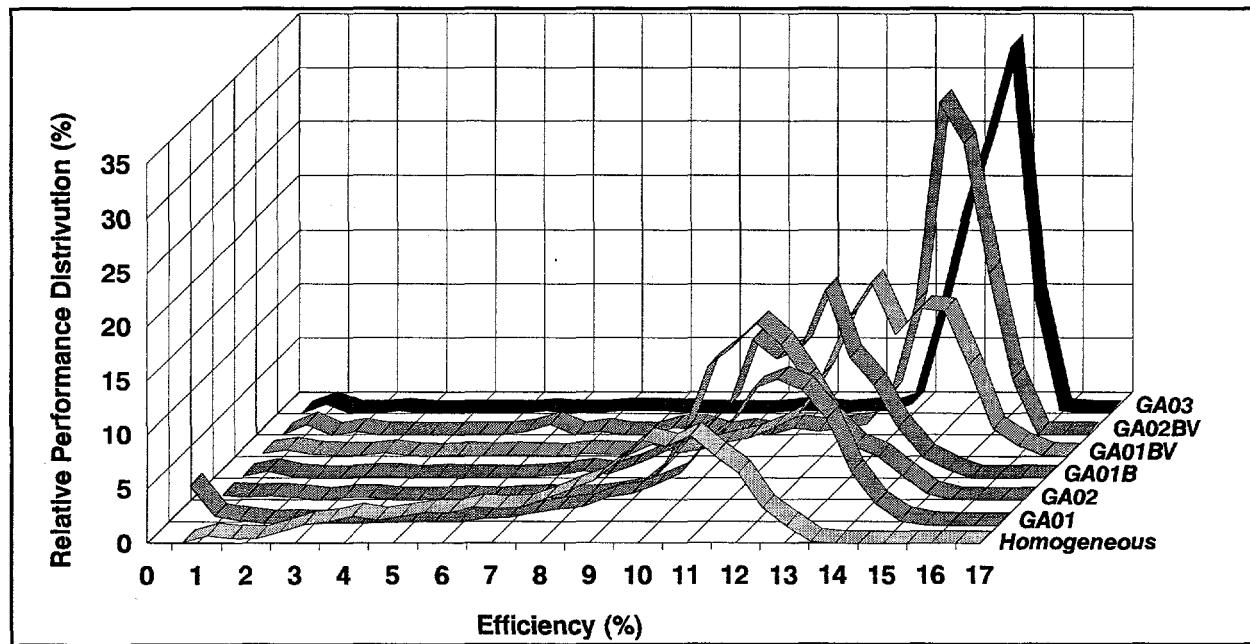


Figure 16. Absorber development distribution progression.
(100 mW/cm², ASTM air mass 1.5 global spectrum, 25° C)

Figure 17 contrasts the initial homogeneous absorber cell process with the final graded absorber process. The average performance for the 6139 cells in the homogenous absorber process is 8.6%, whereas the average for the 807 graded absorber cells in the final process is 13.8%. The significant statistical data for these two populations are summarized in Table 8. Perhaps more noteworthy than the shift in average performance is that cells with efficiency below 10% have been virtually eliminated.

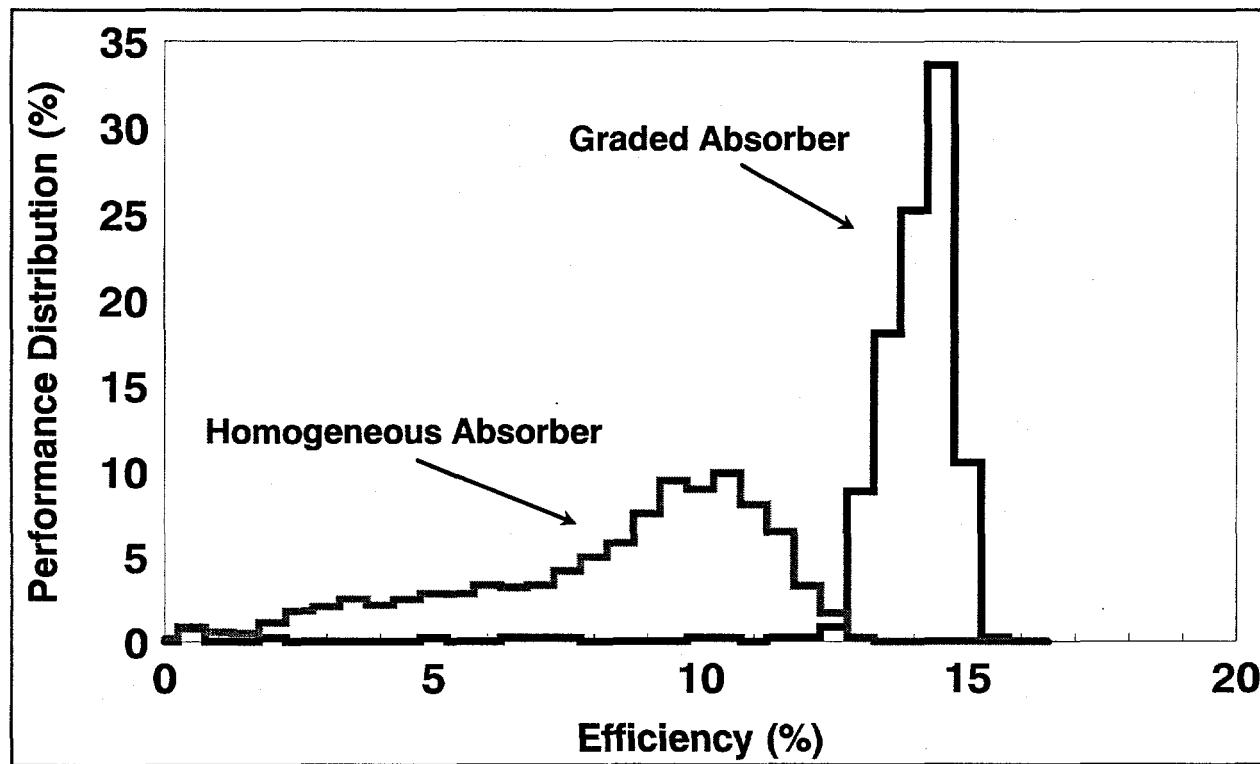


Figure 17. Homogenous vs. graded absorber cell distribution.
(100 mW/cm², ASTM air mass 1.5 global spectrum, 25° C)

Table 8. Statistical data for cell efficiency populations represented in Figure 17.

	Homogeneous Absorber	Graded Absorber
Mean	8.57	13.76
Standard Deviation	2.79	1.88
Median	9.38	14.10
Sample Count	6139	807

(100 mW/cm², ASTM air mass 1.5 global spectrum, 25° C, 3.3 cm² active area)

The improved average performance attained with graded absorbers also produced several high efficiency cells, with the champion device tested at 16.2% active area efficiency (3.3 cm², V_{oc}=558 mV, J_{sc}=41.0 mA/cm², FF=.708). The I-V curve for this cell is presented in Figure 18. An improved understanding of the behavior of the absorber and junction in graded absorber devices will be essential in guiding future absorber composition and formation process optimization.

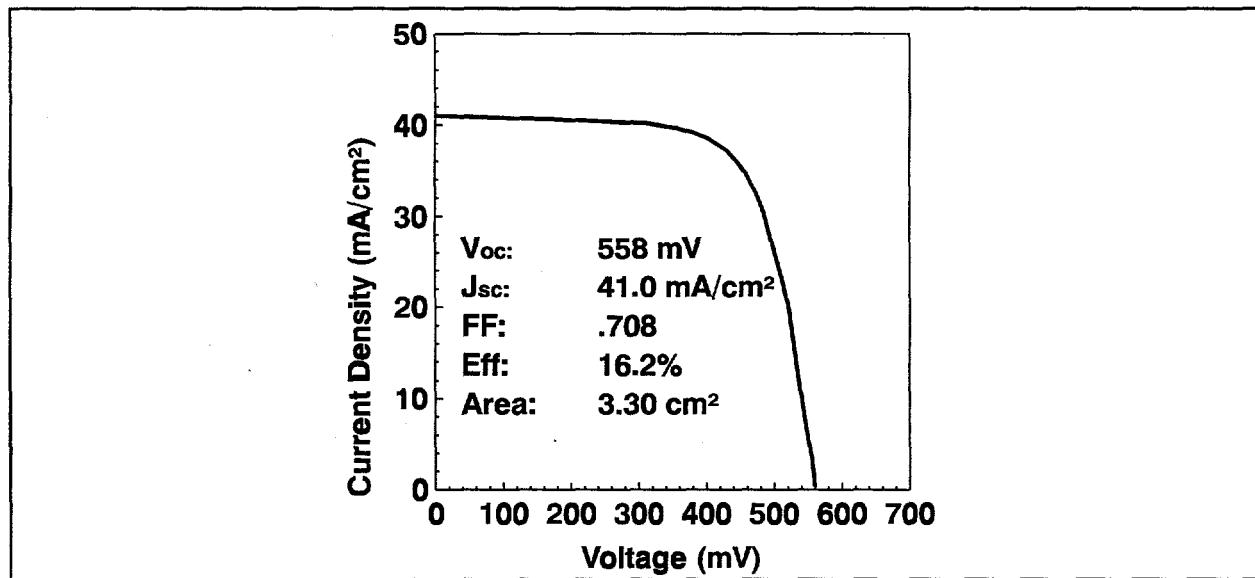


Figure 18. Champion graded absorber cell I-V curve.

(100 mW/cm², ASTM air mass 1.5 global spectrum, 25° C)

Defects

This section summarizes the investigations into substrate-induced defects and the interactions between the substrate and the absorber formation process. The cleanliness and surface condition of the incoming glass substrates can significantly affect the performance and yield of the CIS modules [33]. Phase 2 efforts in this area were to characterize specific physical defects and correlate them with specific electrical defects, quantify the impact of these defects on module performance, to develop and implement simple diagnostics for evaluating the quality of substrates, and to develop and implement substrate preparation techniques to mitigate the impact of these defects.

Defect Classification

Much of the focus of Phase 1 of this contract focussed on the classification and determination of the origins of the various defects that give rise to cell and module performance losses. Many of the results of these efforts have been reported elsewhere [16, 34-36]. There are four primary types of these defects, summarized in Table 9.

Table 9. Summary of Cell Defect Types.

Defect Type	Affected Area
Particle on the CIS surface suppresses the growth of ZnO	5 μm particle suppresses growth over a 90 μm area
Pinhole in the base electrode propagates through the CIS and the ZnO	6 μm pinhole affects a 200 μm diameter area
Particle at the interface bewteen CIS and the base electrode; no visible defect on the ZnO or CIS	5 μm particle affects a 160 μm diameter area
Scratch in the glass propagates through the Mo, the CIS and the ZnO	0.1 μm scratch affects a 250 μm diameter area

Most of these defects can be seen by the naked eye or under a microscope, and correlate with regions of low photoresponse, represented by the dark areas in the optical beam induced current (OBIC) image shown in Figure 19.

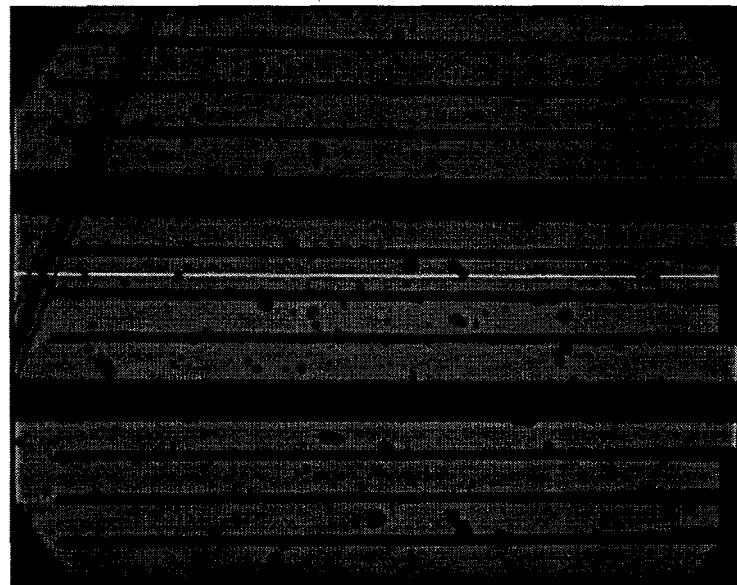


Figure 19. OBIC-imaged defects in CIS cells.

A related defect characteristic of monolithically integrated modules that employ an isolation scribe in the base electrode is the poor adhesion in the area near this scribe line. Although the scribe itself is typically only .001"-.003" wide, the affected area can be up as much as .020"-.060" wide. This behavior manifests itself in tape-pull adhesion tests, in which pairs of dark stripes of CIS detach at the CIS-Mo interface on either side of the isolation scribe. In severe cases, the CIS film actually curls up spontaneously from the substrate, causing series, shunt and reliability problems with the interconnect region. A representative tape-pull adhesion test and an optical micrograph of a spontaneously failed base electrode scribe are shown in Figure 20.

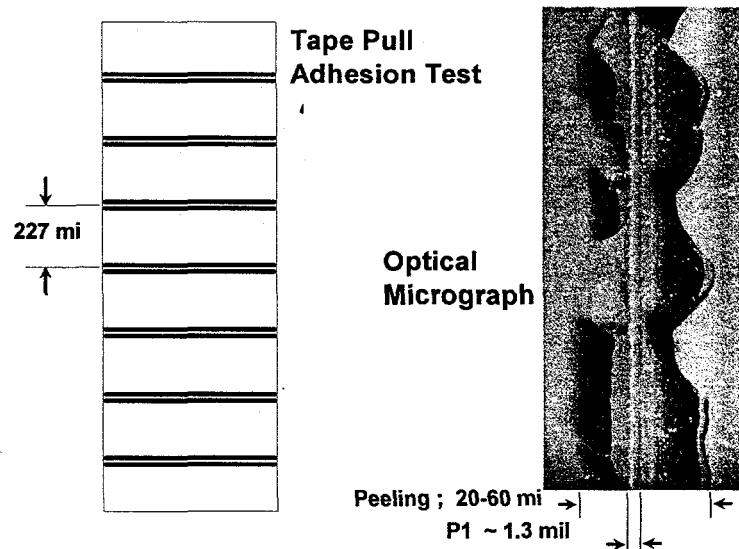


Figure 20. Near-interconnect adhesion failure.

Impact of Defects

Defects can reduce module output through reduced collection area (such as the lack of transparent conductor), shunting (adhesion failure before or during transparent conductor deposition), and durability (marginal interconnect adhesion). Although prevention of the formation of these defects was the primary thrust of our investigation, most shunting defects could be located and removed from a finished device, with a resulting improvement in device performance. Figure 21 shows two I-V curves for the same 60 cm^2 module before and after such defect microsurgery. For the module in question this resulted in a 9 rel% increase in efficiency. The improvement can be even more dramatic for defect-rich substrates if one has the patience and skill to isolate these defects.

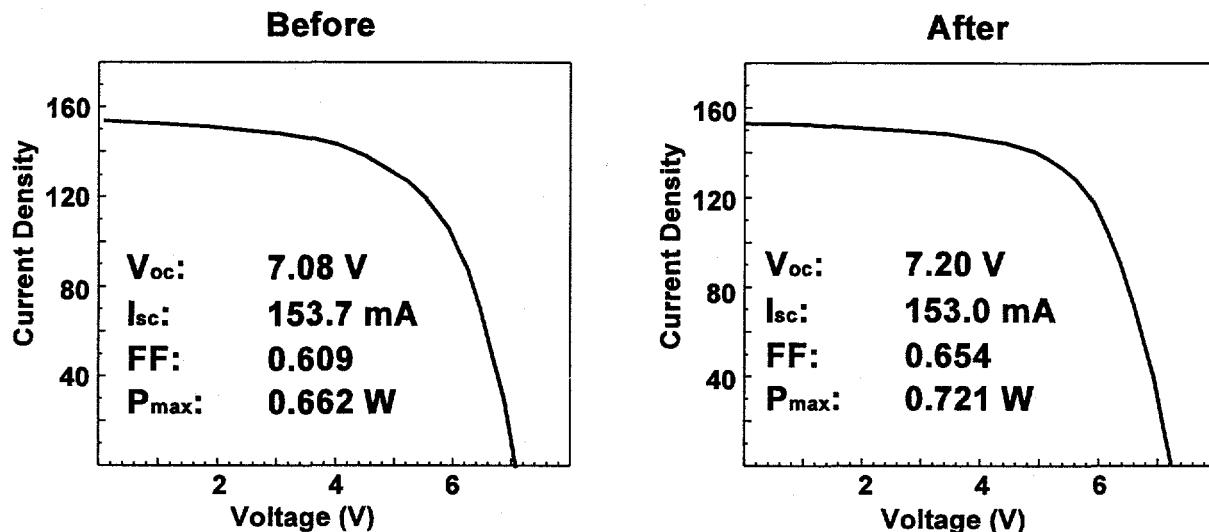


Figure 21. Impact of defect repair on modules .

Defect Diagnostics

Much of the effort in Phase 2 was to develop diagnostics for evaluating substrates and substrate preparation techniques. One such diagnostic that is extremely powerful is OBIC, but this tool requires fabrication of complete devices, can introduce features that are not substrate-related and is cumbersome.

Annealing Mo-coated substrates in moist air in an oven at 525°C for 10 minutes creates visual images essentially identical to those produced using OBIC. Figure 19 is an OBIC image of a cell in which a scratch was made in the glass underneath the base electrode. Evident in both the OBIC image and the air annealed samples are the circular dark spots, many of which exhibit a characteristic concentric "ring" feature. Likewise, in the corresponding scratch in the air-annealed sample and the OBIC near the scratch exhibit the same halo effect along the length of the scratch.

This imaging technique greatly improves the capability of quickly evaluating various substrates and substrate preparation techniques and has proven to be successful at predicting the behavior of substrates in the fabrication of CIS cells and modules.

Substrates and Substrate Preparation

The substrate can affect the CIS cells and modules by means of its composition, mechanical properties, surface chemistry, and surface condition. Several groups have begun to study the influence of these various contributors to the behavior of CIS [9, 36]. Soda-lime glass is desirable because it is abundant, smooth, an insulator, cheap and reasonably inert. All of the highest efficiency devices reported have been made using soda-lime glass as the substrate material. One of the key objectives of this contract was to achieve the performance milestones utilizing low-cost substrates.

Soda-lime glass can be contrasted with significantly different glasses, such as Corning 7059. Figure 22 is an OBIC image of cells made on 7059, in which there are virtually no defect features. Barely visible in this image is a scratch that was made in the substrate (across the left of the picture) that is identical in size to the one imaged in Figure 19. Cells made on 7059 glass, however, are typically 20-40% lower in performance, limited by poor voltage.



Figure 22. OBIC image of cells on 7059 substrate.

Figure 23 is an SEM image of air-annealed molybdenum-coated soda-lime glass on a scratched substrate. Figure 24 is an identical sample on 7059 glass. There are tremendous morphological structural features in the soda-lime glass that are completely absent from the 7059 sample. Figures 25 and 26 are SEM close-up views of the regions near the scratch for these two substrates.

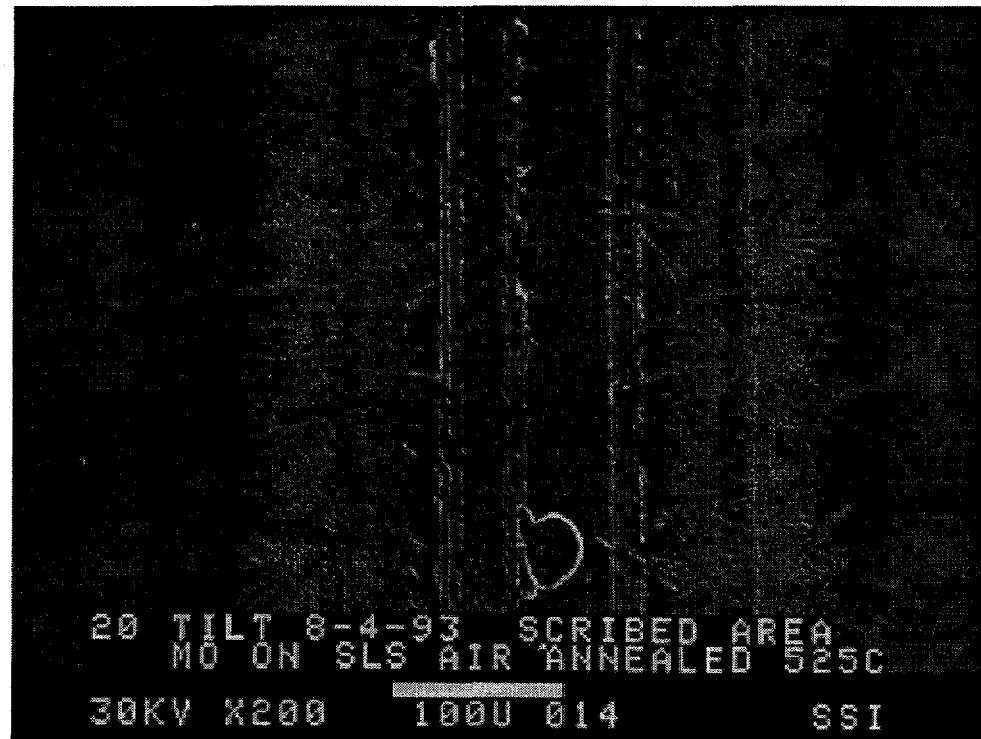


Figure. 23. SEM of air-annealed molybdenum in scratched region on soda-lime glass.

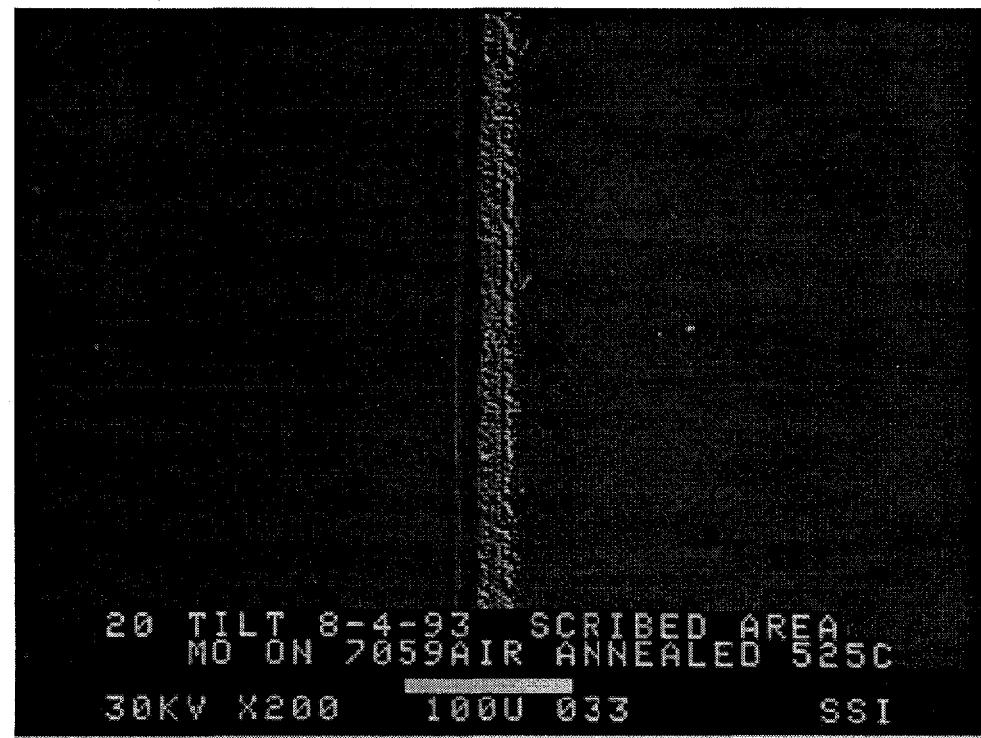


Figure 24. SEM of air-annealed molybdenum in scratched region on 7059 glass.



Figure 25. SEM Cross-section of air-annealed molybdenum in scribed region on soda-lime glass.

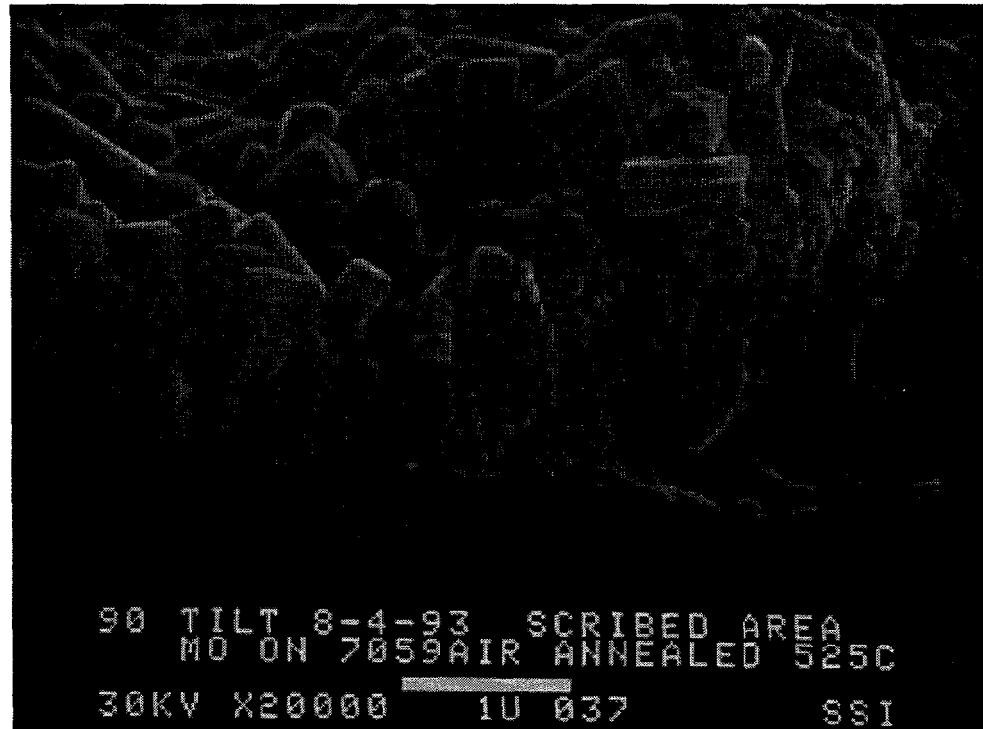


Figure 26. SEM cross-section of air-annealed molybdenum in scribed region on 7059 glass.

A number of techniques for substrate preparation, aimed at a low-cost scalable process, were under investigation during Phase 2, including polishing, etching, coating, surface modifiers and wash methods. Substrate samples from various vendors were also tested. The air annealing technique greatly improved the ability to screen these samples and techniques and predict the probable occurrence of defects.

In general, substrates that produce few defects in CIS appear defect-free through the air-annealing diagnostic. SSI is continuing to evaluate the most effective approaches to mitigating substrate-induced defects, and applying these techniques to large-area processing.

Interconnects

This section details the development of alternate strategies for fabricating interconnects and diagnostics implemented for characterizing and quantifying interconnect performance. During Phase 2, a new champion unencapsulated module was produced with 11.7% efficiency for a 60 cm² aperture area 14-cell module.

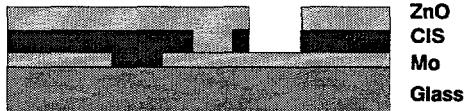
Alternate Patterning Strategies

One alternative to solving the near-interconnect adhesion problems for CIS modules is to avoid it. If the interconnect can be formed after the absorber formation process is performed, the problem disappears because there are no patterns. Two such approaches were demonstrated on CIS modules during Phase 2 [34,16]. Figure 27 is a cross-section view of three interconnect strategies for forming a thin film photovoltaic module interconnect.

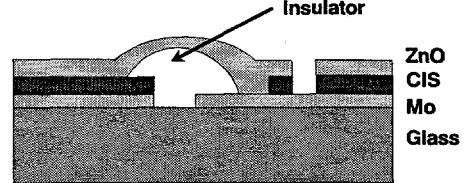
The standard interconnect consists of three cuts: an isolation scribe in the base electrode (before absorber formation), an interconnect via through the absorber to the base electrode (before the transparent conductor deposition), and an isolation cut in the transparent conductor (after transparent conductor deposition).

The post absorber interconnect consists of three cuts and deposition of a line of insulating material. After the absorber formation process, the entire stack of CIS/Mo is cut with a laser, a line of insulating material (usually a polymer) is applied over the cut to prevent shunting, and the module is completed as in the standard

STANDARD INTERCONNECT



POST-ABSORBER INTERCONNECT



POST-DEVICE INTERCONNECT

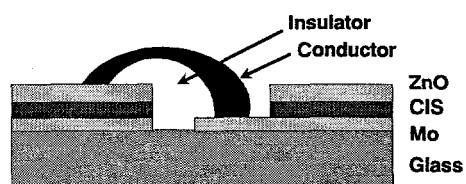


Figure 27. Interconnect cross-sections.

interconnect: a via is cut through the absorber to the base electrode before the transparent conductor is deposited and an isolation cut in the transparent conductor is made after it is deposited. This approach has the advantage that there are no near-scribe adhesion problems, but has the added complexity of depositing the insulator.

The post device interconnect consists of two or three cuts and deposition of two materials: an insulator and a conductor. All patterning steps are performed after the complete device stack is finished. The entire ZnO/CIS/Mo stack is cut with a laser, a via landing/ZnO isolation scribe is performed adjacent to the cut, an insulating material is deposited over the base electrode cut to avoid shunting, and finally a conductive material is deposited over the insulator to connect the transparent conductor of one cell to the base electrode of the next. This approach has the advantage of postponing all patterning steps until after all sensitive deposition steps are completed, but has the added complexity of deposition of two extra materials, an insulator and a conductor.

Unencapsulated Module Results

These techniques have been successfully applied to CIS modules. The best unencapsulated module results utilizing these strategies are shown in Figure 28.

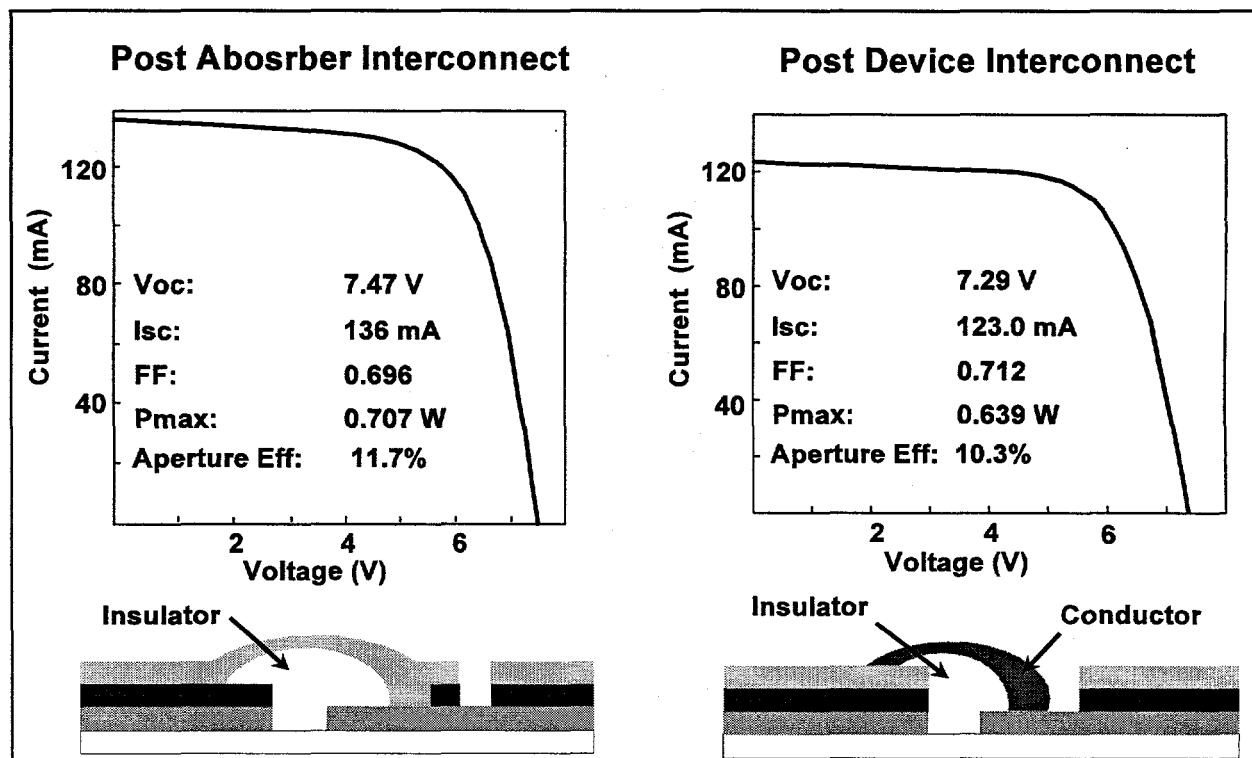


Figure 28. Champion module performance for alternate interconnects. (100 mW/cm² ASTM air mass 1.5 global spectrum, 25°C)

Interconnect Diagnostics

Two techniques for evaluating interconnects have been developed and are detailed in this section. The first is a method for quantifying series resistance effects in finished modules, called "dark forward bias voltage mapping", and the second is an alternate structure that can be fabricated to evaluate interconnect performance even through environmental testing in an encapsulated package, called an "interconnect test structure".

Dark Forward Bias Voltage Mapping

A brief review of this technique was discussed in the Phase 1 section [37, 38], but the value and further refinements of the technique warrant further review. A single very high interconnect resistance can render an entire module unusable (taken in the upper limit, a single open interconnect would prevent any current flow). Control of the process parameters such as cutting speed, tip pressure and laser settings is straightforward, but the interconnect via contact resistance is difficult to control with a direct feedback diagnostic because the contact is not made until a later stage in the process. To evaluate the interconnect series resistance, this simple non-destructive diagnostic for modules was developed for initial setup and periodic process qualification. The apparatus is illustrated schematically in Figure 29, which employs a power supply and a voltmeter. The power supply is used to flow current through the module circuit in the dark in the forward bias direction near the one-sun short circuit current value. The voltmeter is then used to measure voltage drop from cell to cell. This voltage should be roughly equivalent to the one-sun open-circuit voltage of each cell. Higher values indicate high series resistance. A section of a module that appeared to have a blocking junction (negative curvature in the I-V curve near V_{oc}) (Figure 6, 30) was analyzed using this technique, and it was found that the poor fill factor was being caused by several high-resistance interconnects (Figure 7, 31). Eliminating these high resistance interconnects greatly improves average module performance.

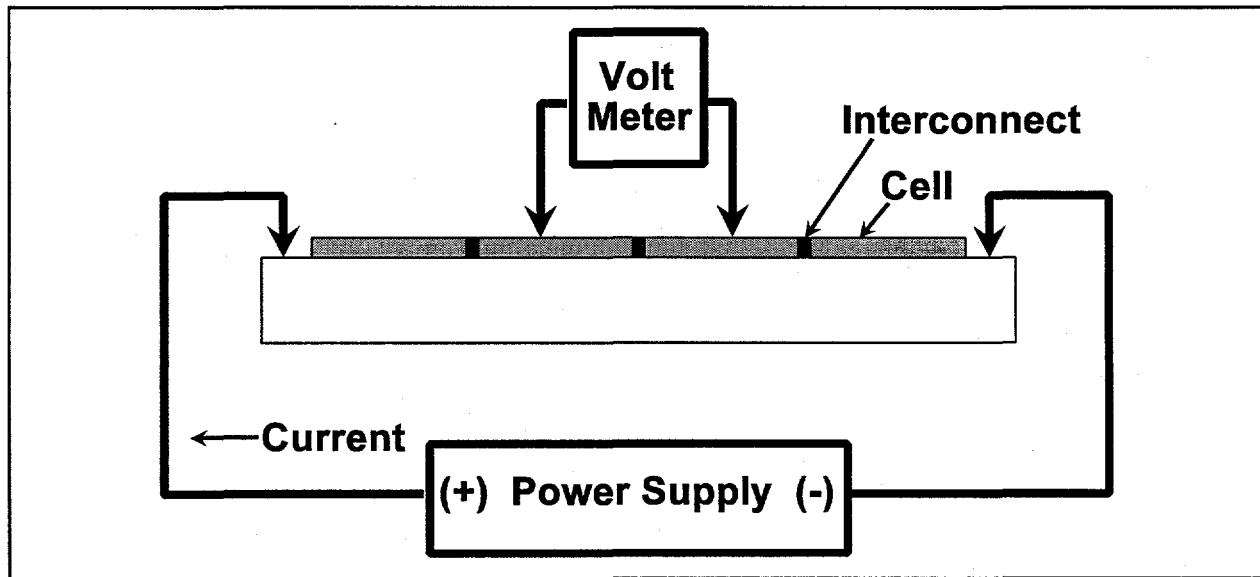


Figure 29. Dark forward bias interconnect diagnostic apparatus.

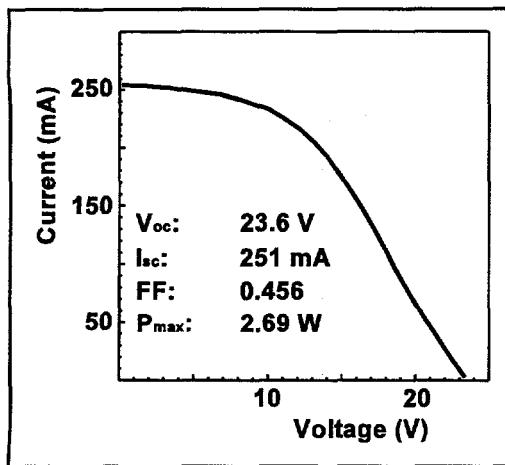


Figure 30. I-V curve of low FF module slice.

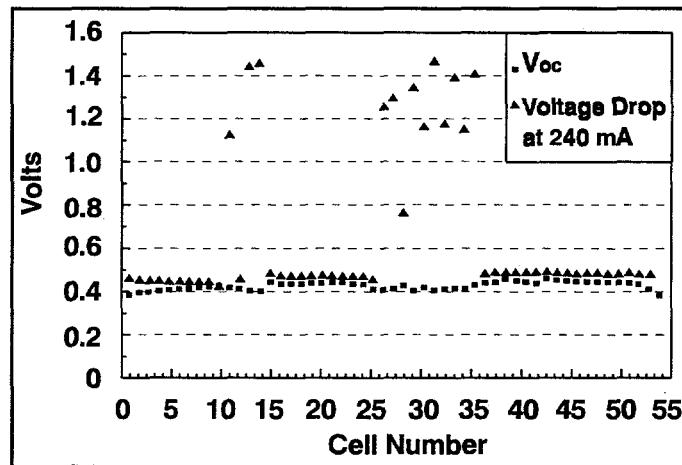


Figure 31. Dark forward bias voltage data for module in Figure 30.

Interconnect Test Structures

To evaluate interconnect performance independent of cell material effects, and to evaluate the effectiveness of the various components of the alternate interconnect strategies, a number of "interconnect test structures" were developed. These are essentially module plates with double back-to-back interconnects along the current path length of the module, illustrated in Figure 32. The structure can then be measured for resistance changes either from one end to the other (through a number of interconnects) or individually. The structure can also be laminated and subjected to environmental testing to evaluate the durability of various interconnects and interconnect materials. Cross-sectional views of the various interconnect test structures that can be used for evaluating the new alternate interconnects are illustrated in Figure 33.

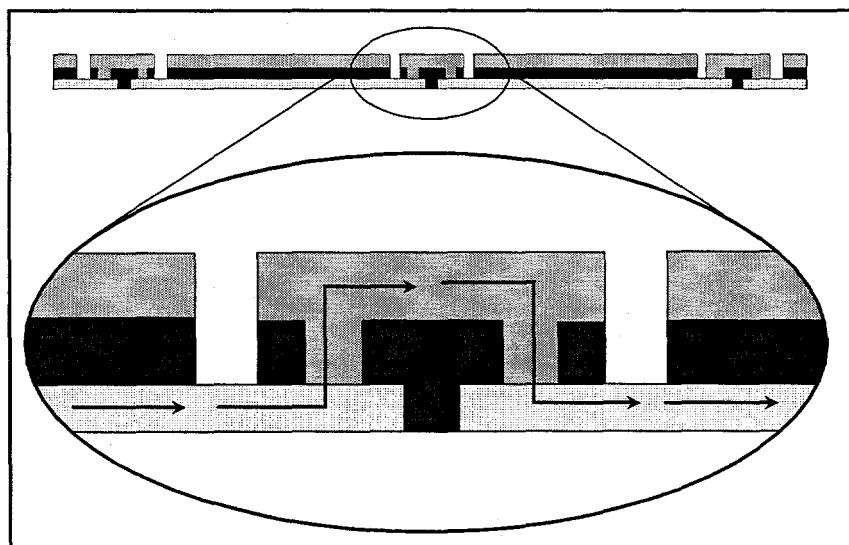


Figure 32. Standard interconnect test structure.

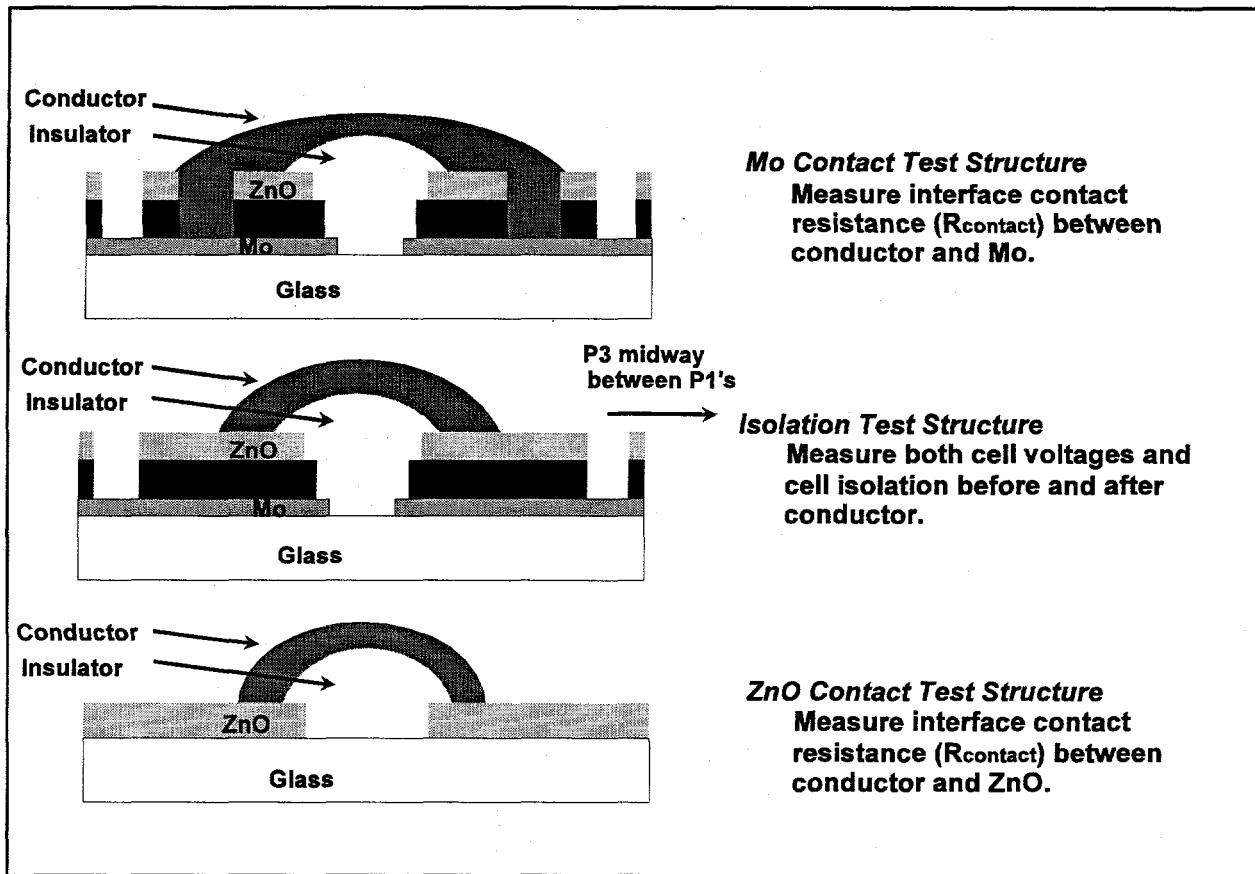


Figure 33. Alternate interconnect test structures.

Module Durability

Graded absorber materials appear stable through lamination heat and pressure cycles. Figure 34 is a distribution plot of the change in performance for 851 cells, split into two groups and subjected to the lamination thermal cycle and thermal & pressure cycle, using mylar as a protective layer to enable retesting of the devices. No statistically significant change in cell performance was noted.

A topic related to the evaluation of module stability is the peculiar behavior of CIS materials upon exposure to sunlight: many of them improve significantly when exposed to light, and generally better cells exhibit less relative improvement. This phenomena has been observed by several groups [39-41]. As shown in Figure 35, there are two basic populations of low-performing cells. The first group shows a monotonic relationship of greater relative improvement on light soaking with lower initial performance; the performance of these cells appears to be dominated by absorber/junction behavior. The second exhibits no effect whatsoever; the performance of these cells is dominated by physical defects. The effects are reversible; improvements that are seen in a few minutes disappear over a 24-48 hour period in SSI devices.

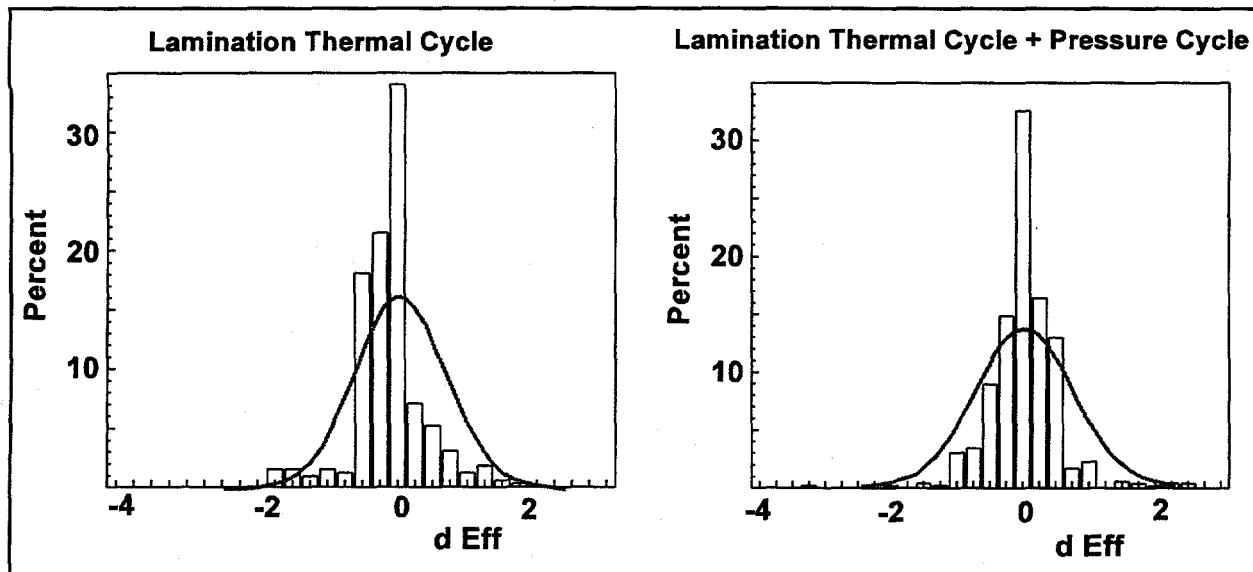


Figure 34. Device performance through lamination cycle.

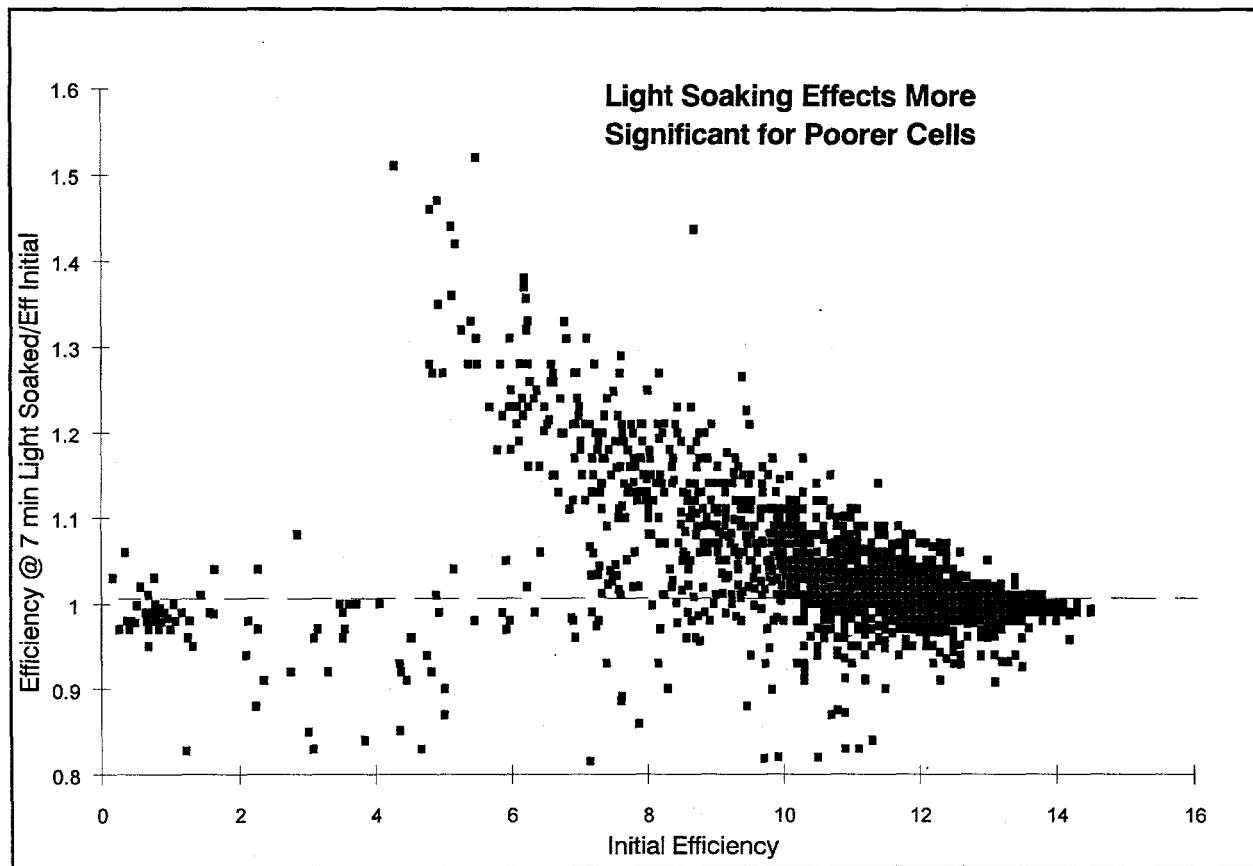


Figure 35. Light soaking effects.

The fundamental mechanism for this behavior may hold the key to greatly improved performance of CIS cells and modules. This behavior also points out the extreme caution that must be exercised when attributing changes in performance to environmental testing, in that the testing methodology must correct for these effects.

In addition to NREL's outdoor exposure testing of CIS modules, SSI continued to monitor a number of CIS modules subjected to outdoor exposure at the Camarillo, California site. Figure 36 illustrates the behavior of these modules. Many modules show the same stable behavior as those monitored at NREL, but some do exhibit a loss in performance which is attributed to the interconnect reliability issues highlighted in this section.

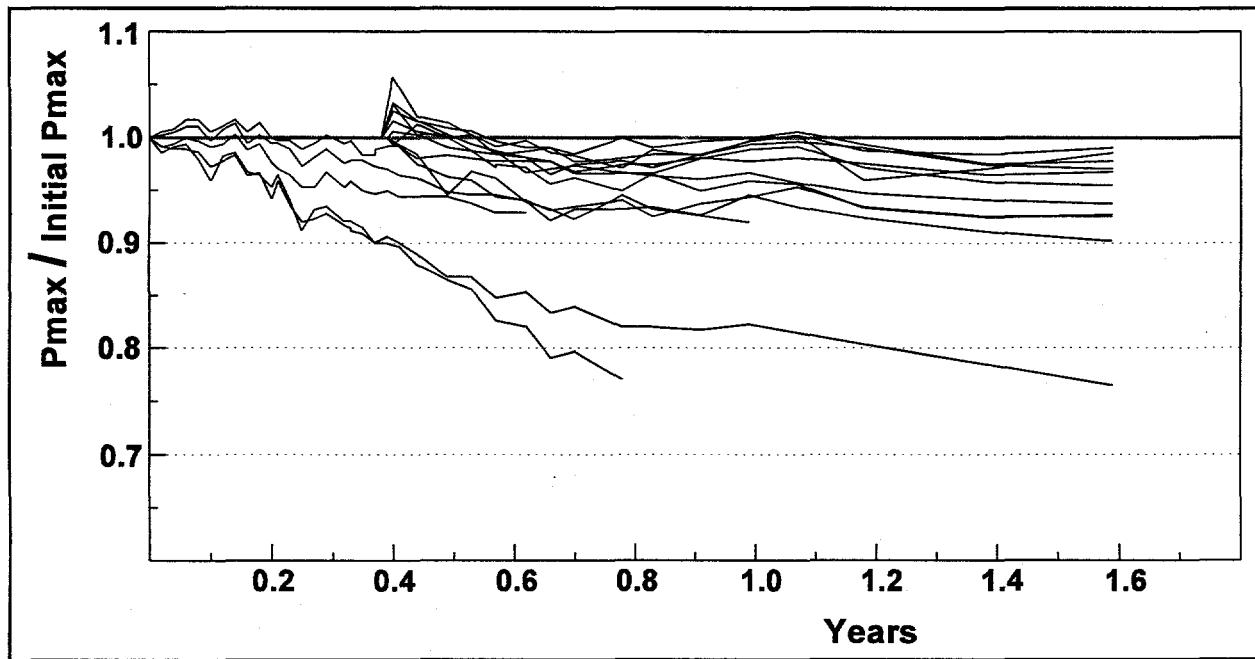


Figure 36. SSI outdoor module performance summary.
(100 mW/cm² ASTM air mass 1.5 global spectrum, 25°C)

Phase 3

Overview

In Phase 1, the emphasis of the research effort was on establishing the baseline large area CIS module fabrication processes including detailed characterization of the cells and interconnects. Environmental durability of laminated and framed large-area CIS modules was also demonstrated [42].

In Phase 2, the initial focus was to implement the processing and characterization methods demonstrated in Phase 1 to meet the contract deliverables schedule and to produce statistically significant quantities of large area modules for outdoor and accelerated environmental testing. Over 2300 1x4 foot CIS modules were fabricated. Phase 2 champion module efficiency was 9.7%. The distribution of module efficiencies peaked at about 8%.

Although the process produced high-efficiency cells and modules, the yield of these modules was poor. The origins of module reproducibility problems were unclear. Large area module fabrication was temporarily suspended to determine the critical issues affecting yield losses in module fabrication by using small area test devices (3.3 cm^2 active area cells) and modules (60 cm^2 aperture area) as the experimental test bed. This shift greatly enhanced the ability to identify root causes of yield loss in module fabrication. The most critical issues determining module yield were grouped into three major categories:

1. The uniformity and reproducibility of the absorber formation process dominates the fundamental performance of the material over a large area.
2. The interaction of the substrate with the films requires appropriate substrate selection and preparation to minimize defects that lead to shunting and areas of poor photoresponse.
3. Performance losses near interconnects can reduce module performance and can cause inadequate performance through module durability testing.

The issues in categories one and two were addressed through the adoption and further refinement of a graded absorber formation process in which the surface layer of CIS incorporates sulfur [9], combined with the appropriate substrate preparation. Performance losses near interconnects were addressed by developing alternate techniques for fabricating interconnects. Interconnects were made after the formation of the absorber by application of insulating and/or conducting materials. Prior to development of these alternate techniques, "classic" interconnects incorporated a pattern in the base electrode prior to the reaction of precursors to form CIS [42]. The alternate patterning techniques culminated in the demonstration of a CIS record 11.7% aperture area efficiency integrated mini-module.

In Phase 3, addressing the three critical issues defined in Phase 2 was continued and extended. Substrate and base electrode preparation techniques were developed which minimize the number of defects that lead to shunting, areas of poor photoresponse and losses near interconnects. These Phase 3 techniques are distinct from the techniques developed in Phase 2.

Studies of the interactions between the substrate, base electrode, precursors and the reaction process allowed the development of the distinct Phase 3 base electrode preparation techniques. Parallel developments in each of these areas eliminated the need for the alternate patterning techniques developed in Phase 2. For example, modification of the reaction process was necessary to avoid loss of adhesion when using the Phase 3

substrate and back electrode preparation techniques. SIMS depth profiles indicate a significantly reduced degree of reaction of the base electrode, particularly with selenium. The combined effect of improvements in substrate/base electrode preparation techniques and reaction process have allowed the return to the more production capable "classic" patterning, reduced the number of substrate-induced defects, and resulted in champion module efficiencies with an encapsulated 12.8% efficient minimodule on 68.9 cm² and an NREL-verified 12.7% efficient circuit on 69 cm² with a prismatic cover (excellent agreement between NREL and SSI solar simular measurements were again demonstrated during Phase 3). Development of this electrode preparation technique was expedited by process screening based on observation of alternative base electrodes after oxidation in moist air.

This champion encapsulated mini-module efficiency is the highest mini-module efficiency for any thin film technology. A record large area (3860 cm²) encapsulated module efficiency of 10.3% has also been demonstrated (verified by NREL). Additional contract deliverables included 4 encapsulated large area modules (~3870 cm²) for reliability testing at NREL. SSI also supplied NREL with a one kilowatt array of large area (~3890 cm²) approximately 30 watt modules. The NREL verified performance of this array represents a significant step toward meeting the efficiency target of the U.S. DOE Five-Year Plan Goals of 8-10% efficient commercial thin film flat plate modules.

The major challenge to move from development to production is to improve reproducibility rather than to improve champion device efficiencies. Therefore, emphasis has been placed on reduction of process variation. The reduction of variation efforts are based on the application of the statistical process control (SPC) discipline, improved diagnostics, and improved protocols. Using statistical analysis has demonstrated that the largest source of variation in the current process is due to the block of process steps from CdS dip through final patterning. The second largest source of variation is from the block of process steps prior to the reaction process. The reaction process and testing introduce relatively low variation for this data set. The largest sources of variation are naturally addressed first. Significant progress has been made in the reduction of variation that is related to CdS deposition.

Reduction of variation efforts also accelerate progress in other tasks by providing a consistent and well defined baseline process.

Substrate and Base Electrode Studies

During Phase 2, alternative patterning techniques were developed to avoid poor adhesion near patterns in the base electrode. These techniques relied on forming interconnects after the formation of the absorber by applying insulating and/or conducting materials. Parallel and related efforts to reduce the number of defects using alternative substrate preparation and base electrode deposition techniques and alternative reaction process were begun during Phase 2. However, these approaches were not immediately successful. During Phase 3, improved understanding of the interactions between the substrate, base electrode, precursors and the reaction process allowed the development of glass/base electrode preparation techniques which simultaneously decreased the number of defects and improved adhesion near patterns in the base electrode. These developments were expedited by process screening based on observation of candidate substrate/base electrodes after oxidation in moist air. This section discusses substrate preparation and base electrode deposition studies. Reaction process changes to accommodate these glass/base electrode improvements are discussed in a later section.

Sputtering Conditions

Studies of the impact of sputtering conditions on base electrode properties were conducted prior to the contract and have been conducted throughout all phases of the contract. Prior to the contract, experiments demonstrated that efficiency is dependent on thicknesses of the base electrode and the pressure during its deposition. Base electrodes are typically deposited as multiple layers. For the base electrode approaches developed during both Phase 2 and Phase 3, experiments demonstrated the general trend of improving efficiency with decreasing thicknesses and decreasing pressure (Figure 37). Adhesion between base electrode and substrate is typically good; however, as with efficiency, adhesion between the base electrode and absorber layer may be dependent on conditions during deposition.

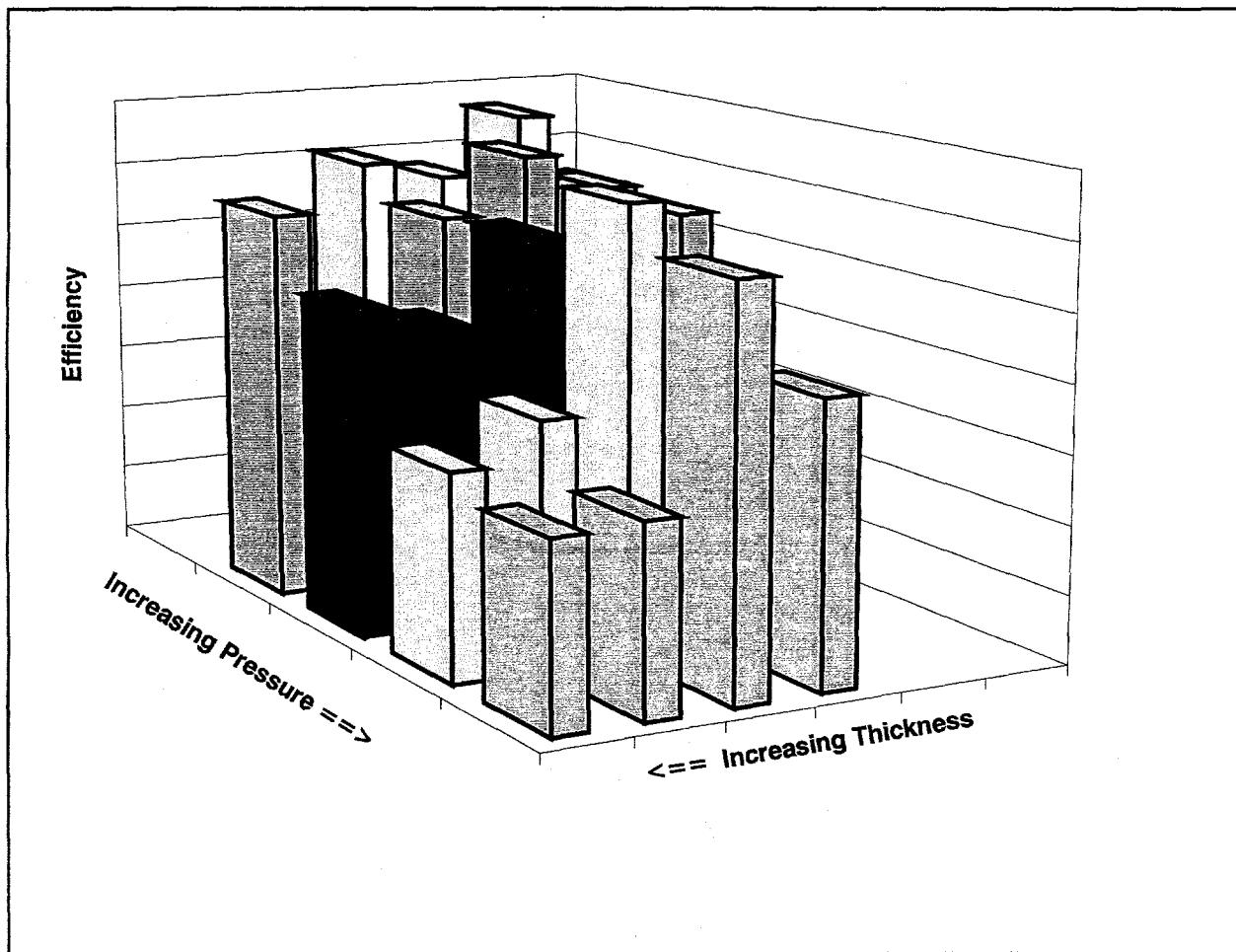


Figure 37. Improving efficiency with decreasing thicknesses and decreasing pressure.

Substrate and Base Electrode Studies

Criteria for base electrode selection include good ohmic contact to CIGSS, good adhesion to glass, the ability to survive in the hostile atmosphere of the reaction process, good conductivity and low cost. Molybdenum

is the most common choice to meet all of these criteria. Numerous substrate types, barrier layers (coatings) and substrate treatments were tested using the air anneal procedure discussed in the section on Phase 2 and by fabricating CIGSS devices. Typical samples included substrate and base electrode variation alone and in combination with scratches (simulated defects) and laser patterns in the base electrode. Substrate candidates included:

- Fused Silica
- Ba-borosilicate (Corning 7059)
- Borosilicate
- Alkali-borosilicate
- Alkali-aluminosilicate
- Sodalime
- Ba-boro-aluminosilicate

Barrier layer candidates included:

- TiB₂
- Cr₂O₃
- SiO₂
- MoSi₂
- Cr

Substrate treatments included:

- Cleaning
- HF Etching
- Acid Leach
- Polishing
- Lapping
- Ion etching

In the following, results from sodalime glass and Corning 7059 glass with standard substrate preparation and base electrode deposition techniques are compared as an example of the range of results observed. Corning 7059 glass has low sodium as compared with about 14% sodium for sodalime glass. The thermal expansion coefficient for 7059 glass is about half that of sodalime glass and 7059 glass typically has a pristine surface.

The appearance of Mo-coated sodalime glass after an air anneal varies from brown to a purple-grey. The appearance of similar films on 7059 glass after an air anneal is a uniform matte-grey. Regions of the base electrode adjacent to scratches, a pattern in the base electrode or defects are typically affected by the air anneal in a way that gives these regions an appearance that is distinct from the general appearance of the base electrode. The terms "affected zone" or "affected regions" will be used for these regions. This difference in visual appearance of the affected zone is used to anticipate differences during reaction to form CIGSS for similar discontinuities in the substrate or base electrode. For sodalime glass, the affected zone around a scratch or pattern in the base electrode extends for about 750 μm . For 7059 glass the affected zone adjacent to a scratch is minimal and the affected zone adjacent to a pattern in the base electrode extends for only 25 or 50 μm .

These results for air annealed Mo on sodalime and 7059 glasses parallel observations for the two glasses when they are used as the substrate for device fabrication. Adhesion testing and OBIC imaging indicates that the affected zone near patterns in the base electrode are narrow for 7059 glass and relatively wide for

sodalime glass. Similarly, defects in the substrate/base electrode do not affect as large a region around the defects for 7059 glass as they do for sodalime glass.

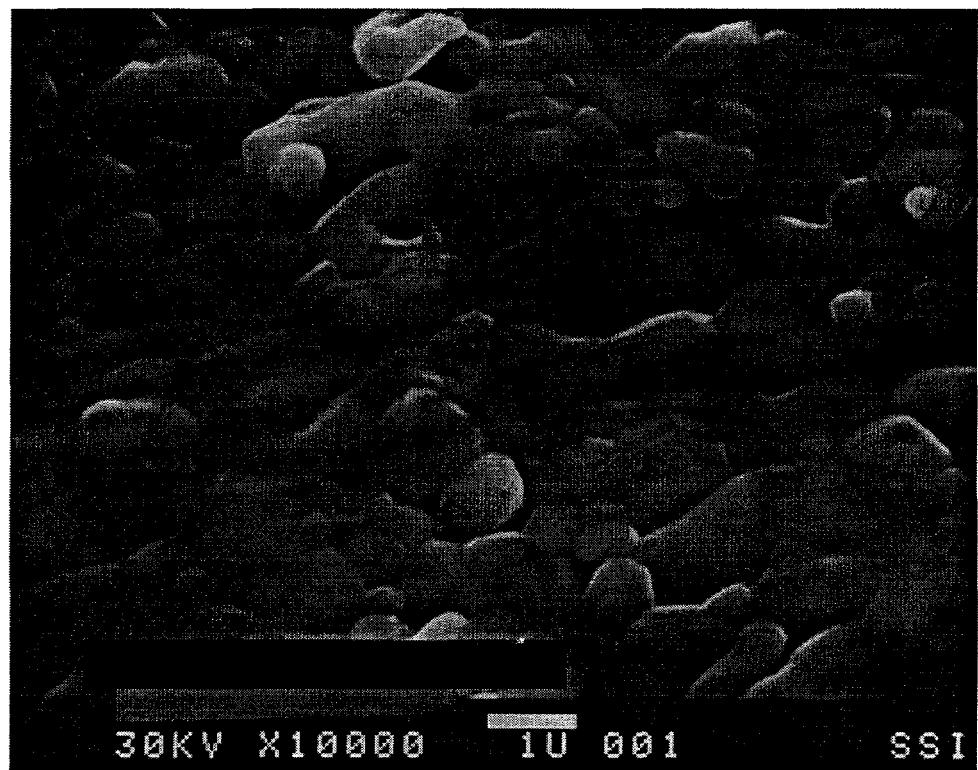
Although the affected zone around patterning lines and defects is small for 7059 glass, test structure cell performance is consistently poorer for 7059 glass than for sodalime glass. Therefore, air annealing is a survey technique that must be supported by device performance data. Differences in device performance may be related to surface quality (7059 glass has a pristine surface), differences in Na content, differences in expansion coefficient or, differences in CIGSS morphology (Figure 38). SEM micrographs of the affected region on air annealed sodalime glass indicate a change in local morphology. SIMS analysis at NREL indicates high Na concentrations in this region. Structures appear to emanate from the defect and across the surface of the base electrode (Figure 23, 39). This change in morphology is not apparent for 7059 glass substrates.

A possible explanation for the observed morphology is that sodium diffusion from the alkali glass substrates is more pronounced at discontinuities in the glass or base electrode. The existence and/or impact of discontinuities in the glass or base electrode are dependent on substrate preparation and base electrode deposition techniques. The combination of O₂, Mo and Na may cause the formation of compounds similar to a molybdenum bronze (Na_{0.9}Mo₆O₁₇). Mo bronzes have been formed by heating mixtures of MoO₃ and Na₂MoO₄ to 550°C [44, 45]. This model explains the relative extent of affected zones for sodalime glass and 7059 glass based on the availability of Na. However, attempts to identify the Mo bronze on air annealed samples by XRD have been unsuccessful. Selenium rather than oxygen may form similar compounds during reaction to form absorbers. Similar morphologies for air annealing and for annealing in selenium-containing atmospheres are observed.

Another hypothesis is that corrosion reactions produce the observed morphology of affected regions. Experiments were conducted to explore the role of corrosion in the development of affected regions. A standard base electrode was deposited on Corning 7059 and sodalime glass substrates. A pattern line was cut across the samples and electrical isolation of the two sides of the sample was verified. Leads were attached to the substrate and the two sides were electrically biased during air annealing. Despite the patterning, as the sodalime glass heated, current began to flow, indicating the presence of some conduction across the patterned base electrode. The sample was removed and inspected. The base electrode on the negative side of the isolation cut was much more corroded, especially near the pattern in the base electrode. No current flow and no corrosion was observed when 7059 glass was subjected to the same procedures.

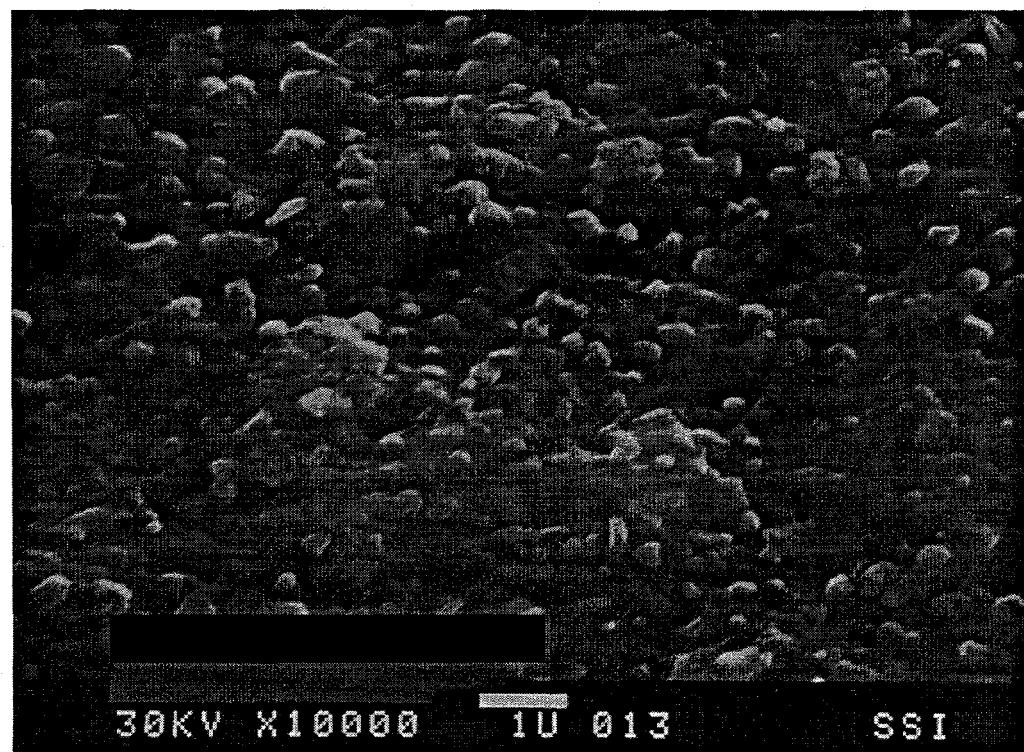
These experiments indicate that a corrosion mechanism involving Na may play a role in the development of affected regions. However, the connection between observations for air annealing and conditions during absorber formation has not been made conclusively. Additional exploration of the affected regions included annealing in inert gas (He) and hydride gases (H₂Se and H₂S). The reactions responsible for formation of the affected regions for air annealing, absorber formation and other experimental conditions were not determined conclusively. However, the air anneal procedure produces similar morphologies which has made the air annealing a useful survey technique for screening alternative substrate/base electrode preparation techniques.

The liquid crystal display (LCD) industry has experience with undesirable sodium diffusion from sodalime glass [46, 47]. Several companies are marketing low sodium or barrier coated glass to the LCD industry. However, low sodium glass is not a cost effective solution for the manufacture of large-area thin film photovoltaic modules. Surveying numerous substrate types, barrier layers and substrate treatments using the air anneal procedure has led to the development of a cost effective substrate option with minimal affected region. A glass/base electrode preparation technique has been demonstrated with good performance, good



30KV X10000 1U 001

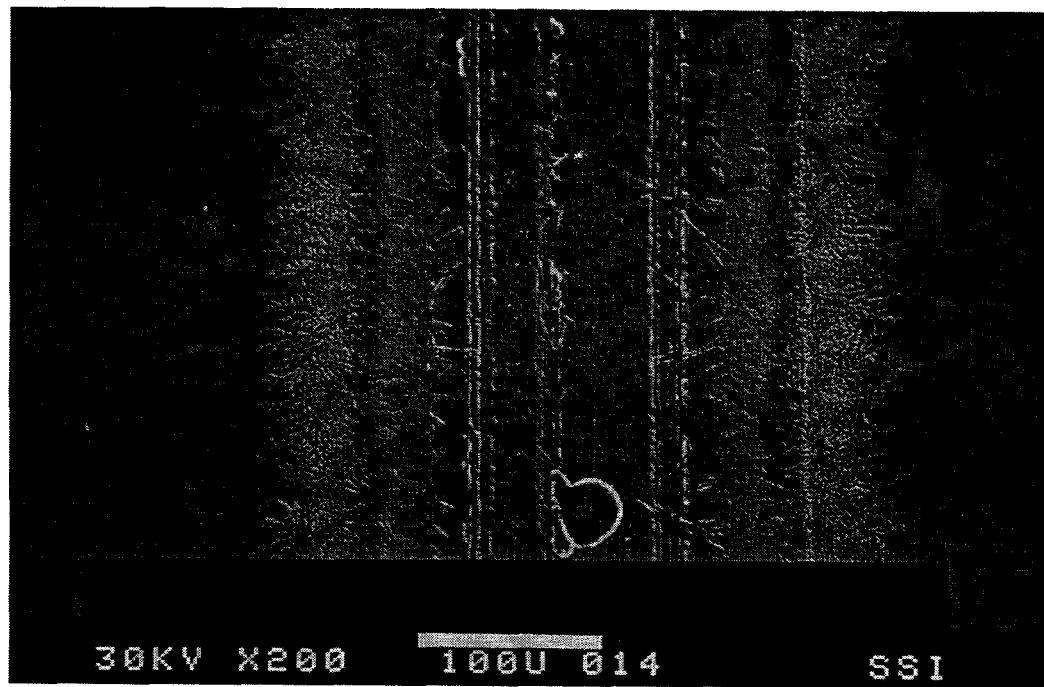
SSI



30KV X10000 1U 013

SSI

Figure 38. CIGSS morphology for SLG (top) and 7059 glass (bottom).



30KV X200

100U 014

SSI

Figure 39. SEM micrograph of the affected region on air annealed sodalime glass.

adhesion, minimal dead region as determined by OBIC scanning and good yields. OBIC images of gridded test structure devices are shown in Figure 40 for the substrate and base electrode preparation techniques used in Phases 1 and 2 versus Phase 3. Each image includes three devices. Three dark horizontal lines are visible on each device due to grid shadowing. A scratch which crosses the lower two devices in each image simulates the effect of patterning the base electrode for a module. For the preparation techniques used in Phases 1 and 2, the effect of the scratch is clearly visible as a linear feature with degraded performance. A large number of randomly located low performance dark spots are also visible which are due to defects in the base electrode or substrate [33]. Similar effects around actual interconnects dictated the development of the post absorber formation techniques for fabricating interconnects during Phase 2. For the preparation techniques used in Phase 3, the scratch has minimal affect on performance; there are few defects related to the base electrode or substrate. Later sections of this report discuss reaction process changes to accommodate these glass/base electrode improvements and the implications of these developments on module design.

Absorber Structure

Criteria for definition of a production capable absorber formation reaction process include good efficiency, uniformity and yield. An additional criteria is compatibility with changes in glass/base electrode fabrication techniques. Efforts to improve the performance and understanding of the graded absorber structure will be discussed in this section. Reaction variations, precursor variations, measurements and modeling will be discussed. The main emphasis will be on alterations to the reaction process in concert with changes in the base electrode preparation techniques which allowed return to "classic patterning."

Reaction Studies

During Phase 3, improved understanding of the interactions between the substrate, base electrode, precursors and the reaction process allowed the development of distinct Phase 3 substrate and base electrode preparation techniques. As with the Phase 2 techniques, these Phase 3 techniques minimized the number of defects that led to shunting. However, the Phase 3 techniques also minimized areas of poor adhesion near interconnects and allowed the return to "classic patterning". Modifications of the reaction process were necessary to avoid loss of adhesion with the Phase 3 substrate and back electrode preparation techniques. In general, simultaneous improvement or alteration of multiple process steps is necessary for progress. Assignment of any one attribute to the improvement in any one process step is somewhat artificial.

Figure 41 shows efficiency results for a series of variations in reaction conditions. In this and other experiments, design of experiment methods (Taguchi Methods) were used to select variations in the absorber formation process parameters such as reaction time, reaction temperature and reactant concentrations. In Figure 41, the results from eight reaction condition groups with about 128 test structure cells in each group are labeled with a letter above the group. Some processes, such as process A, led to poor efficiency. Process C leads to poor yield. Distinctions between the efficiency for other groups are less clear. However, beneficial features of certain sets of reaction conditions are observed that are not obvious in the efficiency data alone. For example, the SEM micrographs in Figure 42 are from reaction process D (top) and F (bottom). The thickness of the Mo prior to reaction was the same for both of these processes. Reaction causes an expansion of the Mo base electrode due to reaction with Se. The Mo thickness after reaction is an indication of the degree of reaction between Mo and Se. Although the yield and efficiencies are similar

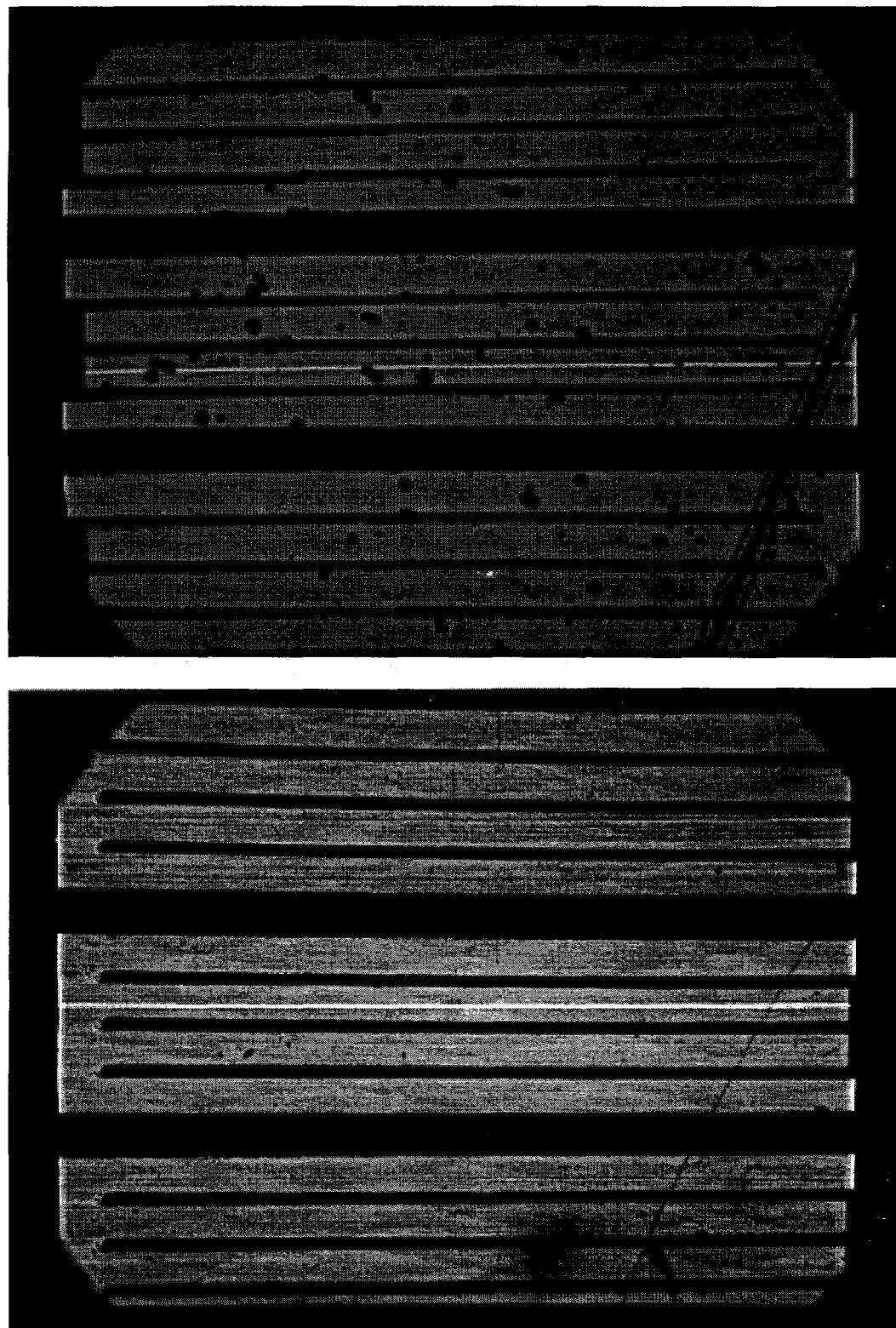


Figure 40. OBIC images representative of Phases 1 and 2 (top) and Phase 3 (bottom) substrate and base electrode preparation techniques.

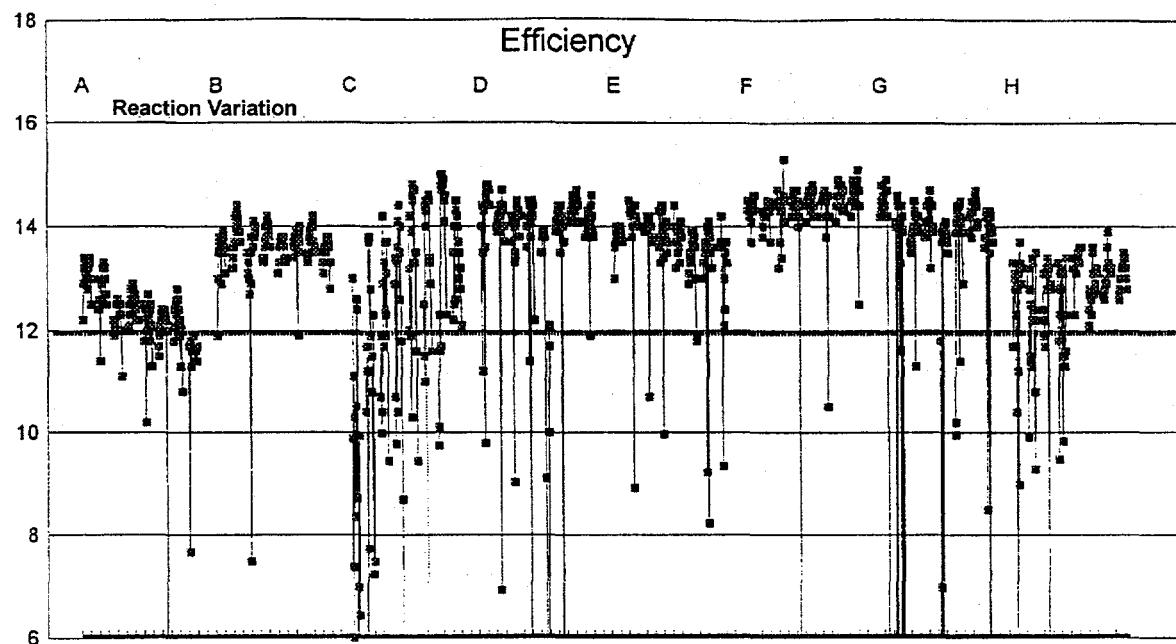
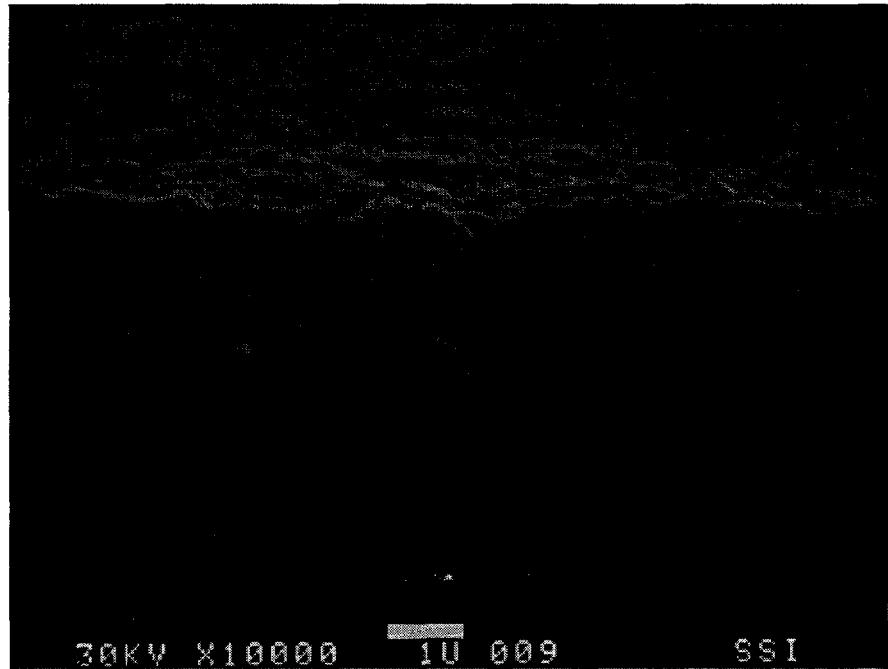
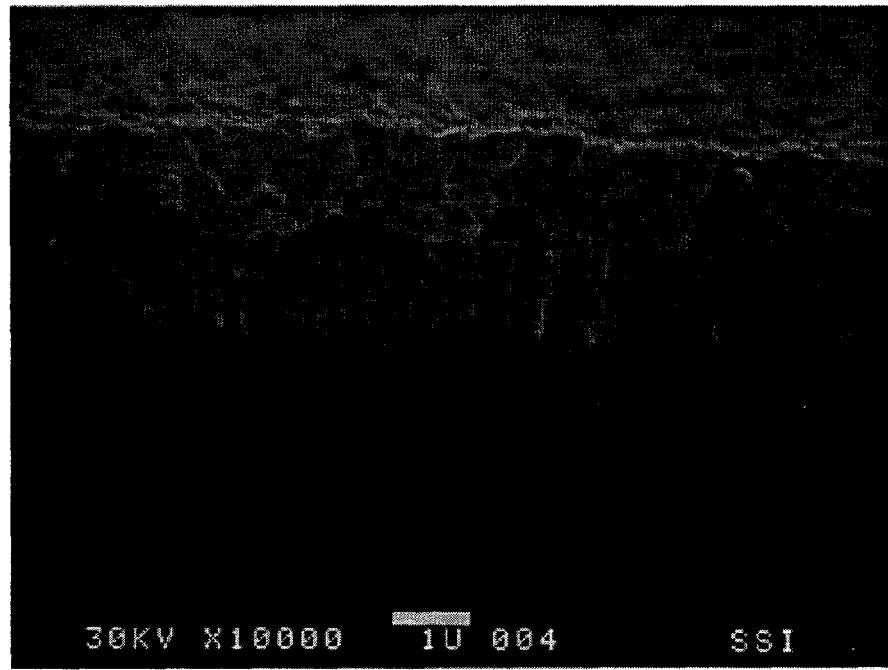


Figure 41. Efficiency results for a series of variations in reaction conditions.



30KV X10000 10 009

SSI



30KV X10000 10 004

SSI

Figure 42. SEM images for two reaction conditions showing differences in the degree of reaction with Mo. See text for description.

for the two sets of reaction conditions, the degree of reaction with the Mo base electrode is considerably lower for the F process conditions.

SIMS depth profiles supplied by NREL, Figure 43, characterize the differences for the two sets of reaction conditions of Figures 42. Elements are labeled as the profiled element plus Cs which reflects the use of techniques developed at NREL to improve the quality of SIMS profiling [48]. The Se, S, Ga and In depth profiles in the absorber layers are typical of the SSI graded absorber reaction process [9]. For the set of reaction conditions of process D (left), a layer of Mo reacted with Se is indicated in the central section of the depth profile by a broad plateau with a high Mo signal along with a high Se signal. For the set of reaction conditions of process F (right), the layer of Mo reacted with Se is significantly thinner. The reaction conditions of process D with the higher degree of reaction with Mo was found to periodically yield poor adhesion between the Mo and the substrate. Reaction conditions of process F consistently yield good adhesion for the Phase 3 substrate/base electrode process. Although the distinction between the efficiency for the two processes groups was minimal, improvements in adhesion are obtained for only one. This reaction process dependent improvement in adhesion for alternative substrate/base electrode fabrication techniques is one part of the overall process change which has allowed return to "classic patterning" (discussed in a later section).

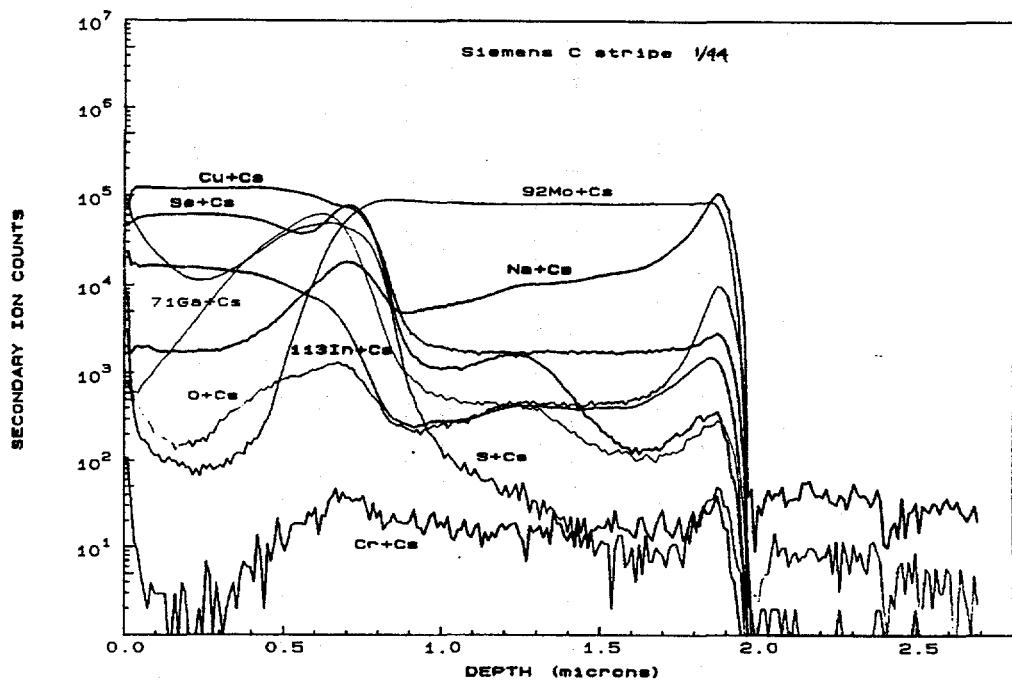
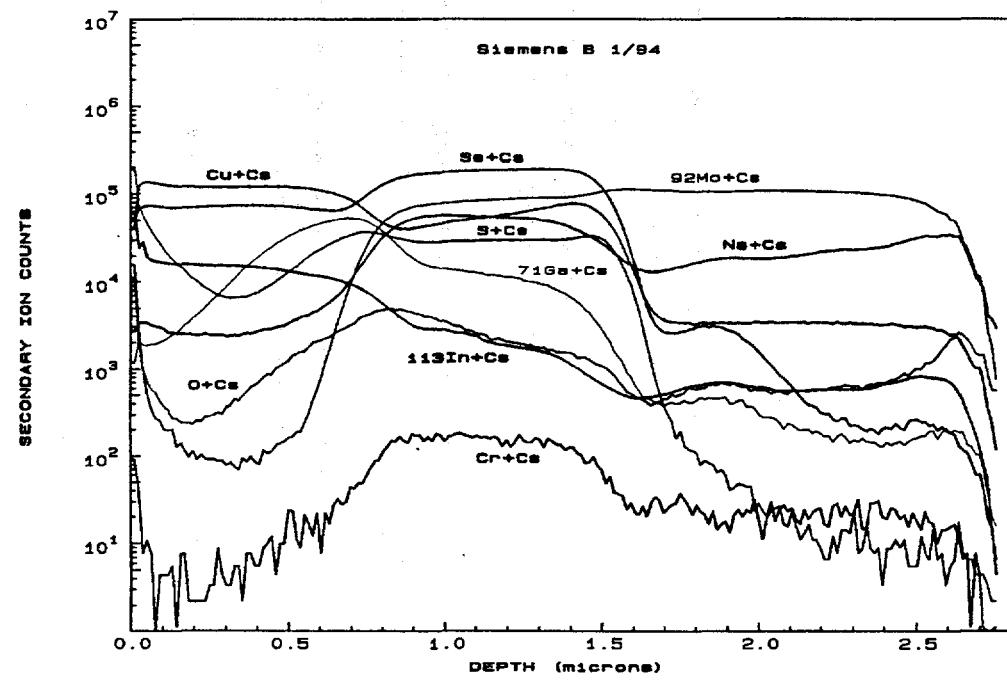
Precursor Studies

Variations in precursor deposition conditions have been studied to improve efficiency, uniformity and yield. Spectral response measurements of graded absorber devices indicate potential improvements for changes in absorber layer thickness, Ga and/or S concentration profiles in the absorber, reaction condition changes or precursor changes. Although the bandgap in the bulk of the sulfur graded absorber is near the bandgap of CIS without sulfur, spectral response measurements indicate a loss in current due to reduced collection at the long wavelength end of the active spectral range for CIS. This section will discuss efforts to improve the efficiency by regaining this lost current and other potential improvements related to changes in precursor deposition conditions.

Figure 44 shows efficiency results for a series of variations in precursor deposition conditions for constant graded absorber reaction conditions. Precursor deposition conditions including power, thickness and other deposition details were varied. In Figure 44, the results from ten precursor deposition variations with about 64 test structure cells in each group are labeled with a letter above the group.

The square of the quantum efficiency for data near the bandgap, which is proportional to absorption for simplifying assumptions, is plotted in Figure 45 for the groups of precursor deposition conditions of Figure 44. Linear extrapolation to zero quantum efficiency is used as an indicator of relative band gap in the base of the absorber although it is recognized that this is an oversimplification for a graded absorber structure. Letters adjacent to groups of devices with similar character in this plot refer to the precursor groups in Figure 44. The thickness for these groups is also indicated by labels indicating the percent thickness relative to "baseline" thickness ($\sim 1.2\mu\text{m}$). Improvements in short circuit current relative to baseline thickness devices is given in an insert.

Groups with thicker than baseline precursors are seen to have improved quantum efficiency. Five and seven percent improvements in short circuit current are observed for absorber thickness of 150% and 200% of baseline absorber thickness respectively. However, the improved quantum efficiency does not necessarily lead to improved efficiency. Open circuit voltage is lower for the cells with higher short circuit currents. Counter-varying current and voltage trends were reported for variations in reaction conditions which led to



Results from S. Asher, NREL

Figure 43. SIMS depth profiles supplied by NREL characterize the differences for the two sets of reaction conditions of Figures 42.

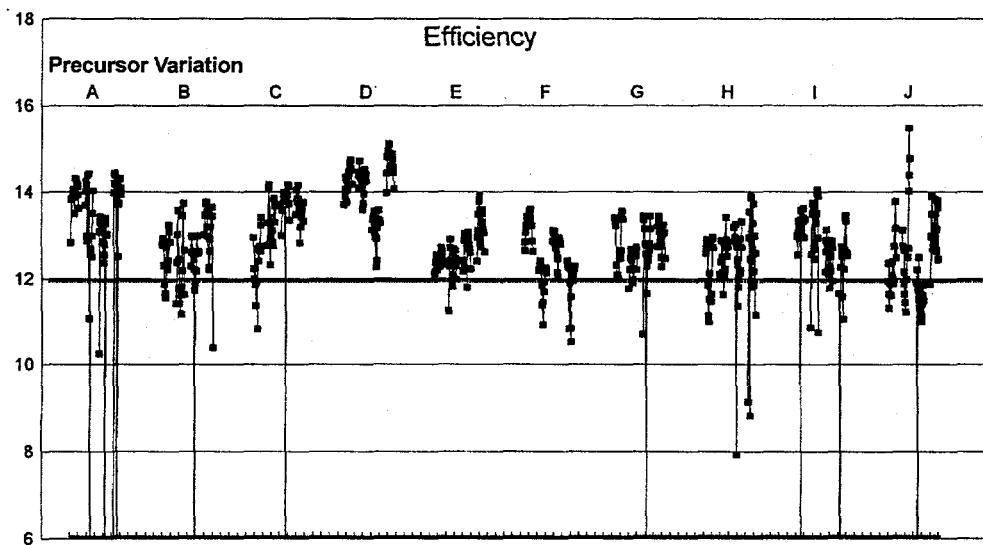


Figure 44. Efficiency results for a series of variations in precursor deposition conditions for constant graded absorber reaction conditions.

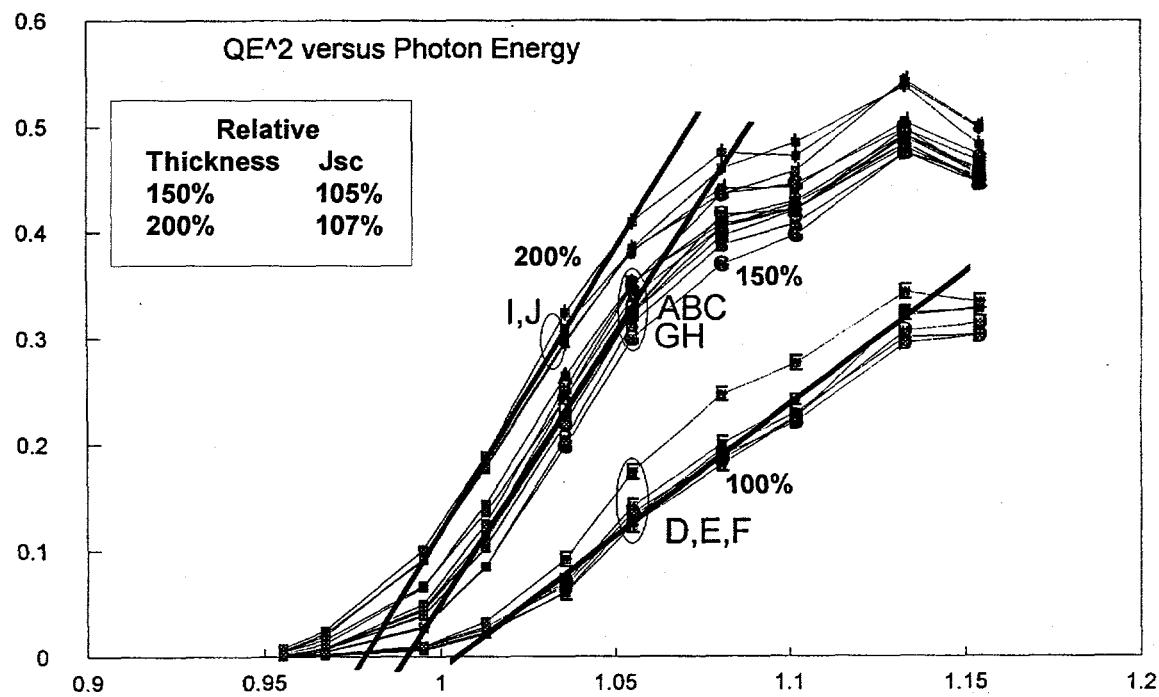


Figure 45. The square of the quantum efficiency for data near the bandgap for the groups of precursor deposition conditions of Figure 44. Linear extrapolation to zero quantum efficiency is used as an indicator of relative band gap.

differences in sulfur content [9]. Counter-varying current and voltage trends observed for variations in the precursors thicknesses may also be related to sulfur content. Reverse saturation currents, diode quality factors and fill factors are not as simply related to thickness and sulfur content as are open circuit voltage and short circuit current. These parameters vary with precursor deposition conditions including power, thickness and other deposition details.

SIMS depth profiles from NREL on representative samples indicate that:

The sulfur concentration profile is sharper at the front of the absorber for thicker absorber layers.

The sulfur concentration in the bulk is lower for thicker absorber layers.

The gallium profiles from back to front of the absorbers are similar for all groups of precursors independent of deposition conditions including overall thickness. That is, the gallium concentration at the front of a device is lower for thicker absorber layers.

Profile differences are observed for Na and other elements. However, trends in the profiles are not as distinct.

One explanation for the increase in short circuit current with increasing thickness of the absorber layer is that long wavelength photons are more likely to be absorbed for thicker films. However, this explanation does not explain the observed decrease in open circuit voltage with increasing thickness. Differences in the sulfur and gallium profiles are alternate explanations for the differences in the short circuit and open circuit voltage. Lower sulfur concentrations and therefore lower bandgaps in the bulk of the absorber for thicker absorber layers equally well explain increasing short circuit current with increasing thickness. Nonlinear interactions between gallium and sulfur have been observed that affect carrier concentration, depletion width and open circuit voltage [49]. Low concentrations of Ga in S-based CIGSS compounds leads to increased open circuit voltage. Therefore, since the gallium concentration at the front of a device is lower for thicker absorber layers, the SIMS profiles also explain decreasing open circuit voltage with increasing thickness. Modeling results will be discussed that are consistent with the SIMS data.

Device Modeling

Background - Graded Absorber Structures

I-III-VI₂ multinary compounds based on CuInSe₂ and one or more additional elements from groups I (Ag), III (Al, Ga) and VI (S, Te) have demonstrated considerable potential in thin film solar cells. Both the bandgap and lattice constant of I-III-VI₂ multinary compounds can be adjusted by changing the relative amounts of constituent elements [27]. Their use is proposed in shifted bandgap device structures, graded bandgap device structures, and to form back surface field regions [10, 17, 18, 27, 29, 30, 50]. Composition of multinary compounds can also affect the mechanical properties of constituent thin films, giving rise in certain instances to improved adhesion [28, 51, 52].

Development efforts at SSI have included homogeneous and graded absorber layers. Initial motivations for exploring potential I-III-VI₂ absorbers with bandgaps higher than CIS were to improve cell efficiency and to obtain attributes that are beneficial for the integration of the cells into modules. For uniform bandgap absorbers, the theoretical maximum efficiency is a function of bandgap through the counter-variation of open circuit voltage and short circuit current. The bandgap of CIS is about 1.0 eV, which is below the

theoretically optimal bandgap of about 1.4 eV [25]. The higher bandgaps of I-III-VI₂ multinary absorbers place them closer to the theoretical maximum.

As with theoretical efficiency, the counter-variation with change in bandgap of open circuit voltage and short circuit current is an important consideration for module integration. Higher bandgap absorbers generate higher voltages and lower photocurrents than do CIS absorbers in devices with comparable efficiencies. Higher voltage allows more latitude in the tradeoff between the number of cells in a module and the power losses in the transparent conducting oxide (TCO). Decreasing the current density decreases the resistive power loss in the TCO. Wider cells with fewer interconnects lead to higher active area by decreasing the total interconnect area. An equally important benefit of higher voltage cells in modules is that, for the same module voltage, the temperature dependence of module voltage is lower for fewer higher voltage cells. Higher bandgap absorbers also are less effected by plasma absorption in the front TCO, which becomes significant at wavelengths longer than about 900 nm.

Solar cells based on homogeneous and graded I-III-VI₂ absorber layers have been fabricated at SSI with active area efficiencies ranging from 11% to 16% [9]. Equally important achievements have been made in the ability to select I-III-VI₂ absorber layer structures for improved manufacturability. As mentioned, Ga has been incorporated in I-III-VI₂ absorber layers to improve adhesion. Uniformity, yield, and process variability are also dependent on the I-III-VI₂ absorber structure. Within the limits of the processing explored at SSI, better uniformity and yield with less process variability has been demonstrated for graded than for uniform composition high gap I-III-VI₂ absorbers. Optical beam induced current (OBIC) scans of devices with homogeneous high gap I-III-VI₂ absorber structures indicate that the output is an average of low and high output areas with spatial variations on the order of a half-millimeter and larger.

Sources of spatial OBIC signal variations for the high sulfur content, high bandgap I-III-VI₂ absorbers have been studied by microscopic analysis and by exploration of process latitude in the two-stage process. Scanning electron micrograph (SEM) and energy dispersive spectroscopy (EDS) studies of absorber surfaces indicate structural and compositional variations on a microscopic scale. Large grains are seen separated by a matrix of fine grains with a periodicity of about 5 μm . This microscopic variation of structure is observed over large areas and seems to be inherent for particular combinations of precursors, reactants and reaction processes. EDS analysis indicates that the observations are related to sulfur- and indium-rich structures. For high sulfur concentrations, these sulfur- and indium-rich features are consistent with the coexistence of the InS and CuInS₂ phases [53]. Sources of spatial OBIC signal variations for the high sulfur content, high bandgap I-III-VI₂ absorbers are apparently related to microstructure. However, for the graded absorber approach, SEM and EDS analysis indicate spatially uniform absorbers.

Measured and Modeled Graded Absorbers

Spectral response. Spectral response data for devices with graded absorbers can be explained by sulfur and/or Ga concentration versus depth into the absorber data as determined by Auger or SIMS depth profiling (Figure 43). Spectral response for wavelengths shorter than about 0.8 μm is similar for Cu(In,Ga)Se₂ and graded Cu(In,Ga)(SeS)₂ devices (Figure 15). For wavelengths longer than about 0.8 μm the response is lower for graded Cu(In,Ga)(SeS)₂ devices. As observed, lowered spectral response for the longer wavelengths should be expected for an absorber with this type of graded bandgap. A larger fraction of the illumination penetrates through the depletion region to the base region where generated carriers are less efficiently collected [30]. Collection at long wavelengths may also be reduced by lower absorption in the higher bandgap sulfur and gallium-rich layer at the back of the device structures.

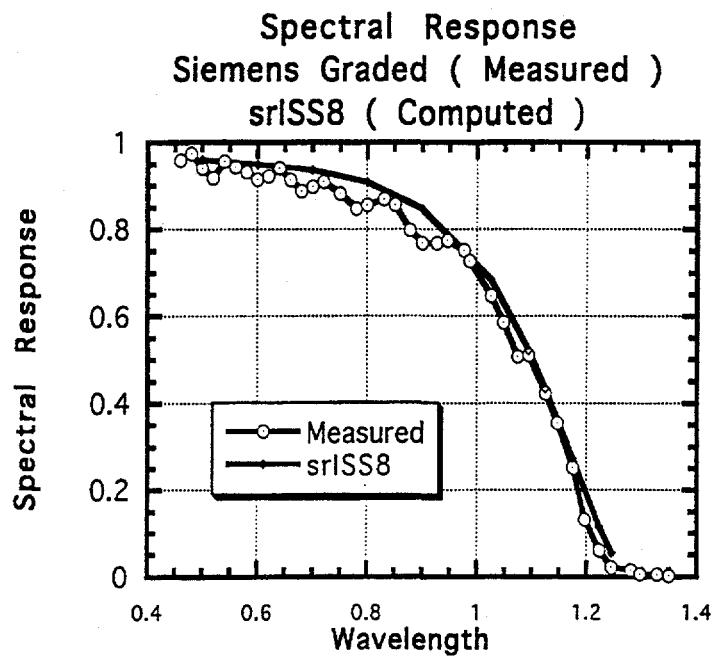
Graded absorber device performance has been compared with device performance modeling at Purdue University using "A Device Emulation Program and Tool" (ADEPT) software [54]. Reasonable agreement between actual and modeled data has been obtained with a simple model. For example, reasonable agreement between measured and modeled spectral response is demonstrated by Figure 46. The assumed energy band diagram is shown in Figure 47. The model assumptions are that the sulfur-rich high bandgap $\text{Cu}(\text{In},\text{Ga})(\text{SeS})_2$ at the front of the absorber structure introduces an offset in the valence band with minimal offset in the conduction band [9, 30]. Assuming that the valence band offset is dominant, grading of the sulfur concentration should minimize the effect of the relatively small conduction band offset [55]. A relatively small bandgap gradient is assumed at the back of the device since the actual bandgap profile is unknown.

Current versus voltage characteristics. Current versus voltage characteristics for I-III-VI₂ devices are determined by space charge recombination [20, 21]. Modeled positional dependence of recombination rate and fraction of total recombination is shown in Figure 48 for a graded absorber device biased at near the maximum power point. Measured and modeled current versus voltage characteristics are consistent with lower space charge recombination current for graded absorber devices. Recombination in the space charge region is decreased by lowered majority carrier concentration due to the offset in the valence band. The position and/or slope of quasi-Fermi levels are also altered by the bandgap grading which affects the probability of recombination and the volume with high probability of recombination.

Theoretical Efficiency. For uniform bandgap absorbers, the theoretical maximum efficiency is a function of bandgap through the counter-variation of open circuit voltage and short circuit current. The bandgap of CIS is about 1.0 eV, which is below the theoretically optimal bandgap of about 1.4 eV [25]. The higher bandgaps of multinary I-III-VI₂ absorbers places them closer to the theoretical maximum. The commonly accepted value for optimal bandgap of about 1.4 eV is based on the optimistic assumption that recombination is limited only by Auger recombination. However, this is not the case for realistic assumptions regarding known materials that are appropriate for commercial photovoltaic devices. The optimal bandgap for devices with realistic assumptions regarding recombination mechanisms and therefore larger reverse currents will be lower than the optimal bandgap based on the assumption of Auger limited recombination. The functional form of the efficiency versus bandgap curve is altered. The efficiency versus bandgap curve is not simply shifted to lower efficiencies with the peak at the same wavelength.

Uniform bandgap absorbers are typically assumed in theoretical efficiency calculations. Efforts to decrease recombination current, from realistic recombination mechanisms, by using alternative structures such as graded absorbers will also change the character of the counter-variation in open circuit voltage and short circuit current. Alternative structures effectively add additional degrees of freedom to the theoretical efficiency versus bandgap calculation. Again, the efficiency versus bandgap curve is not simply shifted to lower efficiencies with the peak at the same wavelength. For alternative structures the character of this curve is altered and the peak efficiency is shifted.

Combined considerations and model results. The impact of change in graded absorber device structures has been modeled at Purdue University using ADEPT software. Device parameters as a function of front sulfur rich layer thickness and for changes in the assumed bandgap of the multinary bulk semiconductor are plotted in Figures 49 a-d. Counter-variation of open circuit voltage and short circuit current are predicted for increases in both front layer thickness and bulk semiconductor bandgap. The thickness of sulfur rich layer is assumed to be about 0.12 μm for the base case. Increasing the thickness of this layer increases voltage and efficiency; however, fill factor is lower for the thickest case modeled than for the base case. Small increases in the base semiconductor bandgap dramatically improve efficiency.



Results from R. Schwartz, J. Grey, Purdue University

Figure 46. Agreement between measured and modeled spectral response.

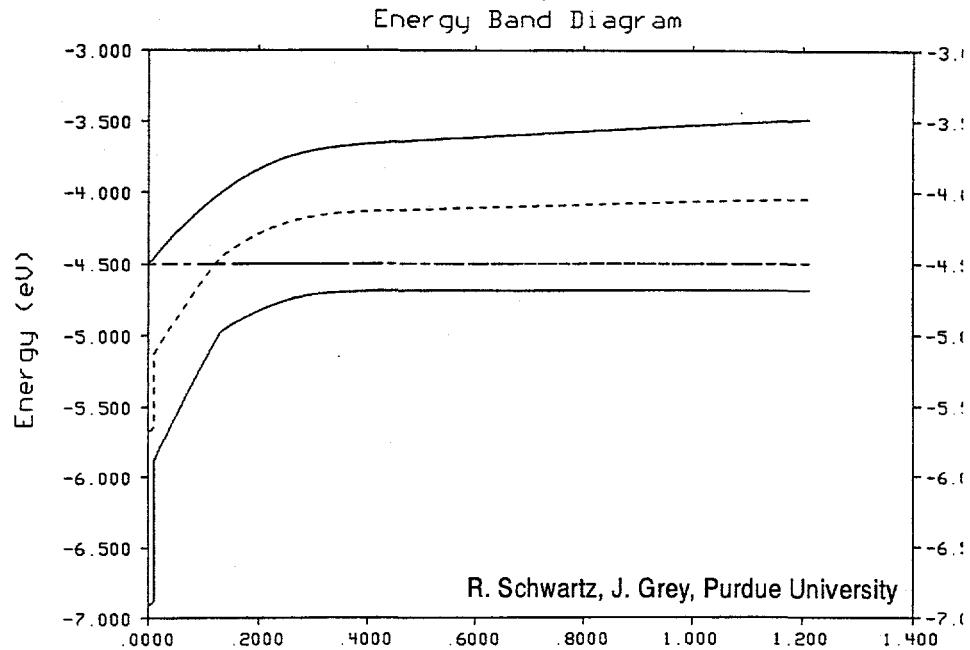


Figure 47. Assumed energy band diagram for computer modeling of device performance.

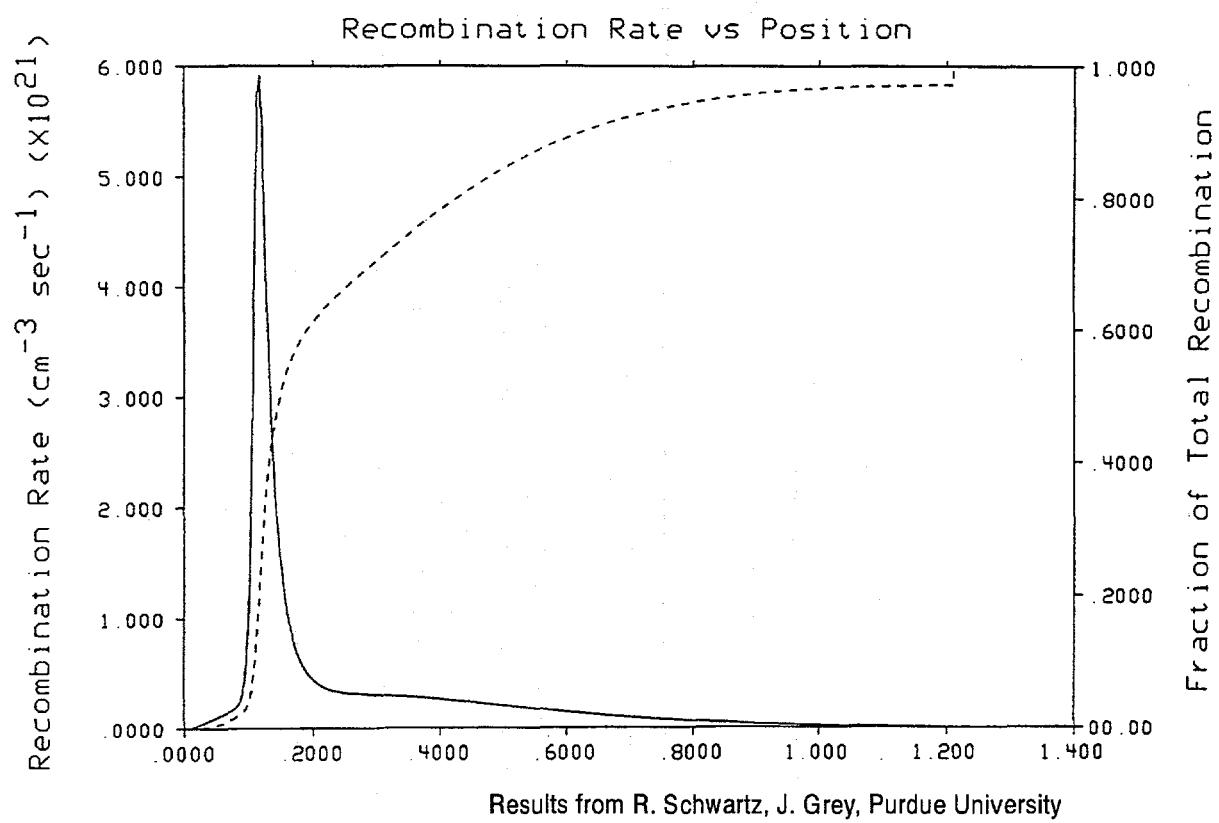


Figure 48. Modeled positional dependence of recombination rate and fraction of total recombination.

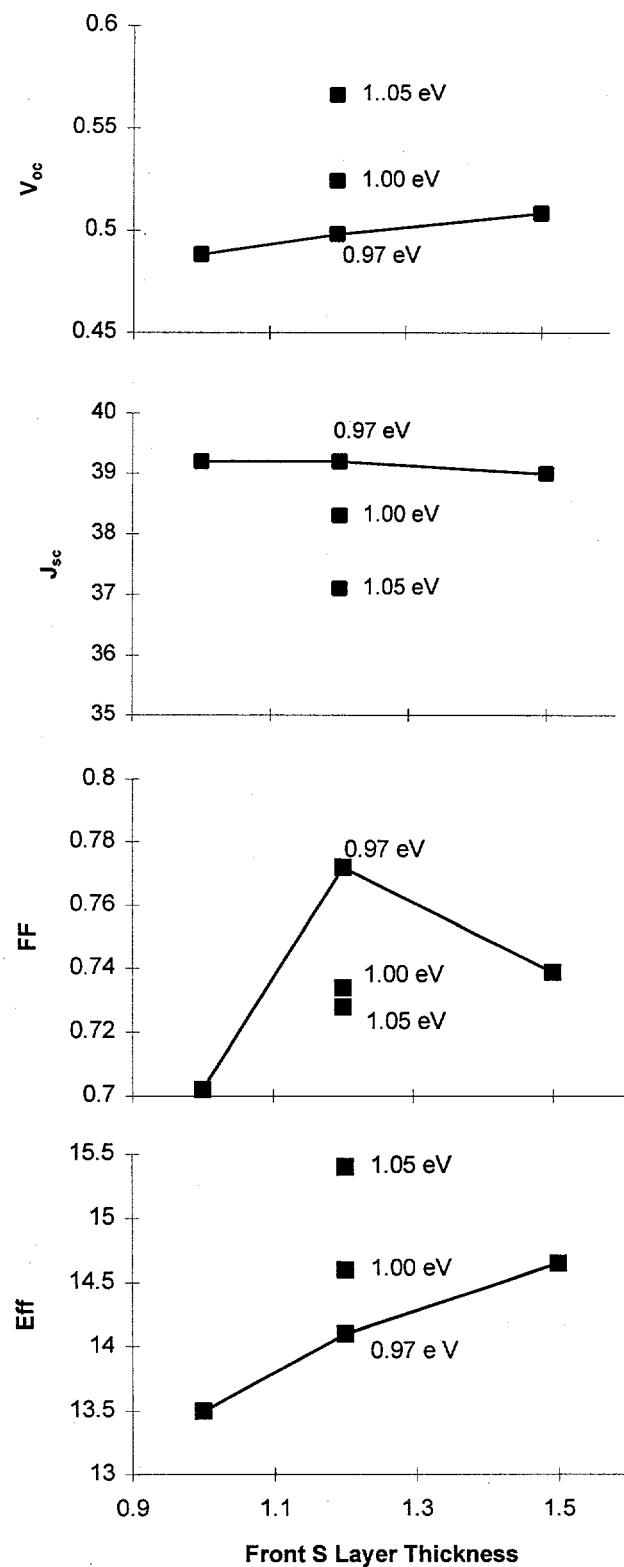


Figure 49. Modeled device parameters as a function of front sulfur rich layer thickness and for changes in the assumed bandgap of the multinary bulk semiconductor.

Increasing current and decreasing voltage with increasing absorber thickness was discussed in the Precursor Variations section. One explanation for the increase in short circuit current with increasing thickness of the absorber layer is that long wavelength photons are more likely to be absorbed for thicker films. However, this explanation does not explain the decrease in open circuit voltage with increasing thickness. Differences in the sulfur and gallium profiles are alternate explanations for the differences in the short circuit and may explain the counter-varying open circuit voltage.

The model results are qualitatively in agreement with the observed current, voltage, spectral response and SIMS characteristics discussed for experiments such as absorber thickness variations. Carrier concentrations and therefore built-in voltage has been experimentally shown to be dependent on gallium and sulfur concentration and interplay between the gallium and sulfur concentration [50]. For absorber thickness variations, if it is assumed that the bandgap and voltage are dependent on these concentrations and their interplay, model predictions are consistent with the SIMS elemental profile results from NREL. Comparing observed and modeled results, the observed lower sulfur (and/or Ga) concentrations and therefore lower bandgaps in the bulk of the absorber for thicker absorbers, or the observed thinner front S-rich region for thicker absorber layers, explain the decrease in open circuit voltage. The increase in short circuit current with increasing thickness is consistent with a longer absorption length or the lower bandgap in the bulk. A model based exclusively on increased absorption length with increasing thickness is consistent with the observed increase in current but not the observed decrease in voltage.

Circuit Design

As discussed, Phase 3 substrate and base electrode preparation techniques combined with modification of the reaction process allowed return to the more robust "classic patterning" of mini-modules. Mini-module performance for classic and post absorber interconnect approaches will be discussed in this section. Short circuit current improvements due to prismatic covers will also be discussed.

Prismatic Covers

Several methods have been explored for diverting light to an active region of a module that would normally strike the inactive region of an interconnect. Investigations have been performed and performance improvements have been realized for light diverting approaches based on reflection and refraction, ie. prismatic covers.

An example of a prismatic cover is shown in Figure 50. Light that would normally strike an interconnect is refracted to an active region of the mini-module due to the groove in the cover sheet. Table 10 shows cell parameter improvements for prismatic covers made of silicone and quartz. Index matching fluids were used to simulate lamination or other encapsulation methods for the case of a quartz prismatic cover. Degradation of the short circuit current is observed for the quartz prismatic cover without index matching fluid. Improvements in I_{sc} of up to 3.5% are observed for a quartz prismatic cover with index matching fluid.

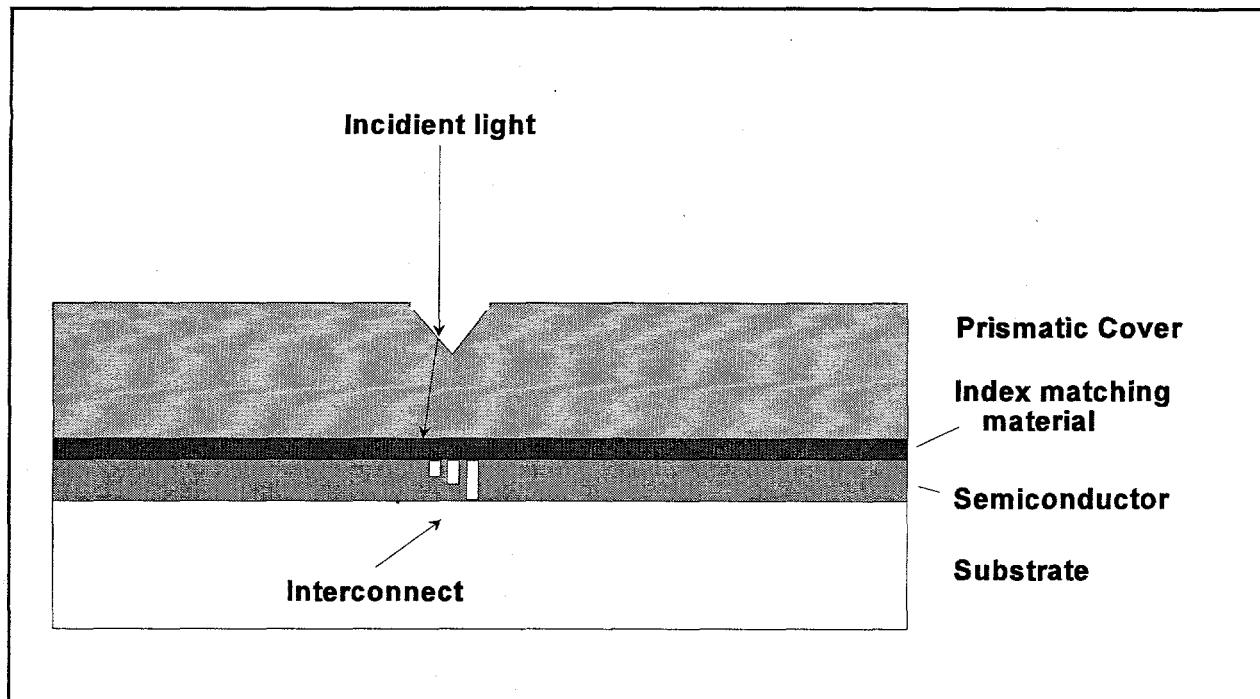


Figure 50. Prismatic cover concepts.

Table 10. Prismatic Covers Improve Module Performance.

Configuration	Voc	FF	% change in Isc
Pre-Test	7.25	.645	-----
Silicone, no fluid	7.25	.644	1.1 increase
Quartz, no fluid	7.22	.649	8.0 decrease
Quartz, with fluid	7.26	.642	3.5 increase

Mini-module Performance

Figure 25 in the Phase 2 section illustrates "classic patterning" (described as standard patterning in Figure 25) and post-absorber interconnect formations methods. Typical distributions and champion results for post-absorber and classic patterning are shown in Figures 51 and 52. Mini-module champion efficiency with the post absorber interconnect process is 11.7%. Mini-module champion efficiency with the "classic patterning" interconnect process and a prismatic cover is 12.7% (NREL verified). The distribution for the "classic patterning" approach is higher in efficiency and narrower than for the post absorber interconnect process (both distributions are for mini-modules without prismatic covers).

Based on these studies, standard mini-module processing returned to the "classic patterning" approach combined with the improved substrate and base electrode preparation techniques and modification of the reaction process. Distributions for additional groups of mini-modules with this combination of processes are discussed in the following section entitled "Process Development and Scaling"

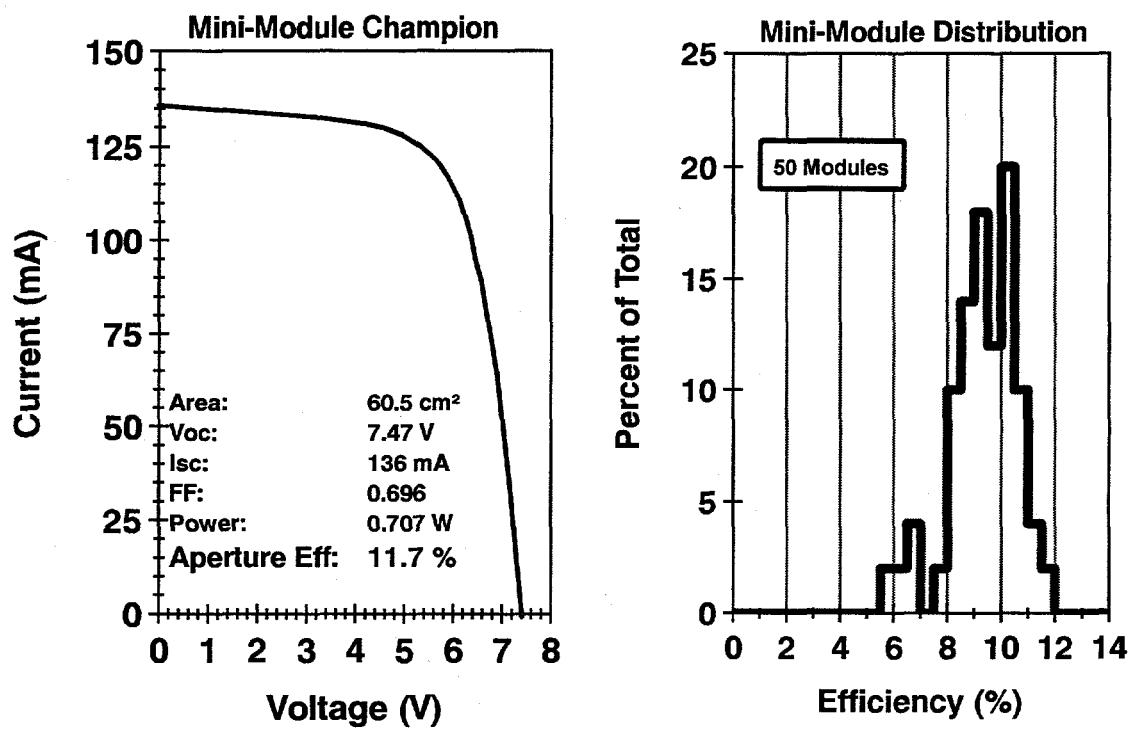


Figure 51. Champion and distributions for post-absorber patterning.

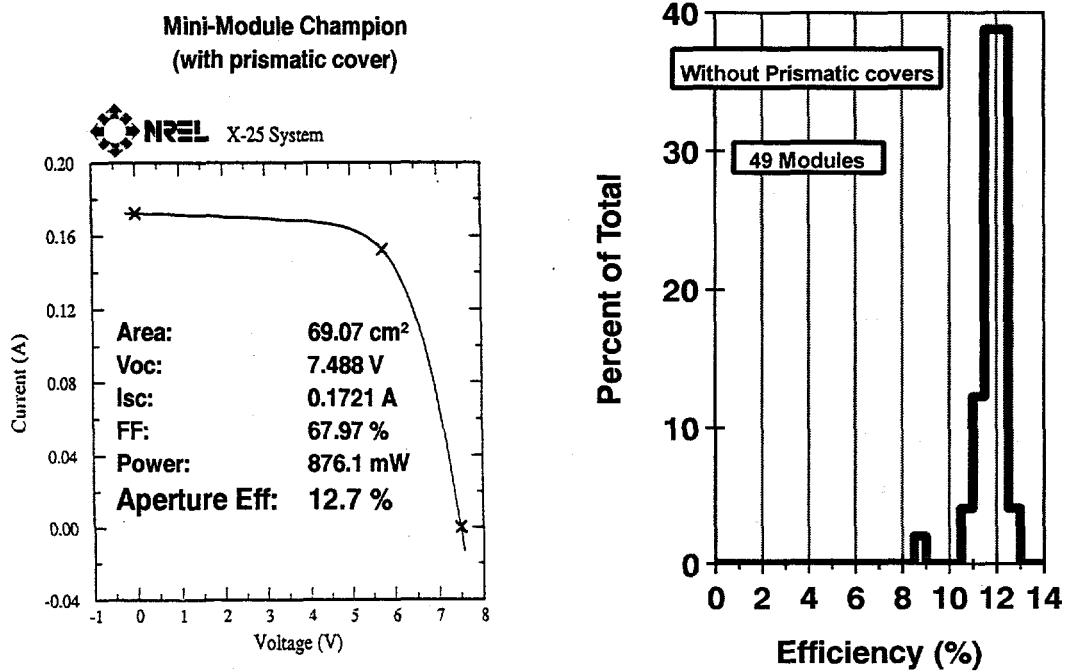


Figure 52. Champion and distributions for classic patterning.

Environmental Testing and Transient Effects

Accelerated and Outdoor Testing at NREL

Long term outdoor stability of CIS and CIS-based absorbers has been demonstrated by testing at NREL. Figure 53 traces performance for large area modules since 1988 and for new generations of modules periodically added to the study. Excellent stability is demonstrated for six years of outdoor exposure. Stability of the approximately 1 kW Siemens CIS array installed and tested at NREL has also been demonstrated for an exposure of approximately one year (Figure 54).

Preliminary NREL testing has recently demonstrated stability through standard 200 thermal cycle testing Table 11 [56]. These tests included measurements before and after the applied environmental stress. Ground continuity, dry and wet Hi-pot and wet insulation resistance tests were passed in the NREL testing. However, as discussed in the Phase 2 section, past measurements at SSI have shown mixed results; both stability and significant losses through accelerated environmental testing or outdoor testing have been observed. Inconsistent results such as these are an indication of a process that is not in control as defined by the statistical process control methodology. Obtaining control and an understanding of this issue was emphasized in Phase 3 and addressed using mini-modules as the test bed.

Table 11. Preliminary Module Qualification Testing.

Test	Isc (A)	Voc (V)	FF	Pmax (W)
Baseline	2.28	22.39	58	29.57
Post initial*	2.35	22.43	57	30.19
200 Thermal Cycles	2.34	22.04	56	28.71

* After ground continuity, dry and wet Hi-pot and wet insulation resistance tests

Lamination and Stability

As discussed, CIS based modules have demonstrated stability in field conditions. However, transient changes in module performance are often observed for the thermal exposures encountered during lamination or accelerated environmental testing. Any transient effects such as these are an issue when considering predictability as it relates to a production process. These transient effects must also be considered when performing or defining procedures for accelerated environmental testing. Experience at SSI indicates that transient effects must be considered to properly interpret test results that might be used to project performance in the field since accelerated testing may activate mechanisms that are not dominant in service.

Transient effects induced by lamination and accelerated environmental testing, and effects such as sensitivity to light exposure history and sweep rates during current versus voltage testing, are assumed to be related. Characterization, isolation and elimination of thermal and light-induced effects was defined as a major task for Phase 3. Progress in addressing these issues is discussed in this section.

Siemens Solar CIS Modules
Measured with SPIRE 240A at STC

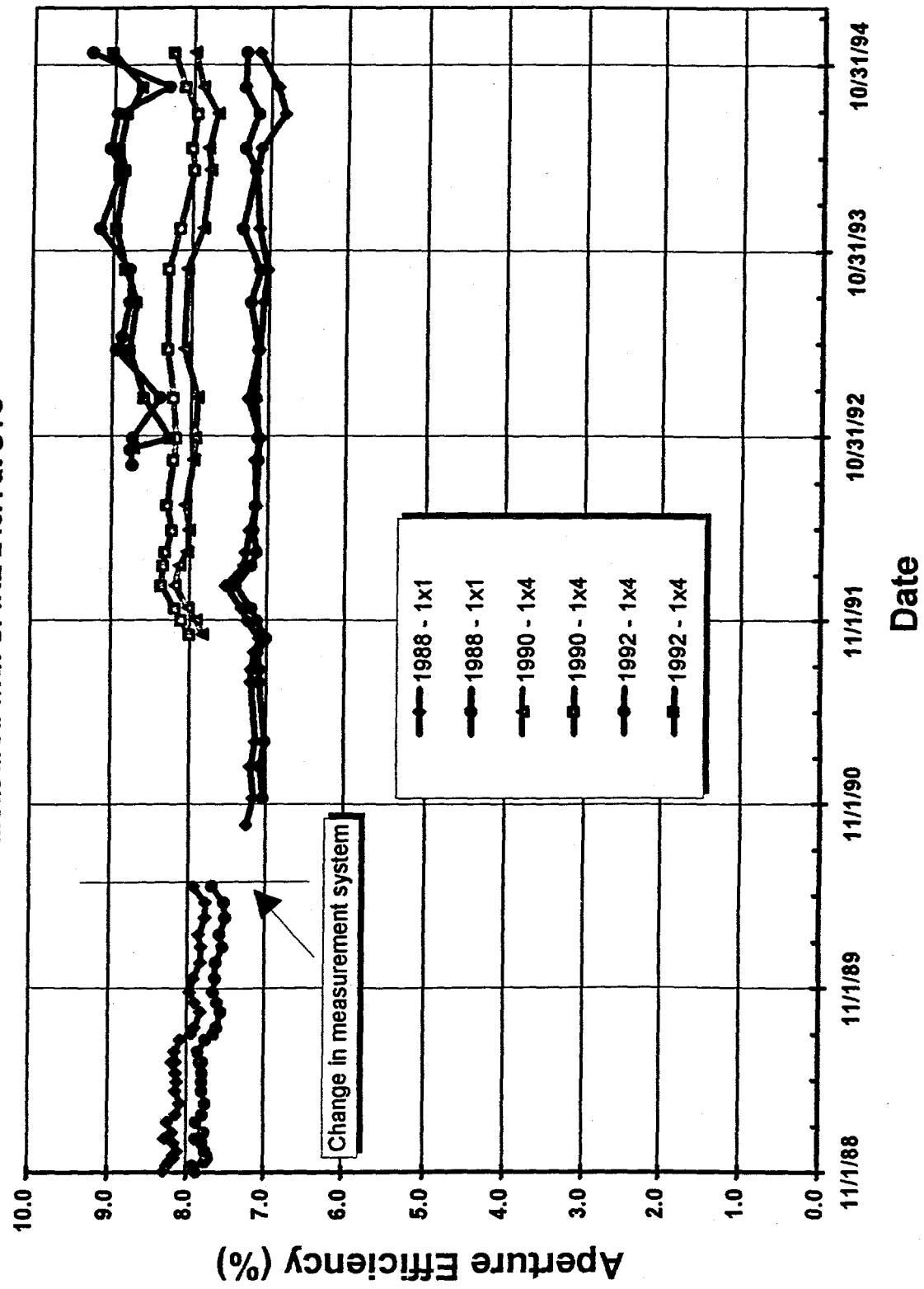
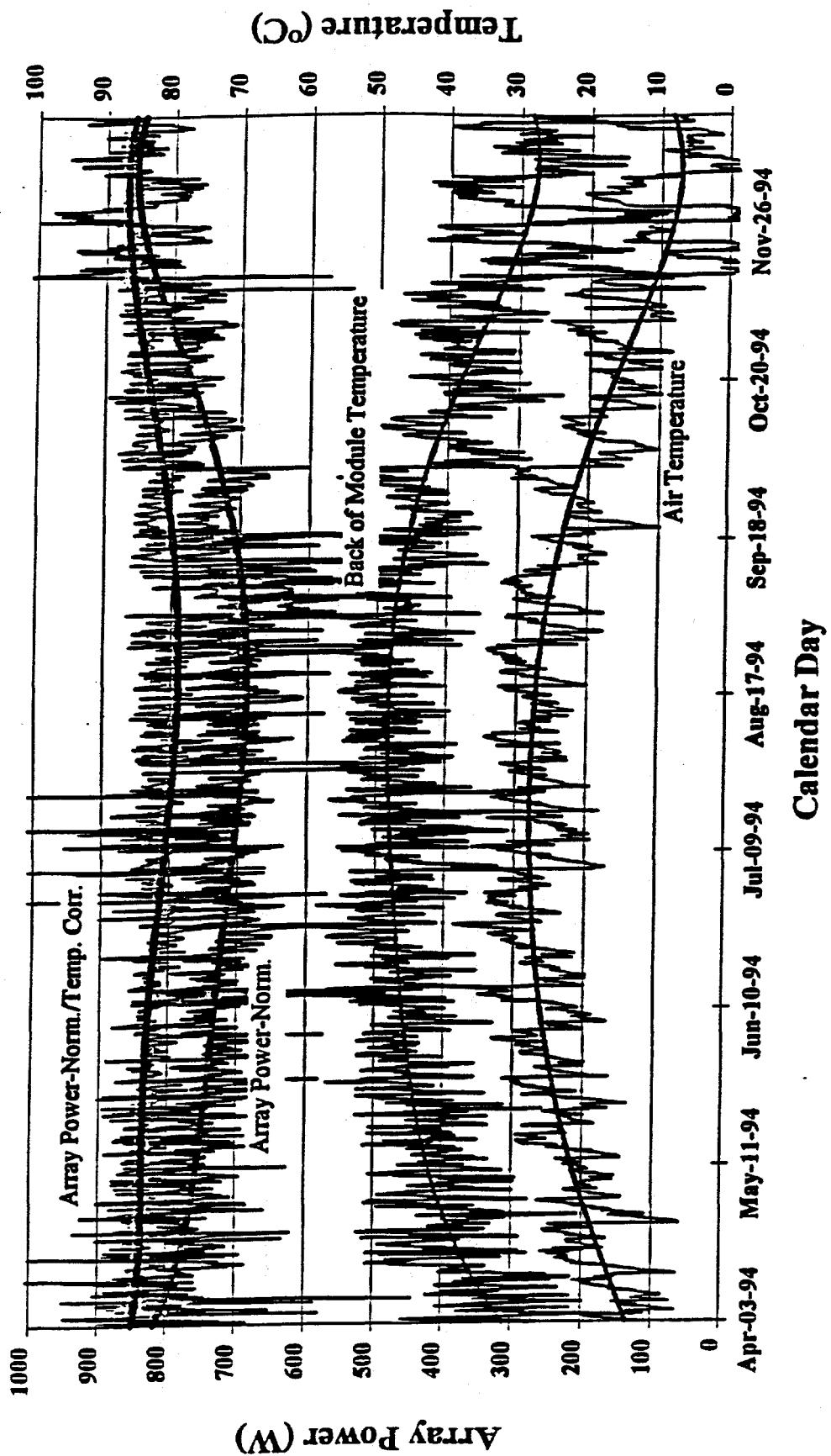


Figure 53

Siemens Solar CIS Corrected Array Power versus Calendar Day



Photovoltaic Module and System
Performance and Engineering Project

National Renewable Energy Laboratory

Figure 55 is a plot of relative efficiency as a function of time after lamination normalized to efficiency measured prior to lamination. This data is from an early Phase 3 process generation. This plot illustrates that efficiency after lamination may range from 65 - 85% of the efficiency prior to lamination. Efficiency changes are dominated by changes in FF. In most cases, efficiency improves with time and approaches or exceeds the initial efficiency. This "recovery" in efficiency is typically accelerated by light exposure [39].

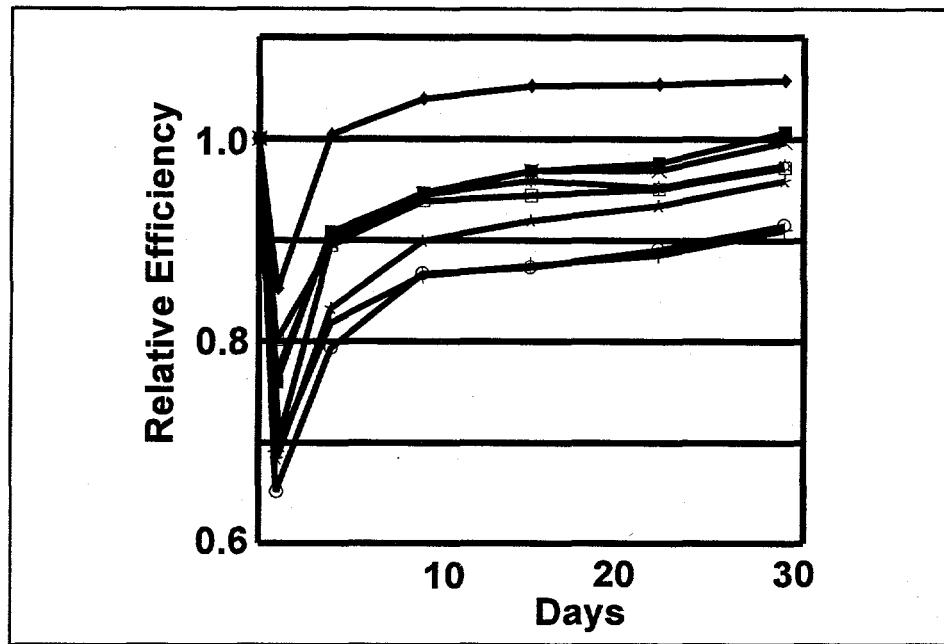


Figure 55. Relative efficiency as a function of time after lamination normalized to efficiency measured prior to lamination.

Lamination procedures with shorter heating times were developed. A group of mini-module laminated with these procedures showed a much smaller transient lamination loss averaging 3 to 4%. However, statistical process control (SPC) techniques indicate the process is not "in control" as indicated by sporadic results outside the control limits in Figure 56 (SPC terms are discussed in more detail in a later section). Since the process is not "in control," low lamination losses may be typical but are not necessarily predictable. Also, changes in the lamination process do not explain all observed changes in performance for this group of mini-modules. The following observations were also made for this group of mini-modules: minimal sensitivity to light soaking, minimal differences in measured FF between continuous illumination and pulsed illumination test conditions, and minimal differences in performance after lamination related to the time between ZnO deposition and lamination. The mechanisms responsible for some of these observable device properties are thought to be related to the mechanisms responsible for temporary lamination losses. However, observation of these properties do not require lamination. Lamination process improvements can not explain observations of differences in related device properties for the group of modules that demonstrated much smaller transient lamination losses; there is not necessarily a causal relationship between the changes in lamination procedures and lower transient losses due to lamination. Another aspect of the overall process may be responsible for some or all of the observations. The lack of a causal relationship between the lamination process and observations before and after lamination may be the reason that the process is not "in control" and not predictable.

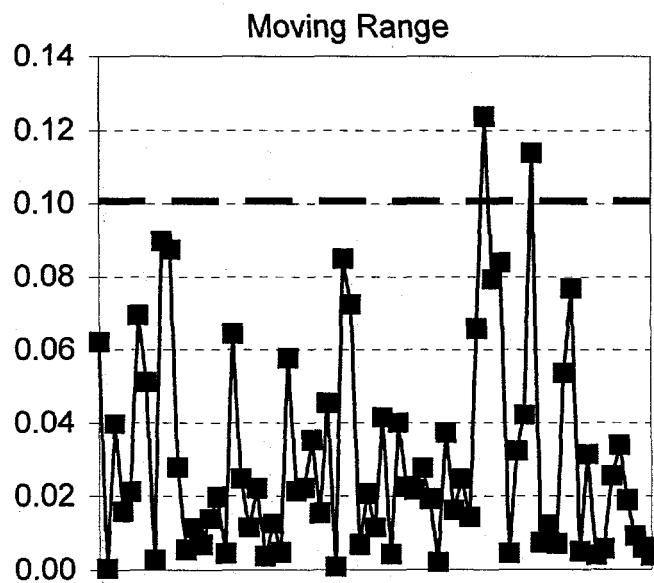
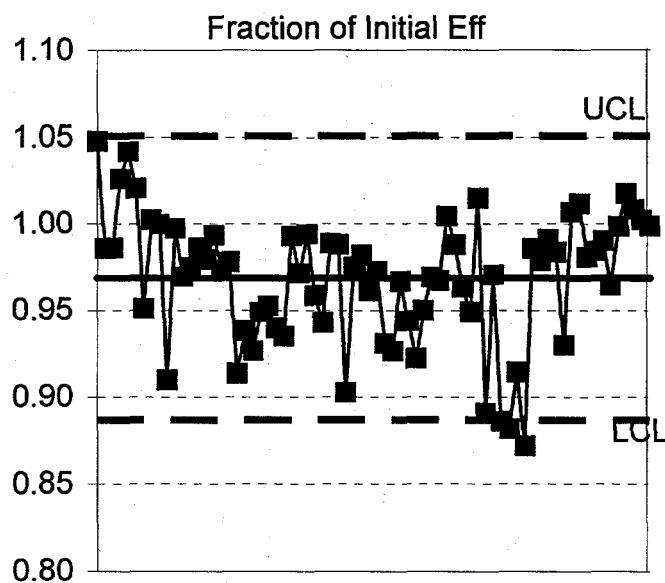


Figure 56. Statistical process control chart for lamination.

Experiments were performed to separate heating affects from other aspects of lamination. An oven was used to subject mini-modules to the same thermal cycle used in lamination. A similar temporary loss and recovery pattern was observed. After recovery, the efficiencies were the same as prior to lamination. Experiment were also performed to test if light exposure while laminating would decrease losses related to lamination. A heat lamp was used to simultaneously supply light and heat to simulate lamination. No significant difference in the recovery pattern was observed. After recovery, the efficiencies were the same as prior to lamination for lamination combined with light exposure.

Light Induced Effects and Outdoor Testing

Demonstrated stability in field conditions and transient changes in module performance related to thermal exposures have been discussed. The related issues of sensitivity to light exposure history and outdoor testing will be discussed in this section. Typically, fill factor and open circuit voltage improve while short circuit current decreases slightly leading to an overall slight improvement in efficiency relative to the efficiency prior to lamination. As seen in Figure 57 for light exposures up to 3 minutes long, short term exposures have been shown to decrease the reverse saturation current which explains the observed improvements in fill factor and open circuit voltage. This mechanism has not been shown to be responsible for observed effects of long term exposures. Changes in short circuit current and the sources of variability in the response to thermal or light exposures are not well understood. However, overall improvements in performance are observed for long term outdoor exposure. Efficiencies for a laminated and "light soaked" module may be higher than for the unlaminated predecessor. Record efficiency of 12.8% was achieved after light soaking for a laminated mini-module (Figure 58).

Characterizing light-induced effects was defined as one of the main tasks for Phase 3. This task was addressed by measuring performance versus outdoor exposure time for large numbers of mini-modules. Figure 59 illustrates typical results. Cell parameters normalized to pre-lamination values are plotted as a function of outdoor exposure time. For this group of mini-modules the average transient change in efficiency due to lamination was relatively low at about 4%. After about 90 days of outdoor exposure the efficiency is about 2% higher than prior to lamination. Fill factor improves by about 5%, short circuit current decreases by about 4% and open circuit voltage improves by about 1%.

Relationships between thermally induced performance degradation and accelerated performance recovery induced by light exposure were explored. Mini-modules which had recovered to approximately pre-lamination performance with outdoor exposure were held at 85°C in the dark and periodically measured. The mini-modules were cooled to room temperature prior to measurement. Each measurement consisted of a current versus voltage measurement immediately after the beginning of exposure in a solar simulator and after two minutes of exposure. After 257 hours of thermal exposure the devices were exposed for 1.5 hours in the solar simulator and periodically measured. Light exposure was continued for a longer term with outdoor exposure. One day of outdoor exposure was assumed to be equivalent to five hours of one sun exposure in the solar simulator. Experimental control devices were kept in the dark at room temperature and only exposed to light with testing which paralleled the testing of experimental devices.

Control devices showed good stability over the 257 hours of testing. Deterioration of the fill factor with thermal exposure and recovery with exposure to light are shown in Figure 60. Only the fill factor changed significantly. The downward trend through 257 hours is due to the thermal exposure. Data points with nearly the same time of measurement are the measurements immediately after the beginning of exposure in a solar simulator and the higher fill factor measurement after two minutes of exposure. Increasing sensitivity

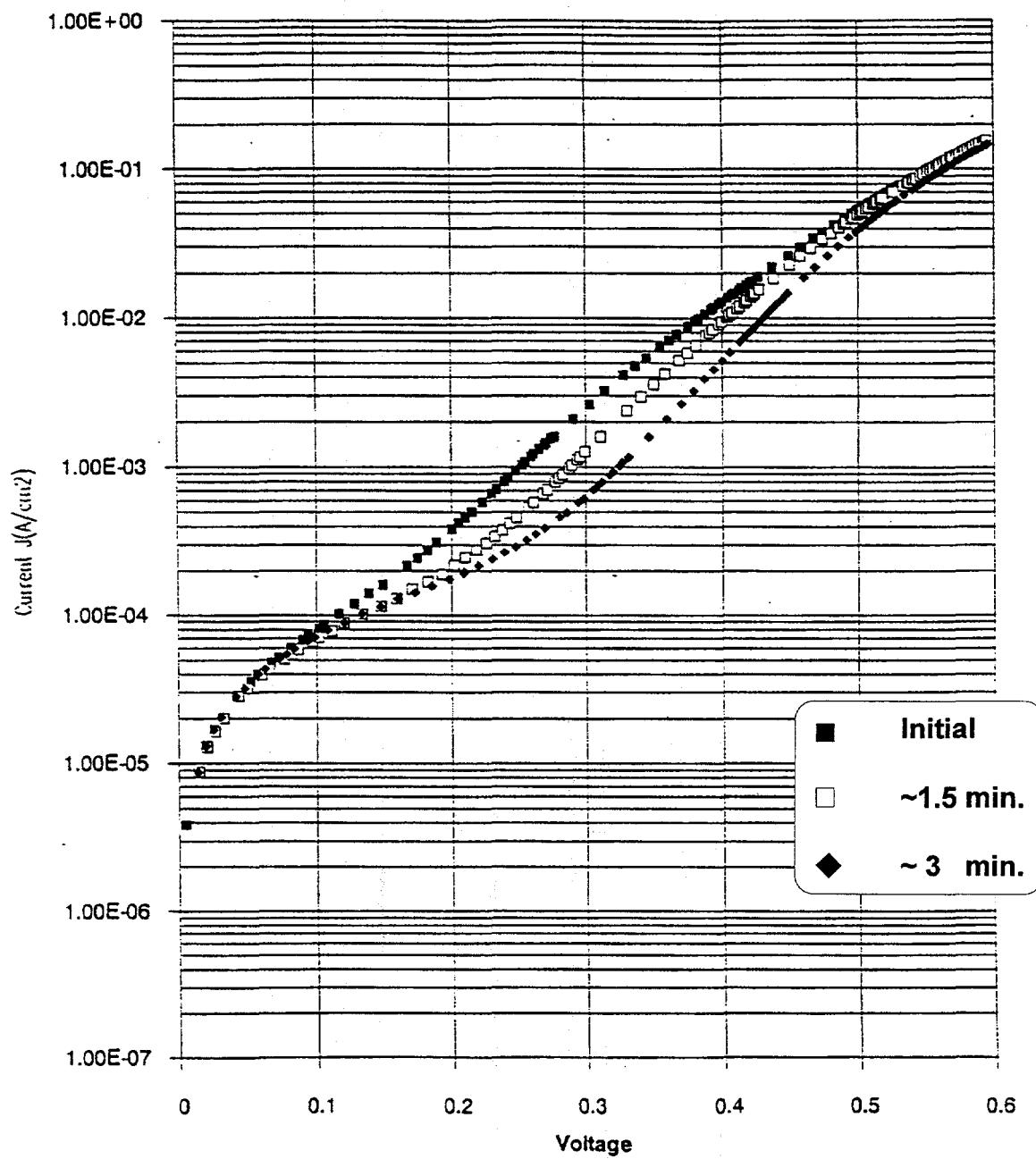
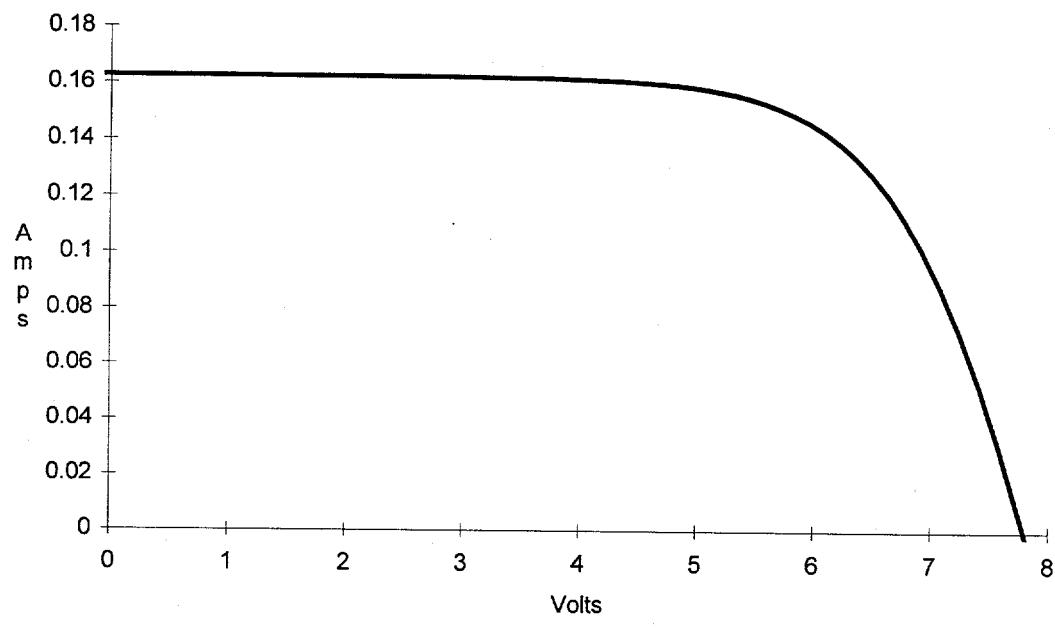


Figure 57. Log current vs. voltage with light soaking.



V _{oc}	7.79	V
I _{sc}	0.163	A
FF	0.691	
Eff	12.8	%
Area	68.9	cm ²

Figure 58. Record efficiency of 12.8% achieved for a laminated mini-module after light soaking.

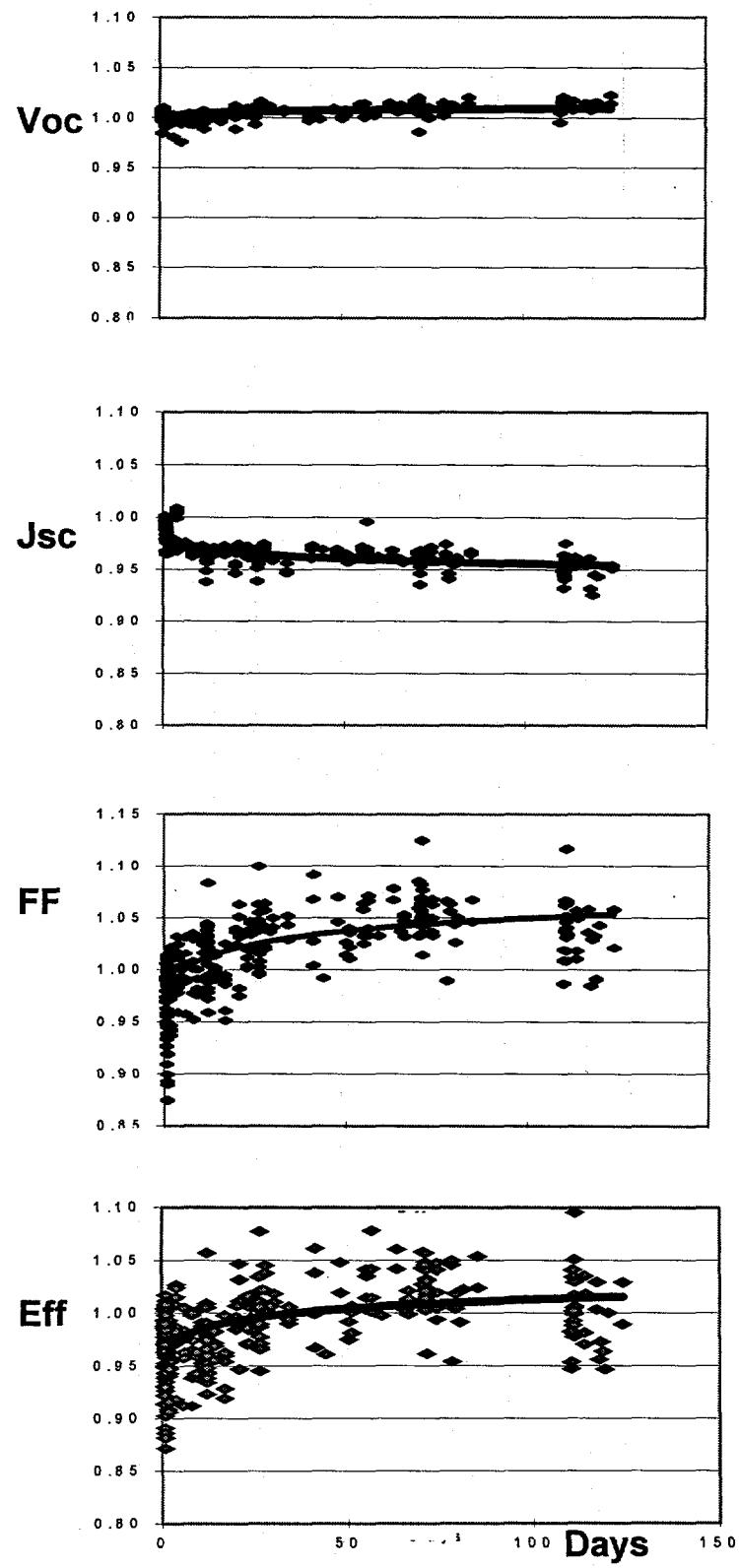


Figure 59. Performance versus outdoor exposure time.

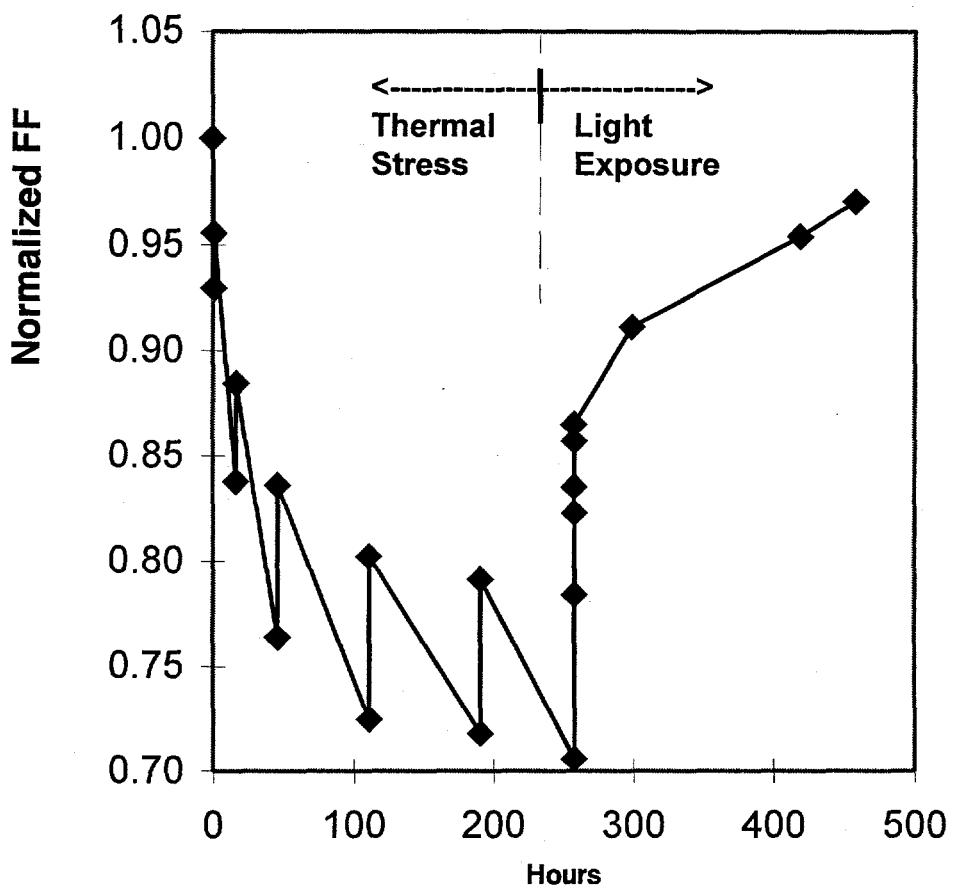


Figure 60. Deterioration of the fill factor with thermal exposure and recovery with exposure to light.

to light exposure is observed with increasing degradation due to thermal exposure which directly links the two mechanisms.

Short term exposure in the solar simulator and longer term outdoor exposure at the end of the thermal degradation schedule demonstrate recovery due to light exposure which varies linearly with the log of time (Figure 61). As seen in these degradation and recovery plots for a poorer device (Figures 60 and 61), time frames as long as 700 or 800 hours (140 to 160 days at about 5 hours/day) may be required for full recovery. Recovery due to light exposure which varies linearly with the log of time is also typical of other thermally induced degradations such as degradation due to lamination.

The degree of degradation can be significantly different for devices from the same process lot and therefore nominally the same processing. Data for four devices from the above experiment, Figure 62, implies two types of typical reaction to thermal degradation and light exposure. One type of device degrades by about 5% with 257 hours of thermal exposure while the other group degrades by about 20%. No correlation with difference in process has been established. Transient effects such as these are an issue when considering predictability for production or predictability of accelerated environmental testing. As with lamination, statistical process control techniques indicate that recovery from thermal degradation or accelerated environmental testing is not "in control" and therefore not predictable.

Edge Seals

A visual examination of laminated mini-modules revealed water ingress and corrosion for initial lamination procedures. Many mini-modules did not have complete seals at the edge of the laminate and a voltage driven corrosion was observed for circuits that were not totally encapsulated. All leads showed considerable weathering which may be reflected in small long term changes in FF. The minimodule circuit was redesigned based on these results. This redesign includes the removal of all films from a 1 cm perimeter region.

Alternative Packaging

Several types of adhesive backed clear polymer films from different vendors were used to laminate mini-modules. In all cases, performance after lamination and/or light exposure was poorer than for a glass front cover sheet. Losses in fill factor were observed for outdoor exposure. The loss in fill factor is thought to be due to an interaction between the adhesives and the CIS devices. Alternative formulations are being pursued with vendors.

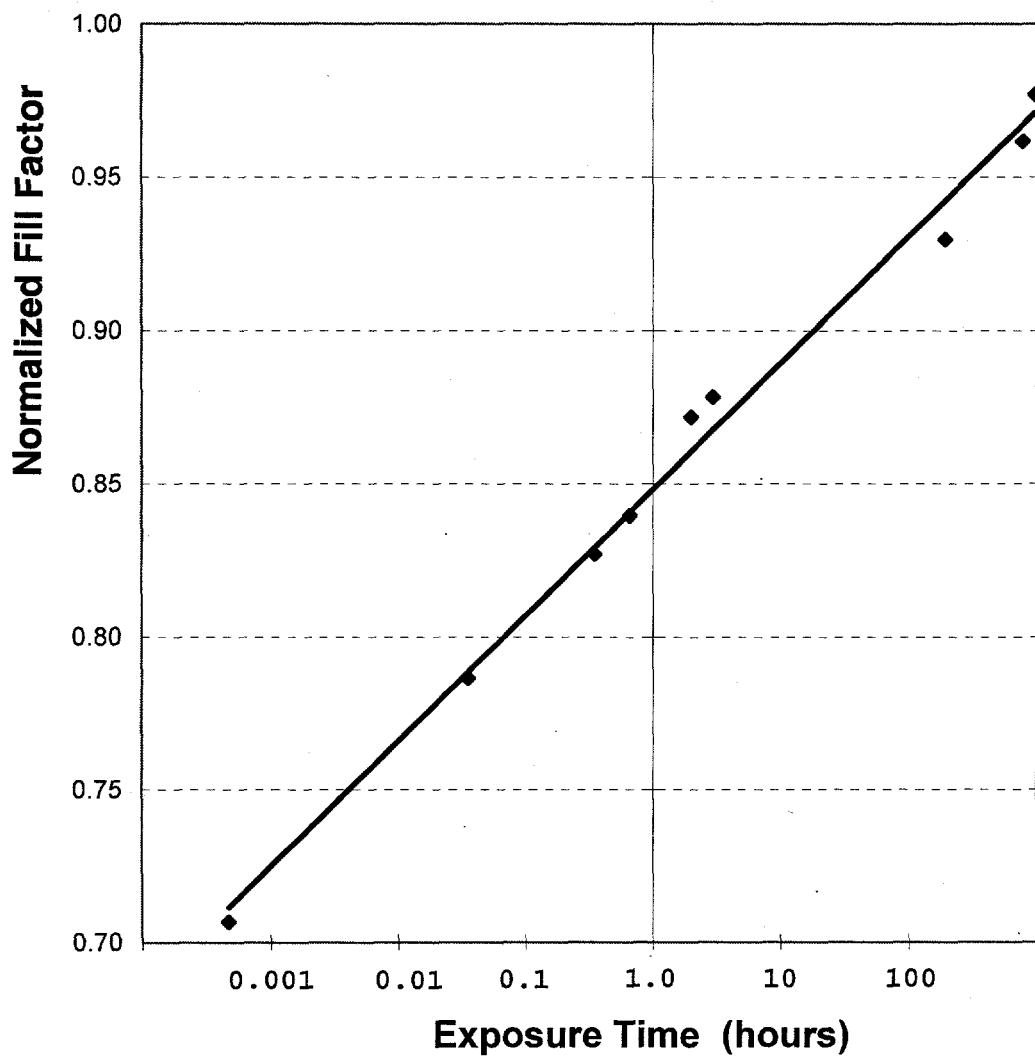


Figure 61. Recovery due to light exposure which varies linearly with the log of time.

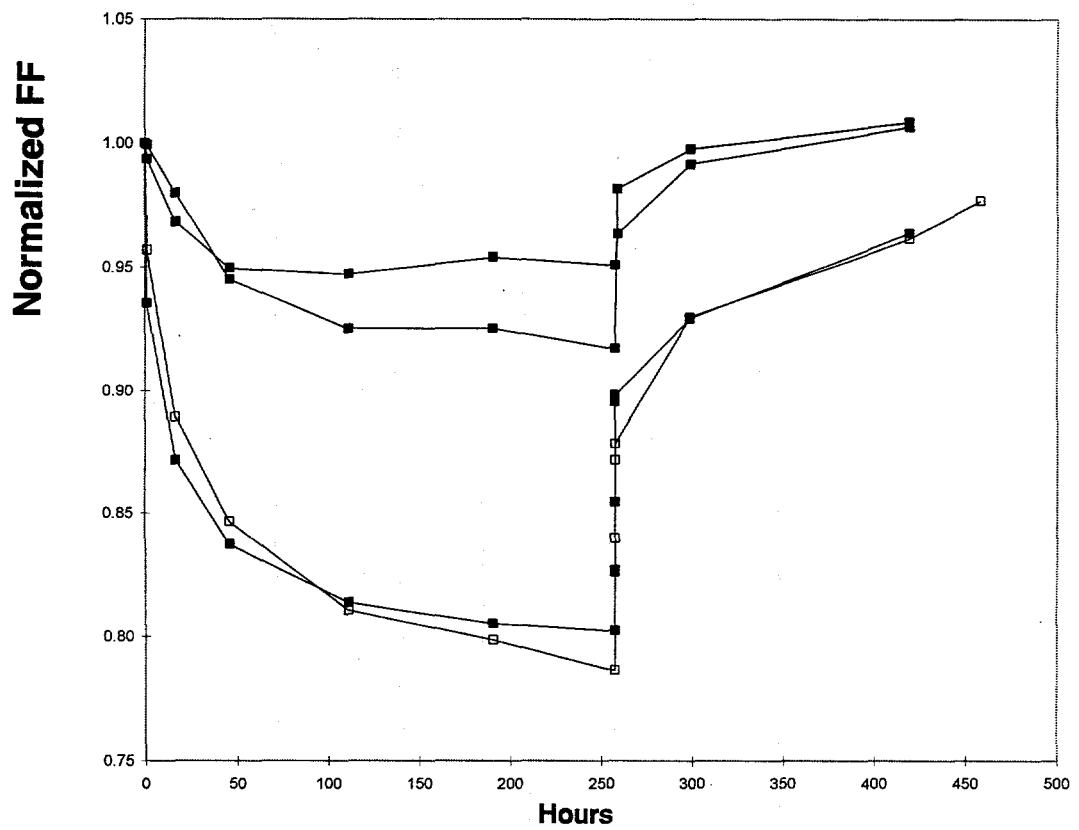


Figure 62. Similar figure as Figure 60 showing that the degree of degradation can be significantly different for devices from the same process lot and therefore nominally the same processing.

Process Development and Scaling

Reduction of Variation

The major challenge to move from development to production is to improve reproducibility rather than to improve performance of champion devices. High efficiency has been demonstrated with CIS based absorbers. Environmental stability of complete modules has been demonstrated. However, process repeatability and predictability has not yet been demonstrated.

Efforts to improve reproducibility have been emphasized during Phase 3 of this contract. Application of Statistical Process Control (SPC) methods has been a key aspect of the reduction of variation efforts. This approach requires a significant change of orientation, with the focus upon continual reduction of variation in processes rather than upon higher efficiency per se. The first goal is the attainment of stable processes, demonstrated by achieving a good level of statistical control, while further improvement of the average performance level is made easier by the creation of this stable basis. Accompanying the statistical tools are improved process definition and documentation aimed toward the ISO9000 standard, improved feedback from individual process steps, and systematic approaches to problem solving and communication of process information. Continued training of all personnel is also a key to successful implementation.

The results or outcome of any process display variation. Statistical Process Control, developed originally at Bell Laboratories, is an empirical discipline rooted in a statistical basis. It provides a means for discerning between the natural random variation inherent in a stable process and variation which indicates that a process has become unstable and that a specific, assignable cause for the instability can be found. Proper selection of the right scheme for sampling the output of a process allows data from any process to be charted versus time and "Control Limits" to be calculated from the process data itself. A continued random trend within these limits is a good indicator that the process is stable over time. Figure 63 illustrates a common SPC method, "Individual-Moving Range", in this case charting efficiency vs. date of fabrication for mini-modules with closely related processing. This data set will be referred to as group 1 and consists of 163 mini-modules. Over 150 mini-modules are typically processed in each group in order to obtain a useful representation of the process. The heavy dark horizontal line at just over 11% efficiency is the process mean for this group, while the dashed horizontal lines at about 12.7% and 9.3% are the upper and lower control limits (UCL and LCL). Some points in Figure 63 fall outside the control limits. Therefore, the process cannot be said to be "in statistical control." Other patterns or trends in the charted data, e.g. long sequences of consecutive points which all fall on one side of the mean also signal a lack of statistical control. Identifying and eliminating the special causes responsible for these observations lead to improved predictability and performance. Predictability, as judged by these SPC criteria, is a critical issue for assessing production capability. Predictability is necessary for confidence in the results of experiments designed to improve a process, confidence in scale-up of a process, and required for in the commitment to move a process from development to production.

The data in Figure 63 is from a timeframe when the flow of parts from CdS dip through the end of processing was designed to determine the relative importance of CdS deposition. This experimental design was based on previous experience. Analysis of variation (ANOVA) of previous data sets ("group 0", Figure 64) indicated that the largest source of variation was due to the block of process steps from CdS dip through final processing. This block includes ZnO deposition and two patterning steps (P2 and P3 in Figure 64). The other blocks of process steps for group 0 were (Figure 64): process steps prior to the reaction process (Mo, P1, Precursors), the reaction process, and testing. CdS deposition could not be separated from the other members of the group due to the grouping of parts in the process stream.

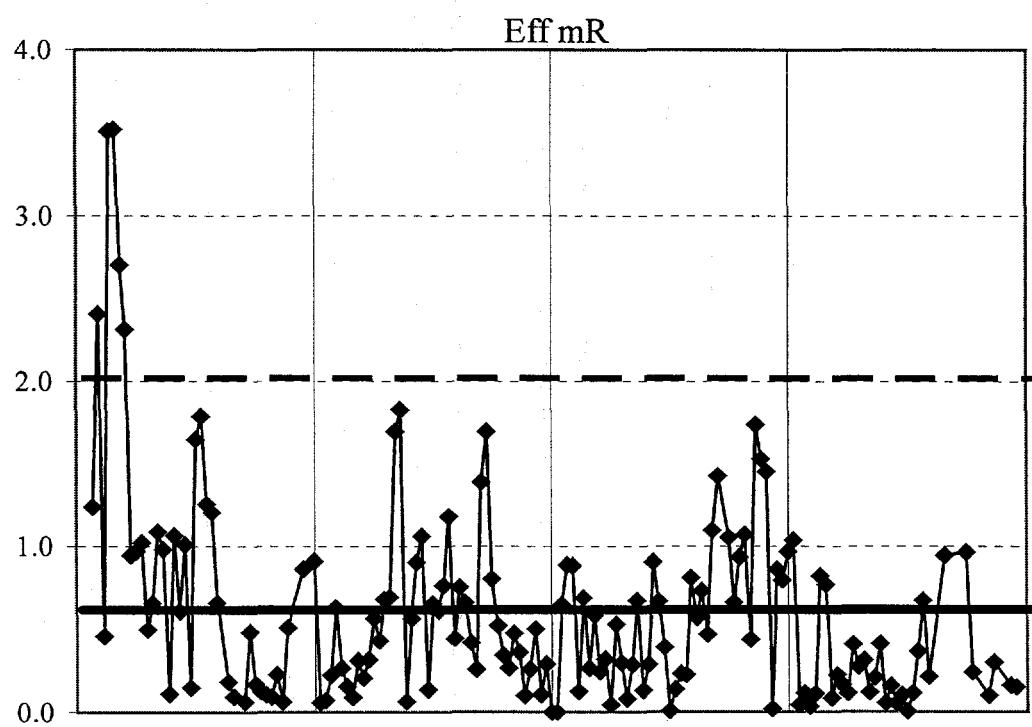
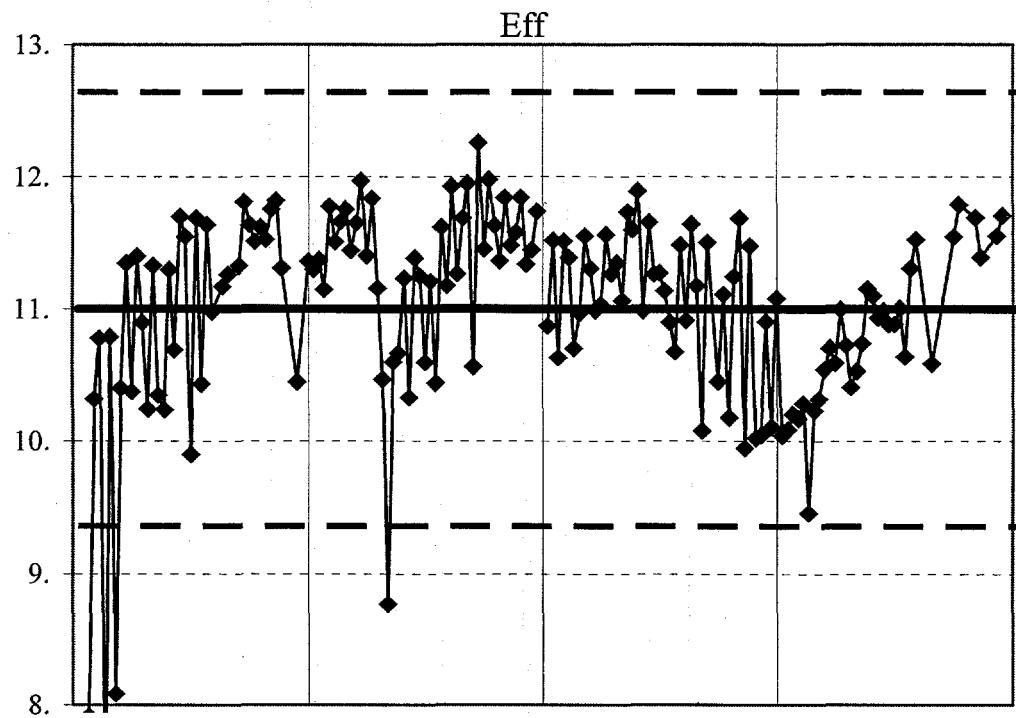


Figure 63. "Individual-Moving Range" chart of efficiency vs. date of fabrication for mini-modules with closely related processing (Group 1).

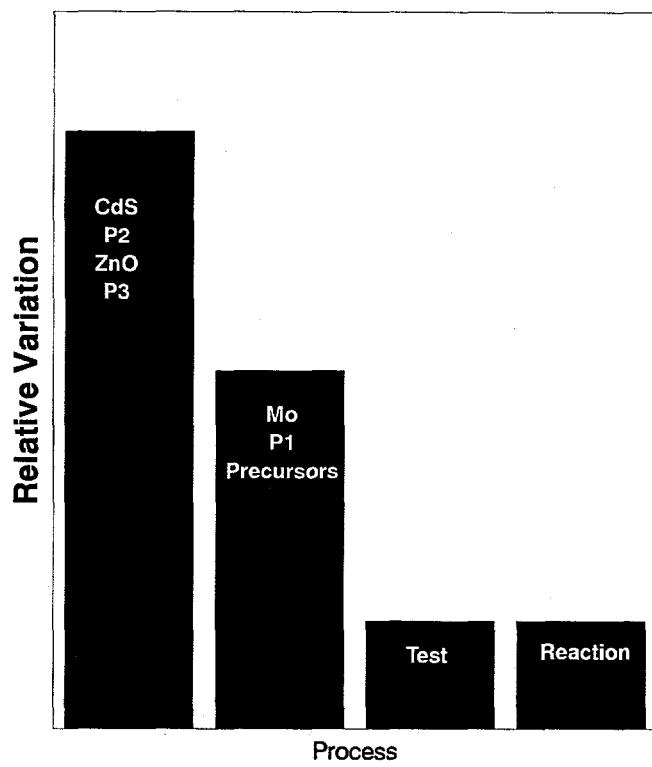


Figure 64 ANOVA for "group 0" indicating that the largest source of variation was due to the block of process steps from CdS dip through final processing.

The flow of parts for the ANOVA plot in Figure 65 was defined to allow separation or deconvolution of the CdS process from other processes by assuring that CdS deposition groups were composed of parts from multiple groups for all other process steps. This is the same data set as in Figure 63; efficiency vs. date of fabrication for mini-modules with closely related processing. This data set will be referred to as group 1 and consists of 163 mini-modules. In addition, several aspects of the CdS deposition process were evaluated. A CdS deposition procedure (CdS Procedure A in Figure 65) was shown to introduce variation and effectively reduce the functional size of the data set for statistical analysis aimed at separating the CdS deposition from other process steps. Effects due to patterning steps were separable while the CdS and ZnO deposition steps remain coupled in Figure 65. The influence of this specific part of the CdS dip procedure was demonstrated as a major source of variation.

A subsequent group of over 100 mini-modules, group 2, was processed with improved CdS procedures. ANOVA indicates 85% reduction in variation (Figure 66). This example illustrates how implementation of SPC techniques have been used successfully to identify the source and then demonstrate reduced process variation. The SPC methodology applies statistical analysis and a framework for systematic experimentation, analysis, and interpretation of data. Process steps with the largest impact on performance variation are addressed before addressing process with less impact on variation. The approach is iterative. Reduction of variation efforts continue with emphasis placed on the next largest source of performance variation.

Large Area Modules

Large area modules have been fabricated with record efficiencies during Phase 3 of this contract. A large area (3860 cm^2) encapsulated module with aperture area efficiency of 10.3% has been demonstrated and verified by NREL (Figure 67). This result is due to the previously described progress in the areas of substrate/base electrode preparation techniques and reaction process definition. Progress was achieved by scaling progress on small area test devices and mini-modules to large areas.

Although high efficiency large area modules have been fabricated during this phase of the contract, initial efforts to transfer processes from small reactors to an existing large reactor met with limited success due to yield and reproducibility issues. The difficulty in scaling is related to both the part size and the geometry or design concept of the existing large area reactor. These issues were addressed in both large and small scale reactors during Phase 3 of this contract. Experience gained throughout the three phases of this contract indicates that the design concept of the existing reactor is not appropriate for large scale production. Future efforts will address the design requirements anticipated for large-area reactors.

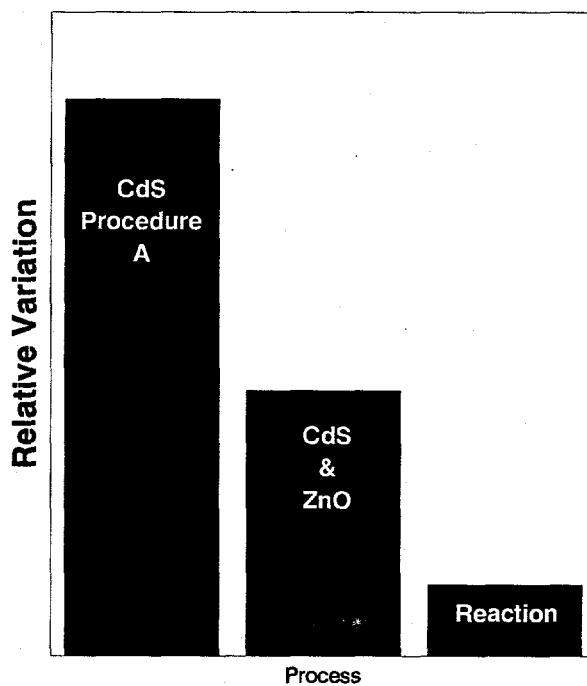


Figure 65. "Group 1" (see text) - Relative Process Variation

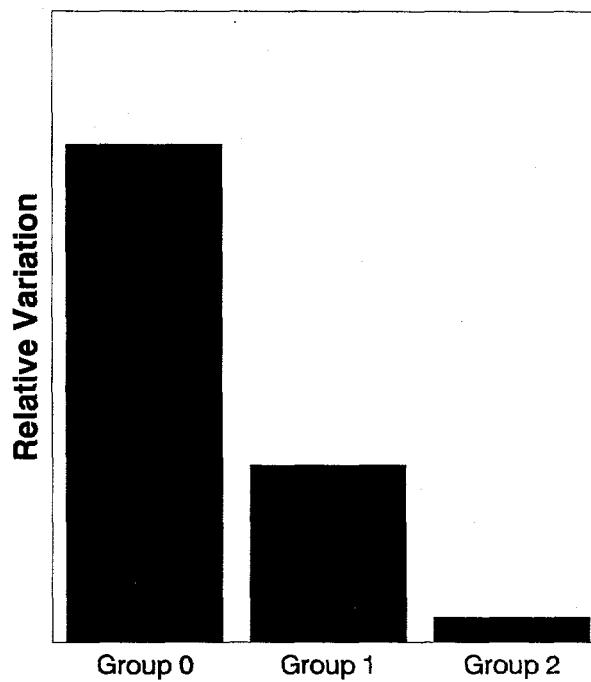
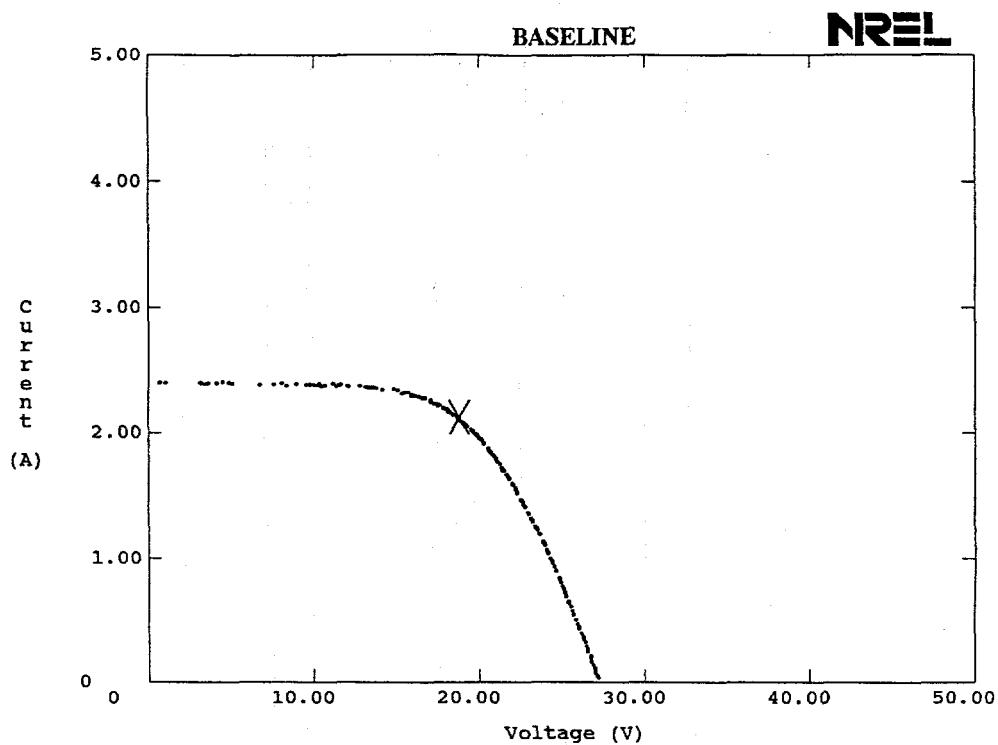


Figure 66. 85% reduction in variation illustrating how implementation of SPC techniques have been used to successfully identify the source and then to demonstrate reduced process variation.



Voc	27.2 V
Isc	2.40 A
Pmax	39.7 W
V _{pmax}	18.8 V
I _{pmax}	2.11 A
Fill Factor	60.6 %
Efficiency	10.3 %

Figure 67. Large area (3860 cm²) encapsulated module with aperture area efficiency of 10.3% verified by NREL.

Conclusions

Siemens Solar Industries (SSI) has pursued the research and development of CuInSe₂ (CIS) thin film PV technology since 1980. The objective of this contract (No. ZN-1-19019-5) was to achieve progress toward the polycrystalline thin-film milestones of the DOE Five Year Plan. SSI began this 3-year, 3-phase cost-shared contract on May 1, 1991 with the overall project goal of fabricating a large area, stable, 12.5% aperture efficient encapsulated CIS module by scalable, low-cost techniques on inexpensive substrates.

Demonstrated encapsulated module efficiencies (encapsulated 12.8% efficient mini-module on 68.9 cm² and a NREL-verified 12.7% efficient circuit on 69 cm² with a prismatic cover) are the highest mini-module efficiencies for any thin film technology. A champion large area (3860 cm²) encapsulated module efficiency of 10.3% has also been demonstrated (verified by NREL). This is the first thin film module of its size to exceed the 10% efficiency level. SSI also supplied NREL with a one kilowatt array of large area (~3890 cm²) approximately 30 watt modules. The NREL verified performance of this array is a significant step toward meeting the efficiency target of the U.S. DOE Five-Year Plan Goals of 8-10% efficient commercial thin film flat plate modules.

Long term outdoor stability of CIS and CIS-based absorbers has been demonstrated by testing at NREL. Excellent stability has been demonstrated for six years of outdoor exposure. Stability of the 1 k W Siemens CIS array installed and tested at NREL has also been demonstrated for an exposure of approximately one year.

All contract milestones were met in Phase 1 and Phase 2. Yield and predictability issues are paramount when considering production of CIS modules by scalable, low-cost techniques on inexpensive substrates. High-efficiency cells and large area modules were demonstrated; however, the yield of these modules was poor. Therefore, a strategic decision was made to deemphasize large area module fabrication and address yield issues using small area test devices and modules. This shift greatly enhanced the ability to identify root causes of yield loss in module fabrication and make progress on the overall project goal of fabricating large area, stable, and efficient encapsulated CIS modules by scalable, low-cost techniques on inexpensive substrates.

The most critical issues determining module yield were grouped into three major categories: 1) the uniformity and reproducibility of the absorber formation process, 2. the interaction of the substrate with the films and 3) performance losses near interconnects. The issues in categories one and two were addressed through the adoption and further refinement of a graded absorber formation process in which the surface layer of CIS incorporates sulfur, combined with the appropriate substrate preparation. Studies of the interactions between the substrate, base electrode, precursors and the reaction process allowed the

development of base electrode preparation techniques which addressed the issue of performance losses near interconnects. These studies of interactions indicated the need to modify both the substrate / back electrode preparation techniques and the reaction process.

The major challenge to move from development to production is to improve reproducibility rather than to improve champion device performance. Therefore, current emphasis has been placed on reduction of process variation based on the application of the statistical process control (SPC) discipline, improved diagnostics, and thorough protocols. These tools have been used to identify major sources of process variation and to successfully reduce this variation. Reduction of variation efforts also accelerate progress in other tasks by providing a consistent and well defined baseline process.

The foundations have been laid to meet the thin-film milestones of the DOE Five Year Plan. Outdoor testing has demonstrated excellent intrinsic module stability. Future plans include scaling these results to larger areas and emphasizing the reduction of variation methodology to demonstrating the potential of CIS as a future commercial product.

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13. ABSTRACT (Maximum 200 words) This report is the final subcontract report, describing work performed by Siemens Solar Industries (SSI) under a 3-year subcontract to fabricate a large-area, stable, 12.5% (aperture)-efficient encapsulated CuInSe ₂ (CIS) module by scalable, low-cost techniques on inexpensive substrates. The demonstrated encapsulated module efficiencies (encapsulated 12.8%-efficient mini-module on 68.9 cm ² and an NREL-verified 12.7%-efficient unencapsulated circuit on 69 cm ² with a prismatic cover) are the highest reported mini-module efficiencies for any thin-film technology. A champion large-area (2860 cm ²) encapsulated module efficiency of 10.3% was also demonstrated (and verified by NREL). This is the first thin-film module of its size to exceed the 10% efficiency level. SSI also supplied NREL with a 1-kW array of large-area (~3890 cm ²) approximately 30-W modules. The NREL-verified performance of this array is a significant step toward meeting the efficiency target of the U.S. DOE Five-Year Plan goals of 8%-10%-efficient commercial thin-film, flat-plate modules. Long-term outdoor stability of CIS and CIS-based absorbers was demonstrated by testing at NREL. Excellent stability was demonstrated for 6 years of outdoor exposure. The stability of the 1-kW Siemens CIS array, installed and tested at NREL, was also demonstrated for an exposure of about 1 year. The foundations have been laid to meet the thin-film milestones of the DOE Five-Year Plan. Outdoor testing has demonstrated excellent intrinsic module stability. Future plans include scaling these results to larger areas and emphasizing the reduction of variation methodology to lay the foundation for demonstrating the potential of CIS as a future commercial product.			
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