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LDRD 10729 Ultra Miniaturization of RF using Microwave Chip on Flex Technology, FY02 Final Report

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Abstract

This report describes the activities on the "Ultra Miniaturization of RF" project conducted as part of Sandia's Laboratory Directed Research and Development (LDRD) program. The objective was to evaluate a multichip module technology known as Microwave Chip on Flex (MCOF) [1], which is a newer form of the standard high density interconnect (HDI) technology originally developed by General Electric and Lockheed Martin [2,3]. The program was a three-year effort. In the first year, the team focused on understanding the technology and developing a basic design library. In the second year, devices and interconnects used at L, X, and Ku frequency bands were evaluated via a test coupon (with no application specific circuit design). In the third year, we designed, fabricated, and evaluated a specific Ku-band circuit. The circuit design and layout was performed by Sandia, and the module fabrication was performed by Lockheed Martin Government Electronic Systems.

In MCOF technology [1], bare die are placed face down on an adhesive backed flex circuit. The first level of the circuit is a pre-patterned titanium copper thin film metal system on a polyimide dielectric material. The complete module is then framed and filled with an epoxy encapsulant. The module is flipped and via holes are laser drilled through subsequent interconnect layers. Each addition layer is adhered to the top of the module and laser drilling repeated. The baseline design consisted of the original pre-patterned layer plus two additional metal layers. The base of the module is then machined so the heat spreader and frame are planar for a good thermal and electrical connection to the next assembly. This report describes the efforts conducted to evaluate the technology and its applicability to Sandia RF systems.

Table of Contents

Figures

Tables

1.0 Introduction

This report describes the effort conducted to evaluated HDI-MCOF technology for use in miniaturizing Sandia RF and microwave circuits. It will be presented in two sections. The first section will describe an initial design and the thorough evaluation of individual devices and their interconnections. It includes a summary of the design and recommendations for a follow up design. The second section will describe the follow up Ku-band module design and its performance. The Ku-band module design was based on the miniaturization of an existing circuit implemented using soft substrates and chip and wire assembly. This approach facilitates a direct comparison between MCOF and traditional assembly techniques. These sections will be followed by the final conclusions.

2.0 Initial Design and Test Description:

The initial High-Density Interconnect (HDI) modules were designed by George Sloan (SNL 2345). The design included devices that could be utilized at L, X and Ku-bands. The design rules developed by Lockheed Martin [4] were strictly followed, which included system interconnect and transmission lines parameters. The design layout enabled the testing of individual devices with coplanar ground-signal-ground (GSG) probes, as well as combining subcircuits with top surface ribbons. It also featured via-hole-grounded shield walls and an array of transmission lines which included via connected microstrip to stripline transitions for evaluation of the dielectric properties.

Twenty modules were built. Each module included four active monolithic microwave integrated circuits (MMICs) and eight passive structures. These devices are typically of those that would be used to design a Sandia Transmit / Receive (T/R) module or RF tag. A picture of the initial HDI module design with all the surface mount components attached is shown in Figure 1. An AutoCAD file in figure 2 shows the module top view. It includes labels of the active devices and passive structures. The active devices were labeled U1 through U5. The passive structures were labeled s1 through s7.

Initial Design and Test Description:

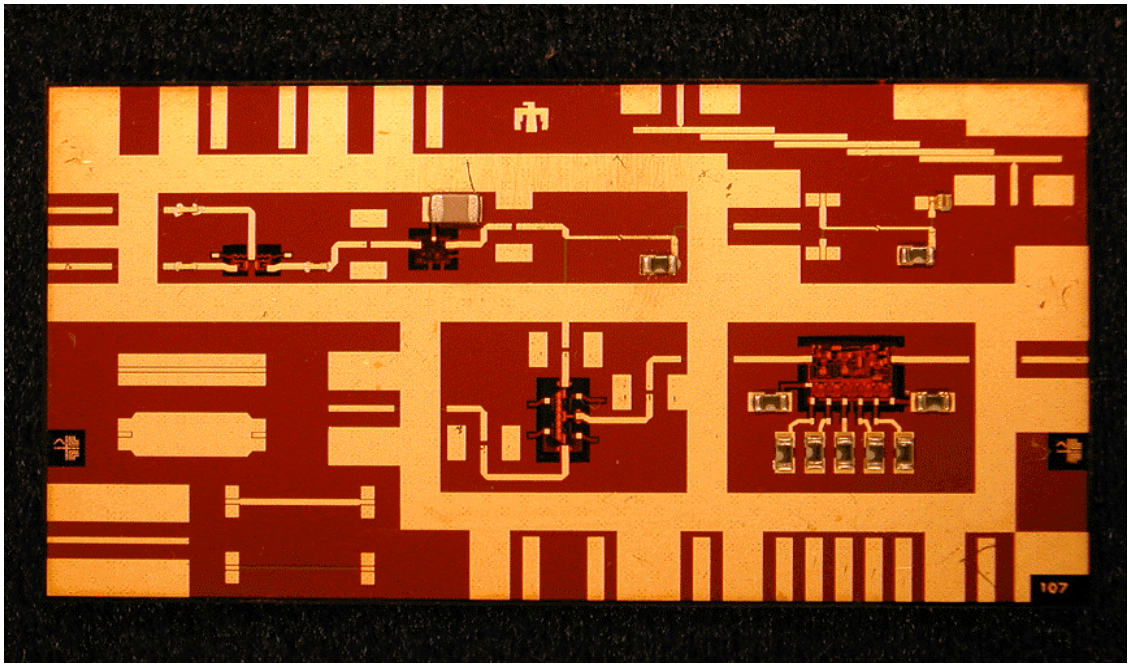

Figure 1 HDI module with SMT passive top-level components installed

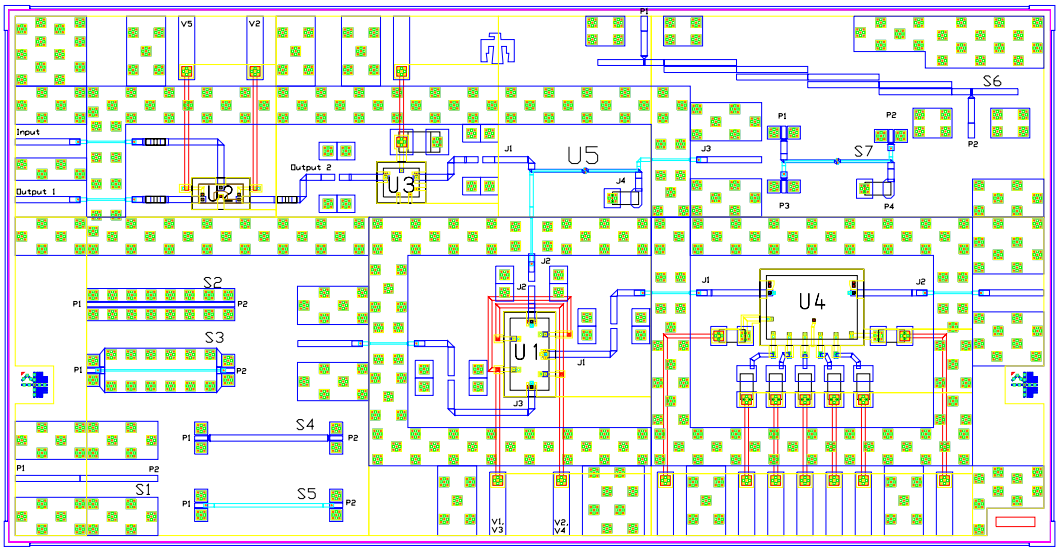

Figure 2 AutoCAD drawing of HDI module with circuit symbols

1.0 Initial Design and Test Description:

Sandia provided the MMIC die for the HDI modules. The approach was to test all devices before assembling them into modules. Each active device was then mounted on a gold plated, 30 mils thick [1]Silvar ™ shim (heat spreader). The MMIC die were attached using [2]Staystik 181™. The shims were designed to be 10 mils longer and wider than the corresponding die so that the MMICs could be centered on the heat spreader as shown in Figure 3. On-wafer electrical tests were performed on all devices prior to module assembly, except for the TriQuint Semiconductor (TQS) switch. (The TQS switch had a microstrip interconnect which was not compatible with our on-wafer probes.) Instead, a special heat spreader assembly (see figure 4) was utilized to obtain test data for subsequent comparison with the HDI module data. Table 1 lists the active devices and their part numbers, along with functional descriptions of their proposed use.

Circuit Symbol	Active Device description and Part numbers
U1	Alpha Switch [5], GaAs IC SPDT non-reflective DC to 18 GHz, P/N AS018M2-00
U2	TriQuint Semiconductor Switch [6], SPDT FET Switch, P/N TGS8122-SCC
U3	M/A Com Low Noise Amplifier [7] , GaAs MMIC Amplifier, P/N MAAM71200
U4	TQS Phase Shifter [8], 6-18 GHz 5 bit, P/N TGP6336-EEU

Table 1 Active devices used in the initial Sandia HDI module design.

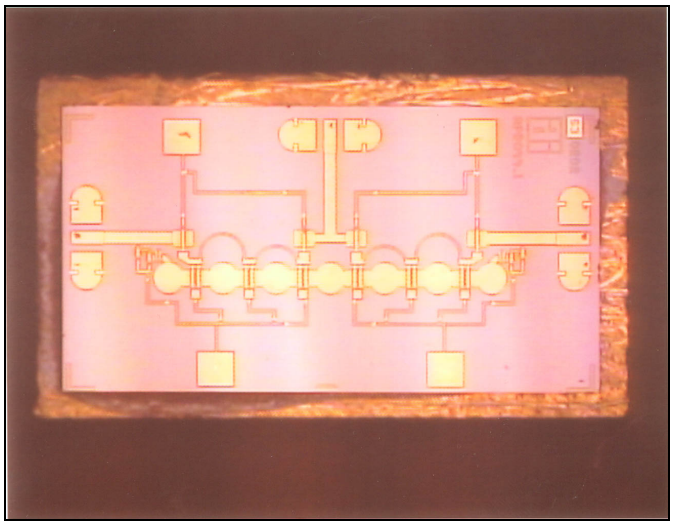

Figure 3 Alpha Switch MMIC Die (U1) on a Silvar™ heat spreader prior to assembly in a HDI module. Alpha die are suitable for coplanar waveguide (CPW) on-wafer testing.

[1] Silvar is a nickel-iron alloy and silver developed Texas Instruments Advanced Packaging Group

[2] Staystik is a silver filled thermal plastic adhesive used for a die attach manufactured by STAYSTICK INC.

2.0 Initial Design and Test Description:

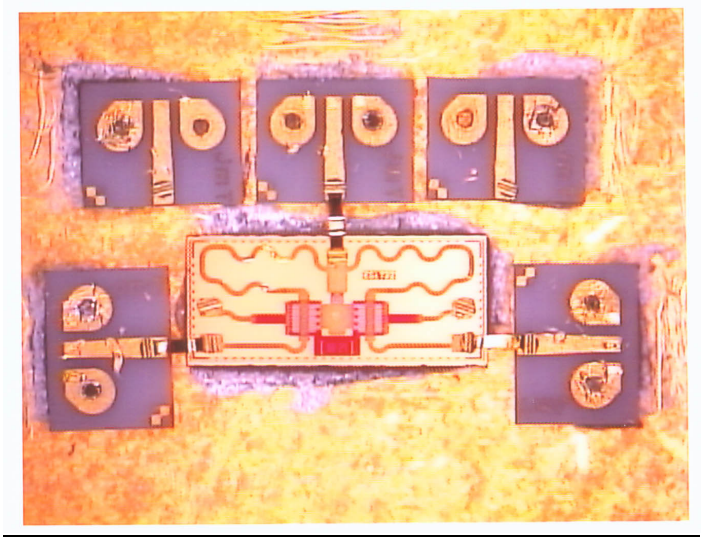

Figure 4 is a TriQuint Semiconductor (TQS) Switch in the special heat spreader configuration. The TQS switch has microstrip interconnect and required Jmicro Technology (JMT) ProbePoint™ (PP0503) CPW to microstrip alumina transitions to enable on-wafer probing.

Table 2 is a list of the passive device structures that were characterized. The description includes the type of structure and the probe spacing. U5 is not an active device. It is the same passive structure as S7 with a different probe pitch. (It is located in the RF signal path so it was given a U circuit symbol.)

Structure #	Passive Device description and probe pitch spacing
S1	Microstrip transmission line with signal side ground, wide pitch
S2	Coplanar Waveguide (CPW) with ground plane, narrow pitch
S3	CPW to strip line, narrow pitch
S4	CPW to microstrip, narrow pitch
S5	CPW to buried microstrip, narrow pitch
S6	CPW to Coupled Line Bandpass Filter, wide pitch
S7 / *U5	CPW to 4 port Coupled Line Coupler, narrow pitch / * wide pitch for U5

Tables 2 Passive structures in the Sandia HDI module that were characterized

2.1 Test Methods and Setup:

Testing of the initial HDI modules and mounted die was accomplished using on-wafer probes to obtain S parameters. Two types of probes were utilized which had an effect on the frequency response that could be achieved. The (ACP40GSG150)[3] probe had a narrow pitch and was used to test mounted die and the passive structures (S2, S3, S4, S5, and S7). The narrow pitch probe was capable of accurate calibration up to 40 GHz. The (ACP40GSG950)[4] probe had a wide pitch and was used to test the other passive structures (S1, S6), as well as all active HDI devices (which were designed with a wide pitch similar to that used on S1). This wide pitch probe was capable of accurate calibration up to 20 GHz.

Small signal s-parameters were taken on all devices using an HP8510C Vector Network Analyzer (VNA) (Figure 5). RF connections were made using on-wafer probes mounted on a manual Cascade Microtech Summit 9000 Probe station. DC connections were made using Alessi probes and power was applied with Tektronics power supplies (series 5000). All of the on-wafer calibrations and s-parameter measurements were taken with [5] WinCal™ using the (LRRM) calibration method. The calibration reference plane was set at the wafer probe tips. Agilent Technology's Advanced Design System (ADS) software [9] was utilized for model development and analysis. Agilent Technology's High Frequency Structure Simulator (HFSS), a 3D Electro Magnetic (EM) simulator [10], was employed for the design and analysis of the more complex structures.

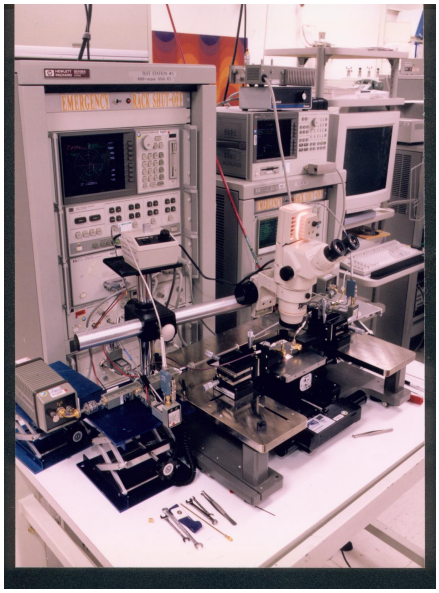

Figure 5 Vector Network Analyzer (VNA) test setup and probe station with Air Coplanar Probes (APC).

[3] Cascade MicroTech's Air Coplanar, 40 GHz, ground-signal-ground, 150 um center to center spacing

[4] Cascade MicroTech's Air Coplanar, 40 GHz, ground-signal-ground, 950 um center to center spacing

[5] WinCal is a VNA calibration and measurement software. Line-Reflect (open)-Reflect (short)-Match is the calibration method utilized. The preceding items were both developed by Cascade MicroTech.

2.2 Measurement Summary:

The Alpha switch, the M/A Com LNA, and the TQS Phase Shifters performed mostly as expected. The devices exhibited a slightly higher loss due to the encapsulation of the die. The additional loss was between 0.4 to 1.2 dB for each die. Isolation for the off-state switches was significantly degraded. Normally this would be of great concern; however, in this case, there was a poor ground connection between the backside of the heat spreader and the wafer probe ground. It is expected that this isolation would improve with a better system ground. The TQS switch had poor overall performance. We believe this is due to the fact that the die did not include a good topside ground for HDI connection. Also, the control lines were routed directly over some of the dies critical RF structures.

The passive structures (S1 through S7) were designed using a relative dielectric constant of 3.2 and a loss tangent of .008. The transmission lines performed as expected, and yielded a frequency response greater than 28GHz. The attenuation constants for the various lines ranged from 0.044dB/mm to 0.081dB/mm. The corresponding phase constants varied from 17.5 degrees/mm to 21.4 degrees/mm (all comparisons were made at 10GHz). Table 3 contains a complete summary of the critical line parameters. The coupled line filter (S6) and broadside coupler (S7) designs had higher center frequencies and higher losses than the models predicted. This would imply that the HDI modules have a lower relative dielectric constant and higher loss tangent than was originally advertised by Lockheed Martin's design guide [4].

Structure #	Freq. (GHz)	Z0 (ohms)	Attenuation (dB/mm)	Phase (degrees/mm)	Er *	TanD*
S1	>20	51.4	0.054	18.3	3.0	0.029
S2	>40	53.3	0.044	17.5	3.0	0.018
S3	>40	40.7	0.081	19.3	3.0	0.034
S4	>40	51.4	0.039	18.8	3.0	0.022
S5	>40	50.0	0.044	21.4	>3.0	~0.018

Table 3 is a comparison of critical transmission line parameters at 10 GHz.
* Er is the relative dielectric constant and TanD is the loss tangent

Via connections on the initial HDI modules were also a problem. Some vias had a higher than desired resistance of 3 to 250 ohms, where a normal via resistance is less than 0.080 ohms. This problem caused higher insertion loss on some via connected transmission lines. In one case, a high resistance via prevented the DC bias connection to a phase shifter. Figure 6 is an illustration of the HDI construction [11], showing metal and dielectric levels. Table 4 shows the complete metal stack composition and metal thickness, while Table 5 lists the via holes sizes. Seven of fourteen modules were found to have at least one via problem from metal 3 (MT3) to metal 2 (MT2). Since there is no direct access to vias below MT2, the full extent of the problem could not be easily determined. Our investigation showed that the via failures were the result of faulty metalization. The problem appears to be a void in the underlying metal. Figure 7 is a cross section image of a faulty (high resistance) via obtained by means of a focused ion beam (FIB) cut. Notice that the grainer looking metal (Ti/Cu/Cu) did not completely fill. The gold (Au) top metal is unable to fill the void leaving an open circuit or a high resistance path. Figure 8 is a FIB taken of a normal low resistance via. The good via

clearly shows complete coverage of the underlying (Ti/Cu/Cu) metal and a complete gold metalization.

2.2 Measurement Summary:

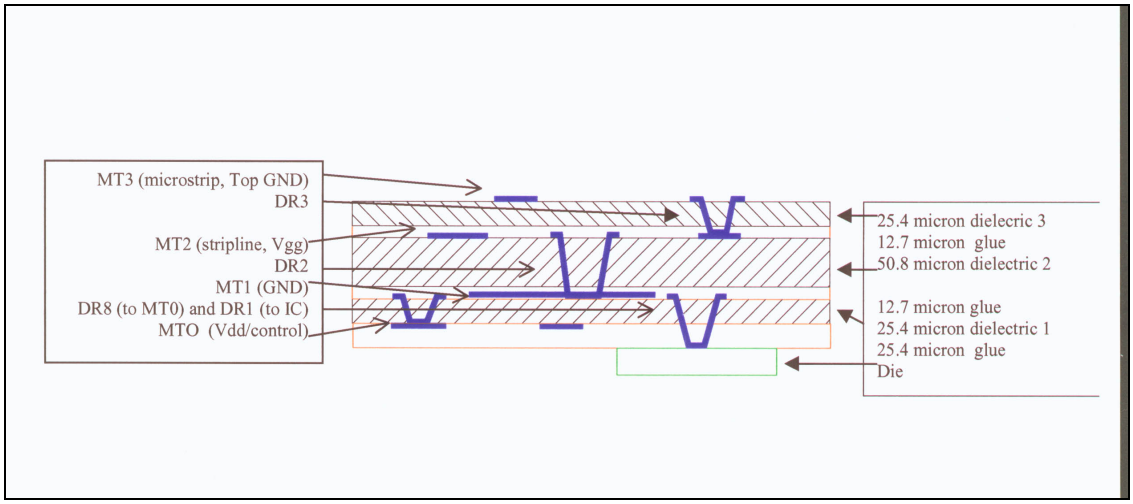

Figure 6 is an illustration of HDI construction [11]

Metal Layer	Sputtered Metal Seed Layer(Angstroms)	Electroplated Metal(microns)	Sputtered /Plated(Angstroms unless indicated*)	Total (microns)
MT0	120 Ti, 3K Cu	15 Cu	None	15.312
MT1	1K Ti, 6K Cu	4 Cu	1K Ti	4.8
MT2	1K Ti, 6K Cu	8 Cu	1K Ti	8.8
MT3	1K Ti, 3K Cu	4 Cu	1K Ti, 1K TiW, 1um *Au Plated	5.6
Backside	1K Ti, 1K TiW	1 Au	None	1.2

Tables 4 HDI Metal layers composition from Lockheed Martin's design guide [4]

Drill Layer	Nominal Via size	
	Top	Bottom
Drill 1 (DR1)	60 microns	35 microns
Drill 8 (DR8)	45 microns	25 microns
Drill 2 (DR2)	90 microns	60 microns
Drill 3 (DR3)	45 microns	25 microns

Table 5 HDI via hole and drill sizes from Lockheed Martin's design guide [4]

2.2 Measurement Summary:

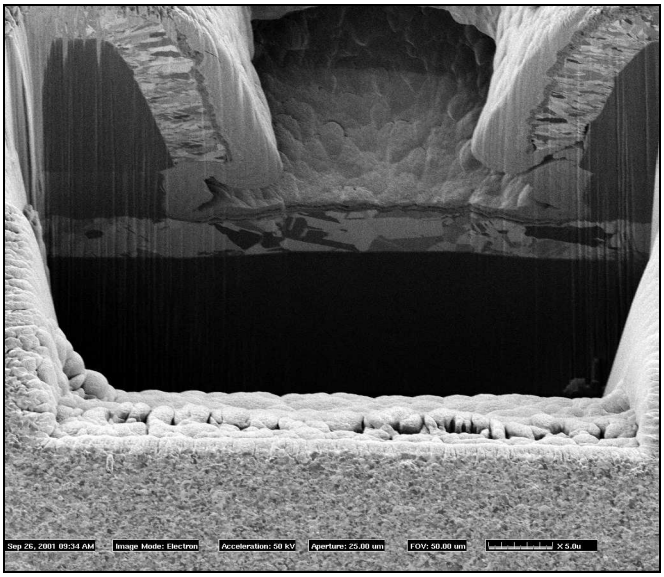

Figure 7 is a cross-section image of a high resistance via hole taken with a focused ion beam system. (Courtesy of Ed Cole, Failure Analysis Department, 1739)

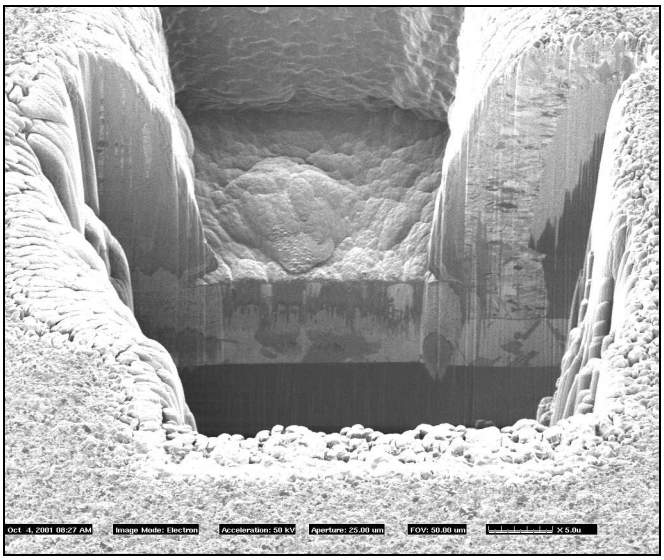

Figure 8 is a cross-section image of a (normal) low resistance via hole taken with a focused ion beam system. (Courtesy of Ed Cole, Failure Analysis Department, 1739)

2.3 Active Device Test Results:

2.3.1 Alpha Switch:

The measured results for the Alpha Switch (U1) [5] in HDI are plotted in Figure 9. The switch has a typical on-state insertion loss of 4.67 dB, and a return loss of greater than 10 dB (at 10GHz). Figure 10 shows the corresponding isolation state measurements.

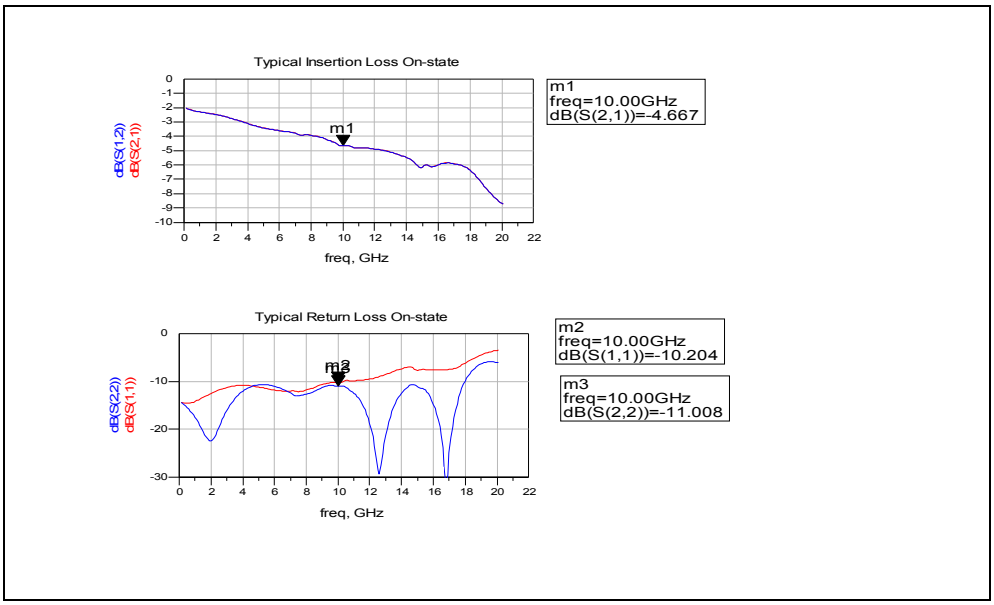

Figure 9 Alpha Switch Typical Insertion Loss. The top plot is S21 and S12 insertion loss in dB. The bottom plot is the input and output return loss.

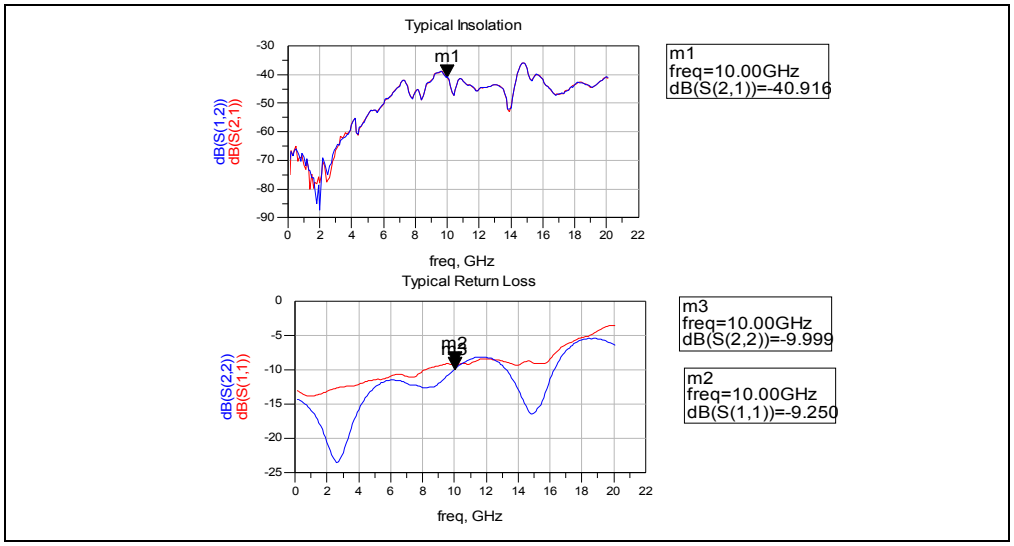

Figure 10 Alpha Switch typical isolation in HDI. The top plot is S21 and S12 isolation in dB. The bottom plot is the associated input and output return loss.

2.3.1 Alpha Switch:

Twelve of fourteen Alpha switches were found to be functional and these results are summarized in tables 6, 7, and 8. Table 6 is a summary of the average measurements of HDI-embedded switches. Table 7 contains an average of the pre-assembly die results. Table 8 is an estimate of the average insertion loss caused by die encapsulation and transmission lines to the measurement points.

State	Path	Insertion loss or Isolation(dB)	Input Return Loss(dB)	Output Return Loss(dB)
On	J1-J3	4.67	10.5	10.7
On	J1-J2	4.04	10.13	12.9
Off	J1-J3	40.3	8.6	9.66
Off	J1-J2	40.7	11.1	13.2

Table 6 Average HDI measurements for U1-Alpha Switch, at 10 GHz

State	Path	Insertion loss or Isolation(dB)	Input Return Loss(dB)	Output Return Loss(dB)
On	J1-J3	2.9	8.9	11.2
On	J1-J2	2.89	10.13	12.9
Off	J1-J3	54.7	Not measured	Not measured
Off	J1-J2	54.7	Not measured	Not measured

Table 7 Average pre-assembly device measurements for U1-Alpha Switch, at 10 GHz

Path	Die Insertion Loss(dB)	Transmission Line loss(dB)	Die loss due to HDI(dB)	HDI total loss(dB)
J1-J3	2.9	.5	1.27	4.67
J1-J2	2.89	.28	0.87	4.04

Table 8 Average loss of device die due to encapsulation (U1-Alpha Switch), at 10 GHz

2.3.2 TriQuint Semiconductor Switch:

The TQS Switch [6] (U2) had undesired in-band resonance points that adversely affected the insertion loss and isolation. We believe the primary cause is that the die lacked good signal side ground pads to access for HDI connections. (The die depends on the chip backside to provide a low inductance ground path; only a single questionable pad was available for a topside HDI ground connection.) Another probable source of switch's poor performance was the routing of control lines over critical RF lines. Whatever the cause, it appears that this type of die was a poor choice for inclusion in an HDI module. Hence, one clear lesson learned is that die used in HDI modules should have coplanar launches with multiple topside grounds, and control pads that can be accessed without crossing over RF lines. Figure 11 clearly illustrates that the performance of this type of die is unacceptable in the current HDI configuration. More investigation would be needed to determine if some alternative layout could solve the problem. One idea would be to have direct via connections between MT1 (HDI ground) and the die shim. The easier course of action is to simply avoid this type of die.

2.3.2 TriQuint Switch:

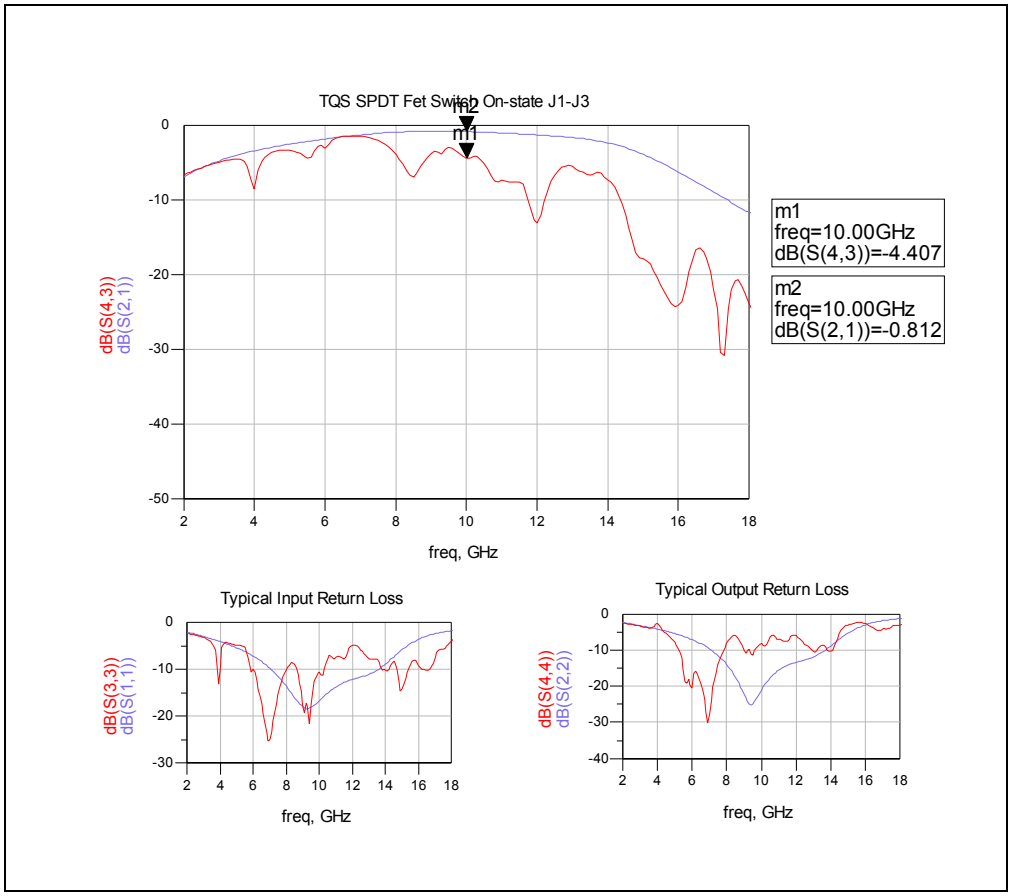

Figure 11 TriQuint Semiconductor switch (U2) on state J1-J3 red (Marker1) in a HDI module and blue (Marker2) is nominal device die. The top plot is S21 on-state transmission in dB and the bottom two plots are input and output return loss in the on state.

2.3.3 M/A Com LNA:

The M/A Com LNA [7] (U3) had a nominal gain of 15.6 dB and return loss greater than 10dB (at 10 GHz). The packaged gain is about 0.5 dB less than the pre-assembly (die only) value. Figure 12 shows a comparison of the pre-HDI and post-HDI measurements. The plot shows that the encapsulation process shifted/degraded the LNA's upper pass band edge and reduced the overall gain. The actual shift at the high frequency corner is about 1.3 GHz and is represented by makers 3 and 4. It should also be mentioned that three of fourteen devices had no gain and drew excessive bias current. The actual cause of failure could not be determined without additional analysis. It is unknown whether the die failure was the result of the HDI process or pre-assembly handling.

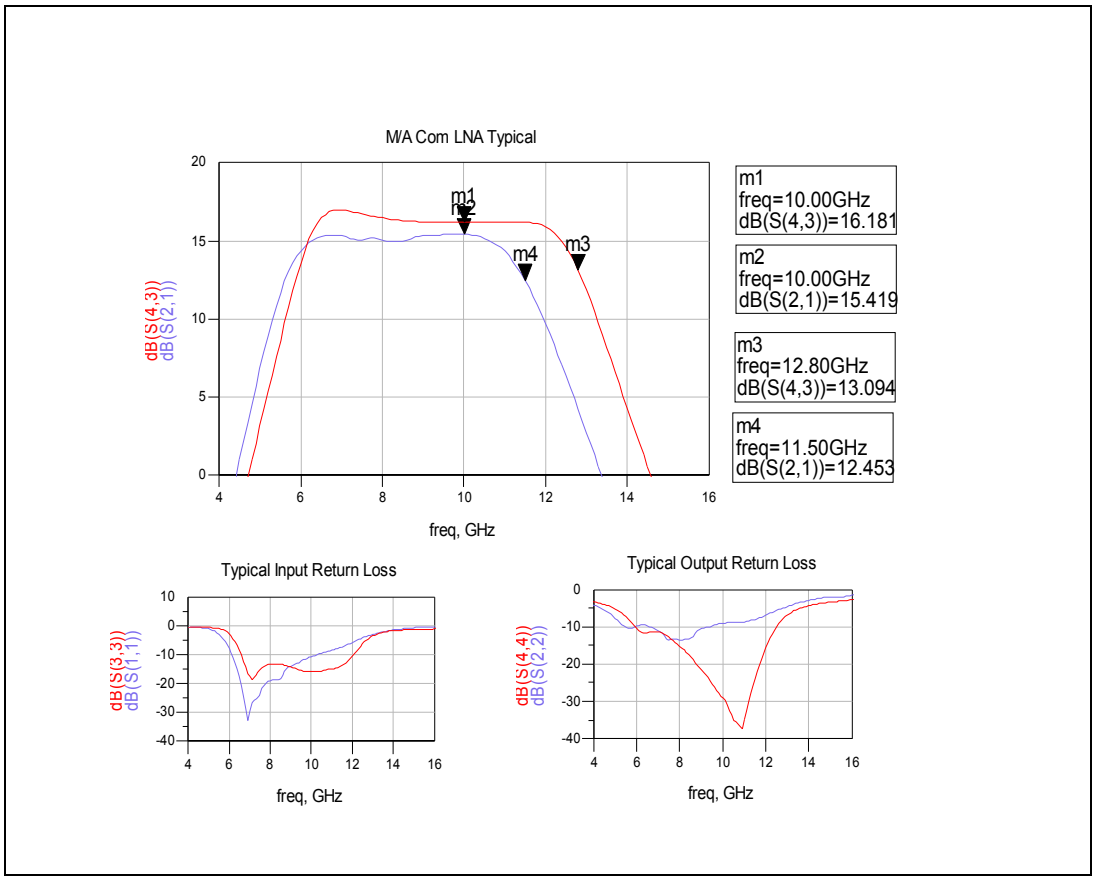

Figure 12 M/A Com LNA (U3) is a comparison of pre (in RED) and post (in BLUE) HDI assembly using nominal device measurements. The top plot is device gain (S21 in dB) Markers 1 and 2 represent the Gain at 10 GHz. The lower plots are input and output return loss under nominal bias.

2.3.4 TriQuint Phase Shifter:

Given that the LNA manifested detuning, it was surprising that the complicated TQS Phase Shifter [8] (U4) did not show any degradation in relative phase due to the topside dielectric. Figure 13 shows that the measured phase variation was less than 1 degree across the entire programmable range (at 10 GHz). For this MMIC, we made extensive use of a new HDI process where the glue is laser ablated, prior to die insertion, in areas that will cover critical structures. A post-insertion examination showed that none of the more than 100 air-bridges on the die were damaged during processing. This exceptional result proves that the new glue ablation process will protect critical paths and air bridges. The final measurements did show an additional insertion loss of about 2dB, which is consistent with the results for the other encapsulated MMICs. Figure 14 compares the pre/post assembly insertion and return losses.

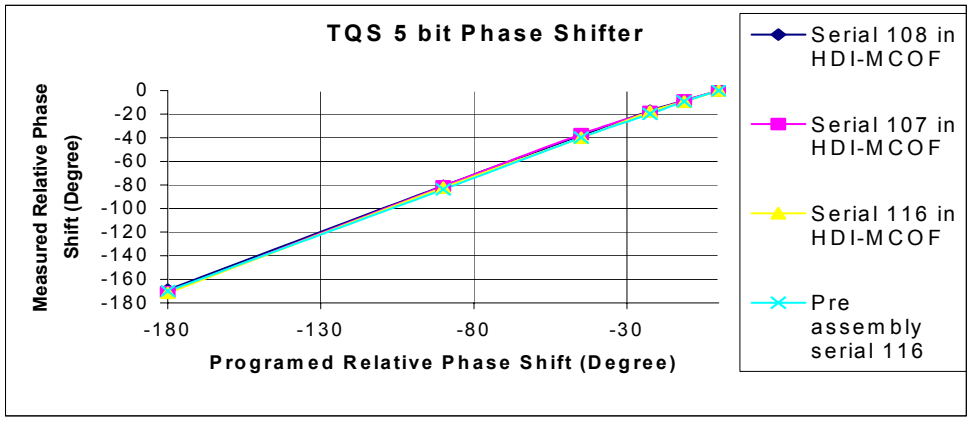

Figure 13 is the TQS Phase shifter that shows a relative phase shift at 10 GHz. The bottom trace is a pre-assembly measurement from HDI serial #116 while the other three were HDI module results.

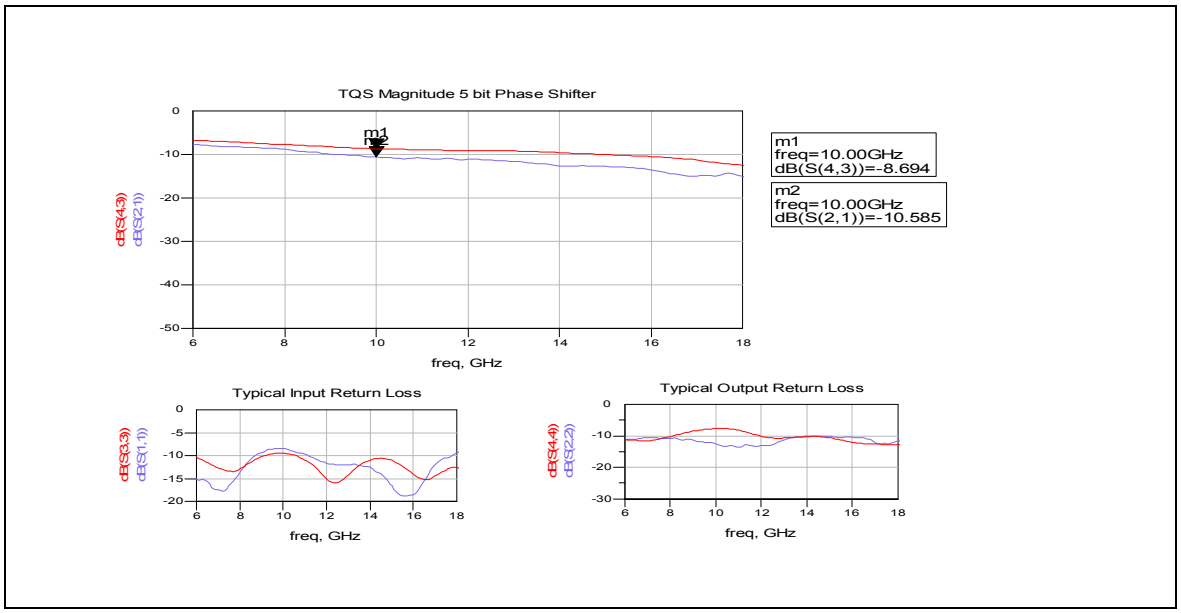

Figure 14 is a comparison of the TQS Phase Shifter pre and post assembly for insertion loss and input and output return loss. The top plot is insertion gain in dB pre-assembly (in RED) and post-assembly (in BLUE). The bottom two plots are the associated input and output return loss.

2.4 Passive Device Structures:

2.4.1 Microstrip Transmission Line (S1):

The microstrip transmission line with signal side ground (S1) has a good overall performance. The characteristic impedance (Z0) is 51.4 ohms. The attenuation constant is 0.054dB/mm with a phase constant of 18.3 degrees/mm at 10GHz. The frequency response was greater than 20GHz. As shown in figure 15, the measured/modeled data agreement was excellent out to 16 GHz. Only two S1 lines were tested and both were good. The model data was obtained from ADS using the microstrip line circuit definition and is illustrated in Figure 16. S1 type lines were used extensively throughout the module and estimates for these line losses used in this report came from the above attenuation constant.

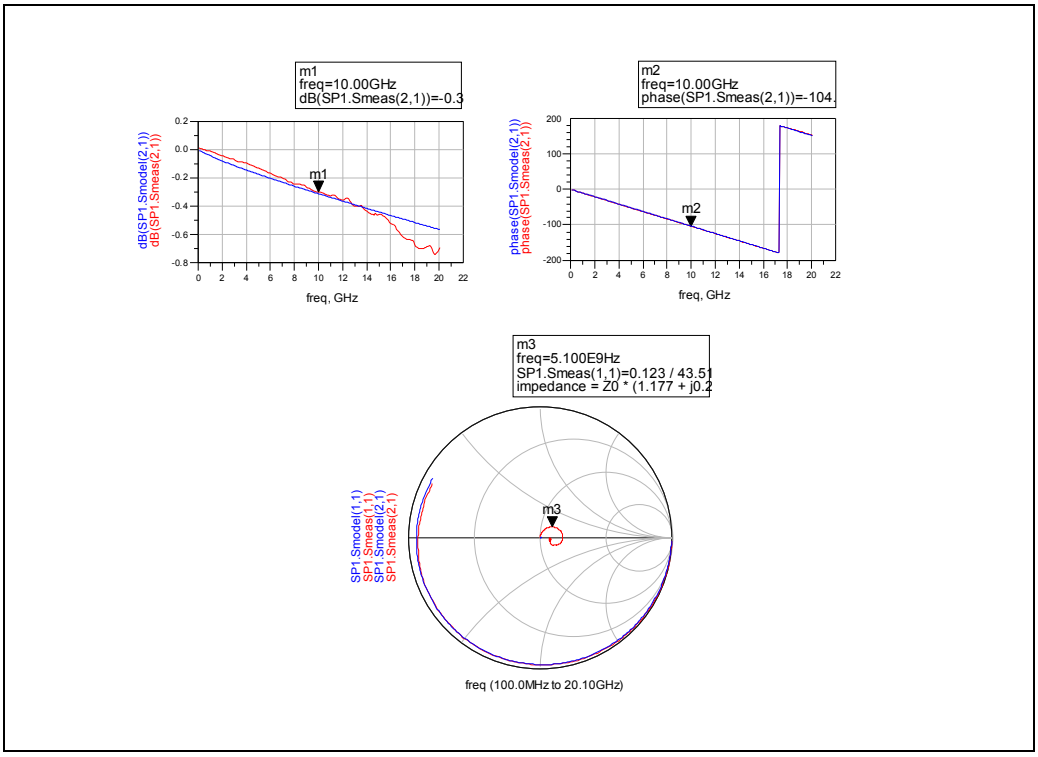

Figure 15 is a plot of a microstrip transmission line with signal side ground (S1). The top two plots are S21, measured versus modeled in dB and phase in degrees. The bottom smith chart is S11 and S21, measured versus modeled data from 0.1 to 20.1 GHz.

2.4.1 Microstrip Transmission Line (S1):

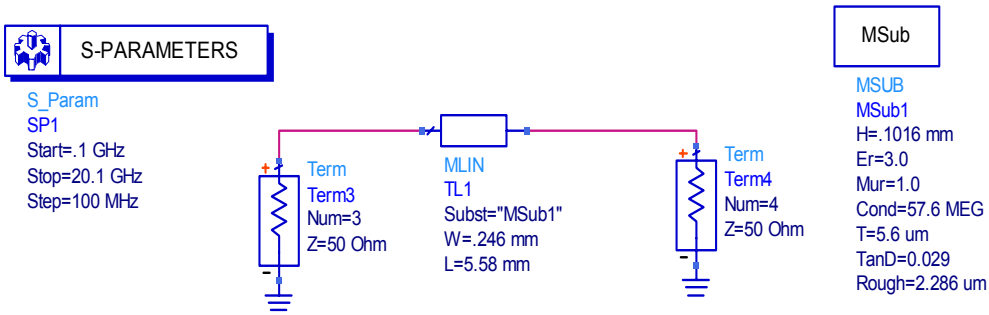

Figure 16 is the model circuit file definition from ADS using a microstrip line and the following substrate parameters:

Physical parameter

Line width = 0.246 mm

Line length = 5.580 mm

Substrate parameters:

H	=	0.1016 mm	substrate thickness
Er	=	3.0	relative dielectric constant
Mur	=	1.0	relative permeability
Cond	=	5.76e7	conductor conductivity in Siemans / meter
T	=	5.6 um	conductor thickness
TanD	=	0.029	dielectric loss tangent
Rough	=	2.286 um	conductor surface roughness (RMS value)

2.4.2 Coplanar Waveguide to Microstrip Transmission Line (S4):

The CPW-to-microstrip structure (S4) has excellent performance. The characteristic impedance (Z0) is 51.4 ohms. The attenuation constant is 0.039 dB/mm with a phase constant of 18.8 degrees/mm at 10 GHz. The frequency response was greater than 40 GHz. All fourteen lines tested were good and had similar performance. The measured versus modeled data was excellent out to 28 GHz and is shown in Figure 17. The circuit model and substrate parameters were the same as S1 (Figure 16), except for the loss tangent and physical line length. (The loss tangent was decreased to 0.022, and the line length was increased to 5.784.)

2.4.2 Coplanar Waveguide to Microstrip Transmission Line (S4):

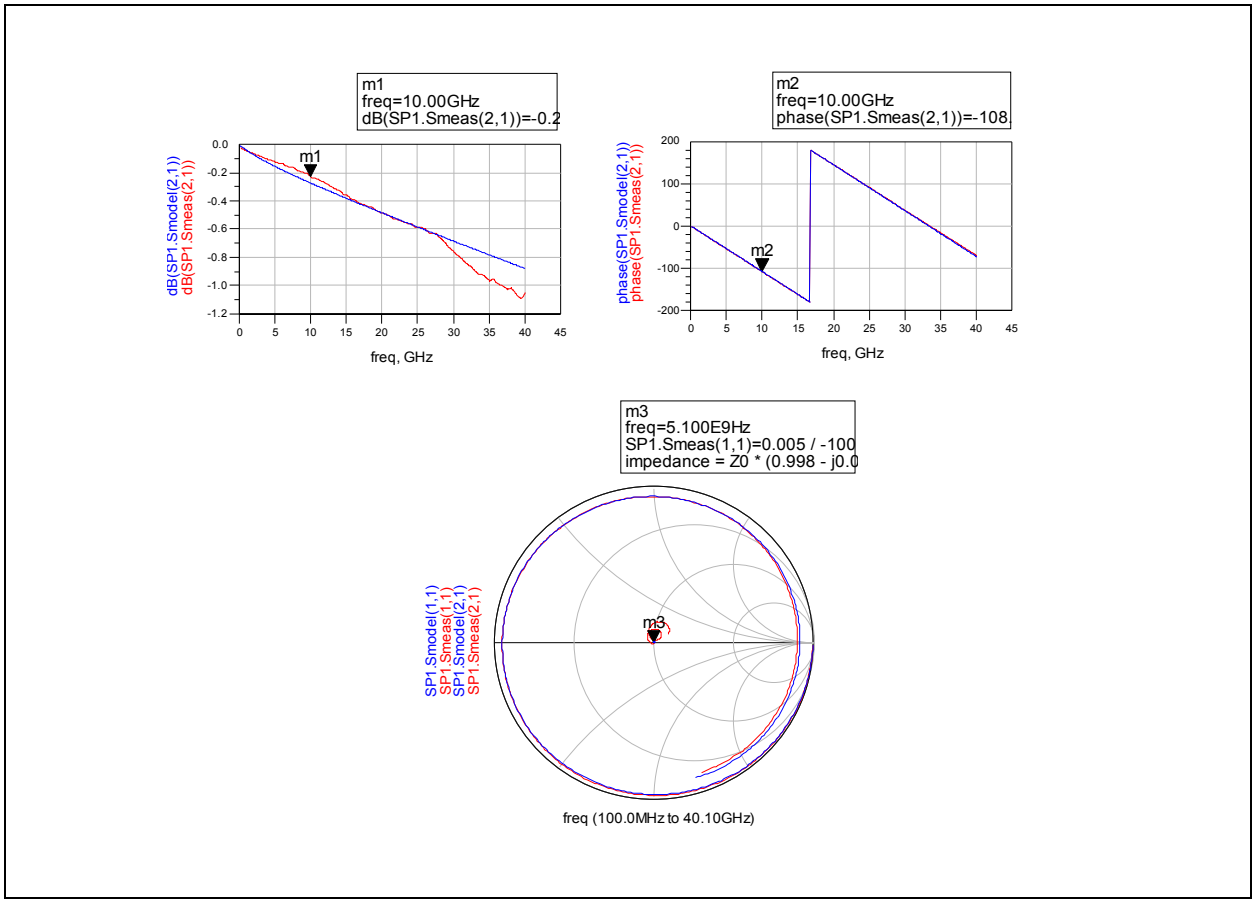

Figure 17 is a plot of a coplanar waveguide to microstrip transmission line (S4). The top two plots are S21, measured versus modeled in dB and phase in degrees. The bottom smith chart is S11 and S21, measured versus modeled data from 0.1 to 40.1 GHz.

2.4.3 Coplanar Waveguide Transmission Line (CPW) (S2):

The CPW transmission line (S2) also has excellent performance. The characteristic impedance (Z0) is 53.3 ohms. The attenuation constant is 0.044 dB/mm with a phase constant of 17.5 degrees/mm at 10 GHz. The frequency response was greater than 40 GHz. All fourteen lines tested were good and had similar performance. The line was modeled as a coplanar waveguide with ground plane (CPWG) and it used the same substrate as S1 except for the loss tangent, which was 0.018. The model used a CPW structure that is defined by Figure 18. The following physical parameters were also used for S2: Line width = 174.1 um; Line length = 5.808 mm; Line gap = 42.04 um. The measured versus modeled data had excellent agreement out to 30 GHz and is shown in Figure 19.

2.4.3 Coplanar Waveguide Transmission Line S2:

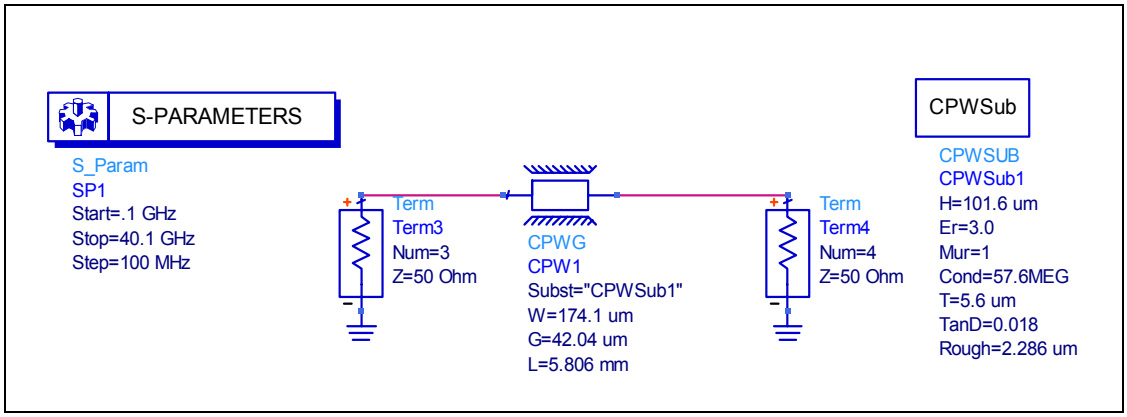

Figure 18 is a coplanar waveguide transmission line circuit model file. The loss tangent of 0.018 is lower than all other lines.

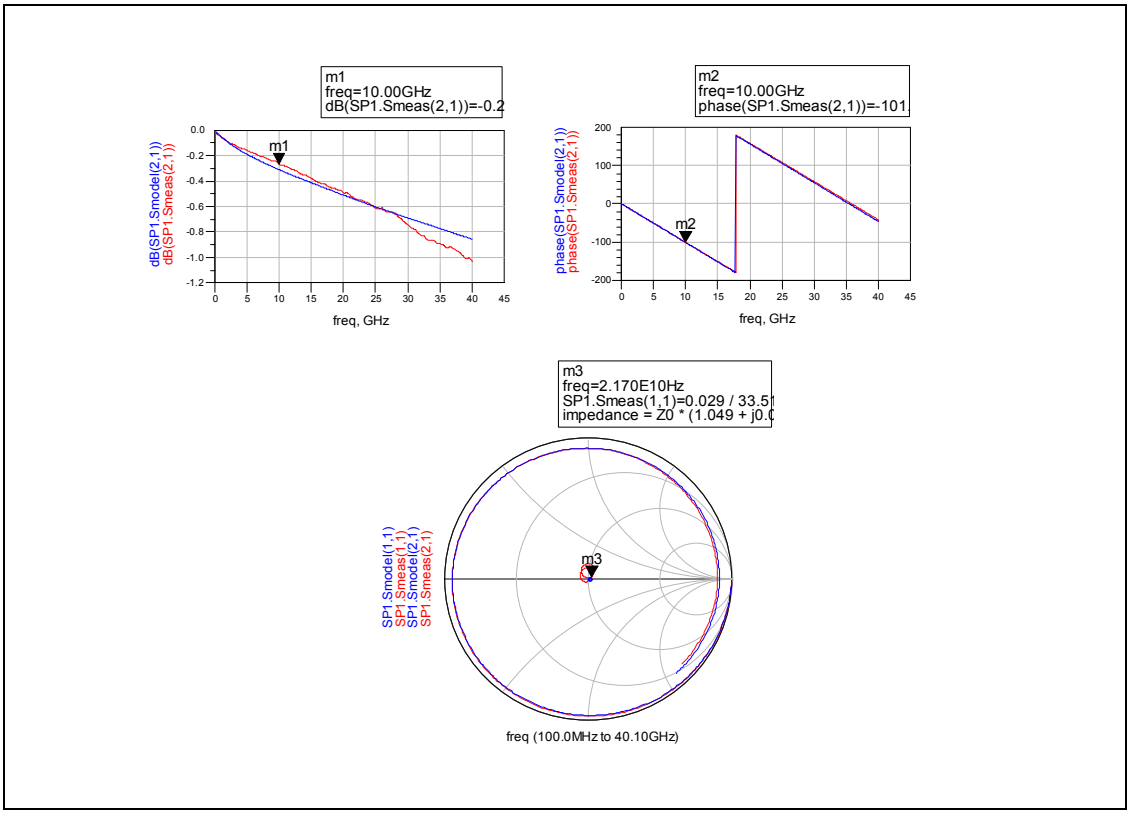

Figure 19 is a plot of a coplanar waveguide transmission line with measured versus modeled data. The top two plots are S21, measured versus modeled in dB and phase in degrees. The bottom smith chart is S11 and S21, measured versus modeled data from 0.1 to 40.1 GHz.

2.4.4 CPW to strip line (S3):

The CPW-to-stripline structure (S3) demonstrated poor performance. The design parameters were taken directly from an existing LM design, which we later learned would not yield a 50 Ohm line. The characteristic impedance (Z0) is only 40.71 ohms. The attenuation constant is 0.081 dB/mm with a phase constant of 19.3 degrees/mm at 10 GHz. The frequency response had some ripple but was still usable past 40 GHz. Twelve of fourteen lines tested good and had similar performance. The two bad lines had high resistance via holes that caused excessive insertion loss. The line was modeled as a coplanar waveguide with a via an offset stripline. This is a complex line structure and the above constants represent an average of the complete structure. Figure 20 shows the model circuit file that was used for simulation. The majority of the substrate parameters were the same as the previous, except for the loss tangent on the stripline substrate section (SsubO). It was almost twice as high as the other lines. The measured versus modeled data was excellent out to 30 GHz and is shown in Figure 21.

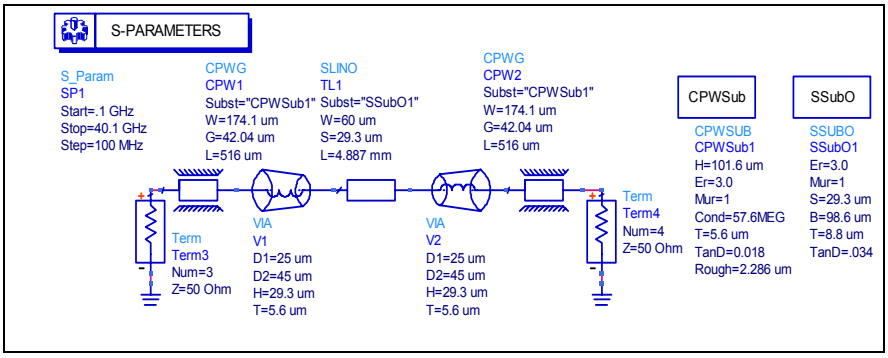

Figure 20 is a circuit model file of an offset stripline (S3). This model includes the CPW launch to via hole and then to stripline connections. The complex line required two sets of substrate parameters. Substrate (SSUBO) parameters are for the stripline and substrate (CPWSUB) parameters are for the coplanar waveguide section.

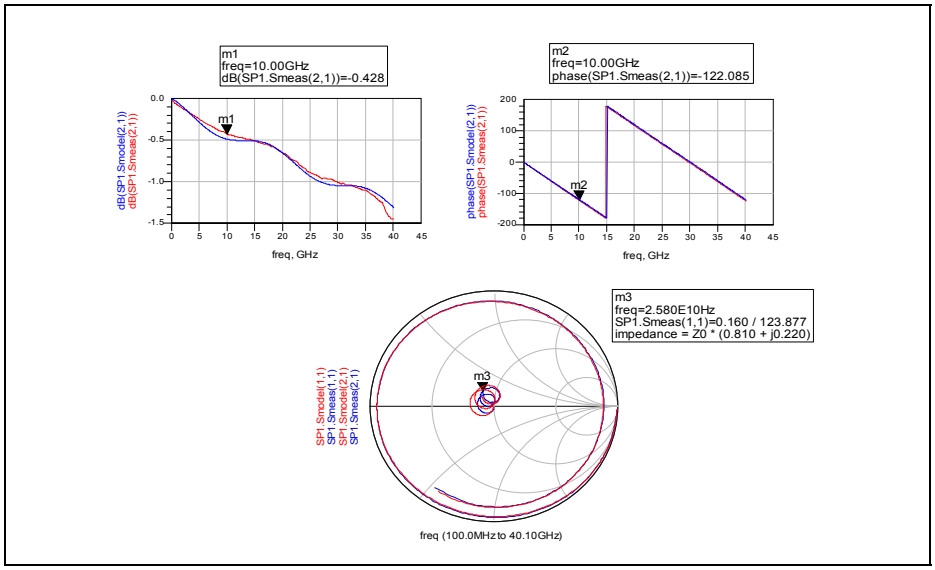

Figure 21 is a plot of a stripline with measured versus modeled data. The top two plots are S21, measured versus modeled in dB and phase in degrees. The ripple is due to the low Z0 of the stripline. The bottom smith chart is S11 and S21, measured versus modeled data from 0.1 to 40.1 GHz.

2.4.5 CPW to Buried Microstrip Transmission Line (S5):

The CPW-to-buried microstrip line (S5) has good performance. The characteristic impedance (Z0) is about 50 ohms. The attenuation constant is 0.044 dB/mm with a phase constant of 21.4 degrees/mm at 10 GHz. The frequency response was greater than 40 GHz. Ten of fourteen lines tested were good and had similar performance. The bad lines all had high resistance vias. This line was not modeled due the unavailability of a buried microstrip line element in ADS. A more complex 2D or 3D electromagnetic simulation would have been required to model this multilayer structure. The measured data was excellent out to 28 GHz and is shown in Figure 22. However, it did have a slightly higher phase shift than the standard microstrip line (S4) due to the topside dielectric loading.

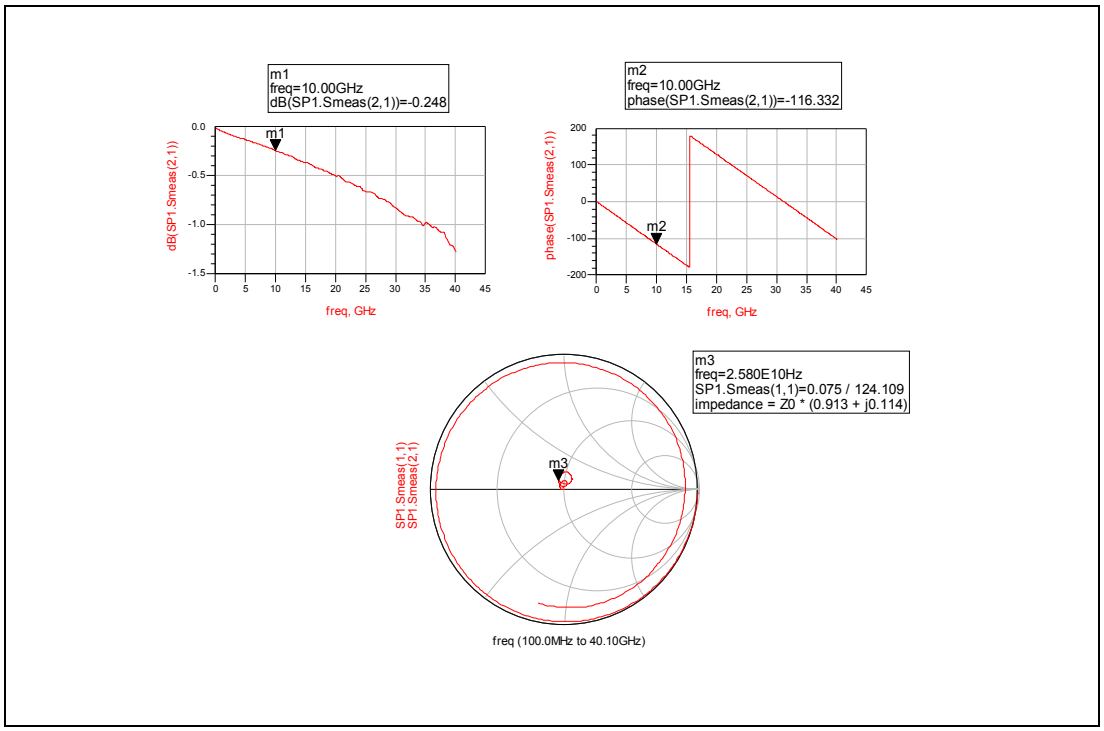

Figure 22 is a plot of a CPW to buried microstrip transmission line with measured data. The top two plots are S21 in dB and phase in degrees. The phase length is slightly higher than all other lines. The bottom smith chart is S11 and S21 measured data from 0.1 to 40.1 GHz.

2.4.6 Coupled Line Bandpass Filter (S6):

The Coupled Line Bandpass Filter (S6) was designed to be a Ku-band filter. The measured pass band had a slightly higher center frequency than was intended. The insertion loss was also slightly higher by about 0.4 dB, when the excess transmission lines are taken into account. The return loss and filter roll-off are similar to the modeled values, and are shown in Figure 23. These results are consistent with the transmission line measurements. This filter is impressive for its small size and high performance. The filter used the minimum line spacing (42 microns) allowed in HDI.

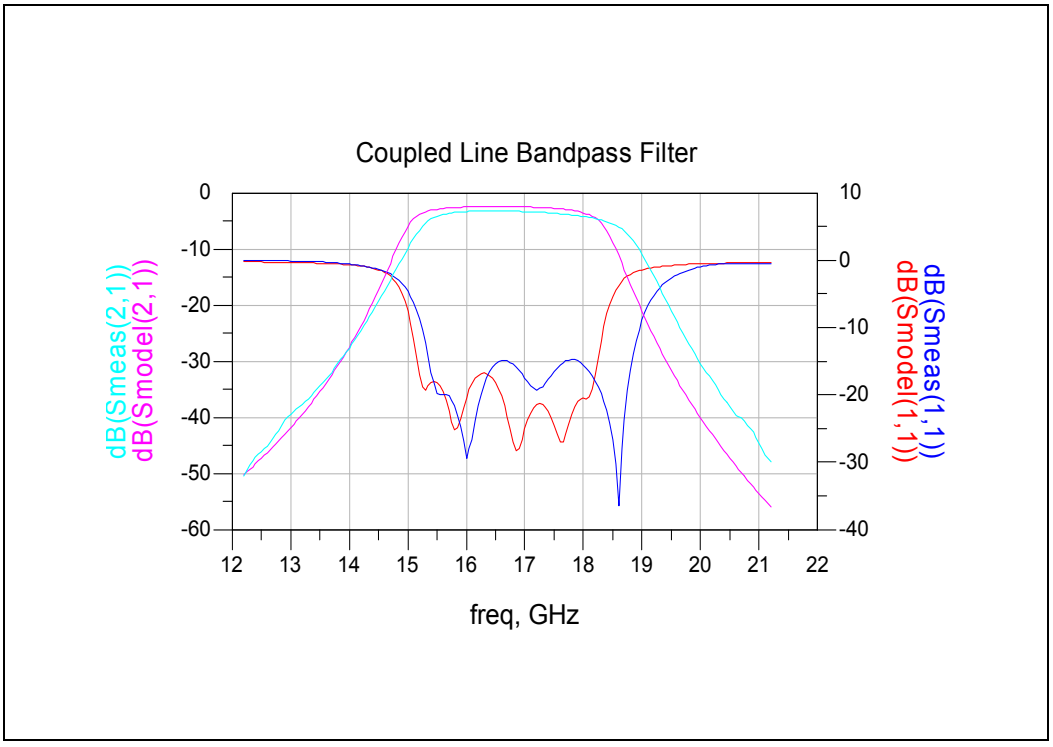

Figure 23 is a plot of Coupled line Ku-band bandpass filter measurement versus modeled data. The left axis is S21 (transmission), the right axis is S11 (input return loss).

2.4.7 Broadside Coupled Line Coupler (S7):

The broadside coupler (S7) is an X-band circuit element, which was designed and modeled using HFSS. The 3-D simulator was necessary to fully model the broadside, multilayer approach used. The coupler is woven to preserve symmetry: each arm of the coupler has half its length on MT2 and half on MT3. The thin HDI layers facilitate high coupling factors that are not practical in single-layer, edge-coupled designs. The direct port is about 2.8 dB down, the coupled port is 4.5 dB down, and the isolated port is 22.2 dB down. The coupler demonstrates octave bandwidth. Figure 24 shows the measured versus model data.

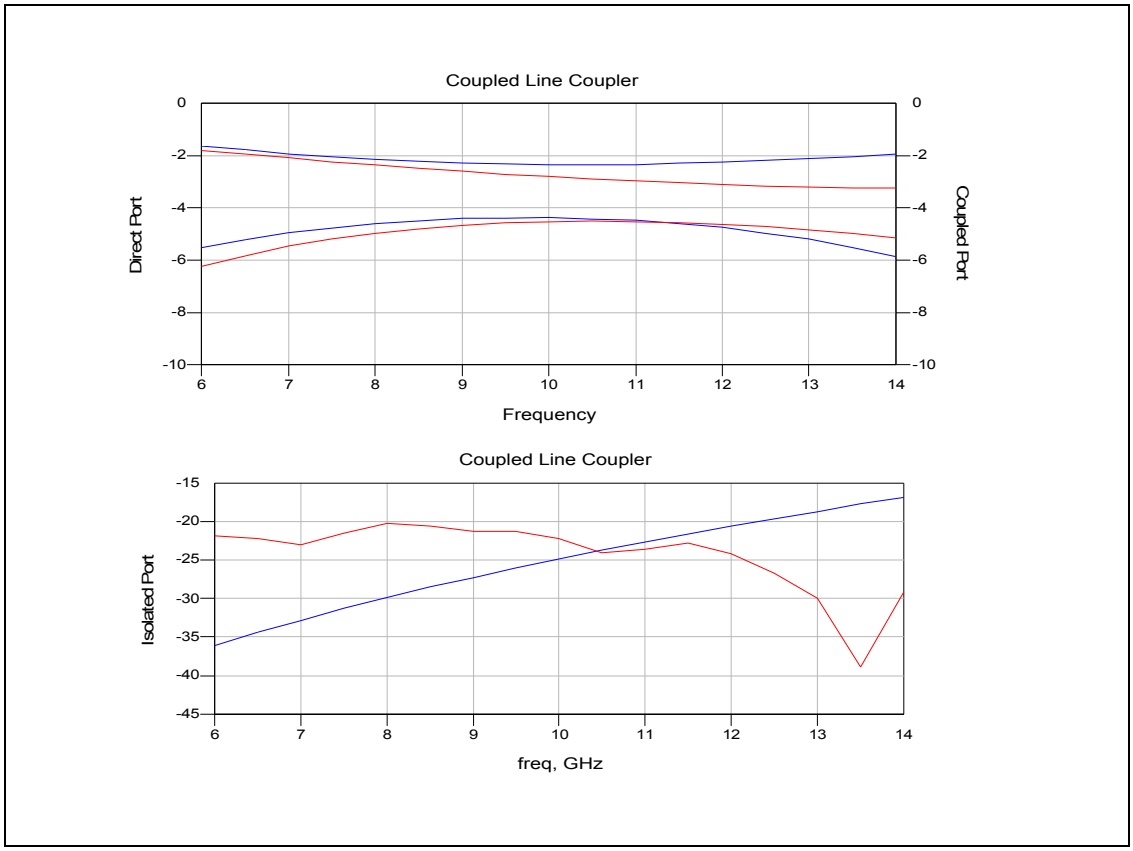

Figure 24 X-band Coupled Line Coupler (S7) measured (in RED) versus simulated (in BLUE) data. The top plot is the direct port (left y-axis) and the coupled port (right y-axis). The bottom plot is the isolated port.

2.5 Probe and test point design issues:

Several probing issues were encountered that are worth noting to improve any future module designs. Probes station capabilities and limitations should be considered during the design process. The types of probes, location of test points, number of simultaneous probes and the desired frequency response are all critical considerations. Adequate spacing between adjacent probes should be considered during initial layout. Passive structure S7 is an example of a structure where all the desired ports could not be probed at the same time: the adjacent probe was too close for the orientation of the launches. This required that the third and forth ports be

terminated with SMT resistors. SMT components are another source of potential probe interference. For example, the input port of U5 was blocked by the by-pass capacitor from U3. The capacitor had to be removed to enable testing. A probe with a higher attack angle would have possibly worked, but such a probe was not readily available.

In summary, test requirements, test point locations, and probing capabilities should be considered in the design phase. General-purpose RF probes and probes stations provide the most flexibility. Narrow pitch probes have higher frequency response and should be utilized when broadband characterization is desired. The alternative to general-purpose probing is specially configured probe assemblies, but they tend to be much more complicated, expensive, and limited.

2.6 Summary of initial design:

The use of components which are typically used in L, X and Ku-band circuits was demonstrated. A better understanding of HDI-MCOF technology and design requirements were obtained.

MMICs are designed to have air above the die. The adhesive and polyamide above the die in HDI-MCOF can change the tuning of these devices. Mis-tuned devices can have poor return loss and additional insertion losses not typical of competing technologies.

The measured loss tangent (TanD) was higher than advertised in the Lockheed Martin design guide. It caused higher insertion loss on all high frequency microwave elements. These losses were higher than most competing technologies, especially at frequencies above Ku band. The measured relative dielectric constant (Er) was lower than advertised. This is not as much of a problem as long as it is known prior to the design. A better characterization of these parameters would help designers improve overall circuit performance.

In any technology where re-work is not possible, all of the components must be produced with a high yield. At least half of the modules tested have high resistance via holes. This is not acceptable for most Sandia applications. Fortunately, the subsequent section shows that this problem did not occur in the next design. Lockheed Martin believes that the via failure problem was a one-time processing issue.

The post-processing shape of the HDI modules is another issue worth mentioning. One module was severely warped and demonstrated significant “potato chipping.” It would not have mounted into a next assembly module without causing undo mechanical stress to the module. There were also some more subtle variations among the samples and some indications of de-lamination of top layers that were not fully documented. Fortunately, the next section of this report shows that this problem was resolved in the follow-on design by including an aluminum frame in the encapsulation process.

On a positive note, we were pleased with the success of the filter and coupler. The small size and high performance achieved is impressive. Also, we were pleased and surprised

by the successful HDI packaging of the complex, delicate phase shifter MMIC. The inclusion of a phase shifter is critical if the technology is to be viable for T/R modules.

3.0 Ku-band Module Design

The module design has a transmitter and receiver (T/R) section. The center frequency is at 16.7 GHz with a bandwidth of 2 GHz and an intermediate frequency (IF) of 1 GHz. It features 4 different types of GaAs MMIC chips and a total of 11 active devices on each module. This is relatively low packing density when compared with the capabilities of the MCOF technology. Table 9 contains a complete parts list and device description. The physical size of the module is (1.2 x 1.3 x .04) inches. This is less than half the size of a chip and wire design. A picture of the module along with an AutoCAD drawing with circuit symbols is illustrated in figures 25 and 26 respectively. The design also features a pair of coupled line filters and a coupled line coupler. All these components are typical of low to medium power RF and microwave circuit design.

Circuit Symbol	Description and Part Number
U1, U3, U6, U8, U10	Hittite Switch [12], GaAs MMIC SPDT DC-20GHz, HMC347
U2, U4, U9	Hittite LNA [13], GaAs MMIC LNA 15-24 GHz, HMC262
U5, U7	Hittite Mixer[14], GaAs MMIC Double Balanced 14-23 GHz, HMC203
U11	Velocium Medium Power Amplifier [15], Monolithic HEMT, APH196C

Table 9 Ku-band Active device Parts List and description

The transmitter (Tx) section utilized an off-module, low-side local oscillator (LO) at 15.7 GHz to up convert the IF to the RF transmitter frequency. The LO was sent through a T/R switch then to the Tx mixer (U7) or Rx mixer (U5). The nominal IF input power level was specified to be -10dBm. The mixer (U7) had a nominal conversion loss of 10 dB. The signal was then directed to an LNA (U8) with a nominal linear gain of 25.1 dB and an output power of 0 dBm at compression. The signal was then filtered through a coupled line band pass filter (BPF) with a bandwidth of 2 GHz and a nominal insertion loss of 3dB. The final block included another switch (U10) with a 2.2 dB loss and a power amplifier (U11) with a nominal gain of 19.1 dB. The filter was designed with a wider bandwidth than necessary to ensure that the center frequency would pass even if the dielectric constant varied from nominal. The LNA (U8) limits the power available to the power amp and thus the overall transmitter output power and compression point. The nominal transmitter output power out is 13.7dB at the module 1dB compression point.

The receiver (Rx) section input had a switch (U1) and LNA (U2) followed by the BPF filter and another switch (U3) and LNA (U4). The signal was then sent to a coupled line coupler with the direct port feeding an off-module detector and the coupled port feeding a low side mixer (U5) (which was driven by the off-module LO through the T/R switch (U6)). The coupler was designed with a direct port loss of less than 1 dB and a coupled port loss of 15 dB. Ken Plummer (2346) defined the circuit requirements; a copy of the block diagram is shown in figure 29.

3.0 Ku-band Module Design:

The original chip and wire design (upon which the HDI module was based) utilized similar components, but the placement of the filters was different. The filter in the transmitter was placed after the mixer, which resulted in 3 dB more power at both the input and output of the power amp. The filter in the receiver was placed after the LNA providing less power to the coupler and power detector.

A total of 18 modules were processed on two different carriers. A carrier consists of a nine inch circular wafer. Nine modules were assembled on each carrier in a 3 x 3 arrangement. Sandia received 15 total modules.

A few changes in design parameters were made to this module in an attempt to improve performance relative to the first HDI module. A dielectric constant of 3.1 and a loss tangent of 0.008 were used in the design of the filter and coupler. The width of the strip line that is used to connect RF lines between shield walls (underpass) was changed from 60 microns to 48 microns (the minimum width possible). The new 48 micron line has a characteristic impedance of about 47 Ohms, which is as close to 50 Ohms as one can get in this layer geometry. (The original width was erroneously based on a lower frequency Lockheed Martin design). An aluminum frame was added for mechanical strength and to prevent de-lamination and warping of the module. Two types of aluminum frames were evaluated. The first type of frame was a shield wall structure. This frame has the same shape as the exterior wall, and has two openings that separate the transmitter and receiver sections. The frame thickness was about the same as the thickness of the die and shims. The second type of frame was a full module design, which has a continuous base with openings only around the die/shims. Pictures of these frames are shown in figure 27 and 28, respectively. A super via hole was also incorporated in the Ku-band module. The super via holes extend past the ground plane all the way down to the wall frame. This completes the electrical and mechanical connection to the wall. All normal via holes extend only to the ground plane at the metal 1 layer.

Gregg Wouters (1751) and George Sloan (2345) designed the module, and Al Sun of Lockheed Martin provided the final design review/approval.

3.0 Ku-band Module Design:

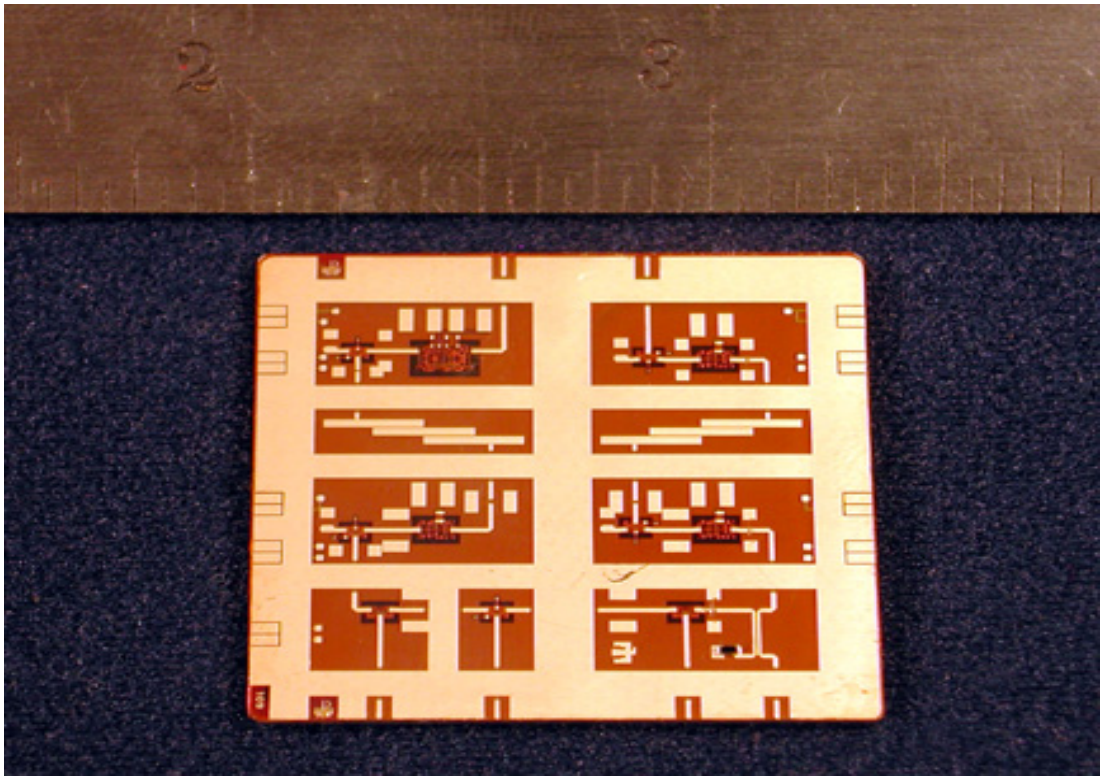

Figure 25 Ku-Band Transmitter Receiver Module (top view)

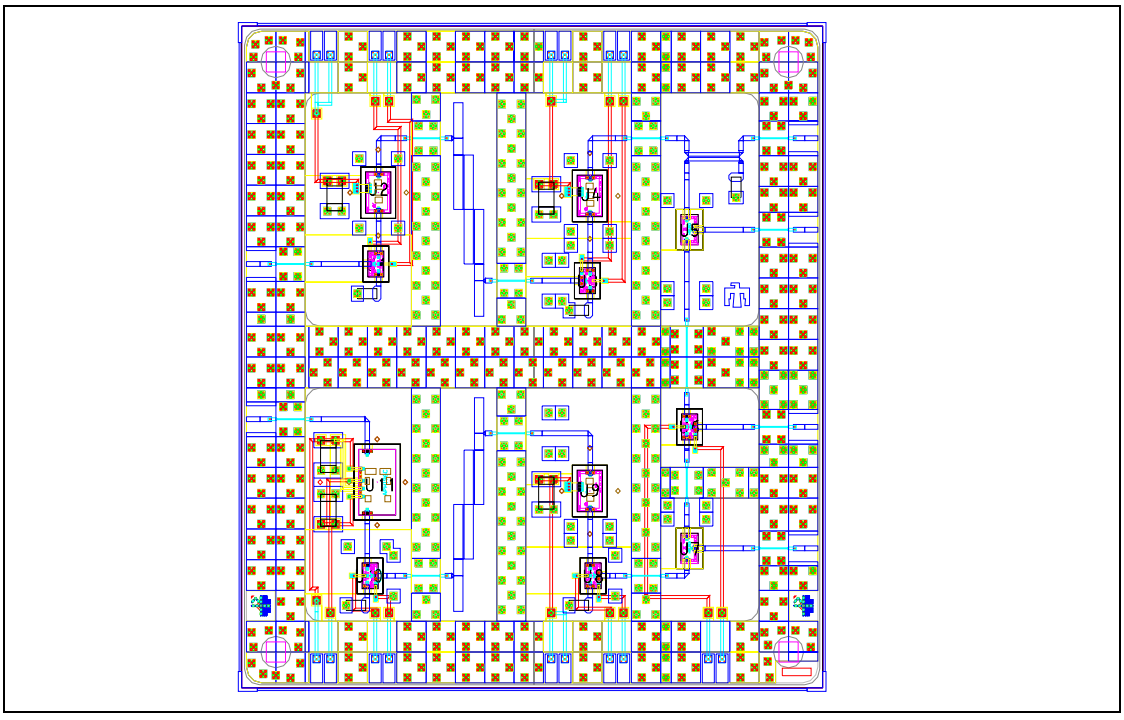

Figure 26 AutoCAD drawing of Ku-Band Module

3.0 Ku-band Module Design:

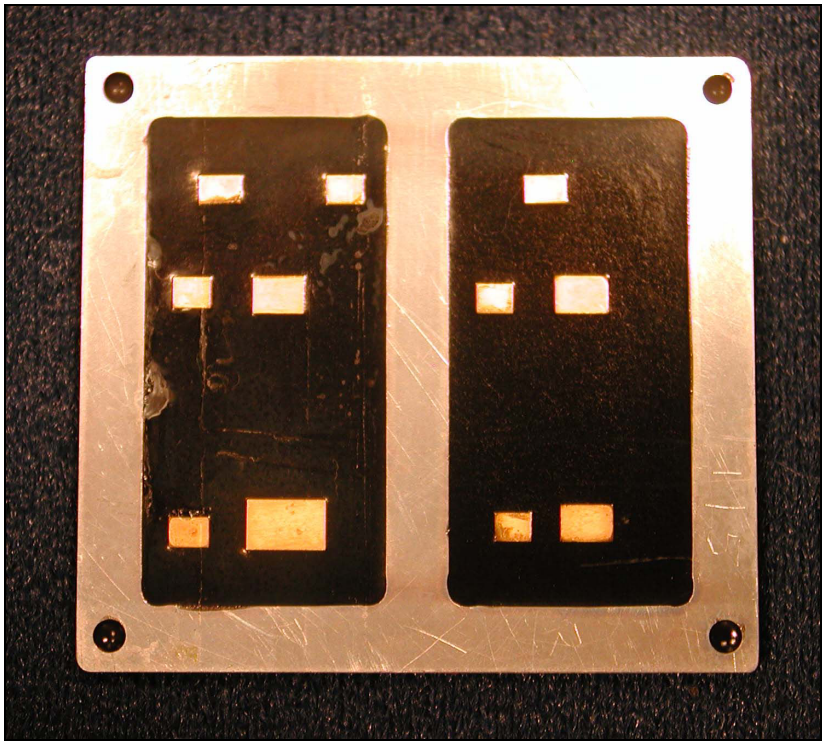

Figure 27 Ku-band Module bottom view showing the aluminum shield frame

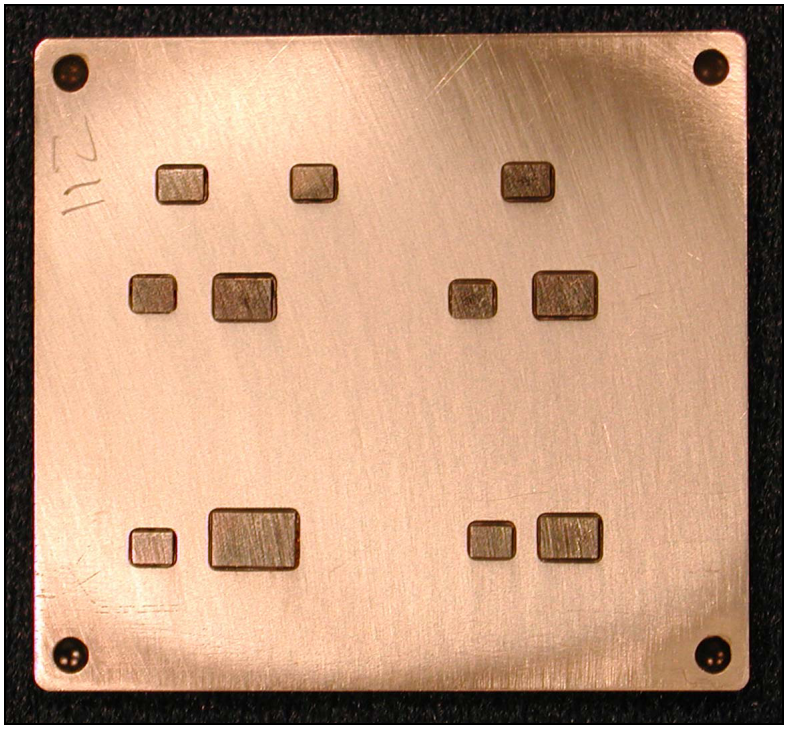

Figure 28 Ku-band Module bottom view showing the full wall design

3.0 Ku-band Module Design:

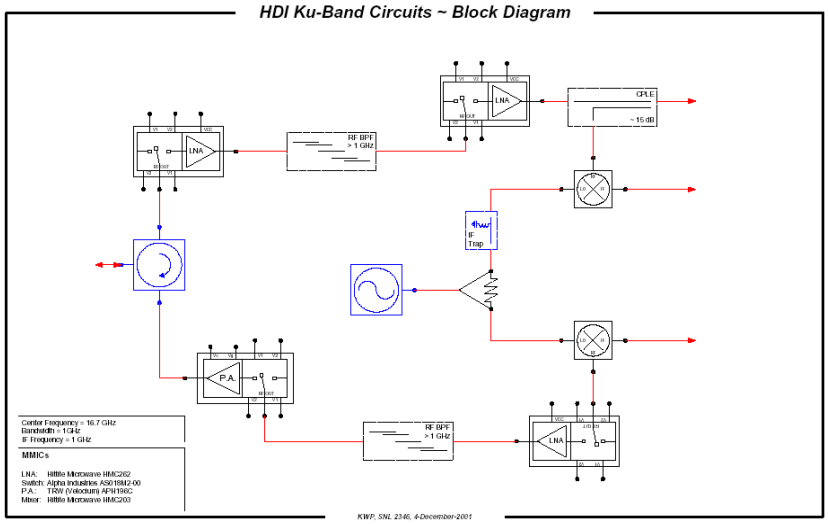

Figure 29 Ku-band Block Diagram

3.1 Test Matrix

During the fabrication process, LM discovered that many of the larger die were cracked. An investigation determined that the die attach material had not been uniformly applied during the die/shim assembly process at Sandia. This error, which did not occur in the first module, resulted in voids under the corners of many of the die. The subsequent processing steps resulted in the cracking of many of these "hanging corners". One possibility is that adhesive or molding compound flowed under the exposed corners and cracked the die due to differences in thermal expansion coefficients. The end result is that only four modules passed complete visual inspection by Lockheed Martin. All of the surviving modules had the full module frame design. It is presumed that the full module frame design prevented the flow of adhesive or molding compound under the die, or was rigid enough to prevent subsequent processing stress from cracking the die.

The Sandia drawings were done manually in AutoCAD, since we did not have access to an intelligent layout package, such as the Mentor system recommended by LM. Thus, the final continuity check of the drawing was manual. A design error occurred on the control lines to the local oscillator T/R switch. An error in the AutoCAD drawing did not properly isolate the lines from the ground layer (metal 1) as they passed through to higher layers. On one module these lines were manually isolated and the switch function was verified.

It was not possible to comprehensively test all modules due to budget and schedule (late delivery) constraints. Instead the modules were sorted and evaluated based on the locations of cracked die. Partially defective modules were tested and used to develop assembly procedures for the pristine full wall modules. Modules 101 and 104 were evaluated for transmitter performance. Modules 111 and 114 were tested for receiver performance, while modules 108 and 109 had bad die in both sections so only the embedded passive filters and couplers were tested. Module 107 was tested for both transmitter and receiver functionality. However the transmitter had an RF short at the

3.1 Test Matrix

switch (U10). The RF short appeared to be a single point failure and not representative of a design flaw. An additional pristine full wall module 103 was tested to verify this fact. Module 107 was also used for additional testing of the filter and coupler. (We determined that the initial results from modules 108 and 109 were corrupted by a faulty probe termination.) A single point system ground was accomplished by mounting all modules to a 1/8-inch thick copper plate prior to testing. A complete test matrix is shown in table 10.

Module #	Frame type	Section tested	Functional Rx	Functional TX
101	Shield Wall	Transmitter	N/A	Yes
103	Full Wall	Transmitter	N/A	Yes
104	Shield Wall	Transmitter	N/A	Yes
107	Full Wall	Transmitter/Receiver	Yes	No
107	Full Wall	Filters/couplers	N/A	N/A
108	Shield Wall	Filters/couplers	N/A	N/A
109	Shield Wall	Filters/couplers	N/A	N/A
111	Shield Wall	Receiver	Yes	N/A
114	Shield Wall	Receiver	Yes	N/A

Table 10 Ku-Band Module Test Matrix

3.2 Transmitter Test Results:

The results indicate that the HDI implementation compares well to the chip and wire version. HDI has almost the same output power when the placement of the band pass filter is accounted for. Both designs demonstrated less than nominal gain/power for different reasons. The HDI design suffered gain degradation due to mismatch losses caused by parasitic dielectric loading. The chip and wire version had problems due to transmission loss caused by interconnect bond wires of excessive length. Both problems appear to have roughly the same effect when compared directly. Also, it appears that the full wall version has lower power and less gain. The cause of this is not known without additional testing and analysis. The results presented in table 11 compare the HDI and chip and wire designs as well as the nominal (expected) HDI block values.

Module #	Frame type	Pout at P1dB	Small Signal Gain	Lo Power
101	Shield Wall	12.7 dBm	23.8 dB	11.3 dBm
104	Shield Wall	10.1 dBm	21.2 dB	11.3 dBm
103	Full Wall	8.0 dBm	19.2 dB	12.0 dBm
Nominal HDI Block	N/A	13.7 dBm	26.2 dB	N/A
Chip & Wire (B2 w/caps)	N/A	16.4 dBm *	20.0 dB	N/A

Table 11 Transmitter Test Results

* The placement of the band pass filter was before the LNA provides 3 dB more power in compression than in the MCOF-HDI design.

3.3 Receiver Test Results:

Table 12 below compares the HDI module with a chip and wire design and a nominal functional block. The gain for the HDI module is less than nominal by as much as 10 dB. Individual chips/subcircuits were isolated in order to determine the cause of the reduced gain. The cause was determined to be the LNA. It appears that the LNA is sensitive to the parasitic loading caused by the kapton layers over the die. The loading causes significant match degradation at both the input and output ports. The mismatch loss was calculated to be about 5 dB per LNA. This accounts for the difference in small signal gain and is likely the cause of the reduced transmitter gain as well.

Module #	Frame type	Pout at P1dB	Small Signal Gain	Lo Power
111	Shield Wall	-27.0 dBm	7.2 dB	12.2 dBm
114	Shield Wall	-30 dBm	1.5 dB	12.2 dBm
107	Full Wall	-28.3 dBm	8.0 dB	12.2 dBm
Nominal HDI Block	N/A	-28 dBm	17.0 dB	N/A
Chip & Wire (B3 wo/caps)	N/A	-26.7 dBm	1.3 dB	N/A

Table 12 Receiver Test Results

Figure 30 illustrates the receiver gain response using a constant LO frequency of 15.7 GHz. The overall bandwidth is about 0.6 GHz (module 114).

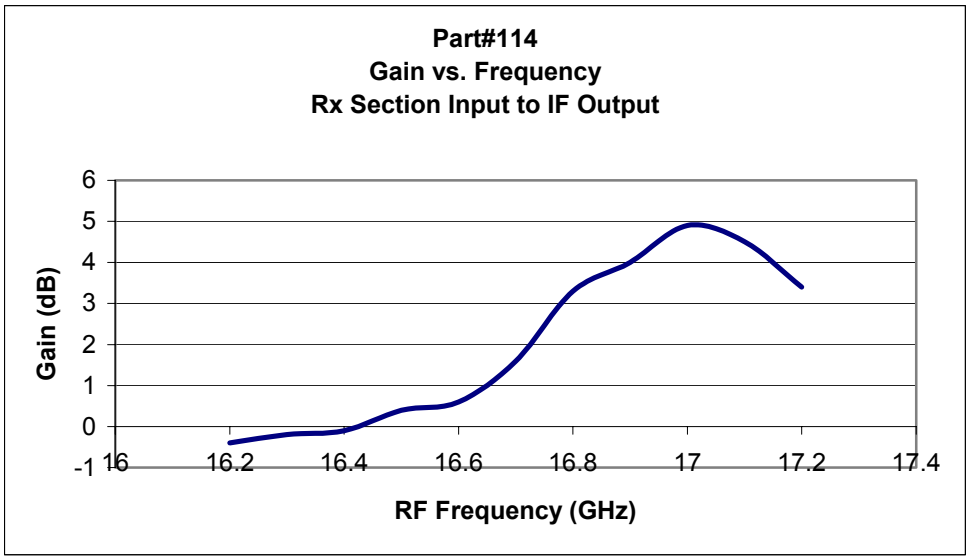

Figure 30 Plot of Gain versus frequency with a fixed LO frequency (15.7 GHz)

3.4 Coupled Line Bandpass Filter Test Results:

Table 13 summarizes the results for Tx/Rx insertion loss, Tx/Rx return loss, and filter bandwidth measurements. The data shows good consistency between the few modules measured.

Module #	Filter section	Insertion Loss	Return Loss	Bandwidth
107	Receiver	2.8	>12dB	15.7 – 18.1 GHz
108	Receiver	3.0	>10dB	15.6 – 18.1 GHz
108	Transmit	3.1	>10 dB	15.6 – 18.0 GHz
109	Receiver	3.2	>10 dB	15.6 – 18.0 GHz
109	Transmit	3.0	>10 dB	15.7 – 18.1 GHz

Table 13 Band Pass Filter at center frequency of 16.7 GHz

Figure 31 compares the measured and simulated data for the edge-coupled filter design (module 107). The comparison shows good agreement except for a slight skew at the upper band edge of about 0.4 GHz. The simulation assumed a relative dielectric constant of 3.1. Measured data from the first and second HDI designs show that the actual value is probably closer to 3.0. The filter data confirms the dielectric measurements of the initial design and demonstrates that the HDI glue/layering process appears to be repeatable.

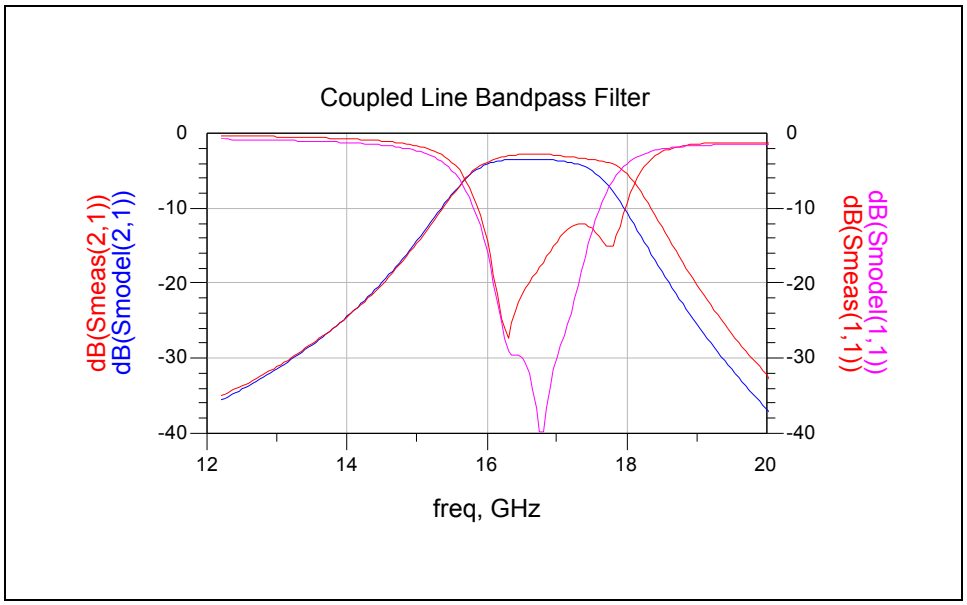

Figure 31 Coupled Line Band Pass Filter showing measured (in red) versus modeled data (in blue).

3.5 Coupled Line Coupler:

The direct path S21 and S11 measurements for the microstrip coupler are shown in figure 32. The insertion loss measurement shows excellent agreement with the model prediction. The measured return loss was a few dB above the predicted value. We suspect the measurement was degraded by nonideal probe effects and terminations. Also, the measurements included the stripline underpasses used at both the input and output ports of the direct path. (As previously mentioned, these stripline sections have a slightly low characteristic impedance (47 Ohms), which could degrade the overall return loss). The measurements in figure 33 show the corresponding coupled path response. The insertion loss is close to the desired 15 dB, but the return loss is somewhat less ideal than predicted (but still very acceptable).

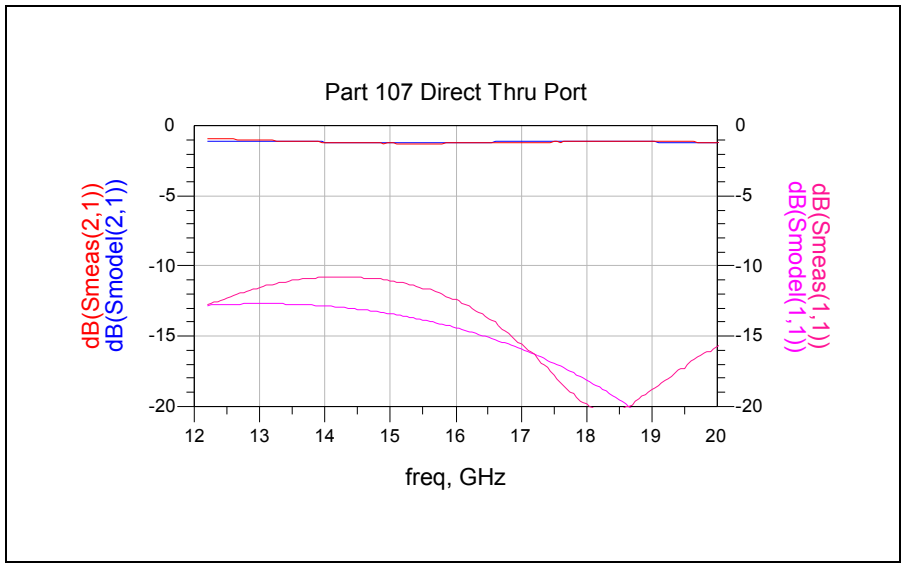

Figure 32 Direct Port insertion loss(left axis) and return loss (right), measured (in red) versus modeled (in blue)

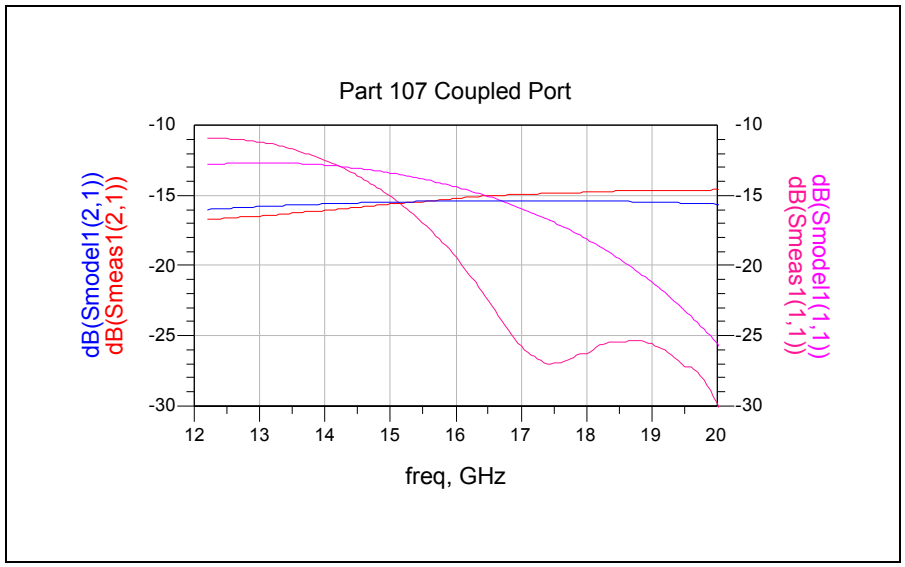

Figure 33 Coupled port insertion loss (left axis) and return loss (right axis), measured (in red) versus modeled (in blue)

4.0 Final Conclusions:

The design of components used at L, X and Ku bands was successfully demonstrated using the HDI-MCOF technology. The design team developed a much better understanding of the complex manufacturing process and technology issues involved in HDI packaging. The technology is well suited for die interconnection as well as supporting microwave structures, including couplers (both edge and broadside), filters, and combiners. A variety of different transmission lines can be implemented in HDI that are free of resonance, and maintain a controlled impedance through multiple circuit board levels. Shield walls and isolated cavities are easy to design-in; however their shielding effectiveness was not fully verified by this effort.. The prototype modules proved that it is possible to design in test points between functional circuits without reducing performance. We demonstrated that given good material parameters, circuit models were effective in predicting circuit performance.

The second module showed that the use of aluminum frames and super vias were successful in eliminating the via failure and de-lamination problems encountered in the initial module. The frames also prevented the warpage seen in the first design. The success of the full module frame also demonstrated that the glue thickness was adequate to prevent any metal zero control lines from shorting out on the frame. Unfortunately, the second module also taught us that die cracking can occur if the die/shim attachment process is not adequate. However, the problem of the "hanging corners" can be easily avoided by ensuring a uniform full paste coverage of the die backside during attachment.

Both the first and second modules taught us that some microwave MMICs are adversely affected by having material directly above them (dielectric loading instead of air). The adhesive, polyamide, and via hole metalization above the die faces appears to detune the input and output impedances of some active devices. Mistuned devices and the resulting circuit mismatches can produce overall gain and bandwidth reductions not found in competing technologies. This phenomenon was observed on the LNAs used in both designs and the TQS Switch of the initial design.

Another problem concerned the use of stripline architectures. For typical layer profiles, the use of stripline is limited by the fact that the design rules will not allow a true 50 Ohm line. As stated, stripline is useful to create ground wall underpasses to connect separate cavities. The initial underpass design copied from LM was 60 microns wide yielding a 41 Ohm line. The subsequent Sandia design was 48 microns wide yielding a 47 Ohm line. Ideally, a 42 micron line is desired; hence, the availability of finer metal resolutions on interior layers would be useful.

The thin film metal system permits fine line patterns and spacing on the order of 48 micron lines with 42-micron gaps. HDI is capable of producing precise RF and microwave structures. Thus, in addition to full modules, HDI could be used to produce leadless piece parts such as transmission lines, tuning structures, filters, couplers and combiners, etc. These structures could be singulated and used as components in other multichip module technologies.

4.0 Final Conclusions:

HDI-MCOF has the potential to produce an extreme level of miniaturization with high chip density and good electrical/mechanical performance. At this point, the primary concerns are parasitic electrical effects and the immaturity of the manufacturing process. The process Sandia evaluated is still undergoing changes and does not appear to be supported by a high volume customer base, which would help to perfect procedures. The result is that significant changes are and tweaks are still being evaluated. This leads to reliability concerns that have not stood the test of time or volume production. Additional expenses and development time in this area may be necessary to address these concerns. Both Sandia designs had some MMICs, which demonstrated undesirable parasitic effects, manifested as bandwidth and impedance degradations. We believe this could be overcome with careful layout and additional analysis, but this would require significant expense and has some risk. For example, all new die not previously used in the MCOF process should be evaluated on a special coupon. The coupon would be used to assess the adverse electrical effects of the adhesive and interconnect system above the die prior to final module design.

Perhaps the most striking feature of HDI is that it yields an ultra thin flat package that offers die protection and surface mount compatibility. Thus, this technology would be well suited for applications that would especially benefit from a thin profile. Two obvious applications would be covert tags and communication devices. The technology would also be useful to produce ultra-miniature drop in subcircuits that are part of more traditional interconnect technologies. The knowledge gained from this evaluation effort gives us an effective template on which to base future designs.

It is the authors' opinion that several design iterations would be necessary to produce high performance, fieldable modules. As of 2002, the cost for a prototype run (two carriers) is on the order of $60K, which is on the high end when compared to competing technologies. Nevertheless, at present, HDI offers the ultimate in miniaturization. For the right application, it is a very attractive technology. Lastly, the authors' wish to note that the original LDRD plan had hoped to include some advanced Sandia devices, such as RF MEMs switches or GaN amplifiers. Unfortunately, no such devices became available in time for inclusion in the last module. However, we have learned that GE did recently demonstrate the inclusion of an RF MEMs switch in an HDI module, and is continuing to pursue the concept.

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