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Micromachined VLSI 3D Electronics

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Micromachined VLSI 3D Electronics 1
U.S DEPARTMENT OF ENERGY I 1
Micromachined VLSI 3D Electronics 2
Phase I Summary. 2
Introduction. 4
Silicon Through Wafer Via Fabrication. 4
Via wall isolation. 9
Contact Formation 12
Testing 19
Conclusions 19

Phase I Summary.

The phase I program investigated the construction of electronic interconnections through the thickness of a silicon wafer. The novel aspects of the technology are that the length to width ratio of the channels are as high as 100:1 so that the minimum amount of real estate is used for contact area. Constructing a large array of these through wafer interconnections will enable two circuit die to be coupled on opposite sides of a silicon circuit board providing a high speed connection between the two.

NanoSciences' patented high aspect ratio silicon etch process was used to prepare the silicon substrate containing the through wafer vias. Modifications to the process were attempted to develop a process by which individual channels can be created at predetermined locations on the wafer surface. In addition to the standard process, a variation utilizing an electrode was tried. The position of a via is then determined by the position of the electrode on the surface. The electrode was used to electrochemically machine vias through the wafer.

Both electroless plating and traditional electroplating were used to build the through wafer metallization. Ni was the material of choice for the preliminary work since electrodeposition of nickel is extremely well understood. Each process, electroless plating and electroplating, has distinct benefits depending on the final application for the through wafer via.

The difficulties encountered during the program included isolating the through wafer metallization from the wafer substrate without distorting the wafer, obtaining uniform deposits along the entire length of the via and preventing voids from forming in solid metal deposits. Despite these difficulties, however, the program was successful in demonstrating that through wafer vias can be produced reliably at predetermined locations on a wafer surface. Further refinement the processes developed during the program during phase II will demonstrate the commercial viability of the silicon circuit board technology.

The potential commercial significance of the program is that the construction of circuit boards based on silicon will take the revolution in system miniaturization to a new level. Chip scale packaging concerns over thermal expansion mismatch between the circuit board and the die will no longer be a problem that restricts die attachment to large contact pads. Overall system performance will improve as the signal delays between die and the real estate consumed for contact structures will be reduced. More features will be enabled in handheld devices that will usher in a new era of communication appliances for everyday use.

Introduction.

The Phase I project investigated the construction of through wafer vias so that electronic systems could be built on a silicon wafer circuit board very much as they are presently constructed on printed circuit boards. The silicon circuit board is attractive for several reasons: (1) chip scale packaging can be leveraged to the fullest extent as the thermal expansion mismatch between the circuit board and the active die is eliminated, (2) smaller contact pads may be used, reducing the amount of real estate required for contacts on circuit die and, hence, lowering circuit cost, (3) opens the possibility of integrating passive components such as resistors, capacitors, inductors and low performance active circuitry onto the circuit board directly, lowering system assembly costs while simultaneously improving reliability, (4) improve overall system performance by reducing signal delays through reduction of signal line length, inductance and capacitance. The vias are created using NanoSciences' patented electrochemical etch process for micromachining high aspect ratio channels through a silicon wafer. Systems built using the micromachining technique can be used to construct 3D VLSI electronic systems.

Several unique challenges were confronted during the course of the program. The first was the creation of channels precisely where needed in order to bond two die together. NanoSciences is expert in the creation of high aspect ratio structures in silicon to build microchannel plate electron multipliers, but creating a circuit board requires that only a few channels are placed precisely where needed. Modifications of the standard etch process were employed during the program. An electrochemical machining technique was also explored.

Electrical isolation and metalization of the vias also presented challenges due to both size and materials issues. In order to pass signals through the wafer the signal embedded in the via must be electrically isolated from the surrounding silicon substrate. The creation of the signal line itself can be accomplished by a variety of deposition techniques, each having performance or manufacturing advantages.

Testing the electrical performance of the through wafer structures was complicated by the small size of the vias and their close proximity to each other. Contact structures were built over groups of vias for electrical performance testing to determine whether any major failure modes exist. Overall, the evaluation of performance carried out during phase I indicated that the isolation between groups of vias and the conductivity through the vias are adequate for silicon circuit board applications and should be further developed during a phase II program.

The next sections contain detailed descriptions of the work carried out during the program.

Silicon Through Wafer Via Fabrication.

The first program task was to build the silicon through wafer vias. NanoSciences' standard high aspect ratio etching process was used to etch <100> oriented silicon wafers up to 400 μm deep. A typical cross-section for an etched wafer is shown in Figure 1.

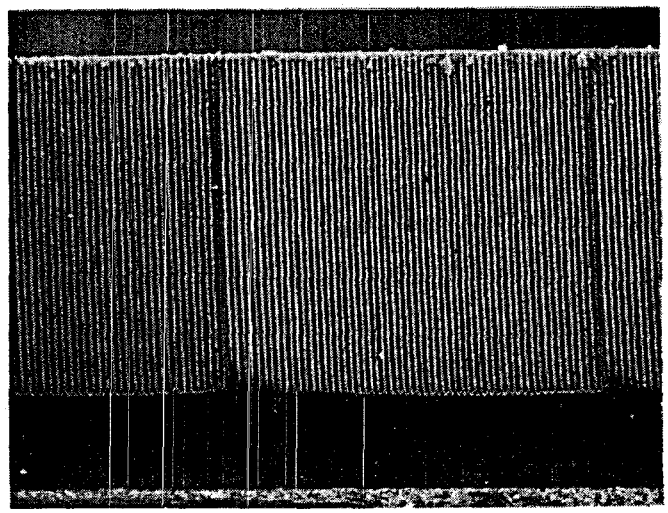

Figure 1. Typical cross-section for a silicon wafer etched using NanoSystems' high aspect ratio silicon etch process. The channels are ~400 μm deep, and are 7 μm wide on 8 μm centers.

While this process has been used to build microchannel plate electron multipliers, silicon circuit board applications would be better served with a substrate containing only a few vias through which signal lines can be built. Attempts were made to modify NanoSciences's standard etch process to allow only a select number of vias to be created. Figure 2 shows a SEM photo depicting results of using the standard etch process to create isolated channels. Silicon nitride is used as the masking material. Lateral etching is apparent at the periphery of the patterned area. An analysis of the cross-section of this structure shows that the channel depth is only 20 μm. This indicates that the process will create lateral channels at about the same rate as vertical channels and is unsuitable for building silicon circuit boards.

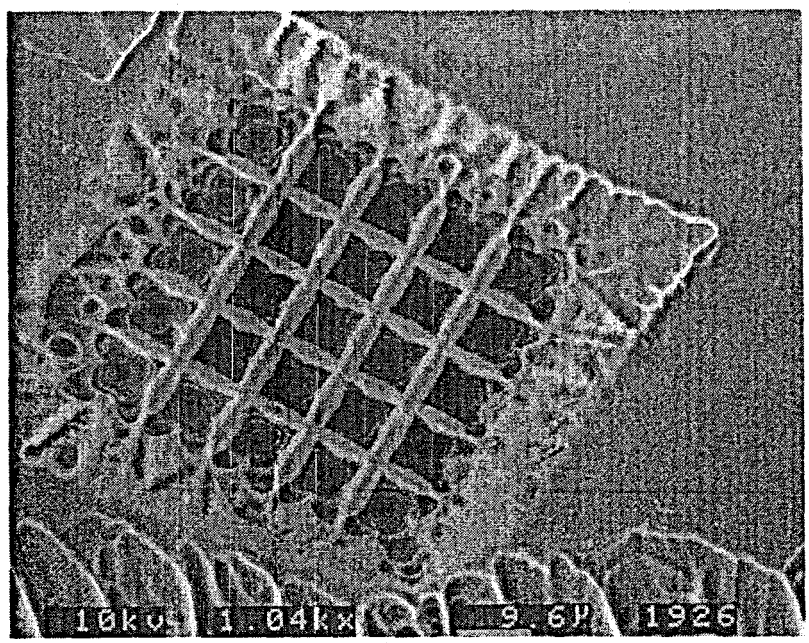

Figure 2. SEM photo showing isolated channel etching using NanoSciences' present high aspect ratio process. Note the lateral etching along the periphery of the patterned region.

Modest attempts were made to modify the process to achieve isolated channel etching. Process modifications included using isolated contact structures to restrict current to the etching area and variations of the masking scheme were used to accomplish as similar goal. The conclusion drawn from this work is that in order to create isolated channels a new approach to the process must be taken that would entail a new research effort.

The use of NanoSciences' present electrochemical process to build silicon circuit boards has the advantage of being able to create features across the entire wafer simultaneously. The difficulties encountered, however, led us to try to create isolated vias using an alternate electrochemical machining technique. In this process a single wire electrode is used to "drill" a via at a chosen spot on the wafer. The size of the wire electrode will, in part, determine the width of the via. A schematic of the apparatus used is shown in Figure 3.

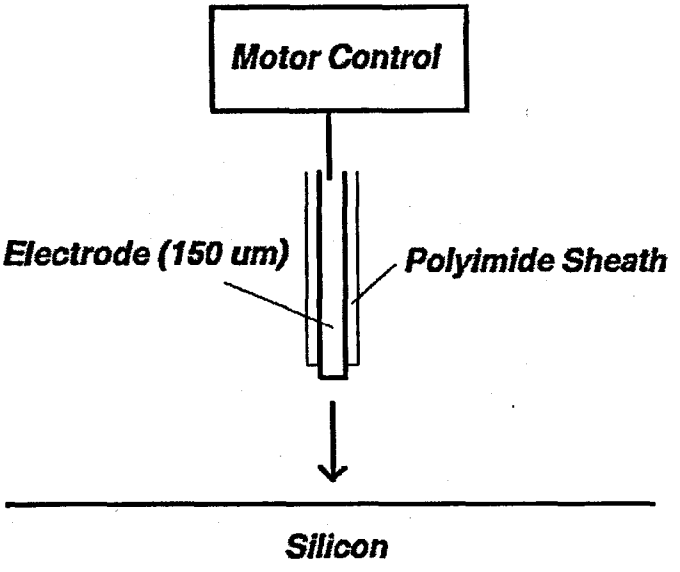

Figure 3. Schematic of the apparatus used to electrochemically machine vias through a silicon wafer.

A Stainless steel wire 100 μm in diameter was used as the machining electrode. The wire was coated with polyimide to suppress etching everywhere along it length except at the tip. A high precision position controller was used to lower the electrode toward the surface of the silicon wafer. The electrolyte was flowed over the wafer surface, contacting both the electrode and the wafer. When current is passed through the cell comprising the wafer, electrolyte and electrode, etching proceeds in the location of the electrode. Examples of vias created using this method is shown in Figure 4.

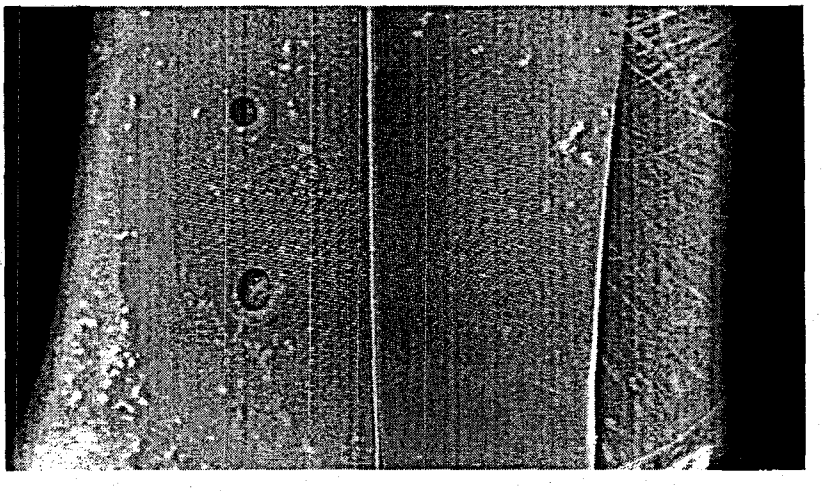

Figure 4. A pair of vias created by the electrochemical machining process in the center of a 100 mm silicon wafer.

The vias were created by passing a fixed current through the electrode and keeping it constant for the duration of the etch. The speed of the motor lowering the electrode was coordinated with the current so that the electrode would not crash into the silicon substrate. A dozen vias were created with this technique. Typically, 50 μA of current were used with a complete via being created in about 4 hours for a 450 μm thick wafer.

Only bare silicon wafers used in the electrochemical machining experiments so that the surface was unprotected. The lack of a mask accounts for the outer rings that can be seen on the surface that are actually an etch pit created before the electrode penetrated the surface plane. The use of a silicon nitride mask to define the locations of the vias will prevent the surface from becoming pitted.

Although we were successful in creating through wafer vias utilizing electrochemical machining, there are several drawbacks to the process that may prevent it from becoming a significant contributor to silicon circuit board manufacture.

First, building a circuit board will require the construction of a complicated electrode. Although the number of vias used in a silicon circuit board will be small compared to the millions of channels in a microchannel plate, it would not be unreasonable to expect that several thousand vias could be required to build systems with complex processors and ASICs. The construction of such an electrode will be expensive because the electrodes themselves must be made of fine wire and ultimately have a high aspect ratio. This introduces the second problem – the real esate occupied by the electrochemically machined vias is extremely large. The via created by the 150 μm wire is shown more closely in Figure 5.

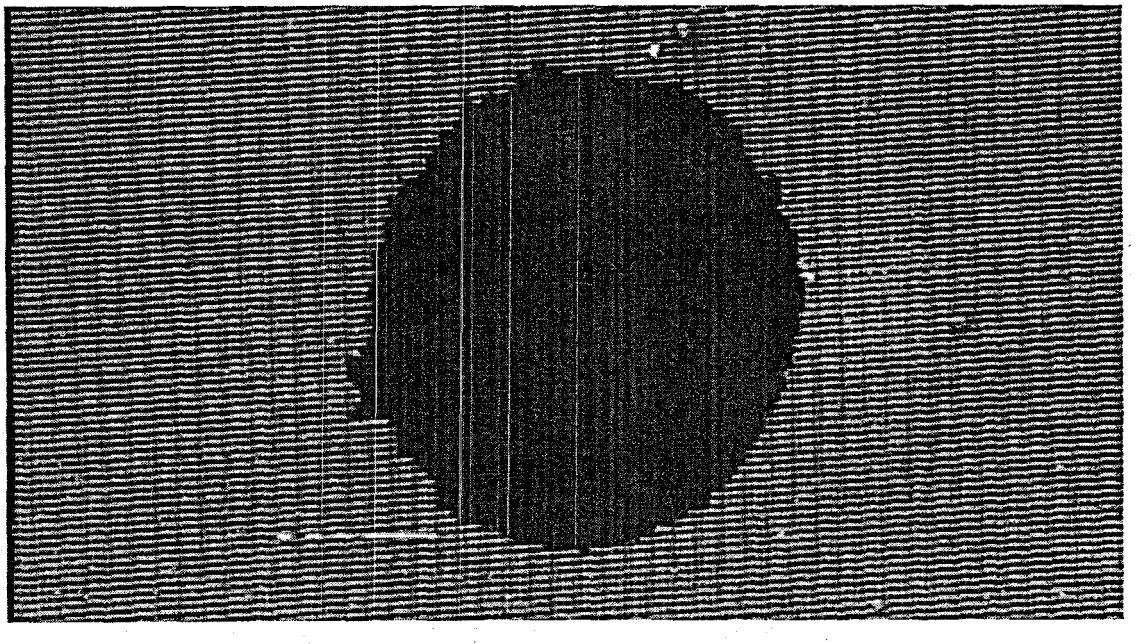

Figure 5. Close-up view of the electrochemically machined silicon through wafer via.

The width of the via is ~500 μm, about three times the width of the wire electrode used. Large area vias, however, will not allow one of the main advantages of the proposed technology to be

exploited – direct die attachment to the silicon circuit board – since the contact pads on integrated circuits are typically separated by less than 100 μm.

The extra width is necessary so that the wire may be plunged down into the wafer, the hydrogen gas created at the electrode can escape and fresh electrolyte can get down into the channel being drilled. Unfortunately, this means that the electrode width will need to be about 10 μm in order to create vias 30 μm in diameter. Producing such an electrode will be difficult as it needs to be ~500 μm in length for use with 100 mm wafers and over 800 μm long when used with 200 mm wafers. Wire structures with this high aspect ratio are difficult to build as the motion of the electrolyte alone can cause them to bend.

For these reasons, the electrochemical machining process is not being considered for further development for silicon circuit board applications.

Via wall isolation.

In order to proceed with the program microchannel plate template structures were used to build through wafer vias. Once an array of silicon channels is etched to a depth of 400 μm, the silicon on the backside of the wafer is removed using grinding and polishing processes. The details of the process are proprietary, but the surfaces remaining after the treatment are flat and free of scratches and debris.

The isolation of the silicon substrate from the signal lines can be accomplished in several ways. The simplest and most cost effective is to use thermal oxidation to grow an isolation oxide on the channel walls. Microchannel template structures were placed in an oxidation furnace in flowing dry oxygen for up to six hours to grow the isolation oxide. When removed from the furnace, the parts had a characteristic color change representative of the oxide thickness grown. Typically, the pieces are oxidized for four hours in dry oxygen resulting in an oxide layer ~2000 A thick as measured using a dektak profilometer on a bare wafer included in the oxidation run.

Using thermal oxidation for isolation was thought to be advantageous for several reasons. First, the process is simple, requiring only an oxidation furnace and an oxygen supply. Second, the process is amenable to batch processing as many wafers or substrates can be oxidized in the same furnace at the same time.

The drawback to thermal oxidation, however, lies in the mechanical deformation of the wafer when a three dimensional structure is oxidized. As silicon oxidizes it absorbs oxygen atoms from the ambient gas in the furnace. The absorption of the atoms results in a volume expansion of the surfaces within a channel or via. The expansion causes stresses in the surrounding wafer that is large enough, very thick oxide layer, can cause mechanical failure of the wafer. The stresses are particularly large in isolated vias. The stress causes mechanical deformation of the wafer surface around the via that can be observed by looking at the via with the naked eye.

The stress and deformation of the surface created by the thermal oxidation process precludes thermal oxidation from being a viable means of electrically isolating vias in a silicon circuit

board technology. As will be seen shortly, however, thermal oxidation was the only cost effective means available to build via structures to complete the program tasks.

A second approach attempted for isolating the channel walls used spin-on glass. Spin-on glass materials are widely used in the semiconductor business for providing isolation between metallization layers on integrated circuits and for planarizing the surfaces of circuits. The materials are low cost and flow easily. The ease of application of the material warranted investigation of it as a low cost, simple technique to provide isolation to the channel walls.

Several pieces of microchannel plate substrate were immersed in a solution of spin-on glass and isopropanol in an ultrasonic bath. The ultrasonic treatment was thought to be necessary to insure that the spin-on glass mixture completely penetrated the channels of the matrix. After filling the channels with spin-on glass, the samples were cured at 80°C on a hot plate to remove most of the solvent from the glass mixture. Higher temperature treatments were then performed to densify the glass.

Initial results with the material showed that the amount of material contained within the channels was too great to build a thin uniform layer on the surface. This is a common problem with spin-on glass materials in that there is an optimal thickness to the layers before they crack. The spin-on glass was then mixed in a 1:10 ratio with isopropanol to reduce the total amount of material in the channels so that the optimal glass thickness would be achieved after all of the solvent has been removed during the glass baking procedure.

Even after the spin-on glass concentration was reduced, problems still persisted in coating the channel walls. The cause has been traced primarily to the solvent escaping from the center of the channels and the formation of glass particles across the channel instead of solely on the channel wall surfaces. An SEM photo of one attempt with a 1:10 solution is shown in Figure 6. It should be noted that the thinned solution appears to form clumps after the heat treatment series leading to a discontinuous layer. The photo shows that only nodules of glass appear to have formed.

A superior method of isolating the silicon substrate is to use chemical vapor deposition to coat the channel walls with either silicon nitride or silicon dioxide. In particular, low pressure chemical vapor deposition (LPCVD) is ideally suited to coating the high aspect ratio vias. NanoSciences has developed a LPCVD process for applying multiple layers on the walls of the high aspect ratio channels used in its silicon microchannel plates and has used this know-how to coat structures for through wafer vias.

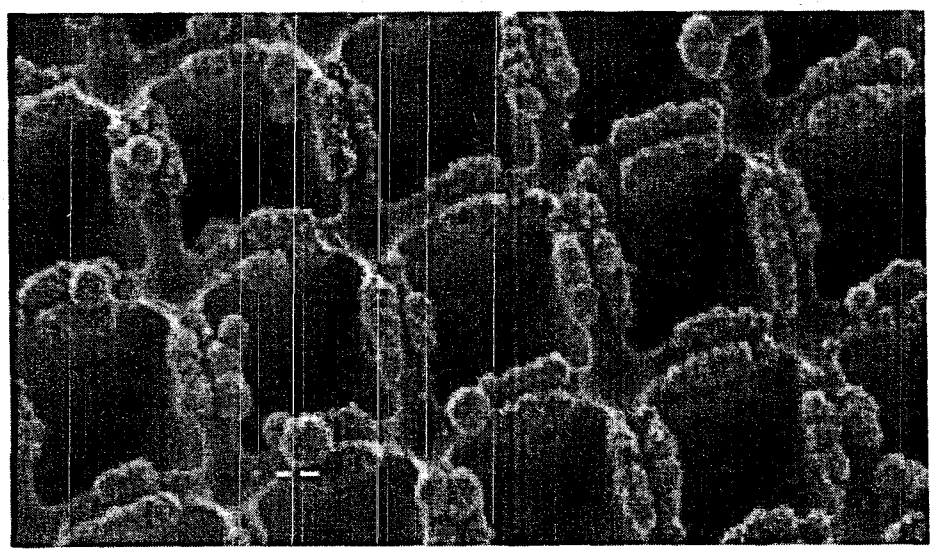

Figure 6. SEM photo of the surface of a wafer using spin-on glass as an isolation layer. Note the nonuniform coverage and beading of the glass on the surface.

NanoSciences' prowess at this deposition process is shown in the SEM pictures of Figure 7 where a bilayer of silicon dioxide and silicon nitride has been deposited on the walls of a silicon microchannel plate. The left hand panel shows that the process is able to apply a conformal coating over the tops of the channel walls as well as along the entire length of the channel.

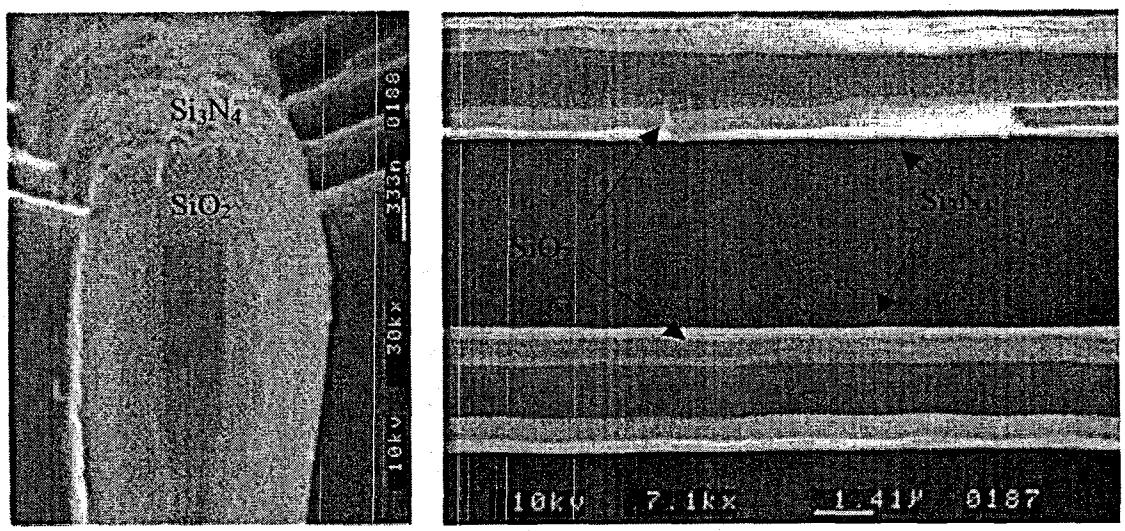

Figure 7. Scanning electron micrograph of uniform Si_3N_4 and SiO_2 layers on the walls of a silicon channel plate. The thickness of the layer is uniform along the entire length of the 340 µm channels.

The process used to grow the layers shown in Figure 7 flows the reactant gases through a tube furnace at a combined pressure of 60-70 mTorr. Silicon nitride is deposited using a mixture of

silane and ammonia in a ratio of ~1:3. Silicon dioxide is deposited using a mixture of silane and oxygen at a ratio of ~1:1. In both cases the flow rate of the gases is more than one liter per minute in order to insure that enough reactant travels through the tube for uniform deposition.

LPCVD is ideally suited to coating substrates for silicon circuit applications with through wafer vias. One process concern, however, is the consumption of reactants in the reactor during deposition. A substrate containing a large number of through wafer vias, such as a precursor substrate for a microchannel plate, will have an effective surface area 40 times that of a solid wafer. This means that 40 times the reactants will be required to deposit a uniform layer all of the exposed surfaces compared to that required for a solid wafer. The greater usage of reactants is in opposition to the requirements for low pressure in order to insure a uniform coating along all of the channel walls.

The situation is not as bleak for the silicon circuit boards with through wafer vias, however. Since the number of vias will likely only be tens of thousands per wafer instead of ten of millions as in the microchannel plate, the increase in the effective wafer surface area will be small and can be easily accommodated.

Contact Formation

Two methods of creating the electrical contacts through the wafer were attempted. Both electroless plating and electroplating were used to build nickel signal lines within the through wafer via. Each of these processes has advantages depending on the performance required from the via. Electroless plating is advantageous for building a via that contains a through hole in the center. The through hole may be used for soldering for die attach. Electroless plating may also have the advantage of speed. Since the entire surface of the channel walls are coated simultaneously, the metal deposition step may occur in a much shorter time than is possible by electroplating a column of metal through the thickness of the wafer.

The one area where electroplating has a distinct advantage over electroless plating is when the via must be plugged solid with metal, either for vacuum sealing or for current carrying capacity. Electroless plating will always leave voids within a solid metal plug, trapping electrolyte within the channels where electroplated metal will not.

Electroless Plating

In this project electroless nickel plating was used to coat the inside of the channel walls. The deposition conditions were varied to try to find the optimal conditions for applying a uniform coating to the walls. A commercial electroless nickel bath was purchased from Transene Corporation (Electroless Nickel Plating Ammonia Type, ENPAT). This solution is particularly formulated to provide good electrical contact to both n and p-type silicon. The primary process conditions that were adjusted were the plating time and the plating bath temperature. Variation of the plating time changes the thickness of the deposit while variation of the bath temperature will control the rate of the nickel deposition.

The electroless plating procedure was carried out by first cleaning the silicon matrix. The next steps include preparing the surface of the wafer by sensitizing and then activating. Each step was carried out by placing the wafer into a beaker containing the appropriate solution and sonicated (water temperature of sonicator same as that called for in experiment) for approximately 2 minutes and then rinsing with distilled water. The sample is then placed into the next solution for the same amount of time followed by rinsing. The last step was to place the wafer into a preheated electroless nickel bath (~90°C, unless otherwise specified) and sonicating for 1, 5 10, or 20 minutes. The temperature of the plating bath was varied to vary the deposition rate on the channel walls. Deposition was attempted in baths at 55, 75, and 85°C.

The electrical conductivity through the wafer was evaluated by attaching the plated wafer to a copper foil with silver paint. Care was taken to limit the amount of silver paint so that it did not wick through the channels of the wafer. An Ohm meter was used to measure the though wafer resistance. All samples measured as electrical shorts indicating that plated metal had made a continuous electrical path through the wafer.

SEM imaging was used to inspect the degree to which the electroless plating process was effective in depositing nickel metal on the walls of the channels. Figure 8 shows a SEM image of a typical sample cross-section showing the nickel metal plated on the channel walls. Close inspection reveals that the bright metal in the channels is in tubular form. A planar view of the substrate shows that the ends of the channels are blocked by nickel deposition, however. Further work will be required to refine the process to prevent overgrowth of the channel openings while effectively coating the walls.

Figure 8. SEM image of a cross-section showing electroless nickel deposition through the channels.

A plan view of the plated substrate is shown in Figure 9. The metal layer appears to coat the walls uniformly. The filler material in the center is polishing compound used to polish back the surface to expose the layer structure on the walls.

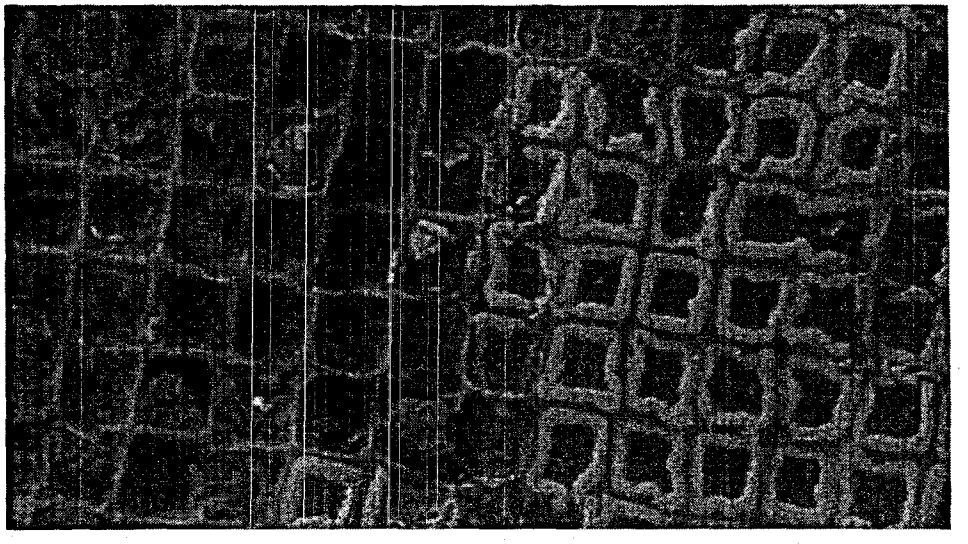

Figure 9. Electroless plating of the through wafer vias with electroless nickel.

Additional work was performed to determine the deposition rate of the electroless plating bath. The concentration of the bath as well as its temperature were varied in order to determine optimal deposition conditions. Ideally, the rest potential could be identified for the nickel electroless solution using a Cu-foil working electrode. It is imperative to maintain a constant temperature in this portion of the experiment because the rest potential changes with temperature. The optimal operating temperature for the electroless nickel as given in the literature is 90°C. This was used as the starting point.

The plating cell was set-up with a Cu foil working electrode, a Ag/AgCl reference electrode, and a Pt wire auxiliary electrode. Repetitive voltage scans are performed to determine the deposition rate. Once the rest potential is identified the objective is to repetitively scan voltage beginning at the Eo (rest potential), proceed to a reductive potential of Eo -1 V and finally out to an oxidative potential of Eo + 0.2V. Each scan is saved and another scan initiated immediately. A total of ten voltage scans are used to determine the deposition rate.

In the beginning of the experiment it was important keep in mind that the voltammetry may be perfectly reversible (ie both chemically and kinetically). Scanning from 0.6 V => 0.0 V => 0.6 V. Work at 90°C caused problems with the working electrodes so that most of the work was performed at lower temperature.

A known electrochemical system (Hexaamine Ruthenium (III) Chloride/ Na-2SO4) was used to test the response at elevated temperatures. It was found that bath temperatures beyond 50°C caused the voltammetry to become highly irreversible. After finding this, the nickel solution was tested once more at room temperature. The resulting CV (cyclic voltammogram) exhibited both forward and return waves and also a lot of crossing over in the outer potential regions. It was proposed that this could be due to the presence of the ammonium citrate and the hypophosphite in the solution. It is possible that these two components react adversely within the system. In

order to test this hypothesis, a solution of pure Ni ion was prepared using $NiSO_4 \cdot 6H2O$ with Na_2SO_4 used as the electrolyte. A more inert working electrode of Au was used in initial work. The resulting voltammetry was not reversible, but did show a forward wave. The working electrode was then exchanged for the Cu foil which again showed an increase in current, but no distinct wave. It was thought, however, that a reduction was taking place. In a later experiment bubbles were streaming from the auxiliary electrode. Instrumental malfunction was ruled out as a possible cause.

The next avenue of exploration will be the effect of pH. The copper foil electrode works well and produces reversible waves in the Ruthenium system, however, when applied to the Ni system, does not produce comprehensible data. There are many variables within this system that may be contributing to the problems that have arisen. We are continuing to examine all possibilities to accurately determine the rest potential of the electroless nickel plating solution. Further work will be required to accurately determine the optimal conditions for nickel deposition.

In addition to electroless nickel deposition, electroless Cu deposition was also attempted during the program. Copper is of particular interest because of the recent incorporation of copper interconnections as a standard process for integrated circuit manufacture. A four part commercial electroless Cu chemical system was purchased from Transene Corporation. The four part system is normally used to plate through holes on printed circuit boards and comprises a two part plating bath (solutions A&B), a surface sensitizer (solution D) and a surface activator (solution C). This system was used to plate Cu in a microchannel plate substrate. Following the manufacturer's directions resulted in a Cu layer being deposited as shown in Figure 10.

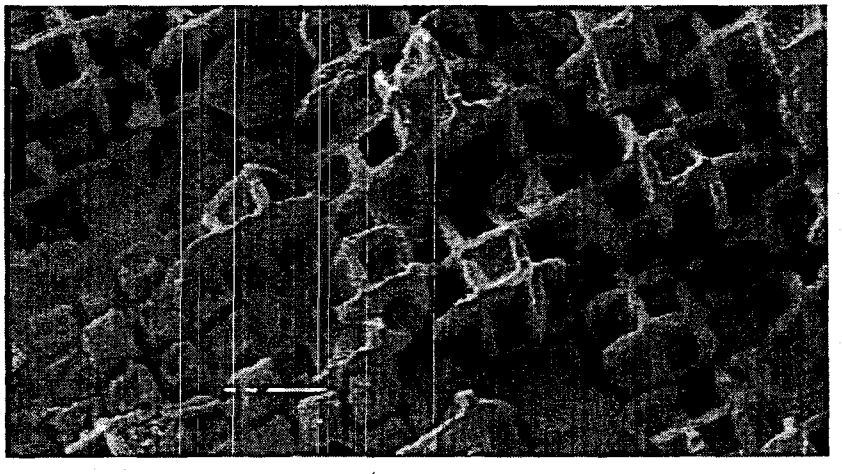

Figure 10. SEM photo showing the deposition of Cu in a microchannel plate substrate using electroless plating.

As can be seen in the photo copper deposited on both the interior walls of the channels as well as over the front faces of the substrate. The deposition rate was determined to be 5 μm/hr which is

apparently too fast to prevent the channel ends from closing over. Additonal work with the copper will be necessary to optimize the process.

Electroplating

Electroplating of solid signal lines through the channels requires a working electrode on the work piece. Initial thoughts of using an electroless plating process to deposit a strike electrode on the channel walls was abandoned because that process would suffer from the same drawbacks as using electroless plating to fill the channels completely, voids would be trapped in the channels. Simply depositing metal onto one side of the sample and using it as the strike is unacceptable because all of the metal would need to be interconnected, forcing additional processing to be required after plating.

The solution to the problem is to use a patterned plating jig that is pressed against on side of the substrate. The pattern represents the areas on the wafer where through wafer vias are desired. After the plating process is completed, the pattern may be peeled from the substrate and reused. A photo of the plating fixture developed for this purpose is shown in Figure 11. The fixture base holds a stainless steel sheet with a mask attached to it that contains a pattern for the contact pads that will lie over the through wafer vias. When the stainless steel electrode and pattern are peeled away from the wafer the plated contact pads will remain on the surface.

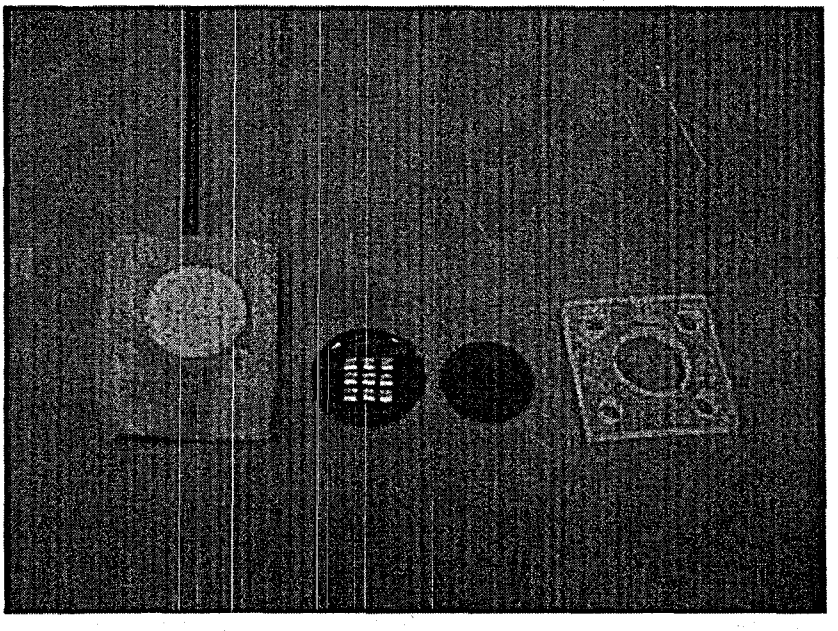

Figure 11. Electroplating fixture developed for through wafer via plating.

The fixture has been used successfully to electroplate through wafer vias in bare silicon as well as isolated silicon substrates. The mask used comprises a pattern cut directly in to a tape that is applied to a sheet of stainless steel. The adhesion of the deposited nickel to the stainless steel is porr so that it may be easily peeled away at the conclusion of the process. A photo of both sides of these samples is shown in Figure 12.

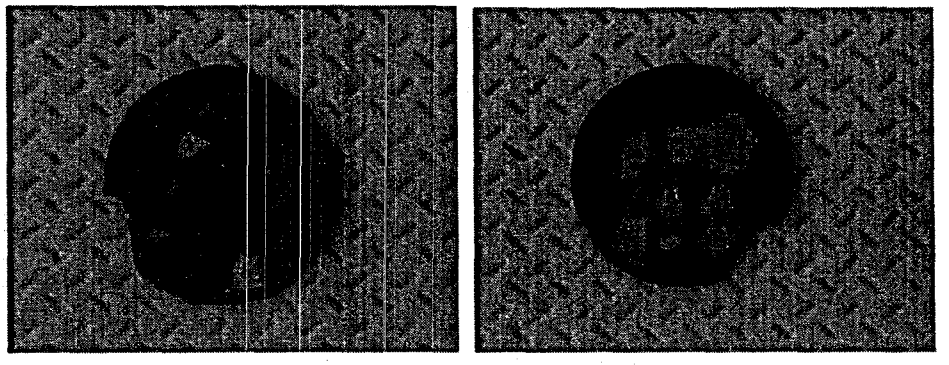

Figure 12. Photo showing the front (left) and back/electrode (right) sides of a wafer with through wafer vias.

The typical conditions we have used for electroplating nickel into the channels use a nickel sulfamate bath from Altotech (Ni-SF 2015) with a Ni concentration of 150 g/l. Boric acid is added to this at a concentration of 30 g/l. The entire bath is placed in an ultrasonic bath and plating is carried out at a current density of 3 mA/cm^2 for 3 to 6 hours.

As can be seen in Figure 12 the electroplating process leaves metal on the back side of the wafer where the pattern allows the plating process to proceed. On the front side of the wafer metal only covers the surface where it plates up through the wafer. Since the samples used in this effort are precursor microchannel plate substrates and are full of channels, this is an excellent demonstration of the power of the process.

Successfully plated pieces have been cross-sectioned and viewed using a SEM. From the pictures it is clear that solid metal lines have been plated through the wafer. A cross-section of an electroplated through wafer region is shown in Figure 13. Note that Ni rods appear to be bending out of the substrate. This is an artifact of the cleave used to create the cross-section.

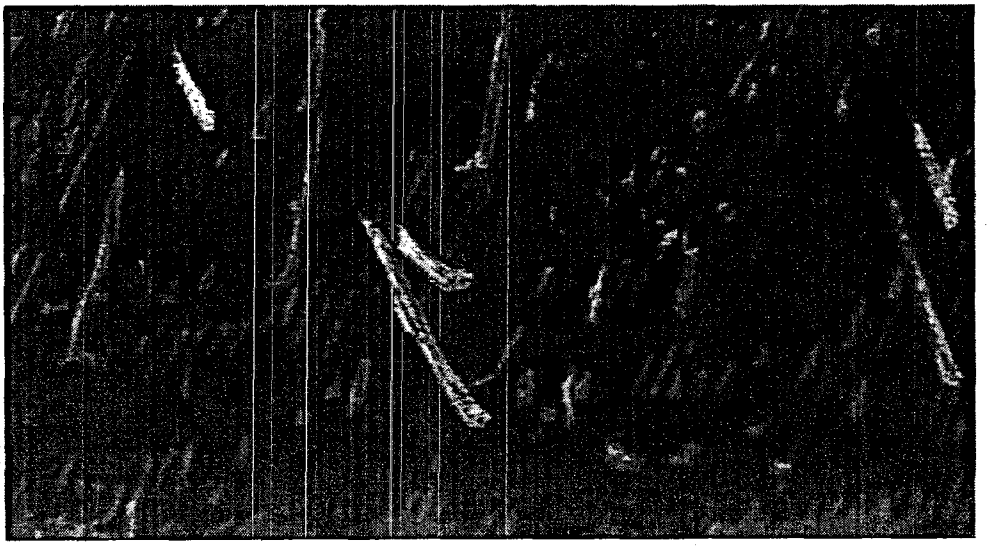

Figure 13. Cross-section of nickel plated through wafer vias.

Improvements to the process can be achieved by using a better mask material on the strike electrode. The tape presently used is very thick compared to the thickness of the desired contact pads and the mask is not precisely placed on the wafer surface. These two factors lead to the excess plating on the backside (Note the upper right hand contact pad). A better masking scheme will be developed during the phase II program to prevent this spill over. The proximity of the masking layer to the susbstrate also explains the nonuniform plating achieved. Without near intimate contact between the mask and the substrate to be plated, more material will need to be deposited in some locations before plating proceeds up through the channels. This results in the nonuniform pattern on the front side of the wafer shown in Figure 12. Aditional improvements to the process will include patterning the front side of the wafer to contain the plating within specific contact areas.

The electroplating process ahs also been used to coat the walls of the channels. Figure 14 shows a sample that has a walls coating of nickel as the result of electroplating. It is unclear how the conditions of the bath can be used to create such structures, but further investigation may make it possible to use this process to construct coaxial structures in the vias.

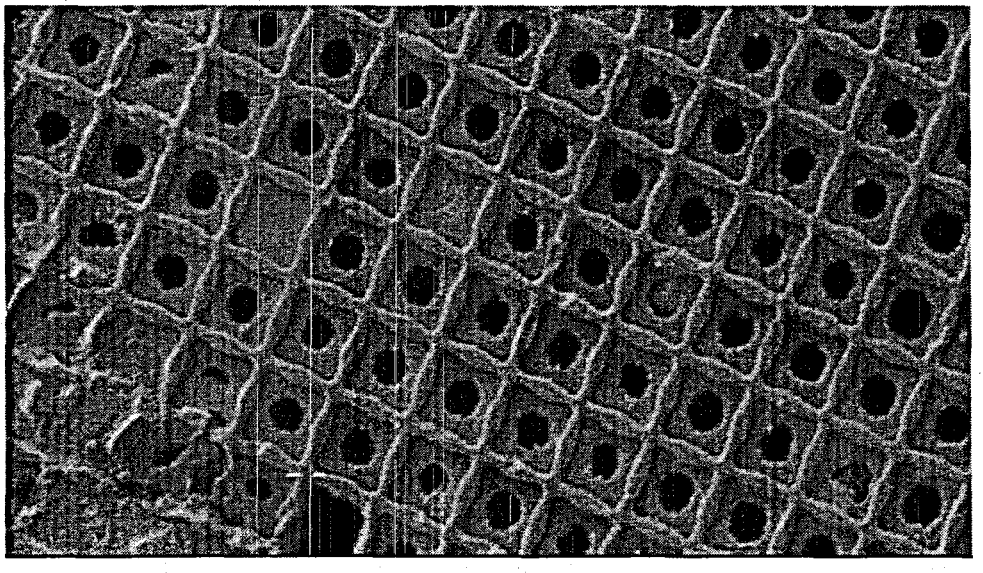

Figure 14. Vias filled using a nickel electroless plating process.

A significant test of the ability of the electroplating technique is to show that metal is deposited only in the through wafer vias lying directly above a patterned contact on the plating mask. In this case the use of microchannel plate precursor substrates acts as an enormous benefit and perhaps the most stringent test of the deposition technique since they have over 80% open area. After electrodeposition the substrates are rinsed in deionized water and dried in a small convection oven. After drying a simple optical transmission test reveals that the deposited metal only fills the vias overlying the contact pads as light is easily transmitted through out the rest of the area of the substrate.

Testing

Electrical testing of the vias was carried out using a digital multimeter. Samples were plated and contained electrical contact pads as shown in Figure 12. The samples were set on an aluminum foil and the resistance between each pad on the top to the foil was measured. In all cases each of the contacts was a short circuit, indicating that nickel metal was plated through the entire thickness of the substrate. The resistance values were too low to determine the actual number of plated through holes in each of the 1 mm x 1mm contact areas. Both bare silicon and oxidized silicon samples were tested and had the same result.

Isolation testing was performed by setting the samples on a glass plate and measuring the resistance between contact pads on the top surface of the plated samples. Both bare silicon plates and oxidized plates were tested. As expected, the resistance between contact pads on samples made using bare silicon was finite. Typically, the resistance between neighboring contacts was 1.5 to 2 MΩ indicating that the nickel made electrical contact to the substrate.

Initial measurements of the oxidized samples were surprising in that the resistance between contact pads was only 1 to 10 kΩ. Inspection of the samples under an optical microscope revealed that Ni metal had over plated most of the top surface of the samples. Removal of the excess Ni in a HCl etch solution was performed for 30 minutes. The contact pads on the back side of the sample were protected with photoresist during this procedure.

The resistance between the contact pads was measured after the removal of the excess Ni. The resistance between any two contact pads exceeded 20 MΩ, indicating that the connection is an open circuit.

Conclusions

We have investigated the construction of through wafer vias in silicon that will be suitable for high-speed signal transmission as well as power distribution between and among integrated circuit die attached to a silicon circuit board. We have successfully demonstrated through wafer vias and interconnections using both electroless plating and electroplating. Electric isolation of the substrate was achieved in this work using thermal oxidation. Up to 100 V were applied across neighboring vias with no evidence of leakage between them. The current carrying capacity of an individual channel could not be determined due to the number of channels that comprised a complete via.

We were also successful in demonstrating a technique by which manufacturing of silicon circuit board may be not only feasible, but also economical. The electrodeposition of metal using a reusable mask that can be peeled from the workpiece will allow rapid fabrication of many substrates at low cost.

Several challenges still remain before the silicon circuit board technology will be practical. Creating isolated vias is the top priority so that the remainder of the real estate can be used for other cross connections. We believe this can be accomplished during phase II through

modifications of the existing high aspect ratio silicon etch process. The second challenge is to build a system for LPCVD of silicon dioxide on the channel walls to isolate the substrate from interior signal lines and to isolate metal layers within the via. The third challenge is to refine the metal deposition steps so that control of the structures can be achieved. All of these challenges can be met and overcome during the course of the phase II program.