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WRCIP Environmental Test *Shoot-Out*, PEMs vs. CHP Surface Mount Transistors

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(Abstract follows on next page)

Abstract

An early concern in the War Reserve COTS Insertion Program(WRCIP) was the reliability of Plastic Encapsulated Microelectronics(PEMs). PEMs and Surface Mount Technology(SMT) had not previously been used to any extent in Sandia Arming Fusing and Firing (AF&F) systems. An interest was expressed in making as direct a comparison as possible between the reliability of PEMs packaging and the previously employed Ceramic Hermetic Packaging(CHP). Although we were unable to identify a component which was available with the same semiconductor die in the two types of packaging, we were able to select an SMT bipolar junction transistor from two different manufacturers which was available in both PEMs and CHP formats with near identical electrical specifications. The PEMs part was a Small Outline Transistor(SOT) in a PEMs SOT23 gull-wing package, while the CHP part was in a Leadless Chip Carrier(LCC) package. Both components were Commercial-Off-The-Shelf(COTS) and each was procured in both a PNP and an NPN transistor configuration. The PEMs transistors were furnished on a reel without any prescreening, while the CHP transistors had been screen tested by the manufacturer to JANTXV requirements. Both parts were subjected to Destructive Physical Analyses(DPA) to examine the construction methods and quality and to determine important components materials and dimensions for other analyses. The general quality and workmanship of the parts examined was quite high for both types of packaging. After electrical function testing, samples of each package and transistor type were subjected to temperature cycling(-65 to + 150°C), thermal shock cycling(-55 to + 150°C), and temperature and humidity aging in a Highly Accelerated Stress Test(HAST) at 130°C and 85% relative humidity with 48 V reverse bias to collector-base, emitter junctions. The last test is commonly used for PEMs but not for CHP. No electrical failures were observed in the temperature cycling and thermal shock groups of either package type after 5000 temperature cycles and 500 thermal shock cycles. In the HAST experiment which was run to a total accumulated time of 1750 h, No HAST induced failures were observed in the CHP parts or the PEMs NPN transistors. In the case of the PEMs PNP transistors, valid failures were observed at and beyond 1250 h. However, when the accelerated test failure distribution function is extrapolated to lower temperatures and humidity values characteristic of an assumed stockpile-to-target-sequence (STS), we predict that the lifetime of the PEMs parts is comfortably in excess of 30 y. An investigation of temperature cycling following HAST for the surviving PEMS PNP transistors showed that no failures were observed in the 1st 100 cycles (-65 to + 150°C). After 300 cycles, 2 parts out of 32 on test failed. The CHP transistor has a significantly shorter predicted solder fatigue lifetime than the PEMs part when the parts are mounted onto a polyimide-glass PWB. Thus the overall or printed wiring board level reliability of the PEMs part may be greater than that of the CHP part if organic laminate PWBs are used.

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I. Introduction

The idea for a comparison of the reliability of Plastic Encapsulated Microelectronics(PEMs) vs. Ceramic Hermetic Packaged(CHP) components arose from discussions held early in 2001. There had been opinions expressed that electronic component reliability would be enhanced if CHP parts were used in lieu of PEMs for the W76-1 Arming, Fusing, and Firing(AF&F) system application. In early 2001 we discussed the feasibility of making a direct comparison of PEMs vs. CHP reliability in environmental testing, using a component which had an identical pinout in both formats and which was as nearly electrically identical as possible[1]. Paul Plunkett of Dept. 1734 was the main source of inspiration for initiation of this test program.

In general, it is difficult to obtain exactly the same semiconductor device in both PEMs and CHP formats. Most IC manufacturers customize the IC die design, layout, passivation, etc. to the type of packaging that will be used. We did, however, identify a discrete semiconductor part, a bipolar junction transistor (BJT) which was available in both PEMs and CHP suface mount formats. Although these parts were made by different manufacturers, they did have the same nominal electrical specifications. A detailed description of the two types of components is presented below in Section II.

The selected components presented a sharp contrast with respect to the presumed level of ruggedness and reliability. The CHP part was the Microsemi HS2222ATXV(NPN) and HS2907ATXV (PNP) in a ceramic Hermitic Small Outline Transistor(HSOT) LCC package. The PEMs "equivalents" were made by On Semiconductor, the MMBT2222A(NPN) and MMBT2907A(PNP). These were packaged in the Small Outline Transistor 23(SOT23) package with gull-wing leads. Both parts had the same surface mount footprint but very different lead configurations. The MMBT PEMs cost about $0.10 per part in small quantities. The CHP parts cost about $9.00 per part.

The CHP parts were manufactured to the JANTXV quality level according to the MIL-PRF-19500 specification[2]. A brief but understandable description of the JAN series of quality levels is given on the Crystalonics website[3]. Briefly, the JAN(Joint Army Navy) designation implies:

1. That the manufacturer has complied with all requirements for manufacture of MIL-type components.

2. That the component has satisfied all applicable test requirements.

3. That the test data will remain on file for at least five years.

4. That the JAN data are available from the supplier upon request.

The additional TX quality level signifies a 100% screen including: storage bake, temperature cycling, fine and gross leak tests, and burn-in. The V level signifies 100% visual inspection prior to lid-seal.

The PEMs MMBT transistors were Commercial Off the Shelf(COTS) and were supported only by the data sheet[4] and manufacturer published reliability data. There was no mention of any screening performed on these components.

II.Components selected

The WRCIP Environmental Test Shoot-Out was to be a comparison of the traditional hermetic components vs. the "new" plastic encapsulated microelectronics, PEMS. Component selection was based on the need of the next assembly users for smaller components thereby restricting us to surface mount packages. The 2N2222A /2N2907A transistors were selected as good representatives of past and futures designs. Component selection at this point narrowed down to the packages available for these BJT transistors; the plastic encapsulated SOT-23 surface mount and the ceramic hermetic small outline transistor, the HSOT, which is a three pin leadless chip carrier design matching the footprint of the plastic SOT-23 package.

A. PEMS SOT-23 BJT: The MMBT2222ALT1 and MMBT2907ALT1

These components were selected as the best candidates for the plastic encapsulated components. These transistors were originally manufactured by Motorola, Inc, a 6 sigma company, which spun off their discrete component product line to On Semiconductor. On Semiconductor continues to produce the Motorola line at the same facilities using the same specifications and processes. An initial manufacturer assessment was done to assure that the quality level of the manufacturer was adequate for use in SNL designs. There is no100% testing required at the manufacturer for this product.

B. Ceramic LCC BJT: The HS2222ATXV and HS2907ATXV HSOT

These components are manufactured in a HSOT (Hermetic Small Outline Transistor) package by Sertech Labs, a Microsemi Company. They were chosen as being representative of a traditional "SA" component. They are hermetic parts and are manufactured to Mil-Prf-19500/JANTXV standards by a company which SNL considers to be a *known good manufacturer*. SNL has an ongoing purchasing relationship with Microsemi and Honeywell FM&T has done internal audits on the company to DOE/KCP requirements. These components have had the traditional mil-spec/JANTXV testing: 100% pre seal visual on the die, electrical tests per product specification(slash sheet in mil-spec terms), burn-in, and hermeticity.

III. Test plan

After some discussion, we selected a PEMs reliability test suite as being the most suitable for comparison purposes. This suite included temperature cycling, thermal shock, and temperature and humidity testing (Highly Accelerated Stress Test or HAST). The CHP parts had an operating junction & storage temperature range of –65 to +200°C while the PEMs parts were rated from –55 to + 150°C. For temperature cycling, we selected a basic or first test of 1000 cycles at MIL-STD 883 condition C, -65 to + 150°C. For the PEMs parts this represents an “up-

rating" situation, as it is beyond data sheet specifications. For thermal shock, we selected a range of –55 to +150°C because of thermal shock equipment limitations.

The temperature cycle and thermal shock exposures were performed at Analytical Solutions Inc.[5] using the applicable procedures from MIL-STD-883E[6]. Temperature cycling is covered by Method 1010.7 and thermal shock by Method 1011.9. Neither method specifies a fixed number of cycles for the test. The JEDEC temperature cycling industrial standard recommends 1000 temperature cycles for "Qualification"[7]. The JEDEC thermal shock industrial standard specifies 15 shock cycles[8].

For HAST, we selected a relatively standard condition of 130°C and 85% relative humidity(RH), with 48 V reverse bias to the collector-base junction, with the emitter and base connections tied together. The basic time interval was 250 h. HAST is not a standard test for CHP because, in theory, no moisture can penetrate through the package and lid-seal to the surface of the transistor. Since all of the CHP had been leak tested, according to the JANTXV rating, we expected no failures for these parts. However, we wanted to investigate the possibility of a micro-crack forming during the test, with consequent moisture intrusion.

The JEDEC standard for HAST specifies a 96 h exposure at 130°C and 85% RH [9]. We selected a longer exposure time, 250 h, based on the fact that this longer time is used by a number of other industrial firms. In addition, our analysis indicates that the 96 h time is somewhat short of that necessary to enable extrapolation of accelerated test data to prediction of sufficient lifetime under operational and storage conditions. Life prediction is discussed below in Sec. VIII.

The test plan developed by Lori Curtis of 1734 is shown in Fig 1. There are three legs or sections in the environmental portion of the plan; temperature cycling, thermal shock, and HAST. The fundamental intervals or durations shown for the three tests were; temperature cycle-1000 cycles, thermal shock-100 cycles, HAST-250 h, as described above. In the Shoot-out we extended these basic levels in an attempt to obtain failures. The temperature cycle and thermal shock legs were extended to 5000 temperature cycles and 500 shock cycles, respectively. The HAST aging was extended out to 1750 h. During the tests, any parts which failed electrical test were removed for failure analysis.

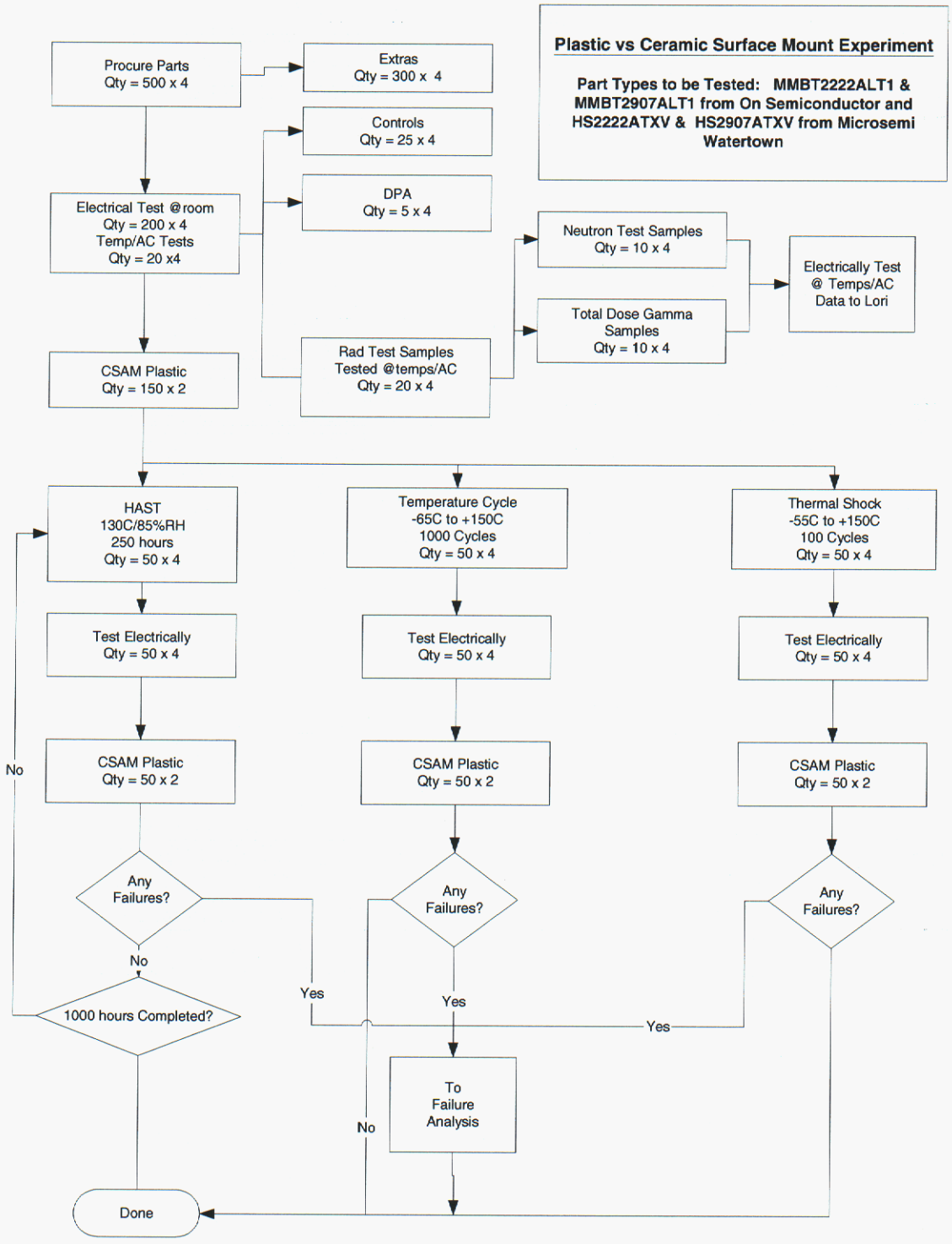

Fig 1. Flowchart showing the test plan for the environmental test portion of the "Shoot-out". There are three legs in the test plan; temperature cycle, thermal shock, and HAST.

IV. Component Analyses

A. DPA

A destructive physical analysis(DPA) of both components was performed by Analytical Solutions Inc(ASI). In the case of the PEMs/MMBT part, we had additional measurements made beyond the usual ASI suite. These measurements included identification of packaging and die materials and measurements of various die and package dimensions. The added information is used for various types of analyses, such as the solder fatigue analysis described below.

1. PEMs/MMBT

An optical micrograph of several PEMs/MMBT parts is shown in Fig 2.

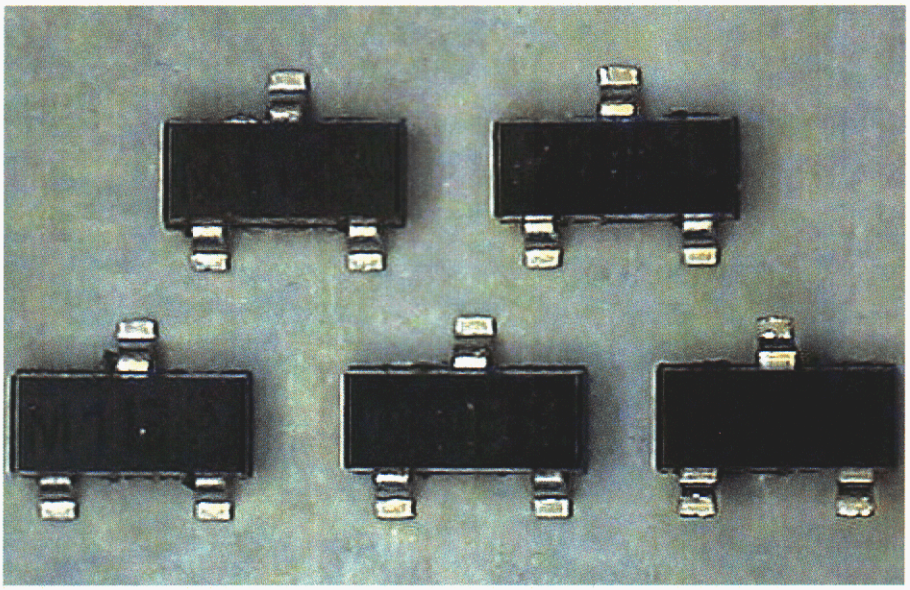

Fig 2. Optical micrograph of top view of five MMBT parts. These parts are about 115 mils in the long dimension and 95 mils in the short dimension, including the leads.

An ASI supplied SEM cross-section of the PEMs part is shown in Fig 3. The various components of the packaged transistor are shown. The mold compound is loaded with fused silica to reduce its CTE.

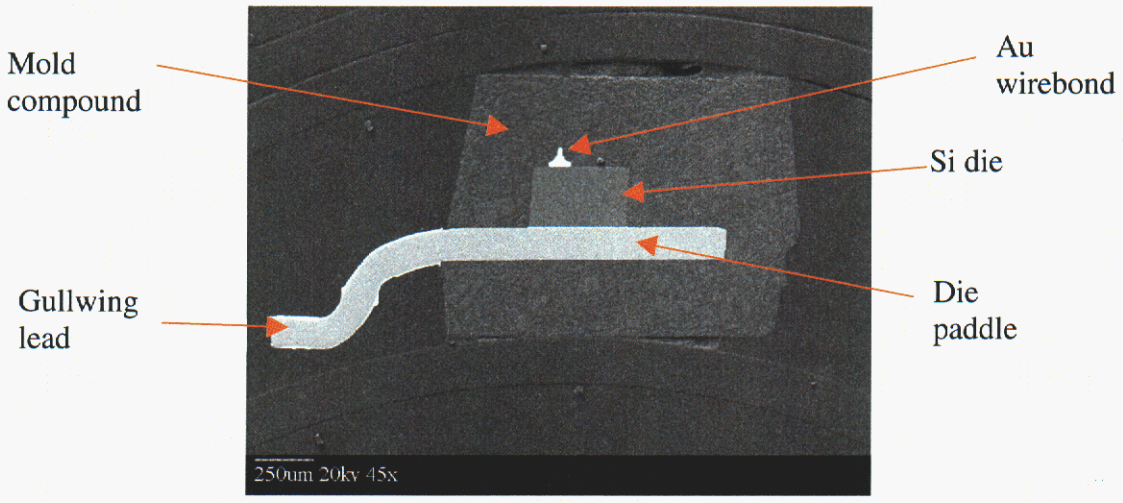

Fig 3. SEM cross-section of the PEMs/MMBT transistor showing die, die paddle, gullwing lead, and mold compound.

In the DPA, the mold compound in the die region is removed by an etching process. An SEM micrograph of a part after mold compound removal is shown in Fig 4.

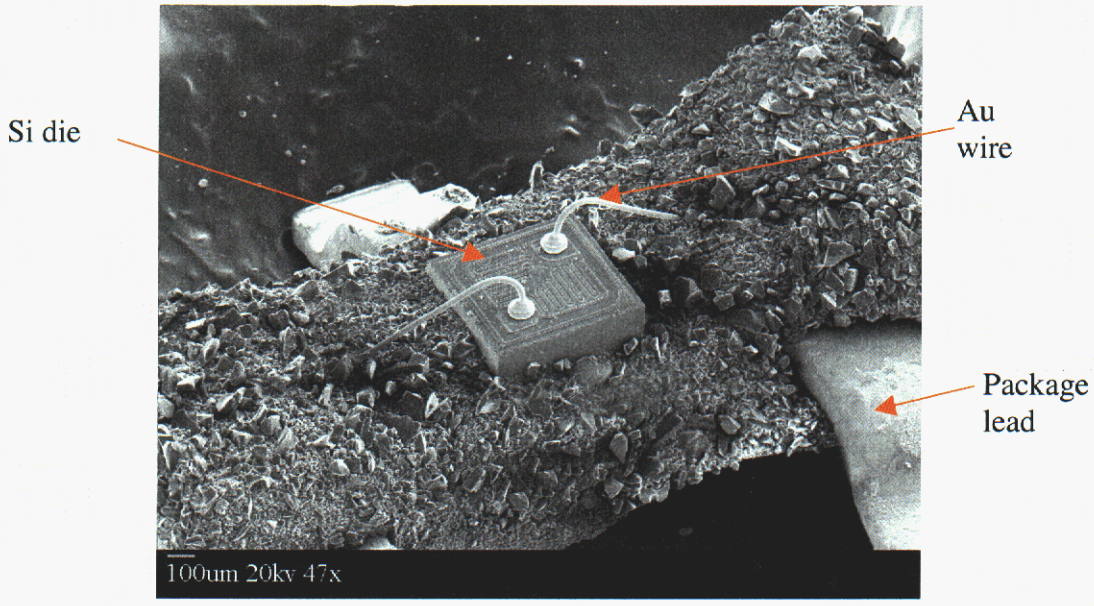

Fig 4. PEMs/MMBT semiconductor die after epoxy removal (decapsulation). The debris around the die is mostly composed of the fused silica particles from the etched epoxy region. The Au wires from the die to the leadframe have not been attacked by the etchant.

The DPA revealed that the Si transistor die had a 0.7 µm thick Si_xN_y passivation layer and that the top level metal was Al with a thickness of 1.4 µm. There was no die coat used between the die top and the mold compound. The die attach layer was solder with a 2.3 µm thickness.

2. CHP/LCC

An optical micrograph of several of the CHP parts is shown in Fig 5.

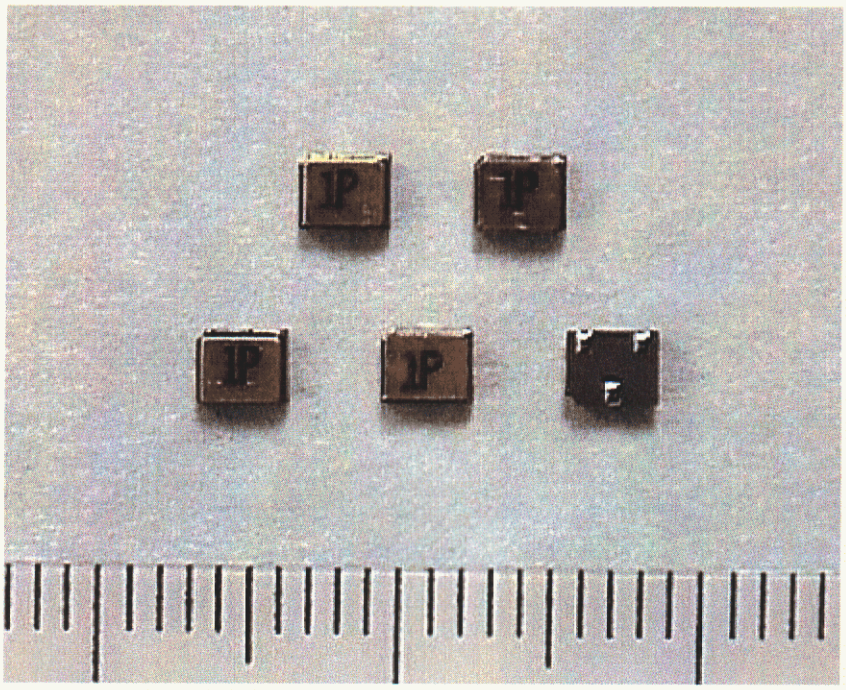

Fig 5. Five of the CHP/LCC parts in HSOT format. The bottom right part is bottom up, showing the three solder pads on the die bottom. These pads have the same footprint as the MMBT gullwing leads.

The cavity of a part with the lid removed is shown in Fig 6. This transistor also used SiN passivation but the thickness was not determined in the normal DPA which was used in this case.

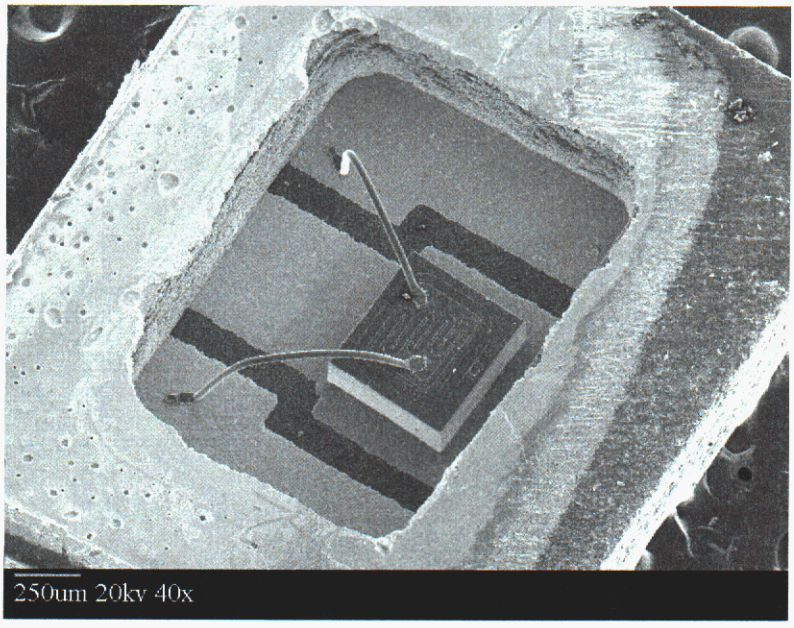

Fig 6. CHP/LCC transistor with the lid removed. The wires are Al, with wedge bonds on die and Au header pads.

B. CSAM

In the case of the PEMs component C-mode scanning acoustic microscopy(CSAM) was used to search for delaminations between the mold compound and the die or die paddle surfaces. This technique is not normally employed with CHP because the cavity produces a strong reflection of the ultrasonic pulses and prevents investigation of the underlying Si die.

As indicated in the test plan, Fig 1, A CSAM scan was made of each part before and after environmental exposure. A typical image from our Sonix CSAM is shown in Fig 7. If a void is present, the reflected ultrasonic pulse from the void region has a phase inversion relative to the phase of the incident pulse. The CSAM system detects this inversion and displays it in red. The red portions of the image in Fig 7 occur at the perimeter of the leadframe and die paddle regions and are probably not true delaminations. In a black and white copy, the red regions will appear dark in color. A CSAM machine indication of a delaminated region is indicated in the figure. An X-ray image of the part is shown in for comparison in Fig 8.

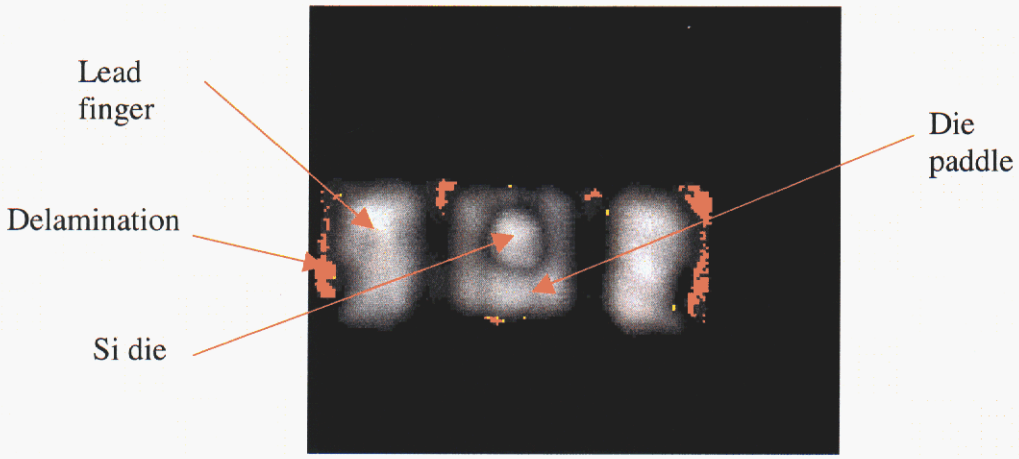

Fig 7. CSAM phase inversion image of an MMBT part before HAST exposure. This part is MMBT2222, part # 26.

Comparison of the X-ray and CSAM images allows all features of the CSAM image to be identified with corresponding parts of the package. It should be noted that the Si die is not very visible in the X-ray because the Si has a low atomic number and is not sufficiently absorbing to be resolved relative to the Cu/Ni die pad. The Au wires with high atomic number are clearly defined.

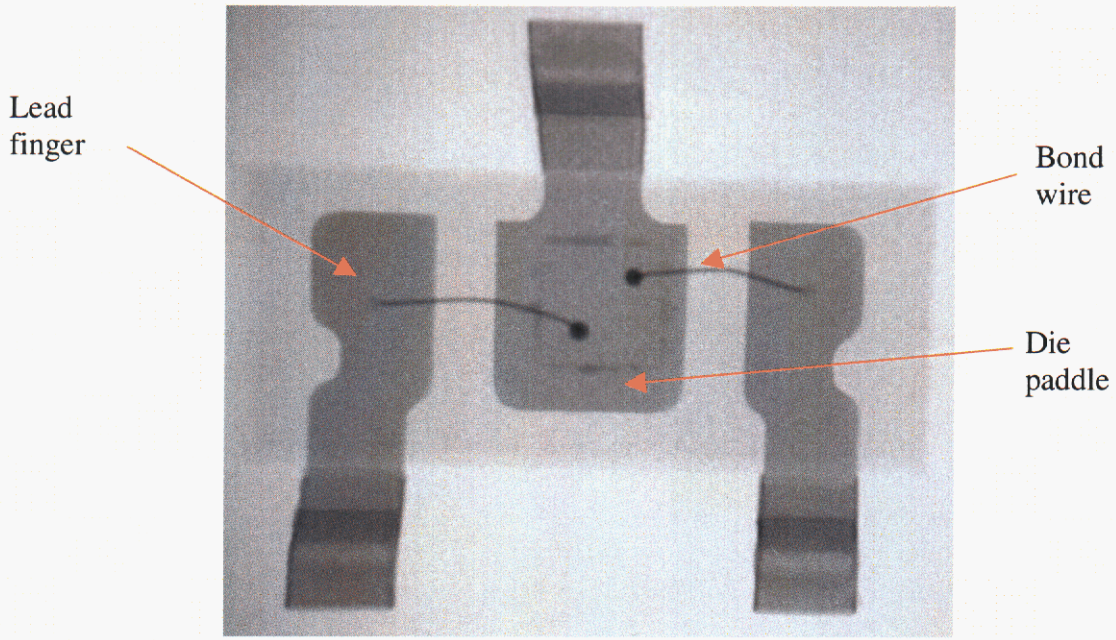

Fig 8. X-ray image made at SNL of the MMBT part showing the lead-frame and bond wires. The Si die is not very visible below the wire bonds above the Cu/Ni die paddle because Si is not sufficiently x-ray absorbing so as to provide sufficient contrast.

There is no universal *standard* for CSAM delamination analysis. The two CSAM system manufacturers, Sonix and Sonoscan, utilizes different algorithms for phase inversion detection. The most applicable general CSAM standard is IPC/JEDEC J-STD-020A [10]. This standard is

used for moisture sensitivity testing but is commonly used for other PEMs environmental tests, such as the ones in this study. A new SNL CSAM standard is under development.

Ref. 10 defines a "measurable delamination change" as a 10% change in delamination area. For the small die in the MMBT package, 0.015 in. on a side, resolution at the 10% level(0.0015 in. = 38 μm) is difficult. For peripherally leaded components the IPC/JEDEC standard lists the following criteria for passing CSAM after an environmental test [10]:

1. No measurable delamination change on the top surface of the die.
2. No measurable delamination change on any wire bonding surface of the die paddle.
3. No measurable delamination change along any polymeric film bridging any metallic features that are designed to be isolated.
4. No measurable delamination/cracking change through the die attach region in thermally enhanced packages.
5. No surface-breaking feature delaminated over its entire length.

For criterion 1. above, we tried to observe any delamination in the die area. For 2. we looked for delamination in the upper region of the lead fingers, as shown in Fig 7 and Fig 8. For 3. we searched for delamination between the die paddle(collector) and lead fingers(emitter and base). For criterion 4., we did not search for die attach voiding because of the small die size and because a solder die attach was used. For item 5. we looked for delaminations extending from the lead fingers or die paddle to the package perimeter.

One of the major difficulties in performing sequential CSAM measurements after each environmental test leg is that of achieving the same machine setup and transducer focus that was used in the previous or preceding measurement. We did not use a "calibration sample" but that would definitely be a good idea for other experiments of this type.

C. Solder fatigue

The fatigue of solder joints of surface mount components is caused by the thermal stresses which are produced by the mismatch of coefficients of thermal expansion (CTE) between the component case, leads, solder, and printed wiring board (PWB). Although this is an assembly rather than an individual component issue, it does influence the selection of components in assemblies. There are several methods and codes for evaluation of solder joint fatigue. As a screening tool, the Solder Reliability Solutions (SRS) code is used to calculate predicted time to solder joint failure from thermomechanical fatigue(TMF) in thermal cycling[11].

The SRS code calculates the work done or energy dissipated in a solder joint during a temperature cycle. The calculation accounts for both global (component case to board) and local (PWB and lead to solder) stress-strain hysteresis loops. Much of the work done is due to solder creep expansion or contraction, so the program considers dwell time at the temperature extremes. Other inputs to the program are the geometries (including amount of solder), materials, cycles per day, and the CTE of the constituents. The calculated strain energy per cycle is then

compared to a time to failure vs. hysteresis loop area correlation derived from historic data to determine the estimated time to first failure (and characteristic life) of the solder joint.

One of the major factors affecting the lifetime is the lead or assembly stiffness. This is, essentially, the spring constant characterizing the package connection to the solder joint and PWB. The stiffer the joint(larger spring constant), the greater the force or stress on the solder joint from a given thermally induced strain. The CHP LCC has a much stiffer joint than the compliant leaded PEMs SOT23 with its gullwing lead. Hence, we would anticipate that the CHP/LCC will have a shorter fatigue life than the PEMs/SOT23. This illustrates the important fact that overall or printed wiring assembly(PWA) level reliability will not automatically be enhanced if the PEMs part is replaced by its CHP equivalent.

The components were analyzed with SRS using the minimum solder area and thickness given in IPC standards. The assumed thermal stress was one cycle per day between 16 and 43 °C. Two hours of dwell time were used at each extreme as an approximation. The SRS code can only analyze for step-change thermal profiles. Thus a daily harmonic profile has to be approximated by a step-function profile.

The spring constants, k, as calculated with the SRS program, given the lead geometries and materials, were; SOT23, k = 3000 lb/in. and HS2907, k = 250,000 lb/in. The large lead stiffness for the CHP/LCC HSOT package leads directly to a short solder fatigue life, as discussed below.

TMF lifetime is maximized when the CTE of the PWB is close to that of the component. In order to match the CTE's of the components two different board types were used. A polyimide/glass board with a CTE of about 14 ppm/°C is a good match for the PEMs/SOT23. An epoxy glass PWB such as FR4 would be even better, with a CTE in the range 14-18 ppm/°C. A polyimide aramide board with a CTE of 7 ppm/°C is a good match for the CHP/LCC. The results of the analysis are given in Table 1.

Table 1 Time to First Failure(y) of Solder Joints as calculated with the SRS model for the two different package types and two board material types.

PWB → Component ↓	Polyimide Glass	Polyimide Aramide
PEMs-MMBT	35 y	19 y
CHP-LCC	15 y	28.5 y

For a target life of 30 years the PEM's part on a polyimide-glass will nominally meet a 30 y life requirement. The ceramic part will not. It is unlikely that an polyimide-aramide PWB would be used in the application because of the presence of other PEMs components which would have a poor CTE match with this material.

Because of the large variation in low cycle fatigue data, the lives given in the table should be used for relative comparison only. In actual use the amount of solder, temperature extremes, and loading ramps will require additional refinement.

V. Tests & Measurements

A. Electrical measurements

1. Test method

Testing was performed at Sandia National Laboratories, Department 1734, in the Test and Characterization Laboratory. The parts were first separated into the different environment test groups, serialized and travelers generated. Serial number identity was maintained by device location in waffle packs. Table 2 lists the parts, test environment and associated traveler number.

DC parametric measurements were performed at room temperature using the TESEC Discreet Test System, Model 881-TT/A, with Test Station Model 7811-A and some custom built test adapters. Some devices were tested using a probing station and associated test equipment and software.

Table 2. Test Travelers

Part Number	HAST	Temperature Cycle	Thermal Shock
MMBT2907ALT1	01-06004-01	01-06004-02	01-06004-03
MMBT2222ALT1	01-06005-01	01-06005-02	01-06005-03
HS2907ATXV	01-06006-01	01-06006-02	01-06006-03
HS2222ATXV	01-06007-01	01-06007-02	01-06007-03

2. Test hardware – software configurations

As previously stated measurements were made on different test configurations depending on the type and purpose of the measurement/test. Table 3 lists the measurement – configuration relationships.

Table 3. Test configurations

Device	Measurement	Equipment	Adapter	Software	Program
MMBT2907ALT1	DC Parameters	TESEC 881-TT/A	TF8010-2	SPEKTRA Test System Ver. 3.0	HS2907A1.tst
MMBT2222ALT1	DC Parameters	TESEC 881-TT/A	TF8010-2	SPEKTRA Test System Ver. 3.0	HS2222A1.tst
HS2907ATXV	DC Parameters	TESEC 881-TT/A	TF8010-1	SPEKTRA Test System Ver. 3.0	HS2907A1.tst
HS2222ATXV	DC Parameters	TESEC 881-TT/A	TF8010-1	SPEKTRA Test System Ver. 3.0	HS2222A1.tst
All Devices	Failure Verification	Probing Station	None	ICCAP Ver. 5.30	Custom Setups

3. Test Programs

Two TESEC programs for the two device types, 2N2907 and 2N2222, were generated. These programs measured the different parameters specified in the device's specification sheet.

4. Failure Verification

Each device was tested on the TESEC at room temperature after every stress step. If the TESEC test indicated that the device had failed, the device would be re-tested. If it failed again, it would then be probed and tested for functionality. The probing test configuration would first test for device functionality by measuring and plotting an h_{fe} versus I_c curve. If a minimal curve could not be measured, then the system would try to verify the functionality of the Base – Emitter and Base – Collector diodes. These measurements would indicate whether the device had failed open or failed short. The failed devices would be removed from experiment and sent for failure analysis.

5. Difficulties and Solutions

During the testing some difficulties arose which made testing difficult. Following is a list of the difficulties, suspected cause and attempted solutions.

Table 4. Difficulties and solutions for electrical measurement problems encountered during the Shoot-out

Problem	Package Type	Cause	Remedy
Unexplained device failures on TESEC	SOT-23 & HSOT	Inserting device backwards into test socket	Inserted diode tests at beginning and end of TESEC Programs
Failures due to bent device leads	SOT-23	The HAST boards use a socket which tends to bend leads	Gently straighten device leads
Corrosion	SOT-23 & HSOT	HAST environment	Scrape corrosion off device
Failures due to bad continuity	HSOT	Removal of HAST corrosion with sandpaper	Cease using sandpaper, probe if necessary
Missing device leads	SOT-23	Lead overstress from straightening	Probe if lead length allows

B. CSAM delamination analysis

For this experiment the CSAM measurements were made in the reflection mode with a 50 MHz transducer. A setup file was generated on test part("50MHz PEMS transistor_2.icp") which was used at each succeeding measurement. One of the major challenges in this experiment was obtaining the same system "setup" each time. The setup file adjusts the receiver gain and gate properties but the focus must be set manually. The operator(M. Montano) developed the following process to make the focus adjustment. The system motors were first initialized, as prompted by the system WINIC software. The "rough" height of the CSAM was then set by setting the rough adjustment to a height of 1.5" at the center of the wing nut on ruler #1(see attached illustration). The *50MHz PEMS transistor_2.icp* parameter file was then opened and the height was checked from the center of the wing nut to ruler #2 and this height was set to 3 3/16 in. The head was then moved over the part to be scanned by clicking on the "go to start" button. Once the head was over the part, the A scan traces were observed to see if they looked like those of the previous scans. If the trace did not look the same, then some fine adjustments were made to the focus height by using the system WINIC software. A test scan would then be performed on the part and the image would be compared to a previous one. Once all of this was verified the CSAM analysis would be performed on the parts.

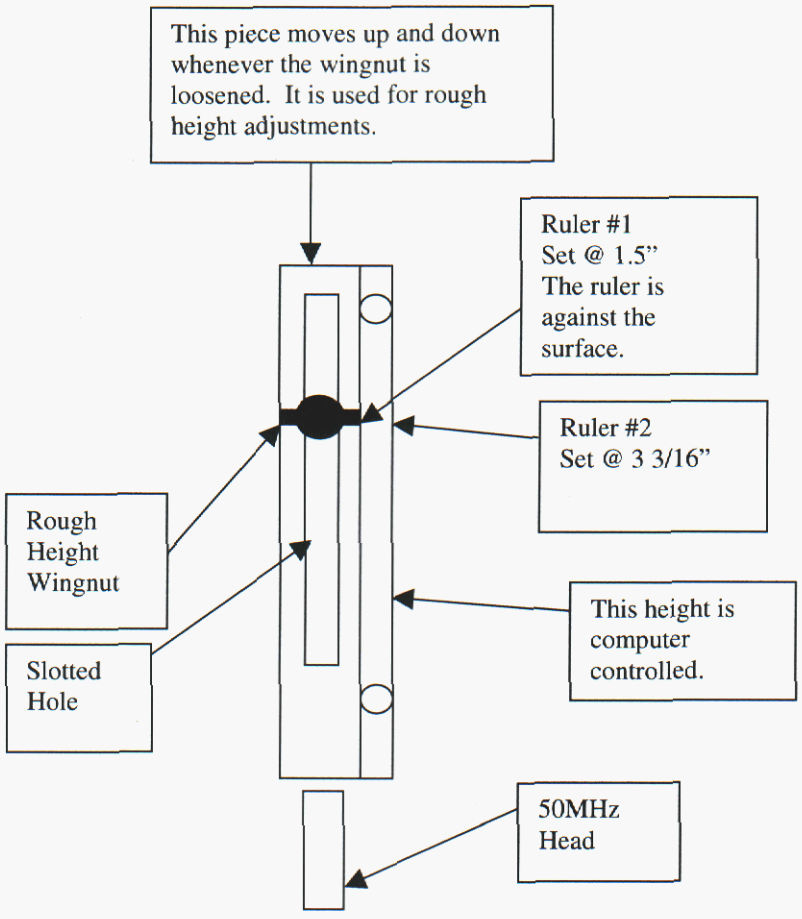

Fig 9. Equipment and scheme for establishing a repeatable CSAM focus on the PEMs SOT23 parts.

C. Environmental tests

1. Temperature cycling

The temperature cycling was performed at ASI in accordance with MILSTD-883, condition C, Method 1010.7[12]. The test system had two chambers, one at –65°C and one at 150°C. A complete cycle lasted 22-23 minutes and the part transfer time was about 10 s. Ref. 12 requires the transfer time be less than 1 minute and the hold time to be greater than 10 min.. The part temperature was believed to stabilize in a few minutes after transfer.

2. Thermal shock

The thermal shock testing was performed in the range 155 to + 150°C in a liquid to liquid environment[13]. The transfer time was 15 s and the dwell time was 5 min. The transfer time exceeded the limit set in Ref. 13, $\Delta t_{transfer} < 10$ s. The dwell time specified in Ref. 13 is $t_{dwell} > 2$ min, so this condition was satisfied.

3. HAST

The HAST was performed in an Express Test 1000 system run at 130°C and 85% RH. The test boards are polyimide with plastic sockets for the components and stitch wire welded connections to minimize the chance the the board connects will be damaged during the HAST.

The HAST bias circuit for PNP and NPN transistors is shown in Fig 10.

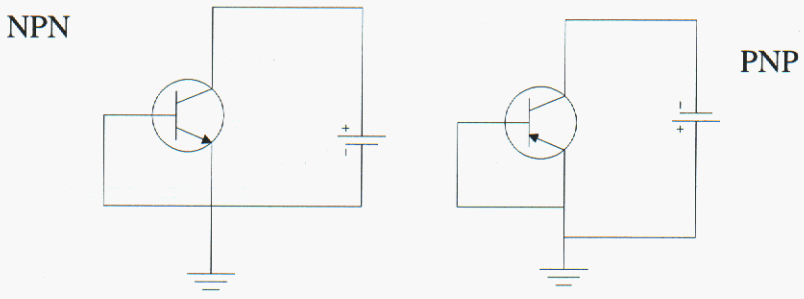

Fig 10. Bias arrangement for the transistors in HAST. The base and emitter leads are tied together at 0 V and the collector is set a +48 V for the NPN(left) and –48 V for the PNP(right).

VI. Test Results & FA

A. Temperature cycling

The temperature cycling test was extended to 5000 cycles at MIL-STD-883 condition C, with electrical and CSAM measurements every 1000 cycles. There were no electrical failures detected for either the PEMs/MMBT or the CHP/LCC components at any measurement point. No difficulties were experienced making electrical measurements and there was no fallout from test induced electrical overstress(EOS). This is an important result because it shows that EOS is not routinely seen when the parts are in good condition and the package leads not damaged by environmental exposure.

The PEMs transistors exhibited a progressive increase in delamination as the test progressed. We did not observe any delamination at the die surface but there was increasing die paddle delamination as the test progressed. An example of relatively moderate delamination is shown in this progressive view of MMBT/2N2222 Part # 89, Fig 11. The red regions indicate a large phase inversion or delamination signal from the CSAM. The yellow regions represent less severe delamination. In black and white, the red regions appear dark and the yellow regions light, relative to the shade of the die paddle.

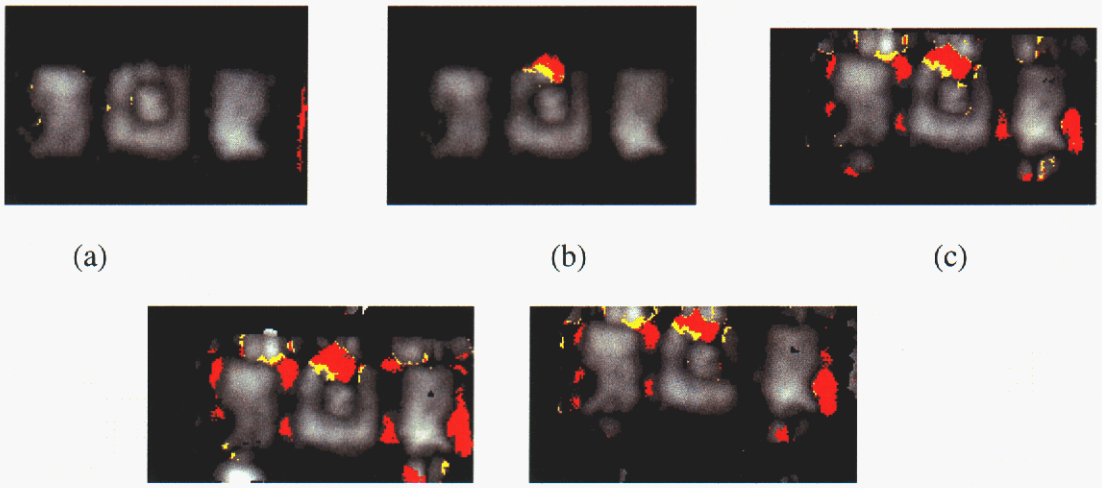

Fig 11. Successive CSAM images for an MMBT/2N2222 part, part # 89. (a) – initial measurements, (b) 1000 cycles, (c) 2000 cycles, (d) 3000 cycles, (e) 4000 cycles.

The successive scans in Fig 11 show the growth of delaminated regions with progressive temperature cycling. A delamination at the bottom of the die paddle(top of image) appears after 1000 cycles(Fig 11 (b)). After 2000 cycles some delamination is evident at the perimeter of the die paddle and lead fingers(Fig 11 (c)). The delamination does not grow appreciably greater in succeeding temperature cycles

Somewhat more severe delamination is shown for part # 115 in Fig 12

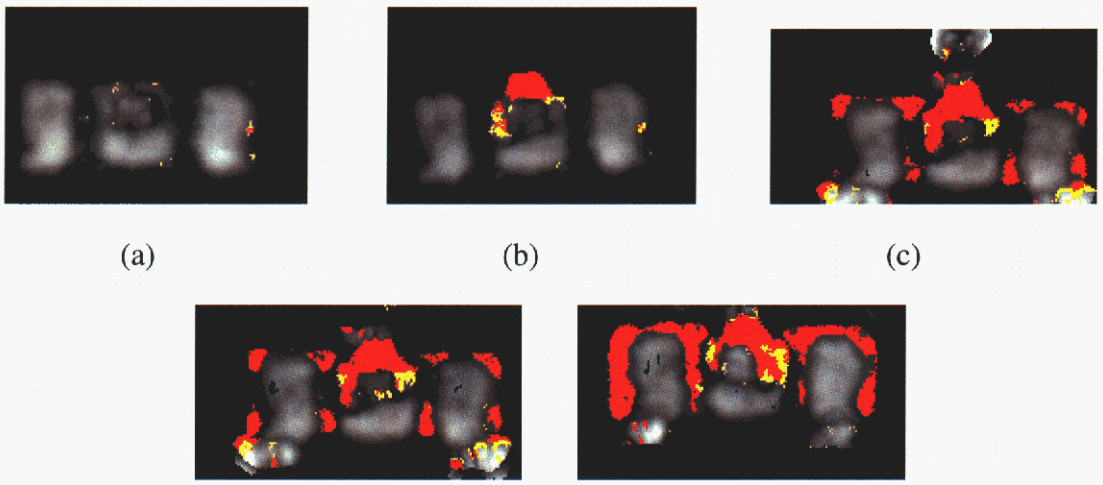

Fig 12. Successive CSAM images for an MMBT/2N2222 part, part # 115. (a) – initial measurements, (b) 1000 cycles, (c) 2000 cycles, (d) 3000 cycles, (e) 4000 cycles.

Within the limits of resolution, there does not appear to be die surface delamination in Fig 12. There is also not clear evidence of delamination between the die pad and either of the

lead fingers. After 4000 cycles, Fig 12(e), there are delaminations in adjacent regions but there is some black or non-delaminated area between the regions. There is no evidence of delamination in the wire bond area on the lead fingers.

B. Thermal shock

The thermal shock test was extended to 500 cycles at –55 to + 150°C., with electrical and CSAM measurements every 1000 cycles. There were no electrical failures detected for either the PEMs/MMBT or the CHP/LCC components at any measurement point. No difficulties were experienced making electrical measurements and there was no fallout from test induced electrical overstress(EOS).

The delamination observed in CSAM was not as severe as that seen in temperature cycling. A representative part is shown in Fig 13. There are no "JEDEC" failures evident in the CSAM data.

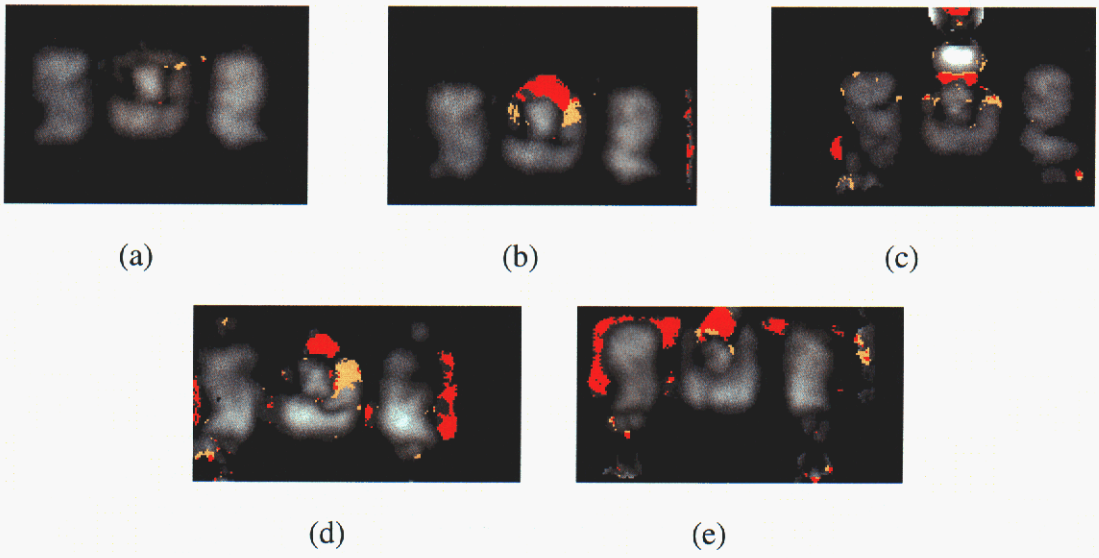

Fig 13. Successive thermal shock CSAM images for an MMBT/2N2222 part, part # 126. (a) – initial measurements, (b) 100 cycles, (c) 200 cycles, (d) 300 cycles, (e) 400 cycles.

C. HAST

The HAST portion of the experiment proved to be the most difficult part, experimentally. Corrosion of solder plated package leads with progressive HAST exposures led to difficulties in both biasing in the HAST system and in electrical measurement using the test socket in the Dept. 1734 laboratory. A number of electrical failures were observed for both PEMs and CHP parts during the test. Most of these were attributed to electrical overstress(EOS) and are not considered to be valid "HAST induced failures". However, starting at the 1250 h measurement point, we started to observe potentially "valid" failures for the MMBT2907 PNP transistors. At 1250 h, one part had a lifted wire bond that showed evidence of Au-Al intermetallic growth. This is a familiar sign and has frequently been observed before [14], [15],[16],[17]. At the 1500 h measurement point, 11 MMBT2907 parts failed electrical test.

Failure analysis has confirmed that 9 of these were "valid", a direct result of bond lift rather than EOS.

A summary of the measurement data for the HAST leg is shown in Table 5.

Table 5. Summary of part failures during the HAST leg of the testing.

Package Type	**PEMs/SOT23**		**CHP/LCC**	
Part Number, Type	MMBT 2907 PNP	MMBT 2222 NPN	HS 2907 PNP	HS 2222 NPN
Parts in Test	50	49	50	50
250 h	No fail	No valid fail-3 EOS HAST handling failures, 1 part broken.	No fail	No valid fail-4 EOS HAST handling failures, 1 part broken.
500 h	No fail-50 parts remaining.	No fail-45 parts remaining.	No fail-50 parts remaining.	No fail-1 part lost in handling-44 parts remaining
750 h	No fail-HAST bias failure-50 parts remaining.	No valid fail-HAST bias fail, 1 EOS fail-44 parts remaining.	No valid fail-HAST bias fail, 1 EOS fail, 1 lost-48 parts remaining.	No fail-HAST bias fail-44 parts remaining.
1000 h	No valid fail, 1 EOS fail, 1 part broken-48 parts remaining. Au/Al intermetallic observed in FA.	No fail-44 parts remaining.	No fail-48 parts remaining.	No fail-44 parts remaining.
1250 h	2 fails: 1 "valid" fail-Au/Al intermetallic, 1 EOS fail.-46 parts remaining	No fail-44 parts remaining.	No fail-48 parts remaining.	No fail-44 parts remaining.
1500 h	11 part failed. 9 confirmed "valid", 2 lost at FA.-35 parts remaining.	No fail-44 parts remaining.	No fail-48 parts remaining	No fail-44 parts remaining.
1750 h	3 fail- 1 EOS, 2 "valid" – Au/Al intermetallic. 32 parts remaining.	No fail-44 parts remaining.	No fail-48 parts remaining	1 EOS fail-47 parts remaining.

A precursor to the MMBT2907 failures at 1250 h was observed in failure analysis of a part which failed at 1000 h. Although the cause of that failure was ascribed to EOS, intermetallic formation was observed and low bond strength was observed at both the base and the emitter

leads, 1.9 and 1.5 g, respectively. This can be compared with an average bond strength ≈ 6 g on new parts. In the case of the MMBT2907 PNP parts, the emitter and base bonds were biased at –48 V relative to the collector.

An SEM micrograph made by ASI of a wirebond from the 1000 h failure analysis is shown in Fig 14.

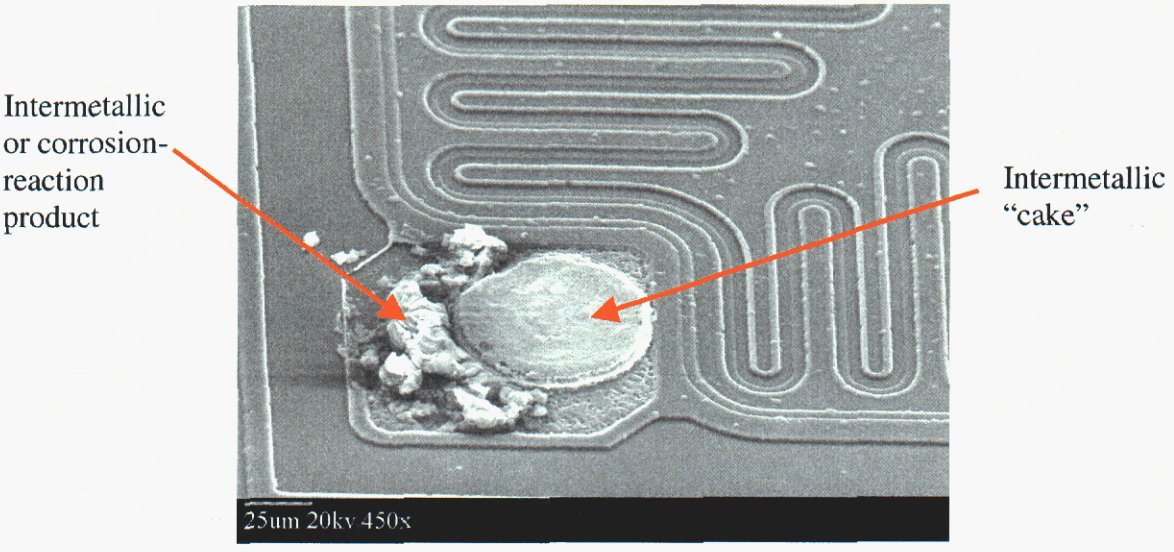

Fig 14. SEM view of the base ball-bond following destructive bond pull testing. One arrow indicates the presence of the intermetallic "cake" which remained adhered to the bond pad. The bond lift occurring at this location is indicative of kirkendall voiding related to the long term HAST exposure. Also indicated is chemical reaction product which formed during the HAST. exposure.

An SEM of a section through a failed wire-bond from a MMBT2907 part after 1500 h of HAST is shown in Fig 15. The crack occurred in a weak intermetallic layer at the top of the reaction zone.

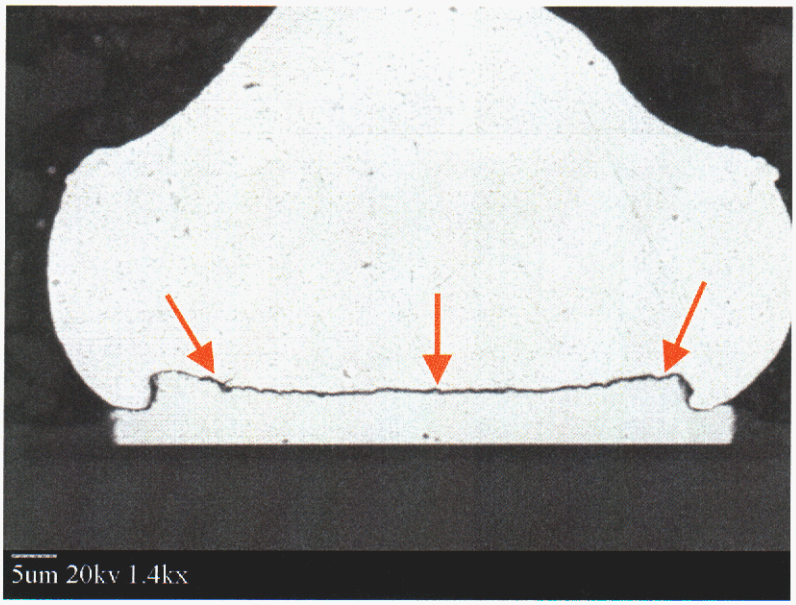

Fig 15. SEM section micrograph of the crack at a gold ball-bond on a failed MMBT2907 part after 1500 h of HAST exposure. The weak Au-Al intermetallic occurs at the top of the intermetallic region, as shown.(from ASI)

In CSAM we observed progressively increasing delamination as the HAST time increased. After the first 250 h exposure only moderate die paddle delamination was seen. No lead finger delamination was evident. At 500 h there was increased die paddle delamination with some initiation of lead finger delamination at the finger perimeters. No "JEDEC" level failures were observed[10]. The severity of the delamination appeared to relatively constant after 750 h of HAST.

A representative set of CSAM images for the first 1250 h of HAST is shown in Fig 16.

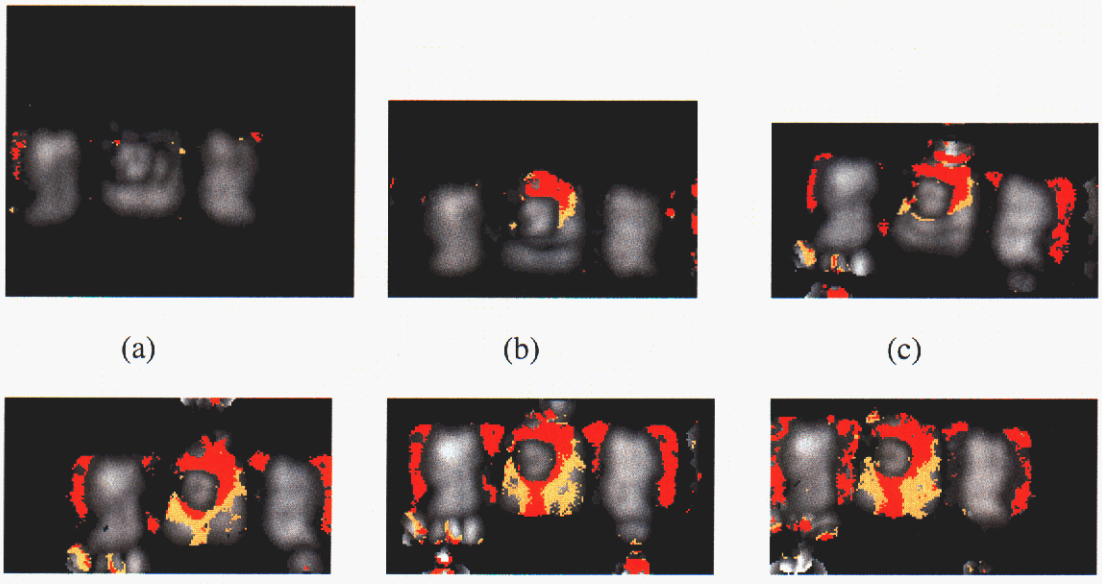

Fig 16. Successive HAST CSAM images for an MMBT/2N2222 part, part # 28. (a) – initial measurements, (b) 250 h, (c) 500 h, (d) 750 h, (e) 1000h, (f) 1250 h.

D. Temperature cycling following HAST

The utility of performing a sequential HAST-temperature cycling test has been discussed by a group at the US Army Aviation and Missile Command (AMCOM) [18]. The idea is that the HAST can produce weakened wire bonds, such as the ones we observed in the HAST experiment discussed above. The subsequent temperature cycling can then potentially break the weakened bonds and produce electrical open circuit failures. In an attempt to evaluate the sequential testing, we took survivor parts from the HAST and subjected them to –65 to +150°C temperature cycling. All of the parts starting the TC had survived 1750 h of HAST at 130°C/85% RH at 48 V bias. The parts were tested electrically after 100, 300, and 500 temperature cycles. The results are shown in Table 1.

Table 6. Results form the temperature cycling following 1750 h of HAST

Package Type	**PEMs/SOT23**		**CHP/LCC**	
Part Number, Type	MMBT 2907 PNP	MMBT 2222 NPN	HS 2907 PNP	HS 2222 NPN
Parts in Test	32	44	48	43
100 cycles	No fail	No fail	No fail	No fail
300 cycles*	2 fail	1 fail	No fail	No fail
500 cycles	1 fail	No fail	1 fail	1 fail

* After 300 cycles, 5 passing parts of each type were sent for decap/delid and bond pull testing. The PEMs parts were all observed to have degraded bond strength accompanied by Au-Al intermetallic formation. The CHP parts all had acceptable bond strength with no evidence of Al corrosion or other bond degradation of the Al-Al wire bonds.

It is interesting to note that no failures were observed after 100 temperature cycles. The AMCOM procedure for PEMs qualification to meet "general missile program requirements" suggests 100 temperature cycles, -55 to +125°C [18]. After 300 cycles several PEMs failures were observed and after 500 cycles, two CHP electrical failures occurred. These were determined to be a result of electrical overstress and are not considered to be valid failures. No evidence of Al corrosion or lifted bonds was found in the delidded CHPs.

VII. Discussion

No electrical failures were observed in either the temperature cycle or the thermal shock portions of the "Shoot-Out" experiment. The test durations were much longer than those commonly used industrial "Qualification" tests. Electrical measurements were easy because the leads were not damaged during the environmental stressing.

The PEMs parts exhibited an increase in CSAM observed die paddle-mold compound delamination in both temperature cycle and thermal shock. It would appear that the cyclical thermal stresses produce this delamination at the weakest interface in the package. There was no evidence of die surface delamination nor was delamination observed in the lead-tip region of the lead frame.

In the HAST portion of the experiment we observed some electrical failures for both types of packaging and both PNP and NPN transistor types. The only valid or HAST produced failures occurred for the PEMS MMBT2907 PNP parts. The first failure is presumed to have occurred sometime in the aging interval 1000 – 1250 h. A plot of the cumulative failure fraction vs. aging time together with a fitted lognormal distribution function is shown in Fig 17. The fitted lognormal distribution is characterized by two parameters; t_{16} and t_{50}, the times to 16% and 50% failure fractions, respectively. For the fitted line t_{16} = 1424 h and t_{50} = 1849 h.

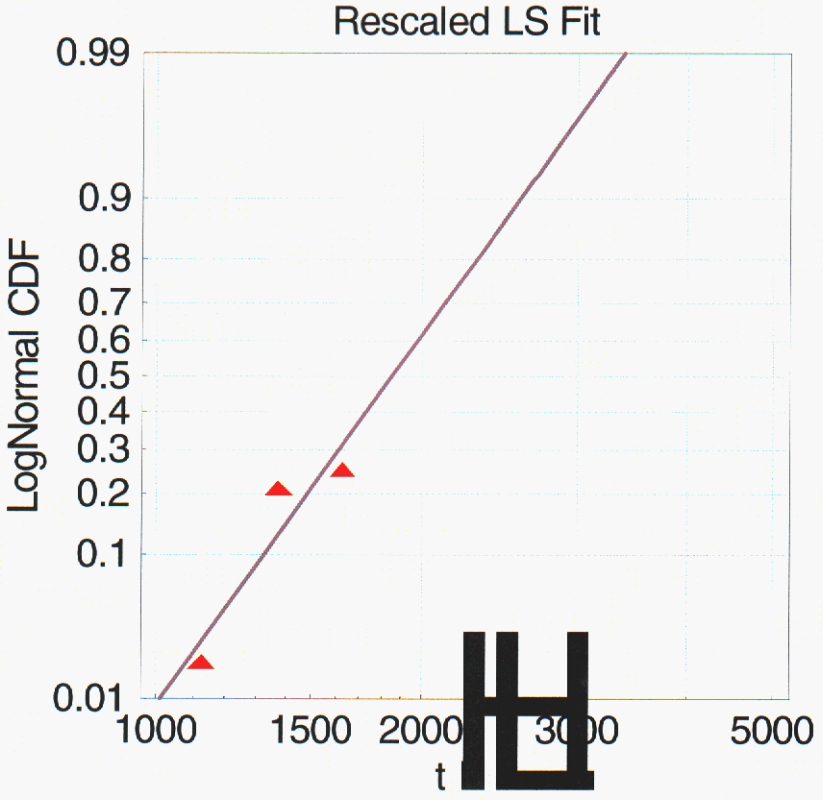

Fig 17. Data points and fitted lognormal distribution function for the failure cumulative distribution function for the MMBT2907 parts after 130°C/85% RH HAST exposure with

a bias of –48 V. The fitted lognormal distribution is characterized by two parameters; t_{16} and t_{50}, the times to 16% and 50% failure fractions, respectively. For the fitted line t_{16} = 1424 h and t_{50} = 1849 h.

In the sequential HAST-temperature cycling test we did not observe any PEMs failures after 100 cycles. A few failures were observed at 300 and 500 cycles. It is possible that the small number of failures was a result of the small die size of the MMBT devices. The shear stress on the wire bonds at the die perimeter increases with die size and so the sequential test would be expected to be more effective for PEMs with larger IC die. However, our result does show that a sequential HAST-TC test is not universally effective in producing failures in PEMs which have weakened Au-Al wire bonds after the HAST portion.

VIII.Lifetime predictions

A. Temperature cycling

The temperature cycling and thermal shock results suggest that either type of package will survive in the intended application. For example, our baseline temperature cycling requirement is one cycle per day from 16 to 43°C, corresponding to a $\Delta T = 26C°$. In the temperature cycle testing we used an accelerated test temperature difference, $\Delta T_{at} = 215C°$. Frequently a Coffin-Manson relationship is used to estimate cycles to failure N_f at use conditions for the measured cycles to failure at accelerated test conditions [19],[20]. The Coffin-Manson relation for the number of temperature cycles to failure when the temperature difference is ΔT has the form,

$$N_f(\Delta T) = C_0(\Delta T)^{-n}, \tag{1}$$

where C_0 is a constant, and n is a constant such that $n \geq 1$. This is a simple relation or compact model that is frequently applied to fatigue phenomena in metals [21]. It is not clear whether thermal cycling induced failures in electronic packages can be adequately described by Eq.(1), but this is the simplest commonly used relation that depends on only one parameter, the cycle temperature difference, ΔT.

When there are data for the cycles to failure, $N_f(\Delta T_{accel})$, from an accelerated temperature cycling test conducted with a temperature difference ΔT_{accel}, then the number of cycles to failure at use conditions, with a temperature difference ΔT_{use} can be calculated from the relation derived from Eq.(1),

$$N_f(\Delta T_{use}) = N_f(\Delta T_{accel})\left(\Delta T_{accel}/\Delta T_{use}\right)^n \tag{2}$$

A conservative lower estimate of the Coffin Manson exponent is $n \approx 1.5$. This is the lowest value listed in a table of Coffin Manson exponents given by Livingston[20] characterizing a number of different mechanisms. Our estimate of the failure probability at accelerated conditions is derived from the observation that 100 of our PEMs components survived 5000 accelerated temperature cycles without failure. We then postulate that the first failure would have occurred 10% later in time or at 5500 cycles. Using the Coffin-Manson law with the ratio $\Delta T_{at}/\Delta T_{use} = 215/26 = 8.3$,

we find the number of cycles to 1% failure at use conditions, $N_f = 5000x(8.3)^{1.5} = 119560$ cycles or 327 y. This is a factor of 10 greater than our required lifetime for the application.

There is also a question as to whether the temperature cycling frequency has an effect on the number of cycles to failure. In the case of solder fatigue it has frequently been found that low cycle fatigue in use conditions is sometimes more severe than high cycle fatigue at accelerated test conditions. Lau suggests that fatigue in use relative to fatigue in accelerated tests is accelerated by the factor [22],

$$N_f(\nu_{use}) / N_f(\nu_{accel}) = \left(\nu_{use} / \nu_{accel} \right)^m , \quad (3)$$

where ν_{use} is the cycling frequency at use conditions, ν_{accel} is the cyling frequency at accelerated test conditions, and m is a constant with a value $m \approx 0.33$. In our case, $= \nu_{use}$ 1 cycle/day and $\nu_{accel} \leq 24$ cycle per day[7]. These values, when inserted in Eq.(3), produce an acceleraton by a factor of 0.35 and reduce the predicted time to failure from 327 y to 114 y.

B. Temperature and humidity

The HAST results can also be used to predict the PEMs lifetime in an application[23], [24]. In the SNL developed application discussed in Refs. 23 and 24, The stockpile to target sequence(STS) temperature and humidity environment is represented by a number of discrete and periodic events, each of which has an associated temperature and relative humidity. The temperature and humidity aging model has two parameters, the humidity exponent n and the thermal activation energy E_a which are not precisely known. As a result, we treat them as random variables in a Monte Carlo analysis. Conservative distribution functions have been utilized for these two parameters. The calculation is most sensitive to E_a. For E_a we used a triangular distribution with values in the range 0.6 – 0.8 eV and a peak value at 0.7 eV. This E_a distribution is consistent with the values reported by Harmon[17] and with the recent measurements by Sorenson et. al[15] for Au-Al intermetallic formation in Au wire-Al bondpad systems.

The last random variable is the time to failure for given values of the lognormal distribution parameters, t_{16} and t_{50}. The STS used for the analysis is a model SLBM environment which we have "postulated" for our early PEMs aging analyses. The model does not account for either voltage acceleration or finite diffusion time effects characterizing moisture diffusion into the plastic mold compound. Inclusion of these effects would make the predicted lifetime longer than that from obtained from our current model.

A result for the predicted lifetime of the MMBT2907 parts is shown in Fig 18. This represents a run with 10,000 trials in order to obtain sufficient accuracy at the low failure fraction(early time) tail of the distribution. The predicted time to 0.1% failure is 47 y and the predicted time to 0.01% failure is 36 y.

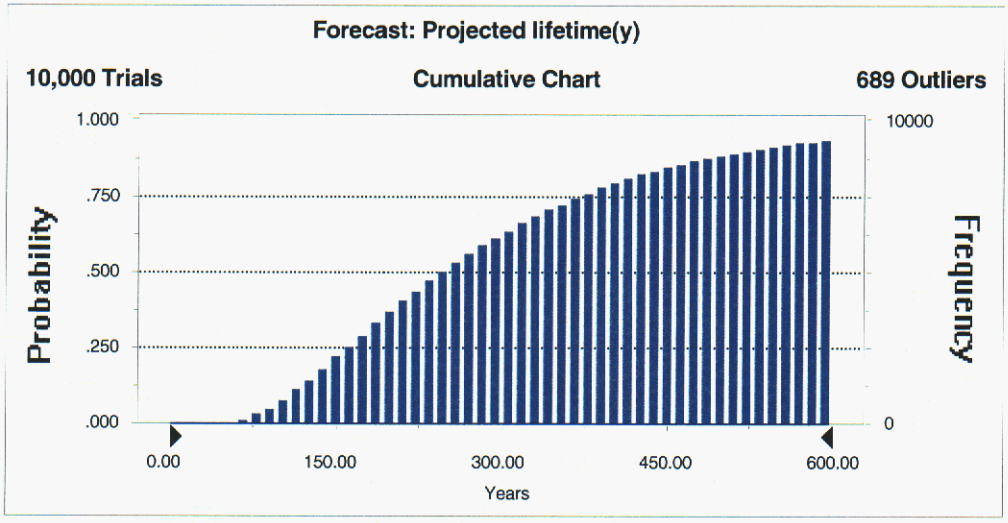

Fig 18. Predicted time to failure for the MMBT2907 PEMs transistor in the model SLBM STS. The median predicted time to failure is about 250 y. The predicted time to 0.1% failure is 47 y.

IX. Conclusions

One major conclusion of this investigation is that there is no significant difference between the PEMs and the CHP transistors in extended temperature cycling and thermal shock testing. In the temperature cycling and shock legs, the test results are conclusive, as no known experimental errors were encountered. The stressing was performed on unbiased parts and the stress conditions produced no artificial damage to the package leads which could influence electrical testing or lead to EOS failures.

In the case of the HAST part of the experiment we detected no HAST induced failures in the CHP parts and the MMBT2222 PEMs parts after a prolonged exposure at 130°C and 85% RH with 48 V reverse bias. In the case of the MMBT2907 PEMs parts, we did observe "valid" HAST induced failures which started in the interval 1000 - 1250 h. However, the failure distribution function estimated from the data when used in our PEMs T&RH aging model, led to a prediction of a sufficiently long life for our application. The HAST portion of the experiment was the most difficult because corrosion of the package leads led to many EOS failures, both in HAST biasing and in electrical testing. This lead corrosion is an artifact of the experiment and would not affect a lead of a part soldered to a PWB.

The sequential HAST-TC experiment showed that 100 temperature cycles at a MILSTD 883 condition C level did not produce PEMs failures, even with parts that had degraded bond strength from the HAST portion. Hence, it is difficult to say whether or not sequential testing should be part of a general PEMs qualification program, as suggested by AMCOM.

The CHP transistors with their HSOT LCC package have a short predicted solder fatigue lifetime relative to the PEMs SOT23 transistors. Hence, there is probably not any increase in overall PWA level reliability found by using the CHP parts in place of the PEMs parts. This conclusion

is based on the observation that there was no observable difference in the component level reliability between the two types of packaging in our extended environmental testing.

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