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G. Caporaso
D. Goerz
R. Hanks
B. Hickman
H. Kirbie
B. Lee
C. Brooksby
R. Saethre

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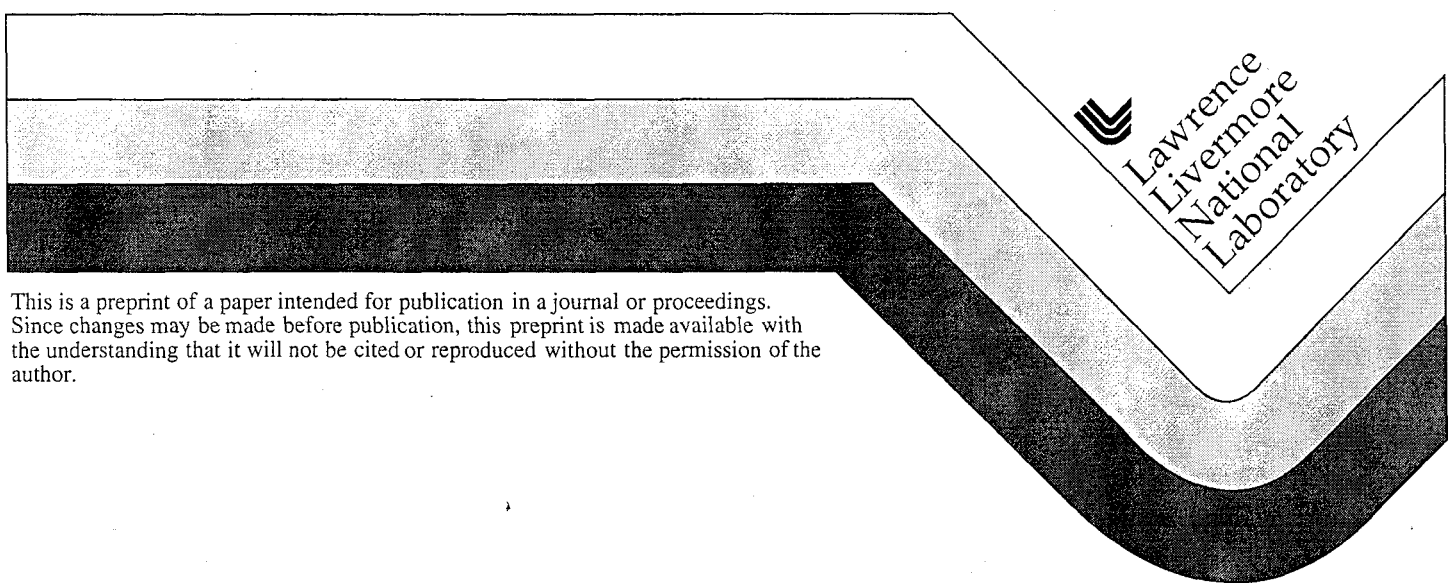

MHZ REPETITION RATE SOLID-STATE DRIVER FOR HIGH CURRENT INDUCTION ACCELERATORS*

G. Caporaso, D. Goerz, R. Hanks, B. Hickman, H. Kirbie, B. Lee,
Lawrence Livermore National Laboratory, Livermore, CA
C. Brooksby, R. Saethre, Bechtel Nevada, Livermore, CA

Abstract

A research team from the Lawrence Livermore National Laboratory and Bechtel Nevada Corporation is developing an all solid-state power source for high current induction accelerators. The original power system design, developed for heavy-ion fusion accelerators, is based on the simple idea of using an array of field effect transistors to switch energy from a pre-charged capacitor bank to an induction accelerator cell. Recently, that idea has been expanded to accommodate the greater power needs of a new class of high-current electron accelerators for advanced radiography. For this purpose, we developed a 3-stage induction adder that uses over 4,000 field effect transistors to switch peak voltages of 45 kV at currents up to 4.8 kA with pulse repetition rates of up to 2 MHz. This radically advanced power system can generate a burst of five or more pulses that vary from 200 ns to 2 μs at a duty cycle of up to 25%. Our new source is precise, robust, flexible, and exceeds all previous drivers for induction machines by a factor of 400 in repetition rate and a factor of 1000 in duty cycle [1].

1 INTRODUCTION

We are developing a radiographic concept for Stockpile Stewardship that is based on a single, high-current induction accelerator driven by solid-state power. The accelerator will produce bursts of 16–20 MeV, 3–6 kA electron beams in long pulses that may vary from 200 ns to 2 μs. Each beam will be cleaved by an electromagnetic "kicker" device that directs the divided beam portions down separate pathways [2]. The chopping action of the kicker may be repeated on the remaining portions of the beam until the desired number of beam segments arrive at a test chamber where they are converted into x-ray sources for radiography. The solid-state driven accelerator enables the viewing process to be repeated at rates exceeding a megahertz while resetting the magnetic material in each accelerator core between pulses. Further information about this and other advanced radiographic methods for Stockpile Stewardship is available in the literature [3].

The two power sources illustrated in Figure 1(a) are inductive voltage adders that sum the voltage contributions from three solid-state modulators. The output voltage from the adders is multiplied by three at the accelerating gap due to the transformer action of three induction cores within the cell. Figure 1(b) is a conceptual design of a three-core cell. Details concerning the operation of an induction accelerator and the behavior of a multicore cell can also be found in the literature [4,5]. Figure 2(a) depicts the basic elements of our prototype induction adder which contains three ARM-II solid state modulators surrounding a voltage summing stalk. When stacked together, the modulators act as independent pulse transformers linked by a common secondary winding.

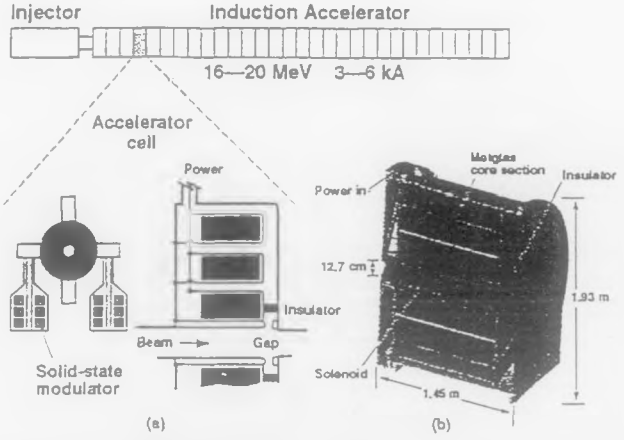

Figure 1: (a) Illustration of a solid-state power system for an induction accelerator. (b) Computer design of a long-pulse, three-core induction cell.

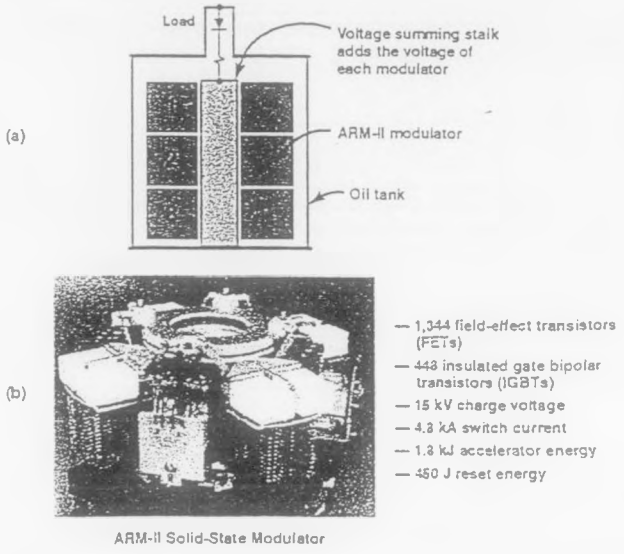

Figure 2: (a) Simple diagram showing the internal elements of a three-stage voltage adder plus (b) a photograph and specifications for an ARM-II solid-state modulator.

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2 ARM-II MODULATOR

The ARM-II modulators each contain four 20-kV, 4-μF capacitor banks that are switched across a tape-wound magnetic core using a modular array of field-effect transistors (FETs). Each modulator also contains a reset system that uses insulated gate bipolar transistors (IGBTs) to switch four 10-kV, 4-μF capacitor banks across the same magnetic core. The goal of the reset system is to control the magnetic states of the modulator and accelerator cell so that a long burst of pulses can be sustained without saturating the magnetic core material.

Figure 3(a) is a simplified circuit diagram of an ARM-II modulator. When the FETs are commanded to close, the 15-kV capacitor voltage appears across the induction core and remains there until the FETs are opened. At that time the core voltage reverses and is held at the 7.5-kV level by the IGBT switches. One should note that the core is loaded by a 3-Ω resistor in series with a diode which acts to load the modulator during the acceleration pulse (negative) but not during the reset pulse (positive). The polarity-dependent loading imitates the effect of an electron beam that is present during acceleration but not during reset. Figures 3(b)–(d) are modulator test data showing a 2-μs pulse. Figure 3(b) shows a voltage waveform with the reset pulse adjusted to match the volt-second value of the acceleration pulse (flux balanced). Figure 3(c) is an expansion of the acceleration pulse showing that the core voltage is well shaped but less than 15 kV due to the 0.75-Ω on-state impedance of the FET array.

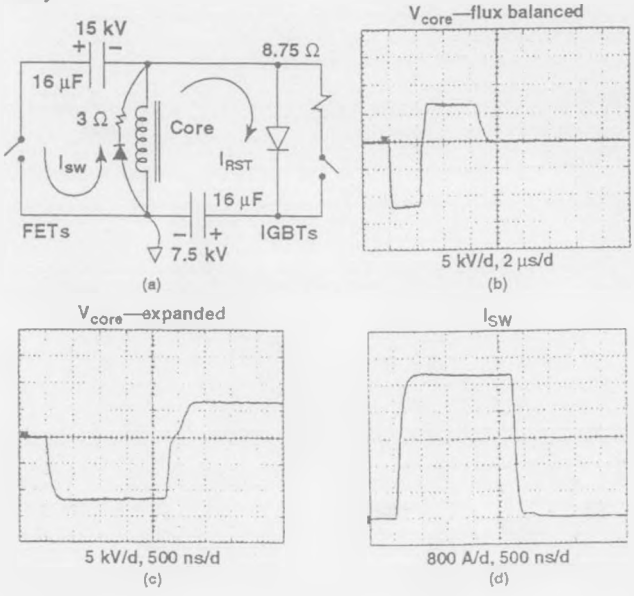

Figure 3: ARM-II performance data showing (a) an idealized ARM-II circuit diagram with (b), (c) voltage wave forms and (d) total FET switch current.

3 INDUCTION ADDER AND CABLE-COUPLED POWER

The ARM-II modulators are built to stack on top of each other as shown in Figure 4.

Figure 4: Adder photograph showing three ARM-II modulators.

Voltage from each modulator is gathered by a voltage-summing stalk and delivered to a set of 50-Ω cable connections that enable us to power an accelerator cell at some remote location. Unfortunately, we have no long-pulse electron beam to accelerate nor a large three-core induction cell, as previously shown. What we have managed to do is scale the original concept, shown in Figure 1(a), down to the power level of the prototype adder, which is able to drive the smallest of the three accelerator cores shown in the figure. The loading effect of a small core, combined with an electron beam, is modeled by the simple network shown in Figure 5(a). In this model, the capacitor represents the lumped effect of the gap, gap insulator, and oil-cavity capacitances. The inductor accounts for the unsaturated inductance of the core while magnetization losses in the core during acceleration are attributed to one of the five 50-Ω resistors. The remaining four 50-Ω resistors imitate the loading effect of a 2.8-kA electron beam. The 110-Ω resistor and reversed diode embody the magnetization losses in the core during the reset pulse. Figure 5(b) shows the oil-immersed cell model connected to the adder via 50-Ω, high-voltage cables.

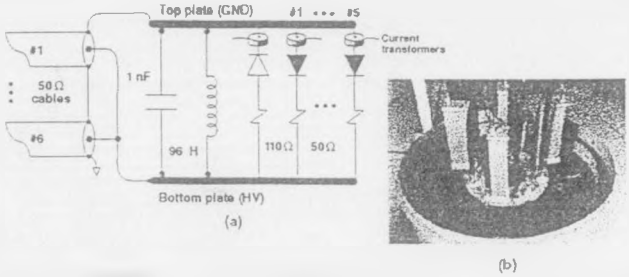

Figure 5: (a) Lumped-element model of an accelerator cell and beam load that is scaled to match the prototype adder and (b) photograph of the lumped-element network connected to the adder for tests.

Figure 6 shows the voltage and current response of the cell model to a burst of 1-μs pulses at a pulse rate of 200 kHz. The adder is adjusted to provide the appropriate amount of reset voltage after each acceleration pulse. Figure 6(c) compares cell voltages for the first and fifth pulses, which shows a voltage drop on the fifth pulse due to capacitor bank droop. Later versions of the adder will eliminate this effect by actively regulating the adder output voltage to the value of the last pulse. The FET switch currents in Figure 6(d) show a peak value of 4.3 kA. Figure 7 illustrates the great flexibility that solid-state power affords an induction accelerator by showing a pulse schedule that changes from pulse to pulse. One should note that the final long pulse (or long burst) avoids saturation by controlling the reset conditions of earlier pulses.

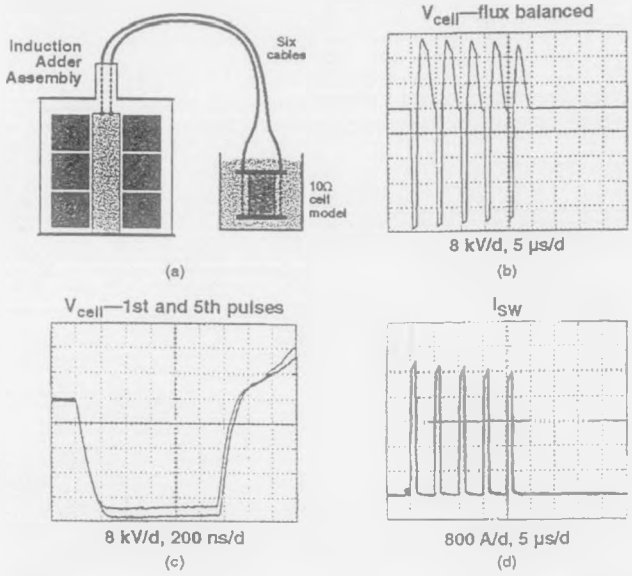

Figure 6: 200-kHz burst data showing (b) five voltage pulses with active reset, (c) comparison of first and fifth voltage pulse at the cell, and (d) burst of FET current pulses with a peak value of 4.3 kA on the first pulse.

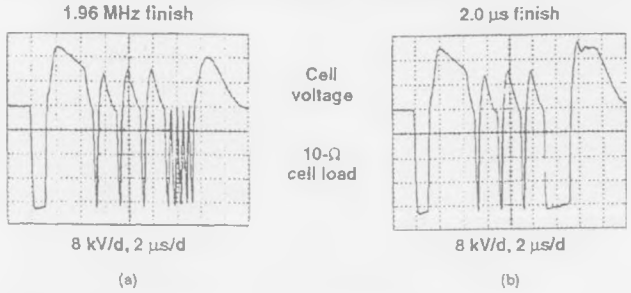

Figure 7: An arbitrary pulse schedule showing (a) cell voltage for a pulse train that finishes with five, 200-ns pulses at 1.96 MHz, and (b) cell voltage showing a pulse train that finishes with a 2-μs pulse.

Figure 8 compares a network simulation of the cell voltage with measured data. The network simulation uses linear circuit elements to model the three-stage adder, power transmission lines, and lumped-element cell. The experimental and simulation data are both processed with a 20-MHz bandwidth filter. We believe the agreement between simulation and experiment is close enough to use the simulation as a design tool for future experiments.

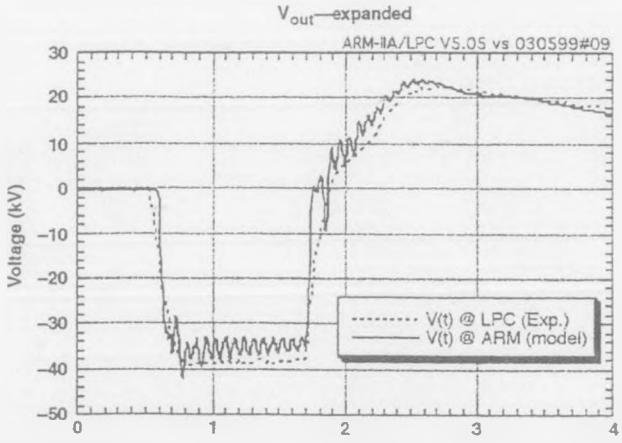

Figure 8: Comparison between measured and simulated cell voltages.

4 SUMMARY AND OUTLOOK

Experiments involving an all solid-state voltage adder and lumped-element cell model have demonstrated the feasibility of powering a high current induction accelerator at pulse rates beyond a megahertz. Further encouragement for solid-state accelerator power is provided by electronic manufacturers who produce devices that continue to increase in speed and power while falling in cost. For example, the estimated cost of powering the accelerator depicted in Figure 1(a) has fallen by a factor of five since work began on the ARM-II modulator. Our latest estimates indicate that solid state power is approaching the cost of conventional accelerator power but with much greater performance and flexibility.

5 REFERENCES

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