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High Performance Electrical Modeling and Simulation Software Normal Environment Verification and Validation Plan, Version 1.0

Steven D. Wix, Carolyn W. Bogdan, Mike F. Deveney, Julio P. Marchiondo and Albert V. Nunez

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Abstract

The requirements in modeling and simulation are driven by two fundamental changes in the nuclear weapons landscape: (1) The Comprehensive Test Ban Treaty and (2) The Stockpile Life Extension Program which extends weapon lifetimes well beyond their originally anticipated field lifetimes. The move from confidence based on nuclear testing to confidence based on predictive simulation forces a profound change in the performance asked of codes. The scope of this document is to improve the confidence in the computational results by demonstration and documentation of the predictive capability of electrical circuit codes and the underlying conceptual, mathematical and numerical models as applied to a specific stockpile driver. This document describes the High Performance Electrical Modeling and Simulation software normal environment Verification and Validation Plan.

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List of Acronyms

AF Arming and Fuzing
ASCI Accelerated Strategic Computing Initiative
BJT Bipolar Junction Transistor
COTS Commercial Off-The-Shelf
CVS Concurrent Versions System
DoD Department of Defense
DOE Department of Energy
DP Defense Programs
eCIS Enterprise Component Information System
FPGA Field Programmable Gate Array
HPEMS High Performance Electrical Modeling and Simulation
IC Integrated Circuit
M&S Modeling and Simulation
NEP Nuclear Explosives Package
PCB Printed Circuit Board
PIRT Phenomena Identification and Ranking Table
RF Radar Frequency
SLEP Stockpile Life Extension Program
SNL Sandia National Laboratories
SPUDS Sandia Parts Unified Data System
SQE Software Quality Engineering
STS Stockpile-to-Target-Sequence
TREE Transient Radiation Effects in Electronics
UGT Underground nuclear Testing
V & V Verification and Validation
VALTS Validation Test Suite
VERTS Verification Test Suite
WRCIP War Reserve COTs Insertion Process

Introduction

Accelerated Strategic Computer Initiative (ASCI) application codes are key components in reaching the 2010 Stockpile Stewardship and Management Program objectives at an affordable cost and without nuclear testing. The High Performance Electrical Modeling and Simulation (HPEMS) ASCI project will develop the high performance software applications needed for characterizing and evaluating weapon electrical systems as computing replaces underground nuclear testing (UGT). It is a formidable challenge to replace the empirical factors and adjustable parameters used in current calculations with predictive physical models. This challenge will produce large, complex applications that will drive the scale of computing machinery.

The requirements in modeling and simulation (M&S) are driven by two fundamental changes in the nuclear weapons landscape: (1) The Comprehensive Test Ban Treaty and (2) The Stockpile Life Extension Program (SLEP) which extends weapon lifetimes well beyond their originally anticipated field lifetimes. The move from confidence based on nuclear testing to confidence based on predictive simulation forces a profound change in the questions asked of codes.

Scope

Ensuring the correctness and reliability of ASCI codes must be an essential goal if simulation is to be useful and acceptable. As simulation codes become more complex, however, it will become increasingly difficult to verify that the simulation results accurately reflect correct physical phenomenon. In addition, as the software projects increase in size, it will become critical to employ the latest techniques in software engineering to produce accurate, reliable, and maintainable software.

Due to the increased dependence on computational simulations when making stockpile judgments, the uncertainties associated with these calculations will need to be reduced. These uncertainties arise from many sources such as errors in coding, inadequate approximations, physical processes not represented in the code, and user errors. The scope of this document is to improve the confidence in the computational results by demonstration and documentation of the predictive capability of electrical circuit codes and the underlying conceptual, mathematical and numerical models as applied to a specific stockpile driver.

This HPEMS project is developing two classes of electrical simulation codes. The circuit codes, Xyce and ChileSPICE, simulate electronic circuits containing analog active and passive devices. The device code, Devi, simulates analog active devices at the semiconductor junction level. Devi is a long-term effort and is not addressed in this plan. An HPEMS project goal is to couple the circuit and device codes as well as other ASCI codes that will predict environmental effects. The scope of this V&V plan is applicable to verification and validation efforts associated with the Xyce circuit code. This plan is also applicable to the ChileSPICE circuit code.

The Stockpile-to-Target-Sequence (STS) under normal environments for components of weapon systems includes the performance of all weapon components, except the Nuclear Explosives package (NEP), in the intended use of a weapon. This environment includes the storage and transportation of the weapon system. Validated modeling and simulation capabilities are required for design and certification of re-entry vehicles under normal environments. Reduced testing capability for experimental determination of normal environment effects on the weapon necessitates much higher fidelity models. Massively parallel implementation of modeling and simulation capabilities is required to meet the expectations for memory and CPU usage of these larger models.

The overarching stockpile driver for the HPEMS project is to simulate the entire electrical portion of a weapon system in all the environments the weapon can encounter. This driver is too large to attempt at this time. The electric circuit codes and models required to achieve simulation of a weapon system in the normal, hostile and abnormal environments are not yet fully developed. Therefore, the HPEMS project will address smaller pieces of the overarching stockpile driver and therefore have a separate V&V plan for each of these pieces.

V&V Planning Process

This plan will follow the "Guidelines for Sandia ASCI Verification and Validation Plans" document, version 2.0. [Pilch] The main content areas are (1) stockpile requirements; (2) key phenomena to be modeled by the code as identified in the PIRT (Phenomena Identification Ranking and Table); (3) software quality engineering (SQE); (4) verification test plan; and (5) code validation test plan. Figure 1 displays the process flow map for the HPEMS V&V Process and the associated inputs.

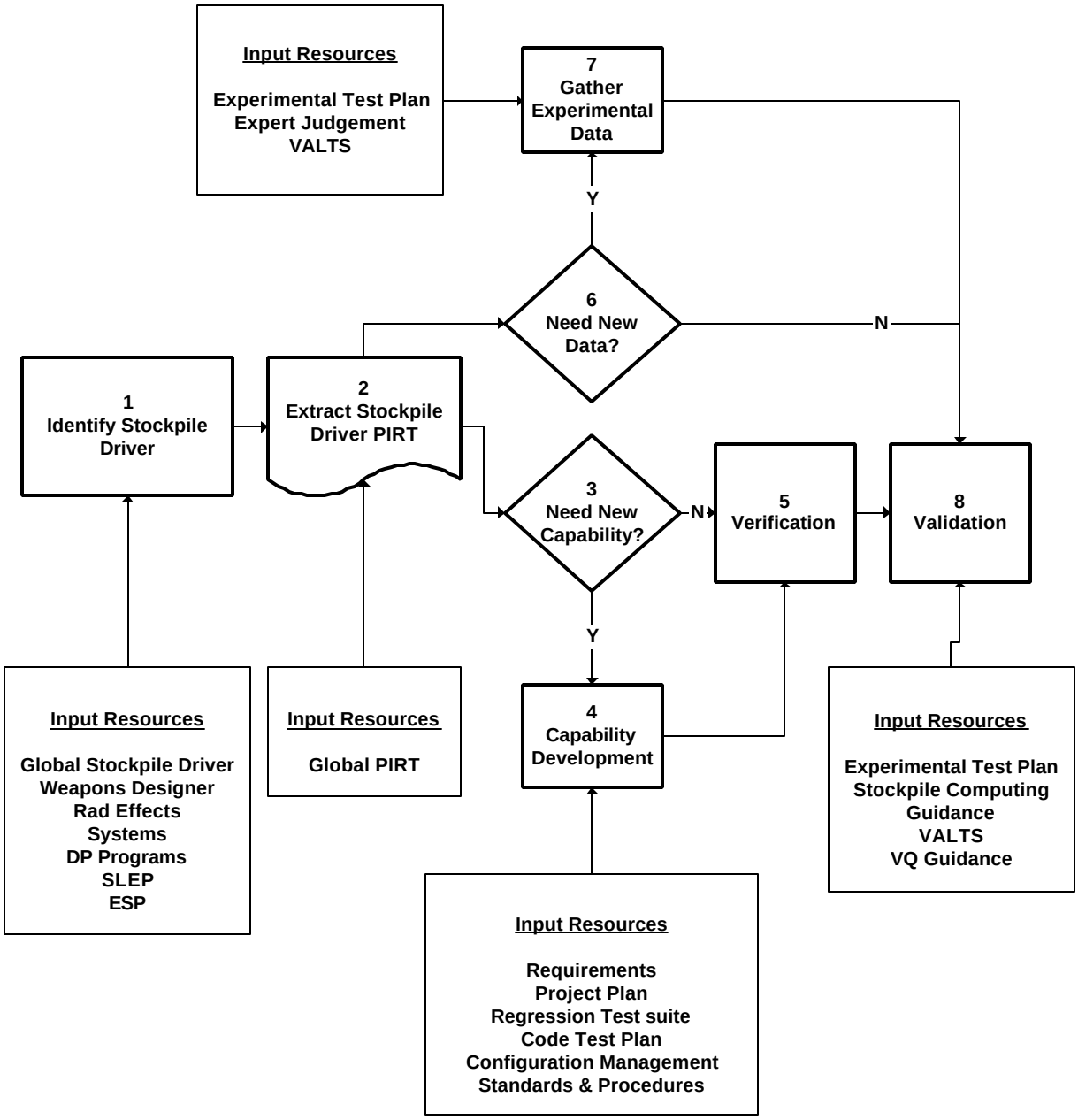

FIGURE 1 - V&V PLANNING PROCESS FLOW

The V&V planning process begins with the identification of a stockpile driver. The identification of the stockpile driver occurs by reviewing the Global Stockpile Driver list and through coordination with Defense Program (DP) customers and by identification, examination and prioritization of external drivers such as the SLEP and the Albuquerque Workload Planning Guidance (AWLPG 99-0). Identification of the stockpile driver requires a high degree of coordination, teamwork and concurrence between all

stakeholders. The ASCI V&V Guidelines [Pilch] are used in the selection of an appropriate stockpile driver.

The next step, Step 2 in Figure 1, in the process is the construction of the V&V plan specific PIRT. We have chosen to develop a Global PIRT to encompass as many of the phenomena associated with electrical simulation as possible. As electrical modeling and simulation matures and the understanding of the physics associated with electrical devices is better understood, the Global PIRT is revised as part of the overall development process.

Step 3 asks the question, "Do we need to develop new electrical modeling and simulation capability?" This question is intended to trigger capability development only when needed. A side effect of this question is to minimize the risk of self-induced bugs in software. If the capability does not need to be modified to perform the modeling and simulation needs of a specific stockpile driver, then the software is not modified.

Step 4, Capability Development, occurs only if Step 3 is answered "Yes". Step 4 consists of all software development activities associated with a specific V&V plan. Activities include all SQE practices, such as software verification and validation, software engineering, and project management, requirements capture, code development, and build/release.

Step 5, Verification, is the verification of the model associated with the stockpile driver identified in Step 1. Per the definition in the ASCI V&V Guidelines [Pilch], verification is defined as

> **Verification** – The process of determining that a computational software implementation correctly represents a model of a physical process,

and informally as

Verification – The process of determining that the equations are solved correctly.
Verification activities include development of a stockpile driver based Verification Test Suite (VERTS) which is derived from a Global VERTS, development of the verification test plan, verification testing, assessment of underlying mathematical models, construction of appropriate stockpile driver based success metrics, and analysis of the results of the verification testing.
Step 6 asks the question, "Are new experimental data needed for validation activities?" Similar to the question asked in Step 3, this question is intended to trigger experimental efforts only when needed. An evaluation of the existing experimental data is performed during this step to answer the question.

If the answer to Step 6 is "Yes", then Step 7 is initiated. Step 7 consists of activities associated with gathering experimental validation data for a specific stockpile driver. These activities include development of an experimental test plan, determining what experiments can actually be performed, and experimentation.

Step 8, Validation, is the validation of the model associated with the stockpile driver identified in Step 1. Per the definition in the ASCI V&V Guidelines [Pilch], validation is defined as

Validation – The process of determining the degree to which a computer model is an accurate representation of the real world from the perspective of the intended model applications,

and informally as

Validation – The process of determining that the equations are correct.

Validation activities include many processes. These processes are:

- The development of a stockpile driver based Validation Test Suite (VALTS) which is derived from a Global VALTS,
- The development of the validation test plan and validation testing,
- The development of stockpile driver based success metrics,
- Determination of the dependence of code models on experimentally measured quantities,
- Application of uncertainty qualification techniques where appropriate,
- Further experimental investigation if needed, and
- Analysis of the results of the validation testing and stockpile driver based success metrics.

V&V Document Tree

The philosophy of the HPEMS project is to reduce redundancy and duplication of efforts as much as possible regarding V&V plans. This philosophy allows efficient utilization of resources and focus on only what tasks are needed during the V&V process. To reduce redundancy and duplication of effort in each V&V plan, a document tree was developed. Figure 2 presents the document tree for this V&V plan.

The document tree consists of three layers. The uppermost layer is the V&V plan, and this document is an example of such a plan. The middle layer is the reference document layer. Documents such as the Global PIRT, Global VERTS, Global VALTS, ASCI V&V guidance [Pilch] and SQE guidance documents [SNL][Hodges-1][Hodges-2] comprise this layer. The lowest level documents are the actual project documents associated with the V&V plan. Documents at this level include code-specific test plans, project management documentation, code and problem specific VERTS and VALTS, and detailed stockpile computing guidance documents such as code-specific user guides, model data sources and technical guidance.

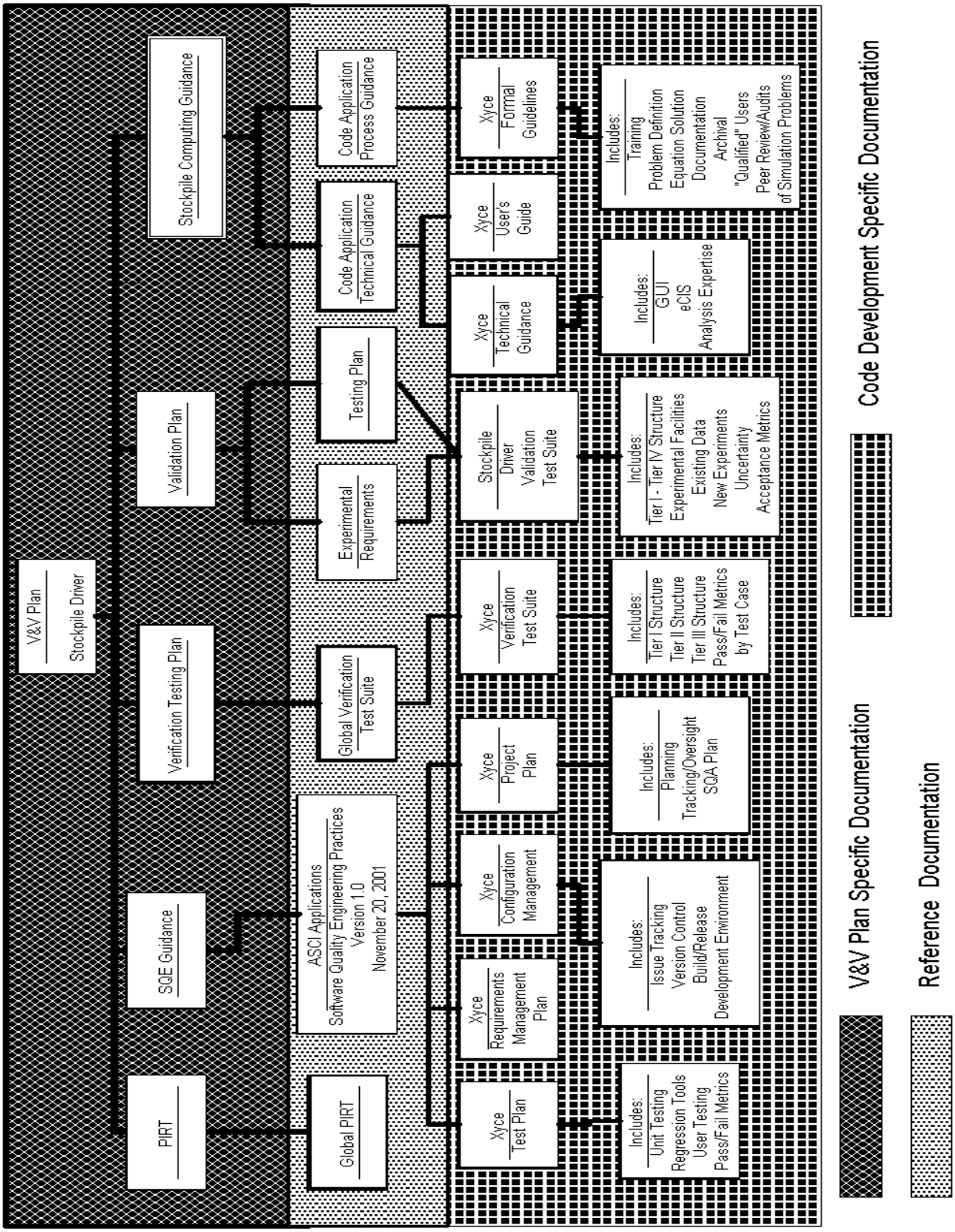

FIGURE 2 - HPEMS V&V DOCUMENT TREE

The document tree presented in Figure 2 reduces redundancy and duplication of effort by reuse of relative documentation. A goal of the document tree is to allow rapid construction of a V&V plan for a specific stockpile driver. The desire is to reduce the page count of the body of a V&V plan to 10-15 pages. A similar tree exists for ChileSPICE.

Stockpile Drivers and DP Customer Requirements

Introduction

In a future that precludes UGTs and emphasizes reducing costs, it will become increasingly important to first introduce a firm physic understanding of device and circuit effects into the certification equation. This "up-front" understanding and the new code capabilities that will follow should dramatically reduce the time and cost to realize the new electronic and optical devices required for future weapon upgrades.

The STS under normal environments for components of weapon systems includes the performance of all weapon components, except the NEP, in the intended use of a weapon. This environment includes the storage and transportation of the weapon system. Validated modeling and simulation capabilities are required for design and certification of re-entry vehicles under normal environments. Reduced testing capability for experimental determination of normal environment effects on the weapon necessitates much higher fidelity models. Massively parallel implementation of modeling and simulation capabilities is required to meet the expectations for memory and CPU usage of these larger models.

Stockpile Driver and DP Customer Requirements

The overarching stockpile driver for the HPEMS project is to simulate the entire electrical portion of a weapon system in all the environments the weapon can encounter. This driver is too large to attempt at this time. The electric circuit codes and models required to achieve simulation of a weapon system in the normal, hostile and abnormal environments are not yet fully developed. Therefore, the HPEMS project will address smaller pieces of the overarching stockpile driver and therefore have a separate V&V plan for each of these pieces. This plan is driven by the need to design and certify the electrical system of the W76-1 in the absence of underground nuclear testing and by the FY01 Normal Environment ASCI Milepost Calculation. The W76-1 weapon's arming and fuzing system (AF) is a responsibility of Sandia National Laboratories (SNL) to both the Department of Energy (DOE) and the Department of Defense (DoD). These two DP customers require that SNL certify electrical systems for which we have responsibility for normal, hostile and abnormal STS environments. We want to develop, verify and validate an electrical circuit code, named Xyce, which will be used for design margin analysis in a normal STS environment for the majority of the electrical subsystems in the W76-1 AF. The electrical subsystems that will be simulated in the STS environment are the Main Logic Board, Timer (FPGA) and Radar. Each electrical subsystem is required to function properly through a normal STS temperature range environment. Performing this simulation will aid in the phase 6.3 development for the W76-1. Phase 6.3 is the Development Engineering Phase when the development portion of the

refurbishment program is undertaken. We have to achieve this goal by May 2002 in order to meet our DP customer's phase 6.3 flight test deadline.

To reiterate, the stockpile driver for this V&V plan is the electrical circuit code simulation in a STS environment of the Main Logic Board, Timer (FPGA) and Radar subsystems contained in the W76-1 AF. The DP customers are SLEP, the weapon system designers in SNL departments 2331 (Power and Controller Electronics), 2333 (Radar Fuses), 2612 (Firing Set and Optical Engineering) and 2616 (Firing Set, Fuze and Switch Tube) as well as the reliability engineers in SNL department 8418 (Reliability and Electrical Systems). These subsystems are comprised of different types of unique electrical devices. The M&S requirements for this V&V plan are derived from the Stockpile Driver PIRT. In the PIRT, we have identified the importance of each electrical device type with respect to electrical system performance by environment. The equations and code which model each of these environmental effects must be verified and validated as described in the HPEMS Verification Testing and Validation Plans. The stockpile driver normal STS environment PIRT is in the next section and is used as a reference list for the M&S requirements of this V&V Plan. Our customer's requirement is +/- 20% accuracy for the calculations of these phenomena if the simulation is to make any substantive design impact. Our DP customers provided this accuracy requirement in September 2000 during the planning phase for the electrical simulation portion of the FY01 ASCI Milepost calculation. The +/- 20% accuracy is for design impact, not weapon certification. It is anticipated that the accuracy requirements will increase for future calculations.

Phenomena Identification and Ranking Table

The Phenomena Identification and Ranking Table is the methodology by which the essential physical phenomena are defined. The PIRT ranks the importance of code activity associated with implementing the phenomena and provides the basis for gauging associated fidelity requirements. The PIRT is a logical mapping between stockpile, M&S requirements and prioritized V&V activities.

The PIRT represents in three respects the refined model requirements that result from stockpile requirements. First, the PIRT identifies a set of needed physical phenomena to which code V&V requirements directly map. Second, the PIRT prioritizes the relative importance of the needed physical phenomena to the DP modeling and simulation objectives of the code. Third, the PIRT measures the current and future ability of the code to accurately represent and implement the needed physical phenomena.

Electrical systems are constructed from many independent components. These components are hierarchically grouped into families based on technology, functionality and usage. Examples of family classes are transistors, resistors and capacitors. Within each class, there is a further division into related components. For example, a transistor can be categorized into a bipolar junction transistor, a junction field effect transistor and a metal oxide semiconductor field effect transistor. Each component may have

a different response to the same external environmental stimuli. A BJT (bipolar junction transistor) reacts differently in a radiation field when compared to a resistor response in the same radiation field. The Global PIRT was constructed based on the hierarchy found in electronic components.

A three rank scoring system (H, M, L) was used in development of the Global PIRT. The ranking was performed on a component by component basis. Phenomena were attached to each component and the modeling activities sliced through all components. A scoring of high, medium and low was assigned. The importance of each phenomenon for three different types of modeling activities was ranked. The assignment was performed using the consensus of experts in each phenomenon and with inputs from the DP customers.

The Circuit Code PIRT was extracted from the Global PIRT to specifically meet the stockpile driver requirements of this V&V Plan. Since the Global PIRT listed radiation environments and device code model adequacy, we were able to remove these columns and rows when extracting the stockpile driver specific PIRT for circuit level simulation in a normal STS environment. Therefore, the effects needed in this PIRT are thermal excursions, low dose radiation and model equation functionality. The PIRT systematically identifies physical phenomena required for the modeling and simulation needs of the stockpile driver. These are the phenomena the code must address, formulate, and implement to succeed in its stockpile mission. Each of the electric circuit device models listed in the PIRT must be implemented in the code, have its model equations verified and validated to meet our DP customer's requirements for an accuracy of +/-20%. The phenomena and model adequacy are prioritized in the PIRT.
We already have large quantities of experimental data for different electrical devices such as transistors, diodes and linear IC's (Integrated Circuits). These data are located in a database named Sandia Parts Unified Data Sources (SPUDS) at the following address:

http://www.star.sandia.gov/index.html

The existing data will aid in the validation of many model types, however we will need to extract model parameters for the unique electrical devices contained in the W76-1 Main Logic Board, Timer (FPGA) and Radar subsystems that we are simulating for design margin analysis. The following is an example description of a Tier I test example contained in the HPEMS Verification Test Suite. It is used to simulate and calculate by hand the exact values that verify, or describe mathematically the behavior of the diode and the expected simulator output:

Diode Circuit Netlist
****
* Tier No.: 1
* Description: Simple diode circuit to test the validity of the diode model.
* Input: 5V DC Source
* Output: Diode voltage and current
* Circuit Elements: diode, resistor
* Analysis:

```
*       A diode is forward biased with a 5V source.  With a 100fA saturation
*       current, the diode current and voltage are determined by the following
*       equations:
*               (1) Id=Is[exp(Vd/Vt) - 1]
*               (2) Vin=Id*R + Vd = Is[EXP(Vd/Vt)-1]*R + Vd
*               (3) Vt= k* T/q
*               where,
*               k = Boltzmann's constant = 1.38* 10^-23 J/K
*               T = temperature in degrees Kelvin = 300
*               q = electronic charge = 1.6*10^-19 C
*               Therefore:
*               Vt=25.86mV, and using
*               R=2K, Is=100fA, Vin=5V
*       We substitute equation (1) into equation (2) and solve for the diode voltage Vd.
*       The diode current can be found by solving (2) after Vd is found.
*       Results:
*               Vd=0.6158V  and Id=2.19mA

VIN 1 0 DC 5V
R1 1 2 2K
D1 3 0 DMOD
VMON 2 3 0
.MODEL DMOD D (IS=100FA)
.DC VIN 5 5 1
.PRINT DC I(VMON) V(3)
.OPTION LIST ACCT
.END
```

DIODE SIMULATION OUTPUT:

Diode Circuit Netlist
DC transfer characteristic

Index	voltage_sweep	vmon_branch	v(3)
	VIN	ID	VD
0	5.000000e+00	2.192078e-03	6.158450e-01

Each of the unique devices listed in the PIRT below is verified for each of the environment phenomena listed with similar test circuits that are contained in the HPEMS Verification Test Suite. Please reference this document, named VERTS_Netlists.doc, for further examples at:

\\Wileycoyote\Elec_Sim\V&V Plans\VERTS

Table 1 - Phenomena Identification and Ranking Table

Circuit Code PIRT for Warhead	**Stockpile Drivers**			
Weapon Electrical System Simulation	Importance to Electrical System Performance			Circuit Code Model Adequacy
	Predict Performance	Design Space Exploration	Certification	
A Bipolar Junction Transistor (BJT)				
Functionality	H	H	L	Adequate
Thermal Excursions	M	M	L	Adequate
Low-Dose Rate Radiation	H	M	L	Inadequate
B Junction Field Effect Transistor (JFET)				
Functionality	H	H	L	Adequate
Thermal Excursions	M	M	L	Adequate
Low-Dose Rate Radiation	H	M	L	Inadequate
C Metal Oxide Semiconductor Field Effect Transistor (MOSFET)				
Functionality	H	H	L	Adequate
Thermal Excursions	M	M	L	Adequate
Low-Dose Rate Radiation	H	M	L	Inadequate
D Diode				
Functionality	H	H	L	Adequate
Thermal Excursions	M	M	L	Adequate
Low-Dose Rate Radiation	H	M	L	Inadequate
E Zener Diode				
Functionality	H	H	L	Adequate
Thermal Excursions	M	M	L	Adequate
Low-Dose Rate Radiation	H	M	L	Inadequate
F Resistor				
Functionality	H	H	L	Adequate
Thermal Excursions	M	M	L	Adequate
Low-Dose Rate Radiation	H	M	L	Inadequate
G Capacitor				
Functionality	H	H	L	Adequate
Thermal Excursions	M	M	L	Adequate
Low-Dose Rate Radiation	H	M	L	Inadequate
H Inductor				
Functionality	H	H	L	Adequate
Thermal Excursions	M	M	L	Adequate

Circuit Code PIRT for Warhead	**Stockpile Drivers**			
Low-Dose Rate Radiation	H	M	L	Inadequate
Integrated Circuit Boards				
Board Parasitic Effects	H	H	L	Inadequate

Software Quality Engineering

Software quality engineering practices are required to achieve confidence in results generated with computer codes. The software must be designed so that results are defensible, traceable, and reproducible. Design activities must include repeatable methods for translating requirements information and models (scientific and software) into representations that convey software data structure, architecture, algorithms, and interface features.

Software Quality Engineering (SQE) is an important contributor to establishing the confidence in the calculations associated with the stockpile driver described previously. Guidance for SQE activities is provided in the ASCI and Sandia National Laboratories SQE documents [SNL] [Hodges-1] [Hodges-2] documents. The following table lists the SQE documents that HPEMS has developed, many of which are referenced in the HPEMS V&V Document Tree. The same SQE documents also apply to ChileSPICE.

Table 2 – SQE Documents Referenced in the HPEMS V&V Document Tree

SQE Documents		
Document Name	Draft Copy Exists	Final Copy/SAND Report Exists
HPEMS Project Plan	Y	N
Xyce Project Plan	Y	N
Xyce Configuration Management Plan	Y	N
Xyce Code Requirements Management Plan	Y	N
Xyce Code Test Plan	Y	N
Xyce Verification Test Suite (VERTS) Plan	Y	N
HPEMS VERTS	Y	N
Stockpile Driver Validation Test Suite (VALTS) Plan	N	N
Xyce Formal Guidelines Document	Y	N

Software Engineering

Software Engineering is the systematic, disciplined, and quantifiable approach to the development, operation, and support of software, i.e., the application of engineering to software. Activities include the following:

- Identification of a life cycle model,

- Development (e.g., requirements, design, implementation, test, release),
- Operation (e.g., execution on multiple platforms, regression tests, V&V tests),
- Support (e.g., change analysis, implementation, test, and release),
- Measurement of product and process attributes,
- Reviews and assessments of products and processes and
- Training on software engineering activities.

The balance among activities, and the relationships with modeling and simulation, verification and validation, and project management depends on many factors including the maturity of the software. Software Engineering also involves the application of engineering principles, which address the following:

- Customer stockpile certification problems,
- Derivation of conceptual physics phenomena models, associated mathematical models, numerical models and solution algorithms

Project Management

Project Management is the systematic approach for balancing the project work to be done, resources required, methods to be used, procedures to be followed, schedules to be met, and the way that a project is organized. Activities include: identification, analysis, and mitigation of project risks; controlling requirement changes; planning for project tasks, schedule, and cost; tracking project progress and status; providing oversight of process improvement; and training project personnel in management activities. These activities are described in detail in the HPEMS and Xyce Project Plans.

The philosophy of the HPEMS project is to release early and release often. A release early, release often philosophy is an iterative approach to software development and has the following benefits:

- Risk reduction through demonstrable progress;
- Progress measured in products, not documentation or engineering estimates;
- Continuous integration; and
- Continuous end user involvement.

A quarterly release cycle is used and at the beginning of each quarter, the project sets goals and internal team milestones for that quarter. Milestones are usually in the form of added capability to the code. At the end of each quarter, a code freeze occurs and a release process, which includes a final build and test for that release, is conducted. If a feature cannot be included for that quarterly release, the feature is not included, but is a top priority for the next quarterly release.

Configuration Management

Configuration management activities are version management, issue tracking, and release management. The Xyce Configuration Management Plan addresses these activities in detail. CVS (Concurrent Versions System) is the primary tool used for version and release management. Bugzilla is the primary issue-tracking tool. It is expected that the HPEMS project will migrate to the Dimensions tool for issue tracking and change management as time and resources allow. As other tools and capabilities are

developed for ASCI software engineering, it is also anticipated the HPEMS project will migrate to these tools. These activities are described in detail in the Xyce Code Configuration Management Plan.

Requirements Management

Customers are engaged in the requirements capture activities for the HPEMS project. Use case techniques are used where appropriate and where resources allow such an activity. Details of requirement activities are in the Xyce Code Requirements Management Plan.

Software Verification

The software verification activities for this V&V plan include methods to verify the software construction from unit level to integrated software component level. Even scientific model application design and requirement specifications, where applicable. All these activities use similar test suites to achieve the required confidence in the software implementation. Also included are Measurements/Metrics, which is the activity of collecting information for the characterization, understanding, and evaluation of processes and products. Metrics show how selected site-specific practices satisfy related attributes of specified principles and consequently contribute to meeting the V&V program's goals of confidence in codes and credibility in results. Only metrics that can be demonstrated to meet project and/or the V&V program's goals are chosen. The Xyce Code Test Plan describes these processes in detail.

Verification Test Suite

The Verification Test Suite (VERTS) is a test suite that is used for verification of the electrical circuit simulation codes currently being developed by the HPEMS code development team. It includes many suitable test problems from the available literature. If analytical solutions are unavailable, a test problem is created whose solution is well known in the literature. Verification is the process of determining that the equations implemented in the codes are solved correctly.

Acceptable performance of the simulation codes on the VERTS is the main factor that determines whether the code is ready for validation studies [ASCI V&V Guidelines]. The goal of the software verification process is to increase our confidence in the implementations of the required phenomena and their numerical behavior. This includes the mathematical equations needed to correctly solve the physics and algorithms used by the code.

Structure and Construction of the VERTS

Mechanics, boundary conditions, constitutive models, material properties, initial conditions and element topologies make up the test matrix. For the circuit models, verification will consist of a series of test problems that have known solutions for each component of the overall model. This approach creates a matrix of code modules versus test problems. This type of organization allows an analyst to easily verify the modules of the developed code as they are modified. A preliminary version of an acceptance test

plan is created, including a verification matrix relating requirements to the tests used to demonstrate that they are satisfied. The test problems are further refined into their tiers.

- **Tier I** – tests with exact analytical solutions. These tests are designed to ensure that the basic model device equations are functional and are producing correct analytical results when compared to hand calculations.
- **Tier II** – tests with semi-analytical solutions. These tests are semi-analytical in nature. Hand calculations of these circuits are too complex for a reasonable evaluation of circuit performance. The results of these circuits are compared to experimental data to ensure that performance, accuracy and convergence criteria are met.
- **Tier III** – idealized problems suitable for code comparison exercises. These tests are typically complex subcircuits and large system circuits. These tests are designed to ensure that performance, accuracy and convergence criteria are met at the subcircuit and circuit level. Tier III tests are also designed to ensure that multiple component circuits are functional and are meeting performance, accuracy and convergence criteria. Code comparison exercises are the main method for evaluating Tier III tests.

The structure of the VERTS is a building block structure similar to the structure of the PIRT. As mentioned in the discussion of the PIRT structure, electrical systems are constructed from many independent components. In an electrical system design, these components are assembled into subsystems and the subsystems are assembled into systems. The VERTS is constructed in a similar fashion. Tier I tests are based on single components and small (2-3 component) subsystems. Tier 2 tests are mostly subsystems, while Tier 3 tests are large subsystems (e.g. Radiation Hard Pentium Full Multiplier Circuit, 88000 transistors) and will eventually include system level tests. While this structure is suitable for basic assessment of the code under development, it is vital that the VERTS structure reflects the requirements outlined by the PIRT for a particular stockpile driver. Specific VERTS will be developed for each stockpile driver. Each will contain test cases from the global VERTS as well as circuit netlists that assess specific model or simulation requirements specified by the PIRT.

This structure for verification testing is advocated in the AIAA V&V Guide [AIAA]. The structure reflects the critical importance of accurate assessment of coded execution of verification test problems. The details of the test matrix can be found in the Xyce Verification Test Suite Plan. The following list is the structure in the table of contents for the Xyce Verification Test Suite Plan and outlines the test methods applied:

Testing Approach
Unit Testing
Regression Testing
Test Suite Structure
Automated Regression Testing
Manual Regression Testing
Comparison Techniques
Pass/Fail Criteria
    User Acceptance Testing
Test Environment
Test Methods

Hardware
Software
Programs and scripts
ParaSoft CodeWizard
Aprobe
Concurrent Versions System (CVS)
PVCS Dimensions Issue Tracking Data

The test matrix VERTS for this V&V plan is presented in Appendix A. It was constructed in a similar fashion as the PIRT. A Global VERTS was constructed during the initial development of the HPEMS circuit codes. The Xyce VERTS was extracted from the Global VERTS to specifically meet the stockpile driver requirements of this V&V Plan. The VERTS systematically identifies specific tests required for the modeling and simulation needs of the stockpile driver.

Since Xyce is not a three-dimensional code, in the test matrix for the VERTS, the column labeled "# of nodes" refers to the number of device terminals connected in the circuit, not the number of mesh analysis nodes. For example, a diode has two terminals as does a resistor and a voltage source, so if these three devices are connected in parallel then the circuit contains two nodes. A SAND report will be released Oct. 2001 for the HPEMS Verification Tier I Test Suite and revisions during FY02 will include Tiers II and III. Currently the netlists contained in the verification test suite can be found at the following location:

\\Wileycoyote\Elec_Sim\V&V_Plans\VERTS\VERTS_Netlists_Tier1.doc

The following is an example of a Tier I test circuit which uses Kirchoff's Law and the semiconductor equations that describe the device model and which are implemented in the code. The test circuit and results are used to verify the accuracy of the simulation code.

N-Channel JFET Circuit

```
**********************************************************************
* Tier No.: 1
* Directory/Circuit Name:  NJFET/NJFET.cir
* Description:   Circuit netlist to test current-voltage characteristics of the n-channel JFETmodel.
* Input:   VDD
* Output: I(VMON), V(3,2) , V(2)
* Analysis:
*For the self-biased NJFET circuit the general algebraic solution for the bias point is:
* ID  =  {[-B – SQRT(B**2 – 4*A*C)] / 2*A}
* Where,
* A = RS**2  =  (600)**2 = 3.6E+5
* B = -{2*|VP|*RS + (VP**2) / IDSS} =  -{2 * 4 * 600 + 16/10.0E-3} = -6.4E+3
* C = VP**2 = (-4)**2 = 16
* Therefore,
* ID = {[-(-6.4E+3) – SQRT((-6.4E+3)**2  –  4 * 3.6E+5 * 16 )] / 2 * 3.6E+5} = 3.009mA
* VGS = ID*RS = 3.009E-3 * 600 = 1.806 V
```

```
* |VDS| = |VDD| – ID*(RD + RS) = 15 – 3.009E-3 * (1.5k + 600) = 8.7V
* Note:
*       IDSS = BETA * VP**2 = 6.25E-4 * (-4)**2 = 10.0E-3 A
*       VP = VTO = -4V
*
*       The circuit simulation should yield       the following outputs:
*       I(VMON) = Drain Current                         Id = 3mA
*       V(3,2) = Drain-Source Voltage                   Vds = 8.7V
*       V(0,2) =Gate-Source  Voltage                    Vgs = 1.8V
********************************************************************************
VDD 4 0 DC 15V
VMON 5 3 0
RD 4 5 1.5K
RS 2 0 600
J 3 0 2 NJFET
.MODEL NJFET NJF BETA=6.25E-4 VTO=-4V
.DC VDD 15 15 1
.PRINT DC I(VMON) V(3,2) V(2,0)
.OPTIONS ACCT
.END
```

NJFET OUTPUT:

N-Channel JFET Circuit
DC transfer characteristic

Index	voltage_sweep VDD	vmon_branch ID	v(3)-v(2) VDS	v(2) VGS
0	1.500000E+01	3.009442E-03	8.680173E+00	1.805665E+00

VERTS Acceptance Metrics

The tolerance for the Regression Test Suite contained in the VERTS presented in Appendix A is, in most cases, 2%. The 2 % tolerance comes from a comparison of baseline results with results from each test. The baseline results are from a series of analytical and numerical calculations with an analysis of each of the baseline results. Expert judgement on calculation results is also used as an acceptance metric. An automated program, named Compare, was written to analyze the simulator's output for discrepancies between the CVS repository simulation data and the current regression test suite output.

A run_test_suite script compares the current output data to the expected output, or reference data. The output data is organized in a collimated format. The first column contains the independent variable, typically time or voltage. Successive columns contain important voltage or current values specified by the input files print statement. For each independent variable value, there are corresponding dependent values.

The column of values for each of the dependent variables defines how that variable varies as a function of the independent variable. Ideally, each of these functions matches the function defined by a reference run that has been determined by the Test Specialist to be 'correct'. The compare program performs this verification by comparing the reference and the current output and assuring that these functions are identical to within a specified tolerance. The compare program allows a tolerance to be specified in both the independent and the dependent variables. Conceptually this corresponds to taking plots of the reference and current functions and making sure that these are coincident within a certain distance by 'fattening' one of them and making sure that the other lies within the fattened trace.

As a practical matter, it is insufficient to merely allow for errors in the dependent variable because many circuits have abrupt transitions that can be slightly miss-timed, but still are correct within acceptable tolerances. For this reason, the traces are fattened in both the directions of the independent variable as well as the dependent variable. The specific amount of fattening in each direction is currently a relative amount of +/-2percentage. Thus for a value of 1 volt in the reference plot, the test plot would need to lie within the range 0.98-1.02 volts. For a value of 0 volts in the reference plot, the test value would need to be within 1 microvolt of zero because there is a minimum absolute tolerance of 1 microvolt or ampere for values that are near zero. A transition like a fast rising edge would need to appear at a time within that observed in the reference plot. Thus, a transition that occurs at 0.001 seconds would need to occur in the range 0.00098-00102 seconds in order to pass the test.

The choice of +/-2percentage accuracy was based on a survey of the users, DP customers and HPEMS team members all of whom use the code for analysis. There is a trade off between accuracy and time to solution that can be controlled in the netlist if the user chooses to specify. For the default value of the accuracy tolerances (which is what most users use) the accuracy is consistently within the 2% value.

Validation Plan

A building block approach is also used for the validation effort of this stockpile driver. Again, electrical systems are constructed from many independent components. Characterization of each electrical component is paramount in the overall validation plan. Validation efforts will be coordinated with efforts such as the War Reserve Commercial Off-The-Shelf (COTS) insertion process (WRCIP). The COTS project has developed processes for model validation and these processes will be used as part of this stockpile driver V&V plan as they mature.

The methodology for validation of electrical circuit models is uncertain at this time because validation is a process that electrical code developers and users are just beginning to define. However, certain activities have been identified as validation activities. These activities include

- Gathering of experimental test data at the component, subsystem and system levels,
- Error estimation associated with experimental test data,
- Uncertainty quantification of model results and experimental test data,
- Comparison of experimental test data and model results at the component, subsystem and system levels, and
- Success metrics associated with the validation activities.

Validation is the quantitative and qualitative confrontation of code "predictions" with "suitable" experimental data [Trucano]. Codes drive the experiments. Suitable experiments are not defined by goals of scientific exploration. Certain experiments should push the code capability to the limit. Some fraction of the experiments should aim to defeat the code so as to sharpen the boundaries of the region of applicability of the code.

The following are questions that must be considered and answered through the validation activities:

- How do we quantitatively increase our confidence that a computer simulation correctly represents the underlying conceptual models?
- How do we quantitatively increase our confidence that a computer simulation is an accurate representation of the real word?
- How do we measure confidence in our simulations?
- How do we quantitatively measure the risk associated with using computer models for our customers?
- How do we quantitatively deal with real uncertainties in our computational modeling?

Methodology

The fundamental approach to validation involves identification, quantification and comparison of error and uncertainty in the circuit model associated with the previously identified stockpile driver and experimental data. The validation of the stockpile driver identified in this V&V plan will apply a process that includes validation activities identified previously. Statistical methods, such as design of experiments, will be used, where appropriate, to minimize the amount of required validation. A model will be validated when it reproduces empirical results within a set range of error tolerance.

Structure and Construction of the VALTS

The validation testing will use a four tiered approach. The tiers are defined [Pilch] as

> **Tier I** – Designed to explore the validity of the implemented models by concentrating on separable effects (or single phenomena).

Tier II – Designed to explore the validity of the implemented models by concentrating on coupled effects between distinctly identified phenomena.

Tier III – Designed to explore the validity of the implemented models by concentrating on integral phenomenal, in which many coupled effects may be present.

Tier IV – A "Certification Experimental Campaign" or confirmatory experimental activity should be planned for assessing the readiness of the code for stockpile computing.

Each device-type model category (e.g. BJT) that requires validation is listed in the PIRT in Table 1. The subsystem level components which will be validated are the main logic board, Timer (FPGA) and RF Deck. The list of unique device part numbers (e.g. 2N2222) is classified and will not be included in this document. Each device and subsystem will be validated from –55C to 125C, for low-dose rate radiation effects and for Printed Circuit Board (PCB) parasitic effects.

Four phenomena were identified in the PIRT for the stockpile driver addressed by this V&V plan. The phenomena are

- Electrical device and subsystem performance in a nominal environment,
- Temperature effects on electrical devices and subsystems,
- Low-dose rate radiation effects on electrical devices and subsystems, and
- PCB parasitic effects including mutual coupling and signal cross talk.

Figure 3 illustrates how the PIRT links requirements to validation and verification activities.

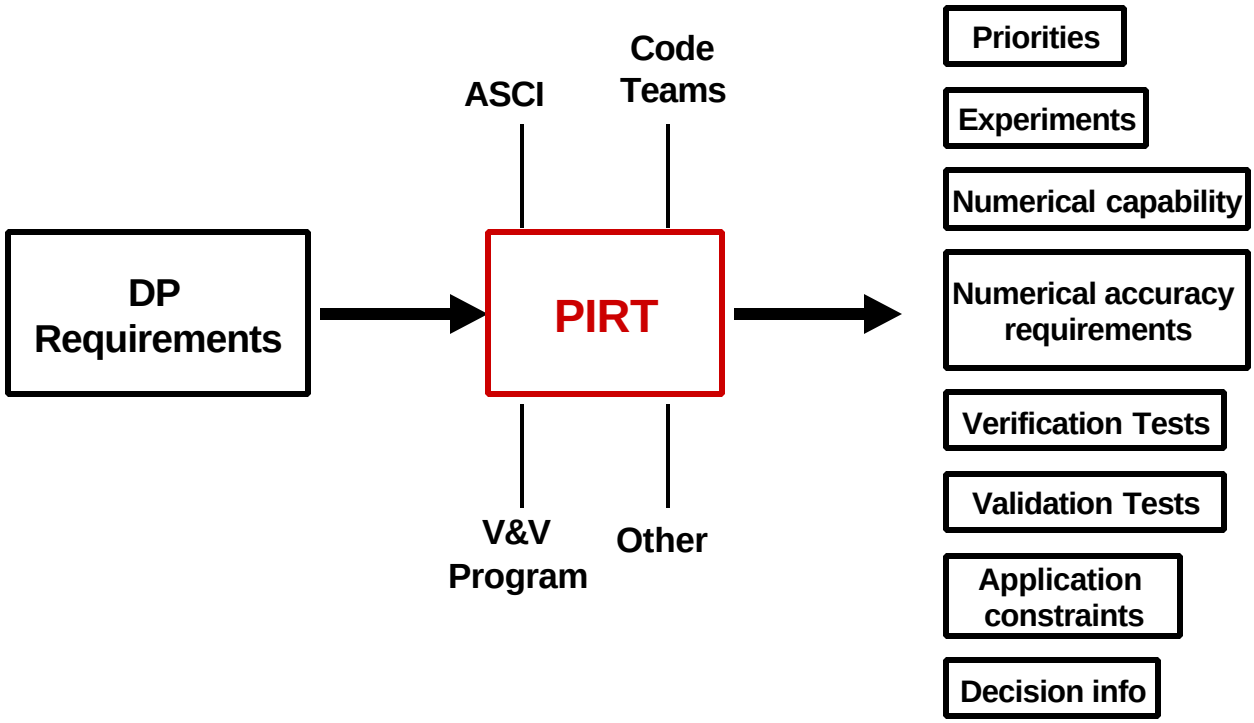

FIGURE 3 – PIRT DRIVES VALIDATION REQUIREMENTS

All individual components were lumped into the category, "Components". Components include devices such as transistors, resistors, capacitors and PCBs. Details of individual component testing and prioritization of such testing are presented in the Stockpile Driver Validation Test Suite document. Subsystems are collections of components. For this document, subsystems for which this stockpile driver is applicable were lumped into the category, "Subsystems." Details of subsystem testing and prioritization of such testing are presented in the Stockpile Driver Validation Test Suite document.

Potential coupled effects between each of the four previously identified phenomena were identified. These coupled effects are

- Low-dose radiation effects and constant temperature effects in individual components,
- Low-dose radiation effects and transient temperature effects in individual components,
- Subsystem functionality and PCB parasitic effects,
- PCB parasitic effects and subsystem constant temperature effects,
- PCB parasitic effects and subsystem transient temperature effects,
- Low-dose radiation effects and subsystem transient temperature effects,
- Low-dose radiation effects and subsystem constant temperature effects,
- Low-dose radiation effects and PCB parasitic effects,
- Low-dose radiation effects, PCB parasitic effects and subsystem constant temperature effects,
- Low-dose radiation effects, PCB parasitic effects and subsystem transient temperature effects.

All of the phenomena were categorized per the four tiered approach cited previously. The phenomena also were divided as to applicability to the component or subsystem level. This categorization is presented in Appendix B.

VALTS Acceptance Metrics

Validation metrics beyond some of the Tier 1 activities are unclear at this time. Validation metrics for electrical modeling and simulation are part of a process that electrical code developers, experimentalists and users are just beginning to define. Product Specification requirements will be used to test and validate the accuracy of each electrical device and subsystem identified in the stockpile driver [W76-1 Timer (FPGA) and RF Deck]. At this time, the Product Specifications have not been written and therefore more detail concerning the VALTS metrics cannot be provided. Uncertainty quantification techniques will be used to define such metrics**.**

Stockpile Computing Guidance

Stockpile computing guidance for electrical modeling and simulation is in its infancy at Sandia National Laboratories. However, there are similarities among the code efforts regarding stockpile computing guidance in the following areas:

- Code documentation,
- Code theory guides,
- Code configuration and platforms,

- Model data sources, and
- Model archive and retrieval.

As electrical modeling and simulation stockpile computing matures, the guidance will also mature. Recommendations from Lee [Lee] will be used to aid in the stockpile computing guidance maturation process.

Circuit simulation has been performed for at least 20 years and SPICE was first made available in the late 1970s. A wealth of expertise in how to perform circuit simulation is available in the literature. Training classes in the use of commercial circuit simulation codes are available. Training requirements are part of our overall stockpile guidance effort and some level of expertise must be shown in order to perform electrical modeling and simulation stockpile computing. As stated previously, the guidance of electrical modeling and simulation stockpile calculations will mature as the capability matures.

A DP customer might be concerned with two factors for performing stockpile computing. The first factor is that the appropriate level of technical expertise be applied when performing stockpile computing. The second factor is the specific constraints associated with the formality of the stockpile problem that is being addressed by the code. [Pilch] The HPEMS code, Xyce, can be used for exploratory (design margin analysis) purposes and have few or no formal DP process constraints associated with it. It also can be used as part of a very formal stockpile process (weapon system certification) and involve very rigorous DP process requirements and constraints. The use of Xyce for the stockpile driver described in this plan is for design margin analysis of several subsystems contained in the W76-1. Technical expertise will be used to perform the following:

- Proper problem definition (input)
- Proper execution of Xyce, and
- Proper analysis and accurate communication of results of the code application.

Most of this guidance will come from the code team to assure proper technical use of the code. Other forms of guidance provided by the code team includes:

- Code documentation, such as User's Guides and theory manuals,
- Appropriate criteria for doing stockpile calculations (to be designated),
- Minimum standards of user expertise for performing such calculations (to be defined),
- Input and output inspections,
- Use of code execution and analysis environments (scripts, GUI's, & other interfaces), and
- Use of analysts to perform the required stockpile application of the code.

The nature of electrical modeling and simulation on the circuit level allows the creation of individual component models and assembly of these models into subsystem and system level models. Sandia National Laboratories has a collection of these models and associated test data in the SPUDS portion of eCIS.

Development of circuit models will rely on the component models and associated test data in SPUDS, and in a new model development effort. Known "good" models are crucial in raising the confidence level in the results of a stockpile calculation. Our guidance will include processes for use, submittal and

archiving of models and associated test data in SPUDS. Details of the processes are presented in the Xyce Formal Guidelines Document (Figure 2).

Uncertainty quantification is also another important area for raising the stockpile computing confidence level. For the stockpile driver identified in this plan, techniques such as "design of experiments" calculations will be used in conjunction with tools such as DAKOTA (Design Analysis Kit for Optimization and Terascale Applications) to quantify uncertainty. The DAKOTA toolkit, developed at SNL for ASCI applications use, provides a flexible, extensible interface between analysis codes and iteration methods. DAKOTA contains algorithms for optimization with gradient and non-gradient based methods, uncertainty quantification with sampling, analytic reliability, and stochastic finite element methods, parameter estimation with nonlinear least squares methods, and sensitivity/primary effects analysis with design of experiments and parameter study capabilities.

References

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[Lee]J. R. Lee (1998), "Certainty in Stockpile Computing: Recommending a Verification and Validation Program for Scientific Software", Sandia National Laboratories Report SAND98-2420.

[Pilch], M. Pilch, T Trucano, J. Moya, A. Hodges, G. Froehlich, , and D. Peercy, Sandia National Laboratories, (2000), "Guidelines for Sandia ASCI Verification and Validation Plans – Content and Format: Version 2.0," SAND2000-3101,

[SNL]Sandia National Laboratories, (1995), "Sandia Software Guidelines, Volume 1-5, Documentation," SAND85-2345,

Appendix A- Normal Environment Verification Test Suite (VERTS)

NAME	Circuit Description	TIER	Sources	#Nodes	Analysis	Output
ABM_ABS	Test of ABM Absolute Value Function	1	DC Voltage	5	DC	Voltage
ABM_ACOS_ ASIN	Test of ABM Arccosine and Arcsine Functions	1	DC Voltage	4	DC	Voltage
ABM_ATAN_ TAN	Test of ABM Arctangent and Tangent Functions	1	Sine Voltage	4	TRAN	Voltage
ABM_EXPLN	Test of ABM Exp and Natural Log Functions	1	Pulse Voltage	4	TRAN	Voltage
ABM_HYP	Test of ABM Hyperbolic Functions, .PARAM, .FUNC, IF Statements	1	DC Voltage	15	DC	Voltage
ABM_LOG	Test of ABM Log Base 10 Function	1	PWL Voltage	5	TRAN	Voltage
ABM_SCT	Test of ABM Sine, Cosine and Tangent Functions	1	DC Voltage	6	DC	Voltage
ABM_SQRT	Test of ABM Square Root Function	1	PWL Voltage	4	TRAN	Voltage
CAPACITOR	Test of Capacitor Model	1	Pulse Current	3	TRANS	Voltage
CCCS	Test of Current-Controlled Current Source Model and Transfer Function Analysis	1	DC Voltage, CCCS	4	DC	Voltage
CCVS	Test of Current-Controlled Voltage Source Model	1	DC Voltage, CVCS	5	DC	Voltage
CLC	Simple RLC Circuit	1		4	TRANS	Voltage
DIFFPAIR	Simple Differential Pair Circuit	1	Sine & DC Voltage	10	TRANS	Voltage
DIGITIZER	Test of Lookup Table Functionality	1	DC and Sine Voltage	4	TRAN	Voltage
DIODE	Test of Diode Model	1	DC Voltage	4	DC	Current, Voltage
IEXP	Test of Exponential Current Source Model	1	IEXP	3	TRANS	Current
INDUCTOR	Test of Inductor Model	1	Pulse Voltage	3	TRANS	Voltage
IPULSE	Test of Pulse Current Source Model	1	IPULSE	3	TRANS	Current
IPWL	Test of Piecewise Linear Current Source Model	1	IPWL	3	TRANS	Current

NAME	Circuit Description	TIER	Sources	#Nodes	Analysis	Output
ISFFM	Test of Single Frequency Current Source Model	1	ISFFM	2	TRANS	Voltage
ISIN	Test of Sine Current Source Model	1	ISIN	3	TRANS	Current
ISWITCH	Test of Current Controlled Switch Model	1	DC Current	5	DC	Current
MINDUCTORS	Test of Inductor Coupling Model	1	AC Voltage	8	AC	Current
NJFET	Test of N-Channel JFET Model	1	DC Voltage	5	DC	Current, Voltage
NL_RESISTOR	Test of .PARAM, .FUNC, IF Statements	1	DC Voltage	4	TRAN	Voltage
NMESFET	Test of N-Channel MESFET Model	1	DC Voltage	4	DC	Current
NMOS	Test of N-Channel MOSFET Model	1	DC Voltage	6	DC	Current, Voltage
NPN	Test of NPN Bipolar Transistor Model	1	DC Voltage	6	DC	Current, Voltage
PJFET	Test of P-Channel JFET Model	1	DC Voltage	6	DC	Current, Voltage
PMOS	Test of P-Channel MOSFET Model	1	DC Voltage	5	DC	Current, Voltage
PNP	Test of PNP Bipolar Transistor Model	1	DC Voltage	8	DC	Current
RC	Simple RC Circuit	1	Pulse & AC Voltage	3	TRANS	Current, Voltage
RESISTOR	Test of Resistor Model	1	DC Voltage	2	DC	Current, Voltage
SEMIC_CAPACITOR	Test of Semiconductor Capacitor Model	1	Pulse Voltage	4	TRANS	Current, Voltage
SEMIC_RESISTOR	Test of Semiconductor Resistor Model	1	DC Voltage	3	DC	Current, Voltage
TFANALY	Test of Transfer Function Analysis	1	DC and Sine Voltage	7	TF	Voltage Gain, Input and Output Impedance
TRANSLINE	Test of Lossless Transmission Line Model	1	PWL Voltage	4	TRAN	Voltage
TRIODE	Test of Lookup Table Functionality	1	DC Voltage	3	DC SWEEP	Current
VCCS	Test of Voltage-Controlled Current Source Model	1	DC Voltage	4	DC	Voltage
VCVS	Test of Voltage-Controlled Voltage Source Model	1	DC Voltage	5	DC	Voltage

NAME	Circuit Description	TIER	Sources	#Nodes	Analysis	Output
VEXP	Test of Exponential Voltage Source Model	1	VEXP	2	TRAN	Voltage
VPULSE	Test of Pulse Voltage Source Model	1	VPULSE	2	TRAN	Voltage
VPWL	Test of Piecewise Linear Voltage Source Model	1	VPWL	2	TRAN	Voltage
VSFFM	Test of Single Frequency (FM) Voltage Source Model	1	VSFFM	2	TRAN	Voltage
VSIN	Test of Sine Voltage Source	1	VSIN	2	TRAN	Voltage
VSWITCH	Test of Voltage-Controlled Switch Model	1	PWL & DC Voltage	5	TRAN	Voltage
1N759_-55	Test of TC Zener Model at -55C	2	Pulse & DC Voltage, DC Current	5	TRAN	Resistance
IRFF9130	Test of Power Mosfet Model at 125C	2	Pulse and DC Voltage	17	TRAN	Voltage
MC3086	Transformer Circuit - Test of .PARAM Syntax	2	Sine & DC Voltage	7	TRANS	Voltage
PULSE_LOAD	Pulse Load Circuit - Sandler Circuit	2	DC & Pulse Voltage	8	TRANS	Current, Voltage
TEST1	Test of BSIM3 Model Implementation - NMOS	2	DC Voltage	3	DC	Current, Voltage
TEST10	Test of BSIM3 Model Implementation - PMOS @100^{O}	2	DC Voltage	4	DC	Current, Voltage
TEST11	Test of BSIM3 Model Implementation - PMOS	2	DC Voltage	5	DC	Current, Voltage
TEST12	Test of BSIM3 Model Implementation - PMOS	2	DC Voltage	6	DC	Current, Voltage
TEST14	Test of BSIM3 Model Implementation - PMOS @100^{O}	2	DC Voltage	7	DC	Current, Voltage
TEST3	Test of BSIM3 Model Implementation - NMOS @100^{O}	2	DC Voltage	8	DC	Current, Voltage
TEST4	Test of BSIM3 Model Implementation - NMOS	2	DC Voltage	9	DC	Current, Voltage
TEST5	Test of BSIM3 Model Implementation - NMOS	2	DC Voltage	10	DC	Current, Voltage

NAME	Circuit Description	TIER	Sources	#Nodes	Analysis	Output
TEST6	Test of BSIM3 Model Implementation - NMOS @-55^{O}	2	DC Voltage	11	DC	Current, Voltage
TEST7	Test of BSIM3 Model Implementation - NMOS @100^{O}	2	DC Voltage	12	DC	Current, Voltage
TEST8	Test of BSIM3 Model Implementation - PMOS	2	DC Voltage	13	DC	Current, Voltage
TEST9	Test of BSIM3 Model Implementation - PMOS @-55^{O}	2	DC Voltage	14	DC	Current, Voltage
1N4733	Test of 1N4733 Device - Sandler Circuit	3	DC Current, Voltage	8	OPERATING PT	Voltage
4049OSC	Test of 4049 HEX Buffer Circuit - Sandler Circuit	3	DC Voltage	6	TRANS	Voltage
BSIM1	Test of NMOS BSIM1 Implementation	3	DC Voltage	12	DC	Current
BSIM2	Test of NMOS BSIM2 Implementation	3	DC Voltage	12	DC	Current
COMPARATOR	Test of BSIM3 Model Implementation - One Bit Comparator	3	Pulse & DC Voltage	15	TRANS	Voltage
GAIN	Test of BSIM3 Model Implementation - Simple MOSFET Gain Stage	3	DC & AC Voltage	4	AC	Voltage
HA26003	Test of HA2600 Op Amp Supply Current	3	DC & AC Current and Voltage	22	TRANS	Voltage
LM185	Test of LM185 Subcircuit	3	DC Current	18	DC	Voltage
LM2901	Test of LM2901 Comparator	3	DC & Sine Voltage	20	TRANS	Voltage
LOAD	Test of Simple Load Circuit - Sandler Circuit	3	DC Current & Voltage	19	DC	Voltage
LTRA1	BJT Driver - 24 Inch Lossy Line - Diode Ckt	3	DC & Pulse Voltage	~200	TRANS	Voltage
LTRA2	Interconnect Simulation	3	DC & Pulse Voltage	~300	TRANS	Voltage

NAME	Circuit Description	TIER	Sources	#Nodes	Analysis	Output
LTRA3	BJT Driver - 20 Inch Coupled Line - Diode Ckt	3	DC & Pulse Voltage	~300	TRANS	Voltage
MC2929	Tests Implementation of PSpice compatible Transformer Model in ChileSpice - aka Nonlinear Coupled Inductor	3	Sine Voltage	7	TRANS	Voltage
MC2930	Tests Implementation of PSpice compatible Transformer Model in ChileSpice - aka Nonlinear Coupled Inductor	3	Sine Voltage	6	TRANS	Voltage
MCNC_BJT_BJTINV	BJT Inverter Circuit	3	Pulse & DC Voltage	12	TRANS	Voltage
MCNC_BJT_LATCH	BJT Static Latch Circuit	3	Pulse & DC Voltage	13	TRANS	Voltage
MCNC_BJT_NAGLE	741 Op Amp Circuit	3	Sine, AC, DC Voltage	29	TRANS	Voltage
MCNC_BJT_OPAMPAL	Four Unity Gain Op Amps in Series	3	Sine & DC Voltage	29	TRANS	Voltage
MCNC_BJT_RCA	RCA 3040 Wideband Op Amp	3	Sine & DC Voltage	20	TRANS	Voltage
MCNC_BJT_SCHMITECL	ECL Compatible Schmitt Trigger Circuit	3	PWL & DC	9	TRANS	Voltage
MCNC_BJT_VREG	Voltage Regulator	3	DC Voltage	20	DC	Voltage
MCNC_MOS2_AB_AC	CMOS Class AB Op Amp	3	AC & DC Voltage	26	AC	Voltage
MCNC_MOS2_AB_INTEG	CMOS Integrator Circuit	3	PWL & DC Voltage	28	TRANS	Voltage
MCNC_MOS2_CRAM	MCNC CRAM Circuit	3	PWL & DC Voltage	25	TRANS	Voltage
MCNC_MOS2_E1480	MOS Flip Flop Circuit	3	Pulse & DC Voltage	~100	TRANS	Voltage

NAME	Circuit Description	TIER	Sources	#Nodes	Analysis	Output
MCNC_MOS2_G1310	RCA 1310 Standard Cell	3	Pulse & DC Voltage	17	TRANS	Voltage
MCNC_MOS2_MOSRECT	MOSFET Diode Bridge	3	Sine & DC Voltage	8	TRANS	Voltage
MCNC_MOS2_MUX8	8 Bit Multiplexer	3	PWL Voltage	~100	TRANS	Voltage
MCNC_MOS2_REG0	Hybrid Pi Model of 3.3V Regulator	3	AC Voltage	16	AC	Voltage
MCNC_MOS2_SCHMITFAST	CMOS Schmitt Trigger w/Large Hysteresis	3	DC Voltage	8	DC	Voltage
MCNC_MOS2_SCHMITSLOW	CMOS Schmitt Trigger w/Small Hysteresis	3	DC Voltage	8	DC	Voltage
MOS6INV	MOSFET Invertor	3	PWL & DC Voltage	21	TRANS	Voltage
MOSAMP2	MOSFET Amplifier	3	Pulse & DC Voltage	22	TRANS	Voltage
MOSMEM	MOSFET Memory Cell	3	Pulse & DC Voltage	10	TRANS	Voltage
ONESHOT	Test of BSIM3 Model Implementation - One Shot Trigger	3	Pulse & DC Voltage	15	TRANS	Voltage
OPAMP	Test of BSIM3 Model Implementation - Op Amp	3	DC & AC Voltage	11	AC	Voltage
SCHMITT	CD4093 Nand Schmidt Trigger Circuit	3	DC & Pulse Voltage	25	TRANS	Voltage
TL431	TL431 Test Circuit - Sandler Circuit	3	Pulse Current, DC Voltage	16	TRANS	Voltage
UA741	Test of Behavioral Model of UA741 Op Amp Circuit - Sandler Circuit	3	DC Current, Voltage	~18	TRANS	Voltage
Fullmult2	Test of BSIM3 Model Implementation as Full Multiplier section of Radiation Hard Pentium Processor	3	DC & Pulse Voltage	~308000	TRANS	Voltage

Appendix B- Normal Environment Validation Test Suite (VALTS)

Experiment Level	Tier	Phenomena	Comments
Component	1	Nominal	Room Temperature, individual component
Component	1	Thermal	Transient temperature,
Component	1	Low-dose rate radiation	Constant temperature
Component	1	PCB parasitic effects	
Subsystem	1	Nominal	Room Temperature
Subsystem	1	Thermal	Transient temperature
Subsystem	1	Low-dose rate radiation	
Subsystem	1	PCB parasitic effects	
Component	2	Low-dose rate radiation & thermal	Constant temperature
Component	2	Low-dose rate radiation & thermal	Transient thermal
Subsystem	2	Thermal & PCB parasitic effects	Constant temperature
Subsystem	2	Thermal & PCB parasitic effects	Transient temperature
Subsystem	2	Low-dose rate radiation & thermal	Constant temperature
Subsystem	2	Low-dose rate radiation & thermal	Transient thermal
Subsystem	2	Low-dose rate radiation & PCB parasitic effects	
Subsystem	3	Low-dose rate radiation & PCB parasitic effects & Thermal	Constant temperature
Subsystem	3	Low-dose rate radiation & PCB parasitic effects & Thermal	Transient thermal

Distribution

1	MS 0525	1734	P.V. Plunkett
1	MS 0525	1734	R. B. Heath
1	MS 0525	1734	M Deveney
1	MS 0525	1734	L Waters
1	MS 0525	1734	T Russo
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1	MS 0525	1734	J Everts
1	MS 0525	1734	R Sikorski
1	MS 1071	1730	M Knoll
1	MS 1081	1762	F W Sexton
1	MS 1081	1762	P E Dodd
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1	MS 0481	2114	D Thomas
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1	MS 0533	2333	W H Schaedla
1	MS 0501	2338	M K Lau
1	MS 0501	2338	G R Laguna
1	MS 0537	2331	P A Molley
1	MS 0537	2331	A Muyshondt
1	MS 0537	2331	S Limary
1	MS 0537	2331	B Wampler
1	MS 0537	2331	B Rush
1	MS 1137	6536	A L Hodges
1	MS 9202	8418	K D Marx
1	MS 9202	8418	S L Brandon
1	MS 9409	8732	W P Ballard
1	MS 0835	9140	J M McGlaun
1	MS 0835	9142	J S Peery
1	MS 0828	9133	M Pilch
1	MS 0819	9211	T G Trucano
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