SANDIA REPORT
SAND2001-3858
Unlimited Release
Printed December 2001

High Performance Electrical Modeling and Simulation Verification Test Suite - Tier I

Regina L. Schells, Carolyn W. Bogdan and Steve D. Wix

Prepared by
Sandia National Laboratories
Albuquerque, New Mexico 87185 and Livermore, California 94550

Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy under Contract DE-AC04-94AL85000.

Issued by Sandia National Laboratories, operated for the United States Department of Energy by Sandia Corporation.

Available to DOE and DOE contractors from
U.S. Department of Energy
Office of Scientific and Technical Information
P.O. Box 62
Oak Ridge, TN 37831

Telephone: (865)576-8401
Facsimile: (865)576-5728
E-Mail: reports@adonis.osti.gov
Online ordering: http://www.doe.gov/bridge

Available to the public from
U.S. Department of Commerce
National Technical Information Service
5285 Port Royal Rd
Springfield, VA 22161

Telephone: (800)553-6847
Facsimile: (703)605-6900
E-Mail: orders@ntis.fedworld.gov
Online order: http://www.ntis.gov/ordering.htm

SAND2001-3858
Unlimited Release
Printed December 2001

High Performance Electrical Modeling and Simulation Verification Test Suite - Tier I

Regina L. Schells
Carolyn W. Bogdan and Steven D. Wix
Components Information and Models Department,
Sandia National Laboratories
P.O. Box 5800
Albuquerque, NM 87185-0525

Abstract

This document describes the High Performance Electrical Modeling and Simulation (HPEMS) Global Verification Test Suite (VERTS). The VERTS is a regression test suite used for verification of the electrical circuit simulation codes currently being developed by the HPEMS code development team. This document contains descriptions of the Tier I test cases.

Table of Contents

List of Tables

1 Introduction

1.1 Purpose

This document describes the High Performance Electrical Modeling and Simulation (HPEMS) Global Verification Test Suite (VERTS). The VERTS is a regression test suite used for verification of the electrical circuit simulation codes currently being developed by the HPEMS code development team.

1.2 Scope

A software verification process is necessary to increase our confidence in the implementation of the required model equations and their numerical behavior. This includes the mathematical equations needed to correctly solve the physics and algorithms used by the code. Verification has been described in the Accelerated Strategic Computing Initiative (ASCI) V&V Guidelines as:

1. The process of determining that the equations are solved correctly.
2. The process of determining that a computational software implementation correctly represents the model of the physical process.

Acceptable performance of the simulation codes on the VERTS is the main factor that determines whether the code is ready for validation studies [ASCI V&V Guidelines].

This document outlines a Global VERTS that is used for verification of two electrical circuit simulation codes, ChileSPICE and Xyce. The Global VERTS was constructed during the initial development of the HPEMS ChileSPICE code. Test cases in the Xyce VERTS are extracted from the Global VERTS as functionality is added to the code. The VERTS structure, construction and assessment criteria are outlined in this document.

1.3 Acronyms and Abbreviations

ASCI	Accelerated Strategic Computing Initiative
DP	Defense Programs
HPEMS	High Performance Electrical Modeling and Simulation
PIRT	Phenomena Identification and Ranking Table
VERTS	Verification Test Suite
SNL	Sandia National Laboratories

2 Verification Test Suite (VERTS)

The VERTS is a regression test suite used to assess the performance of electrical circuit simulation codes, ChileSPICE and Xyce, which are currently being developed by the HPEMS team. Testing activities, including generating test cases, are done in parallel with code development activities. The VERTS is comprised of circuit netlists and their expected simulation outputs. A circuit netlist specifies the circuit components and their connections, the type of analysis to be performed, and the desired output. The simulation code parses the netlist, performs the desired analysis and generates an output file.

ChileSPICE is Sandia's enhanced shared memory version of Spice3F5, which was originally developed at the University of California at Berkley. Xyce is a parallel electrical circuit simulation code that is being developed to support the simulation needs of the Sandia National Laboratories (SNL) electrical system designers. ChileSPICE is a development test bed for Xyce, which is intended to be the production simulator.

2.1 Key Areas

Three key areas will be addressed in describing the VERTS:
1. Structure: Why was the verification test suite chosen?
2. Construction: How was the verification test suite chosen?
3. Assessment: How is the VERTS executed? When are verification tests passed?

2.1.1 VERTS Structure

The structure of the VERTS is the logic by which the test suite is defined and applied to test the code [ASCI V&V Guidelines]. The HPEMS VERTS is structured according to the three-tier taxonomy first introduced in Version 1 of the ASCI V&V Guidelines.

- Tier I – tests with exact analytical solutions. These tests are designed to ensure that the basic devices are functional and are producing correct results when compared to exact analytical solutions (i.e., hand calculations).
- Tier II – tests with semi-analytical solutions. These tests are semi-analytical in nature. Hand calculations of these circuits are too complex for a reasonable evaluation of circuit performance. The results of these circuits are compared to experimental data to ensure performance, accuracy and convergence criteria are met.
- Tier III – idealized problems suitable for code comparison exercises. These tests are typically complex subcircuits and circuits. These tests are designed to ensure performance, accuracy and convergence criteria are met at the subcircuit and circuit level. Tier III tests are also designed to ensure that multiple component circuits are functional and are meeting performance, accuracy and convergence criteria. Code comparison exercises are the main method for evaluating Tier III tests.

While this structure is suitable for basic assessment of the code under development, it is vital that the VERTS structure reflects the requirements outlined by the Phenomena Identification Ranking Table (PIRT) for a particular stockpile driver. Specific VERTS will be developed for each stockpile driver. They will contain test cases from the global VERTS as well as circuit netlists

that assess specific model or simulation requirements specified by the PIRT.

The PIRT is the methodology by which the key physical phenomena are defined. The PIRT ranks the importance of code activity associated with implementing the phenomena and provides the basis for gauging associated fidelity requirements. Electrical systems are constructed from many independent components. These components are hierarchically grouped into families based on technology, functionality and usage. Examples of family classes are transistors, resistors and capacitors. Within each class, there is a further division into related components. For example, a transistor can be categorized into a bipolar junction transistor, a junction field effect transistor and a metal oxide semiconductor field effect transistor. Each component may have a different response to the same external environmental stimuli. A BJT (bipolar junction transistor) reacts differently in a radiation field when compared to a resistor response in the same radiation field. The Global PIRT was constructed based on the hierarchy found in electronic components.

This document addresses Tier I test cases. The Tier II and III tests will be documented in reports that will be released by September 2002.

2.1.2 VERTS Construction

Discussion of the construction of the VERTS answers the basic question of how the VERTS is actually populated with the appropriate tests. In an electrical system design, the components are assembled into subsystems and the subsystems are assembled into systems [HPEMS V&V Plan]. The VERTS is similarly constructed. In accordance with the three-tier taxonomy outlined previously, Tier I circuits test the individual component device models to verify that the simulator produces accurate results. Tier II circuits consist of netlists that contain a variety of components that are integrated into subsystems. Tier III circuits are netlists that test large subsystems and will eventually include system level test cases.

Tier I test cases are designed to test the codes':
- Basic Circuit Elements - transistors, resistors, capacitors, inductors, sources, etc.
- Simulation Analysis types - AC, DC, transient, transfer function, etc.
- Enhanced features - parameters, functions, look-up tables, analog behavioral modeling elements, etc.

These problems are small (2-3 components) and demonstrate that the circuit code can solve mathematical device model equations correctly when compared to exact analytical solutions. As device models, analysis types and enhanced features are added to the code, associated test cases are developed and added to the VERTS.

2.1.3 Execution of VERTS

The VERTS is organized in a directory tree with three main subdirectories: Netlists, Output Data, and Test Scripts. Each test case in the VERTS has a subdirectory containing the input and expected (or reference) output file in the Netlist and Output Data directories, respectively. The input file directory contains one input file and any necessary model library files. The output file directory contains the expected results in an output file. The Test Scripts directory contains the various scripts needed to perform an automated or manual regression test. This directory

structure allows for exercising VERTS regression testing automatically or manually, and is detailed in the [HPEMS/Xyce Test Plan].

For automated regression testing a set of scripts is used to build the executables, execute the regression testing, collect the output results, compare them to expected results and report the results to the code development team. A report containing the test results is generated. This report lists the test date, computational platform used, each test name with the associated pass/fail results for each executable (serial, parallel or both) that is used. Each regression test run issues an email message containing the test reports to each member of the HPEMS code development team. A cron job is used to schedule regression testing on a nightly basis.

Manual regression testing is useful for code developers testing code changes before committing them to the repository. They can run the test suite using the executables compiled in their working directory. The process for manual regression testing is similar to the automated test process. A developer checks out the test scripts from the CVS repository, runs the test script using their compiled serial or parallel executables and a test results file is created in the developer's current directory.

2.1.4 VERTS Assessment

As new features are added to the code, VERTS regression testing is used to test these new features and verify that the changes to the code did not create any bugs. Code assessment by the VERTS is a simple pass or fail. For each test case in the VERTS, the current simulation output is recorded and compared to the reference output results. The reference output has been determined by the Test Specialist to be 'correct' based on hand calculations for Tier I tests. A compare program performs verification by comparing the reference and the current results and assuring that they are identical to within a specified tolerance of +/-2%. When the current results match the reference within 2%, then a pass is recorded in the test report; otherwise, fail is recorded in the test report. As detailed in [HPEMS Xyce Test Plan], the compare program allows a tolerance to be specified in both the independent and the dependent variables. Conceptually this corresponds to taking plots of the reference and test data and making sure that these are coincident within a certain distance by 'fattening' one of them and making sure that the other lies within the error margin of the fattened trace. As a practical matter it is insufficient to merely allow for errors in the dependent variable because many circuits have abrupt transitions that can be slightly miss-timed, but still are correct within acceptable tolerances. For this reason the reference traces are fattened in both the direction of the independent variable as well as the dependent variable. The specific amount of fattening in each direction is currently a relative amount of ±2%. Using time and voltage as the independent and dependent variables, respectively, the test value for comparison must meet the following criteria:

$$(1 - Tol_V) < V/V_{REF} < (1 + Tol_V) \qquad (1)$$
$$(1 - Tol_T) < T/T_{REF} < (1 + Tol_T) \qquad (2)$$

where,

V, T = test voltage and time, respectively
Tol_V, Tol_T = voltage and time tolerance, respectively
V_{REF}, T_{REF} = reference voltage and time, respectively

Thus for a value of 1 volt in the reference plot, the test plot would need to lie within the range 0.98-1.02 volts. A transition like a fast rising edge would need to appear at a time within that observed in the reference plot. Thus a transition that occurs at 0.001 seconds would need to occur in the range 0.00098-00102 seconds in order to pass the test.

For values near zero where the relative tolerance test is too restrictive, there is also a minimum absolute tolerance of 1 μvolt or 1 picoamp. For a value of 0 volts in the reference plot, the test value would need to be within 1 μvolt of zero.

The choice of 2% tolerance is based on the accuracy that electrical circuit designers typically expect from simulation results, and was set by HPEMS Defense Program (DP) customers.

3 VERTS Netlists

3.1 Tier I Test Cases

The netlists contained in this section are Tier I test cases. A netlist file describes each test case. The first part of the file is a description that includes the circuit name, input and output voltages or currents, and equations used for a hand calculation of the expected results. The next section of the file defines the circuit elements, their connectivity, analysis type, and includes a print statement that defines the node voltages or branch currents to be recorded in the output file. Finally, a plot or a table of the ChileSPICE simulation results is shown.
Table 1. lists the basic circuit elements, test circuit name, description and analysis type for the Tier I test cases. Some of the circuit elements are tested using more than one test case. However, the purpose for each test case is unique as seen in the circuit description column.

Table 1. Basic Circuit Elements Tested by Tier I Test Cases

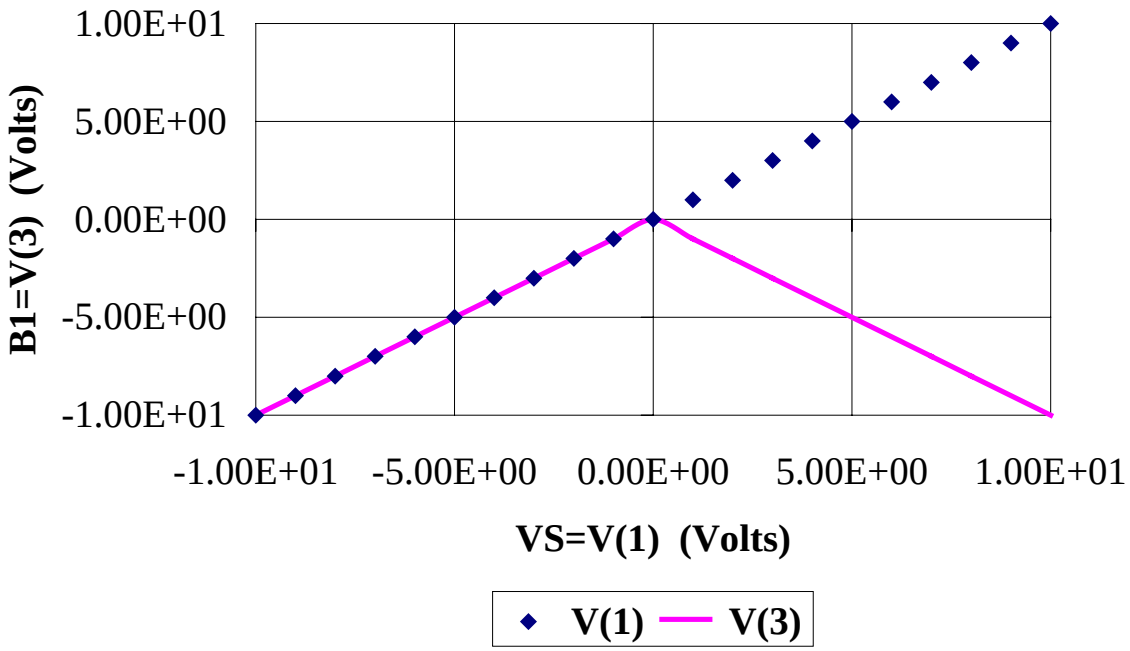
DEVICE TESTED		Circuit Name	Circuit Description	Analysis
B	Nonlinear Dependent Source	ABM_ABS	Test of ABM Absolute Value Function	DC*
		ABM_ACOS_ASIN	Test of ABM Arccosine and Arcsine Functions	DC
		ABM_ATAN_TAN	Test of ABM Arctangent and Tangent Functions	TRAN**
		ABM_EXPLN	Test of ABM Exponential and Natural Log Functions	TRAN
		ABM_HYP	Test of ABM Hyperbolic Functions, .PARAM, .FUNC, IF Statements	DC
		ABM_LOG	Test of ABM Log Base 10 Function	TRAN
		ABM_SCT	Test of ABM Sine, Cosine and Tangent Functions	DC
		ABM_SQRT	Test of ABM Square Root Function	TRAN
		ABM_TIME	Test of F(Y,T) Functionality	TRAN
		POLY	Test of Polynomial Function	DC
C	Capacitor	CAPACITOR	Test of Capacitor Model	TRANS
		SEMIC_CAPACITOR	Test of Semiconductor Capacitor Model	TRANS
D	Diode	DIODE	Test of Diode Model	DC
E	Linear VCVS	VCVS	Test of Voltage-Controlled Voltage Source Model	DC
F	Linear CCCS	CCCS	Test of Current-Controlled Current Source Model and Transfer Function Analysis	DC
G	Linear VCCS	VCCS	Test of Voltage-Controlled Current Source Model	DC
H	Linear CCVS	CCVS	Test of Current-Controlled Voltage Source Model	DC
I	EXP	IEXP	Test of Exponential Current Source Model	TRANS
I	PULSE	IPULSE	Test of Pulse Current Source Model	TRANS
	PWL	IPWL	Test of Piecewise Linear Current Source Model	TRANS
	SFFM	ISFFM	Test of Single Frequency (FM) Current Source Model	TRANS
	SIN	ISIN	Test of Sine Current Source Model	TRANS
J	JFET	NJFET	Test of N-Channel Junction Field Effect Transistor (JFET) Model	DC
		PJFET	Test of P-Channel Junction Field Effect Transistor (JFET) Model	DC
K	Mutual Inductor	MINDUCTORS	Test of Inductor Coupling Model	AC***
L	Inductor	INDUCTOR	Test of Inductor Model	TRANS
M	MOSFET	NMOS	Test of N-Channel Metal Oxide Semiconductor Field Effect Transistor (MOSFET) Model	DC

		PMOS	Test of P-Channel Metal Oxide Semiconductor Field Effect Transistor (MOSFET) Model	DC
Q	BJT	NPN	Test of NPN Bipolar Junction Transistor (BJT) Model	DC
		PNP	Test of PNP Bipolar Junction Transistor (BJT) Model	DC
R	Resistor	RESISTOR	Test of Resistor Model	DC
		SEMIC_RESISTOR	Test of Semiconductor Resistor Model	DC
S	Voltage Switch	VSWITCH	Test of Voltage-Controlled Switch Model	TRAN
T	Transmission Line	TRANSLINE	Test of Lossless Transmission Line Model	TRAN
.TF	TF Analysis	TFANALY	Test of Transfer Function Analysis	TF
V	EXP	VEXP	Test of Exponential Voltage Source Model	TRAN
	PULSE	VPULSE	Test of Pulse Voltage Source Model	TRAN
	PWL	VPWL	Test of Piecewise Linear Voltage Source Model	TRAN
	SFFM	VSFFM	Test of Single Frequency (FM) Voltage Source Model	TRAN
	SIN	VSIN	Test of Sine Voltage Source	TRAN
W	Current Switch	ISWITCH	Test of Current Controlled Switch Model	DC
X	Digital Primitive Subcircuit	AND	Test of AND Gate	TRAN
		NAND	Test of NAND Gate	TRAN
		NOR	Test of NOR Gate	TRAN
		OR	Test of OR Gate	TRAN
		XNOR	Test of XNOR Gate	TRAN
		XOR	Test of XOR Gate	TRAN
Z	MESFET	NMESFET	Test of N-Channel MESFET Model	DC
* DC - DC sweep of an input voltage/current source				
** TRAN - Transient analysis or behavior over time				
***AC - AC Analysis or small signal frequency response				

3.1.1 Test Circuit for the Absolute Value Function

```
**********************************************************************************
* Tier No.:  1
* Directory/Circuit Name: ABM_ABS/abs.cir
* Description:  Test of the of analog behavioral modeling absolute value function.
* Input:  VS
* Output: V(1), V(3)
* Analysis:
*       A DC input voltage, VS, is swept from -10V to 10V in 1V steps. A nonlinear
*       dependent voltage source, B1 or V(3),  is defined as the negative of the absolute
*       value of the source voltage (VS=V(1)). A DC analysis is performed and the output
*       recorded, V(3),  is the voltage defined by the input DC source voltage and the absolute
*       value function.
*
*       This table is a set of hand calculations for the absolute value, ABS, of V(1):
*               V(1)            V(3)=-ABX(V(1))
*               -1.00E+01       -1.00E+01
*               -5.00E+00       -5.00E+00
*                0.00E+00        0.00E+00
*                5.00E+00       -5.00E+00
*                1.00E+01       -1.00E+01
*
**********************************************************************************
VS   1  0  0
RS   1  2  100
R1   2  0  100K
B1   3  0  V = {-(ABS(V(1,0)))}
R2   3  4  100
R3   4  0  100K
.DC VS -10 10 1
.PRINT DC V(1) V(3)
.OPTIONS ACCT
.END
```

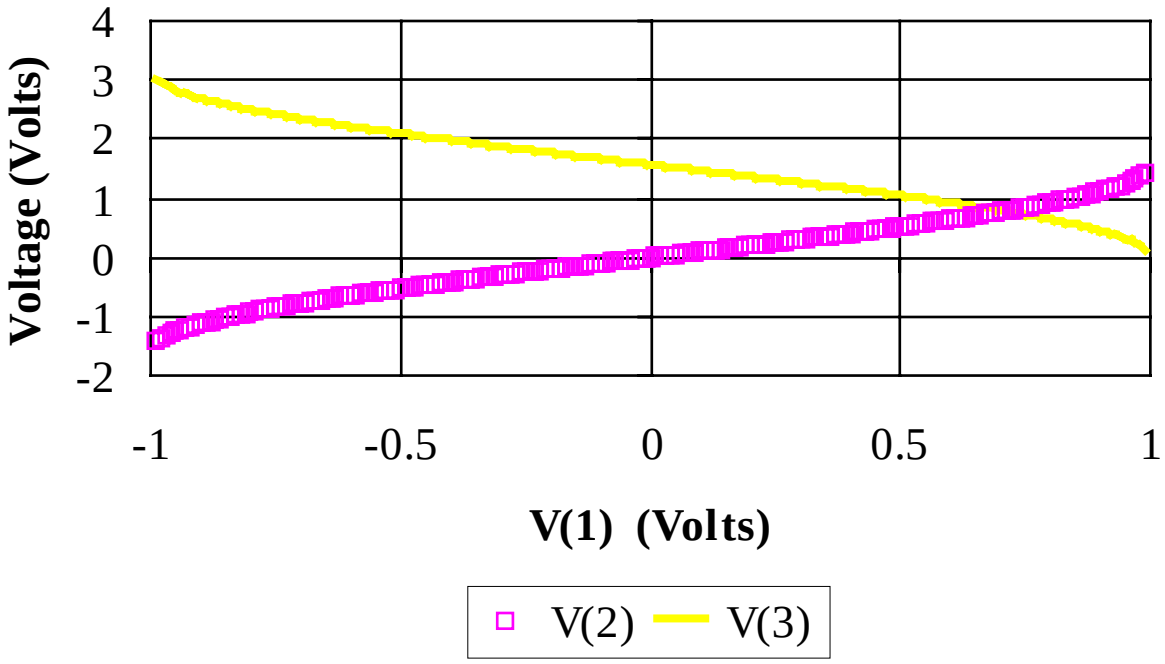
ChileSPICE Simulation Results for the ABS Circuit



3.1.2 Test Circuit for the Arcsine and Arccosine Functions

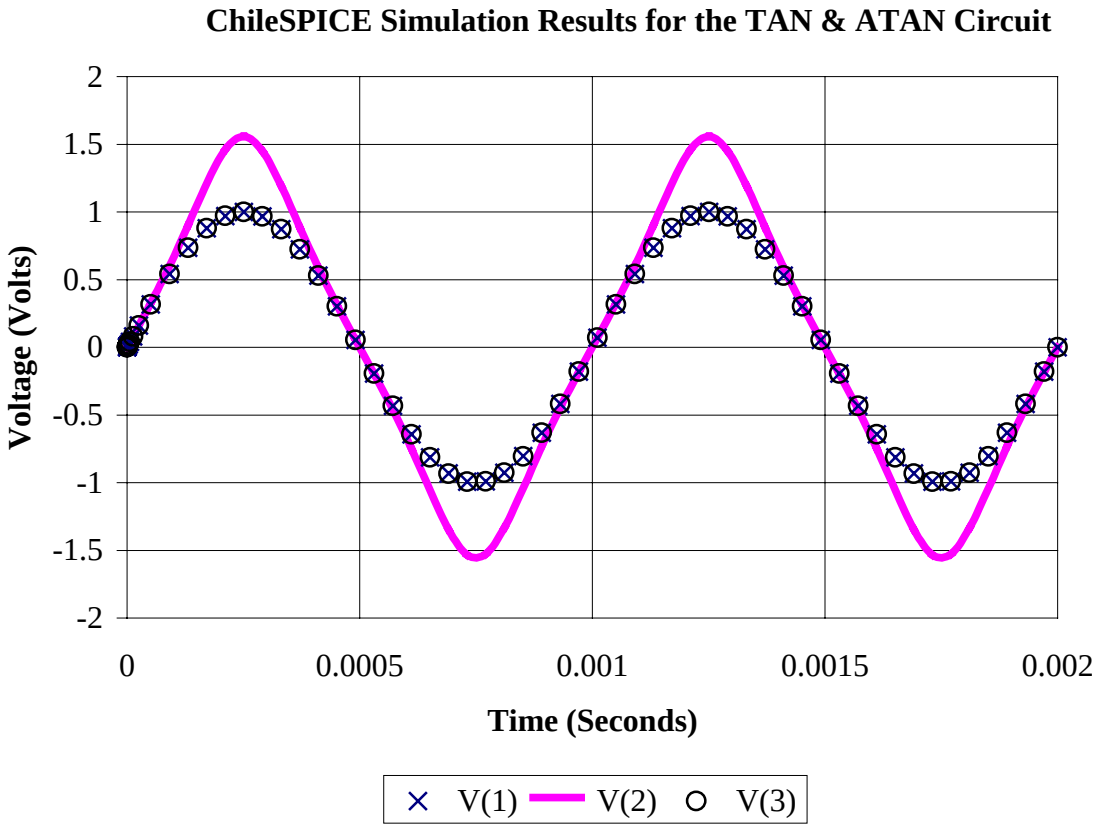
```
**********************************************************************************
* Tier No.:     1
* Directory/Circuit Name: ABM_ACOS_ASIN/acos_asin.cir
* Description:  Test of the analog behavioral modeling arcsine and arccosine functions.
* Input: V1
* Output: V(1), V(2), V(3)
* Analysis:
*       The netlist contains an independent voltage source, V1 or V(1),  which is swept from
*       –0.99V to 0.99V in 0.1V steps.  Two nonlinear dependent voltage sources are
*       used to define the functions as follows:
*               V(2)=B2=ASIN(V(1)) = inverse sine of V(1)
*               V(3)=B3=ACOS(V(1)) = inverse cosine of V(1)
*       A DC analysis is performed and the output recorded is voltages defined by the
*       arccosine and arcsine functions.
*
*       This table is a set of hand calculations for the functions of ACOS and ASIN of X
*               X               ACOS(X)             ASIN(X)
*               -1.0            3.14                -1.570
*               -0.5            2.09                -0.524
*                0.0            1.57                 0.000
*                0.5            1.05                 0.524
*                1.0            0.00                 1.570
**********************************************************************************
V1  1  0  0
R1  1  0  1
B2  2  0  V = {ASIN(V(1,0))}
R2  2  0  1
B3  3  0  V = {ACOS(V(1,0))}
R3  3  0  1
.DC V1 -0.99 0.99 0.1
.PRINT DC V(1) V(2) V(3)
.OPTIONS ACCT LIST
.END
```

ChileSPICE Simulation Results for the ASIN & ACOS Netlist



3.1.3 Test Circuit for the Tangent and Arctangent Functions

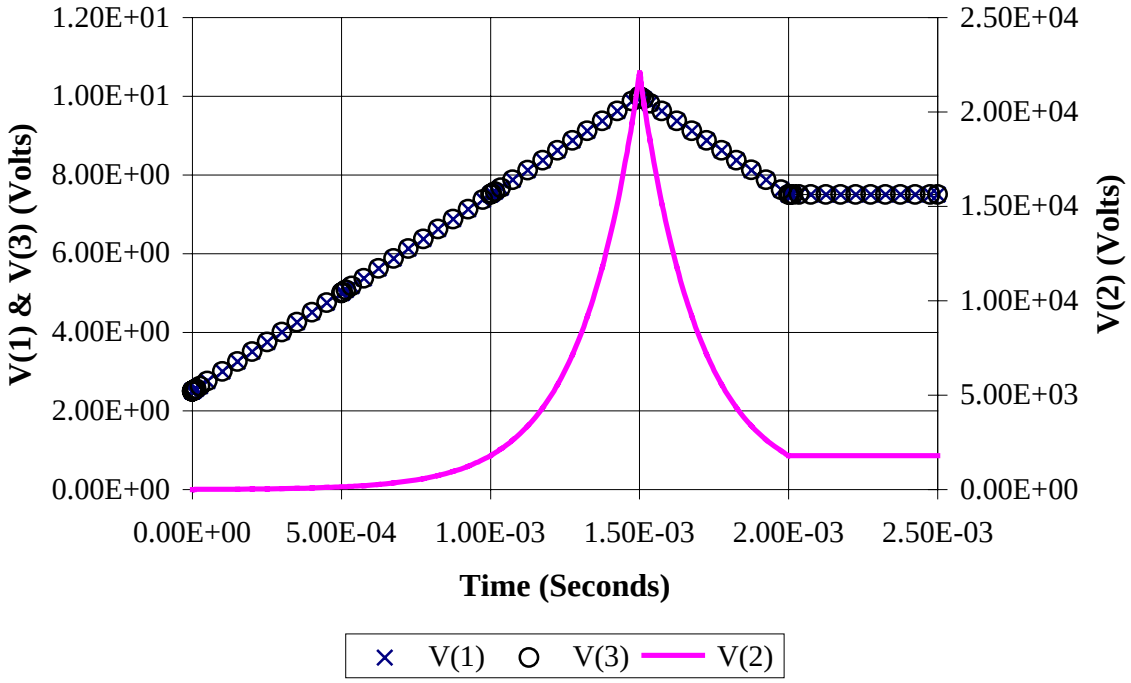
```
**********************************************************************************
* Tier No.:     1
* Directory/Circuit Name: ABM_ATAN_TAN/atan_tan.cir
* Description:  Test of analog behavioral modeling tangent and arctangent functions.
* Input: VS
* Output: V(1), V(2), V(3)
* Analysis:
*       A sinusoidal source voltage, VS or V(1),  with a 1V amplitude and 1KHZ  freq.  is
*       the input to the circuit.  Two nonlinear dependent voltage sources are used to define
*       the functions as follows:
*               V(2)=B2=TAN(V(1)) = tangent of input sine function = V(2)
*               V(3)=B3=ATAN(V(2)) = inverse tangent of B2 (or TAN(VS))=V(1)
*                    = value of the input source VS
*       where,
*               V(1)=VS=SIN(0 1 1KHZ) = SIN(2*PI*(1KHZ)*(TIME))
*       A transient analysis is performed and the output recorded is the node voltages
*       defined by the input source, V(1), the tangent, V(2),  and arctangent, V(3), functions.
*
*       This table is a set of hand calculations for the TAN and ATAN functions
*       TIME            V(1)            V(2)=TAN(V(1))      V(3)=ATAN(TAN(V(1)))
*       (Seconds)       (Volts)         (Volts)             (Volts)
*       0.00            0.00            0.00                0.00
*       0.25E-3         1.00            1.55                1.00
*       0.5E-3          8.98E-11        8.98E-11            8.98E-11
*       0.75E-3         -1.00           -1.55               -1.00
*       1.0E-3          -1.8E-10        1.8E-10             1.8E-10
*       1.25E-3         1.00            1.55                1.00
*       1.5E-3          2.69E-10        2.69E-10            2.69E-10
*       1.75E-3         -1.00           -1.55               -1.00
*       2.00E-3         -3.59E-10       -3.59E-10           -3.59E-10
*
**********************************************************************************
VS  1  0  SIN(0 1 1KHZ)
R1  1  0  1
B2  2  0  V={TAN(V(1,0))}
R2  2  0  1
B3  3  0  V={ATAN(V(2,0))}
R3  3  0  1
.TRAN 0.1MS 2MS
.PRINT TRAN V(1) V(2) V(3)
.OPTIONS ACCT
.END
```


ChileSPICE Simulation Results for the TAN & ATAN Circuit
Voltage (Volts)
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
0
0.0005
0.001
0.0015
0.002
Time (Seconds)
V(1)
V(2)
V(3)

3.1.4 Test Circuit for the Exponential and Natural Log Functions

```
**********************************************************************************
* Tier No.:     1
* Directory/Circuit Name: ABM_EXPLN/exp_ln.cir
* Description:  Test of analog behavioral modeling exponential and natural log functions
* Input: VS
* Output: V(1), V(2), V(3)
* Analysis:
*         The input voltage, VS, is a piece wise linear source with specified time
*         and voltage pairs.  Two nonlinear dependent voltage sources are used to
*         define the functions as follows:
*                 V(2)=B2=EXP(V(1)) = exponent of input voltage = EXP(V(1))
*                 V(3)=B3=LN(V(2)) = ln of B2 (EXP function) = V(1)
*         A transient analysis is performed and the output recorded is the node voltages
*        defined by the input source, V(1),  the exponential, V(2), and natural log , V(3),
*        functions.
*
*        This table is a set of hand calculations for the EXP and LN functions:
*        TIME            V(1)          EXP(V(1))          LN(EXP(V(1))
*        (Seconds)       (Volts)       (Volts)            (Volts)
*        0.00E-3         2.5           12.182             2.5
*        0.50E-3         5.0           148.413            5.0
*        1.00E-3         7.5           1808.042           7.5
*        1.50E-3         10.0          22026.47           10.0
*        2.00E-3         7.5           1808.042           7.5
*        2.50E-3         7.5           1808.042           7.5
*
**********************************************************************************
VS  1  0  PWL(0 2.5V 0.5MS 5V 1MS 7.5V 1.5MS 10V 2MS 7.5V)
R1  1  0  1
B2  2  0  V = {EXP(V(1,0))}
R2  2  0  1
B3  3  0  V = {LN(V(2,0))}
R3  3  0  1
.TRAN 0.02MS 2.5MS
.PRINT TRAN V(1) V(2) V(3)
.OPTIONS ACCT
.END
```

ChileSPICE Simulations Results for the EXP & LN Circuit



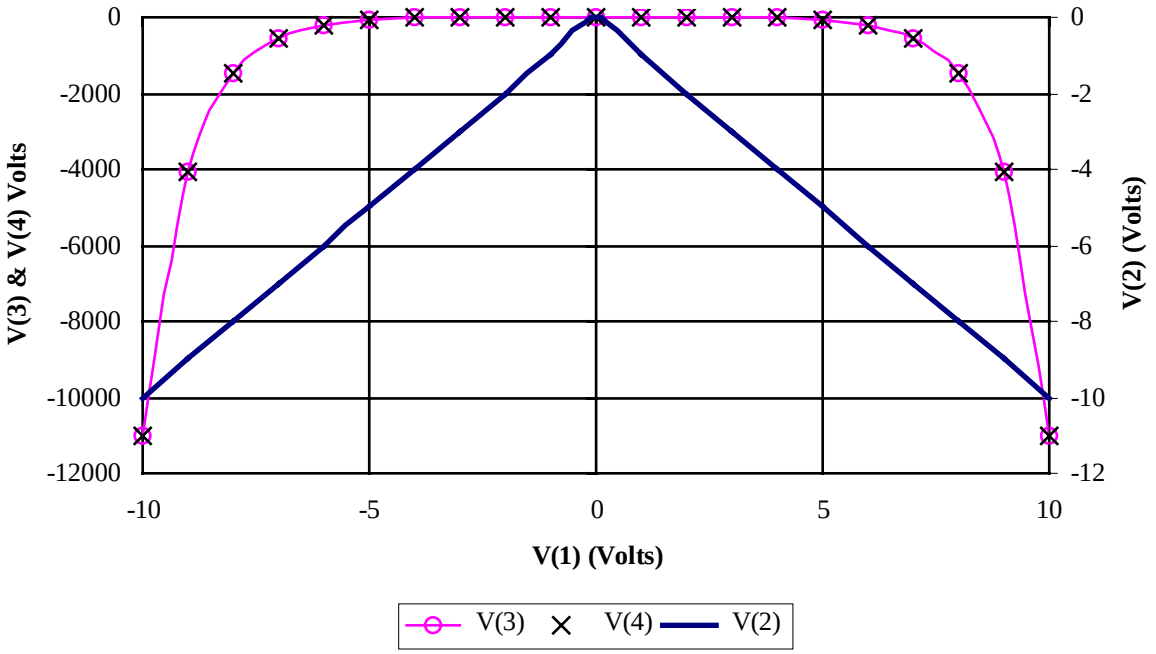
3.1.5 Test Circuit for the Hyperbolic Functions

```
**********************************************************************************
* Tier No.:     1
* Directory/Circuit Name:  ABM_HYP/hyp.cir
* Description:  Test of the analog behavioral modeling functions:
*         SINH, COSH, TANH, ASINH, ACOSH, ATANH
* Input: V(1)
* Output:  V(1), V(2), V(3), V(4), V(5),V(6), V(7),  V(8), V(9), V(10), V(11)
*         V(12), V(13), V(14)
* Analysis:
*         Nonlinear dependent voltage sources are used to define the functions.  See
*         comments in netlist below for description of how functions are used
*
*         The following tables are hand calculations of the functions calculated in this netlist:
*
*         V(1)    V(2)=(-ABS(V(1)))    SINH(V(2))          COSH(V(2))          TANH(V(2))
*         -10             -10          -11013.23287        11013.23292         -0.999999996
*          -8             -8           -1490.478826        1490.479161         -0.999999775
*          -6              -6          -201.7131574        201.7156361         -0.999987712
*          -4             -4           -27.2899172         27.30823284         -0.9993293
*          -2             -2           -3.626860408        3.762195691         -0.96402758
*           0              0            0                  1                   0
*          2              -2           -3.626860408        3.762195691         -0.96402758
*          4              -4           -27.2899172         27.30823284         -0.9993293
*          6              -6           -201.7131574        201.7156361         -0.999987712
*          8              -8           -1490.478826        1490.479161         -0.999999775
*         10              -10          -11013.23287        11013.23292         -0.999999996
*
*         V(1)    V(2)/100=-ABS(V(1))/100     ASINH(V(2)/100)     ATANH(V(2)/100)
*         -10             -0.1                -0.099834079        -0.100335348
*         -8              -0.08               -0.079914911        -0.080171325
*         -6              -0.06               -0.059964058        -0.060072156
*         -4              -0.04               -0.039989341        -0.040021354
*         -2              -0.02               -0.019998667        -0.020002667
*          0               0                   0                   0
*          2              -0.02               -0.019998667        -0.020002667
*          4              -0.04               -0.039989341        -0.040021354
*          6              -0.06               -0.059964058        -0.060072156
*          8              -0.08               -0.079914911        -0.080171325
*         10              -0.1                -0.099834079        -0.100335348
*
*         V(1)            ACOSH(V(1))   Note: ACOSH(V(1))=0 for V(1)<=1
*         -10                   0
*         -8                    0
*         -6                    0
*         -4                    0
*         -2                    0
```

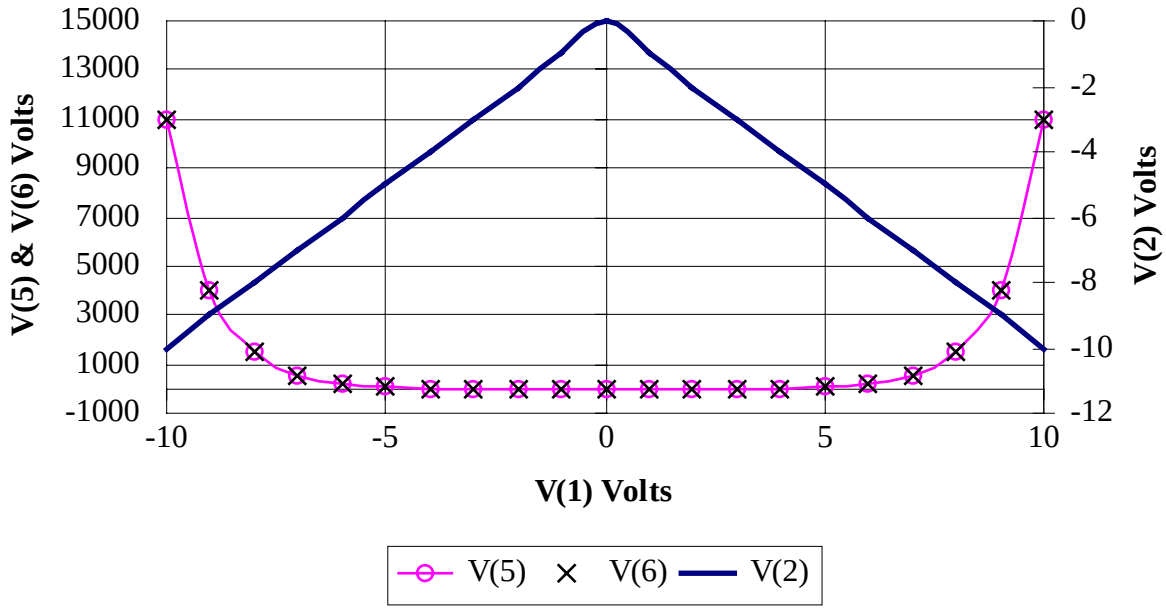
```
*       0                       0
*       2                       0
*       4                       2.063437069
*       6                       2.47788873
*       8                       2.768659383
*       10                      2.993222846
*
********************************************************************************
* Declaration of parameters and functions
.PARAM  HALF=0.5
.PARAM  K=100
.FUNC INVCOSH(A)   {LN( A + SQRT((A**2  - 1)))}
.FUNC INVTANH(A,B,C) {A * LN((1 + (B/C))/(1 - (B/C)))}
* DC source Whose VALUES are used to evaluate the function defined by
* B2 (Voltage @ node * 2, V(2)=(-ABS(V(1))),
* V1 is stepped from –10V to 10V as indicated on the .DC statement line
V1   1  0  0
R1   1  0  1
* Absolute value function that uses V1 to produce a triangular waveform
B2   2  0  V = {-(ABS(V(1,0)))}
R2   2  0  1
* Hyperbolic sine function:  B3=V(3)={SINH(V(2))}
B3   3  0  V={SINH(V(2))}
R3   3  0  1
* Mathematical expression for the hyperbolic sine function: B4=V(4); expected results identical
* to B3 results
B4   4  0  V={(EXP(V(2)) - EXP(-(V(2))))/2}
R4   4  0  1
* Hyperbolic cosine function: B5=V(5)={COSH(V(2))}
B5   5  0  V={COSH(V(2))}
R5   5  0  1
* Mathematical expression for the hyperbolic cosine function: B6=V(6); expected results
* identical to B5 results
B6   6  0  V={(EXP(V(2)) + EXP(-(V(2))))/2}
R6   6  0  1
* Hyperbolic tangent function: B7=V(7)={TANH(V(2))}
B7   7  0  V={TANH(V(2))}
R7   7  0  1
* Mathematical expression for the hyperbolic tangent function: B8=V(8); expected results
* identical to B7 results
B8   8  0  V={(EXP(V(2)) - EXP(-(V(2))))/(EXP(V(2)) + EXP(-(V(2))))}
R8   8  0  1
* Inverse Hyperbolic sine function: B9=V(9)={ASINH(V(2))}
B9   9  0  V={ASINH(V(2))}
R9   9  0  1
* Mathematical expression for the inverse hyperbolic sine function: B10=V(10); expected results
* identical to B9 results
B10  10 0  V={LN(V(2) + SQRT((V(2))**2  + 1 ))}
```

```
R10  10 0  1
* Inverse Hyperbolic cosine function: B11=V(11)=ACOSH(V(1)) FOR V(1)  >= 1
* Use if statement to eliminate computing values less than or equal to 1; function is chosen to be
* positive
B11  11 0  V={IF(V(1)<= 1, 0, ACOSH(V(1)))}
R11  11 0  1
* Mathematical expression for the inverse hyperbolic cosine:
* B12=V(12)
* Defined above by the .func INVCOSH Domain: x >= 1
* Use if statement to eliminate computing values less than or equal to 1; function is chosen to be
* positive expected results identical to B11
B12  12 0  V={IF(V(1)<= 1, 0, INVCOSH(V(1)))}
R12  12 0  1
* Inverse Hyperbolic tangent function: B13=V(13)=ATAN(V(2)/K)
* Use if statement to eliminate computation of positive values that are less than 1 (note: K
* parameter used to make V(2) less than 1)
B13  13 0  V={IF((ABS(V(2))/K) < 1, ATANH(V(2)/K), 0)}
R13  13 0  1
* Mathematical expression for the inverse hyperbolic tangent: B14=V(14)
* Defined above by the .func INVTANH
* Domain: |x| < 1
* Use if statement to eliminate computation of positive values that are less than 1 (note: K
* parameter used to make V(2) less than 1.  The expected results should be identical to B13
B14  14 0  V={IF((ABS(V(2))/K) < 1, INVTANH(HALF,V(2),K), 0)}
R14  14 0  1
.DC V1 -10 10 1
.PRINT DC V(1) V(2) V(3) V(4) V(5) V(6) V(7)
+        V(8) V(9) V(10) V(11) V(12) V(13) V(14)
.OPTIONS ACCT
.END
```

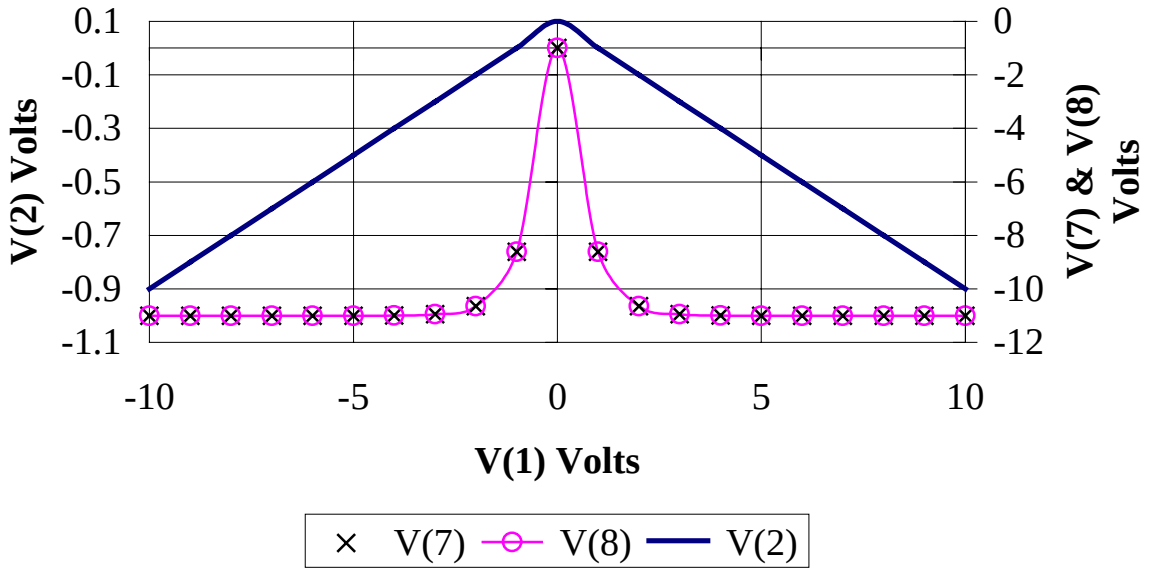
ChileSPICE Simulation Results for the Hyperbolic Functions Circuit
SINH



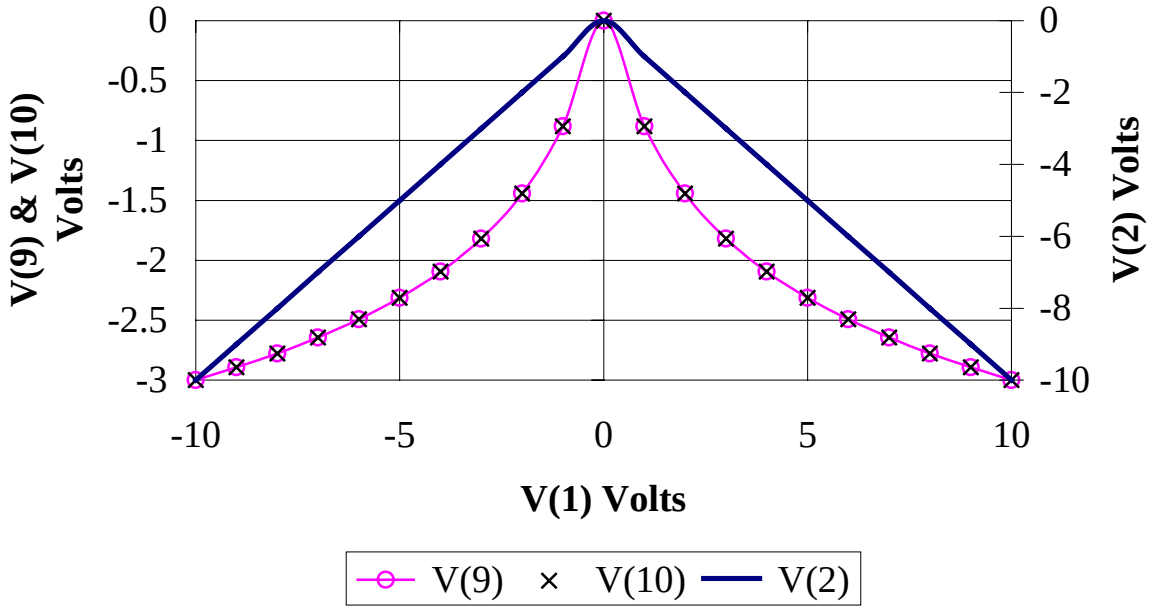
ChileSPICE Simulation Results for the Hyperbolic Functions Circuit
COSH



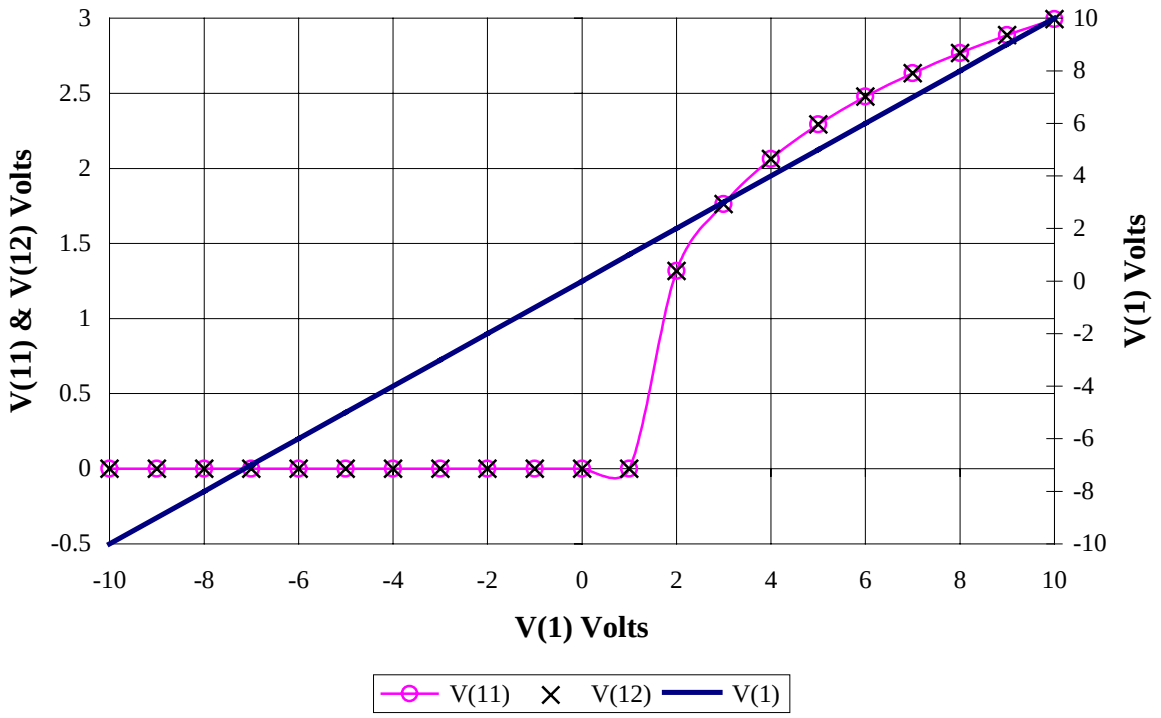
ChileSPICE Simulation Results for the Hyperbolic Functions Circuit
TANH



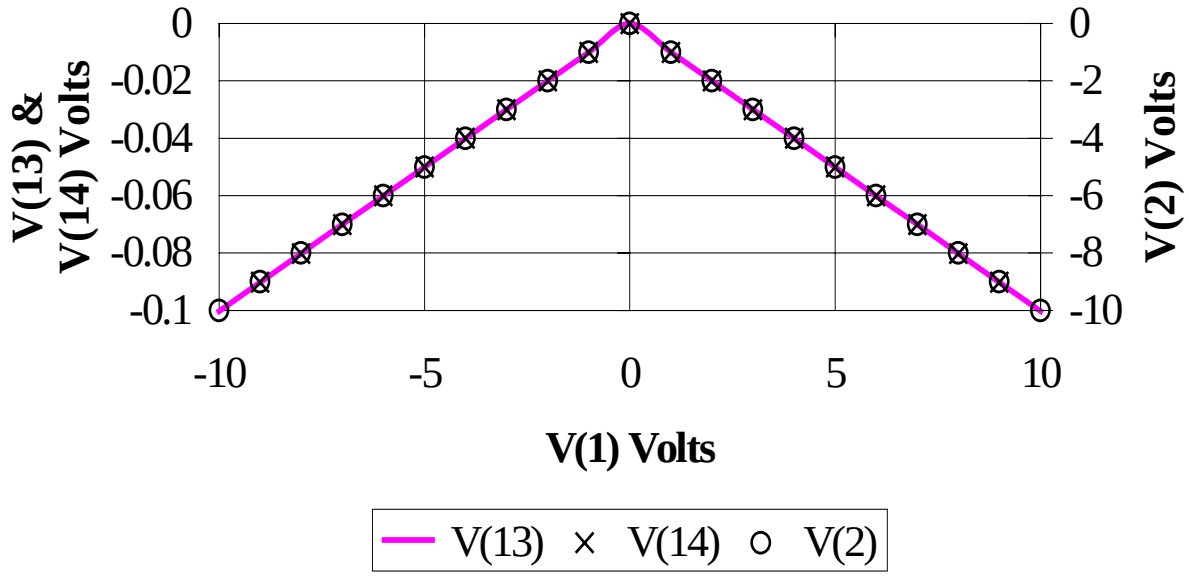
ChileSPICE Simulation Results for the Hyperbolic Functions Circuit
ASINH



ChileSPICE Simulation Results for the Hyperbolic Functions Circuit
ACOSH

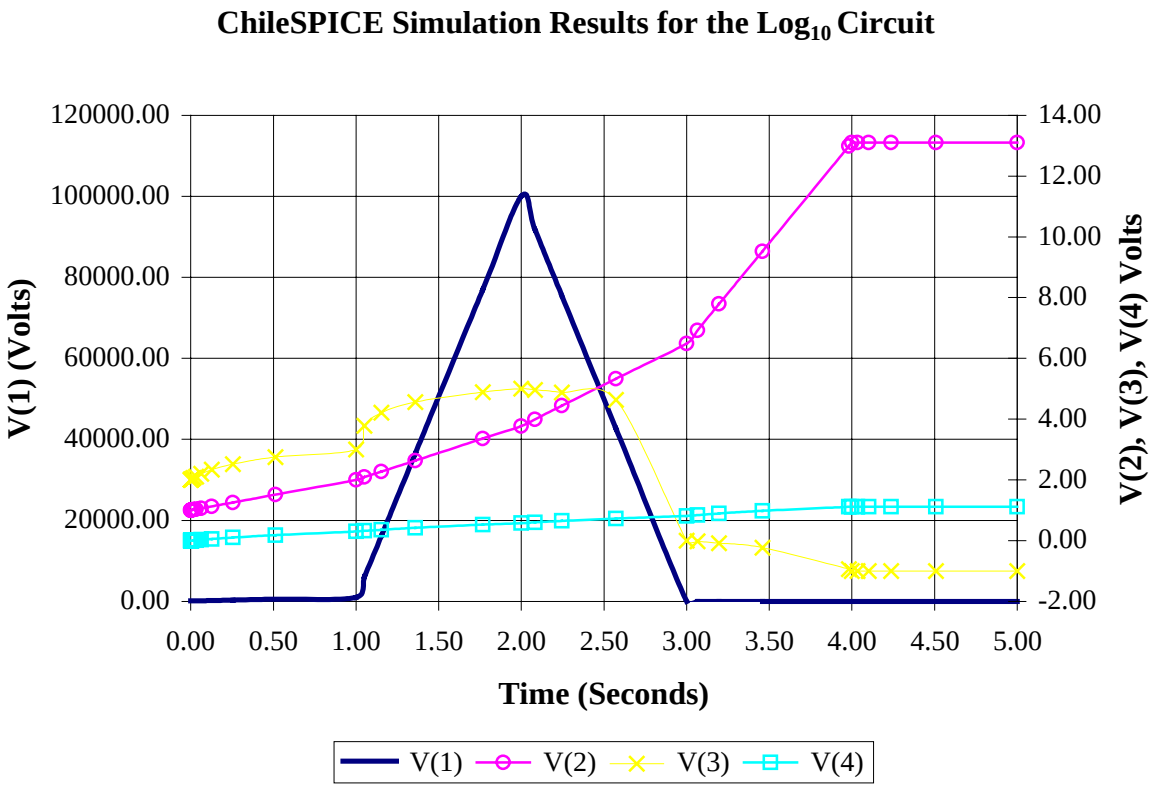


ChileSPICE Simulation Results for the Hyperbolic Functions Circuit
ATANH



3.1.6 Test Circuit for the Log Base 10 Function

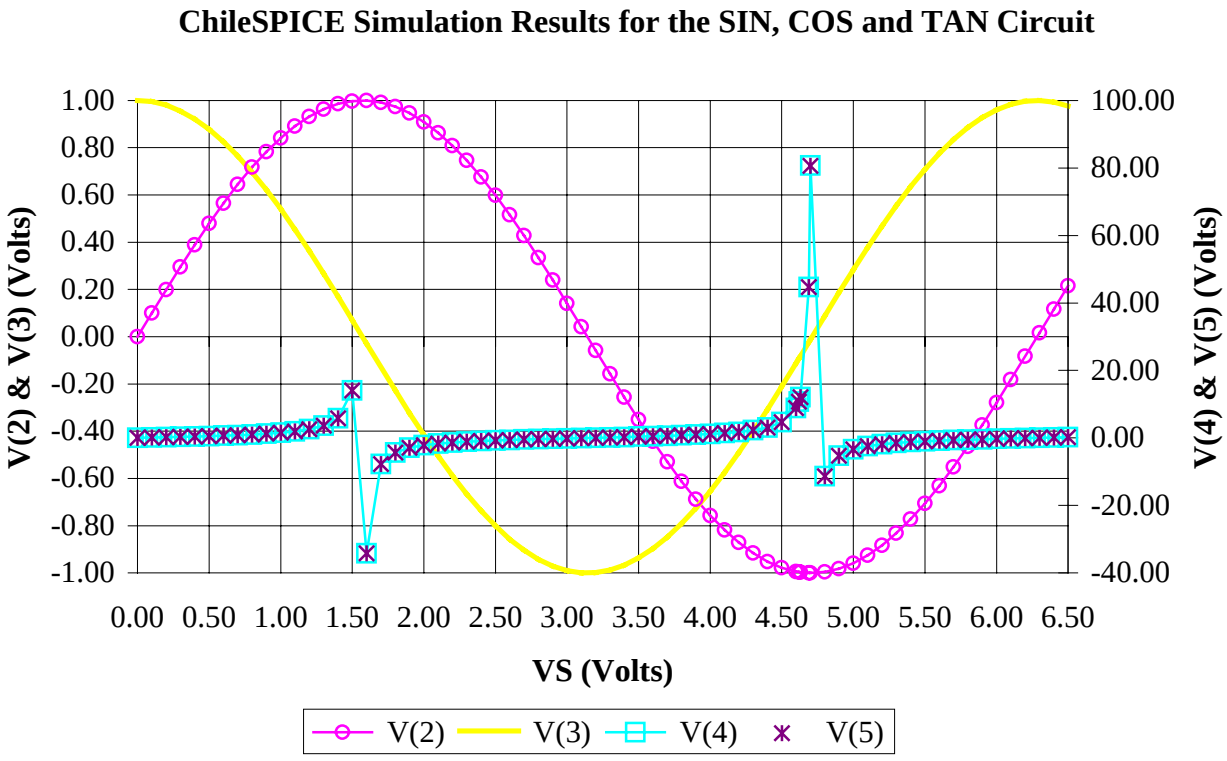
```
**********************************************************************************
* Tier No.:     1
* Directory/Circuit Name: ABM_LOG/log.cir
* Description:  Test of the analog behavioral modeling log function.
* Input: V1, V2
* Output:  V(1), V(2), V(3), V(4)
* Analysis:
*       Two piece-wise linear sources are used to define voltages at various times.
*       These sources are defined as V1=V(1) and V2=V(2), respectively.
*       Two nonlinear dependent voltage sources are used to define the function as
*       follows:
*               V(3)=B3=LOG(V(1))
*               V(4)=B4=LOG(V(2))
*       The values for the PWL sources are chosen such that the log functions are
*       Evaluated for both large [V1=V(1)] and small [V2=V(2)] values.
*       This table is a set of hand calculations for the Log10 function.
*       Note:  The results are the given and expected values for the indicated node voltages.
*
*       TIME(Seconds)           V(1) (Volts)        V(3)=LOG(V(1)) (Volts)
*               0               100                 2
*               1               1000                3
*               2               100000              5
*               3               1                   0
*               4               0.1                 -1
*               5               0.1                 -1
*
*       TIME(Seconds)           V(2) (Volts)        V(4)=LOG(V(2)) (Volts)
*               0               1                   0
*               1               2                   0.301029996
*               2               3.77                0.57634135
*               3               6.49                0.812244697
*               4               13.1                1.117271296
*               5               13.1                1.117271296
**********************************************************************************
V1 1  0  PWL(0S 100V   1S 1000V   2S 1E5V  3S 1V   4S 0.1V)
R1 1  0  1
V2 2  0  PWL(0S 1V   1S 2V   2S 3.77V   3S 6.49V  4S 13.1V)
R2 2  0  1
B3 3  0  V = {LOG(V(1))}
R3 3  0  1
B4 4  0  V = {LOG(V(2))}
R4 4  0  1
.TRAN 1S 5S 0 1S
.PRINT TRAN V(1) V(2) V(3) V(4)
.OPTIONS ACCT
.END
```


ChileSPICE Simulation Results for the Log10 Circuit
120000.00
100000.00
80000.00
60000.00
40000.00
20000.00
0.00
V(1) (Volts)
14.00
12.00
10.00
8.00
6.00
4.00
2.00
0.00
-2.00
V(2), V(3), V(4) Volts
0.00
0.50
1.00
1.50
2.00
2.50
3.00
3.50
4.00
4.50
5.00
Time (Seconds)
V(1)
V(2)
V(3)
V(4)

3.1.7 Test Circuit for the Sine, Cosine and Tangent Functions

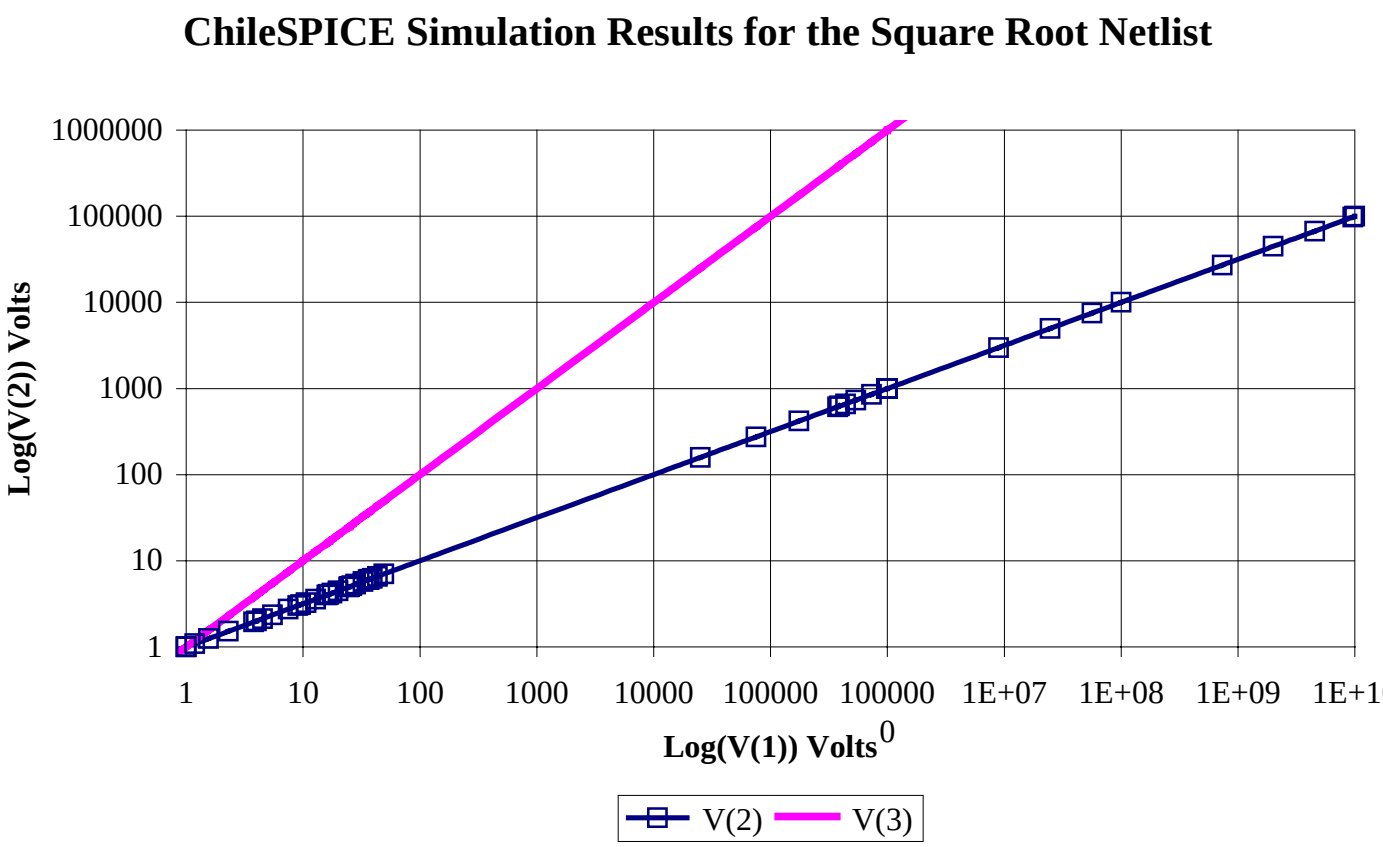
```
**********************************************************************************
* Tier No.:     1
* Directory/Circuit Name: ABM_SCT/sct.cir
* Description:  Test of the analog behavioral modeling sine, cosine and tangent functions.
* Input:  VS
* Output: V(2), V(3), V(4), V(5)
* Analysis:
*       A DC voltage source, VS or V(1),  is used as the circuit input.  Four nonlinear dependent
*       voltage sources are used to define the functions as follows:
*               V(2)=B2=SIN(V(1)) = sine of input source
*               V(3)=B3=COS(V(1)) = cosine of input source
*               V(4)=B4=TAN(V(1)) = tangent of input source
*               V(5)=B5=V(2)/V(3) = mathematical evaluation of the tangent function(SIN/COS)
*
*       This table is a set of hand calculations for the SIN, COS and TAN functions
*       X               SIN(X)              COS(X)              TAN(X)
*       0               0                   1                   0
*       0.5             0.479425539         0.877582562         0.54630249
*       1               0.841470985         0.540302306         1.557407725
*       1.5             0.997494987         0.070737202         14.10141995
*       1.6             0.999573603         -0.029199522        -34.23253274
*       2               0.909297427         -0.416146837        -2.185039863
*       2.5             0.598472144         -0.801143616        -0.747022297
*       3               0.141120008         -0.989992497        -0.142546543
*       3.1             0.041580662         -0.99913515         -0.041616655
*       3.2             -0.058374143        -0.998294776        0.058473854
*       4               -0.756802495        -0.653643621        1.157821282
*       4.6             -0.993691004        -0.112152527        8.860174896
*       4.62            -0.995735173        -0.092257602        10.7929878
*       4.63            -0.996607947        -0.082295803        12.11007009
*       4.69            -0.999749377        -0.02238711         44.65736663
*       5               -0.958924275        0.283662185         -3.380515006
*       5.5             -0.705540326        0.708669774         -0.995584052
*       6               -0.279415498        0.960170287         -0.291006191
*       6.2             -0.083089403        0.996542097         -0.083377715
*       6.5              0.215119988        0.976587626         0.2202772
**********************************************************************************
VS  1  0  0
R1  1  0  1
B2  2  0  V = {SIN(V(1,0))}
R2  2  0  1
B3  3  0  V = {COS(V(1,0))}
R3  3  0  1
B4  4  0  V = {TAN(V(1,0))}
R4  4  0  1
B5  5  0  V = {V(2)/V(3)}
```

```
R5  5  0  1
.DC VS 0 6.5 0.1
.PRINT DC V(2) V(3) V(4) V(5)
.OPTIONS ACCT
.END
```



3.1.8 Test Circuit for the Square Root Function

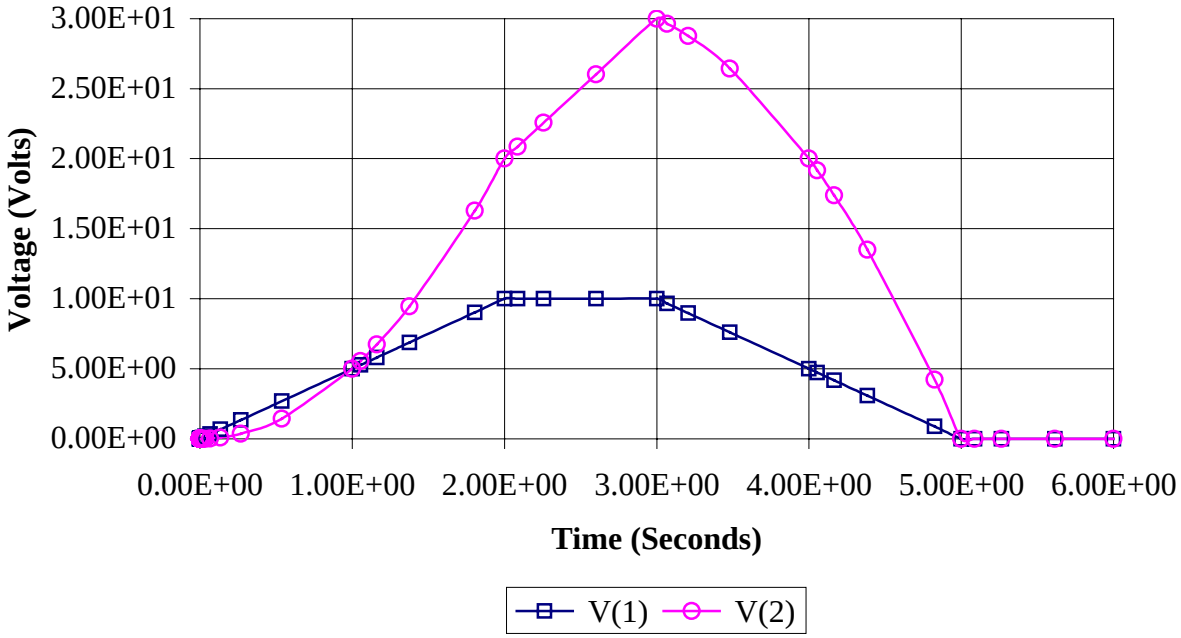
```
********************************************************************************
* Tier No.:     1
* Directory/Circuit Name: ABM_SQRT/sqrt.cir
* Description: Test of the analog behavioral modeling square root function.
* Input: VS
* Output: V(1), V(2), V(3)
* Analysis:
*       A piece-wise linear input voltage source, VS or V(1) is used to define various voltages in
*       time.
*       Two nonlinear dependent voltage sources are used to define the functions as follows:
*               V(2)=B2=SQRT(V(1)) = square root of V1
*               V(3)=B3=(V(2))**2  = value of B2 source squared = V1
*
*       This table shows hand calculations for the square root and square functions
*       The X values represent the values of VS
*
*       V(1)            SQRT(V(1))          V(1)*V(1)
*       0               0                   0
*       1               1                   1
*       4               2                   4
*       9               3                   9
*       16              4                   16
*       25              5                   25
*       36              6                   36
*       49              7                   49
*       390625          625                 3.91E05
*       998001          999                 998001
*       1.00E+06        1000                1000000
*       1.00E+08        10000               100000000
*       1.00E+10        100000              10000000000
*
********************************************************************************
VS   1  0  PWL(0S 0V  1S 1V 2S 4V  3S 9V  4S 16V   5S 25V  6S 36V  7S 49V  8S 390625V
+               9S 998001V 10S 1E6V 11S 1E8V 12S 1E10V)
R1   1  0  1
* SOURCE THAT TAKES THE SQUARE ROOT OF V1
B2   2  0  V = {SQRT(V(1))}
R2   2  0  1
* SOURCE THAT SQUARES THE VALUE OF B2
* RESULTING IN THE ORIGINAL VALUE OF V1
B3   3  0  V = {V(2) * *2}
R3   3  0  1
.TRAN 1S 12S 0 1S
.PRINT TRAN V(1) V(2) V(3)
.OPTIONS ACCT
.END
```


ChileSPICE Simulation Results for the Square Root Netlist
Log(V(2)) Volts
1000000
100000
10000
1000
100
10
1
1
10
100
1000
10000
100000
100000
1E+07
1E+08
1E+09
1E+10
Log(V(1)) Volts
0
V(2)
V(3)

3.1.9 Test Circuit for the F(Y,T) Functionality

```
**********************************************************************************
* Tier No.:     1
* Directory/Circuit Name: ABM_TIME/time.cir
* Description:  Test of the analog behavioral modeling function for using time as a variable
*               defining a nonlinear dependent voltage source
* Input: VS=V(1)
* Output: V(1), V(2)
* Analysis:
*      A piecewise linear  voltage source, VS or V(1),  is used as the circuit input.
*      Nonlinear dependent voltage sources are used to define the function as follows:
*           V(2)=B2=V(1) * TIME
*      where, V(1) is the input voltage and time is the simulation time specified
*      on the .tran line.  The resulting values for V(2) are the product of V(1),
*
*      This table is a set of hand calculations for the B1=V(2) function:
*           TIME              VS=V(1)       V(2)=V(1)*TIME
*           0s                0V            0V
*           1s                5V            5V
*           2s                10V           20V
*           3s                10V           30V
*           4s                5V            20V
*           5s                0V            0V
*           6s                0V            0V
*
**********************************************************************************
VS 1 0 PWL(0S 0V  1S 5V  2S 10V  3S 10V  4S 5V  5S 0V  6S 0V)
R1 1 0 1K
B2 2 0 V=(V(1) * TIME)
R2 2 0 1K
.TRAN 0S 6S 0S 1S
.PRINT TRAN V(1) V(2)
.OPTION ACCT
.END
```

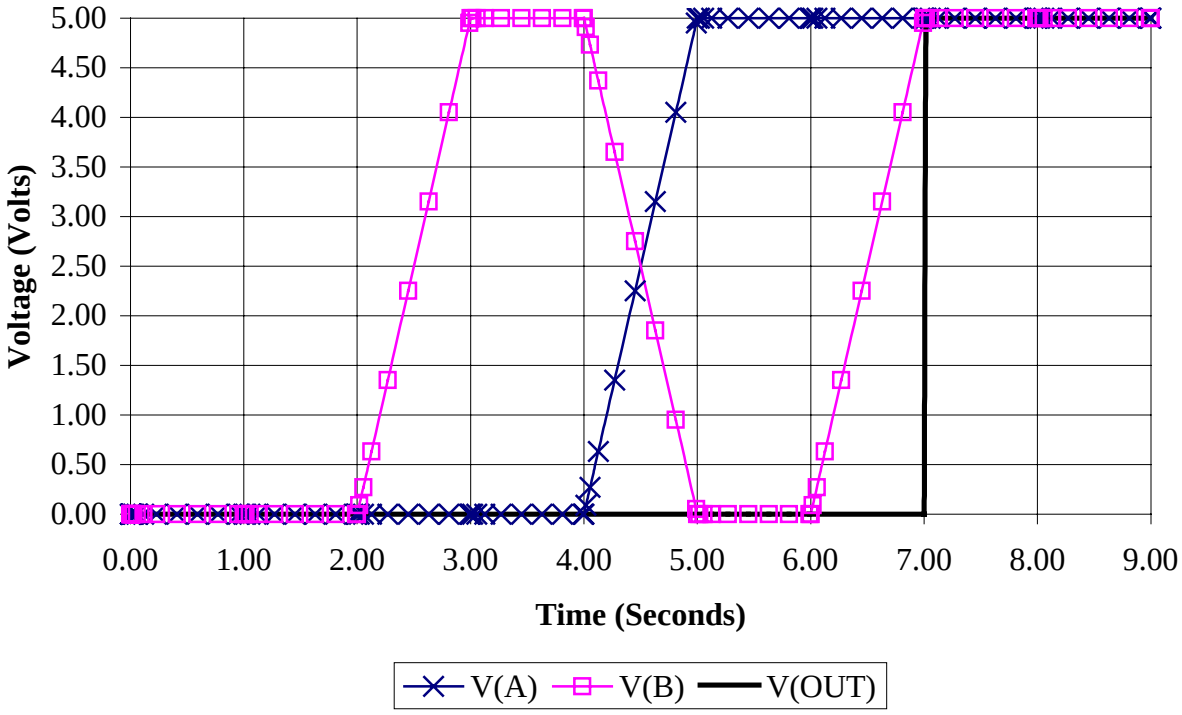
ChileSPICE Simulation Results for the F(Y,T) Circuit



3.1.10 Test Circuit for the AND Gate

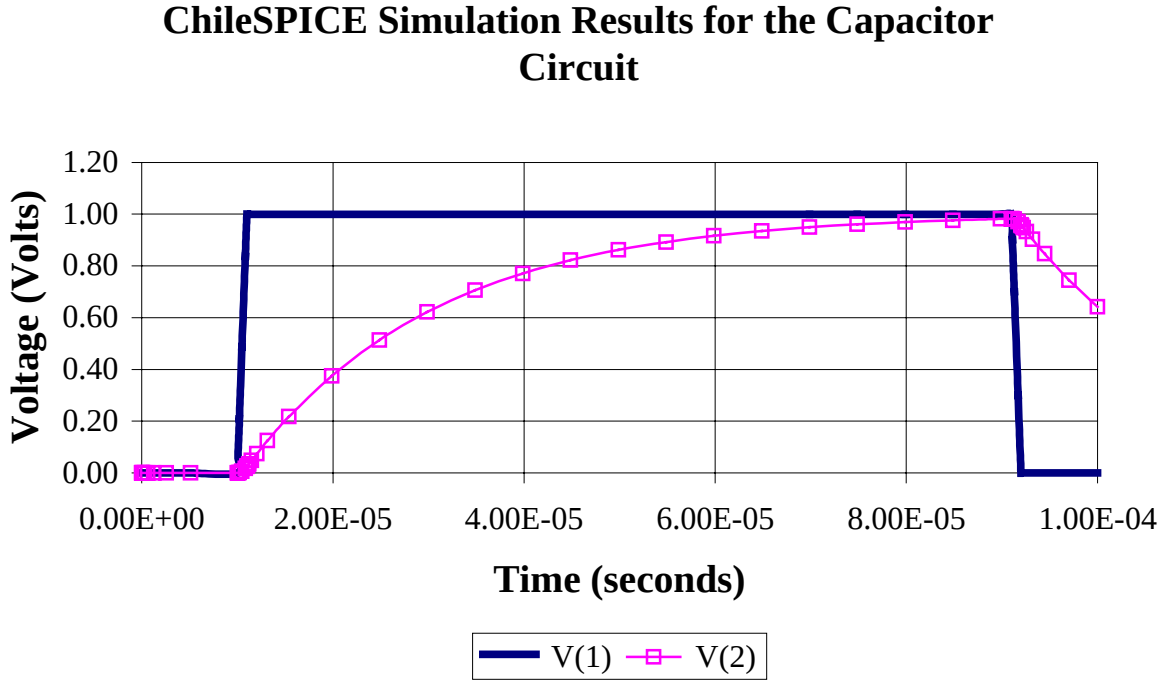
```
**********************************************************************************
* Tier No.:      1
* Directory/Circuit Name: AND/and.cir
* Description:  Test of the digital AND gate used for defining logic circuits.
* Input: VA=V(A), VB=V(B)
* Output: V(A), V(B), V(OUT)
* Analysis:
*       Two piecewise linear  voltage sources, V(A) and V(B),  are used as logic inputs to an
*       AND gate, which is defined internal to the code by a subcircuit.  Parameters are defined
*       in the netlist (by the .PARAMS statement) and passed into the AND subcircuit.  The
*       subcircuit uses the parameters to establish the following values of the output voltage:
*       Rise Time = default_rise= rise/fall output voltage = 1ns
*       Margin = default_margin = margin for output to exceed min/max logic levels = 0.5V
*       High = default_high + default_margin = logic high voltage = 4.5V + 0.5V  = 5V
*       Low = default_low - default_margin = logic low voltage = 0.5V - 0.5V = 0V
*       The logic for the AND gate is the output is high if and only if both inputs are high; for all
*       other combination, the output is low.  This truth table shows the AND expected output
*       for the given A and B time dependent inputs.
*
*       TIME        A(Volts)        B(Volts)        OUT(Volts)
*       0S          0               0               0
*       1S          0               0               0
*       2S          0               0               0
*       3S          0               5               0
*       4S          0               5               0
*       5S          5               0               0
*       6S          5               0               0
*       7S          5               5               5
*       8S          5               5               5
*       9S          5               5               5
*       NOTE: Low = 0V  High=5V
**********************************************************************************
* Set digital default parameters
.PARAM default_rise=1ns
.PARAM default_delay=0
.PARAM default_low=0.5V
.PARAM default_high=4.5V
.PARAM default_margin=0.5V
* Gate Inputs
VA A 0 0V PWL(0 0  1 0  2 0  3 0  4 0  5 5  6 5  7 5  8 5)
VB B 0 0V PWL(0 0  1 0  2 0  3 5  4 5  5 0  6 0  7 5  8 5)
X_AND A B OUT AND
.TRAN 1S 9S
.PRINT TRAN V(A) V(B) V(OUT)
.OPTIONS ACCT
.END
```

ChileSPICE Simulation Results for the AND Gate Circuit



3.1.11 Test Circuit for the Capacitor

```
**********************************************************************************
* Tier No.:  1
* Directory/Circuit Name:  CAPACITOR/capacitor.cir
* Description:  Test of the capacitor model using a simple RC circuit configuration.
* Input:  VIN
* Output: V(1), V(2)
* Analysis:
*       A series RC circuit is connected to a pulsed voltage source that goes from
*       0V to 1V after a 10us delay, with rise and fall times of 1us.  The capacitor
*       voltage should reach 90% of its maximum value, 1V,  in
*             time = (3*R*C) + rise + delay
*                  = (3 * 1E3 * 20E-9) + 1E-6 + 10E-6
*                  = 71us
*               where R=1E3 and C=20E-9
*       Therefore, at 71us, the capacitor voltage should be at least 0.9V.
*       A transient analysis of the circuit voltage versus time is performed to determine
*       the capacitor voltage, V(2).
**********************************************************************************
VIN  1 0 PULSE(0 1 10U 1U 1U 80U)
R    1 2 1K
C    2 0 20N
.TRAN 5U 100U 0 5U
.PRINT TRAN V(1) V(2)
.OPTION  ACCT
.END
```


ChileSPICE Simulation Results for the Capacitor Circuit
Voltage (Volts)
1.20
1.00
0.80
0.60
0.40
0.20
0.00
0.00E+00
2.00E-05
4.00E-05
6.00E-05
8.00E-05
1.00E-04
Time (seconds)
V(1)
V(2)

3.1.12 Test Circuit for the Current Controlled Current Source (CCCS)

```
**********************************************************************************
Tier No.: 1
* Directory/Circuit Name:  CCCS/cccs.cir
* Description:  Test of current controlled current source, CCCS, model using a simple resistor
*       circuit.  A DC operating point analysis is performed to obtain the transfer function
*       characteristics of the circuit i.e., Rin, Rout, and voltage gain, Vout/Vin.
* Input: VS
* Output: V(2), V(3), Rin, Rout, V(3)/VS
* Analysis:
*       The CCCS, F, is a current source that is controlled by the current through the input
*       source, VS, and is defined as:
*               F= k*I=-3*I(VS)
*       where
*               I(VS) = VS/ (R1 + R2) = 20 / (4000) =       5mA
*       Therefore,
*               k*I(VS) = -3 * 5mA =                        -15mA
*       The current through the dependent source is divided evenly through resistors R3 and R4
*        (which are in parallel) giving –7.5 mA through each resistor. The -7.5mA currents go
*        from node 3 to node 0 (anode to cathode), making the voltage at node 3,
*               V(3) = -(R3*7.5mA) = -(500*7.5mA) =         -3.75V
*       Additionally, the voltage at node 2, Rin, Rout and the voltage gain (V(3)/VS) are:
*               V(2) = I * R2 = 5mA * 2500 =                12.5V
*               Rin  = R1 + R2 = 2500 + 1500 =              4K Ohms
*               Rout = R3||R4 = 500||500 =                  250 Ohms
*               GAIN = V(3)/V1 = -3.75/20 =                 -0.1875
**********************************************************************************
VS 1 0 20V
F 3 0 VS -3
R1 1 2 1500
R2 2 0 2500
R3 3 0 500
R4 3 0 500
.DC VS 20 20 1
.PRINT DC V(1) V(2) V(3)
.OPTIONS  ACCT
.TF V(3) VS
.END
```

ChileSPICE Simulation Results for the CCCS Circuit:

Current Controlled Current Source Circuit (CCCS)
DC transfer characteristic

Index	voltage_sweep	v(1)	v(2)	v(3)
0	2.000000E+01	2.000000E+01	1.250000E+01	-3.750000E+00

Transfer function information:
GAIN= transfer_function = -1.87500E-01
ROUT= output_impedance_at_v(3) = 2.500000E+02
RIN= v_input_impedance = 4.000000E+03

3.1.13 Test Circuit for the Current-Controlled Voltage Source (CCVS)

```
**********************************************************************************
* Tier No.: 1
* Directory/Circuit Name:  CCVS/ccvs.cir
* Description: Test of current controlled voltage source model using a simple resistor circuit.
*       A DC operating point analysis is performed to obtain the transfer function characteristics
*       of the circuit (i.e., Rin, Rout, and voltage gain, Vout/Vin).
*  Input: VIN
*  Output: V(2), V(3), V(4), I(VIN), Rin, Rout, V(4)/VIN
* Analysis:
*       The CCVS, H, is a voltage source controlled by the current through the input voltage
*       source, VIN. H is defined as k*I=-0.5*I.  The parameter k must have units of ohms for
*       the product of k and I to be volts.  Therefore,
*               H=V(3)=k*I(VIN)=-0.5*I(VIN)
*       where,
*               I(VIN) = -VIN / (R1 + R2) = 15 / (5 + 10) = -1mA
*       Note: I(VIN) is referenced from the negative to positive node of VIN,
*       which makes its value negative.  The voltage of the dependent source is
*               H = V(3) = -0.5 * -1mA = 0.5V
*       The voltages at nodes 2 and 4 are
*               V(2) = VIN * R2/(R1+R2)= 15 * 5/(5 + 10)=       5V
*               V(4) = V(3) * R4/(R3+R4)= 0.5V * 25/(25+25)=    0.25V
*       Additionally, Rin, Rout and the voltage gain are
*               Rin  = R1 + R2 = 10 + 5 =                       15 Ohms
*               Rout = R3||R4 = 25||25 =                        12.5 Ohms
*               Gain= V(4)/VIN = 0.25/15 =                      1.667E-2
**********************************************************************************
VIN 1 0 15V
H 3 0 VIN -0.5
R1 1 2 10
R2 2 0 5
R3 3 4 25
R4 4 0 25
.DC VIN 15 15 1
.PRINT DC V(2) V(3) V(4) I(VIN)
.OPTIONS ACCT
.TF V(4) VIN
.END
```

ChileSPICE Simulation Results for the CCVS Circuit:

Current-Controlled Voltage Source Circuit (CCVS)
DC transfer characteristic

Index	voltage_sweep V(1) = VIN	v(2)	v(3)	v(4)	vin_branch I(VIN)
0	1.500000E+01	5.000000E+00	5.000000E-01	2.500000E-01	-1.000000e+00

Transfer function information:
GAIN= transfer_function = 1.666667E-02
ROUT= output_impedance_at_v(4) = 1.250000E+01
RIN= vin_input_impedance = 1.500000E+01

3.1.14 Test Circuit for the Diode

```
**********************************************************************************
* Tier No.:  1
* Directory/Circuit Name: DIODE/DIODE.cir
* Description: Simple diode circuit to test the validity of the diode model.
* Input:  VIN
* Output: V(3), I(VMON)
* Analysis:
*       A diode is forward biased with a 5V input source, VIN.   With a 100fA saturation
*       current, Is,  the diode current, I(VMON) or Id,  and voltage, Vd,  are determined by the
*       following equations:
*               (1) Id=Is[exp(Vd/Vt) - 1]
*               (2) Vin=Id*R + Vd = Is[EXP(Vd/Vt)-1]*R + Vd
*               where,
*               Vt=25.86mV, R=2K, Is=100fA, Vin=5V
*
*       The diode voltage can be calculated by finding the value of Vd that makes equation (2)
*       true.  The diode current can be found by solving (1) after Vd is found.
*       Therefore,
*               Vd=0.6158V and Id=2.19mA
**********************************************************************************
VIN 1 0 DC 5V
R1 1 2 2K
D1 3 0 DMOD
VMON 2 3 0
.MODEL DMOD D (IS=100FA)
.DC VIN 5 5 1
.PRINT DC I(VMON) V(3)
.OPTION ACCT
.END
```

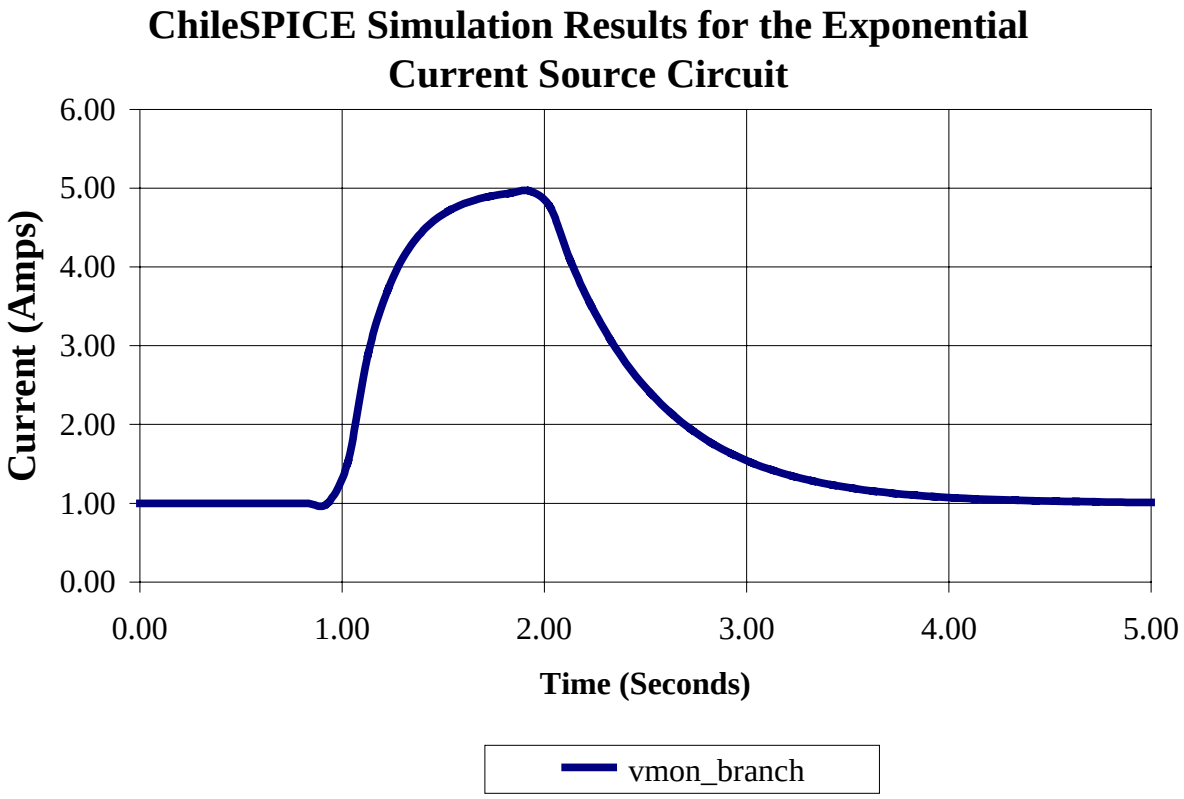
ChileSPICE Simulation Results for the DIODE Circuit:

Diode Circuit Netlist
DC transfer characteristic

Index	voltage_sweep VIN	vmon_branch ID	v(3) VD
0	5.000000E+00	2.192078E-03	6.158450E-01

3.1.15 Test Circuit for the Exponential Current Source

```
**********************************************************************************
* Tier No.: 1
* Directory/Circuit Name:  IEXP/IEXP.cir
* Description: Test of model for an independent current source.
* Input: IEXP
* Output: I(VMON)
* Analysis:
*       The input is described as an exponential time dependent current source, IEXP, that has an
*       initial value of 1A for the first 1s of the simulation.  The current rises exponentially from
*       1A to 5A within 1s, with a 0.2s rise time constant. It then decays from 5A to 1A with a
*        0.5s fall time constant.
*       The general format for an exp voltage source is
*               EXP (I1  I2  TD1  TAU1  TD2  TAU2)
*       Where,
*       I1=initial value=1A     I2=pulsed value=5A    TD1=rise time delay=1s
*       TAU1=rise time constant=0.2s TD2=fall delay time=2S TAU2=fall time constant=0.5S
*       The current is described by the following equation:
*               for  t between 0 and TD1
*               IEXP=I1
*               for t between TD1 and TD2
*               IEXP = i(t)=I1 + (I2-I1)*(1-EXP(-(TIME-TD1)/TAU1))
*               for t between TD2 and TSTOP
*               IEXP=i(t) + (I1-I2)*(1-EXP(-(TIME-TD2)/TAU2))
*
*       Therefore for given values of time, the expected current is:
*               T(seconds)      IEXP(T)
*               0               1
*               1               1
*               1.5             4.67
*               3               1.54
*               5               1
*
*       A zero volt source, VMON, is used as an ammeter to measure the
*       current from the IEXP source.   A resistor is used to provide a closed loop for current
*       flow.
**********************************************************************************
IEXP 0 1 EXP(1A 5A 1S 0.2S 2S 0.5S)
R 2 0 500
VMON 1 2 0
.TRAN 1S 5S
.OPTIONS ACCT
.PRINT TRAN I(VMON)
.END
```


ChileSPICE Simulation Results for the Exponential Current Source Circuit
Current (Amps)
6.00
5.00
4.00
3.00
2.00
1.00
0.00
0.00
1.00
2.00
3.00
4.00
5.00
Time (Seconds)
vmon_branch

3.1.16 Test Circuit for the Inductor

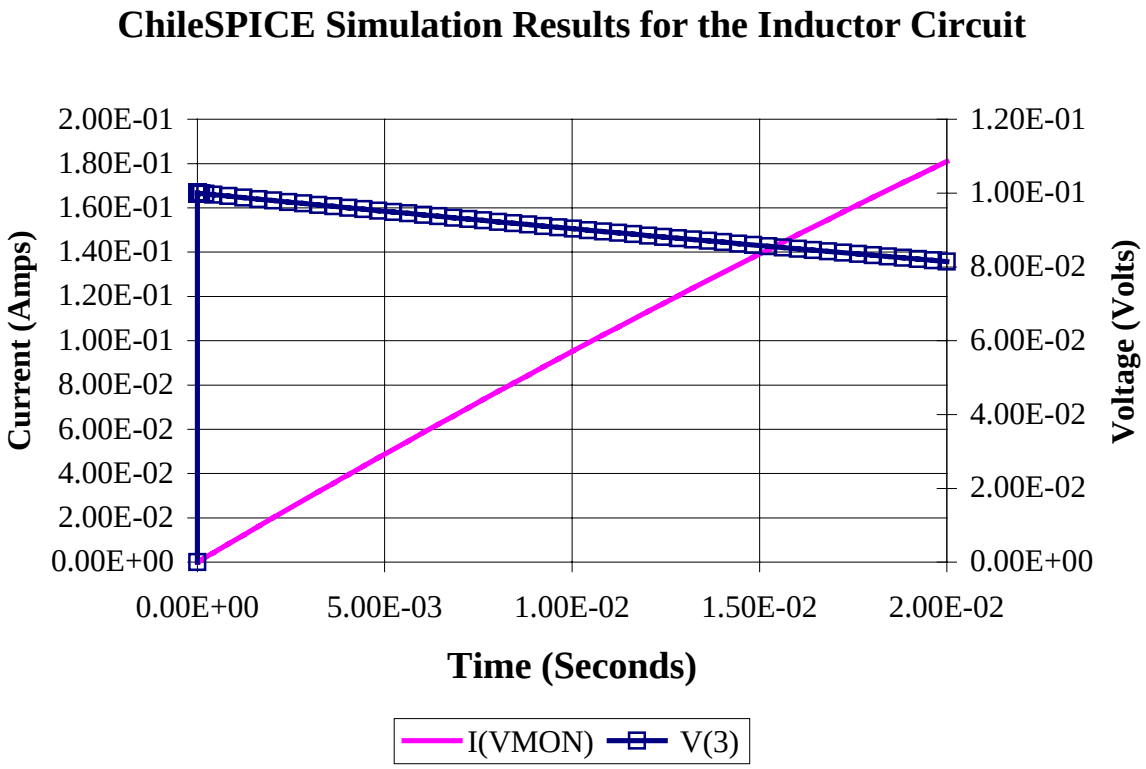
****

* Tier No.: 1
* Directory/Circuit Name: INDUCTOR/INDUCTOR.cir
* Description: Circuit netlist to test validity of the inductor model.
* Input: B1=I
* Output: I(VMON), V(3)
* Analysis:
* A small resistor and a zero volt source, VMON, is placed in series with the inductor.
* However, the inductor is essentially in parallel with the input current source, IS. The
* input current, defined by a nonlinear dependent source, B1, is:
* $B1 = I = 10*t*e^{-5t}$ for t>0
* The voltage generated by the inductor is given by:
* $V(3) = L*dI/dt = L * d(10*t*e^{-5t})/dt = 10 * L * e^{-5t} * (1 - 5t)$
* where L = inductor value = 10mH
* The table below shows calculated values of the inductor's current and voltage, I and
* V(3), for given values time:

Time (Seconds)	I (Amps)	V(3) (Volts)
0.001	0.009950125	0.099501248
0.002	0.019800997	0.098508719
0.003	0.029553358	0.097523615
0.004	0.039207947	0.096545887
0.005	0.048765496	0.095575487
0.006	0.058226732	0.094612364
0.007	0.067592379	0.093656471
0.008	0.076863155	0.09270776
0.009	0.086039773	0.091766182
0.01	0.095122942	0.090831691
0.011	0.104113366	0.089904238
0.012	0.113011744	0.088983778
0.013	0.12181877	0.088070262
0.014	0.130535135	0.087163645
0.015	0.139161523	0.086263882
0.016	0.147698615	0.085370925
0.017	0.156147088	0.084484729
0.018	0.164507613	0.08360525
0.019	0.172780858	0.082732442
0.02	0.180967484	0.081866261

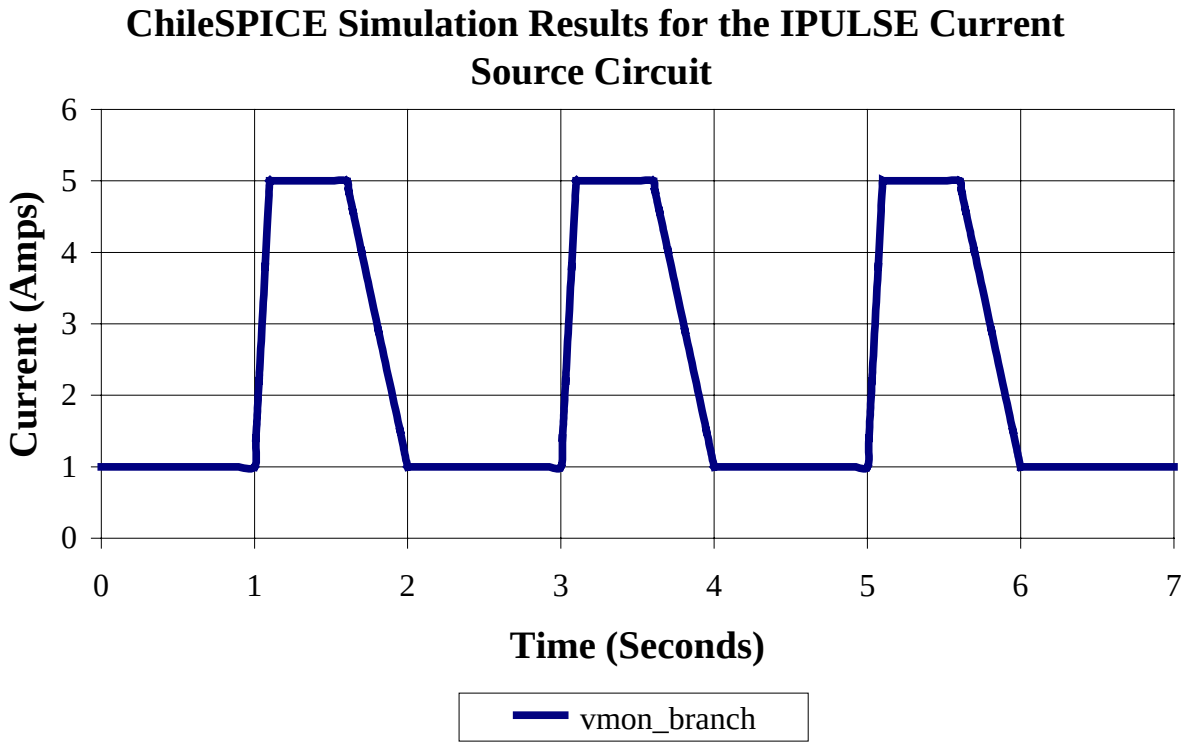
****

```
B1 0 1  I = (10 * TIME * EXP( - 5*TIME))
VMON 1 2 0
R1 2 3  0.000001
L1 3 0 10mH
.TRAN 0 20MS
.PRINT TRAN I(VMON) V(3)
.OPTION ACCT
.END
```


ChileSPICE Simulation Results for the Inductor Circuit
2.00E-01
1.80E-01
1.60E-01
1.40E-01
1.20E-01
1.00E-01
8.00E-02
6.00E-02
4.00E-02
2.00E-02
0.00E+00
Current (Amps)
1.20E-01
1.00E-01
8.00E-02
6.00E-02
4.00E-02
2.00E-02
0.00E+00
Voltage (Volts)
0.00E+00
5.00E-03
1.00E-02
1.50E-02
2.00E-02
Time (Seconds)
I(VMON)
V(3)

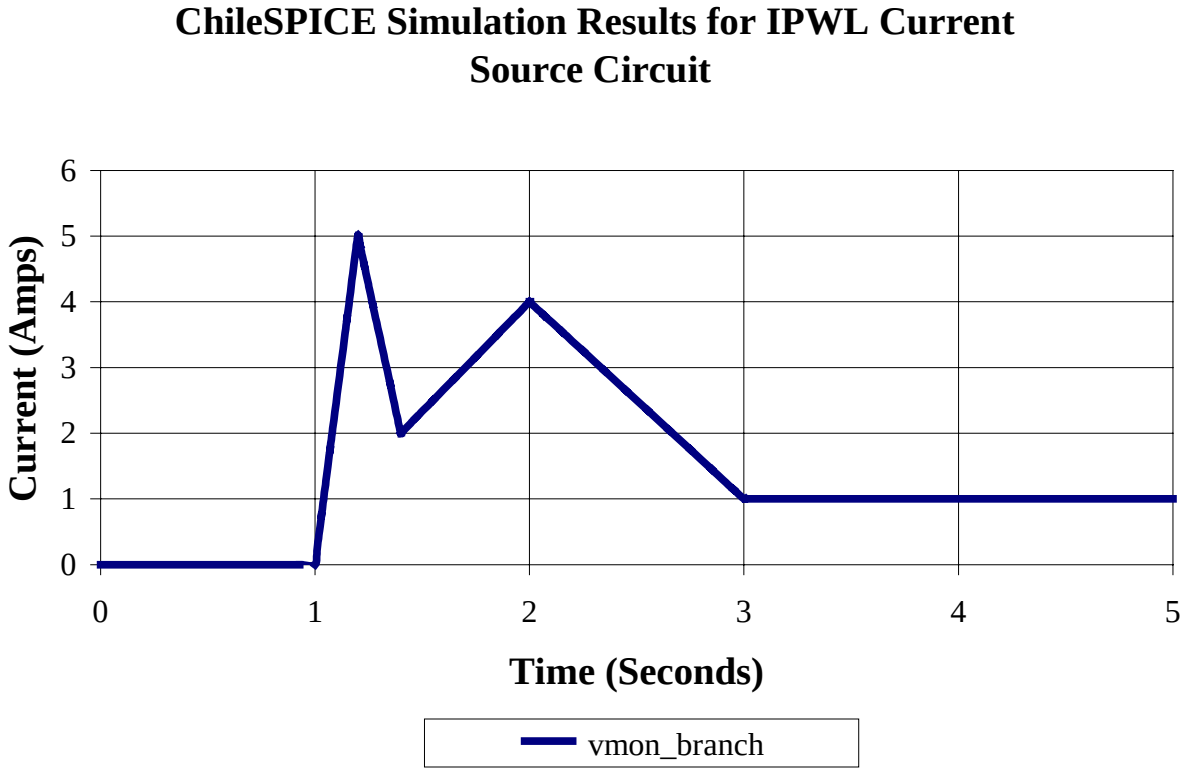
3.1.17 Test Circuit for the Pulse Current Source

```
********************************************************************************
* Tier No.: 1
* Directory/Circuit Name:  IPULSE/IPULSE.cir
* Description: Test of the model for an independent current source.
* Input: IPULSE
* Output: I(VMON)
* Analysis:
*       The current source is described as a pulse signal that starts at 1A and stays there for 1
*       second.  Then the current increases linearly from 1A to 5A during the next 0.1s and stays
*       at 5A for 0.5s.  It then decreases linearly from 5A to 1A in 0.4s.  It stays at 1A for 1s.
*       The cycle is repeated (except for the initial delay) two more times between 3s and 7s.
*       A zero volt source, VMON, is used as an ammeter to measure the current from the
*       IPULSE source.   A resistor is used to provide a closed loop for current flow.
********************************************************************************
IPULSE 0 1 PULSE(1A 5A 1S 0.1S 0.4S 0.5S 2S)
R 2 0 500
VMON 1 2 0
.TRAN 1S 7S
.OPTIONS ACCT
.PRINT TRAN I(VMON)
.END
```



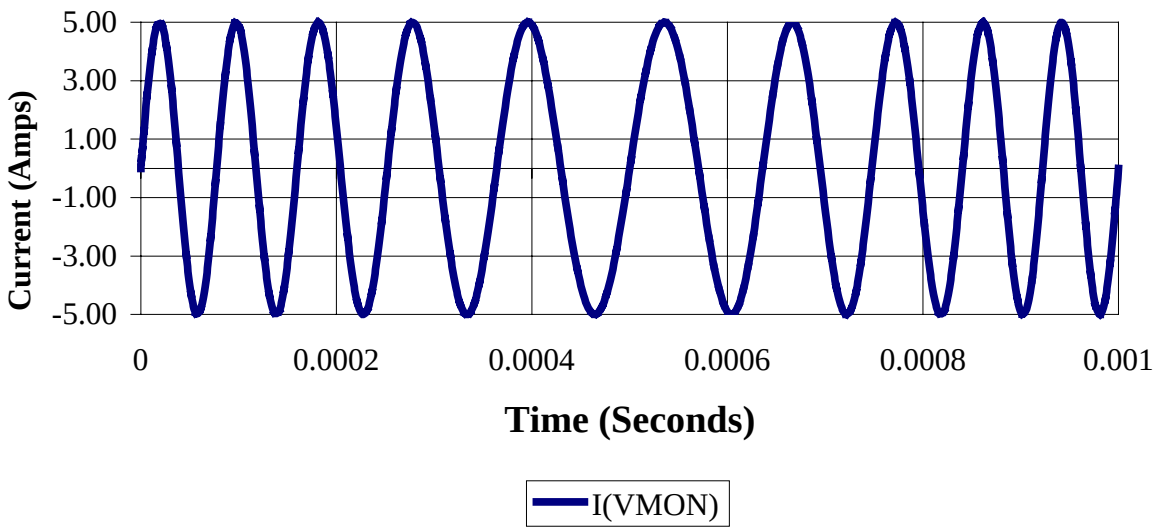
3.1.18 Test Circuit for the Piece Wise Linear Current Source

```
**********************************************************************************
* Tier No.: 1
* Directory/Circuit Name: IPWL/IPWL.cir
* Description: Test of model for an independent pulse current source.
* Input: IPWL
* Output: I(VMON)
* Analysis:
*       A piece-wise linear current source, IPWL, which is a series  of time and current pairs of
*       data points given by:
*
*              Index     Time(s), Current(amps)
*                1        (0.0 , 0.0)
*                2        (1.0, 0.0)
*                3        (1.2 , 5.0)
*                4        (1.4 , 2.0)
*                5        (2.0 , 4.0)
*                6        (3.0 , 1.0)
*
*
*       A zero volt source, VMON, is used as an ammeter to measure the current from the IPWL
*       source.   A resistor is used to provide a closed loop for current flow.
**********************************************************************************
IPWL 0 1 PWL(0 0A  1S 0A  1.2S 5A  1.4S 2A  2S 4A  3S 1A)
R 2 0 500
VMON 1 2 0
.TRAN 1S 5S
.OPTIONS ACCT
.PRINT TRAN I(VMON)
.END
```


ChileSPICE Simulation Results for IPWL Current Source Circuit
Current (Amps)
0
1
2
3
4
5
6
Time (Seconds)
0
1
2
3
4
5
vmon_branch

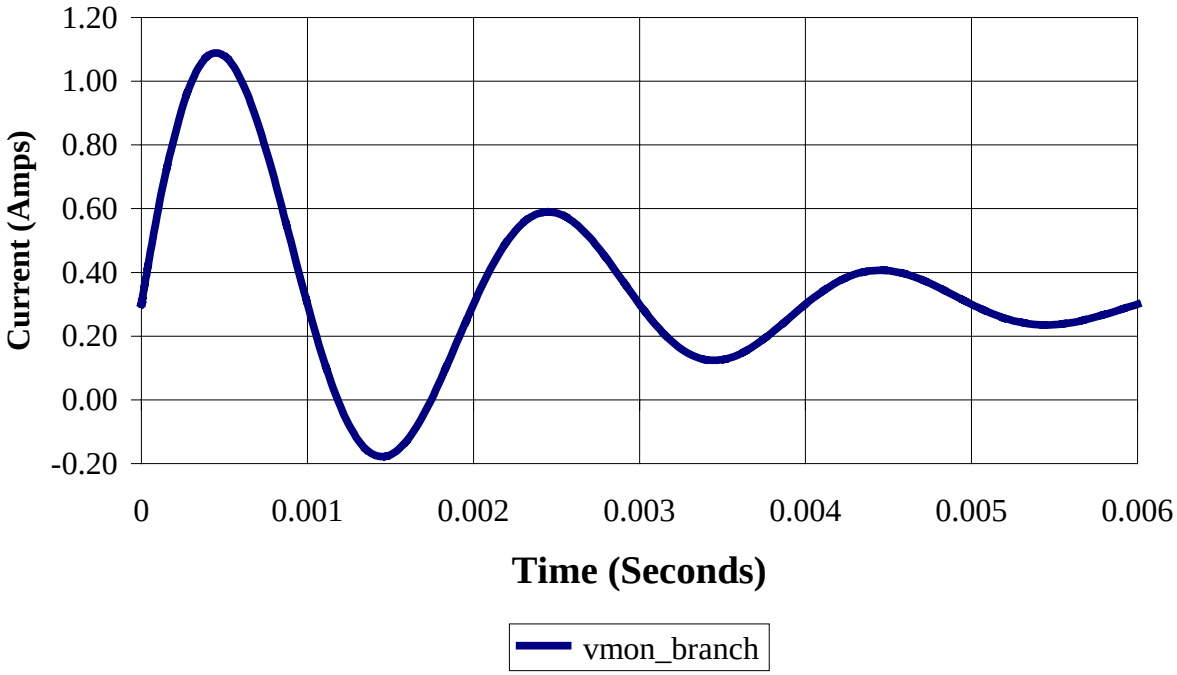
3.1.19 Test Circuit for the Single Frequency FM Source (ISFFM) Current Source

```
**********************************************************************************
* Tier No.: 1
* Directory/Circuit Name:  ISFFM/isffm.cir
* Description: Test of the model for single-frequency  frequency modulated (SFFM) transient
*       independent current source.
* Input:  ISFFM
* Output:  I(VMON)
* Analysis:
*       A single frequency frequency-modulation signal that has no initial current and a
*       peak amplitude of 5A.  It has a carrier frequency of 10KHz.  For the 1ms transient
*       analysis,  10 cycles of the carrier will be output in the 1ms time.  The carrier is
*       modulated at a rate determined by the single frequency (1KHz) and the
*       modulation index (3).
*       The general format for a sffm transient function on a source statement is
*               SFFM (IO  IA  FC  MDI  FS)
*       where,
*               IO=offset current = 0A                  IA=amplitude = 5A
*                FC=carrier frequency = 10kHz          MDI=modulation index = 3
*               FS=signal frequency = 1kHz
*       The current is described by the following equation:
*               ISFFM(t)= IO + IA*sin(2*pi*FC*t + MDI*sin(2*pi*FS*t))
*       Therefore, at the given values of time,  the current should be:
*
*       T               ISFFM(T)
*       0.0000E+00      0.0000E+00
*       1.0000E-04      4.9076E+00
*       2.0000E-04      1.4222E+00
*       3.0000E-04      1.4222E+00
*       4.0000E-04      4.9076E+00
*       5.0000E-04      2.1244E-06
*       6.0000E-04      -4.9076E+00
*       7.0000E-04      -1.4222E+00
*       8.0000E-04      -1.4222E+00
*       9.0000E-04      -4.9076E+00
*
*       A zero volt source, VMON, is used as an ammeter to measure the current from the
*       ISFFM source.   A resistor is used to provide a closed loop for current flow.
**********************************************************************************
ISFFM 0 1 SFFM(0 5 10KHZ 3 1KHZ)
R1 2 0 1
VMON 1 2 0
.TRAN 5US 1MS 0 5US
.PRINT TRAN I(VMON)
.OPTIONS ACCT
.END
```


ChileSPICE Simulation Results for the ISFFM Circuit
5.00
3.00
1.00
-1.00
-3.00
-5.00
Current (Amps)
0
0.0002
0.0004
0.0006
0.0008
0.001
Time (Seconds)
I(VMON)

3.1.20 Test Circuit for the Sinusoidal Current Source

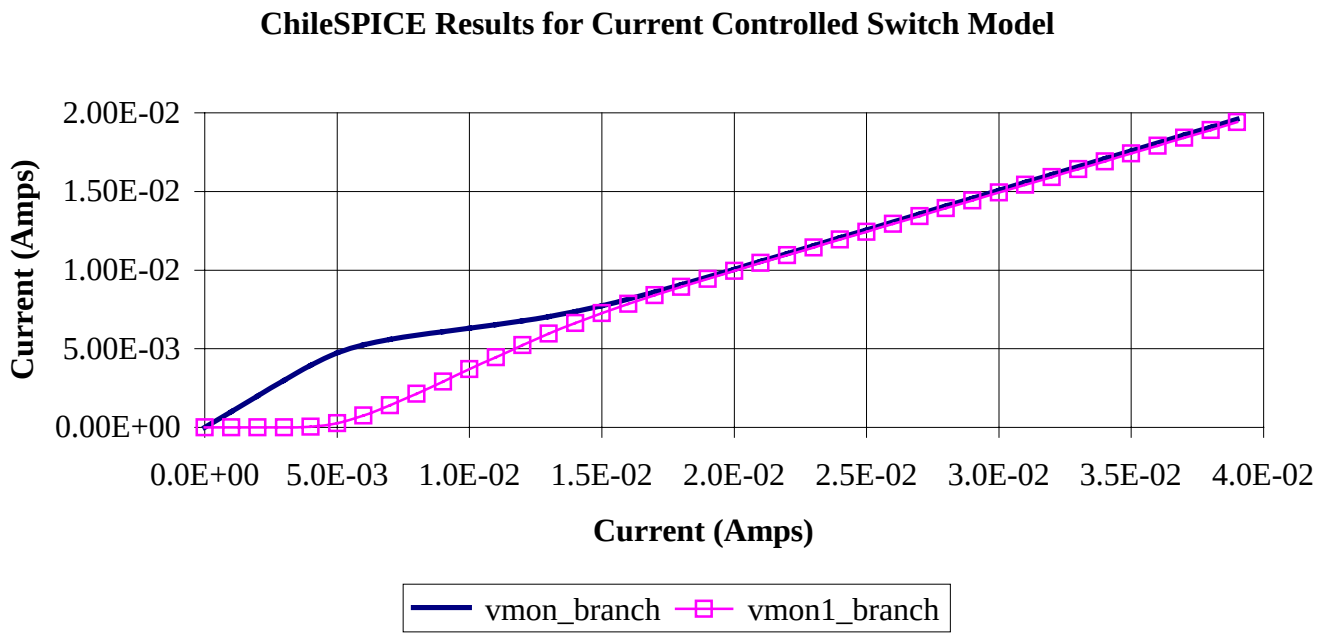
```
********************************************************************************
* Tier No.: 1
* Directory/Circuit Name: ISIN/isin.cir
* Description: Test of model for a sinusoidal  current source.
* Input: ISIN
* Output: I(VMON)
* Analysis:
*       A time dependent current source that supplies a sinusoidal signal of 0.3A initial
*       current, 1A amplitude and      a 500Hz frequency with no initial time delay.  The transient
*       analysis of 6ms will give 3 cycles of a damped sine wave. The damping factor is 500.
*
*       The general format for the sinusoidal function in the current source is
*               SIN(IO IA FREQ TD THETA)
*       where,
*               IO=offset current = 0.3A                IA=amplitude = 1A
*               FREQ=frequency = 500Hz     TD=time delay= 0
*               THETA=damping factor = 500
*       The current is described by the following equation for time > TD:
*               ISIN(t)= IO + IA*sin(2*pi*FREQ*(t –TD))*exp(-THETA(t-TD)
*       Therefore, at given values of time, the current should be:
*
*               T               ISIN(T)
*               0               0.3
*               0.0005          1.078800783
*               0.001           0.299999972
*               0.0015          -0.172366553
*               0.002           0.300000034
*               0.0025          0.586504797
*               0.003           0.299999969
*               0.0035          0.126226057
*               0.004           0.300000025
*               0.0045          0.405399225
*               0.005           0.299999981
*               0.0055          0.236072139
*               0.006           0.300000014
*
*       A zero volt source, VMON, is used as an ammeter to measure the current from the ISIN
*       source.   A resistor is used to provide a closed loop for current flow.
********************************************************************************
ISIN 0 1 SIN(0.3A 1A 500HZ 0 500)
R 2 0 1
VMON 1 2 0
.TRAN 0.06MS 6MS
.PRINT TRAN I(VMON)
.OPTIONS ACCT
.END
```


ChileSPICE Simulation Results for the ISIN Circuit
Current (Amps)
1.20
1.00
0.80
0.60
0.40
0.20
0.00
-0.20
0
0.001
0.002
0.003
0.004
0.005
0.006
Time (Seconds)
vmon_branch

3.1.21 Test Circuit for the Current-Controlled Switch

```
**********************************************************************************
* Tier No.: 1
* Directory/Circuit Name: ISWITCH/iswitch.cir
* Description: Test of the model for a current controlled switch. The switch behaves
*       like a resistor that toggles between a very small off resistance, and a very large
*       on resistance which depends upon the controlling current.
* Input: IS
* Output: I(VMON), I(VMON1) Current through R1 and R2 (measured with 2 zero volt
*       ammeters)
* Analysis:
*       A DC current source, IS, is stepped from 0 to 2mA. The current in the switch, W,  is
*       controlled by the current through R1 (measured through VMON), supplied by the DC
*       input source IS.  The switch is initially open, thereby allowing no current to flow due to a
*       large off resistance, ROFF=1E6 Ohms, of the switch.  When the current through R1
*       reaches ION=10ma, the switch nears transition to the on state, and the switch resistance
*       value is RON=1 Ohm.  The current through R1 and R2 increase linearly from 15 to
*       40mA because the current is now split equally between the two 100 Ohm resistors.
*       The controlling current and the switch current are  defined by the following equations:
*               Iswitch = I(VMON1) = IS  - I(VMON1)
*               I(VMON) = IS * (R2 + Rs  / (R1 + Rs +R2)) =
*       where,
*               I(VMON1) = switch current measure through a zero value voltage source,
*               VMON1
*               I(VMON) = controlling current measured through a zero value voltage source,
*               VMON
*               Rs = switch resistance
*       The switch resistance is defined by the following equations:
*       With  ION > IOFF :
*               For Ic<= ION
*                       Rs=ROFF
*               For : IOFF < Ic < ION
*                       Rs=exp(Lm + 3*Lr*(Ic-Im)/(2*Id) – 2*Lr*(Ic-Im)^3 / (Id)^3)
*               For Ic>=ION
*                       Rs=RON
*               Where,
*                       Ic      = controlling current = I(VMON)
*                       IOFF    = control current for the “off” state = 0 ma
*                       ION     = control current for the “on” state = 10ma
*                       ROFF    = “Off” resistance = 1 MOhm
*                       RON     = “On” resistance = 1 Ohm
*                       Lm      =ln(SQRT(RON*ROFF)) = 6.908
*                       Lr      =ln(RON/ROFF) = -13.816
*                       Im      =(ION+IOFF)/2 = .005
*                       Id      = (ION-IOFF)= 0.01
*
*       The table below is a hand calculation of the switch resistance and the current,
```

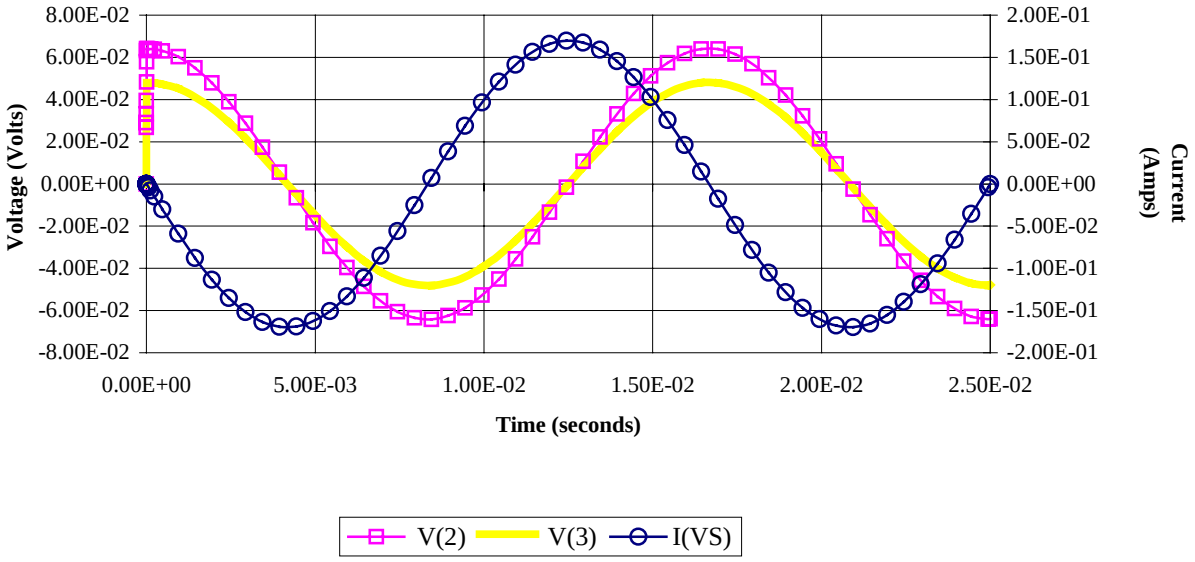
```
*       I(VMON1), through the switch as a function of the controlling current.
*
*       IS              I(VMON)         Rs              I(VMON1)
*       0.00E+00        0.00000         1000000.00      0.00000
*       5.00E-03        0.00458         1000.24         0.00042
*       1.00E-02        0.00502         1.00            0.00498
*       1.50E-02        0.00754         1.00            0.00746
*       2.00E-02        0.01005         1.00            0.00995
*       2.50E-02        0.01256         1.00            0.01244
*       3.00E-02        0.01507         1.00            0.01493
*       3.50E-02        0.01759         1.00            0.01741
*       4.00E-02        0.02010         1.00            0.01990
********************************************************************************
IS 0 1 DC 40mA
VMON 1 1A 0V
R1 1A 0 100
VMON1 2 3 0
R2 3 0 100
W 1 2 VMON W1 OFF
.MODEL W1 ISWITCH (ION=10mA IOFF=0mA RON=1 ROFF=1E6)
.DC IS 0 40mA 1mA
.PRINT DC I(VMON) I(VMON1)
.OPTIONS ACCT
.END
```



3.1.22 Test Circuit for Mutually Coupled Inductors

```
**********************************************************************************
* Tier No.: 1
* Directory/Circuit Name:  MINDUCTORS/MINDUCTORS.cir
* Description: Test of  mutually coupled inductors using coupling coefficent value of k=0.75
* Input: VS = V(1)
* Output: I(VS), V(2), V(3)
* Analysis:
*       The circuit contains two coupled inductors, L1=1mH and L2=1mH, that form a
*       transformer.   The primary side of the transformer is connected to resistor R1 and the
*       secondary is connected to resistor R2. The input signal, VS=V(1),  is a 60Hz sinusoidal
*       waveform with a peak  voltage amplitude of 169.7 V.  The rms value and radian
*       frequency of the input signal are calculated as follows:
*
*       V(1)rms = 0.707 * 169.7 = 119.98 V
*       w = 2*pi*frequency = 2 * 3.14159 * 60 Hz = 376.99 rads/s
*
*       A voltage is induced across L2 from the current in L1. Using a coupling coefficent of
*       k=0.75, the following calculations yield the current through the primary L1, I(VS), and
*       the voltage across the primary and secondary inductors, V(2) and V(3), respectively:
*
*       I1 = I(VS) = VS /  SQRT (R1**2 + XL1**2)
*       where,
*       XL1 = inductive reactance of L1 = 2*pi*frequency*L1= 376.99 * 1mH = 0.377 Ohms
*       Therefore,
*       I1 = 119.98 / SQRT (1000**2 + 0.377**2) =          0.1199 A rms
*          = 0.1199/0.707 =                                169.6 A peak
*       V(2) = I * XL1 = 0.1199 * 0.377 =                  0.0452 V rms
*            =  0.0452/0.707=                              63.9 V peak
*       V(3) = k * V(2) = 0.75 * 0.0452 =                  0.0339 V rms
*            = 0.0339 * 0.707=                             47.9 V rms
**********************************************************************************
VS 1 0 SIN(0 169.7 60HZ)
R1 1 2 1K
R2 3 0 1K
L1 2 0  1mH
L2 3 0   1mH
K1 L1 L2 0.75
.TRAN 100US 25MS
.PRINT TRAN I(VS) V(2) V(3)
.OPTION ACCT
.END
```

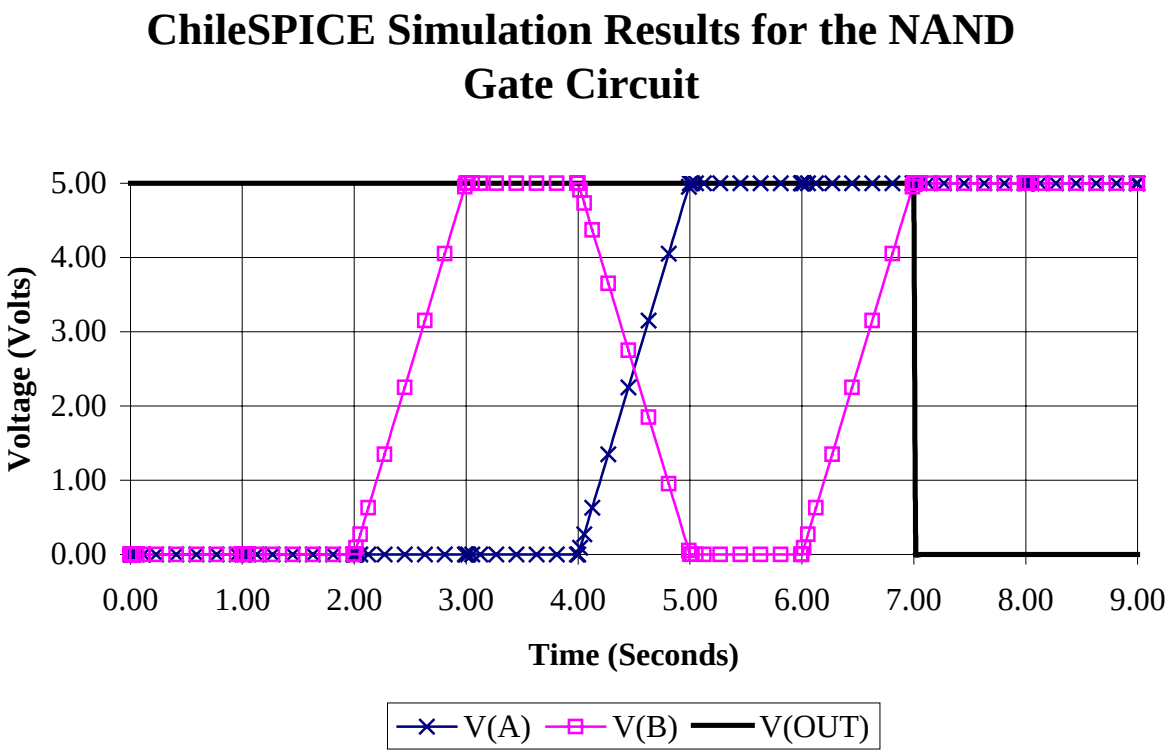
ChileSPICE Simulation Results for MINDUCTORS Circuit



3.1.23 Test Circuit for the NAND Gate

```
**********************************************************************************
* Tier No.:      1
* Directory/Circuit Name: NAND/nand.cir
* Description:  Test of the digital NAND gate used for defining logic circuits.
* Input: VA=V(A), VB=V(B)
* Output: V(A), V(B), V(OUT)
* Analysis:
*       Two piecewise linear voltage sources, V(A) and V(B),  are used as logic inputs to an
*       NAND gate, which is defined internal to the code by a subcircuit.  Parameters are defined
*       in the netlist (by the .PARAMS statement) and passed into the NAND subcircuit.  The
*       subcircuit uses the parameters to establish the following values of the output voltage:
*       Rise Time = default_rise= rise/fall output voltage = 1ns
*       Margin = default_margin = margin by which the output exceeds min/max logic levels
*              = 0.5V
*       High = default_high + default_margin = logic high voltage = 4.5V + 0.5V  = 5V
*       Low = default_low - default_margin = logic low voltage = 0.5V - 0.5V = 0V
*
*       The logic for the NAND gate is the output is low if and only if both inputs are high, and
*       for all other combination the output is high.
*       This truth table shows the NAND expected output for the given A and B time dependent
*       inputs.
*
*       TIME          A(Volts)      B(Volts)      OUT(Volts)
*       0S            0             0             5
*       1S            0             0             5
*       2S            0             0             5
*       3S            0             5             5
*       4S            0             5             5
*       5S            5             0             5
*       6S            5             0             5
*       7S            5             5             0
*       8S            5             5             0
*       9S            5             5             0
*       NOTE: Low = 0V  High=5V
**********************************************************************************
* Set digital default parameters
.PARAM default_rise=1ns
.PARAM default_delay=0
.PARAM default_low=0.5V
.PARAM default_high=4.5V
.PARAM default_margin=0.5V
* Gate Inputs
VA A 0 0V PWL(0 0  1 0  2 0  3 0  4 0  5 5  6 5  7 5  8 5)
VB B 0 0V PWL(0 0  1 0  2 0  3 5  4 5  5 0  6 0  7 5  8 5)
*
X_NAND A B OUT NAND
```

```
.TRAN 1S 9S
.PRINT TRAN V(A) V(B) V(OUT)
.OPTIONS ACCT
.END
```



3.1.24 Test Circuit for the N-Channel JFET

```
**********************************************************************************
* Tier No.: 1
* Directory/Circuit Name:  NJFET/NJFET.cir
* Description:   Circuit netlist to test current-voltage characteristics of the n-channel JFET
*                model.
* Input:   VDD
* Output: I(VMON), V(3,2) , V(2)
* Analysis:
* For the self-biased NJFET circuit the general algebraic solution for the bias point is:
* ID  =  {[-B – SQRT(B**2 – 4*A*C)] / 2*A}
* Where,
* A = RS**2  =  (600)**2 = 3.6E+5
* B = -{2*|VP|*RS + (VP**2) / IDSS} =  -{2 * 4 * 600 + 16/10.0E-3} = -6.4E+3
* C = VP**2 = (-4)**2 = 16
* Therefore,
* ID = {[-(-6.4E+3) – SQRT((-6.4E+3)**2  –  4 * 3.6E+5 * 16 )] / 2 * 3.6E+5} = 3.009 mA
* VGS = ID*RS = 3.009E-3 * 600 = 1.806 V
* |VDS| = |VDD| – ID*(RD + RS) = 15 – 3.009E-3 * (1.5k + 600) = 8.7V
* Note:
*        IDSS = BETA * VP**2 = 6.25E-4 * (-4)**2 = 10.0E-3 A
*        VP = VTO = -4V
*
*        The circuit simulation should yield the following outputs:
*        I(VMON) = Drain Current                  Id = 3mA
*        V(3,2) = Drain-Source Voltage            Vds= 8.7V
*        V(0,2) =Gate-Source  Voltage             Vgs= 1.8V
**********************************************************************************
VDD 4 0 DC 15V
VMON 5 3 0
RD 4 5 1.5K
RS 2 0 600
J 3 0 2 NJFET
.MODEL NJFET NJF BETA=6.25E-4 VTO=-4V
.DC VDD 15 15 1
.PRINT DC I(VMON) V(3,2) V(2,0)
.OPTIONS ACCT
.END
```

ChileSPICE Simulation Results for the NJFET Circuit:

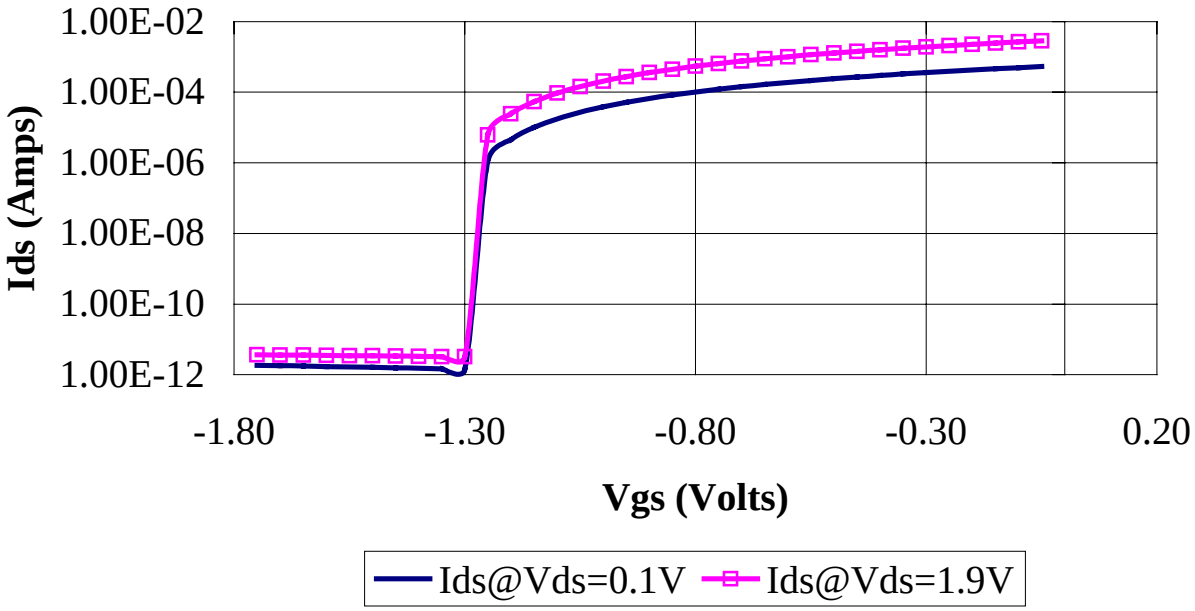
N-Channel JFET Circuit
DC transfer characteristic

Index	voltage_sweep VDD	vmon_branch ID	v(3)-v(2) VDS	v(2) VGS
0	1.500000E+01	3.009442E-03	8.680173E+00	1.805665E+00

3.1.25 Test Circuit for the N-Channel MESFET

```
**********************************************************************************
* Tier No.:  1
* Directory/Circuit Name:
* Description: Test of a simple n channel MESFET circuit to examine the subthreshold
*       characteristics of the device.  Ideally, the drain current of a FET device should
*       should reduce to zero when the device is biased below threshold.  However, a
*       residual subthreshold current exists in this regime.  This circuit shows the turnoff
*       properties of the ideal MESFET model.
* Input: Vgs and Vds
* Output: Ids
* Analysis:
*       This is a 1um NMESFET.  The nominal threshold voltage is –1.3V.  A DC transfer
*       function analysis is described with Vgs swept from –1.75V to 0V in 50mV steps
*       and Vds is stepped from 0.1V to 1.9V in 1.8V steps.
*       For the nonsaturation regime, where Vds <= 3/alpha
*       Id = (1+lambda*Vds)*{(beta*(Vgs-Vto)^2)/(1+B(Vgs-Vto))}*[1-(1-alpha*Vds/3)^3]
*       For the saturation regime, where Vds>3/alpha,
*       Id =  (1+lambda*VDS)*{(beta*(Vgs-Vto)^2)/(1+B(Vgs-Vto))}
*
*       alpha = 3,  beta=1.4E-3, lambda=0.03, Vto=-1.3, B=0.3 (default value)
*
*       for Vds = 0.1V, Vds  which is less than 3/alpha or 1V,
*               @Vgs=-1.5V  Id=-1.6E-12 A
*               @Vgs = -1V   Id=4.4E-8 A
*       for Vds = 1.9V, which is greater than 3/alpha or 1V,
*               @Vgs=-1.5V  Id=3.4E-12 A
*               @Vgs = 0.0V  Id=1.8E-3 A
*
*       The drain current, Id, is measured through the VIDS zero volt source that acts as an
*       ammeter.
**********************************************************************************
VDS 1 0 0
VIDS 1 2 0
VGS 3 0 0
Z1 2 3 0 MESMOD AREA=1.4
.MODEL MESMOD NMF
+ RD=46 RS=46 VTO=-1.3 LAMBDA=0.03 ALPHA=3 BETA=1.4E-3
.DC VGS -1.75V 0 50MV VDS 0.1V 1.9V 1.8V
.PRINT DC I(VIDS)
.OPTIONS ACCT
.END
```

ChileSPICE Simulation Results for the NMESFET Circuit



3.1.26 Test Circuit for the N-Channel MOSFET

```
**********************************************************************************
* Tier No.: 1
* Directory/Circuit Name:  NMOS/NMOS1.cir
* Description:   Circuit netlist to test current-voltage characteristics of the n-channel MOSFET
*                model.
* Input:  VDD
* Output: I(VMON) V(3,2) V(1,2)
* Analysis:
* FOR THE NMOS CIRCUIT BIASED IN THE ACTIVE MODE OF OPERATION :
* VG  =  {R2/(R1 + R2)} * VDD  =  {22E+6 / (69E+6)} * 18  = 5.74V
* ID  =  {[-B – SQRT(B**2 – 4*A*C)] / 2*A}
* Where,
* A = RS**2  =  (500)**2 = 2.5E+5
* B = -2*{(VG – VT) * RS + 1/KP} = -2 * {(5.74 – 2)*500 + 1/0.5E-3} = -7.74E+3
* C = ( VG – VT)**2 = (5.74 – 2)**2 = 13.9876
* Therefore,
* ID = {[-(-7.74E+3) – SQRT((-7.74E+3)**2 – 4 * 2.5E+5 * 2.5E+5 * 13.9876)] / 2 * 2.5E+5}
*     = 1.927mA
* VGS = VG – VS = VG – ID*RS = 5.74 – 1.927E-3 * 500 = 4.78V
* VDS = VDD – ID*(RD + RS) = 18 – 1.927E-3 * 2.7E+3 = 12.8V
*  The circuit simulation should yield the following outputs:
*                I(VMON) = Drain Current          Id=1.927mA
*                V(3,2) = Drain-Source Voltage    Vds=12.8V
*                V(1,2) = Gate-Source Voltage     Vgs=4.776V
**********************************************************************************
VDD 5 0 DC 18V
R1 5 1 47MEG
R2 1 0 22MEG
RD 5 4 2.2K
RS 2 0 500
VMON 4 3 0
M1 3 1 2 2 NFET
.MODEL NFET NMOS (KP=0.5M VTO=2V)
.DC VDD 18 18 1
.PRINT DC I(VMON) V(3,2) V(1,2)
.OPTION ACCT
.END
```

ChileSPICE Simulation Results for the NMOS Circuit:

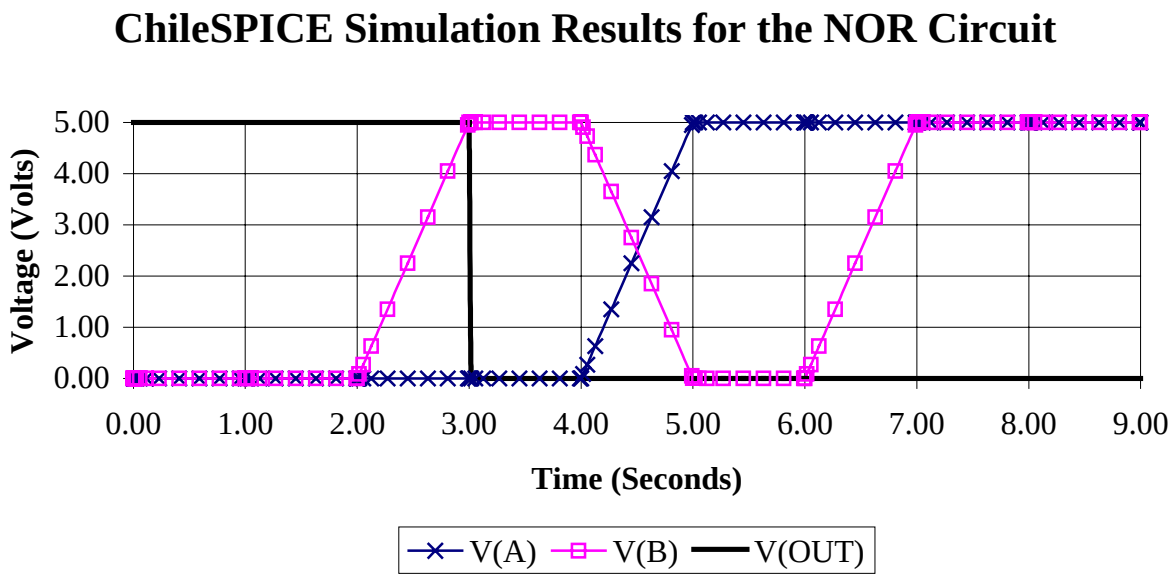
N-Channel MOSFET Circuit
DC transfer characteristic

Index	voltage_sweep	vmon_branch	v(3)-v(2)	v(1)-v(2)
0	1.800000E+01	1.926428E-03	1.279864E+01	4.775916E+00

3.1.27 Test Circuit for the NOR Gate

```
**********************************************************************************
* Tier No.:      1
* Directory/Circuit Name: NOR/nor.cir
* Description:  Test of the digital NOR gate used for defining logic circuits.
* Input: VA=V(A), VB=V(B)
* Output: V(A), V(B), V(OUT)
* Analysis:
*       Two piecewise linear  voltage sources, V(A) and V(B),  are used as logic inputs to a
*       NOR gate, which is defined internal to the code as a subcircuit.  Parameters are defined
*       in the netlist (by the .PARAMS statement) and passed into the NOR subcircuit.  The
*       subcircuit uses the parameters to establish the following values of the output voltage:
*       Rise Time = default_rise= rise/fall output voltage = 1ns
*       Margin = default_margin = margin by which the output exceeds min/max logic levels
*       = 0.5V
*       High = default_high + default_margin = logic high voltage = 4.5V + 0.5V  = 5V
*       Low = default_low - default_margin = logic low voltage = 0.5V - 0.5V = 0V
*
*       The logic for the NOR gate is the output is high if and only if both inputs are low; for any
*       other combination the output is low.
*       This truth table shows the NOR expected output for the given A and B time dependent
*       inputs.
*
*
*       TIME            A(Volts)        B(Volts)        OUT(Volts)
*       0S              0               0               5
*       1S              0               0               5
*       2S              0               0               5
*       3S              0               5               0
*       4S              0               5               0
*       5S              5               0               0
*       6S              5               0               0
*       7S              5               5               0
*       8S              5               5               0
*       9S              5               5               0
*       NOTE: Low = 0V  High=5V
**********************************************************************************
* Set digital default parameters
.PARAM default_rise=1ns
.PARAM default_delay=0
.PARAM default_low=0.5V
.PARAM default_high=4.5V
.PARAM default_margin=0.5V
* Gate Inputs
VA A 0 0V PWL(0 0  1 0  2 0  3 0  4 0  5 5  6 5  7 5  8 5)
VB B 0 0V PWL(0 0  1 0  2 0  3 5  4 5  5 0  6 0  7 5  8 5)
*
```

```
X_NOR A B OUT NOR
.TRAN 1S 9S
.PRINT TRAN V(A) V(B) V(OUT)
.OPTIONS ACCT
.END
```



3.1.28 Test Circuit for the NPN Bipolar Transistor

```
**********************************************************************************
* Tier No.: 1
* Directory/Circuit Name: NPN/NPN1.cir
* Description:  Circuit netlist to determine the current-voltage characteristics of the npn bipolar
*               transistor model. The circuit is configured as a common-emitter configuration.
* Input:  VCC
* Output: I(VMON1), I(VMON2), V(2)
* Analysis:
* FOR THE NPN CIRCUIT, DETERMINE:
* IB = {VCC – VBE} / RB = {12 – 0.7} / 377E+3 = 29.9uA
* IC = BETA * IB = 100 * 29.9E-6 = 2.99mA
* VCE = VCC – IC*RC = 12 – (2.99E-3)*(2E+3) = 6.01V
* The circuit simulation should yield the following outputs:
*       I(VMON1) = Base Current          Ib = 29.7uA
*       I(VMON2) = Collector Current     Ic = 2.97mA
*       V(2) = Emitter Collector Voltage Vce = 6.06V
**********************************************************************************
VCC  4 0 DC 12V
RC 3 4 2K
RB 4 5 377K
* ZERO VOLT SOURCES USED AS AMMETERS TO MEASURE THE
* BASE AND COLLECTOR CURRENTS, RESPECTIVELY
VMON1 5 1 0
VMON2 3 2 0
Q 2 1 0 NBJT
.MODEL NBJT NPN (BF=100)
.DC VCC 12 12 1
.PRINT DC I(VMON1) I(VMON2) V(2)
.OPTION ACCT
.END
```

ChileSPICE Simulation Results for the NPN Circuit:

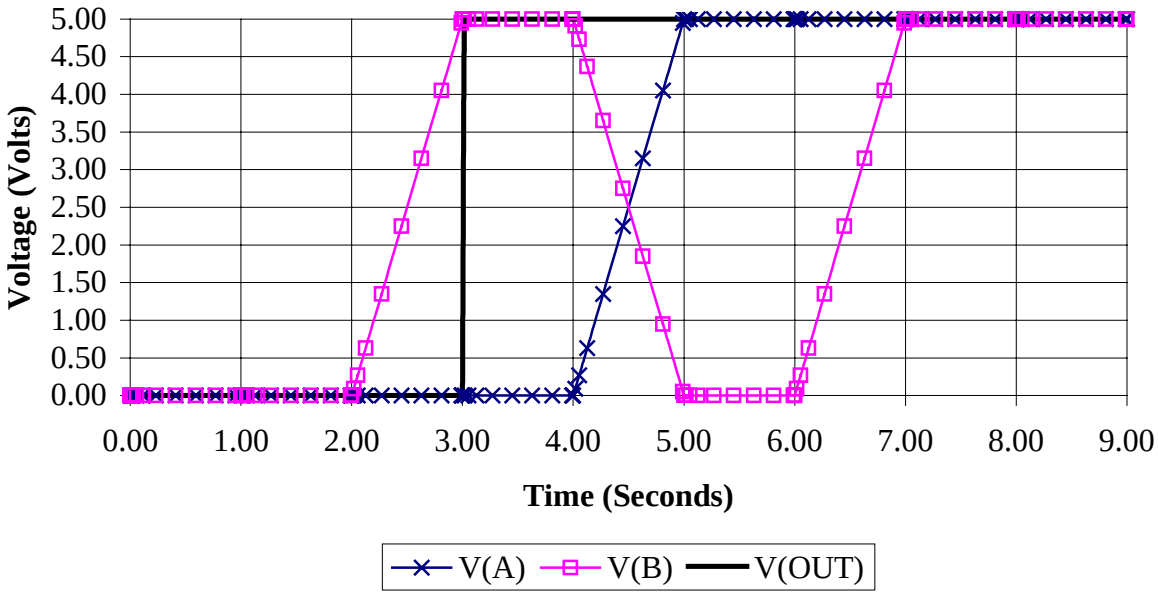
NPN Bipolar Transistor Circuit Netlist
DC transfer characteristic

Index	voltage_sweep	vmon1_branch	vmon2_branch	v(2)
	VCC	IB	IC	VCE
0	1.200000E+01	2.970195E-05	2.970196E-03	6.059609E+00

3.1.29 Test Circuit for the OR Gate

```
**********************************************************************************
* Tier No.:      1
* Directory/Circuit Name: OR/or.cir
* Description:  Test of the digital OR gate used for defining logic circuits.
* Input: VA=V(A), VB=V(B)
* Output: V(A), V(B), V(OUT)
* Analysis:
*       Two piecewise linear  voltage sources, V(A) and V(B),  are used as logic inputs to an
*       OR gate, which is defined internal to the code by a subcircuit.  Parameters are defined
*       in the netlist (by the .PARAMS statement) and passed into the OR subcircuit.  The
*       subcircuit uses the parameters to establish the following values of the output voltage:
*       Rise Time = default_rise= rise/fall output voltage = 1ns
*       Margin = default_margin = margin which the output exceeds min/max logic levels=0.5V
*       High = default_high + default_margin = logic high voltage = 4.5V + 0.5V  = 5V
*       Low = default_low - default_margin = logic low voltage = 0.5V - 0.5V = 0V
*       The logic for the OR gate is the output is high if and only if either one of the inputs is
*       high.  When both inputs are low, the output is low.
*       This truth table shows the OR expected output for the given A and B time dependent
*       inputs.
*       TIME          A(Volts)      B(Volts)      OUT(Volts)
*       0S            0             0             0
*       1S            0             0             0
*       2S            0             0             0
*       3S            0             5             5
*       4S            0             5             5
*       5S            5             0             5
*       6S            5             0             5
*       7S            5             5             5
*       8S            5             5             5
*       9S            5             5             5
*       NOTE: Low = 0V  High=5V
**********************************************************************************
* Set digital default parameters
.PARAM default_rise=1ns
.PARAM default_delay=0
.PARAM default_low=0.5V
.PARAM default_high=4.5V
.PARAM default_margin=0.5V
* Gate Inputs
VA A 0 0V PWL(0 0  1 0  2 0  3 0  4 0  5 5  6 5  7 5  8 5)
VB B 0 0V PWL(0 0  1 0  2 0  3 5  4 5  5 0  6 0  7 5  8 5)
X_OR A B OUT OR
.TRAN 1S 9S
.PRINT TRAN V(A) V(B) V(OUT)
.OPTIONS ACCT
.END
```

ChileSPICE Simulation Results for the OR Gate Circuit



3.1.30 Test Circuit for the P-Channel Depletion Mode JFET

```
*********************************************************************************
* Tier No.: 1
* Directory/Circuit Name:  PJFET/PJFET.cir
* Description:   Circuit netlist to test current-voltage characteristics of the p-channel JFET
*                model.
* Input:   VDD
* Output: I(VMON), V(3,2) , V(1,2)
* Analysis:
*For determining the bias point of the  PJFET circuit the general algebraic solution is:
* ID  =  {[-B – SQRT(B**2 – 4*A*C)] / 2*A}
* Where,
* A = RS**2  =  (1.65E3)**2 = 2.7225E+6
* B = -{2*(|VP| + |VG|)*RS + (VP**2) / IDSS} =  -{2 * (5 + 4) * 1.65E3 + 25/18.0E-3} =
*          -31.09E+3
* C = (|VP| + |VG|)**2 = (5 + 4)**2 = 81
* Therefore,
* ID = {[-(-31.09E+3) – SQRT((-31.09E+3)** 2 –  4 * 2.7225E+6 * 81)] / 2 * 2.7225E6} =
*         4.02mA
* |VDS| = |VDD| – ID*(RD + RS) = 20 – 4.02E-3 * (1.85k + 1.65k) = 5.93V
* Since the JFET is P-channel, VDS is –5.93V
*  VGS = |VG| - ID*RS
*         = | [R2 / (R2 + R1)] * VDD | - ID*RS
*         = [47E3/ (47E3 + 188E3)] * 20 – 4.02E-3*1.65E3
*         = 2.63V
* Note:
*         IDSS = BETA * VP**2 = 7.2E-4 * (-5)**2 = 18.0E-3 A
*         VP = VTO = -5V
*
*         The circuit simulation should yield    the following outputs:
*         I(VMON) = Drain Current                    Id = 4.02mA
*         V(3,2) = Drain-Source Voltage              Vds= -5.93V
*         V(1,2) =          Gate-Source Voltage      Vgs= 2.63V
*********************************************************************************
J  3 1 2 JFET
R1 5 1   188K
R2 1 0   47K
RS 2 0   1.65K
RD 5 4   1.85K
VDD  0 5 20V
VMON 3 4 0
.MODEL JFET PJF BETA=7.2E-4 VTO=-5
.DC VDD 20 20 1
.PRINT DC I(VMON) V(3,2) V(1,2)
.OPTION ACCT
.END
```

ChileSPICE Simulation Results for the PJFET Circuit:

P-Channel Depletion Mode JFET Circuit
DC transfer characteristic

Index	voltage_sweep VDD	vmon_branch ID	v(3)-v(2) VDS	v(1)-v(2) VGS
0	2.000000E+01	4.022105E-03	-5.922631E+00	2.636474E+00

3.1.31 Test Circuit for the P-Channel MOSFET

```
**********************************************************************************
* Tier No.:  1
* Directory/Circuit Name: PMOS/PMOS1.cir
* Description:   Circuit netlist to test current-voltage characteristics of the p-channel MOSFET
*                model.  The transistor is biased in nonsaturation region using resistors R1 and R2
*                to fix the gate voltage at half supply.
* Input:   VDD
* Output:  I(VMON), V(2,3) , V(2,1)
* Analysis:
* FOR THE PMOS CIRCUIT BIASED IN THE NON-SATURATION REGION:
* VSG = VDD - VG = VDD - {R2/(R1+R2)}*VDD = 5 - {50/100}*5 = 2.5V
* ID  = KP*[2*(VSG + VT)*VSD  +  VSD**2)]
*     = 0.2E-3 * {2*(2.5-0.8)*(5  –  7.5E+3 * ID) – (5 – 7.5E+3 * ID)**2}
*     = 0.515mA
* VSD = VDD – ID*RD = 5 – (0.515E-3)*(7.5E+3) = 1.14 V
* The circuit simulation should yield the following outputs:
*        I(VMON) = Drain Current          Id = 0.515mA
*        V(2,3) = Source-Drain Voltage    Vsd= 1.14V
*        V(2,1) = Source-Gate Voltage     Vsg= 2.5V
**********************************************************************************
VDD 2 0 DC 5V
R1 2 1 50K
R2 1 0 50K
RD 4 0 7.5K
VMON 3 4 0
M1 3 1 2 2 PFET L=10U W=160U
.MODEL PFET PMOS (KP=25U VTO=-0.8V)
.DC VDD 5 5 1
.PRINT DC I(VMON) V(2,3) V(2,1)
.OPTION ACCT
.END
```

ChileSPICE Simulation Results for the PMOS Circuit:

P-Channel MOSFET Circuit
DC transfer characteristic

Index	voltage_sweep VDD	vmon_branch ID	v(2)-v(3) VSD	v(2)-v(1) VSG
0	5.000000E+00	5.153525E-04	1.134856E+00	2.500000E+00

3.1.32 Test Circuit for the PNP Bipolar Transistor

```
**********************************************************************************
* Tier No.:  1
* Directory/Circuit Name: PNP/PNP1.cir
* Description:  Circuit netlist simulated in ChileSPICE to determine the validity of the
*               current-voltage characteristics of the PNP bipolar transistor model.  A common
*               collector configuration is biased in the forward active mode.
* Input:  VPOS, VBB
* Output: I(VMON1), I(VMON2), I(VMON3)
* Analysis:
* FOR THE PNP CIRCUIT DETERMINE:
* IE = {VCC – VEC}/RE = {5 – 2.5}/2E+3 = 1.25mA
* IC = {BETA/(1 + BETA)} * IE = 60/61 * 1.25E-3 = 1.23mA
* IB = IC/BETA = 1.23E-3/60 = 20.5uA
* RB = {VCC – VBB – VEB – IE*RE} / IB = {5 – (-2) –0.6 – (1.25E-3 * 2E3)} / 20.5E-6
*      = 190.2K
* The circuit simulation should yield the following outputs:
*               I(VMON1) = Base Current          Ib = 20.5uA
*               I(VMON2) = Collector Current     Ic = 1.23mA
*               I(VMON3) = Emitter Current       Ie = 1.25mA
**********************************************************************************
VCC  1 0 DC 5V
VBB   6 0 DC -2V
RE    1 2 2K
RB    3 4 190K
Q 5 3 7 PBJT
* ZERO VOLT SOURCES ACTING AS AN AMMETER TO MEASURE THE
* BASE, COLLECTOR, AND EMMITTER CURRENTS, RESPECTIVELY
VMON1 4 6 0
VMON2 5 0 0
VMON3 2 7 0
.DC VCC 5 5 1 VBB -2 -2 1
.PRINT DC I(VMON1) I(VMON2) I(VMON3)
.MODEL PBJT PNP (IS=100FA BF=60)
.OPTION ACCT
.END
```

ChileSPICE Simulation Results for the PNP Circuit:

PNP Bipolar Transistor Circuit
DC transfer characteristic

Index	voltage_sweep VCC	vmon1_branch IB	vmon2_branch IC	vmon3_branch IE
0	5.000000E+00	2.050980E-05	1.230588E-03	1.251098E-03

3.1.33 Test Circuit for the Polynomial Source

```
**********************************************************************
* Tier No.:     1
* Directory/Circuit Name:  POLY/poly.cir
* Description:  Test of polynomial function for describing a nonlinear dependent voltage source.
* Input:  VINPUT = V(1)
* Output: V(2), V(3), V(4)
* Analysis:
*        A voltage source, VINPUT, supplies two equal resistors, R1=R2=1k. The nonlinear
*        source, B,
*        is dependent upon the voltage at node 2, V(2), by a given polynomial:
*                B = V(3) = 3 + 2*V(2) + V(2)**2
*      V(2) is established by a voltage divider with Vinput.  Additionally, V(4) is established by a
*      voltage divider with V(3). The equations and expected output are as follows:
*
*                (1) V(2) = VINPUT * [R2/(R1+R2)]
*                (2) V(3) = 3 + 2*V(2) + V(2)**2
*                (3) V(4) = V(3) * [R4/(R3+R4)]
*
*        VINPUT, or V(1), is described on the DC line as varying from -4V to 4V in 1V steps.
*        Therefore, the following output, in volts, is expected:
*
*
*        VINPUT      V(2)        V(3)        V(4)
*        -4.0        -2.0        3.00        1.500
*        -3.0        -1.5        2.25        1.125
*        -2.0        -1.0        2.00        1.000
*        -1.0        -0.5        2.25        1.125
*         0.0         0.0        3.00        1.500
*         1.0         0.5        4.25        2.125
*         2.0         1.0        6.00        3.000
*         3.0         1.5        8.25        4.125
*         4.0         2.0        1.10        5.500
*
**********************************************************************
VINPUT 1 0 1V
B 3 0 V = POLY(1) V(2) 3 2 1
R1 1 2 1K
R2 2 0 1K
R3 3 4 2K
R4 4 0 2K
.DC VINPUT -4 4 1
.PRINT DC V(2) V(3) V(4)
.OPTIONS ACCT
.END
```

ChileSPICE Simulation Results for the Poly Circuit:

Polynomial Source Circuit
DC transfer characteristic

Index	voltage_sweep VINPUT	v(2)	v(3)	v(4)
0	-4.000000e+00	-2.000000e+00	3.000000e+00	1.500000e+00
1	-3.000000e+00	-1.500000e+00	2.250000e+00	1.125000e+00
2	-2.000000e+00	-1.000000e+00	2.000000e+00	1.000000e+00
3	-1.000000e+00	-5.000000e-01	2.250000e+00	1.125000e+00
4	0.000000e+00	0.000000e+00	3.000000e+00	1.500000e+00
5	1.000000e+00	5.000000e-01	4.250000e+00	2.125000e+00
6	2.000000e+00	1.000000e+00	6.000000e+00	3.000000e+00
7	3.000000e+00	1.500000e+00	8.250000e+00	4.125000e+00
8	4.000000e+00	2.000000e+00	1.100000e+01	5.500000e+00

3.1.34 Test Circuit for the Resistor

```
**********************************************************************************
*Tier No.: 1
* Directory/Circuit Name:RESISTOR/RESISTOR.cir
* Description:  Circuit to demonstrate the validity of the linear resistor model.
* Input: VIN=0-5V DC
* Output: V(1), I(V1)
* Analysis:
*       A DC voltage source, V1,  in parallel with a 1K Ohm resistor, is swept from 0-5V in
*       1V increments.  The measured output is the current, I(V1), through the resistor.  This is
*       calculated using Ohm's Law , which yields the linear I-V characteristic for a resistor.
*
*               Voltage=  Current * Resistance = I * R
*       or,
*               I=V/R
*
*       The netlist was simulated using a low (1E-9 Ohms), nominal (1E3 Ohms)
*       and high (1E12 Ohms)  values for the resistance.
*
*       Therefore, for the given resistance and voltage values, I is:
*                       V(Volts)        R(Ohms)             I(Amps)_____
*                       0               1E-9/1E3/1E12       0
*                       1               1E-9/1E3/1E12       1E9/1E-3/1E-12
*                       2               1E-9/1E3/1E12       2E9/2E-3/2E-12
*                       3               1E-9/1E3/1E12       3E9/3E-3/3E-12
*                       4               1E-9/1E3/1E12       4E9/4E-3/4E-12
*                       5               1E-9/1E3/1E12       5E9/5E-3/5E-12
**********************************************************************************
R1 1 0 1K
V1 1 0 5V
.DC V1 0 5V 1V
.PRINT DC V(1) I(V1)
.OPTION ACCT
.END
```

ChileSPICE Simulation Results for the Resistor Circuit:

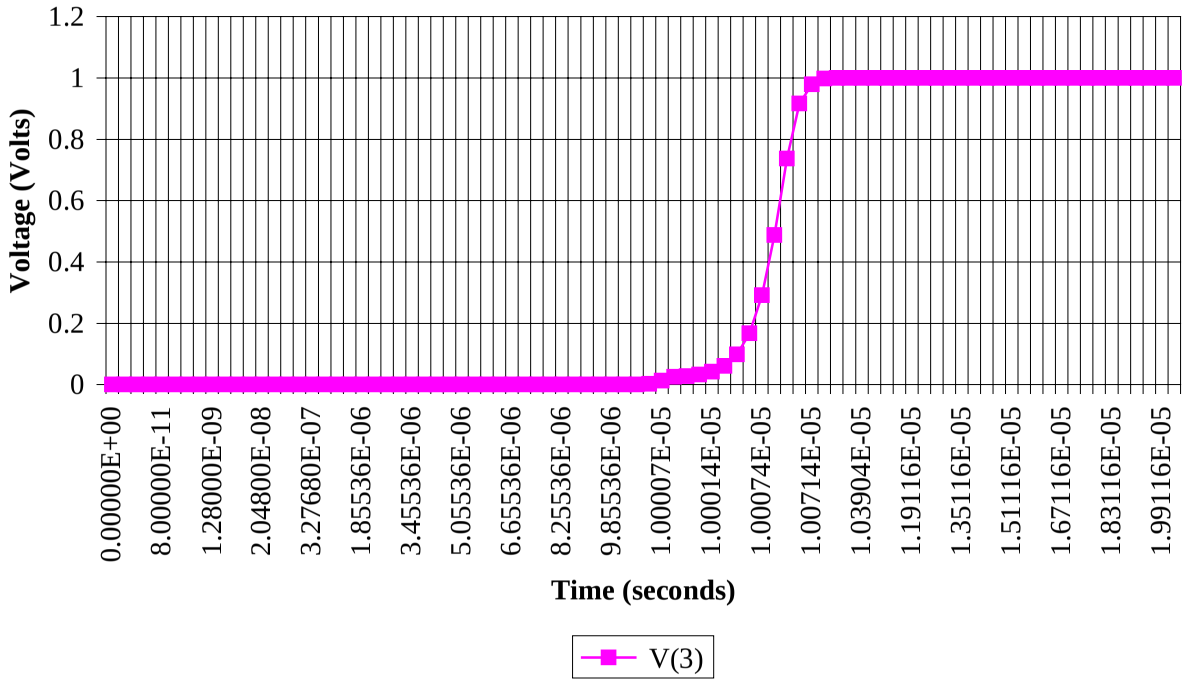
Resistor Circuit
DC transfer characteristic

Index	voltage_sweep V1	v(1)	v1_branch I(V1)=I(R1)
R = 1E-9 Ohms			
0	0.000000e+00	0.000000e+00	0.000000e+00
1	1.000000e+00	1.000000e+00	1.000000e+09
2	2.000000e+00	2.000000e+00	2.000000e+09
3	3.000000e+00	3.000000e+00	3.000000e+09
4	4.000000e+00	4.000000e+00	4.000000e+09
5	5.000000e+00	5.000000e+00	5.000000e+09
R = 1E3 Ohms			
0	0.000000E+00	0.000000E+00	0.000000E+00
1	1.000000E+00	1.000000E+00	1.000000E-03
2	2.000000E+00	2.000000E+00	2.000000E-03
3	3.000000E+00	3.000000E+00	3.000000E-03
4	4.000000E+00	4.000000E+00	4.000000E-03
5	5.000000E+00	5.000000E+00	5.000000E-03
R = 1E12 Ohms			
0	0.000000e+00	0.000000e+00	0.000000e+00
1	1.000000e+00	1.000000e+00	1.000000e-12
2	2.000000e+00	2.000000e+00	2.000000e-12
3	3.000000e+00	3.000000e+00	3.000000e-12
4	4.000000e+00	4.000000e+00	4.000000e-12
5	5.000000e+00	5.000000e+00	5.000000e-12

3.1.35 Test Circuit for the Semiconductor Capacitor

```
********************************************************************************
* Tier No.: 1
* Directory/Circuit Name: SEMIC_CAPACITOR/SEMIC_CAPACITOR.cir
* Description:  Test of semiconductor capacitor model using a simple RC circuit  configuration
* Input:  VIN
* Output: V(3)
* Analysis:
*       A 20 pF capacitor is specified by a length, width and junction capacitance.
*       A transient analysis of the circuit voltage versus time is performed to determine the
*       capacitor voltage, V(3) and current, I(VMON).    To obtain the capacitance value,
*       integrate the  capacitor current (wrt time) then divide by the  capacitor voltage
*       A series RC circuit is connected to pulse voltage source, which goes from 0V to 1V
*       after a 10us delay, with rise and fall times of 1ns. The equation for a
*       semiconductor capacitor's capacitance value is:
*
*               C = CJ*(L-NARROW)*(W-NARROW)+2*CJSW(L+W-2NARROW)
*       where,
*               CJ=1 F/sq.meter, L=20U, W=1U, NARROW=0, CJSW=0
*       This gives a capacitance value of 20pF (20E-12F).
*       The capacitor voltage should reach 90% of its maximum value, 1V, in
*               time = (3*R*C) + rise + delay
*                       time      time
*                  = (3 * 1E3 * 20E-12) + 1E-9 + 10E-6
*                  = 10.06us
*       Therefore, at 10.06us the capacitor voltage should be at least 0.9V.   Using the common
*        simulation data (csd) format for PSpice's Probe, the 20pF capacitance value can be
*        confirmed by dividing the integral of the capacitor current (vmon_branch) by the
*        capacitor voltage (V(3)).
********************************************************************************
VIN  1 0 PULSE(0 1 10U 1N 1N 30U)
R    1 2 1K
C    3 0 CMODEL L=20U W=1U
VMON 2 3 0
.MODEL CMODEL C (CJ=1)
.TRAN 1N 20U
.PRINT TRAN V(3)
.OPTION ACCT
.END
```

ChileSPICE Simulation Results for the Semiconductor Capacitor Circuit



3.1.36 Test Circuit for the Semiconductor Resistor

```
**********************************************************************************
* Tier No.:  1
* Directory/Circuit Name: SEMIC_RESISTOR/SEMIC_RESISTOR.cir
* Description:   Circuit netlist to test the validity of the  semiconductor resistor model.
* Input:  VIN
* Output: V(2), I(VMON)
* Analysis:
*       The circuit consists of a DC voltage source, VIN,  in parallel with a semiconductor
*       resistor, which has length, width and sheet resistance  defined such that the resistance
*       value is 1K ohm.    The equation for a semiconductor resistor is:
*               R = RSH*(L-NARROW)/(W-NARROW)
*       where,
*               RSH=1, L=1000U, W=1U, NARROW=0
*       VIN is swept from 0-5V in 1V increments.  The measured output is the
*       current through the resistor.  The resistance is calculated using Ohm's Law
*       where
*               Voltage=  Current * Resistance = I * R
*       or,     R=I/V
*       Therefore, for the given voltage and current values, R is:
*                       R(kOhm)|  I(mA)  |  V(Volts)
*                          0     |   0   |    0
*                          1     |   1     |    1
*                          1     |   2     |    2
*                          1     |   3     |    3
*                          1     |   4     |    4
*                          1     |   5     |    5
*
*       A zero volt source, VMON, is used as an ammeter to measure the current through R and
*       resistor voltage is measure at node 2, V(2).
**********************************************************************************
R1 2 0 RMOD L=1000U W=1U
VIN 1 0 5V
VMON 1 2 0V
.DC VIN 0 5V 1V
.MODEL RMOD R (RSH=1)
.PRINT DC V(2) I(VMON)
.OPTION  ACCT
.END
```

ChileSPICE Simulation Results for the SEMICONDUCTOR RESISTOR Circuit:

Semiconductor Resistor Circuit
DC transfer characteristic

Index	voltage_sweep VIN=V(1)	v(2)	vmon_branch I thru R1
0	0.000000E+00	0.000000E+00	0.000000E+00
1	1.000000E+00	1.000000E+00	1.000000E-03
2	2.000000E+00	2.000000E+00	2.000000E-03
3	3.000000E+00	3.000000E+00	3.000000E-03
4	4.000000E+00	4.000000E+00	4.000000E-03
5	5.000000E+00	5.000000E+00	5.000000E-03

3.1.37 Test Circuit for a the Transfer Function Analysis

```
**********************************************************************************
* Tier No.:     1
* Directory/Circuit Name:  TFANALY/tfanalysis.cir
* Description:  Test of  transfer function analysis using a simple BJT amplifier to find the small
*       signal voltage gain, input and output impedance.
* Input: VBB, VCC, VS
* Output:  V(2)/VS, Rin, Rout
* Analysis:
*       A simple bjt amplifer circuit is analyzed to determine the small signal transfer function
*       characteristics.  The voltage gain, input and output impedance, which are defined as:
*               Voltage Gain = Small Signal Input Voltage/Output Voltage
*                       =  Av = V(2)/VS
*                       = -(gm*RC)*(rpi / { rpi + RB})
*               Input Impedance = Rin = impedance as seen from the input source VS
*                       = RB + rpi
*               Output Impedance = Rout = impedance as seen the output voltage location
*                       or from the bjt collector to ground = RC
*       where,
*               gm = transconductance = ICQ/VT
*               ICQ = large signal quiescent collector current
*                   ={Beta * IB} = 100 * 10e-6 = 1mA
*               IBQ = large signal quiescent base current
*                   = (VBB - VBE(on)) / RB =  (1.2 - 0.7)/50E3 = 10uA
*               VT=thermal voltage = 26mV
*               gm = 1E-3 / 26E-3 = 38.46 mA/V
*       NOTE:           VBE, the base emitter turn on voltage is assumed to be 0.7V
*               BETA, the common emitter current gain, is 100*
*               rpi = diffusion resistance = Beta * VT / IC = (*00 * 26E-3) / (1E-3) = 2.6kOhms
*       Therefore, the expected results are as follows:
*               Av = V(2)/VS = -(gm/RC)*(rpi / { rpi + RB})
*                  = - (38.46E-3* 6E3) * (2.6E3 / {2.6E3 + 50E3}) = -11.4
*               Rin = RB + rpi = 50E3 + 2.6E3 = 52.6 kOhms
*               Rout = RC = 6 kOhms
* NOTE:  The value used for Vbe may not be the exact value used by the simulator since Vbe
*         is a calculated rather than user defined model parameter for a bjt transistor.
**********************************************************************************
VCC 1 0 DC 12V
VBB 5 0 DC 1.2V
VS  4 5 SIN(0 0.3V 1khz)
RC 1 2 6K
RB 3 4 50K
Q 2 3 0 NBJT
.MODEL NBJT NPN(IS=10FA BF=100)
.TF V(2) VS
.OPTIONS ACCT
.END
```

ChileSPICE Simulation Results for the Transfer Function Analysis Circuit:

Transfer function information:

GAIN = transfer_function = -1.14542e+01

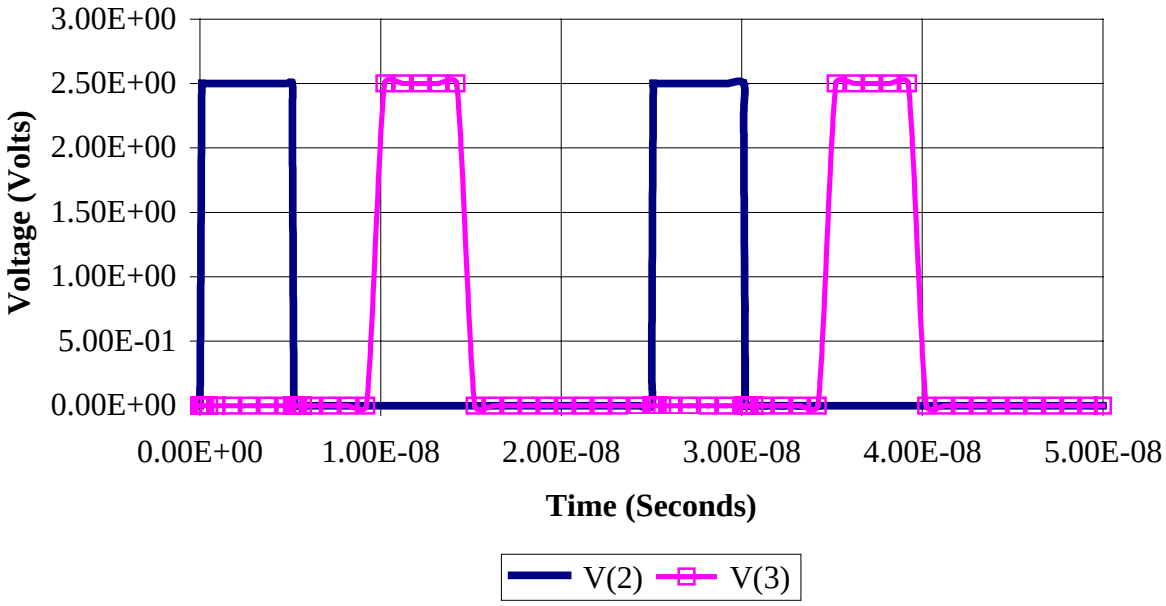
ROUT = output_impedance_at_v(2) = 5.999996e+03

RIN = vs_input_impedance = 5.238257e+04

3.1.38 Test of the Transmission Line Circuit

```
**********************************************************************************
* Tier No.:      1
* Directory/Circuit Name:  TRANSLINE/TRANSLINE.cir
* Description:  Test of Chilespice transmission line model using lossless circuit configuration.
* Input:  VIN
* Output:  V(2), V(3)
* Analysis:
*       The circuit contains a pulse voltage source (VIN), with a
*       50 ohm (RIN) output impedance, connected to a 50 ohm
*       transmission line (TLINE) which is terminated in a 50 ohm
*       (RL) matched load.  The pulse goes from 0V to 5V with no delay,
*       and has a pulse width of 25ns.  The transmission line has a
*       10ns delay. Any change in the input voltage, V(2), of TLINE
*       should occur 10N later at the output (node 3).
*       Therefore, the input voltage rises from 0V to 2.5V in 1ns and
*       remains at 2.5V for 5ns.  The output voltage V(3), does the
*       same as V(2) except that it is delayed by 10ns.
*       Note: V(2) is 2.5V due to the voltage drop across the 50 ohm
*       RIN resistor.
*
**********************************************************************************
VIN 1 0 PULSE(0 5 0 0.1N 0.1N 5N 25N)
RIN 1 2 50
TLINE 2 0 3 0 Z0=50 TD=10N
RL 3 0 50
.TRAN 0.25N 50N
.PRINT TRAN V(2) V(3)
.OPTION LIST ACCT
.END
```

ChileSPICE Simulation Results for the Transline Circuit



3.1.39 Test Circuit for the Voltage Controlled Current Source (VCCS)

```
**********************************************************************************
* Tier No.: 1
* Directory/Circuit Name:VCCS/vccs.cir
* Description: Test of ChileSPICE voltage controlled current source, VCCS, model using a
*       simple resistor circuit.  A DC operating point analysis is performed to obtain the transfer
*       function characteristics of the circuit (i.e., Rin, Rout, and voltage gain, Vout/Vin).
* Input:        VIN
* Output:  V(2), V(3), Rin, Rout, V(3)/V
* Analysis:
*       The VCCS, G,  is a function of the voltage, V(2), across R2 and is defined as
*               G = k*V=0.02*V(2).
*       The k must have the unit of conductance (1/ohms) to make k and V equal amps.
*       The voltage V(2) found by voltage division is
*               V(2) = VIN * R2/(R1 + R2) = 12*900/(1200) = 9V
*       The current through the dependent source, G, is
*               k*V(2) = 0.02 * 9V = 180mA
*       The current through the dependent source is divided evenly through resistors R3 and R4
*        (which are in parallel) giving 90mA through each resistor.  The 90mA currents go from
*       node 0 to node 3 (tail to tip), making the voltage at node 3
*               V(3) = -(R3*90mA) = -(200*90mA) = -18V
*       Additionally, Rin, Rout and the voltage gain are:
*               Rin  = R1 + R2 = 300 + 900 =1200 Ohms
*               Rout = R3||R4 = 200||200 =          100 Ohms
*               GAIN = V(3)/VIN = -18/12 =          -1.5
**********************************************************************************
VIN 1 0 DC 12V
G 3 0 2 0 0.02
R1 1 2 300
R2 2 0 900
R3 3 0 200
R4 3 0 200
.DC VIN 12 12 1
.PRINT DC V(2) V(3)
.OPTIONS  ACCT
.TF V(3) VIN
.END
```

ChileSPICE Simulation Results for the VCCS Circuit:

Voltage Controlled Current Source (VCCS)
DC transfer characteristic

Index	voltage_sweep VIN	v(2)	v(3)
0	1.200000E+01	9.000000E+00	-1.800000E+01

Transfer function information:
GAIN = transfer_function = -1.50000E+00
ROUT = output_impedance_at_v(3) = 1.000000E+02
RIN = vin_input_impedance = 1.200000E+03

3.1.40 Test Circuit for the Voltage-Controlled Voltage Source Circuit (VCVS)

```
**********************************************************************************
* Tier No.: 1
* Directory/Circuit Name: VCVS/vcvs.cir
* Description: Test of ChileSPICE voltage controlled voltage source model using a voltage
* amplifier circuit.  A DC operating  point analysis is performed to obtain the transfer function
* characteristics of the circuit (i.e., Rin, Rout, and voltage gain, Vout/Vin).
* Input:          VIN
* Output: V(2), V(3), V(4), Rin, Rout, V(4)/VIN
* Analysis:
* The VCVS, E, is controlled by the independent source, VIN, in the circuit and is defined as:
*                 E=V(3)=k*VIN=2*VIN = 2 * 10V = 20V
*         The factor k is an amplification value of 2.
*         The voltages at nodes 2 and 4 are
*                 V(2) = VIN * R2/(R1+R2)= 10 * 100K/(100K+250)=9.975V
*                 V(4) = V(3) * R4/(R3+R4)= 20 * 1K/(40+1K)=19.231V
*         Additionally, Rin, Rout and the voltage gain are
*                 Rin  = R1 + R2 = 100K + 250 =                   100.25K
*                 Rout = R3||R4 = 40||1K =                        38.46 Ohms
*                 GAIN = V(4)/VIN = 19.231/10 =                   1.923
**********************************************************************************
VIN 1 0 10V
E 3 0 1 0 2
R1 1 2 250
R2 2 0 100K
R3 3 4 40
R4 4 0 1K
.DC VIN 10 10 1
.PRINT DC V(2) V(3) V(4)
.OPTIONS ACCT
.TF V(4) VIN
.END
```

ChileSPICE Simulation Results for the VCVS Circuit:

Voltage-Controlled Voltage Source Circuit (VCVS)

DC transfer characteristic

Index	voltage_sweep VIN	v(2)	v(3)	v(4) VOUT
0	1.000000E+01	9.975062E+00	2.000000E+01	1.923077E+01

Transfer function information:

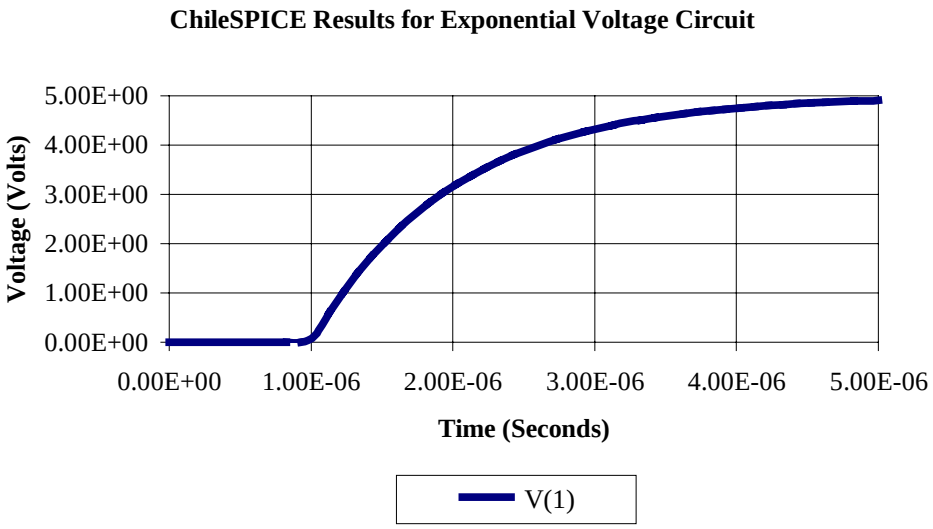
GAIN= transfer_function = 1.923077E+00

ROUT = output_impedance_at_v(4) = 3.846154E+01

RIN = vin_input_impedance = 1.002500E+05

3.1.41 Test Circuit for the Exponential Voltage Source

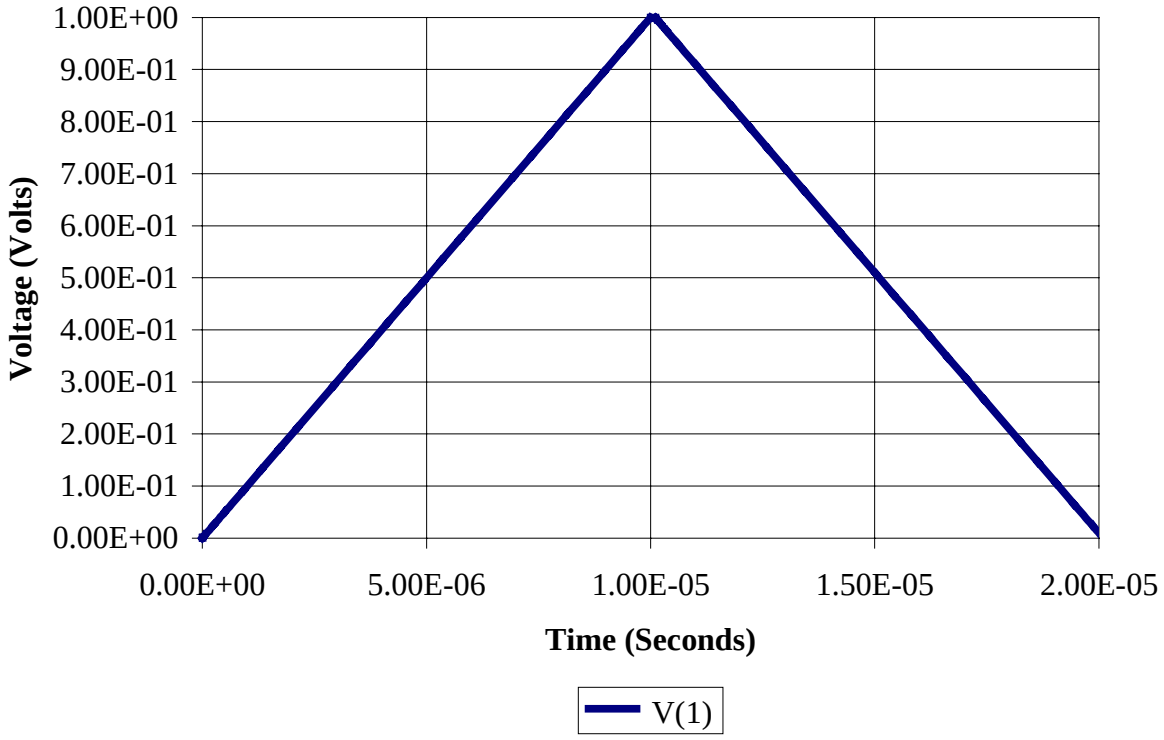
```
**********************************************************************************
* Tier No.: 1
* Directory/Circuit Name: VEXP/VEXP.cir
* Description: Test of the model for an exponential voltage source.
* Input: VEXP
* Output: V(1)
* Analysis:
*      The voltage source, VEXP or V(1),  is described as an  exponential time dependent voltage
*       signal that rises from 0 – 5V after a 1us delay time.  The rise time constant is 1us.  The
*       signal does not decay until after 1s.  Since the transient analysis is from 0 - 5us, the signal
*       will stay at 5V for the duration of the simulation.
*
*         The general format for an exp voltage source is
*                 EXP (V1  V2  TD1  TAU1  TD2  TAU2)
*         Where,
*         V1=initial value=0V   V2=pulsed value=5V  TD1=rise time delay=1us
*         TAU1=rise time constant=1us TD2=fall delay time=1s TAU2=final time constant=0
*
*         The voltage is described by the following equation:
*                 for  t between 0 and TD1
*                 VEXP=V1
*                 for t between TD1 and TD2
*                 VEXP = v(t)=V1 + (V2-V1)*(1-EXP(-(TIME-TD1)/TAU1))
*                 for t between TD2 and TSTOP
*                 VEXP=v(t) + (V1-V2)*(1-EXP(-(TIME-TD2)/TAU2))
*
*         Therefore for given values of time, the expected voltage is:
*                 T               VEXP(T)
*                 0               0
*                 1E-6            3.16
*                 2E-6            4.32
*                 3E-6            4.75
*                 4E-6            4.91
*                 5E-6            4.97
**********************************************************************************
VEXP 1 0 EXP(0V 5V 1US 1US 1S)
R 1 0 500
.TRAN 1US 5US
.OPTIONS ACCT
.PRINT TRAN V(1)
.END
```


ChileSPICE Results for Exponential Voltage Circuit
5.00E+00
4.00E+00
3.00E+00
2.00E+00
1.00E+00
0.00E+00
Voltage (Volts)
0.00E+00
1.00E-06
2.00E-06
3.00E-06
4.00E-06
5.00E-06
Time (Seconds)
V(1)

3.1.42 Test Circuit for the Pulse Voltage Source

```
**********************************************************************************
* Tier No.: 1
* Directory/Circuit Name: VPULSE/VPULSE.cir
* Description: Test of the pulse voltage source model
* Input: VPULSE
* Output: V(1)
* Analysis:
*       The voltage source, VPULSE or V(1), is described as  time dependent voltage signal that
*       generates a sawtooth waveform.  The signal rises linearly from 0V to 1V in 10us.  The
*       voltage remains at its peak value of 1V for 0.1us then decrease back to zero volts in 10us.
**********************************************************************************
VPULSE 1 0 PULSE(0V 1V 0S 10US 10US 0.1US 20.1US)
R 1 0 500
.TRAN 1US 20.1US
.OPTIONS  ACCT
.PRINT TRAN V(1)
.END
```

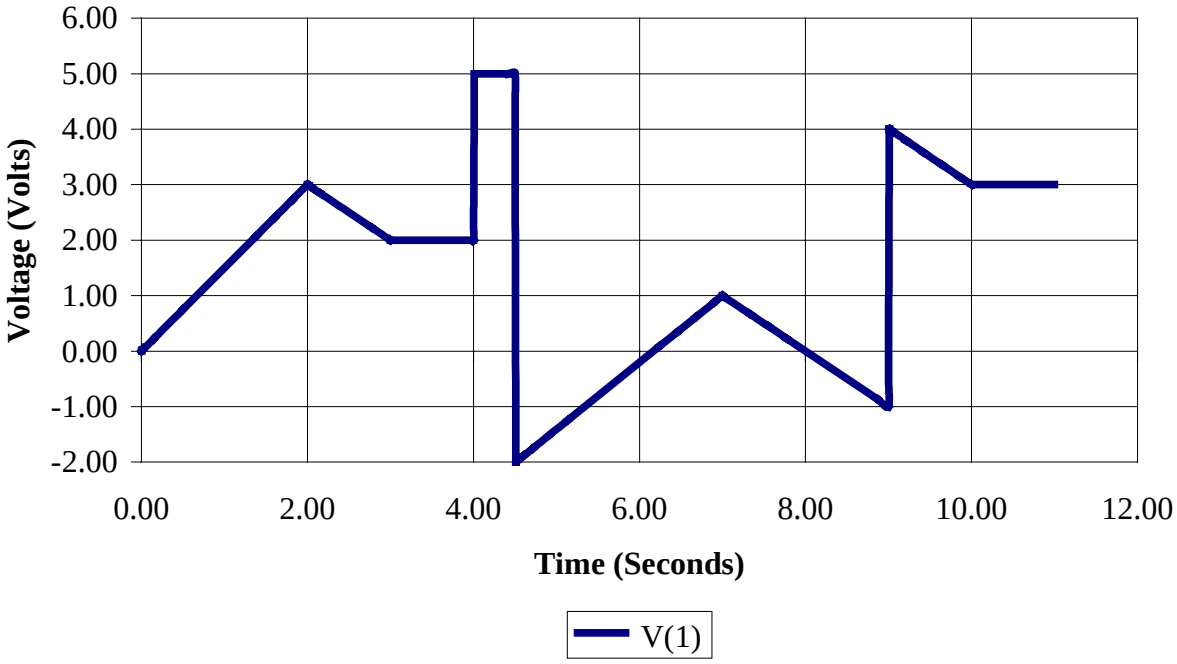
ChileSPICE Simulation Results for the Pulse Voltage Circuit



3.1.43 Test Circuit for the - Piece Wise Linear Voltage Source

```
**********************************************************************************
* Tier No.: 1
* Directory/Circuit Name: VPWL/VPWL.cir
* Description: Test of the piece-wise linear voltage source model
* Input: VPWl
* Output: V(1)
* Analysis:
*       The source, VPWL or V(1), is  as a piece wise linear voltage source which
*       is described by a series  of time and voltage  pairs of data points, given by:
*               index      time(s), voltage(volts)
*               1       (0.0 ,  0.0)
*               2       (2.0 ,  3.0)
*               3       (3.0 , 2.0)
*               4       (4.01 , 5.0)
*               5       (4.51 , -2.0)
*               6       (7.0 , 1.0)
*               7        (9.0 , -1.0)
*               8        (9.01 , 4.0)
*               9       (10.0 , 3.0)
*               10      (11.0, 3.0)
**********************************************************************************
 VPWL 1 0 PWL(0S 0V  2S 3V  3S 2V  4S 2V  4.01V 5V  4.5S 5V
+ 4.51S -2V  7S 1V  9S -1V  9.01S 4V  10S 3V)
R 1 0 500
.TRAN 1S 11S
.OPTIONS ACCT
.PRINT TRAN V(1)
.END
```

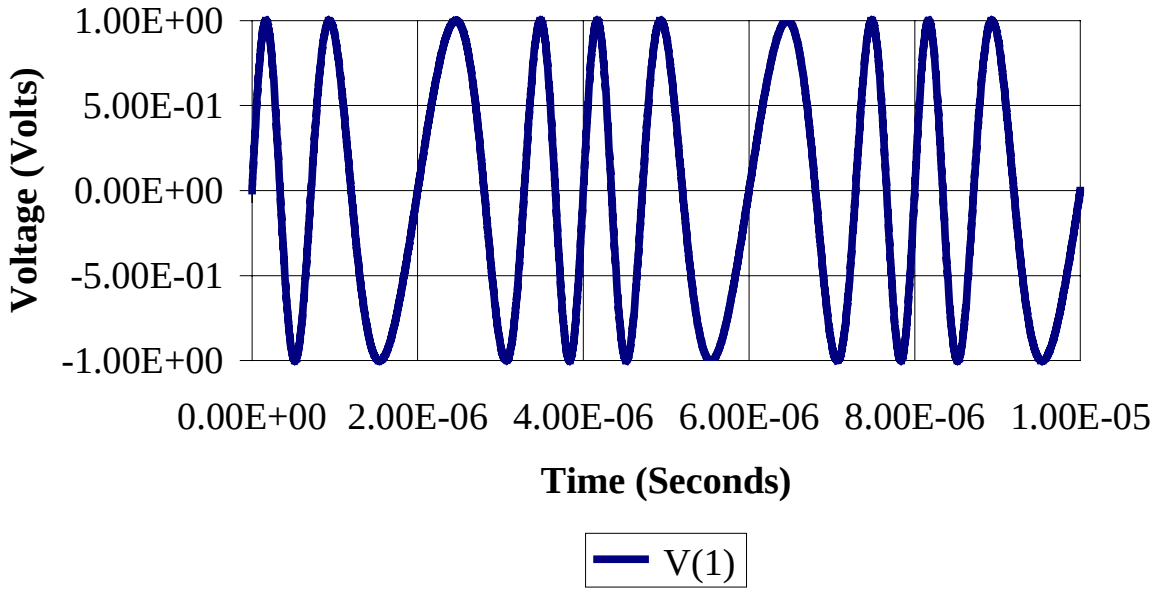
ChileSPICE Simulation Results for the Piece-Wise Linear Voltage Circuit



3.1.44 Test Circuit for the Voltage Single Frequency FM Source (VSFFM)

```
**********************************************************************************
* Tier No.: 1
* Directory/Circuit Name: VSFFM/vsffm.cir
* Description: Test of Chilespice model for a single-frequency frequency-modulated (SFFM)
*              transient voltage source.
* Input: VSFFM
* Output: V(1)
* Analysis:
*       A single frequency - frequency modulation signal that has no initial voltage and a peak
*       amplitude of 1V.  It has a carrier frequency of 1MEG Hz.  For the 10us transient analysis,
*       10 cycles of the carrier will be output in the 10us time. The carrier is modulated at a rate
*       determined by the single frequency (250KHz) and the modulation index (2).
*       The general format for a sffm transient function on a source statement is
*              SFFM (VO  VA  FC  MDI  FS)
*       where,
*              VO=offset voltage = 0V              VA=amplitude = 5V
*               FC=carrier frequency = 1MHz        MDI=modulation index = 2
*              FS=signal frequency = 250kHz
*       The current is described by the following equation:
*              VSFFM(t)= VO + VA*sin(2*pi*FC*t + MDI*sin(2*pi*FS*t))
*       Therefore, at the given values of time,  the voltage should be:
*
*       T              VSFFM(T)
*       0.0000E+00     0.0000E+00
*       1.0000E-04     4.9076E+00
*       2.0000E-04     1.4222E+00
*       3.0000E-04     1.4222E+00
*       4.0000E-04     4.9076E+00
*       5.0000E-04     2.1244E-06
*       6.0000E-04     -4.9076E+00
*       7.0000E-04     -1.4222E+00
*       8.0000E-04     -1.4222E+00
*       9.0000E-04     -4.9076E+00
*
**********************************************************************************
VSFFM 1 0 SFFM(0 1 1MEG 2 250K)
R1 1 0 1
.TRAN 1US 10US 0 0.01US
.PRINT TRAN V(1)
.OPTIONS LIST ACCT
.END
```

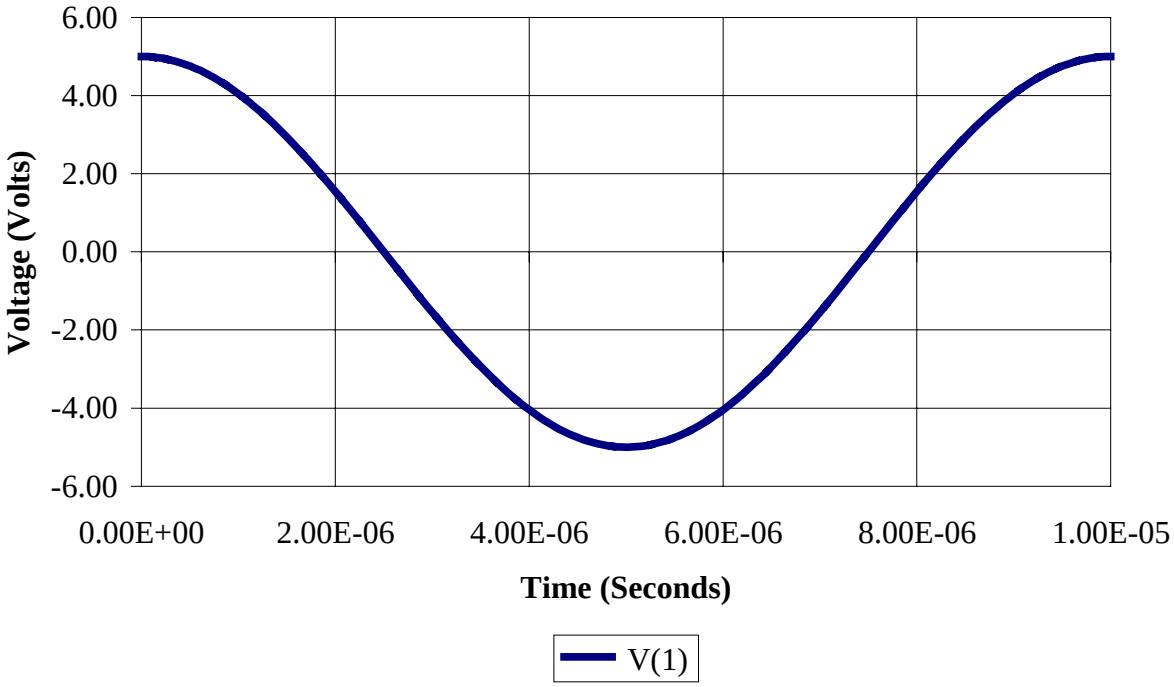
ChileSPICE Simulation Results for the SFFM Voltage Circuit



3.1.45 Test Circuit for the Sinusoidal Voltage Source

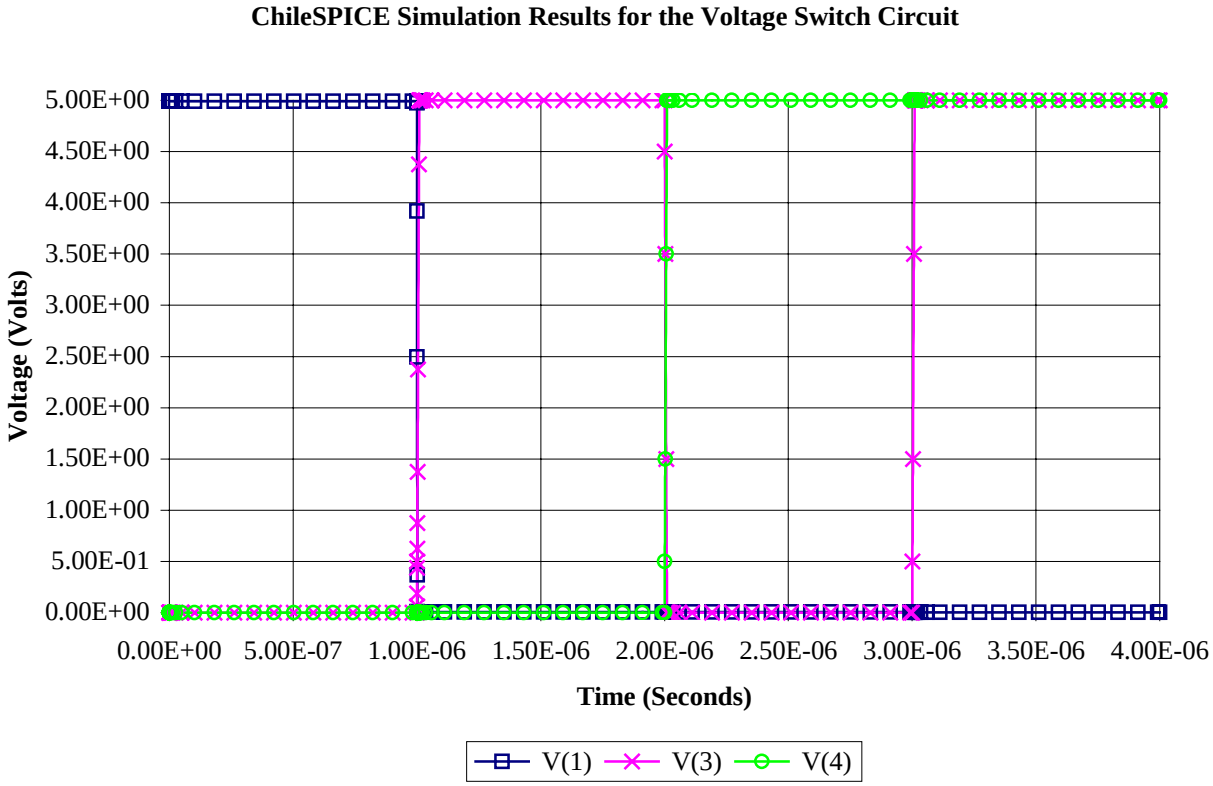
```
**********************************************************************************
* Tier No.:      1
* Directory/Circuit Name: VSIN/VSIN.cir
* Description: Test of the model for an independent sinusoidal voltage source.
* Input: VCOS
* Output: V(1)
* Analysis:
*       The voltage source is described as a sinusoidal time dependent voltage signal that
*       implements a cosine signal by specifying a negative delay equal to 2.5us, or a quarter of
*       the period specified by the 10us in the transient analysis statement.  The signal has a 5V
*       peak value with a100kHz frequency,  or 10us period.
*       The general format for the sinusoidal function in the voltage source is
*               SIN(VO VA FREQ TD THETA)
*       where,
*               VO=offset current = 0A                  VA=amplitude = 5A
*               FREQ=frequency = 100kHz   TD=time delay= -2.5us
*               THETA=damping factor = 0
*       The voltage  is described by the following equation for time > TD:
*               VSIN(t)= VO + VA*sin(2*pi*FREQ*(t –TD))*exp(-THETA(t-TD)
*       Therefore, at given values of time, the voltage should be:
*               T(seconds)      Voltage(T)
*               0.00E+00        5
*               2.00E-06        1.545084972
*               4.00E-06        -4.045084972
*               6.00E-06        -4.045084972
*               8.00E-06        1.545084972
*               1.00E-05        5
**********************************************************************************
VCOS 1 0 SIN(0 5 100K -2.5U)
R 1 0 500
.TRAN 1US 10US
.OPTIONS ACCT
.PRINT TRAN V(1)
.END
```

ChileSPICE Simulation Results for the Sinusoidal Voltage Circuit



3.1.46 Test Circuit for the Voltage Switch Implementation of a NOR Gate

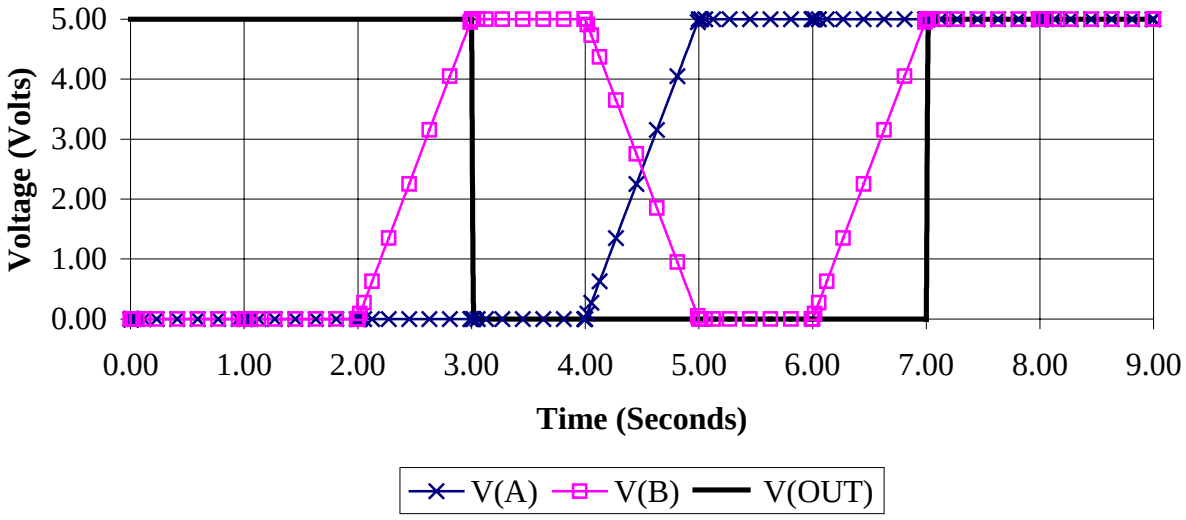
```
**********************************************************************************
* Tier No.: 1
* Directory/Circuit Name: VSWITCH/VSWITCH.cir
* Description: Test of  voltage controlled switch model.  The switch behaves like a resistor that
*       toggles between a very small on resistance, and a very large off resistance which depends
*       upon the controlling voltage.
* Input:  VCC, V3, V4
* Output: V(1), V(3), V(4)
* Analysis:
*               The circuit equivalent to the MOSFET implementation of a
*               NOR gate with the transistors replaced by two switches, S1 and S2,  and
*               a load resistance connected to 5V, VCC or V(2).  The controlling voltages
*               at nodes 3 and 4 represent the two inputs to the NOR gate,
*               which has the following logic table:
*                       InputA          InputB          Output
*                       ____________________________________
*
*                       0(Low)          0(Low)          1(High)
*                       0(Low)          1(High)         0(Low)
*                       1(High)         0(Low)          0(Low)
*                       1(High)         1(High)         0(Low)
*               The two input signals, V(3) and V(4),  are a sequence of logic 0 and 1 described
*               by two PWL voltage sources.  A transient analysis of the circuit from 0 to 4us
*               circuit from 0us to 4us yields the following expected output:
*                               0us     1us     2us     3us     4us
*
*       V(3)=InputA             0       5       0       5       5
*       V(4)=InputB             0       0       5       5       5
*       V(1)=Output             4.99    .005    .005    .025    .025
*Note: V(1)=0.005 and V(1)=0.025 are logic 0.
**********************************************************************************
RL 2 1 1K
S1 1 0 3 0 SW
S2 1 0 4 0 SW
VCC 2 0 5
V3 3 0 PWL (0 0 1U 0 1.01U 5 2U 5 2.01U 0 3U 0 3.01U 5)
R3 3 0 1
V4 4 0 PWL (0 0 2U 0 2.01U 5)
R4 4 0 1
.MODEL SW VSWITCH(RON=1 ROFF=1MEG VON=1 VOFF=0)
.TRAN 0.02U 4U
.PRINT TRAN V(1) V(3) V(4)
.OPTIONS ACCT
.END
```


ChileSPICE Simulation Results for the Voltage Switch Circuit
Voltage (Volts)
5.00E+00
4.50E+00
4.00E+00
3.50E+00
3.00E+00
2.50E+00
2.00E+00
1.50E+00
1.00E+00
5.00E-01
0.00E+00
0.00E+00
5.00E-07
1.00E-06
1.50E-06
2.00E-06
2.50E-06
3.00E-06
3.50E-06
4.00E-06
Time (Seconds)
V(1)
V(3)
V(4)

3.1.47 Test Circuit for the XNOR (Exclusive NOR) Gate

```
**********************************************************************************
* Tier No.:      1
* Directory/Circuit Name: XNOR/xnor.cir
* Description:  Test of the digital exclusive nor, XNOR,  gate used for defining logic circuits.
* Input: VA=V(A), VB=V(B)
* Output: V(A), V(B), V(OUT)
* Analysis:
*       Two piecewise linear  voltage sources, V(A) and V(B),  are used as logic inputs to an
*       XNOR gate, which is defined internal to the code as a  subcircuit .  Parameters are
*       defined in the netlist (by the .PARAMS statement) and passed into the XNOR subcircuit.
*       The subcircuit uses the parameters to establish the following values of the output voltage:
*       Rise Time = default_rise= rise/fall output voltage = 1ns
*       Margin = default_margin = margin which the output exceeds min/max logic levels=0.5V
*       High = default_high + default_margin = logic high voltage = 4.5V + 0.5V = 5V
*       Low = default_low - default_margin = logic low voltage = 0.5V - 0.5V = 0V
*       The logic for the exclusive nor gate is the output is high if and only if both inputs are low
*       or both inputs are high, for any other combination the output is low.  This truth table
*       shows the XNOR expected output for the given A and B time dependent inputs.
*
*       TIME        A(Volts)        B(Volts)        OUT(Volts)
*       0S          0               0               5
*       1S          0               0               5
*       2S          0               0               5
*       3S          0               5               0
*       4S          0               5               0
*       5S          5               0               0
*       6S          5               0               0
*       7S          5               5               5
*       8S          5               5               5
*       9S          5               5               5
*       NOTE: Low = 0V  High=5V
**********************************************************************************
* Set digital default parameters
.PARAM default_rise=1ns
.PARAM default_delay=0
.PARAM default_low=0.5V
.PARAM default_high=4.5V
.PARAM default_margin=0.5V
* Gate Inputs
VA A 0 0V PWL(0 0  1 0  2 0  3 0  4 0  5 5  6 5  7 5  8 5)
VB B 0 0V PWL(0 0  1 0  2 0  3 5  4 5  5 0  6 0  7 5  8 5)
X_XNOR A B OUT XNOR
.TRAN 1S 9S
.PRINT TRAN V(A) V(B) V(OUT)
.OPTIONS ACCT
.END
```

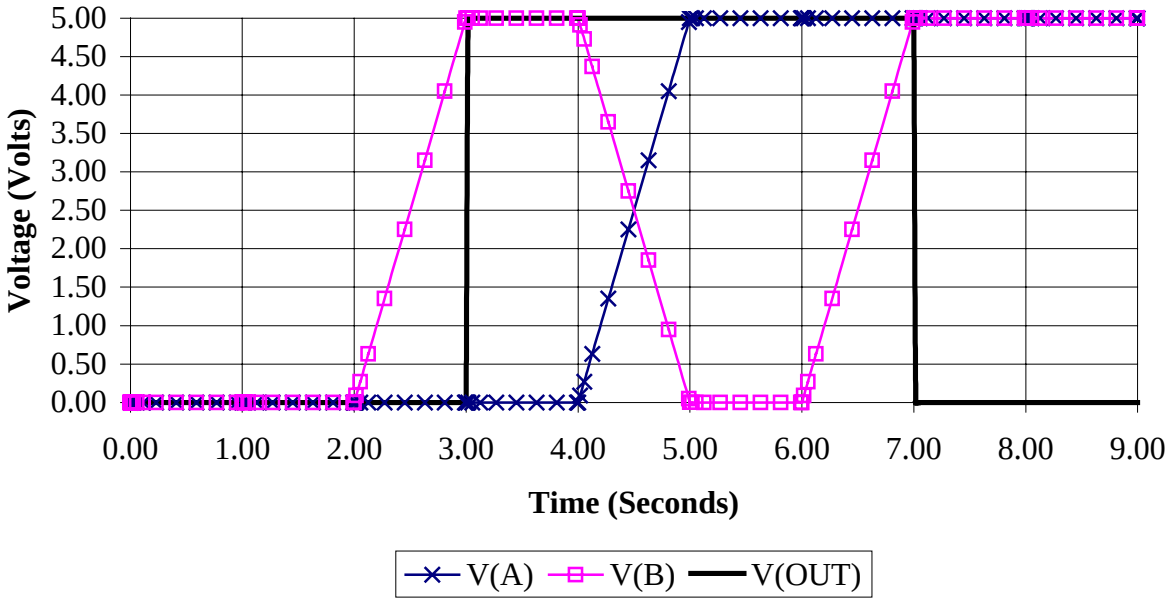
ChileSPICE Simulation Results For the XNOR Circuit



3.1.48 Test Circuit for the XOR (Exclusive Or) Gate

```
**********************************************************************************
* Tier No.:      1
* Directory/Circuit Name: XOR/xor.cir
* Description:  Test of the digital exclusive or, XOR, gate used for defining logic circuits.
* Input: VA=V(A), VB=V(B)
* Output: V(A), V(B), V(OUT)
* Analysis:
*        Two piecewise linear  voltage sources, V(A) and V(B),  are used as logic inputs to an
*        XOR gate, which is defined internal to the code by a subcircuit.  Parameters are defined
*        in the netlist (by the .PARAMS statement) and passed into the XOR subcircuit.  The
*        subcircuit uses the parameters to establish the following values of the output voltage:
*        Rise Time = default_rise= rise/fall output voltage = 1ns
*        Margin = default_margin = margin which the output exceeds min/max logic levels=0.5V
*        High = default_high + default_margin = logic high voltage = 4.5V + 0.5V  = 5V
*        Low = default_low - default_margin = logic low voltage = 0.5V - 0.5V = 0V
*        The logic for the exclusive or gate is the output is high if and only if one input is low and
*        one input is high; when both inputs are simultaneously high or low, the output is low.
*        This truth table shows the XOR expected output for the given A and B time dependent
*         inputs.
*        TIME          A(Volts)          B(Volts)          OUT(Volts)
*        0S            0                 0                 0
*        1S            0                 0                 0
*        2S            0                 0                 0
*        3S            0                 5                 5
*        4S            0                 5                 5
*        5S            5                 0                 5
*        6S            5                 0                 5
*        7S            5                 5                 0
*        8S            5                 5                 0
*        9S            5                 5                 0
*         NOTE: Low = 0V  High=5V
**********************************************************************************
* Set digital default parameters
.PARAM default_rise=1ns
.PARAM default_delay=0
.PARAM default_low=0.5V
.PARAM default_high=4.5V
.PARAM default_margin=0.5V
* Gate Inputs
VA A 0 0V PWL(0 0  1 0  2 0  3 0  4 0  5 5  6 5  7 5  8 5)
VB B 0 0V PWL(0 0  1 0  2 0  3 5  4 5  5 0  6 0  7 5  8 5)
X_XOR A B OUT XOR
.TRAN 1S 9S
.PRINT TRAN V(A) V(B) V(OUT)
.OPTIONS ACCT
.END
```

ChileSPICE Simulation Results for the XOR Gate Circuit



4 References

[ASCI V&V Guidelines] Martin Pilch, Timothy Trucano, Jamie Moya, Gary Froehlich, Ann Hodges, David Peercy (2000), “Guidelines for Sandia ASCI Verification and Validation Plans – Content and Format: Version 2.0”, Sandia National Laboratories, SAND2000-3101

[HPEMS/Xyce Test Plan] Regina L. Schells (June 2001), “HPEMS/Xyce Test Plan”

5 Distribution

EXTERNAL

Tonja Eaton
209 Pinecove Ave
Odenton, MD 2113

Ron Kielkowski
RCG Research, Inc
8605 Allisonville Rd, Suite 370
Indianapolis, In 46250

Mike Davis
Software Federation, Inc.
211 Highview Drive
Boulder, Co 80304

Wendland Beezhold
Idaho Accelerator Center
1500 Alvin Ricken Drive
Pocatello, Idaho 83201

Malcolm Panthaki
CoMeT Solutions, Inc
1601 Central NE
Albuquerque, NM 87106

INTERNAL

1	MS 0525	1734	P V Plunkett
1	MS 0525	1734	R B Heath
1	MS 0525	1734	M Deveney
1	MS 0525	1734	L Waters
1	MS 0525	1734	T Russo
5	MS 0525	1734	R Schells
2	MS 0525	1734	C W Bogdan
1	MS 0525	1734	J Marchiondo
1	MS 0525	1734	A Nunez
2	MS 0525	1734	S D Wix
1	MS 0525	1734	J Everts
1	MS 0525	1734	R Sikorski
1	MS 1071	1730	M Knoll
1	MS 1081	1762	F W Sexton
1	MS 1081	1762	P E Dodd
1	MS 1081	1762	S C Witczak

1	MS 1081	1739	C E Hembree
1	MS 0481	2114	W C Moffat
1	MS 0481	2114	D Thomas
1	MS 0533	2333	D R Weiss
1	MS 0533	2333	W H Schaedla
1	MS 0501	2338	M K Lau
1	MS 0501	2338	G R Laguna
1	MS 0537	2331	P A Molley
1	MS 0537	2331	A Muyshondt
1	MS 0537	2331	S Limary
1	MS 0537	2331	B Wampler
1	MS 0537	2331	B Rush
1	MS 1137	6536	A L Hodges
1	MS 1137	6536	G K Froehlick
1	MS 1137	6536	C M Williamson
1	MS 9202	8418	K D Marx
1	MS 9202	8418	S L Brandon
1	MS 9409	8732	W P Ballard
1	MS 0835	9140	J M McGlaun
1	MS 0835	9142	J S Peery
1	MS 0828	9133	M Pilch
1	MS 0819	9211	T G Trucano
1	MS 0316	9233	S S Dosanjh
1	MS 0316	9233	S A Hutchinson
1	MS 0316	9233	E R Keiter
1	MS 0316	9233	R J Hoekstra
1	MS 0316	9235	H D Hjmarson
1	MS 0638	12326	D E Peercy
1	MS 1110	9214	D E Womble
1	MS 1110	9214	D Day
1	MS 0807	9338	D Shirley
1	MS 9217	8950	T Kolda
1	MS 1194	1644	HC Harjes
1	MS 0537	2331	S L Robinson
1	MS 0986	2665	A Mittas
1	MS 0328	2612	W C Curtis III
1	MS 9018	8945-1	Central Technical Files
2	MS 0899	9616	Technical Library
1	MS 0612	9612	Review & Approval Desk For DOE/OSTI