

LA-UR-01-3355

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Submitted to:

<http://lib-www.lanl.gov/la-pubs/00818423.pdf>

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BEAM POSITION MONITORS FOR THE SNS LINAC *

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Abstract

The Spallation Neutron Source (SNS) linac accelerates 52-mA peak of pulsed H- particles to over 800 MeV. There are three types of accelerating structure in which the beam position must be measured: the drift-tube-linac (DTL); cavity-coupled-linac (CCL); and superconducting-linac (SCL)[1,2]. Beam with a 402.5-MHz structure is injected into a 402.5 MHz DTL, followed by 805-MHz CCL and SCL structures. The position monitor pickups are all of the shorted-microstrip type with apertures of 2.5-cm, 3-cm and 7.3-cm-dia. In all cases, we down convert signals from the beam position pickups to a 50-MHz intermediate frequency (IF) for processing. We use the sampled in-phase and quadrature-phase (I&Q) processing technique to obtain the amplitude and phase information of the IF signals. All of the electronics are PCI-based hardware installed in PC computers employing standard technologies. LabVIEW™ is used for all of the acquisition, processing, and serving of the data to ethernet, and hence, the control system. The design of this beam position system hardware is described herein.

1 INTRODUCTION

The SNS linac is composed of three types of accelerating structures following the injector and RFQ. These are the DTL, CCL and SCL cavities. In most cases there is insufficient room to provide all the diagnostics one would like, so beam position monitor (BPM) pickups are designed to provide both beam-position and beam-phase information. In the case of the DTL, the only available space for the BPMs is within the drift tubes themselves. The design of these pickups has been covered previously [3-5].

With the requirement that both beam position and phase be measured with the same pickup, we chose to utilize the digital in-phase and quadrature-phase measurement technique on down-converted lobe signals.

For the electronics platform we have selected standard PC systems due to their superior performance vs. price as well as the availability of standardized products. Including both hardware and software. We are building the processing electronics in a PCI card format, except the rf reference local oscillator and calibration multiplier sources.

2 BEAM POSITION MONITOR PICKUPS

Beam position monitors will be installed in ten drift tubes within the DTL structures. These BPMs have a 25-mm bore and 32-mm lobe length. Right angle SMA vacuum feedthroughs from Kaman are used in conjunction with a short flexible coaxial cable assembly to get the lobe signals up through the drift tube stem. A prototype BPM has been made, shown in Fig. 1, and the first production units are being fabricated now.



Figure 1: Prototype drift tube BPM. Vacuum connectors from Kaman will be used on the final BPMs.



Figure 2: Prototype CCL BPM.

The BPMs for the CCL and SCL structures are similar in design and utilize a Kaman SMA feedthrough mounted

*Work supported by the Office of Basic Energy Science, Office of Science of the US Dept. of Energy, and by Oak Ridge National Lab.

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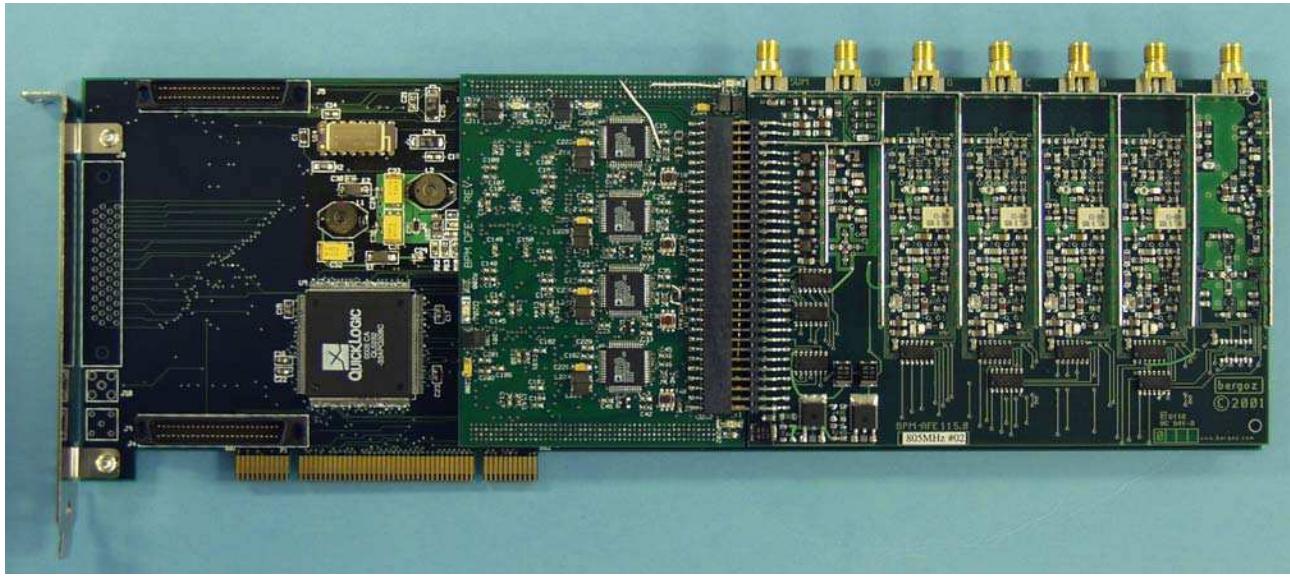


Figure 4: The prototype BPM electronics PCI card showing the motherboard, DFE (center) and AFE (right). The IP module site, where the timing module will be installed, is on the far left.

in a 1.33" Dia. Conflat vacuum flange like the RHIC BPMs used at BNL. These BPMs are being designed with collaboration from P. Cameron at BNL. A CCL prototype BPM is shown in Fig. 2.

The CCL BPMs have a 30-mm bore and a lobe length of 40 mm. The SCL BPMs are of the same type design with a 70-mm bore and 50-mm lobe length.

3 ELECTRONICS

Signals from the BPM pickups at either 402.5 MHz or 805 MHz (depending of location) will be down-converted to a 50-MHz IF for processing. The IF signals are sampled at 40 MHz to generate I and Q data used to calculate the their amplitude and phase (see Fig. 3).

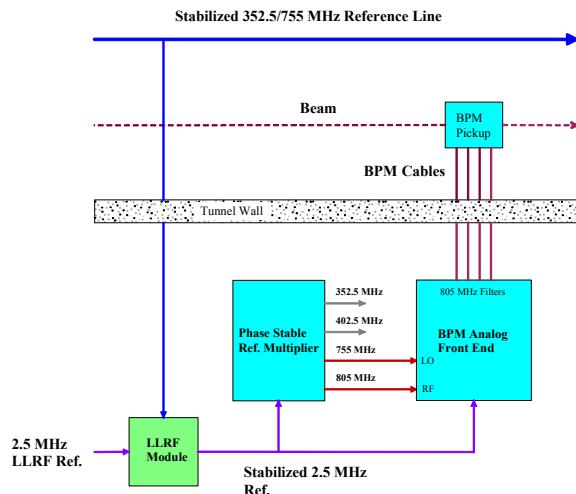


Figure 3: Block diagram of a single BPM system.

All linac frequencies are multiplied from a single precision 2.5-MHz source. The combination of the stabilized reference lines and low level rf (LLRF) system electronics provide a 2.5-MHz reference signal to all BPM electronics locations throughout the linac. At each BPM processing location the 2.5-MHz reference is multiplied up to the desired processing frequency and local oscillator (L.O.) frequency. Depending on location, this is either 402.5/352.5 MHz or 805/755 MHz. The MEBT and DTL BPMs process at 402.5 MHz while the CCL and SCL BPMs process at 805 MHz.

Each BPM processor is a PC-based, networked instrument, with a custom designed PCI card containing the analog and digital processing electronics. The PCI card has four basic parts: the PCI motherboard; the analog front end (AFE); the digital front end (DFE); and the timing IP module.

The AFE contains a four-channel down converter, switching networks for calibration-signal injection at the inputs, calibration signal distribution, L.O. signal distribution, and IF gain control. The prototype AFE was designed by Bergoz to meet LANL specifications.

The DFE samples the four IF signals from the AFE with 14-bit ADCs. Two gate arrays de-convolving the data streams from the four ADCs into eight separate I and Q data streams.

The PCI motherboard has eight large FIFO buffers into which the I and Q data from the DFE are continuously streamed. This data is DMA transferred into the host PCs memory for processing with standard software (LabVIEW). The PCI interface is built into a single gate array, which also contains the specialized functions to control the data acquisition, time-stamping, calibration control, etc.

In the SNS applications, accelerator timing information is provided to the PCI motherboard via a custom IP

module being provided by LBNL and BNL. Direct timing inputs may also be used, if desired.

4 PERFORMANCE STATUS

Testing of all prototype components of the PCI data acquisition are proceeding in parallel. Initial results of the PCI card are promising, with the PCI interface operational. Testing of the data acquisition functions is in progress. The DFE has been partially tested, and the AFE was received from Bergoz as of this writing.

Measurements by Bergoz indicate that the AFE meets the design parameters, though testing with the complete system is required [6]. The channel-to-channel isolation, a critical parameter, was measured to be at least 54 dB at 805 MHz, which is more than adequate for our design. This is without any special shielding covers.

The IF response of the AFE to a pulsed rf input is shown in Fig. 5, and seems to indicate that the transient response will be sufficiently settled in 150 ns to begin taking calibration data in the pulsed-calibration mode. The system is designed to inject a 300-ns-long rf pulse down each BPM cable which is reflected by the shorted end of the pickup lobe. The reflected signals amplitude and phase are measured and used to calibrate the amplitude and phase offset for each of the four input channels.

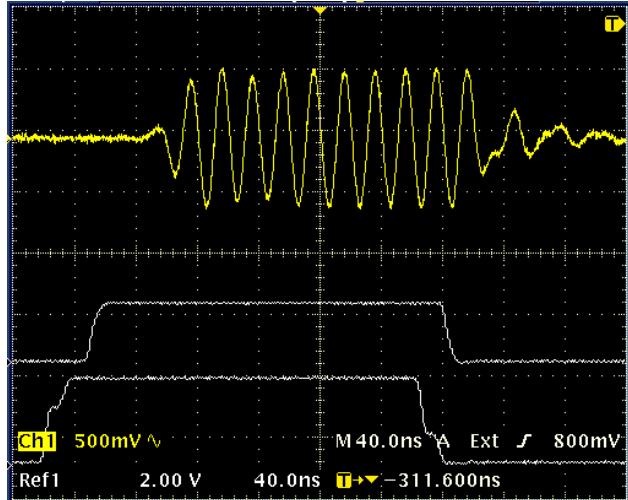


Figure 5: The measured transient response (top trace) of the AFE IF output to an 805-MHz burst at the input.

Simulations of the system to an rf burst indicate that 300-ns is an adequate amount of time to acquire the calibration data as shown in Fig. 6.

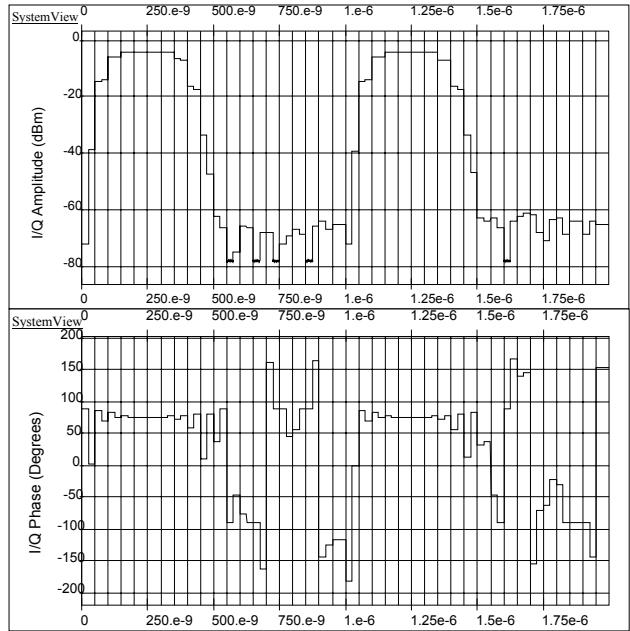


Figure 6: Simulation results of the BPM system to a 300-ns-long, pulsed-rf input as required during calibration. Good calibration data should be available in the period between 200 to 300 ns after the start of the pulse.

5 CONCLUSION

The design of the DTL and CCL BPM pickups is complete with the SCL pickups in progress. Initial testing of the BPM electronics has just begun and looks promising.

6 ACKNOWLEDGEMENTS

We would like to thank Julien Bergoz and Klaus Unser for providing test data for the BPM AFE.

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